



OPA462 高電圧(180V)、大電流(30mA)オペアンプ

1 特長

- 広い電源電圧範囲：
±6V (12V)～±90V (180V)
- 高出力負荷駆動： $I_O \pm 45\text{mA}$
- 電流制限保護
- 過熱保護機能
- ステータス・フラグ
- 独立した出力ディセーブル
- ゲイン帯域幅：6.5MHz
- スルーレート：32V/μs
- 広い温度範囲：-40°C～+85°C
- 8 ピン HSOIC (SO PowerPAD™) パッケージ

2 アプリケーション

- 半導体試験装置
- 光学モジュール
- 実験室およびフィールド用計測機器
- 半導体製造
- マルチパラメータ患者モニタ
- PC / ノート PC 向けディスプレイ・パネル

3 概要

OPA462 は高電圧 (180V)、大電流駆動 (45mA) のオペアンプです。このデバイスはユニティ・ゲイン安定であり、ゲイン帯域幅積は 6.5MHz です。

OPA462 は、過熱状態と電流過負荷に対して内部的に保護されています。±6V～±90V (または 12V～180V の単一電源) の広い電源範囲で動作するように仕様が規定されています。また、Status Flag ピンはオープンドレイン出力であるため、標準低電圧ロジック回路の入力に簡単に接続できます。この高電圧オペアンプは優れた精度と広い出力振幅を実現しており、類似のアンプでよくある位相反転の問題も生じません。

出力は、イネーブル / ディセーブル (E/D) ピンを使用してディセーブルできます。この E/D ピンには共通のリターン・ピンがあるため、低電圧のロジック回路と簡単に接続できます。このディセーブルは入力信号パスに影響を及ぼさずに行われ、電力の節約だけでなく負荷の保護にもなります。

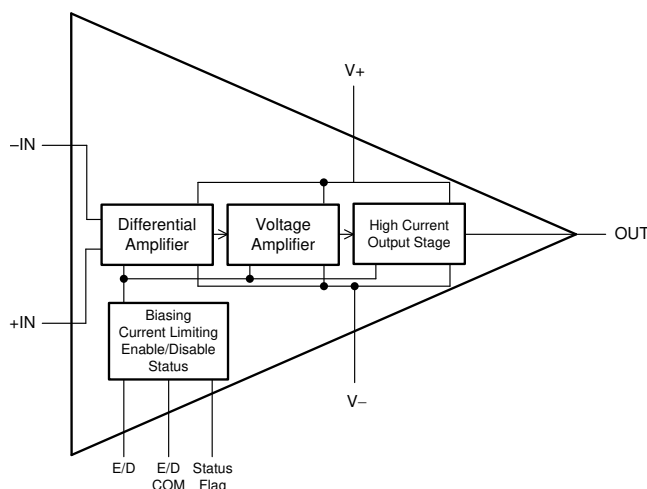
OPA462 は小型の露出メタル・パッド・パッケージを使用しているため、-40°C～+85°Cの産業用温度範囲で放熱を行います。

製品情報⁽¹⁾

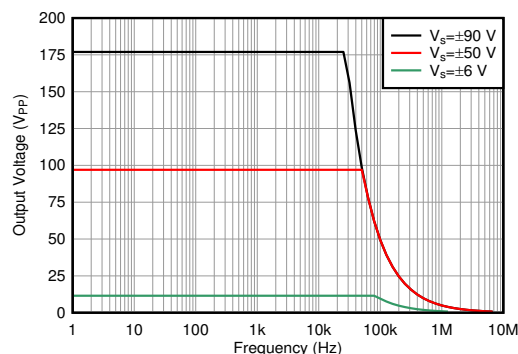
型番	パッケージ	本体サイズ(公称)
OPA462	HSOIC (8)	4.89mm×3.90mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

OPA462 ブロック図



最大出力電圧と周波数との関係



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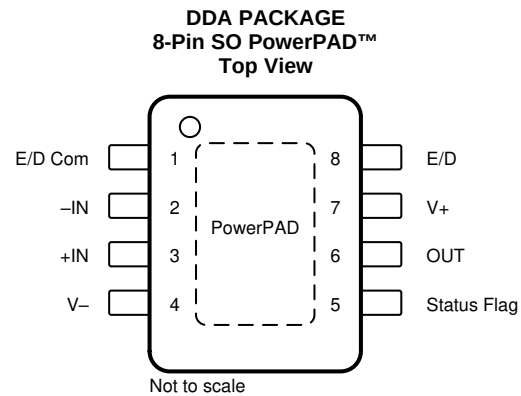
4 改訂履歴

2018年12月発行のものから更新

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•	OPA462 を事前情報 (プレビュー) から量産データ (アクティブ) に 変更	1
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5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
E/D	8	I	Enable or disable
E/D Com	1	I	Enable and disable common
-IN	2	I	Inverting input
+IN	3	I	Noninverting input
OUT	6	O	Output
Status Flag	5	O	Status Flag is an open-drain active-low output referenced to E/D Com. This pin goes active for either an overcurrent or overtemperature condition.
V-	4	—	Negative (lowest) power supply
V+	7	—	Positive (highest) power supply
PowerPAD	PowerPAD	—	The PowerPAD is internally connected to V-. The PowerPAD must be soldered to a printed-circuit board (PCB) connected to V-, even with applications that have low power dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _S	Supply voltage		190	V
+IN, –IN	Signal input pins ⁽²⁾	(V–) – 0.3	(V+) + 0.3	V
	E/D to E/D Com		7	V
	All input pins ⁽²⁾		±10	mA
	Output short circuit ⁽³⁾	Continuous	Continuous	
T _A	Operating	–55	125	°C
T _J	Junction		150	°C
T _{STG}	Storage	–55	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input terminals, Status Flag, E/D, and E/D Com, and Output are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 10 mA or less.
- (3) Short-circuit to ground.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _S	Supply voltage	±6		±90	V
T _A	Specified temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		OPA462	UNIT
		DDA (HSOIC)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	36.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	45.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	11.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	11.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	2.1	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 90\text{V}$, $R_L = 10\text{ k}\Omega$ to mid-supply, $V_{CM} = V_{OUT} = \text{mid-supply}$ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage		I _O = 0 mA		±0.2	±3.4	mV
dV _{OS} /dT	Input offset voltage drift		At T _A = −40°C to +85°C		±4	±20	μV/°C
PSRR	Power supply rejection ratio		V _S = ±6 V to ±90 V		0.03	0.3	μV/V
			V _S = ±6 V to ±90 V At T _A = −40°C to +85°C		0.3	1.5	μV/V
INPUT BIAS CURRENT							
I _B	Input bias current		V _S = ±50V		±30	±100	pA
			At T _A = −40°C to +85°C			±2.2	nA
I _{OS}	Input offset current				±30	±100	pA
			At T _A = −40°C to +85°C			±1.1	nA
NOISE							
e _n	Input voltage noise density		f = 1 kHz		33		nV/√Hz
			f = 10 kHz		23		nV/√Hz
	Input voltage noise		f = 0.1 Hz to 10 Hz		12.5		μV _{PP}
i _n	Current noise density		f = 1 kHz		40		fA/√Hz
			f = 10 kHz		450		fA/√Hz
INPUT VOLTAGE							
V _{CM}	Common-mode voltage		Linear operation	(V−) + 1		(V+) − 3	V
CMRR	Common-mode rejection	Common-mode rejection	−85 V ≤ V _{CM} ≤ 85 V	120	128		dB
CMRR	Common-mode rejection		−85 V ≤ V _{CM} ≤ 85 V At T _A = −40°C to +85°C	116	120		dB
INPUT IMPEDANCE							
	Differential				10 ¹³ 6		Ω pF
	Common-mode				10 ¹³ 3.5		Ω pF
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain		(V−) + 3 V < V _O < (V+) − 3 V	126	135		dB
			(V−) + 3 V < V _O < (V+) − 3 V At T _A = −40°C to +85°C	120	134		dB
			(V−) + 5 V < V _O < (V+) − 5 V, R _L = 5kΩ	126	135		dB
			(V−) + 5 V < V _O < (V+) − 5 V, R _L = 5kΩ At T _A = −40°C to +85°C	120	130		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product		Small-signal		6.5		MHz
SR	Slew rate		G = ±1 V/V, V _O = 80-V step, R _L = 3.27 kΩ		32		V/μs
	Full-power bandwidth				25		kHz
t _S	Settling time		To ±0.01%, G = ±5 V/V or ±10 V/V, V _O = 120-V step		5.2		μs
THD+N	Total harmonic distortion + noise		G = +10 V/V, f = 1 kHz, V _O = 150 V _{PP}		0.0009		%
			G = +10 V/V, f = 1 kHz, V _O = 150 V _{PP} , R _L = 5 kΩ		0.0012		%
			G = +20 V/V, f = 1 kHz, V _O = 150 V _{PP}		0.0015		%
			G = +20 V/V, f = 1 kHz, V _O = 150 V _{PP} , R _L = 5 kΩ		0.0025		%

Electrical Characteristics (continued)

 at $T_A = 25^\circ\text{C}$, $V_S = \pm 90\text{V}$, $R_L = 10\text{ k}\Omega$ to mid-supply, $V_{CM} = V_{OUT} = \text{mid-supply}$ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT							
	Overload recovery		G = −10 V/V	150			ns
V _O	Output voltage swing		R _L = 10 kΩ,	(V−) + 3		(V+) − 1.5	V
			R _L = 5 kΩ,	(V−) + 5		(V+) − 3	V
I _{SC}	Short-circuit current		V _S = ±45 V, At T _A = −40°C to +85°C	±45			mA
C _{LOAD}	Capacitive load drive			200			pF
Z _O	Open-loop output impedance		f = 1 MHz	90			Ω
	Output impedance		Output disabled	160			kΩ
	Output capacitance		Output disabled	36			pF
STATUS FLAG PIN (Referenced to E/D Com)							
	Status Flag delay		Enable → Disable, 10 kΩ pull-up to 5 V	3.5			μs
			Disable → Enable, 10 kΩ pull-up to 5V	11			μs
			Overcurrent delay, 10 kΩ pull-up to 5V	1			μs
			Overcurrent recovery delay, 10 kΩ pull-up to 5 V	9			μs
	Device thermal shutdown	Alarm (Status Flag high)		150			°C
		Return to normal operation (Status Flag low)		130			°C
	Status Flag output voltage		Normal operation	See typical curves			V
E/D (ENABLE/DISABLE) PIN							
V _{SD}	High (output enabled)		Pin open or forced high	E/D Com + 0.8		E/D Com + 5.5	V
	Low (output disabled)		Pin forced low	E/D Com		E/D Com + 0.35	V
	Output disable time			4			μs
	Output enable time			2.5			μs
E/D COM PIN							
	Pin voltage		V _S ≥ 106 V	(V−)		(V−) +100	V
			V _S < 106 V	(V−)		(V+) − 6	V
POWER SUPPLY							
I _Q	Quiescent current		I _O = 0 mA	3.2		3.7	mA
	Quiescent current in Shutdown mode		I _O = 0 mA, V _{E/D} = 0.65 V	1.5		2	mA

6.6 Typical Characteristics: Table of Graphs

表 1. Table of Graphs

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表 1. Table of Graphs (continued)

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6.7 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 90\text{ V}$, and $R_L = 10\text{ k}\Omega$ connected to GND, output enabled (unless otherwise noted)

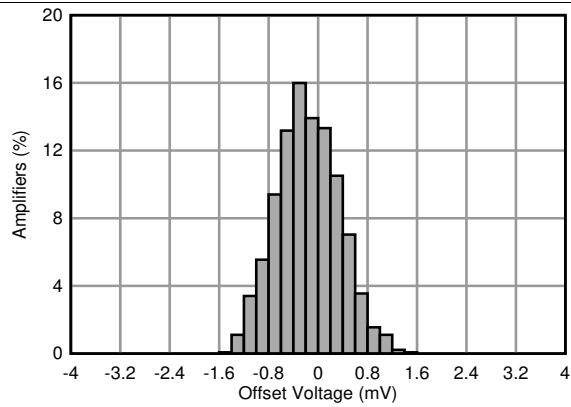


FIG 1. Offset Voltage Production Distribution at 25°C

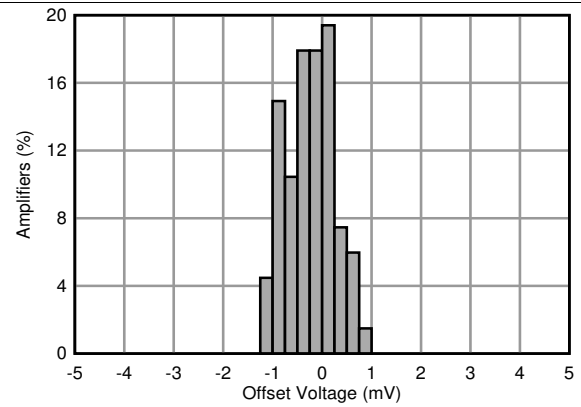


FIG 2. Offset Voltage Distribution at 85°C

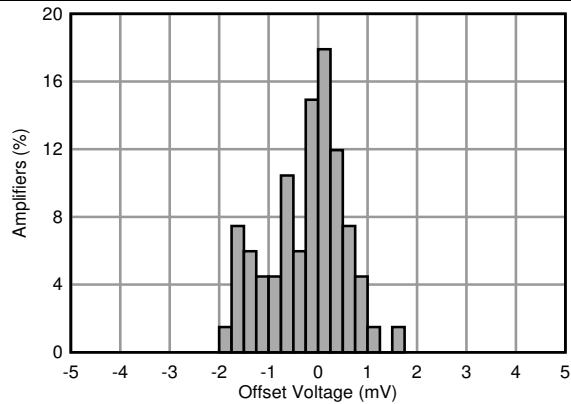


FIG 3. Offset Voltage Distribution at -40°C

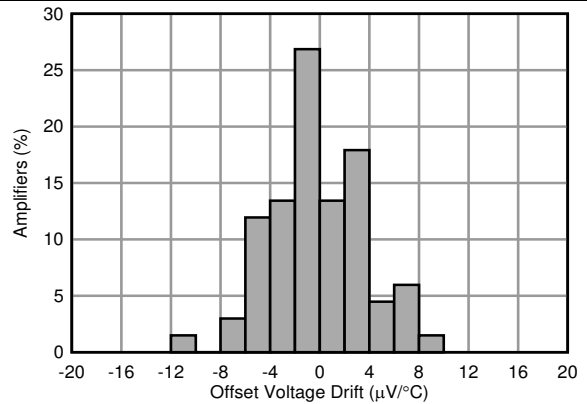


FIG 4. Offset Voltage Drift Distribution from -40°C to +85°C

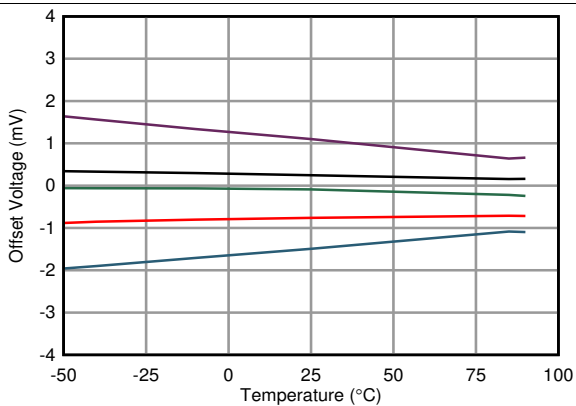


FIG 5. Offset Voltage vs Temperature

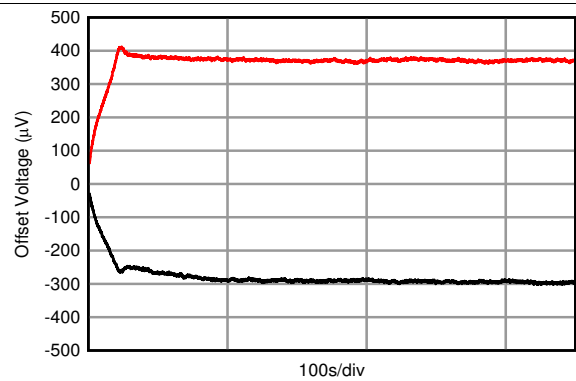


FIG 6. Offset Voltage Warmup

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 90\text{ V}$, and $R_L = 10\text{ k}\Omega$ connected to GND, output enabled (unless otherwise noted)

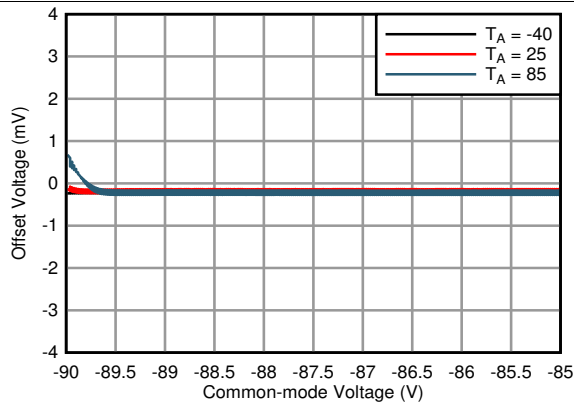


Figure 7. Offset Voltage vs Common-Mode Voltage (Low V_{CM})

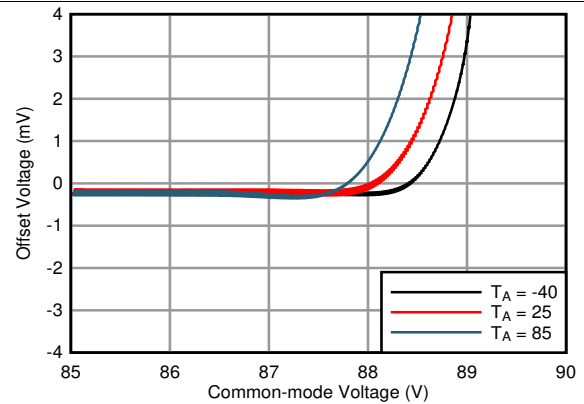


Figure 8. Offset Voltage vs Common-Mode Voltage (High V_{CM})

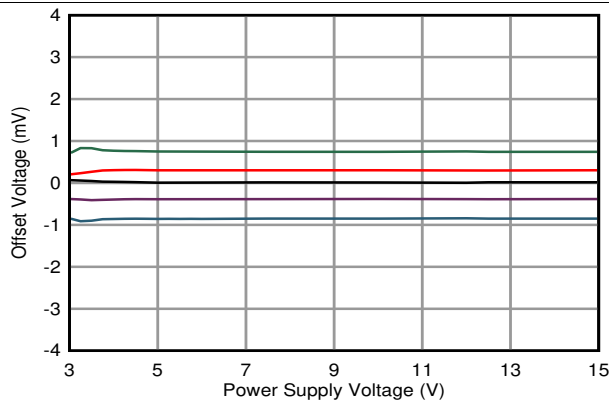


Figure 9. Offset Voltage vs Power Supply (Low Supply)

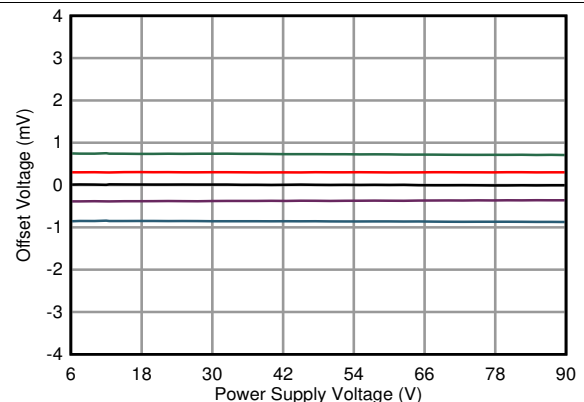


Figure 10. Offset Voltage vs Power Supply (High Supply)

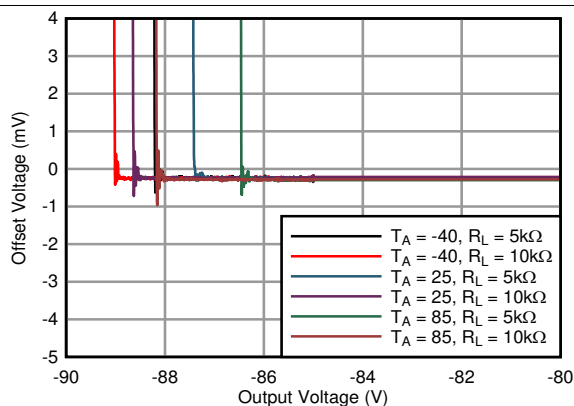


Figure 11. Offset Voltage vs Output Voltage (Low Output)

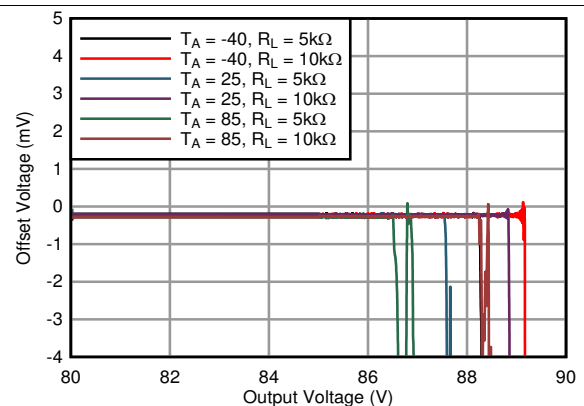


Figure 12. Offset Voltage vs Output Voltage (High Output)

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 90\text{ V}$, and $R_L = 10\text{ k}\Omega$ connected to GND, output enabled (unless otherwise noted)

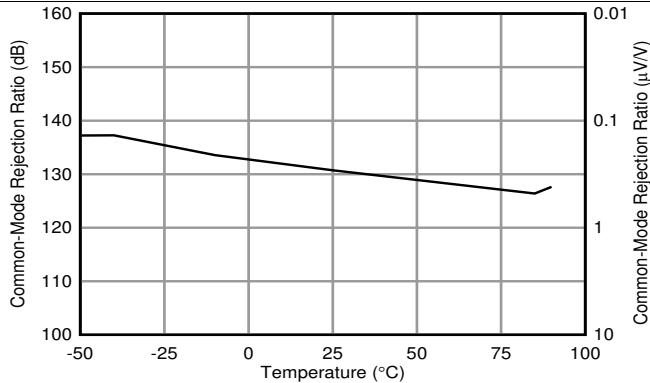


FIG 13. CMRR vs Temperature

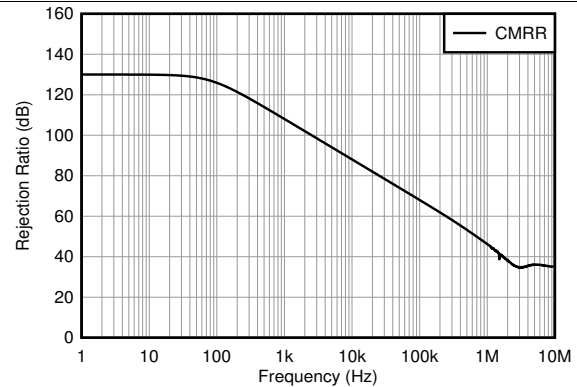


FIG 14. CMRR vs Frequency

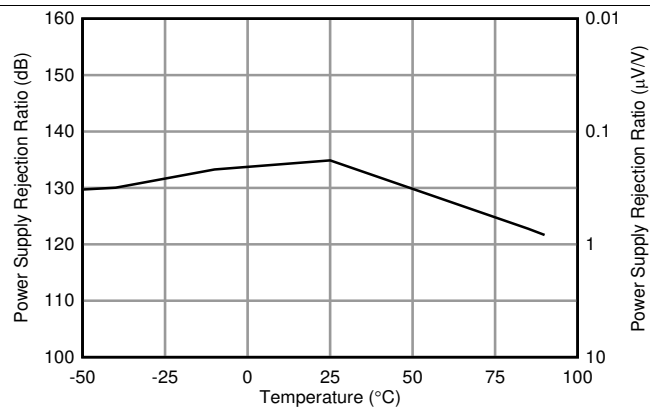


FIG 15. PSRR vs Temperature

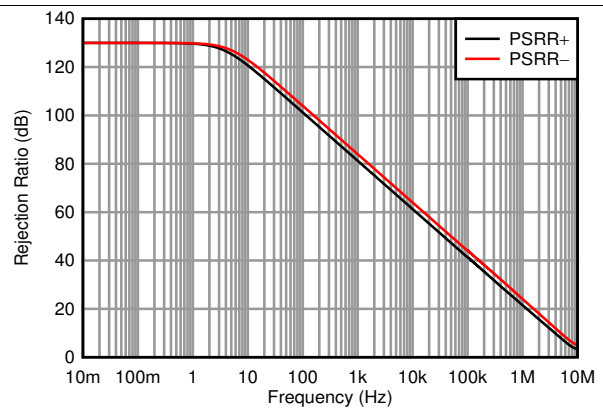


FIG 16. PSRR vs Frequency

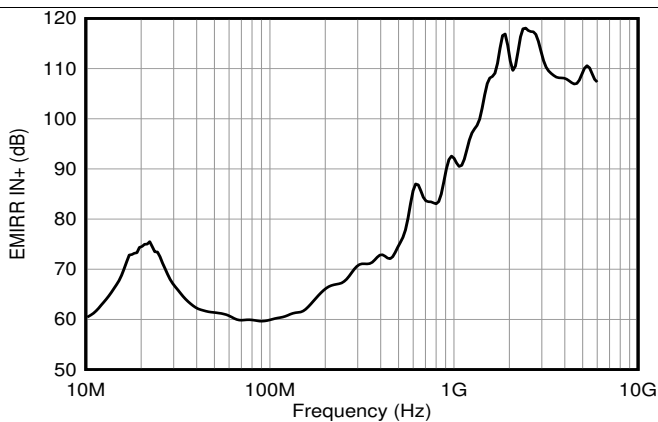


FIG 17. EMIRR vs Frequency

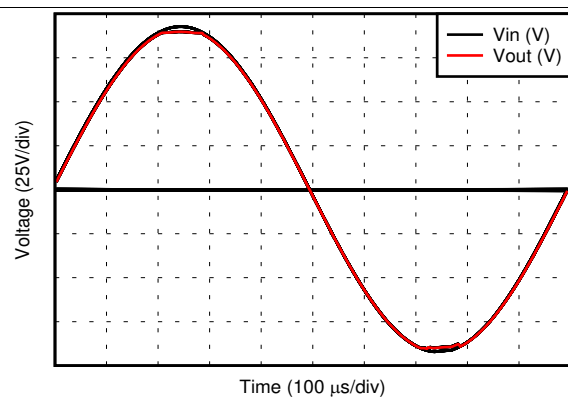


FIG 18. No Phase Reversal

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 90\text{ V}$, and $R_L = 10\text{ k}\Omega$ connected to GND, output enabled (unless otherwise noted)

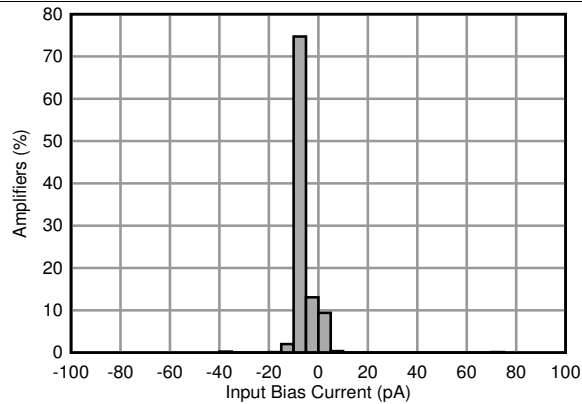


FIG 19. Input Bias Current Production Distribution at 25°C

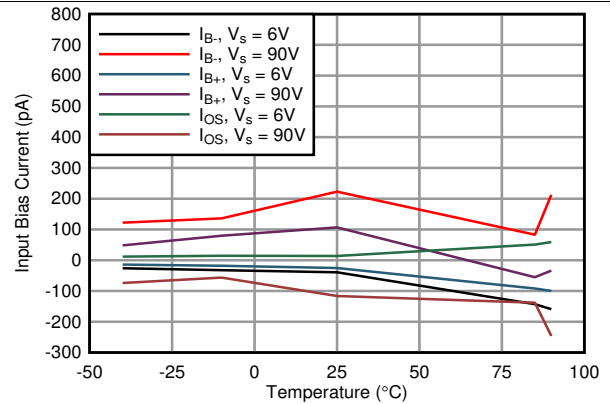


FIG 20. IB vs Temperature

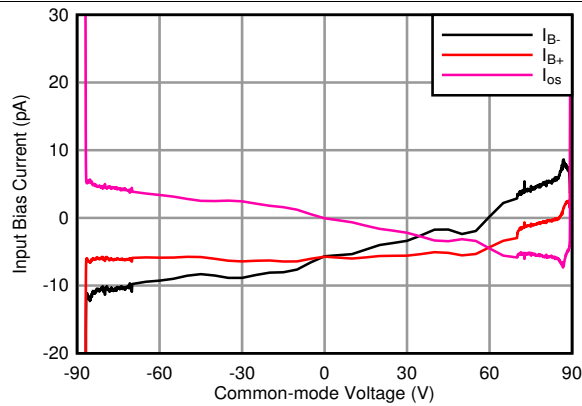


FIG 21. IB vs Common-Mode Voltage

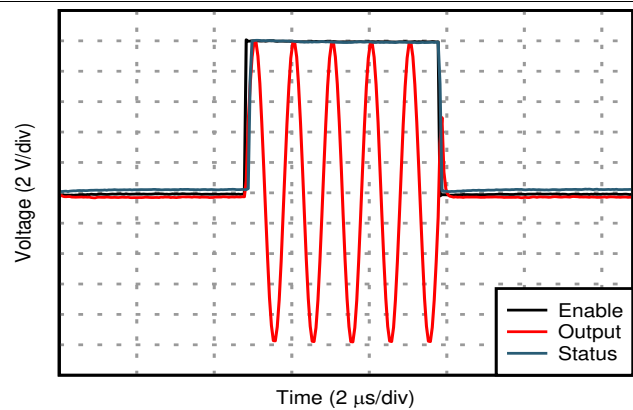


FIG 22. Enable Response

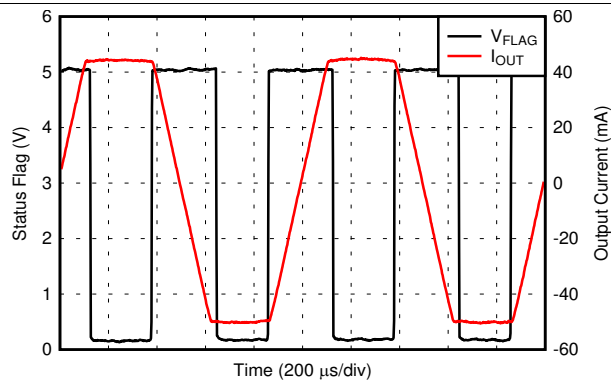


FIG 23. Current Limit Response

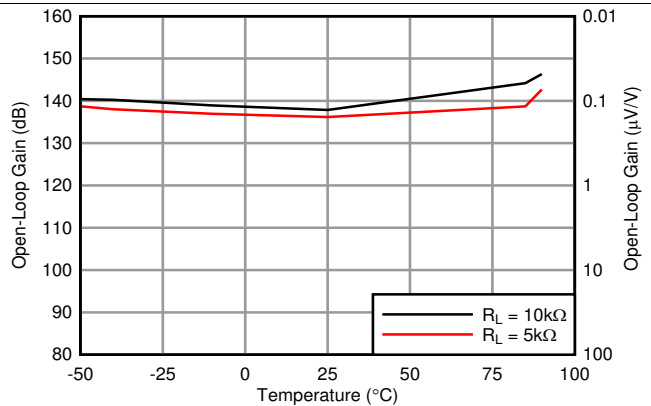
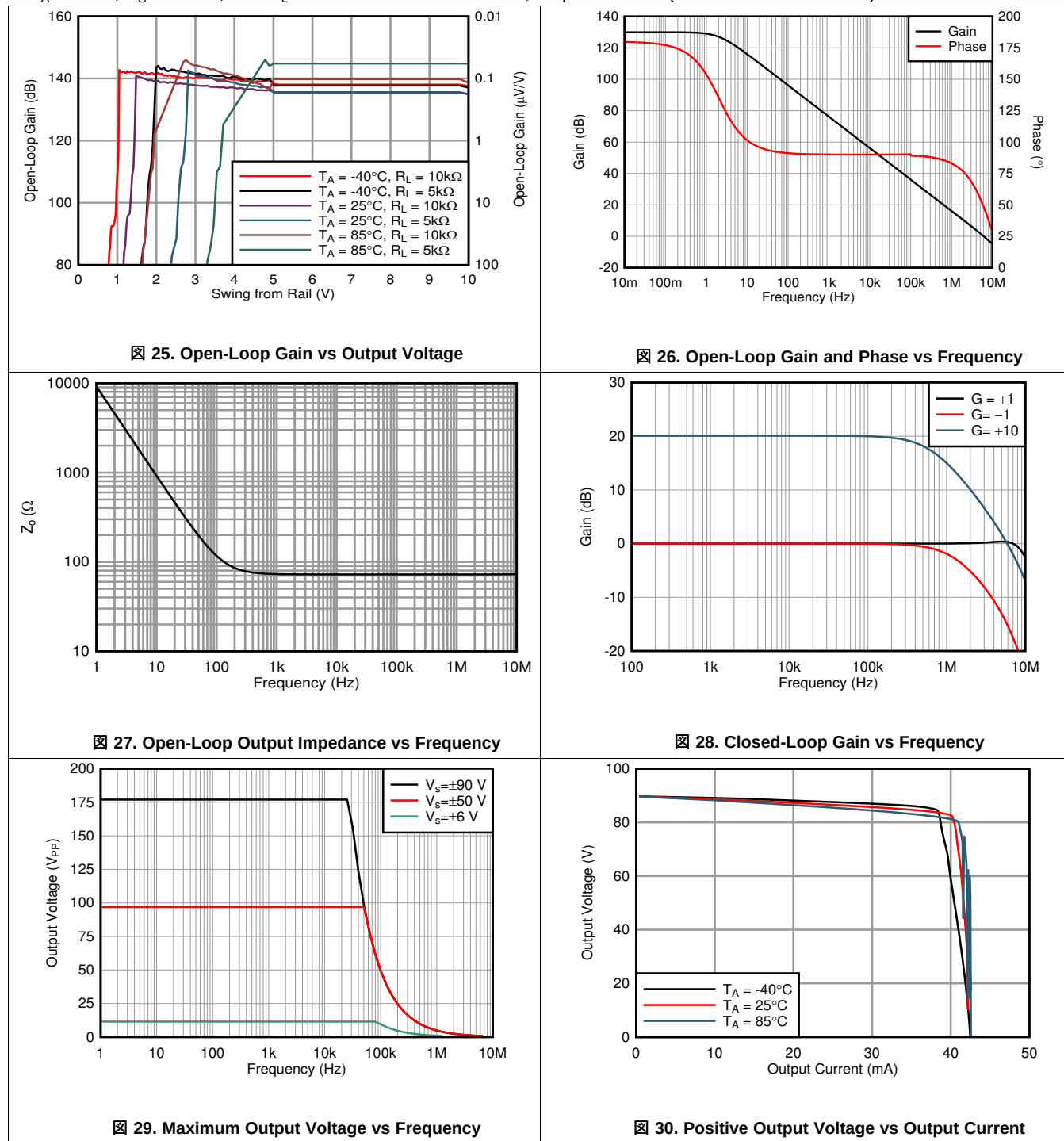


FIG 24. Open-Loop Gain vs Temperature

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 90\text{ V}$, and $R_L = 10\text{ k}\Omega$ connected to GND, output enabled (unless otherwise noted)



Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 90\text{ V}$, and $R_L = 10\text{ k}\Omega$ connected to GND, output enabled (unless otherwise noted)

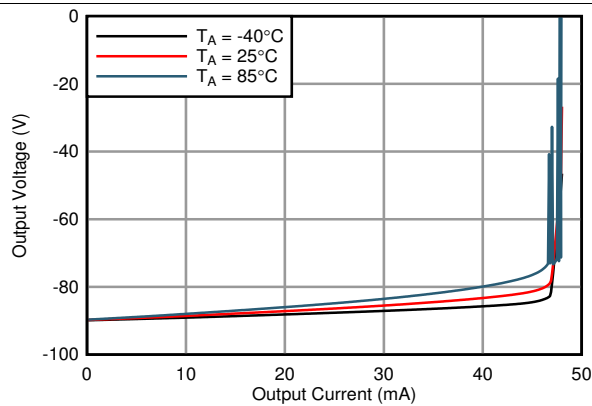


FIG 31. Negative Output Voltage vs Output Current

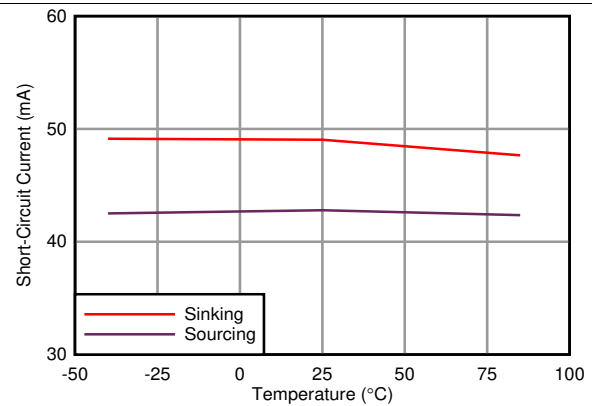


FIG 32. Short-Circuit Current vs Temperature

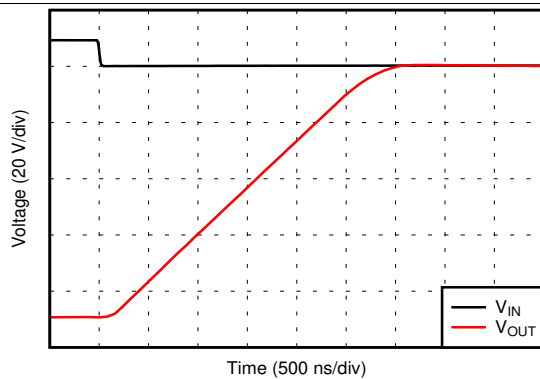


FIG 33. Negative Overload Recovery

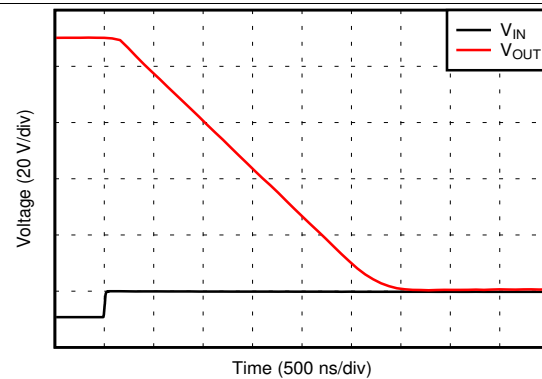


FIG 34. Positive Overload Recovery

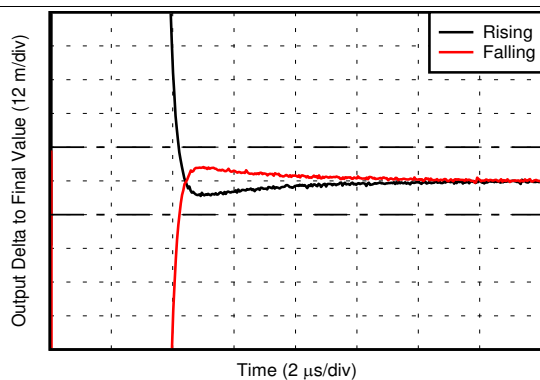


FIG 35. Settling Time

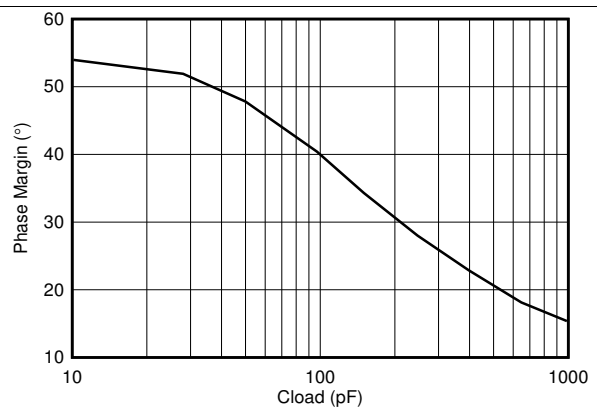


FIG 36. Phase Margin vs Capacitive Load

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 90\text{ V}$, and $R_L = 10\text{ k}\Omega$ connected to GND, output enabled (unless otherwise noted)

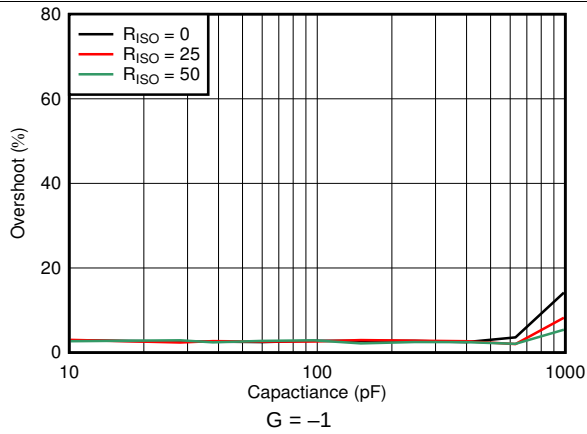


FIG 37. Small-Signal Overshoot vs Capacitive Load

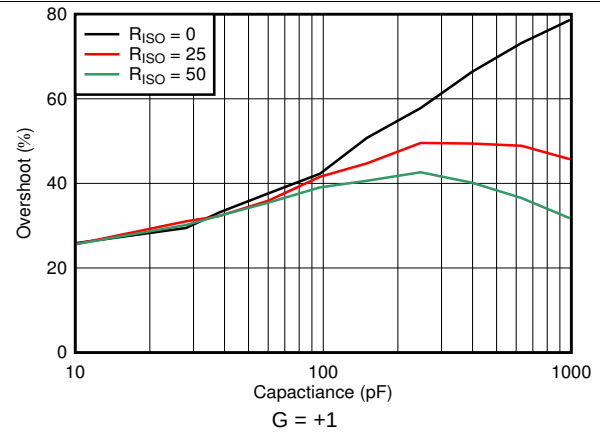


FIG 38. Small-Signal Overshoot vs Capacitive Load

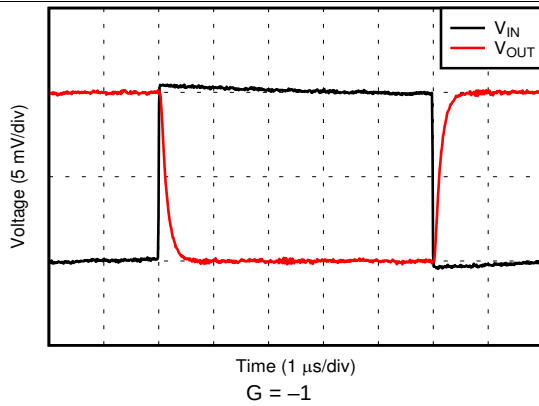


FIG 39. Small-Signal Step Response

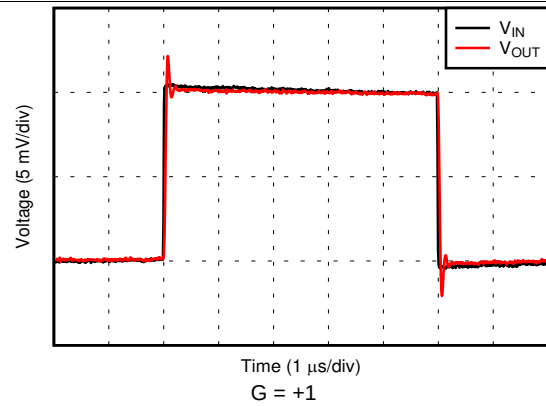


FIG 40. Small-Signal Step Response

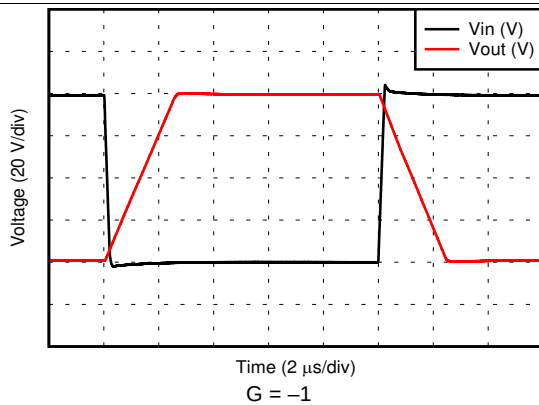


FIG 41. Large-Signal Step Response

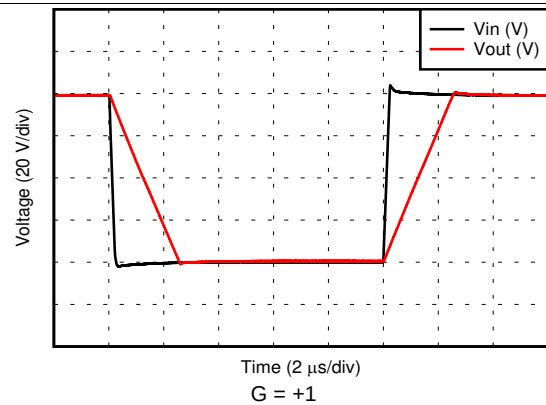


FIG 42. Large-Signal Step Response

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 90\text{ V}$, and $R_L = 10\text{ k}\Omega$ connected to GND, output enabled (unless otherwise noted)

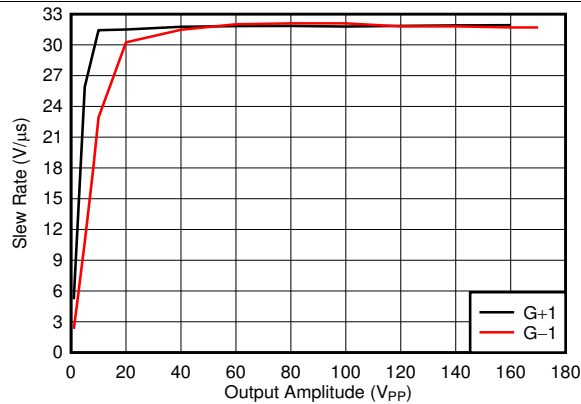


FIG 43. Slew Rate vs Output Step Size

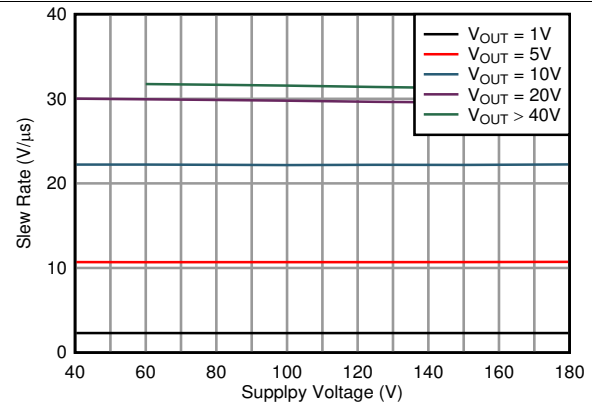


FIG 44. Slew Rate vs Supply Voltage (Inverting)

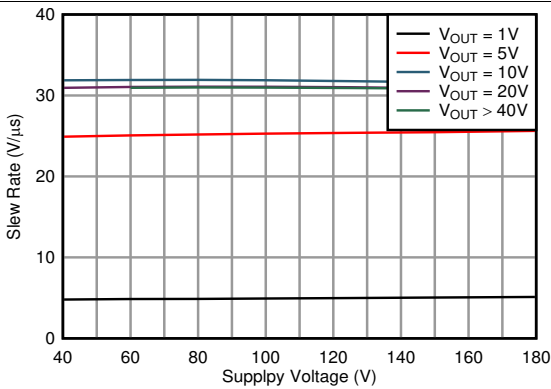


FIG 45. Slew Rate vs Supply Voltage (Noninverting)

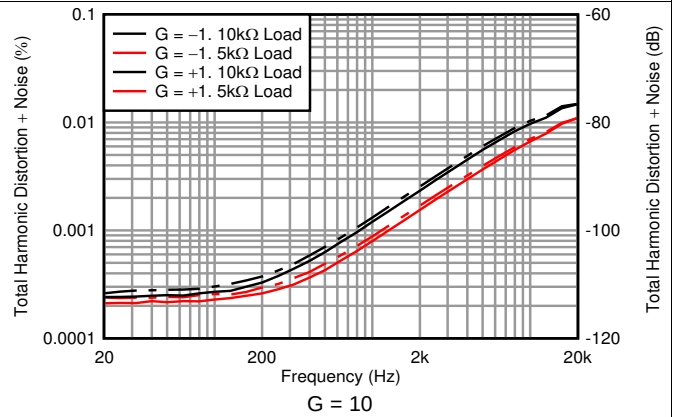


FIG 46. THD+N Ratio vs Frequency

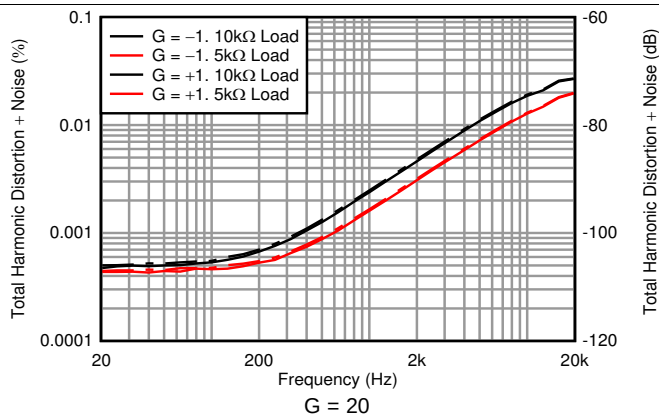


FIG 47. THD+N Ratio vs Frequency

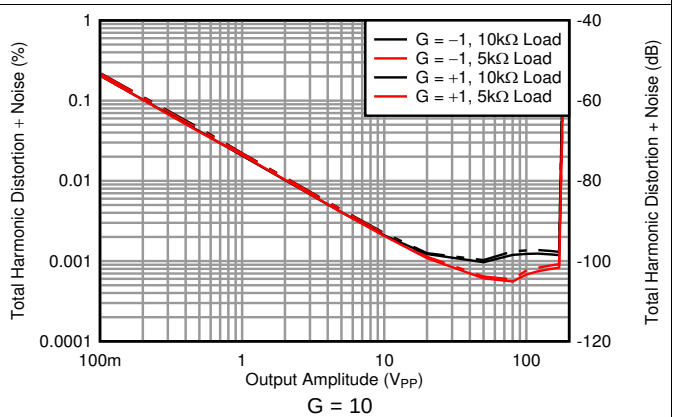
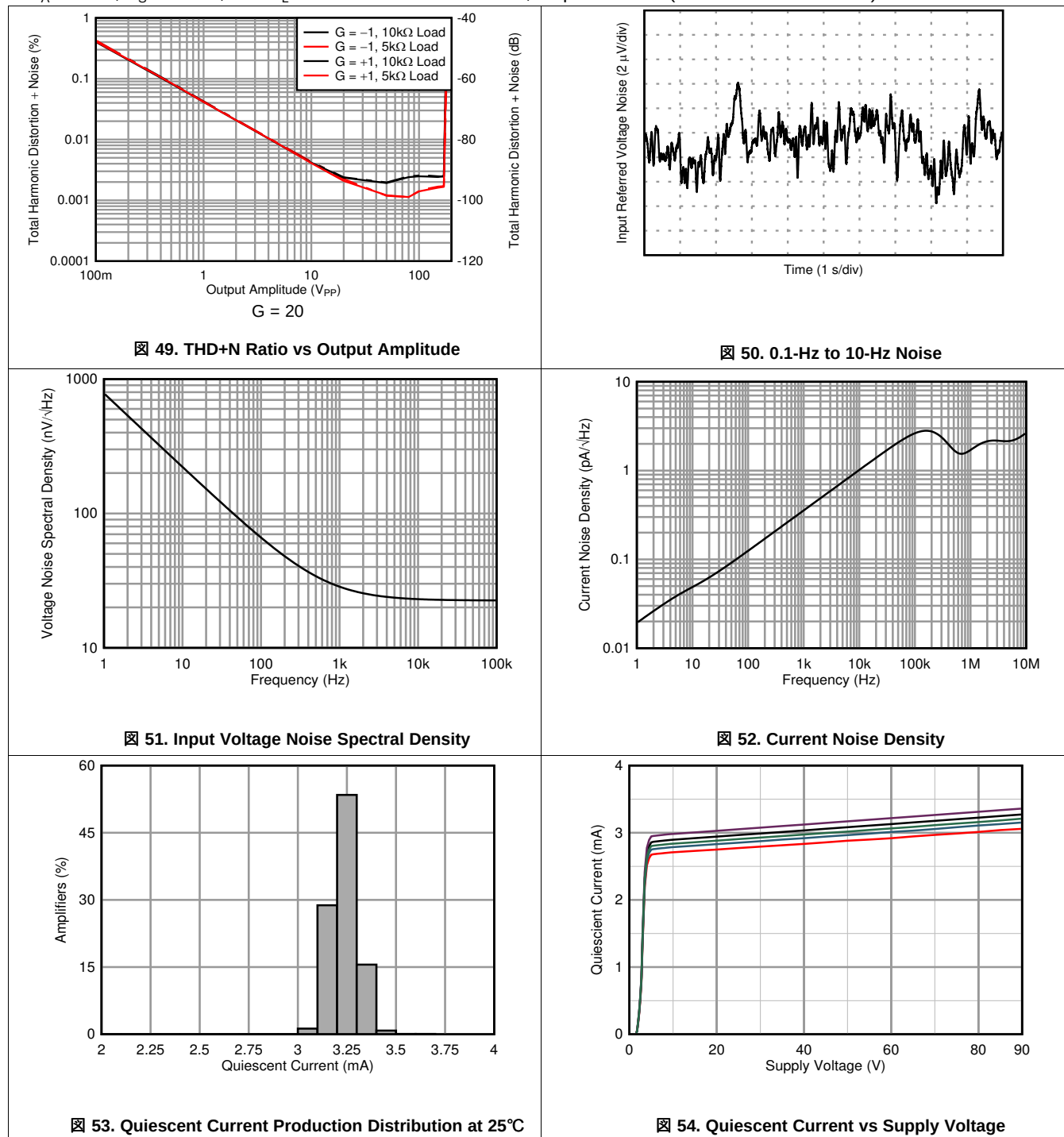


FIG 48. THD+N Ratio vs Output Amplitude

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 90\text{ V}$, and $R_L = 10\text{ k}\Omega$ connected to GND, output enabled (unless otherwise noted)



Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 90\text{ V}$, and $R_L = 10\text{ k}\Omega$ connected to GND, output enabled (unless otherwise noted)

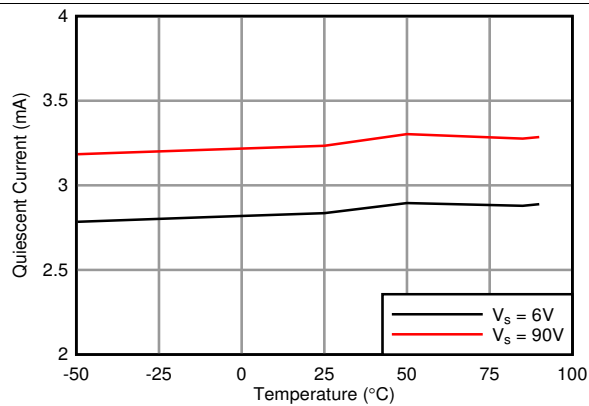


Figure 55. Quiescent Current vs Temperature

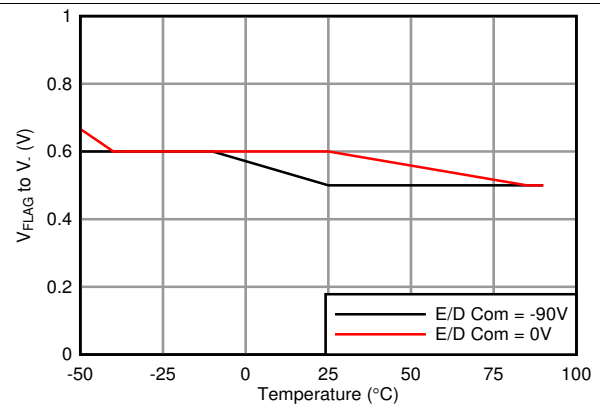


Figure 56. Status Flag Voltage vs Temperature

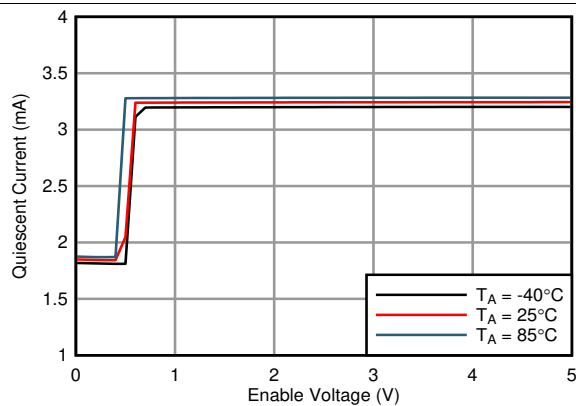


Figure 57. Quiescent Current vs Enable Voltage

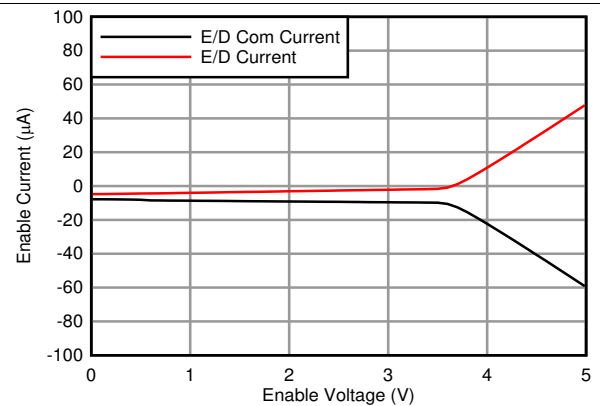


Figure 58. Enable Current vs Enable Voltage

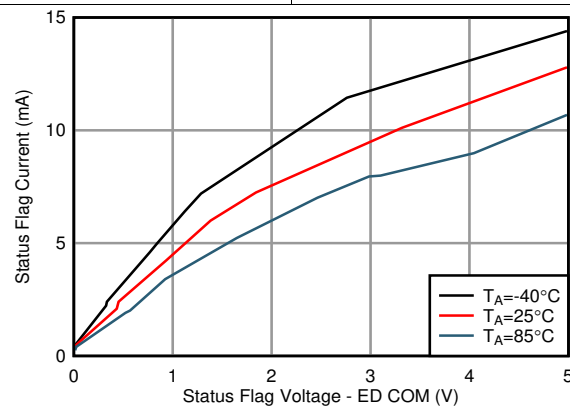


Figure 59. Status Flag Current vs Voltage

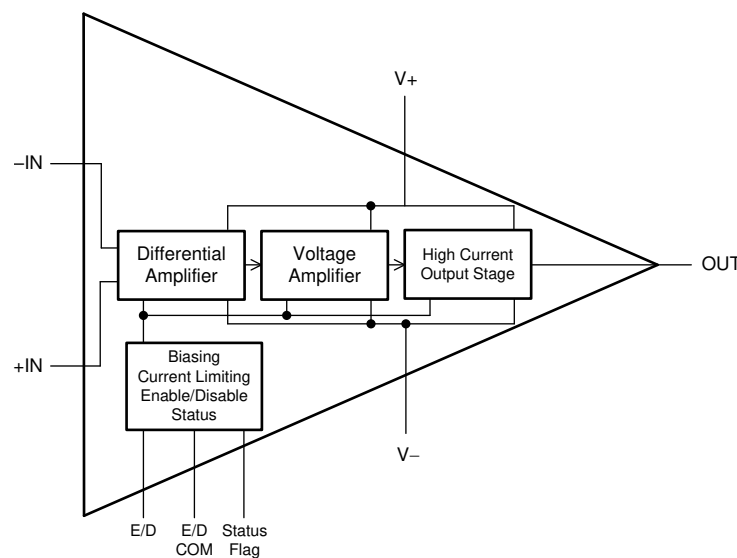
7 Detailed Description

7.1 Overview

The OPA462 is an operational amplifier (op amp) with high voltage of 180 V, and a high current drive of 30 mA. This device is unity-gain stable and features a gain-bandwidth product of 6.5 MHz. The high-voltage OPA462 offers excellent accuracy and wide output swing, and has no phase inversion problems that are typically found in similar op amps. The device can be applied in many common op amp configurations requiring a supply voltage range from ± 6 -V to ± 90 -V.

The OPA462 features an enable-disable function that provides the ability to turn off the output stage and reduce power consumption when not being used. The device also features a Status Flag pin that indicates an overtemperature or overcurrent fault conditions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Status Flag Pin

The Status Flag pin indicates fault conditions and can be used in conjunction with the enable-disable function to implement fault control loops. This pin is triggered when the device enters an overtemperature or overcurrent fault condition.

7.3.2 Thermal Protection

The OPA462 features internal thermal protection that is triggered when the junction temperature is greater than 150°C. When the protection circuit is triggered, thermal shutdown occurs to allow the junction to return a safe operating temperature. Thermal shutdown enables the Status Flag pin, which indicates the device has entered the thermal shutdown state.

7.3.3 Current Limit

Current limiting is accomplished by internally limiting the drive to the output transistors. The output can supply the limited current continuously, unless the die temperature rises to 150°C, which initiates thermal shutdown. With adequate heat dissipation, and use of the lowest possible supply voltage, the OPA462 can remain in current limit continuously without entering thermal shutdown. The best practice is to provide proper heat dissipation (either by a physical plate or by airflow) to remain well below the thermal shutdown threshold. For longest operational life of the device, keep the junction temperature below 125°C.

Feature Description (continued)

7.3.4 Enable and Disable

If left disconnected, E/D Com is pulled near V^- (negative supply) by an internal $10\text{-}\mu\text{A}$ current source. When left floating, E/D is held approximately 2 V above E/D Com by an internal $1\text{-}\mu\text{A}$ source. Even though active operation of the OPA462 results when the E/D and E/D Com pins are not connected, a moderately fast, negative-going signal capacitively coupled to the E/D pin can overpower the $1\text{-}\mu\text{A}$ pullup current and cause device shutdown. This behavior can appear as an oscillation and is encountered first near extreme cold temperatures. If the enable function is not used, a conservative approach is to connect E/D through a 30-pF capacitor to a low impedance source. Another alternative is the connection of an external current source from V^+ (positive supply) sufficient to hold the enable level above the shutdown threshold. [Figure 60](#) shows a circuit that connects E/D and E/D Com. The E/D Com pin is limited to $(V^-) + 100\text{ V}$ to enable the use of digital ground in an application where the OPA462 power supply is $\pm 90\text{ V}$.

When the E/D pin is dropped to a voltage between 0 V and 0.65 V above the E/D Com pin voltage the output of the OPA462 will become disabled. While in this state the impedance of the output increases to approximately $160\text{ k}\Omega$. Because the inputs are still active, an input signal might be passed to the output of the amplifier. The voltage at the amplifier output is reduced because of a drop across this output impedance, and may appear distorted compared to a normal operation output.

After the E/D pin voltage is raised to a voltage between 2.5 V and 5 V greater than the E/D Com, the output impedance returns to a normal state and the amplifier operates normally.

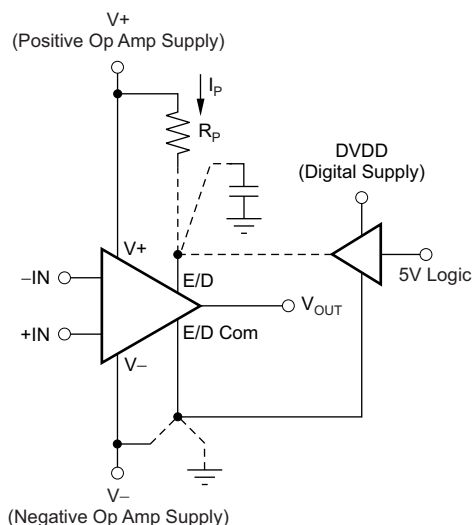


Figure 60. E/D and E/D Com

7.4 Device Functional Modes

A unique mode of the OPA462 is the output disable capability. This function conserves power during idle periods (quiescent current drops to approximately 1 mA). This disable is accomplished without disturbing the input signal path, not only saving power but also protecting the load. This feature makes disable useful for implementing external fault shutdown loops.

8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA462 is a high-voltage, high-current operational amplifier capable of operating with supply voltages as high as ± 90 V (180 V), or as low as ± 6 V (12 V). The high-voltage process and design of the OPA462 allows the device to be used in applications where most operational amplifiers cannot be applied, such as high-voltage power-supply conditions, or when there is a need for very a high-output voltage swing. The output is capable of delivering up to ± 30 mA output current, or swinging within a few volts of the supply rails at moderate current levels. The OPA462 features input overvoltage protection, output current limiting, thermal protection, a status flag, and enable-disable capability.

8.2 Typical Applications

8.2.1 High DAC Gain Stage for Semiconductor Test Equipment

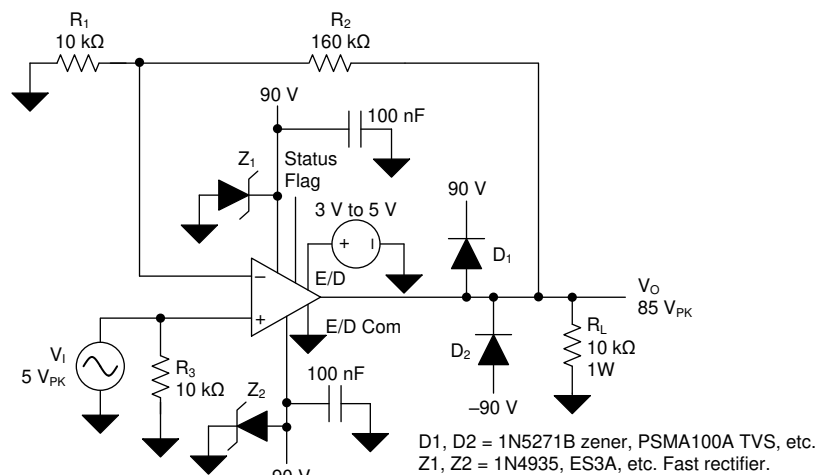


图 61. OPA462, High-Voltage Noninverting Amplifier, $A_V = 17$ V/V

8.2.1.1 Design Requirements

The OPA462 high-voltage op amp can be used in commonly applied op amp circuits, but with the added capability of allowing for the use of much higher supply voltages. A very common application of an op amp is that of a noninverting amplifier with a gain of 1 V/V or higher. 图 61 shows the OPA462 in a noninverting configuration.

The design goals for this circuit are:

- A noninverting gain of 17 V/V (24.6 dB)
- A peak output voltage of 85 V, while driving a 10 kΩ output load
- Correct biasing of E/D and E/D Com
- Protection against back electromagnetic force (EMF)

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

Figure 61 shows a noninverting circuit with a moderately high closed-loop gain (A_V) of 17 V/V (24.6 dB). In this example, a 5- V_{PK} ac signal is amplified to 85 V_{PK} across a 10-k Ω load resistor connected to the output. The peak current for this application is 8.5 mA, and is well within the OPA462 output current capability. Higher output current, typically up to 30 mA, may be attained at the expense of the output swing to the supply rails. A ± 90 - V_{DC} power supply is required for this configuration.

The noninverting amplifier circuit shows the OPA462 enable-disable function. When placed in disabled mode the op amp becomes nonfunctional, and the current consumption is reduced to approximately one-third to one-half the enabled level. An enable active state occurs when the E/D pin is left open, or is biased 3 V to 5 V greater than the E/D Com voltage level. If biased between the E/D com level, to E/D Com + 0.65 V, the OPA462 disables. More information about this function is provided in the [Enable and Disable](#) section.

Op amps designed for high-voltage and high-power applications may encounter output loads that can be quite different than those used in low-voltage, non-power op amp applications. Although every effort is made to make a high-voltage op amp such as the OPA462 robust and tolerant of different supply and different output load conditions, some loads can present potentially harmful circumstances.

Purely resistive output loads operating within the current capability range of the OPA462 do not present an unsafe condition, provided the thermal requirements discussed in the [Layout](#) section. Complex loads that have inductive or capacitive reactive elements might present an unsafe condition, and must be fully considered and addressed before implementation.

A potentially destructive mechanism is the back EMF transient that can be generated when driving an inductive load. D_1 , D_2 , Z_1 and Z_2 in Figure 61 have been added to the basic OPA462 amplifier circuit to provide protection in the event of back EMF. If the voltage at the OPA462 output attempts to momentarily rise above $V+$, D_1 becomes forward-biased and clamps the voltage between the output and $V+$ pins. This clamp must be sufficient to protect the OPA462 output transistor. If the event causes the $V+$ voltage to increase the power supply bypass capacitor, Z_1 , or both, a Zener diode or a transient voltage suppressor (TVS) can provide a path for the transient current to ground. D_2 and Z_2 provide the same protection in the negative supply circuit.

The OPA462 noninverting amplifier circuit with a closed-loop gain of 17 V/V has a small-signal, –3-dB bandwidth of nearly 800 kHz. However, the large-signal bandwidth is likely of greater importance in a high-output-voltage application. For that mode of operation, the slew rate of the op amp and the peak output swing voltage must be considered in order to determine the maximum large-signal bandwidth. The slew rate (SR) of the OPA462 is typically 6.5 V/ μ s, or 6.5×10^6 V/s. Using the 85- V_{PK} output voltage available from the circuit in Figure 61, the maximum large-signal bandwidth is calculated from the slew rate formula. Equation 1, Equation 2 and Equation 3 show the calculation process.

$$SR = 2\pi \times f_{MAX} \times V_{PK} \quad (1)$$

$$f_{MAX} = SR / (2\pi \times V_{PK}) \quad (2)$$

$$f_{MAX} = 6.5 \times 10^6 \text{ V/s} / (2\pi / 85 \text{ V}) = 12 \text{ kHz}$$

where

- $SR = 6.5 \times 10^6 \text{ V/s}$
 - $V_{PK} = 85 \text{ V}$
- (3)

The best practice for a typical parameter such as slew rate to allow for variance. In this example, keeping the large signal f_{MAX} to 10 kHz is sufficient to make sure the output avoids slew rate limiting.

Typical Applications (continued)

8.2.2.2 Detailed Design Procedure

The improved Howland current pump circuit is illustrated in [Figure 63](#). The OPA462 sources an output current of 20 mA when a low-voltage single-ended, 2.5-V reference voltage is applied to the circuit input. The source could be an actual 2.5-V precision reference. If the current-pump output current requires being set to different levels, a voltage output DAC can be used. If the input voltage polarity is reversed, the output current reverses direction, and 20 mA is sunk from the load through the OPA462 output.

The circuit shown in [Figure 63](#) provides the resistance values required to obtain a ± 20 -mA output current with the 2.5-V input voltage applied. The following can be used to select the resistors, thus setting the voltage gain and output current.

- R_{13} sets the gain, and is adjusted by the ratio of R_{14} / R_{15}
- Selecting a low value for R_{13} enables all other resistors to be high, limiting current through the feedback network
- The ratio of $R_{11} / (R_{12} + R_{13})$ must equal R_{14} / R_{15}
- If $R_{14} = R_{15}$, then $R_{12} = R_{11} - R_{13}$

Applying these relationships the resistors are selected or derived as follows:

- Let $R_{14} = R_{15} = 100 \text{ k}\Omega$
- $R_{13} = [(V_P - V_N) (R_{15} / R_{14})] / I_L = [(2.5 \text{ V} - 0 \text{ V}) (105 \Omega / 105 \Omega)] = 125 \Omega$
- $R_{12} = (R_{11} - R_{13}) = (100 \text{ k}\Omega - 125 \Omega) = 99.875 \text{ k}\Omega$

Verifying $R_{11} / (R_{12} + R_{13})$ must equal R_{14} / R_{15} requirement:

- $R_{12} = [R_{11}(R_{15} / R_{14})] - R_{13} = [105 \Omega (105 \Omega / 105 \Omega)] - 125 \Omega = 99.875 \text{ k}\Omega$

The resistor values for R_{11} through R_{15} are seen in [Figure 63](#).

The load is set to be 500Ω , the sourced output current through the load is 20 mA, and the output voltage is 10 V. The voltage directly at the OPA462 output 2.5 V higher, or 12.5 V, which compensates for the voltage drop across the $125\text{-}\Omega$ R_{13} resistor. A feedback capacitor can be added to reduce the ac bandwidth of the improved Howland current pump circuit, if needed. In this example, no capacitor is used.

The improved Howland current pump output is limited to the combined effects of the OPA462 linear output voltage swing range, the voltage drop developed across R_{13} , and the voltage drop developed across load. For a particular output current, a maximum output voltage span can be achieved. This span is referred to as the output voltage compliance range.

The OPA462 current pump sources or sinks a constant current through a load resistance of 0Ω on the low end, to just beyond $4.25 \text{ k}\Omega$ on the high end. This current range is portrayed in the dc transfer plot shown in [Figure 64](#). As shown, the load can vary from 0Ω to $4.25 \text{ k}\Omega$ and the output remains within the span of linear output compliance range.

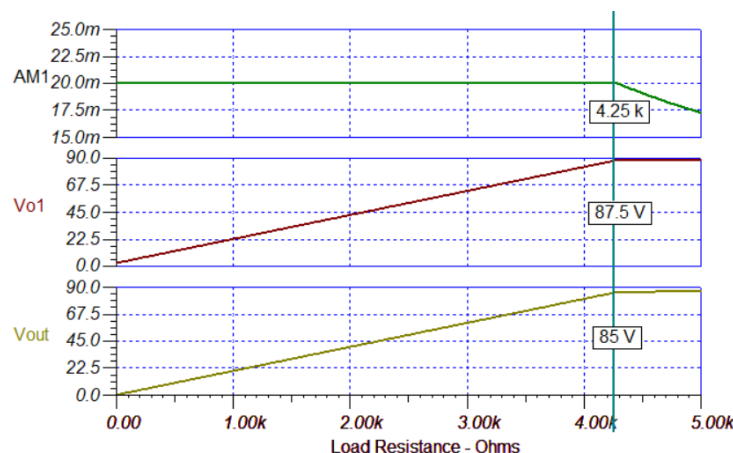


Figure 64. Output Voltage Compliance for an Improved Howland Current Pump

Typical Applications (continued)

The 4.25-k Ω limit is determined by the maximum 85-V drop across the load, and the 2.5-V drop across R_{13} when 20 mA flows through both. This voltage drop results in an output voltage of 87.5 V at the output of the OPA462, close to the positive swing limit. Beyond 4.25 k Ω , current-pump operation is forced outside the compliance range, and the output current is longer maintained at the correct level.

The OPA462 provides this wide output compliance range because of the wide, ± 90 -V power supply rating. If a standard ± 15 -V amplifier supply had been used with the OPA462, or another amplifier rated for ± 15 -V supplies, the maximum load resistance is on the order of approximately 500 Ω to 600 Ω , depending on the particular amplifier linear output range when delivering ± 20 mA. The wide supply range of the OPA462 enables the device to drive a much wider range of loads.

The improved Howland current pump can also be used to generate an accurate ac current with a peak output that matches a specified dc current level. A ± 20 -mA dc current source using the OPA462 has already been discussed; therefore, this current source is applied here to demonstrate how a 400-Hz, 20-mA current is produced.

The same circuit used in [Figure 63](#) is updated so that the 2.5-V dc voltage source has been replaced by a 400-Hz ac source with a peak voltage of 2.5 V, as shown in [Figure 65](#). A sine wave is used in this circuit, but a triangle wave, square wave, and so on, can be used instead. The output current is dependent on the ac input voltage at any particular moment.

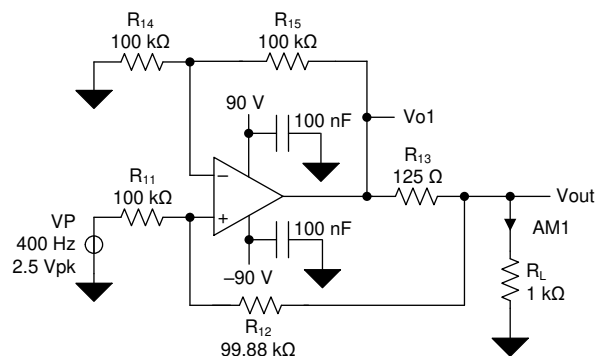


Figure 65. OPA462 Configured as a 400-Hz AC Current Generator

A 2.5-Vpk sine-wave source applied to the input point at R_{11} results in a 20-mA peak current through the load, as shown in [Figure 66](#). The load has been set to 1 k Ω , but any resistance that supports the output compliance range can be used.

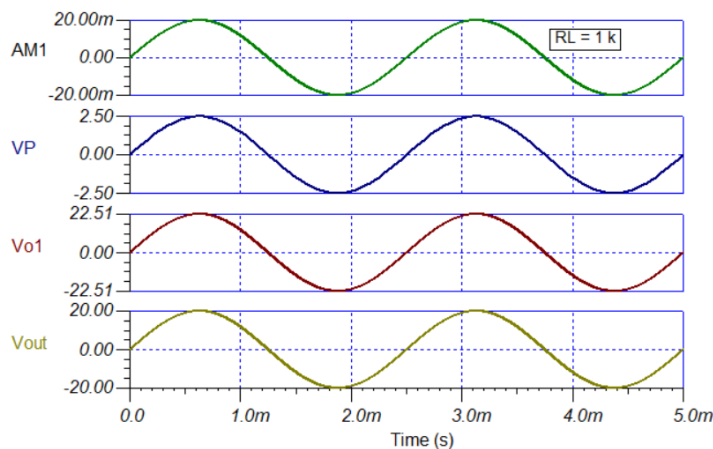


Figure 66. Improved Howland Current Pump Applied as a Peak AC-Current Generator

Typical Applications (continued)

Make sure to consider the power handling ratings of the resistors used with a high-power or high-voltage amplifier such as the OPA462. In this design, when the OPA462 is providing 20 mA dc to a 4.25-k Ω load resistance, the dc power for the load and R_{13} is simply:

- Load Power = $I_2 \cdot R_L = (20 \cdot 10^{-3} \text{ A})^2 (4.25 \cdot 10^3 \Omega) = 1.7 \text{ W}$
- Power $R_{13} = I_2 \cdot R_{13} = (20 \cdot 10^{-3} \text{ A})^2 (125 \Omega) = 50 \text{ mW}$

Clearly, the power dissipation of the load requires attention. However, in this design, R_{13} does not require high power dissipation under these operating conditions. The load must be rated to dissipate the 1.7 W over the expected operating temperature range for this example. Most often, resistor power dissipation is specified at an ambient temperature of 25°C, and reduces as temperature increases. The use of a resistor with a power rating greater than the power that must be dissipated is almost always necessary. For this example, the load may need to be rated for 3 W, or even 5 W, to make sure that the load does not overheat and maintains reliability. In any case, determine the power dissipation for the particular operating conditions. Be especially attentive to the power rating issue regarding surface-mount resistors. The thermal environment in which surface-mount resistors operate may be much different than a resistor exposed in free air.

The improved Howland current pump amplifier circuit relies on both negative and positive feedback for operation. More negative feedback than positive feedback is used, but that does not always provide stability when the output load characteristics are included. When unity-gain stable amplifiers such as the OPA462 are employed, and they drive a resistive load, the amplifier phase margin should be sufficient so that the circuit is stable. However, if the output load is complex, containing both resistive and reactive components ($R \pm jX$), certain combinations degrade the phase margin to the point where instability results. Instability is even more evident when this current pump is used to drive certain inductive loads.

When required, compensation is determined based on the particular circuit to which the OPA462 is being applied. Amplifier stability and compensation is a vast subject covered in numerous TI documents, and TI training programs, such as [TI Precision Labs – Op Amps](#).

9 Power Supply Recommendations

The OPA462 operates from power supplies up to ± 90 V, or a total of 180 V, with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. A power-supply bypass capacitor of at least 0.1 μ F is required for proper operation. Make sure that the capacitor voltage rating is suitable for the high voltage across the full operating temperature range. Parameters that vary significantly with operating voltage are shown in the [Typical Characteristics](#) section.

Some applications do not require an equal positive and negative output voltage swing. Power-supply voltages do not have to be equal. The OPA462 operates with as little as 12 V between the supplies, and with up to 180 V between the supplies.

10 Layout

10.1 Layout Guidelines

10.1.1 Thermally-Enhanced PowerPAD™ Package

The OPA462 comes in an 8-pin SO PowerPAD package that provides an extremely low thermal resistance, $R_{\theta JC(bot)}$, path between the die and the exterior of the package. This package features an exposed thermal pad that has direct thermal contact with the die. Thus, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

The OPA462 SO-8 PowerPAD is a standard-size SO-8 package constructed using a downset leadframe upon which the die is mounted, as [Figure 67](#) shows. This arrangement results in the leadframe being exposed as a thermal pad on the underside of the package. The thermal pad on the bottom of the device can then be soldered directly to the PCB, using the PCB as a heat sink. In addition, plated-through holes (vias) provide a low thermal resistance heat flow path to the back side of the PCB. This architecture enhances the OPA462 power dissipation capability significantly, eliminates the use of bulky heat sinks and slugs traditionally used in thermal packages, and allows the OPA462 to be easily mounted using standard PCB assembly techniques.

注

The SO-8 PowerPAD is pin-compatible with standard SO-8 packages, and as such, the OPA462 is a drop-in replacement for operational amplifiers in existing sockets. Always solder the PowerPAD to the PCB V– plane, even with applications that have low power dissipation. Solder the device to the PCB to provide the necessary thermal, mechanical, and electrical connections between the leadframe die pad and the PCB.

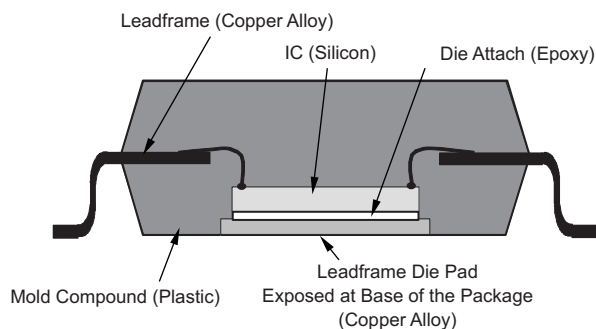


Figure 67. Cross Section View of a PowerPAD™ Package

Layout Guidelines (continued)

10.1.2 PowerPAD™ Integrated Circuit Package Layout Guidelines

The PowerPAD integrated circuit package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat is conducted away from the package into either a ground plane or other heat-dissipating device. Always solder the PowerPAD to the PCB, even with applications that have low power dissipation. Follow these steps to attach the device to the PCB:

1. Connect the PowerPAD to the most negative supply voltage on the device, V_{-} .
2. Prepare the PCB with a top-side etch pattern. There must be etching for the leads, as well as etching for the thermal pad.
3. Thermal vias improve heat dissipation, but are not required. The thermal pad can connect to the PCB using an area equal to the pad size with no vias, but externally connected to V_{-} .
4. Place recommended holes in the area of the thermal pad. Recommended thermal land size and thermal via patterns for the SO-8 DDA package are shown in the thermal land pattern mechanical drawing appended at the end of this document. These holes must be 13 mils (0.013 in, or 0.3302 mm) in diameter. Keep the holes small, so that solder wicking through the holes is not a problem during reflow. The minimum recommended number of holes for the SO-8 PowerPAD package is five.
5. Additional vias can be placed anywhere along the thermal plane outside of the thermal pad area. These vias help dissipate the heat generated by the OPA462 device. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad because they are not in the thermal pad area to be soldered; thus, wicking is not a problem.
6. Connect all holes to the internal power plane of the correct voltage potential, V_{-} .
7. When connecting these holes to the plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations, making the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the OPA462 PowerPAD package must make the connections to the internal plane with a complete connection around the entire circumference of the plated-through hole.
8. The top-side solder mask must leave the pins of the package and the thermal pad area exposed. The bottom-side solder mask must cover the holes of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.
9. Apply solder paste to the exposed thermal pad area and all of the device pins.
10. With these preparatory steps in place, simply place the device in position, and run through the solder reflow operation as with any standard surface-mount component.

This preparation results in a properly installed device. For detailed information on the PowerPAD package, including thermal modeling considerations and repair procedures, see the [PowerPAD™ Thermally Enhanced Package application report](#).

10.1.3 Pin Leakage

When operating the OPA462 with high supply voltages, parasitic leakages may occur between the inputs and the supplies. This effect is most noticeable at the noninverting input, $+IN$, when the input common-mode voltage is high compared to the negative supply voltage, V_{-} . To minimize this leakage, place guard tracing, driven at the same voltage as the input signal, alongside the input signal traces and pins.

Layout Guidelines (continued)

10.1.4 Thermal Protection

Figure 68 shows the thermal shutdown behavior of a socketed OPA462 that internally dissipates 1 W. Unsoldered and in a socket, the $R_{\theta JA}$ of the DDA package is typically 128°C/W. With the socket at 25°C, the output stage temperature rises to the shutdown temperature of 150°C, which triggers automatic thermal shutdown of the device. The device remains in thermal shutdown (output is in a high-impedance state) until it cools to 130°C where the device is again powered. This thermal protection hysteresis feature typically prevents the amplifier from leaving the safe operating area, even with a direct short from the output to ground or either supply. The absolute maximum specification is 180 V, and the OPA462 must not be allowed to exceed 180 V under any condition. Failure as a result of breakdown, caused by spiking currents into inductive loads (particularly with elevated supply voltage), is not prevented by the thermal protection architecture.

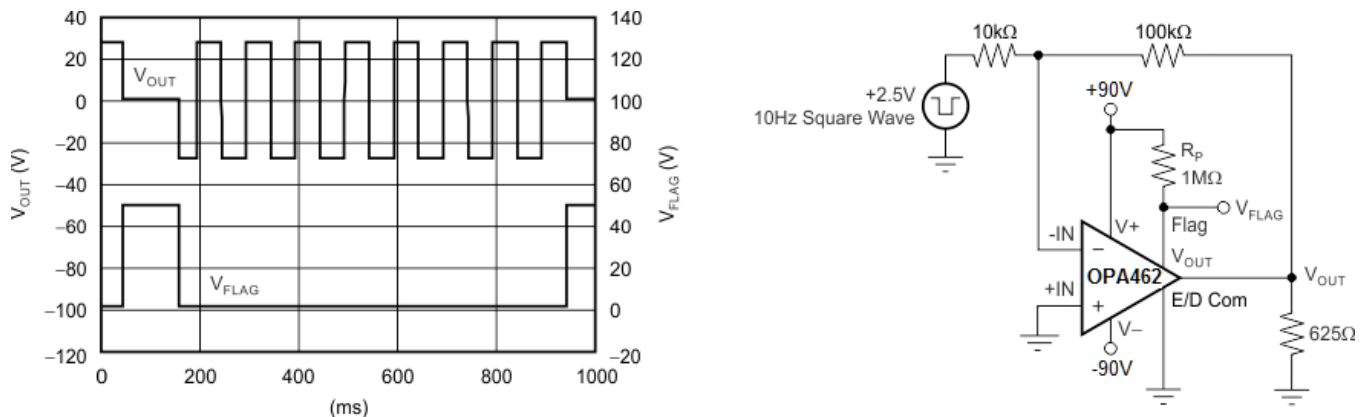


Figure 68. Thermal Shutdown

10.1.5 Power Dissipation

Power dissipation depends on power supply, signal, and load conditions. For dc signals, power dissipation is equal to the product of the output current times the voltage across the conducting output transistor, $P_D = I_L (V_S - V_O)$. Power dissipation can be minimized by using the lowest possible power-supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a dc output voltage of one-half the power-supply voltage. Dissipation with ac signals is lower because the root-mean square (RMS) value determines heating. The [Instruments, Power Amplifier Stress and Power Handling Limitations application bulletin](#) explains how to calculate or measure dissipation with unusual loads or signals.

The OPA462 can supply output currents of up to 45 mA. Supplying this level of current is common for op amps operating from ± 15 -V supplies. However, with high supply voltages, internal power dissipation of the op amp can be quite high. Relative to the package size, operation from a single power supply (or unbalanced power supplies) can produce even greater power dissipation because a large voltage is impressed across the conducting output transistor. Applications with high power dissipation may require a heat sink or a heat spreader.

10.1.6 Heat Dissipation

Power dissipated in the OPA462 causes the junction temperature to rise. For reliable operation, junction temperature must be limited to 125°C, maximum. Maintaining a lower junction temperature always results in higher reliability. Some applications require a heat sink to make sure that the maximum operating junction temperature is not exceeded. Junction temperature can be determined according to Equation 4:

$$T_J = T_A + P_D R_{\theta JA} \quad (4)$$

Package thermal resistance, $R_{\theta JA}$, is affected by mounting techniques and environments. Poor air circulation and use of sockets can significantly increase thermal resistance to the ambient environment. Many op amps placed closely together also increase the surrounding temperature. Best thermal performance is achieved by soldering the op amp onto a circuit board with wide printed circuit traces to allow greater conduction through the op amp leads. Increasing circuit board copper area to approximately 0.5 in² decreases thermal resistance; however, minimal improvement occurs beyond 0.5 in², as shown in Figure 69.

Layout Guidelines (continued)

For additional information on determining heat sink requirements, consult the [Heat Sinking—TO-3 Thermal Model application bulletin](#), available for download at www.ti.com.

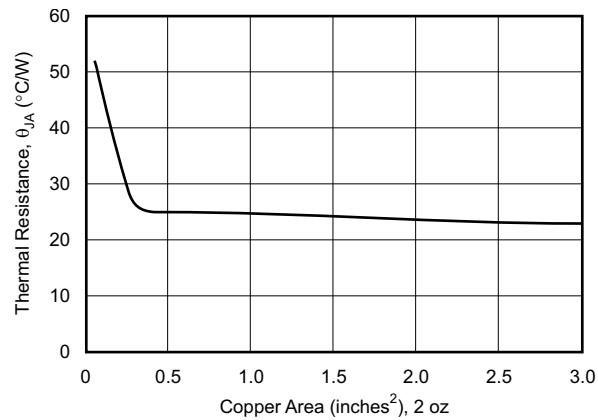


FIG 69. Thermal Resistance vs Circuit Board Copper Area

10.2 Layout Example

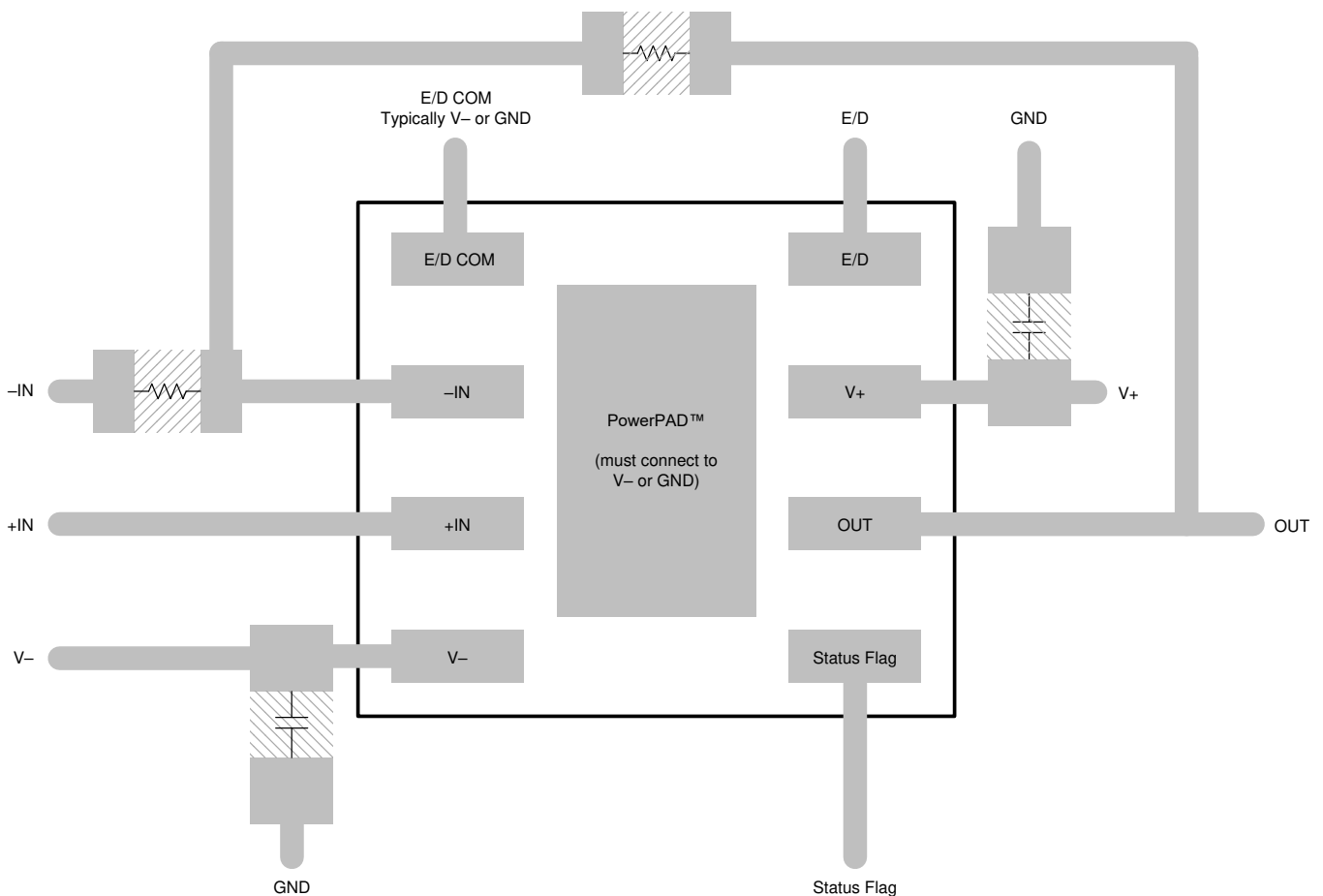


FIG 70. OPA462 Layout Example

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 TINA-TI™ (無料のダウンロード・ソフトウェア)

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TINA-TIはAnalog eLab Design Centerから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

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11.2 ドキュメントのサポート

11.2.1 関連資料

OPA462の使い方に関する以下のドキュメントを参考としてお勧めします。すべてのドキュメントは、特に記述のない限りwww.ti.comからダウンロードできます。

- テキサス・インスツルメンツ、『[HEAT SINKING — TO-3 THERMAL MODEL](#)』アプリケーション広報 (英語)
- テキサス・インスツルメンツ、『[POWER AMPLIFIER STRESS AND POWER HANDLING LIMITATIONS](#)』アプリケーション広報 (英語)
- テキサス・インスツルメンツ、『[Op Amp Performance Analysis](#)』アプリケーション広報 (英語)
- テキサス・インスツルメンツ、『[Single-Supply Operation of Operational Amplifiers](#)』アプリケーション広報 (英語)
- テキサス・インスツルメンツ、『[Tuning in Amplifiers](#)』アプリケーション広報 (英語)
- テキサス・インスツルメンツ、『[放熱特性に優れたPowerPAD™パッケージ](#)』アプリケーション・レポート

11.3 サポート・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.6 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA462IDDA	Active	Production	SO PowerPAD (DDA) 8	75 TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	OPA462
OPA462IDDA.A	Active	Production	SO PowerPAD (DDA) 8	75 TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	OPA462
OPA462IDDAR	Active	Production	SO PowerPAD (DDA) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	OPA462
OPA462IDDAR.A	Active	Production	SO PowerPAD (DDA) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	OPA462

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

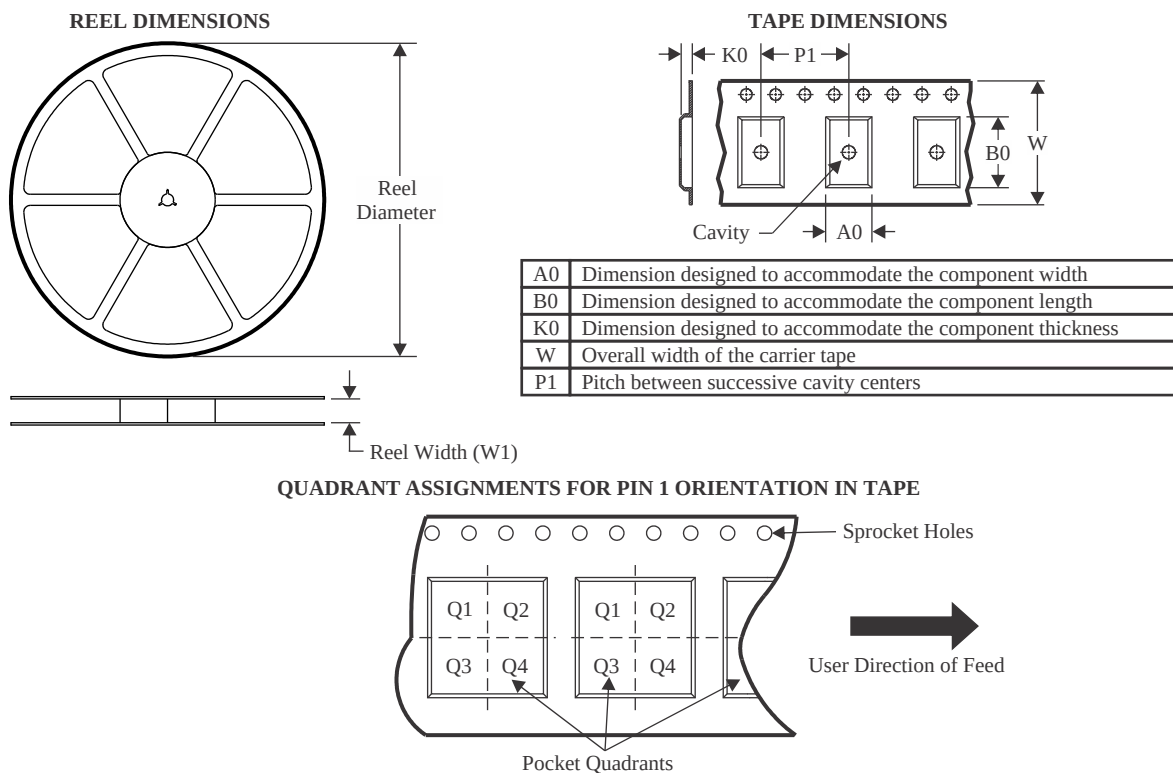
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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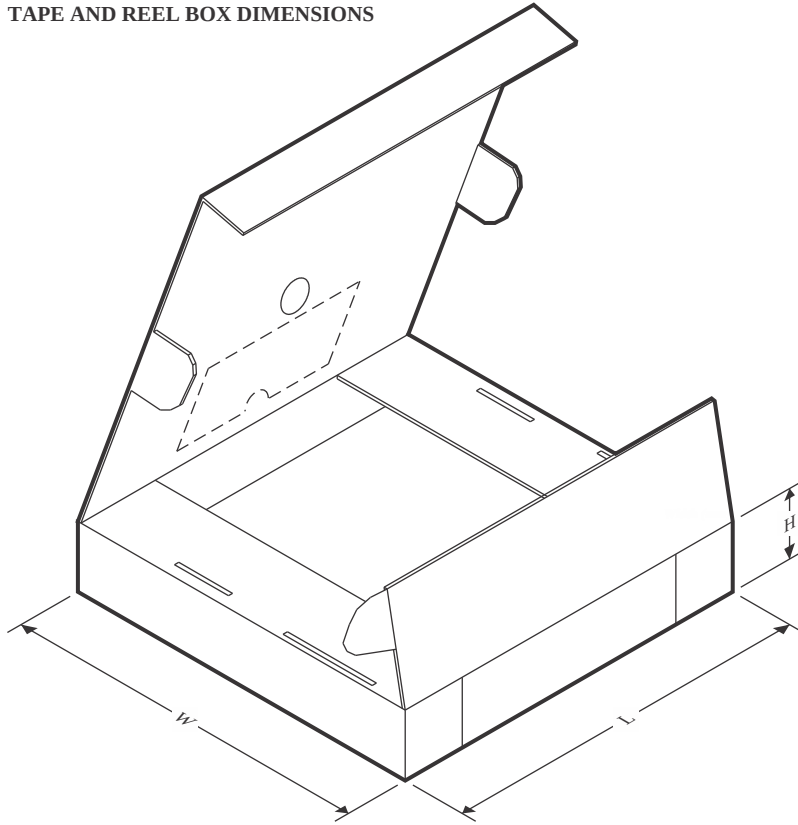
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA462IDDAR	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

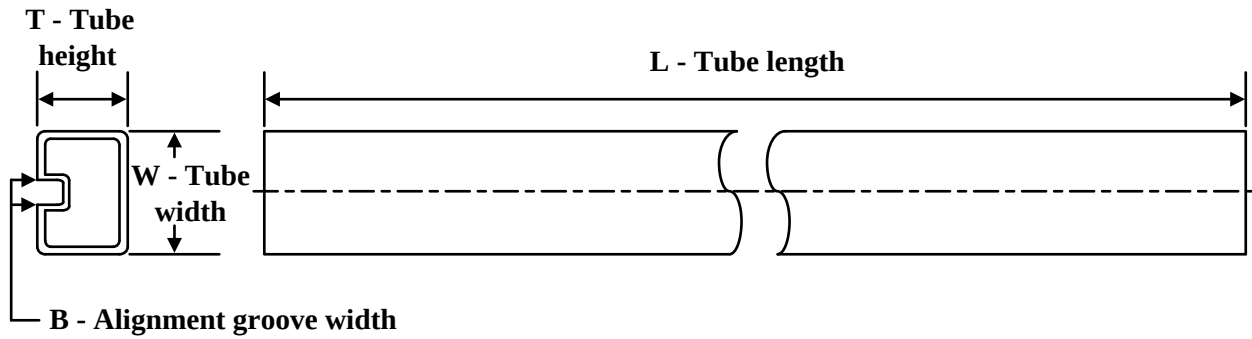
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

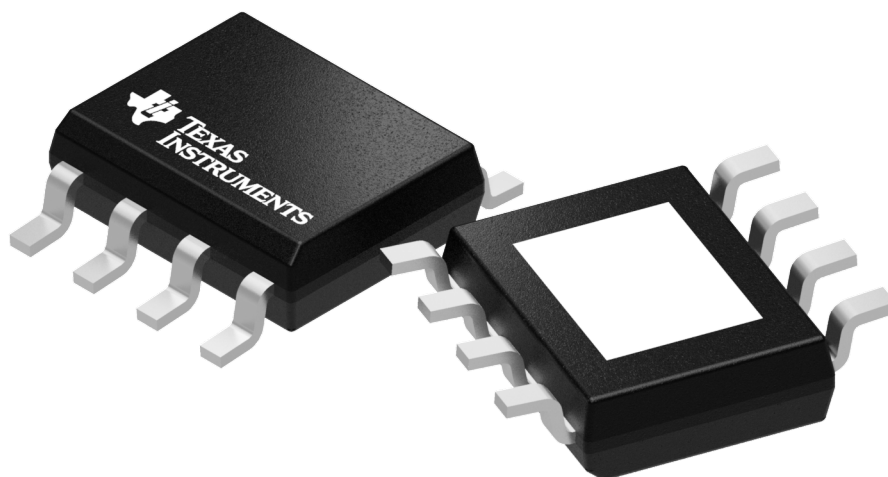
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA462IDDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

TUBE

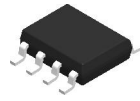


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA462IDDA	DDA	HSOIC	8	75	517	7.87	635	4.25
OPA462IDDA.A	DDA	HSOIC	8	75	517	7.87	635	4.25



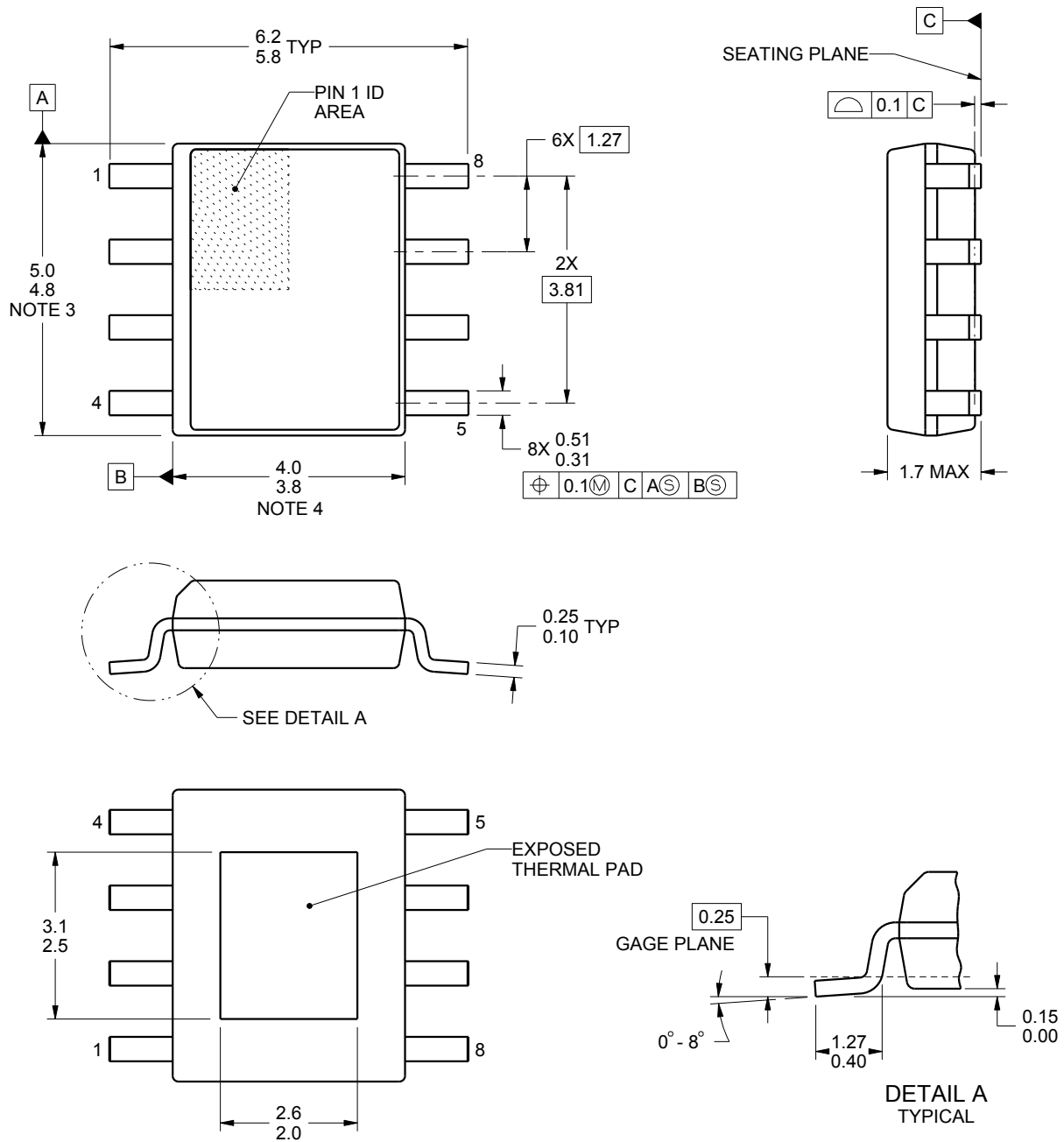
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA0008J

PACKAGE OUTLINE

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



4221637/B 03/2016

PowerPAD is a trademark of Texas Instruments.

NOTES:

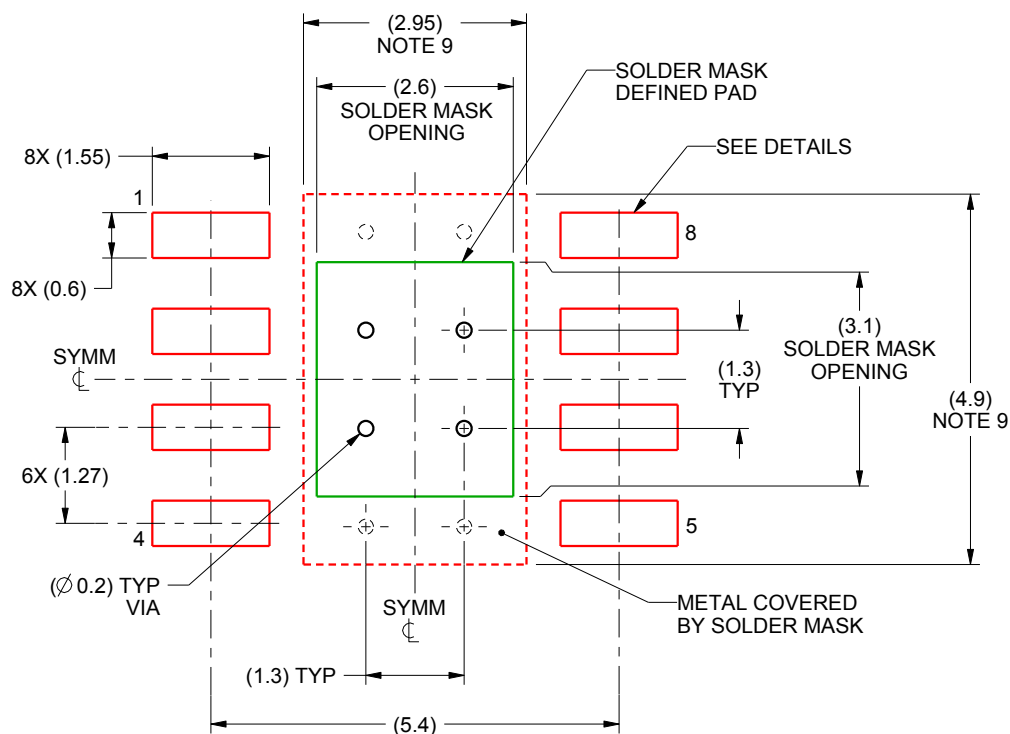
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.

EXAMPLE BOARD LAYOUT

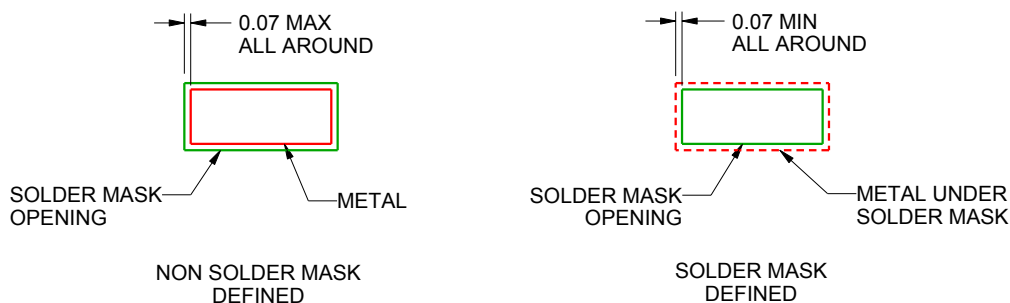
DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS

4221637/B 03/2016

NOTES: (continued)

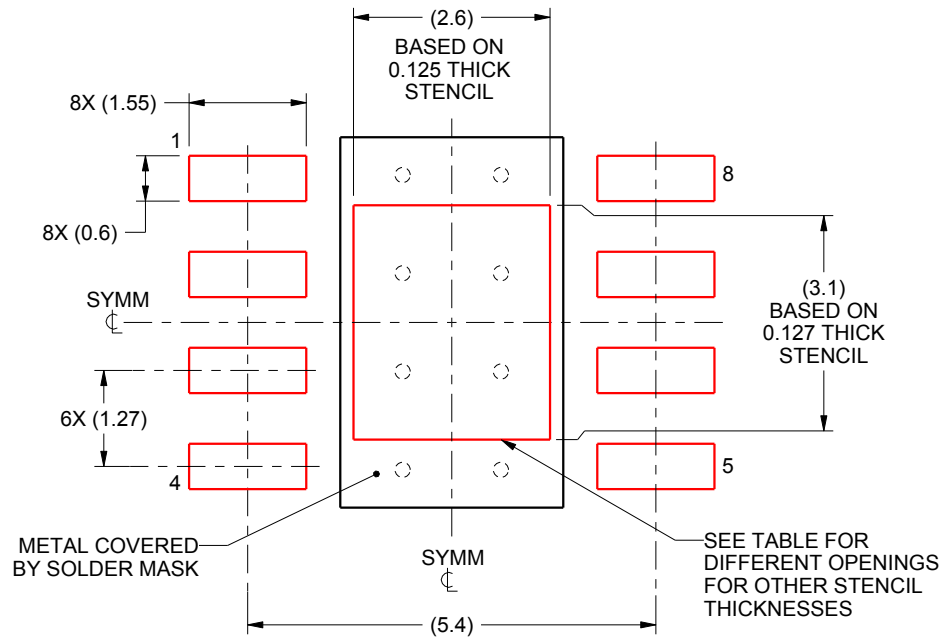
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.47
0.125	2.6 X 3.1 (SHOWN)
0.150	2.37 X 2.83
0.175	2.20 X 2.62

4221637/B 03/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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