OPA521 2.5A狭帯域ライン・ドライバ

1 特長

- 対応プロトコル:
  - CENELECの周波数帯A、B、C、D
  - ARIB STD-T84、FCC
  - FSK、SFSK、NB-OFDM
- 標準への準拠
  - EN50065-1、-2、-3、-7
  - FCC, Part 15
  - ARIB STD-T84
- 規格
  - G3、PRIME、P1901.2、ITU-G.hnem
- 熱および過電流保護機能を内蔵したライン・ドライバ
- 静止電流をピンで選択可能
  - スタンバイ・モードで58µA (標準値)
  - CENELECの周波数帯A、B、C、Dで51mA (標準値)
  - FCC、ARIB STD-T84で78mA (標準値)
- パッケージ: 5mm×5mmの20ピンVQFN
- 動作時接合部温度範囲:
  T_A＝－40℃～＋125℃

2 アプリケーション

- 電力品質測定器
- 商用ネットワークとサーバーのPSU (電源)
- 照明
- ソーラー・アーク保護
- 集中型インバータ

3 概要

OPA521は、CENELECの周波数帯A、B、C、D、およびARIB STD-T84、FCC Part 15の電力線通信(PLC)伝導エミッション要件を満たしたライン・ドライバ・パワー・アンプであり、無効負荷への最大2.5Aの大電流、低インピーダンスのラインを駆動できます。内部保護構造が最適化されているため、外付けの保護部品を最小限に抑え、コスト効果およびスペース効率の高いシステムを実現できます。

OPA521は、3.8MHzの帯域幅で－7V/Vの閉ループ・ゲインを提供します。またモノリシックな集積回路により、電力線通信機器で高い信頼性を実現します。

OPA521ライン・ドライバは、7V～24Vの単一電源で動作し、標準的な負荷電流(I_{OUT}＝2.5A (最大値))では、広い出力振幅により公称24V電源で10V_{PP}の能力が得られます。

過熱および短絡条件に対する保護機能を備えており、異常検出フラグにより、電流および熱の限度値を示します。シャットダウン・ピンも用意されているため、低消費電力状態に移行して、消費電流を58µA (標準値)に抑えることができます。

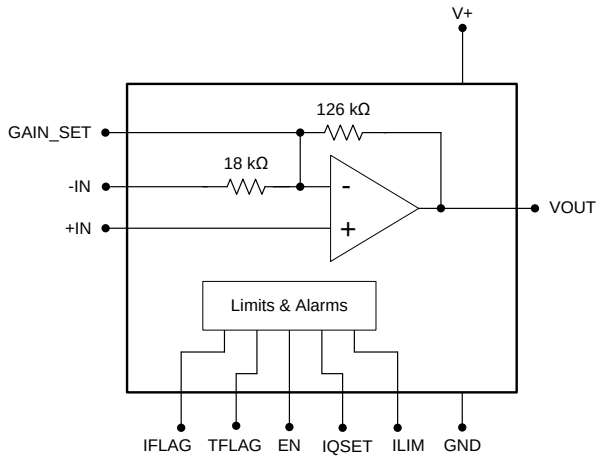
OPA521は表面実装の5mm×5mm、20ピンVQFN (RGW)パッケージで供給されます。－40℃～＋125℃の拡張産業用接合部温度範囲で動作可能です。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
OPA521	VQFN (20)	5.00mm×5.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

OPA521ブロック図



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

目次

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 改訂履歴 ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Electrical Characteristics: Digital ... 6
6.7 Electrical Characteristics: Power Supply ... 6
6.8 Typical Characteristics ... 7
7 **Detailed Description** ... 11
7.1 Overview ... 11
7.2 Functional Block Diagram ... 11
7.3 Feature Description ... 11
7.4 Device Functional Modes ... 12
8 **Application and Implementation** ... 13
8.1 Application Information ... 13
8.2 Typical Application ... 13
9 **Power Supply Recommendations** ... 18
10 **Layout** ... 21
10.1 Layout Guidelines ... 21
10.2 Layout Example ... 23
11 デバイスおよびドキュメントのサポート ... 24
11.1 デバイス・サポート ... 24
11.2 ドキュメントのサポート ... 24
11.3 ドキュメントの更新通知を受け取る方法 ... 24
11.4 コミュニティ・リソース ... 24
11.5 商標 ... 24
11.6 静電気放電に関する注意事項 ... 24
11.7 Glossary ... 24
12 メカニカル、パッケージ、および注文情報 ... 24

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

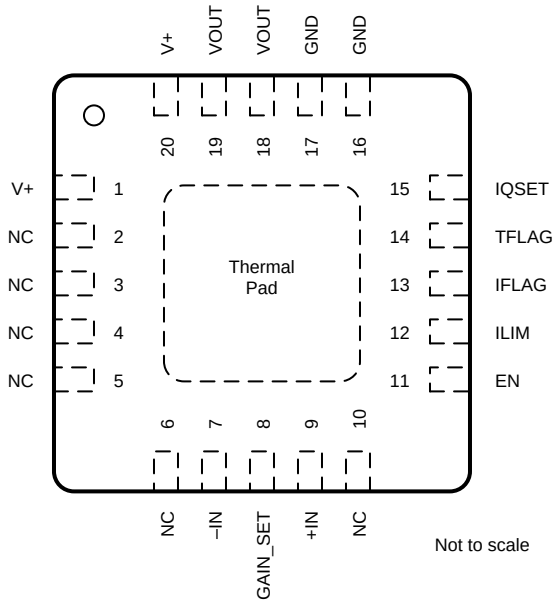
2018年5月発行のものから更新 **Page**

- 生産データを用いたデータシートの初版 ... 1

Copyright © 2018, Texas Instruments Incorporated

5 Pin Configuration and Functions

RGW Package
20-Pin VQFN With Exposed Thermal Pad
Top View



NC - no internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	11	I	Enables the amplifier (active high, high enables the OPA521)
GAIN_SET	8	I	Connect an external resistor to Gain_Set and -IN to increase the gain beyond -7 V/V
GND	16, 17	—	Ground
IFLAG	13	O	Current limit warning flag (open-drain, active high, high signifies current limit condition)
ILIM	12	I	Resistor programmable current limit
+IN	9	I	Non-inverting input (connect to a voltage equal to (V+)/2)
–IN	7	I	Inverting input for closed loop gain = –7 V/V
IQSET	15	I	Quiescent current select (active high, high configures the OPA521 to operate in FCC/ARIB bands, low configures the OPA521 to operate in CENELEC Bands A, B, C, D)
NC	2, 3, 4, 5, 6, 10	—	No internal connection
TFLAG	14	O	Thermal limit warning flag (open-drain, active high, high signifies thermal limit condition)
V+	1, 20	—	Positive power supply
VOUT	18. 19	O	Output
Thermal pad		—	Must be soldered to PCB and connected to GND

Copyright © 2018, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
Supply voltage, V+		Pins 1, 20		26	V
Signal input pins	Voltage[2]	Pins 7, 8, 9, 12	–0.4	(V+) + 0.4	V
		Pins 11, 15	–0.4	3.3	
	Current[2]	Pins 7, 8, 9, 11, 12, 15		±10	mA
Signal output terminals	Voltage	Pins 18, 19	–0.4	(V+) + 0.4	V
		Pins 13, 14	–0.4	3.3	
	Current; short-circuit to GND	Pins 13, 14, 18, 19	Continuous		
Operating junction temperature[3]			–40	125	°C
Storage temperature, T_{stg}			–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.4 V beyond the supply rails should be current limited to 10 mA or less.
(3) The device automatically goes into shutdown above +140℃ junction temperature

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, V+	7		24	V
Output current, DC[1]			1.9	A
Operating junction temperature	–40		125	°C

(1) Under safe operating conditions. See *Power Amplifier Stress and Power Handling Limitations* safe operating area (SOA) information.

6.4 Thermal Information

THERMAL METRIC[1]		OPA521 RGW (QFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	12.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Copyright © 2018, Texas Instruments Incorporated

6.5 Electrical Characteristics

At T_{CASE} = 25°C, V+ = 15 V, IN+ = (V+) / 2, R_{LOAD} = 50 Ω unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
NOISE							
	Integrated output noise	CEN-A	35 kHz to 95 kHz		45		μV_{RMS}
		CEN-B	95 kHz to 125 kHz		32		μV_{RMS}
		CEN-C	125 kHz to 140 kHz		23		μV_{RMS}
		CEN-D	140 kHz to 148 kHz		16.5		μV_{RMS}
		ARIB STD-T84	35 kHz to 420 kHz		114		μV_{RMS}
		FCC-LOW	35 kHz to 125 kHz		55		μV_{RMS}
		G3-FCC	150 kHz to 490 kHz		107		μV_{RMS}
INPUT							
	Input voltage range, IN-		For linear operation, +IN = V+/2	(GND + 0.4)/7		(V+ – 0.4)/7	V
	Input impedance				18		kΩ
FREQUENCY RESPONSE							
BW	Bandwidth		I_{LOAD} = 0 mA		3.82		MHz
SR	Slew rate		V+ = 24 V, V_{OUT} = 20-V step		75		V/µs
	Full-power bandwidth		V+ = 24 V, V_{OUT} = 15 V_{PP}		800		kHz
PSRR	Power-supply rejection ratio		RTI, DC	80	94		dB
			RTI, DC to f = 50 kHz		See Typical Curves		
OUTPUT							
V_O	Voltage output swing	From V+	I_O = 200-mA sourcing, 1-ms pulse			0.5	V
			I_O = 1.5-A sourcing, 1-ms pulse			2.25	V
		From GND	I_O = 200 mA sinking, 1-ms pulse			0.5	V
			I_O = 1.5-A sinking, 1-ms pulse			1.5	V
	Max continuous current, DC		ILIM (pin 12) connected to ground		See *Recommended Operating Conditions*		A
	Output resistance		I_O = 1.9 A, f = 500 kHz		0.1		Ω
	Disabled output impedance		f = 100 kHz		145 || 125		kΩ || pF
	Max output current	Resistor-selectable	ILIM (pin 12) connected to ground		2.5		A
GAIN							
G	Nominal gain		V_{OUT}/V_{IN}		–7		V/V
G_E	Gain error		T_J = -40°C to +125°C	–2%	0.1%	2%	
	Gain error drift		T_J = -40°C to +125°C		±5		ppm/°C
THERMAL SHUTDOWN							
	Junction temperature at shutdown				140		°C
	Hysteresis				10		°C
	Return to normal operation				130		°C

Copyright © 2018, Texas Instruments Incorporated

6.6 Electrical Characteristics: Digital

At T_{CASE} = 25°C, V+ = 15 V, IN+ = (V+) / 2, R_{LOAD} = 50 Ω unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (ENABLE, IQSET)							
	Leakage input current		GND ≤ V_{IN} ≤ 3.3	–1	0.01	1	µA
V_{IH}	High-level input voltage				2	3.3	V
V_{IL}	Low-level input voltage			GND		0.8	V
	EN pin function (active high)	EN pin high	2 < EN < 3.3	Device in normal operation			
		EN pin low	EN < 0.8	Device in shutdown			
	IQSET pin function (active high)	IQSET pin high	IQSET > 2	Device in FCC/ARIB mode (I_Q = 78 mA (typ))			
		IQSET pin low	IQSET < 0.8	Device in CENELEC mode (I_Q = 51 mA (typ))			
DIGITAL OUTPUTS (TFLAG, IFLAG)							
I_{OH}	High-level output current		V_{OH} = 3.3 V			1	µA
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.4	V
I_{OL}	Low-level output current		V_{OL} = 400 mV	4			mA
	TFLAG (active high, open-drain)	TFLAG pin high	TFLAG sink high < 1 µA	Device is in thermal shutdown			
		TFLAG pin low	TFLAG < 0.4 V	Device is not in thermal shutdown			
	IFLAG (active high, open-drain)	IFLAG pin high	IFLAG sink high < 1 µA	Device is in current limit			
		IFLAG pin low	IFLAG < 0.4 V	Device is not in current limit			
SHUTDOWN MODE TIMING							
	Enable time		SD pin transitions from low to high		3		ms
	Disable time		SD pin transitions from high to low		2		ms

6.7 Electrical Characteristics: Power Supply

At T_{CASE} = 25°C, V+ = 15 V, IN+ = (V+) / 2, R_{LOAD} = 50 Ω unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING SUPPLY RANGE						
V+	Power amplifier		7	15	24	V
QUIESCENT CURRENT (ENABLE pin high)						
I_Q	FCC/ARIB mode	I_O = 0 A, IQSET pin high	64	78	88	mA
	CENELEC mode	I_O = 0 A, IQSET pin low	41	51	61	mA
SHUTDOWN (ENABLE pin low)						
EN	Power amplifier	EN pin low		58	130	µA

Copyright © 2018, Texas Instruments Incorporated

6.8 Typical Characteristics

At T_{CASE} = +25°C, V+ = 24 V, IN+ = (V+)/2, R_{LOAD} = 50 Ω unless otherwise noted.

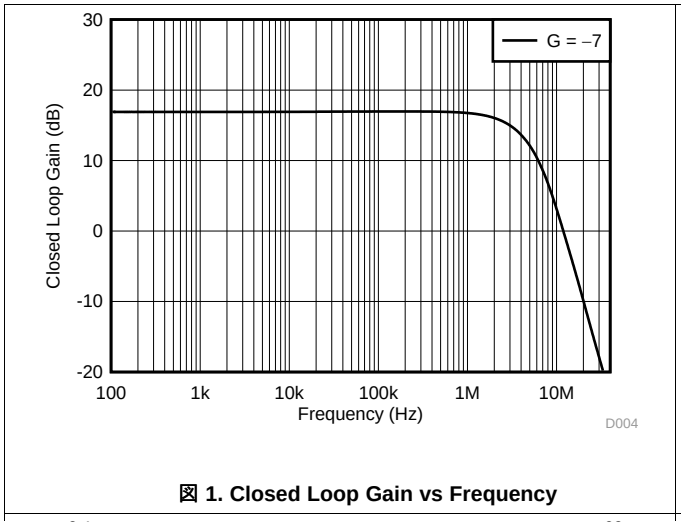


図 1. Closed Loop Gain vs Frequency

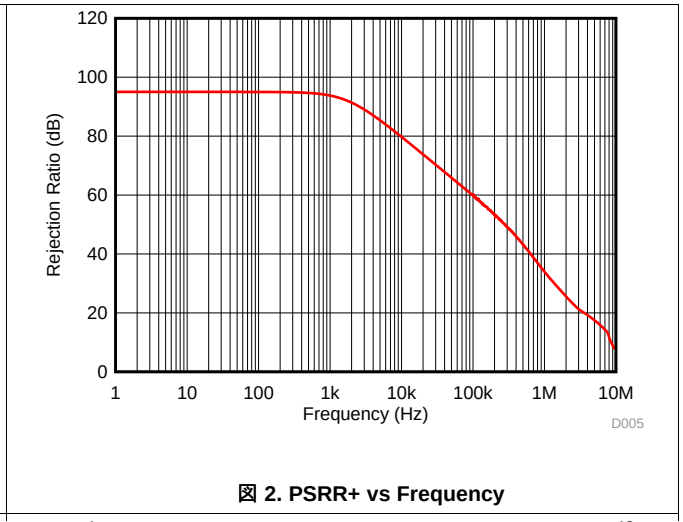
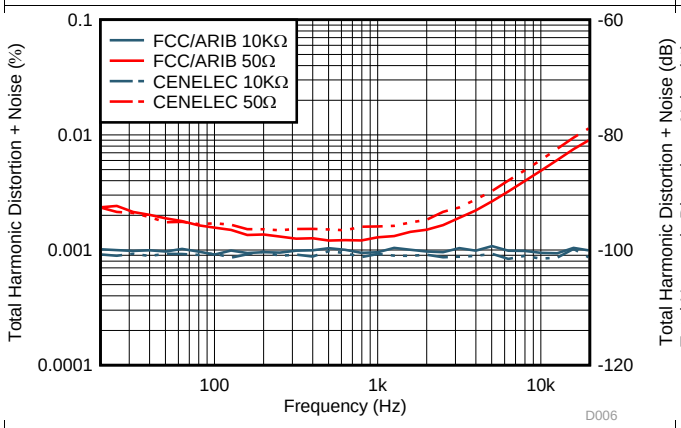
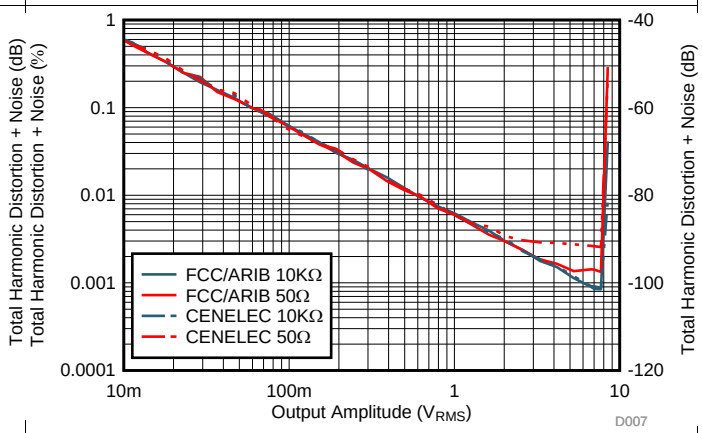


図 2. PSRR+ vs Frequency



V_{OUT} = 7 V_{RMS}

図 3. THD+N vs Frequency



f = 1 kHz

図 4. THD+N vs Output Amplitude

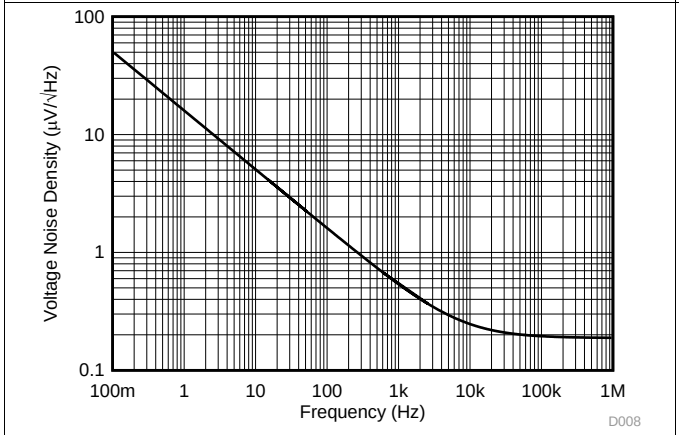


図 5. Input Voltage Noise Spectral Density

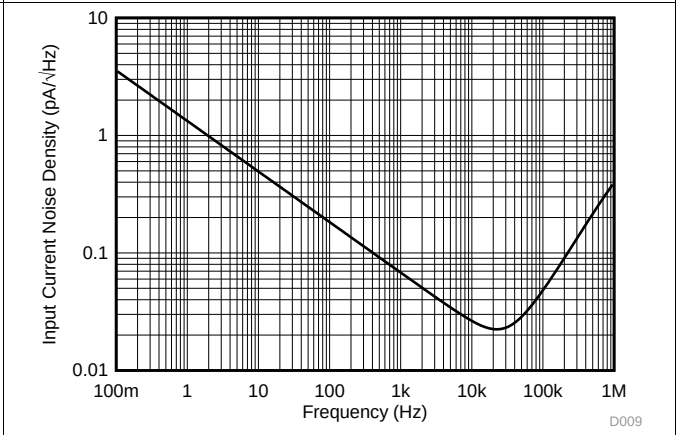


図 6. Input Current Noise Density

Copyright © 2018, Texas Instruments Incorporated

Typical Characteristics (continued)

At T_{CASE} = +25°C, V+ = 24 V, IN+ = (V+)/2, R_{LOAD} = 50 Ω unless otherwise noted.

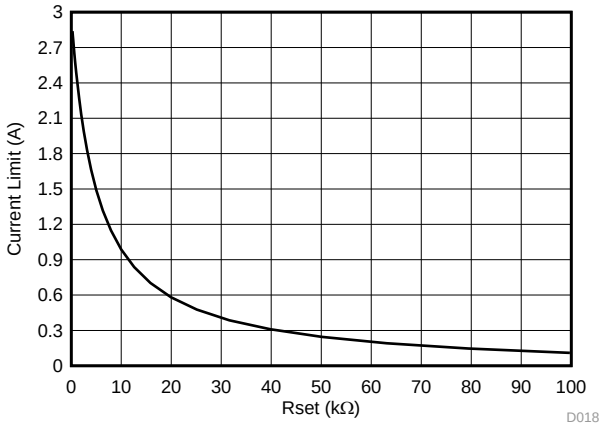


図 7. Maximum Output Current Limit vs R_{SET}

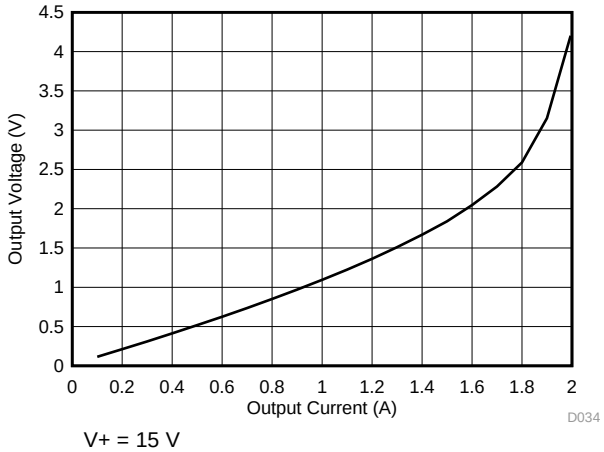


図 8. Output Swing from V+ vs Output Current (Sourcing)

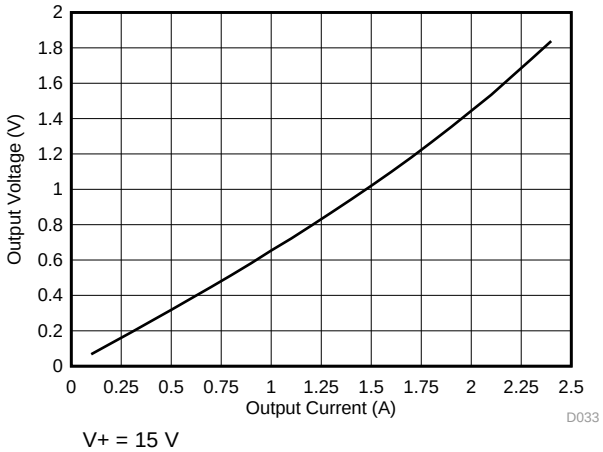


図 9. Output Swing from GND vs Output Current (Sinking)

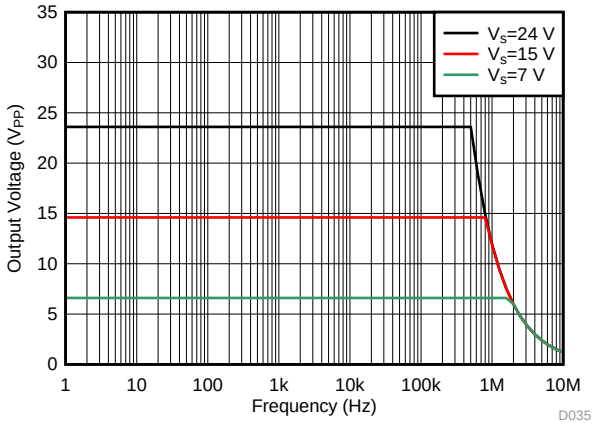


図 10. Maximum Output Voltage vs Frequency

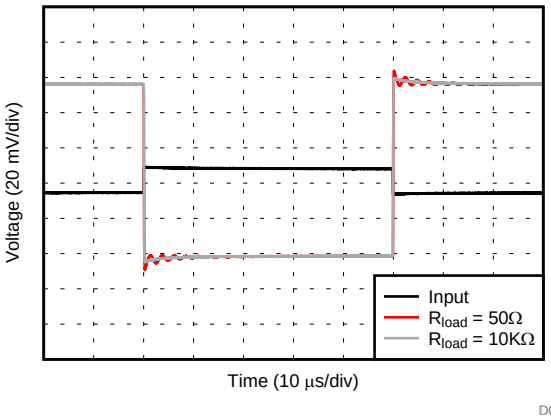


図 11. Small-Signal Step Response

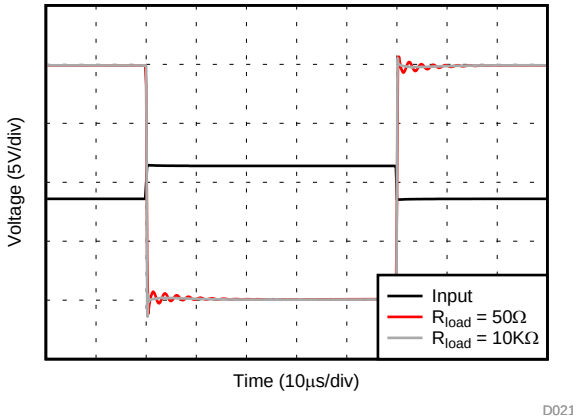


図 12. Large-Signal Step Response

Copyright © 2018, Texas Instruments Incorporated

Typical Characteristics (continued)

At T_{CASE} = +25°C, V+ = 24 V, IN+ = (V+)/2, R_{LOAD} = 50 Ω unless otherwise noted.

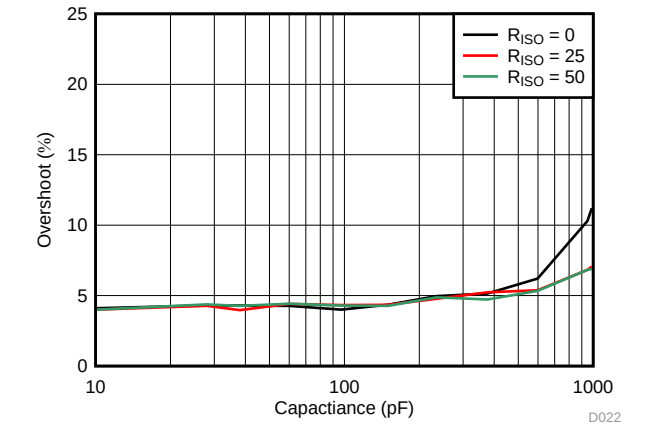


図 13. Small-Signal Overshoot vs Capacitive Load

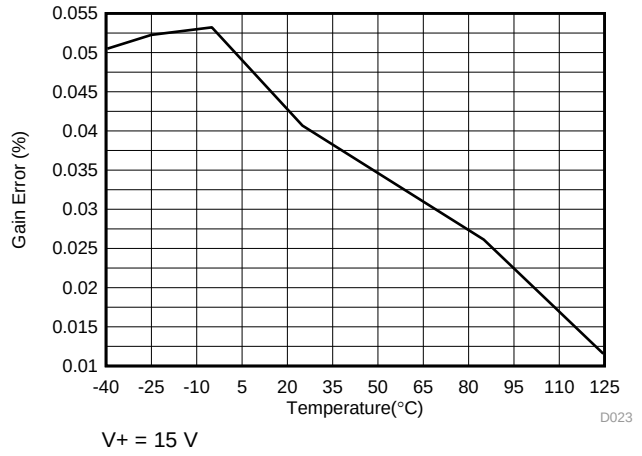


図 14. Gain Error vs Temperature

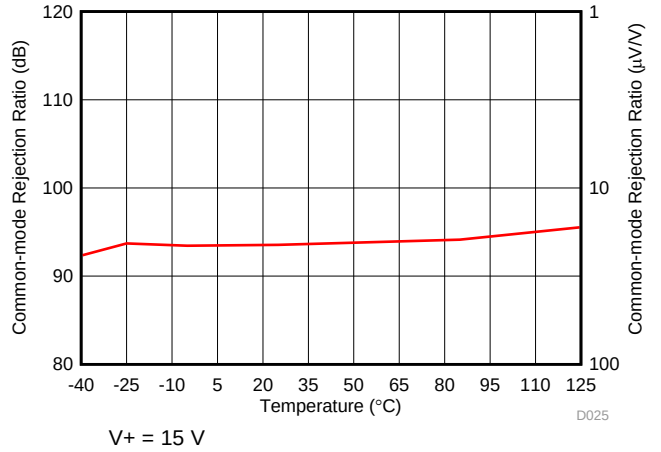


図 15. CMRR vs Temperature

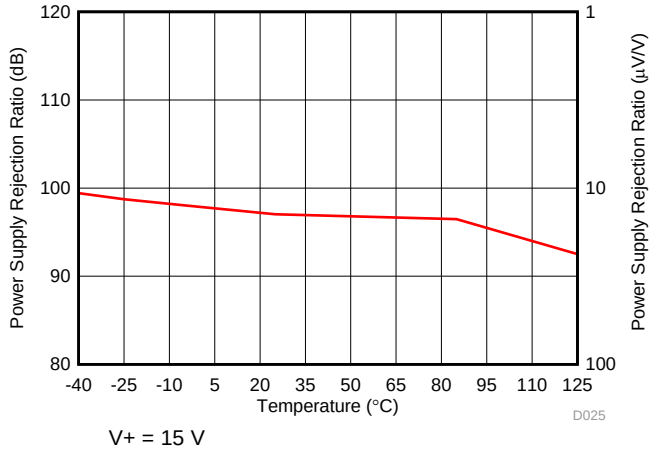


図 16. PSRR vs Temperature

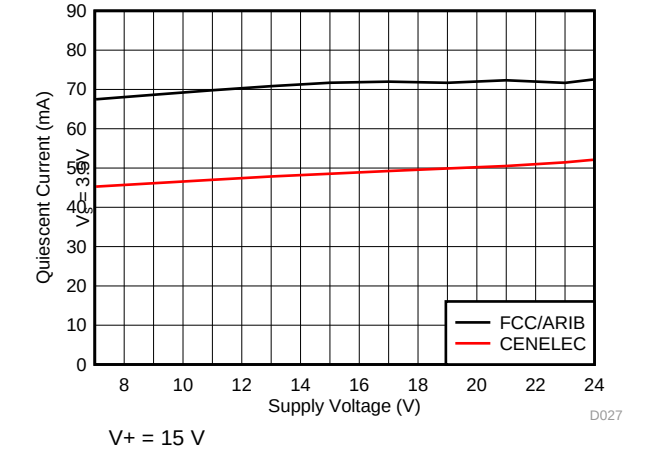


図 17. Iq vs Supply Voltage

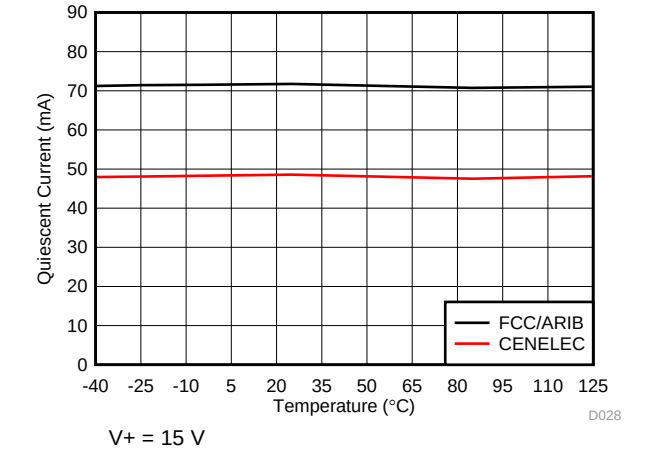


図 18. Iq vs Temperature

Typical Characteristics (continued)

At T_{CASE} = +25°C, V+ = 24 V, IN+ = (V+)/2, R_{LOAD} = 50 Ω unless otherwise noted.

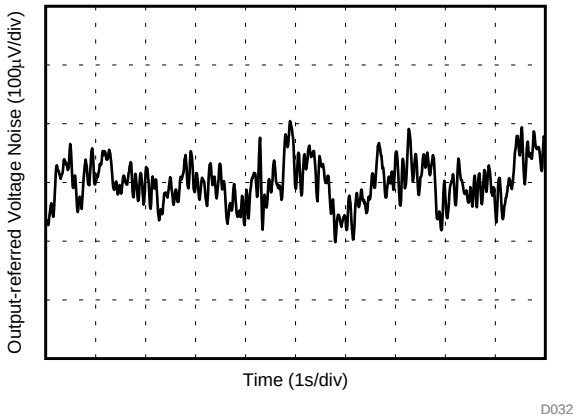


図 19. 0.1-Hz to 10-Hz Noise

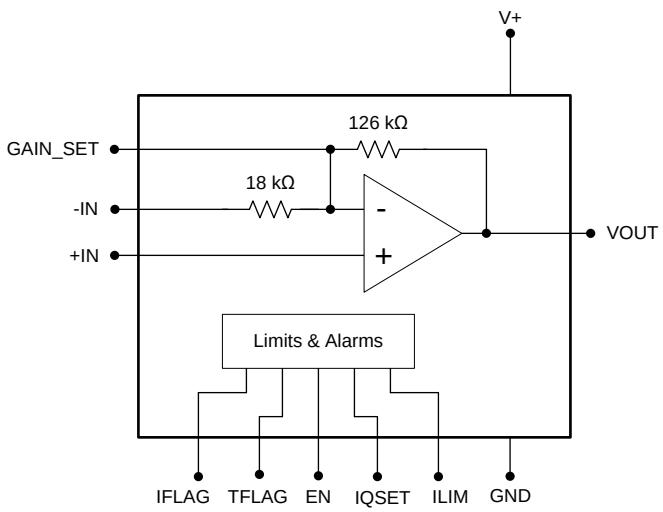
Copyright © 2018, Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

The OPA521 is a power amplifier (PA) designed for power-line communication (PLC) applications. The device features a fixed gain of –7 V/V, low-pass filter response, excellent linearity and low distortion through the bandwidth. The amplifier operates with 7-V to 24-V supplies, and can deliver up to ±1.9 A of continuous current from –40°C to +125°C.

7.2 Functional Block Diagram



7.3 Feature Description

The OPA521 offers an optional output current limit (ILIM), quiescent current (IQSET) selection pins, and a device enable pin. The IFLAG output alarm pin indicates an output current warning and the TFLAG alarm triggers when the internal temperature of the device forces the devices to shut down.

7.3.1 IQSET Pin

This pin sets the operating band of the amplifier by adjusting the quiescent current.

- IQSET > 2 V sets the device to operate in the FCC or ARIB bands
- IQSET < 0.8 V sets the device to operate in the CENELEC bands

7.3.2 EN Pin

When the transmitter is not in use, the output is disabled and placed in a high-impedance state when the EN pin decreases. For typical operation, connect the EN pin to 3.3 V. In disabled mode, the entire device draws 58 μA (typical) of current.

7.3.3 ILIM Pin Current Limiting

The ILIM pin (pin 12) provides a resistor-programmable output current limit. 図 6 shows the typical current limit for a given external R_{SET} resistor attached to this pin.

Several typical target values and the approximate corresponding R_{SET} are provided in 表 1.

表 1. Typical Current Limit and R_{SET} Values

CURRENT LIMIT (A)	R_{SET} (approximate, kΩ)
Maximum Output	Grounded
1	10
0.5	25

Copyright © 2018, Texas Instruments Incorporated

7.3.4 IFLAG and TFLAG Pins

The IFLAG and TFLAG pins are active-high, open-drain outputs that indicate if the OPA521 is in current or thermal limit. Connect these pins to 3.3 V through pullup resistors (for example 10 kΩ).

The maximum output current from the power amplifier is programmed with the external I_{LIM} resistor that is connected between ILIM (pin 12) and ground. IFLAG is set if the amplifier goes to a current limit state if a fault condition occurs. This causes the power amplifier to source or sink more current than the programmed limit value. IFLAG exhibits transient pulses under typical operation. An IFLAG true state for greater than 100 ms is a definite indication of a fault current condition.

The device contains internal thermal shutdown protection circuitry that automatically disables the output stage if the junction temperature exceeds 140°C. The device thermal shutdown protection circuitry lets the amplifier typical normal operation only when the junction temperature falls below 130°C. The TFLAG is active when the device is in thermal shut down mode.

7.4 Device Functional Modes

The OPA521 operates from a single power rail from 7 V to 24 V. The gain is fixed at –7 V/V and can increase with an external resistor that is connected to the GAIN_SET and –IN pins.

Copyright © 2018, Texas Instruments Incorporated

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The application circuit shown in 図 20 is an AC mains-line driver over 40-kHz-to-90-kHz utility band and is based around the European standard (EN56065–1) describing utility and consumer applications. This example shows a possible implementation for differential transmission on the mains line. This applications circuit is designed around the requirements of a domestic electricity meter operating over a utility band of 40 kHz to 90 kHz.

8.2 Typical Application

The impedance of the mains network at these signaling frequencies is relatively low (< 1 Ω to 30 Ω). This circuit has been designed to drive a 2-Ω mains line over the 40-kHz-to-90-kHz bandwidth. The signaling impedance of the mains network fluctuates as different loads are switched on during the day or over a season and it is influenced by many factors such as:

- Localized loading from appliances connected to the mains supply near to the connection of the communication equipment; for example, heavy loads such as cookers and immersion heaters and reactive loads such as EMC filters and power factor corrections.
- Distributed loading from consumers connected to the same mains cable, where their collective loading reduces the mains signaling impedance during times of peak electricity consumption; for example, meal times.
- Network parameters; for example, transmission properties of cables and the impedance characteristics of distribution transformers and other system elements.

With such a diversity of factors, the signaling environment fluctuates enormously, irregularly, and can differ greatly from one installation to another. Design the signaling system for reliable communications over a wide range of mains impedances and signaling conditions. Consequently, the transmitter must be able to drive sufficient signal into the mains network under these loading conditions.

The OPA521 amplifier has 1.9-A output drive capability with short-circuit protection; hence, it adequately copes with the high current demands required for implementing mains signaling systems.

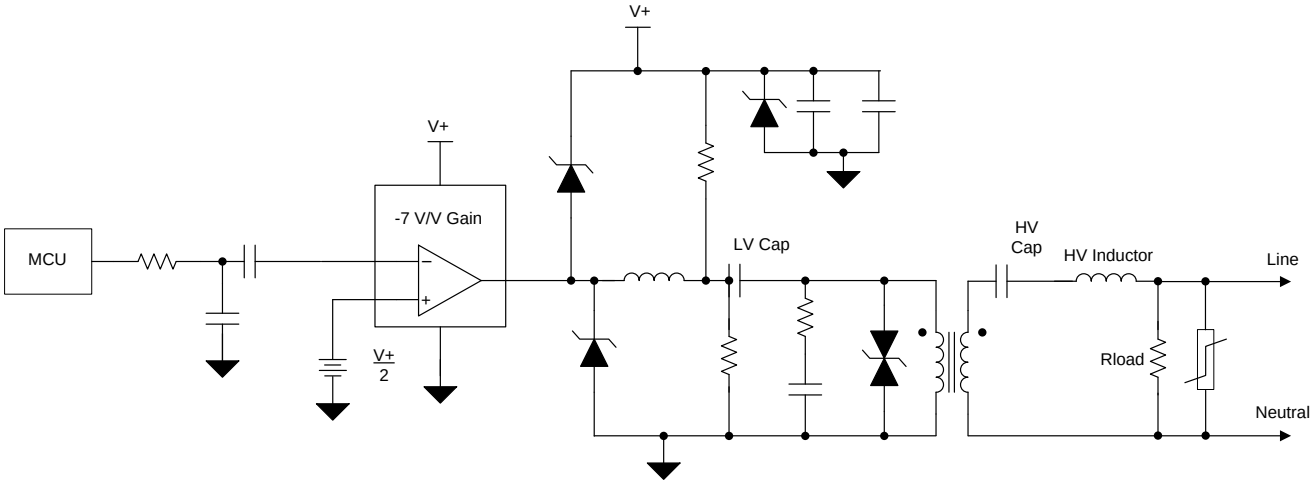


図 20. OPA521 Interface to the AC Mains

Typical Application (continued)

8.2.1 Design Requirements

The primary subsystems of a power-line communication mains-line driver system include the line coupling circuit, circuit protection, and power supply. The following sections detail the design of each.

8.2.2 Detailed Design Procedure

8.2.2.1 Interfacing the OPA521 to the AC Mains

The line coupling circuit is one of the most critical segments of a power-line modem. The line coupling circuit has two primary functions: first, to prevent the high voltage, low frequency of the mains (commonly 50 Hz or 60 Hz) from damaging the low-voltage modem circuitry; and second, as the name implies, to couple the modem signal to and from the ac mains.

8.2.2.1.1 Low-Voltage Capacitor

The low-voltage capacitor (LV Cap) couples the time-varying components of the power amplifier output signal into the line coupling transformer. The LV Cap must have a large enough capacitance to appear as a low impedance throughout the signal band of interest; 10-μF is a common value for signals in the range of 35 kHz to 150 kHz. The voltage rating of the LV cap should be sufficient to withstand the clamping voltage of the TVS diode (that is, the transient voltage suppressor (see Circuit Protection more information) operating under surge conditions. Generally, this limit must be equal to the power amplifier supply voltage or slightly higher.

8.2.2.1.2 High-Voltage Capacitor

The high-voltage capacitor (HV Cap) blocks the low-frequency mains voltage by forming a voltage divider with the winding inductance of the line coupling transformer. In many applications, a maximum reactive power (VA limit) on the HV Cap may be required. To meet this requirement, the HV Cap value is calculated by 式 1.

$$HV_{CAP} = \frac{VA_{LIMIT}}{V_{AC^2} \times 2\pi \times f} \tag{1}$$

For a 240-VAC, 50-Hz application with a 10-VA limit, the maximum value for the HV Cap is shown in 式 2.

$$HV_{CAP} \leq \frac{10}{240^2 \times 2\pi \times f} = 550\ \text{nF} \tag{2}$$

A 470-nF capacitor is frequently used in these types of applications. A metallized polypropylene electromagnetic interference and radio frequency interference (EMI/RFI) suppression capacitor is recommended because of the low loss factor associated with the dielectric, which results in minimal internal self-heating. Operating the capacitor at approximately 80% of its ac-rated voltage ensures a long component operating life. See Circuit Protection of this document for additional discussion on selecting the correct HV Cap value to withstand impulses on the mains.

8.2.2.1.3 Inductor

The inductor that is connected in series with the HV Cap is required when driving low line impedances and the HV Cap is restricted to approximately 470 nF for the reasons previously stated. In applications that operate in the CENELEC A band, the impedance of the 470-nF capacitance at 40 kHz is approximately 8.5 Ω. If the application requires the ability to drive a 2-Ω load, for example, this series impedance is restrictive. Adding the series inductor can mitigate this effect. To properly select the value of the inductance, the operating frequency range of the system must be known. A common example would be the PRIME frequency band, which is approximately 40 kHz to 90 kHz. Selecting the HV Cap and inductor to have a resonant frequency in the center of the frequency band is recommended, and results in a series inductor value of 12.8 μH and HV Cap value of 470 nF. The inductor must be sized to be capable of withstanding the maximum load current without saturation, using this 式 3 as a guideline.

$$L = \frac{1}{\left(HV_{CAP} \times 2\pi \times f\right)^2} \tag{3}$$

Copyright © 2018, Texas Instruments Incorporated

Typical Application (continued)

8.2.2.1.4 Line Coupling Transformer

Most power-line communication transformers are compact, with turns ratios between 1:1 and 4:1, low leakage inductance, and approximately 1-mH of winding inductance. It is the voltage divider formed by the HV Cap and winding inductance that divides down the ac mains voltage and reduces it to negligible levels at the modem output. 図 21 shows the equivalent circuit formed with the HV Cap and the line coupling transformer.

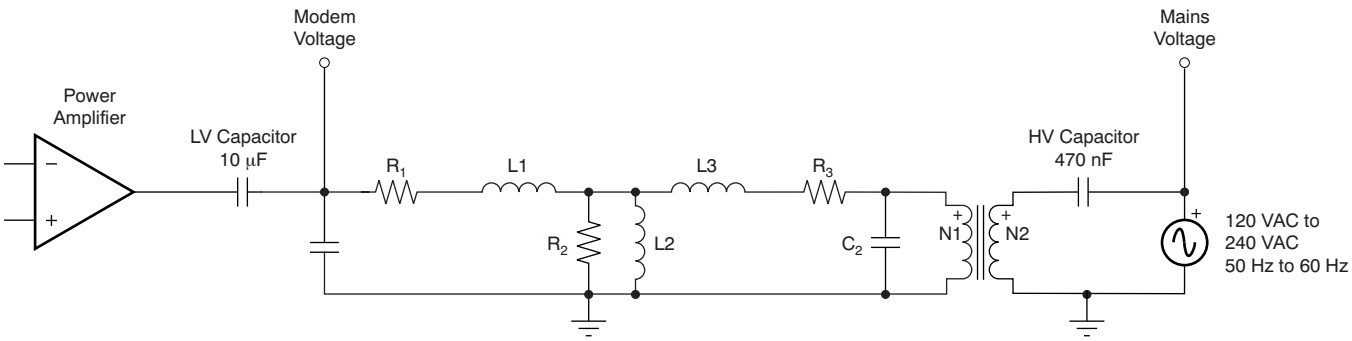


図 21. Voltage Divider with HV Cap and Transformer Equivalent Circuit

Where:

1. R1 is the series dc resistance of the primary winding
2. R2 is the shunt resistance reflecting losses in the core
3. R3 is the series dc resistance of the secondary winding, reflected to the primary side
4. L1 is the primary leakage inductance
5. L2 is the open circuit inductance of the primary winding
6. L3 is the secondary leakage inductance reflected to the primary side
7. C1 is the self-capacitance of the primary winding
8. C2 is the self-capacitance of the secondary winding reflected to the primary side

For the purposes of analysis, this circuit can be simplified as shown in 図 22.

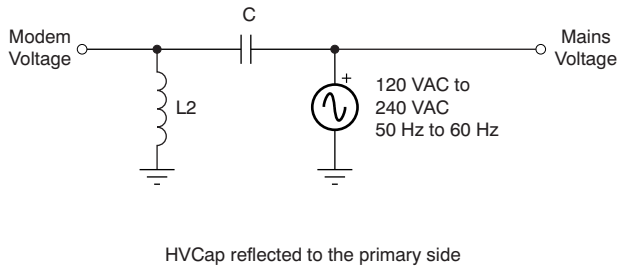


図 22. Simplified AC Mains Voltage Divider

Where:

1. L2 = OCL of the transformer primary
2. C = HV Cap reflected to the primary side

In a typical line coupling circuit the ac mains voltage injected into the modem is approximately 20 mVPP.

Determining the optimal turns ratio (N1/N2) for the power-line communication transformer is simple, and based on the principle of using the maximum output swing capability of the power amplifier together with the maximum output current capability of the power amplifier to achieve maximum power transfer efficiency into the load. Assuming the power-supply voltage and target load impedance are known, the turns ratio is determined as shown in Figure 17, and calculated with Equation 11 and Equation 12.

Copyright © 2018, Texas Instruments Incorporated

Typical Application (continued)

8.2.2.2 Circuit Protection

Power-line communications are often located in operating environments that are harsh for electrical components connected to the ac line. Noise or surges from electrical anomalies (such as lightning, capacitor bank switching, inductive switching, or other grid fault conditions) can damage high-performance integrated circuits if proper protection is not provided. The OPA521, however, can survive even the harshest conditions by using a variety of techniques to protect the device. Layout the protection circuitry in order to dissipate as much of the electrical disturbance as possible with a multilayer approach using metal-oxide varistors (MOVs), transient voltage suppression diodes (TVSs), Schottky diodes, and a Zener diode. These components dissipate the electrical disturbance before the anomaly reaches the device. shows the recommended strategy for transient overvoltage protection.

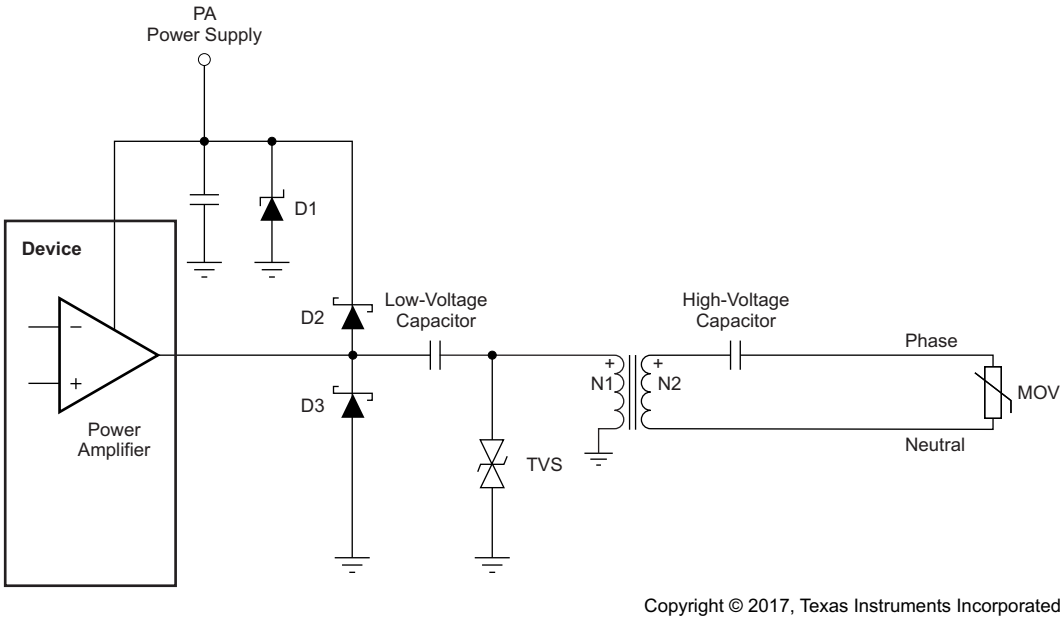


図 23. Transient Overvoltage Protection for OPA521

Note that the high-voltage coupling capacitor must be able to withstand pulses up to the clamping protection provided by the MOV. A metalized polypropylene capacitor, such as the 474MKP275KA from Illinois Capacitor, is rated for 50 Hz to 60 Hz and 250 VAC to 310 VAC, and can withstand 24 impulses of 2.5 kV. 表 2 lists several recommended transient protection components.

表 2. Recommended Transient Protection Components

COMPONENT	DESCRIPTION	MANUFACTURER	MFR PART NO (OR EQUIVALENT)
D1	Zener diode	Diodes, Inc.	1SMB59xxB
D2, D3	Schottky diode	Diodes, Inc.	1N5819HW
TVS	Transient voltage suppressor	Diodec Semiconductor	P6SMBJxxC
MOV	Varistor (for 120 VAC, 60 Hz)	LittleFuse	TMOV20RP140E
MOV	Varistor (for 240 VAC, 50 Hz)	LittleFuse	TMOV20RP300E
HV Cap	High-voltage capacitor	Illinois Capacitor, Inc	474MKP275KA

Copyright © 2018, Texas Instruments Incorporated

8.2.3 Application Curves

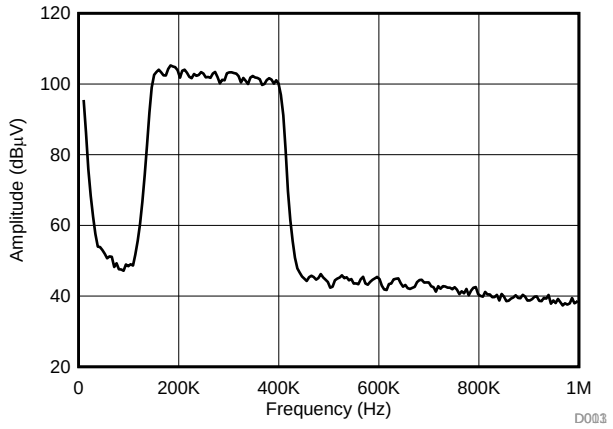


図 24. Measured ARIB Emissions

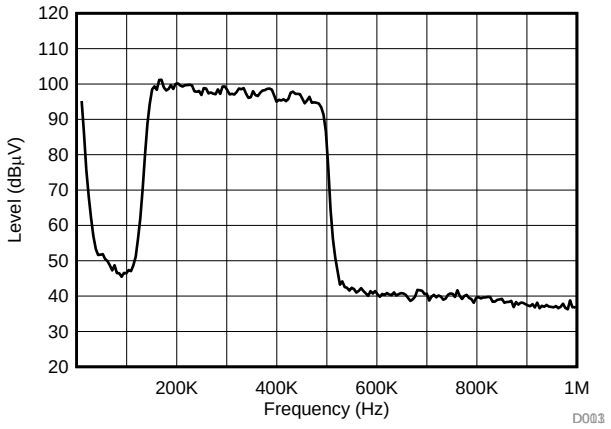


図 25. Measured FCC Emissions

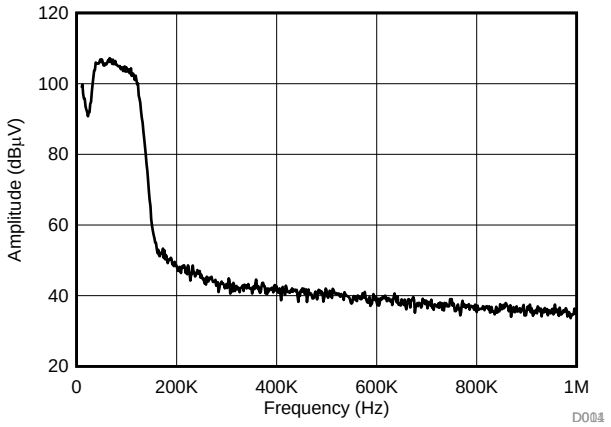


図 26. Measured CENELEC Emissions

9 Power Supply Recommendations

Determining the power-supply requirements requires only a straightforward analysis. The desired load voltage, load impedance, and available power-supply voltage or desired transformer ratio are all the parameters that must be known. In many power-line communication applications, such as PRIME, it is required to drive a 1-V_{RMS} signal into a 2-Ω load. Using 図 27, calculate the minimum power-supply voltage required by adding the peak-to-peak load voltage; the voltage dropped across the HV Cap and inductor, V2; the voltage dropped across the LV Cap, V1; and twice the output swing to rail limit of the power amplifier, VSWING. For FSK and SFSK systems, the peak to average ratio is √2, while for OFDM systems this ratio is approximately 3:1.

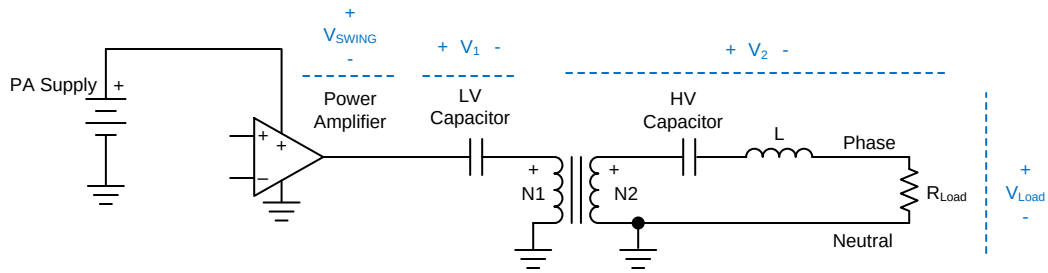


図 27. Typical Line Coupling Circuit

These ratios must be considered when performing calculations that relate the RMS voltages and peak voltages during an analysis. Choosing a large value for the LV Cap results in the voltage drop (V1) becoming negligible in most circumstances. The losses in the transformer are also negligible, even at high load currents, if the proper transformer with a low DCR is used. For FSK and SFSK systems, the voltage drop across the HV Cap and inductor, V2, is also usually negligible; in OFDM systems, because of the wider operating bandwidth, voltage drop V2 can be ignored and accounted for by using a 1.5× multiplier on the load voltage as an approximation.

注

This approximation is only valid with a load impedance of 2 Ω for PRIME and G3. Voltage drop V2 becomes negligible with increasing load impedance. These assumptions greatly simplify the analysis.

表 3. Power-Supply Requirements

PARAMETER	FSK OR SFSK	PRIME OR G3 OFDM	UNIT
Frequency range	63 to 74	35 to 95	kHz
R_{LOAD}	2	2	Ω
V_{LOAD}	1	1	V_{RMS}
V_{LOAD}	1.414	3	V_{PEAK}
V_{LOAD}	2.828	6	V_{PP}
OFDM multiplier	—	1.5	—
V_{SWING}	2	2	V
Turns ration, N1/N2	1.5	1.5	—
PA supply	8.25	17.5	V

表 3 summarizes the power-supply requirements for various power-line communication systems.

Example:

For PRIME or G3 using an OFDM signal with a 2-Ω load and 1-V_{RMS}load voltage:

$PA_{Supply} = V_{LOAD} \times$ OFDM Multiplier × Turns Ration + (2 × V_{SWING})

PA_{Supply} = 6 V × 1.5 × 1.5 + (2 × 2 V)

PA_{Supply} = 17.5 V

Power consumption

Copyright © 2018, Texas Instruments Incorporated

Calculating the power dissipation in the load and in OPA521 also requires some direct calculations. The desired load voltage, load impedance, available power-supply voltage, and the transformer ratio are the only parameters required. In many power-line communication applications, such as PRIME, it is required to drive a 1-VRMS signal into a 2-Ω load. The power dissipation in the power amplifier is determined by calculating the RMS value of the OPA521's output current, and the voltage difference between the power amplifier supply and RMS value of the output voltage. These two values are multiplied, and the quiescent power of the power amplifier is added.

The power in the load is given as 式 4 shows.

$$\text{PA output voltage (RMS)} = \frac{PA_{SUPPLY}}{2} + V_{LOAD_RMS} \times \frac{N_1}{N_2} \tag{4}$$

The power amplifier output current is given as calculated by 式 5.

$$\text{PA power dissipation} = \text{voltage drop across PA} \times PA_{IOUT_RMS} \tag{5}$$

Because the output of the power amplifier is always symmetric around PASupply/2, only the voltage difference between the amplifier supply and the RMS values of the PA output must be considered. 図 28 illustrates this concept for an OFDM signal. 表 4 shows example power dissipation values.

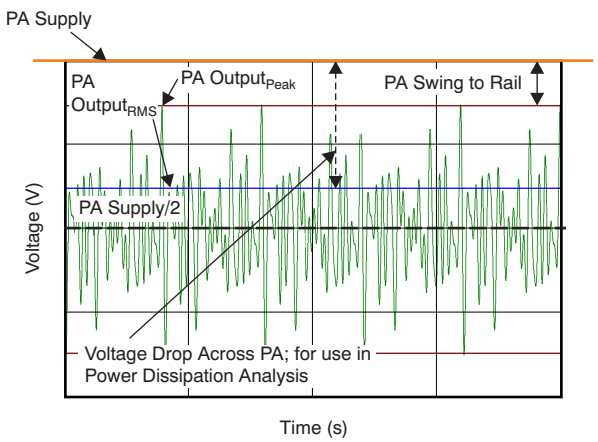


図 28. Typical OFDM Output Waveforms

表 4. Power Dissipation

PARAMETER	FSK OR SFSK	PRIME OR G3 OFDM	UNITS
Turns ration, N1/N2	1.5	1.5	-
R_{LOAD}	2	2	Ω
V_{LOAD}	1	1	V_{RMS}
I_{LOAD}	0.5	0.5	A_{RMS}
PA output voltage	6	10.75	V_{RMS}
Voltage drop across PA	3	6.25	V_{RMS}
PA output current	0.333	0.333	A_{RMS}
PA supply	9	17	V
PA power dissipation	1	2.1	W
Load power dissipation	0.5	0.5	W
Total	1.5	2.6	W

Copyright © 2018, Texas Instruments Incorporated

The power supply itself does not need to be designed to supply the peak power amplifier current continuously. The peak demand for current is supplied by the power-supply bypass capacitance. The power-supply voltage is shown in 図 29 on channel 2, along with the signal voltage at the 2-Ω load on channel 1.

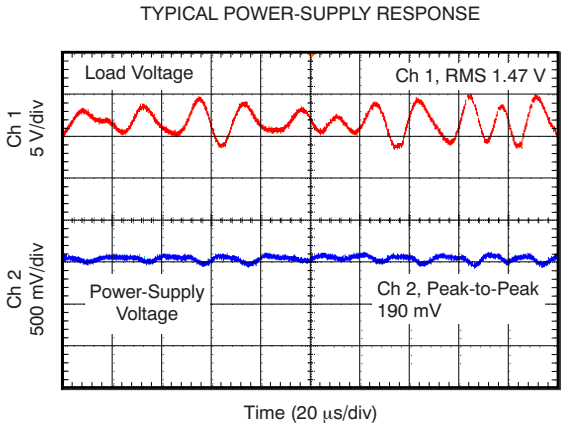


図 29. Typical Power-Supply AC Response

Two power-supply pins and two ground pins are available to provide a path for the high currents associated with driving the low impedance of the ac mains. Connecting the two supply pins together is recommended. Placing a 47-µF to 100-µF bypass capacitor in parallel with a 100-nF capacitor as close as possible to the device is also recommended. Care must be taken when routing the high-current ground lines on the PCB to avoid creating voltage drops in the PCB ground that may vary with changes in load current. /

Copyright © 2018, Texas Instruments Incorporated

10 Layout

10.1 Layout Guidelines

10.1.1 Thermal Considerations

In a typical power line communications application, the device dissipates 2 W of power when transmitting to the low-impedance AC line. This amount of power dissipation can increase the junction temperature, which can lead to a thermal overload that results in signal transmission interruptions if the PCB thermal design is not implemented properly. Proper management of heat flow from the device and good PCB design and construction are required to ensure proper device temperature, maximize performance, and extend the operating life of the device.

The device is assembled in a 5-mm × 5-mm, QFN-20 package. This QFN package has a large exposed thermal pad on the underside that conducts heat away from the device and to the underlying PCB.

Some heat is conducted from the silicon die surface through the plastic packaging material and is transferred to the ambient environment. However, this route is not the primary thermal path for heat flow because plastic is a relatively poor conductor of heat. Heat flows across the silicon die surface to the bond pads through the wire bonds to the package leads, to the top layer of the PCB. While these paths for heat flow are important, the majority (nearly 80%) of the heat flows downward through the silicon die to the thermally-conductive die-attach epoxy and to the exposed thermal pad on the underside of the package (as shown in 図 30). Minimizing the thermal resistance of this downward path to the ambient environment maximizes the life and performance of the device.

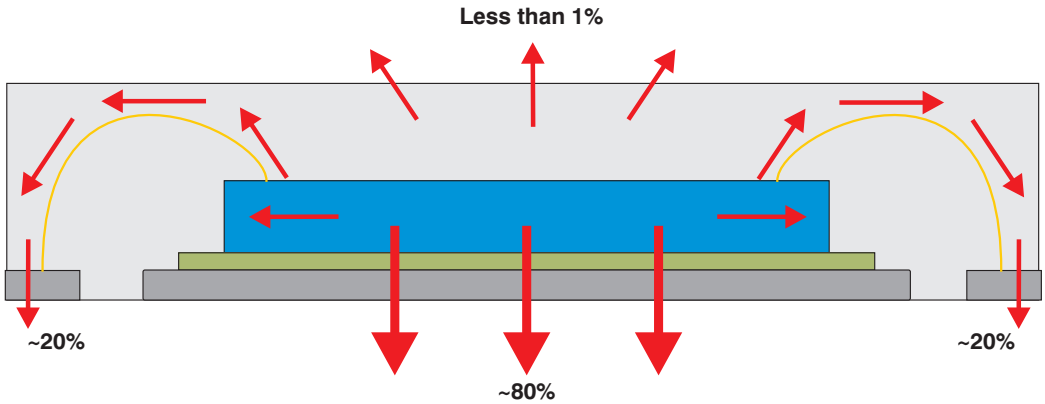


図 30. Heat Flow in the QFN Package

The exposed thermal pad must be soldered to the PCB thermal pad. The thermal pad on the PCB must be the same size as the exposed thermal pad on the underside of the QFN package. See *QFN/SON PCB Attachment* for recommendations on attaching the thermal pad to the PCB. 図 31 shows the direction of heat spreading to the PCB from the device.

Layout Guidelines (continued)

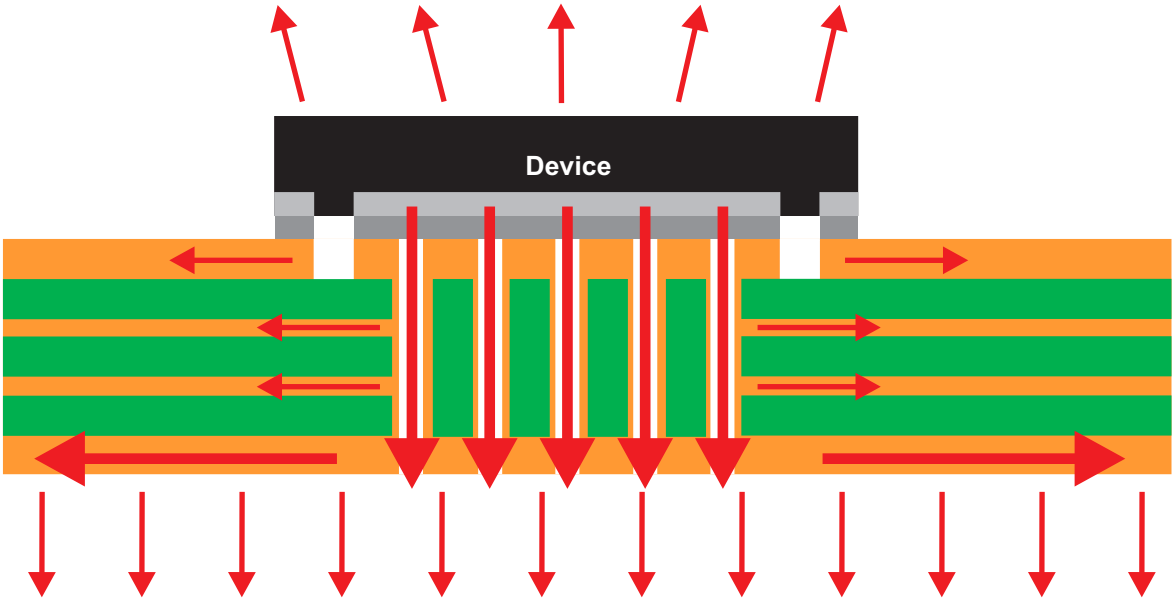


図 31. Heat Spreading to PCB

The heat spreading to the PCB is maximized if the thermal path is uninterrupted. Best results are achieved if the heat-spreading surfaces are filled with copper to the greatest extent possible, which maximizes the percentage of area covered on each layer. As an example, a thermally robust, multilayer PCB design consists of four layers with copper (Cu) coverage of 60% in the top layer, 85% and 90% in the inner layers (respectively), and 95% on the bottom layer.

Increasing the number of layers in the PCB, using thicker copper, and increasing the PCB area are all factors that improve the spread of heat. 図 32 through 図 34 show thermal resistance performance as a function of each of these factors.

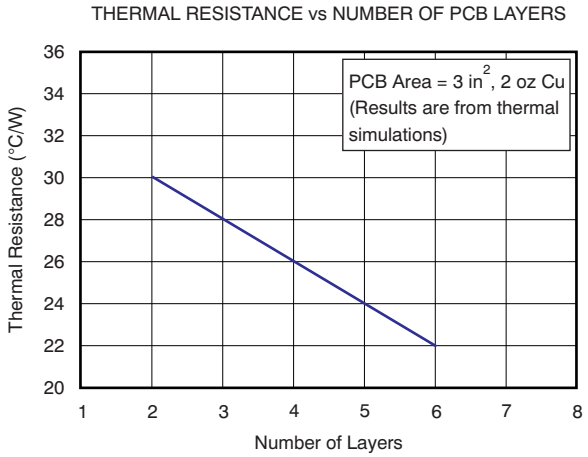


図 32. Thermal Resistance as a Function of the Number of Layers in the PCB

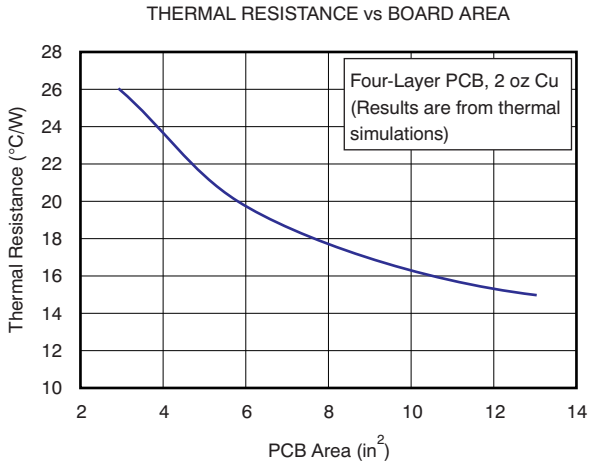


図 33. Thermal Resistance as a Function of PCB Area

Copyright © 2018, Texas Instruments Incorporated

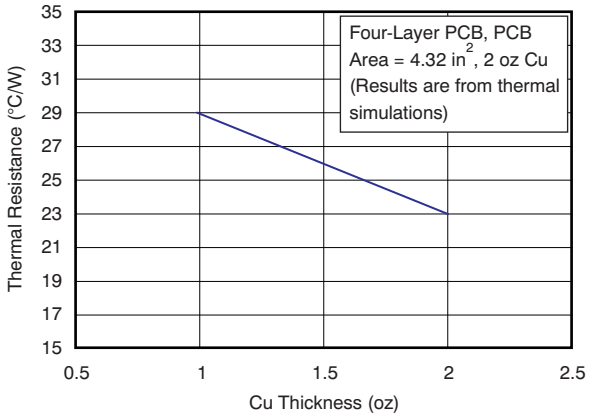


図 34. Thermal Resistance as a Function of Copper Thickness

For additional information on thermal PCB design using exposed thermal pad packages, see *PowerPAD™ Thermally-Enhanced Package* (available for download at www.ti.com).

10.2 Layout Example

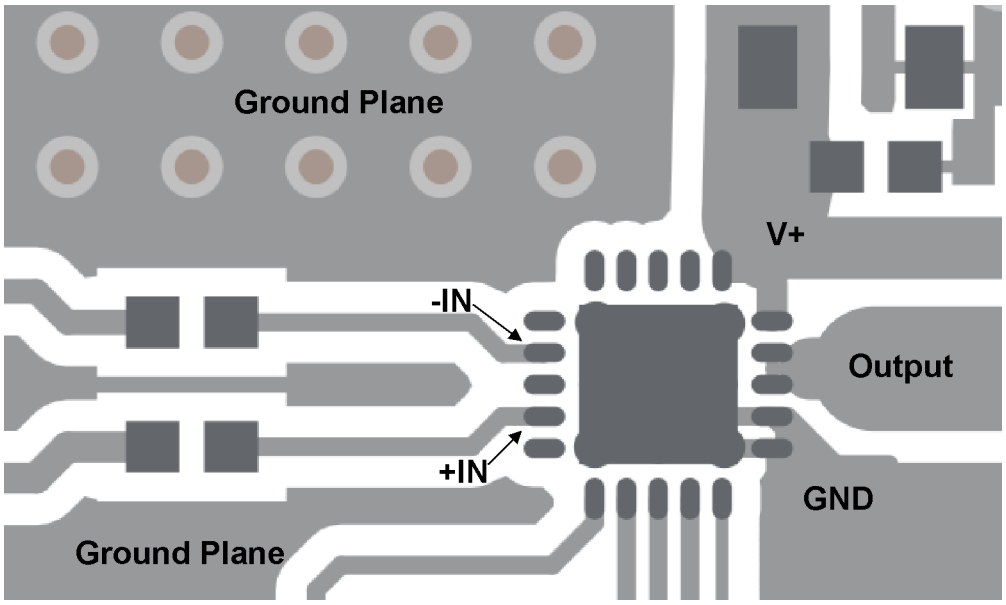


図 35. Recommended Layout for Typical Transformer Coupling Application

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*『放熱特性に優れたPowerPAD™パッケージ』*
- テキサス・インスツルメンツ、*『QFN/SONのPCB実装』*

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.5 商標

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

Copyright © 2018, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA521IRGWR	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 521
OPA521IRGWR.A	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 521
OPA521IRGWT	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 521
OPA521IRGWT.A	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 521

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

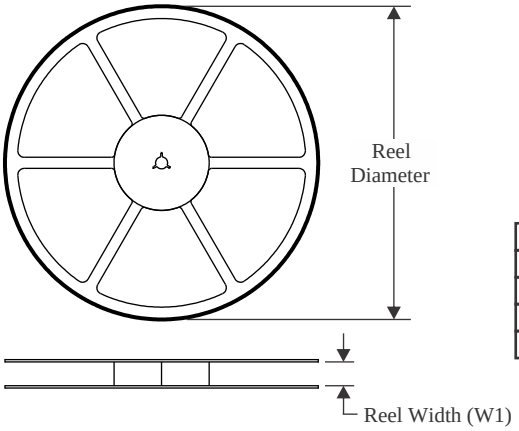
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

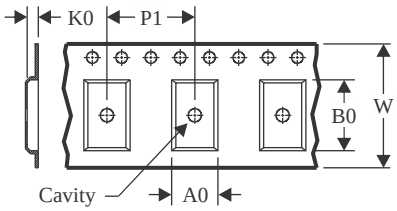
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

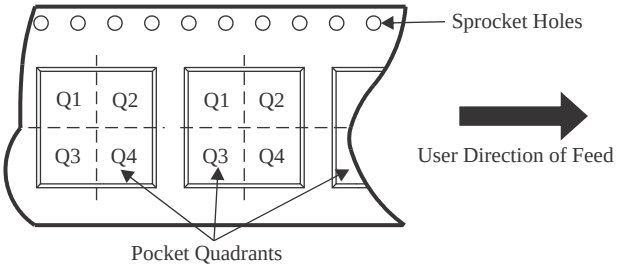


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

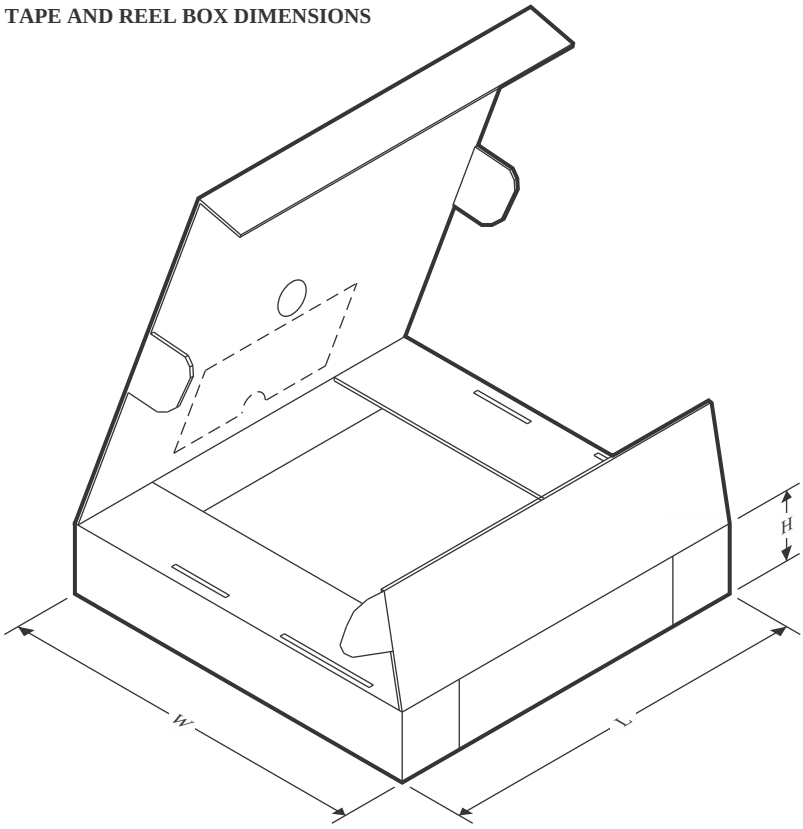
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA521IRGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
OPA521IRGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA521IRGWR	VQFN	RGW	20	3000	360.0	360.0	36.0
OPA521IRGWT	VQFN	RGW	20	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

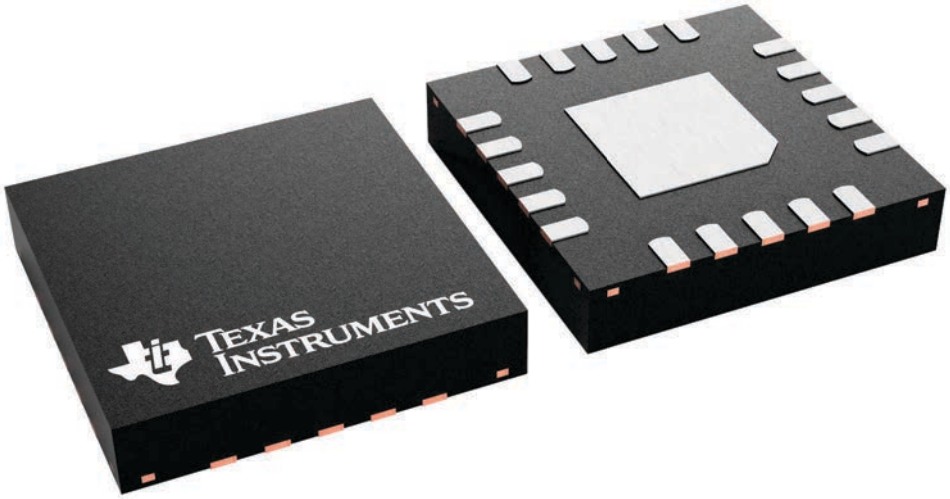
RGW 20

VQFN - 1 mm max height

5 x 5, 0.65 mm pitch

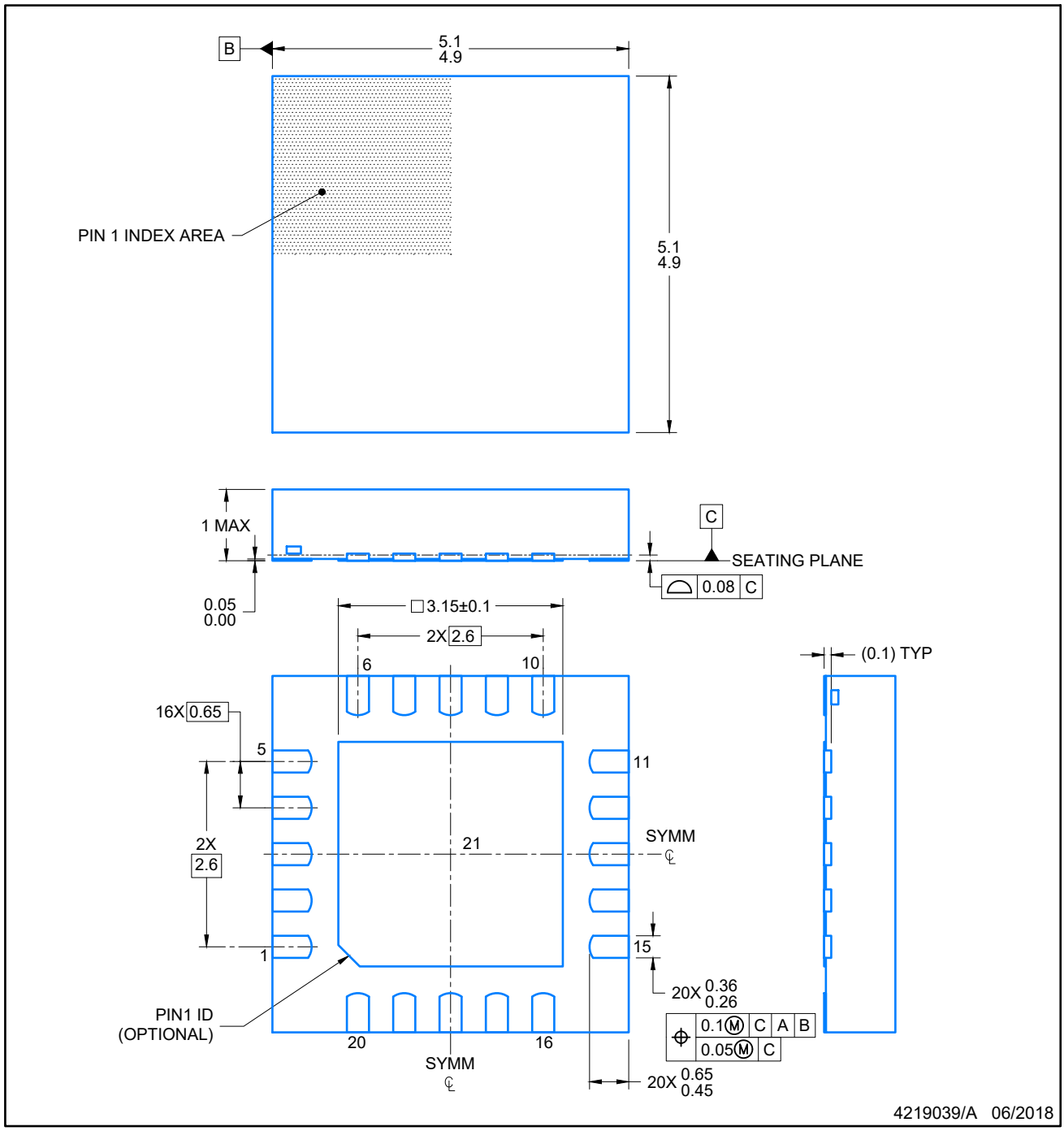
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



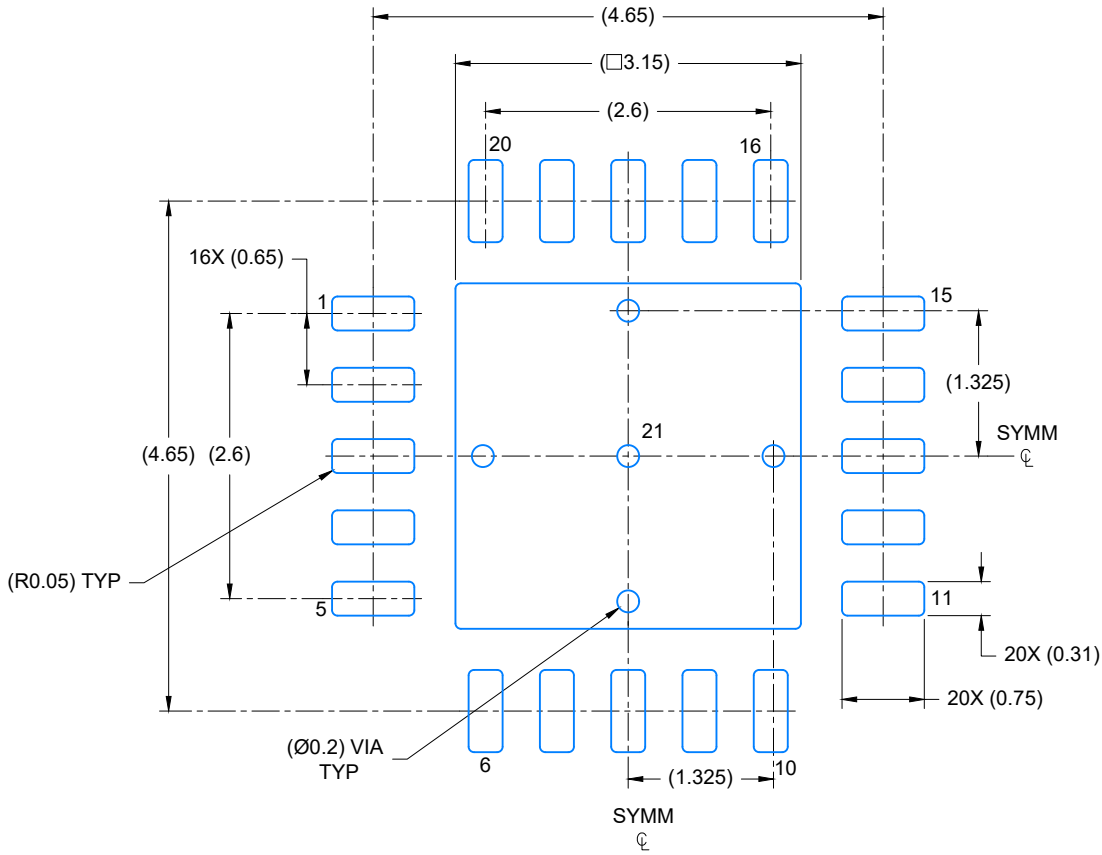
4227157/A

PLASTIC QUAD FLATPACK-NO LEAD



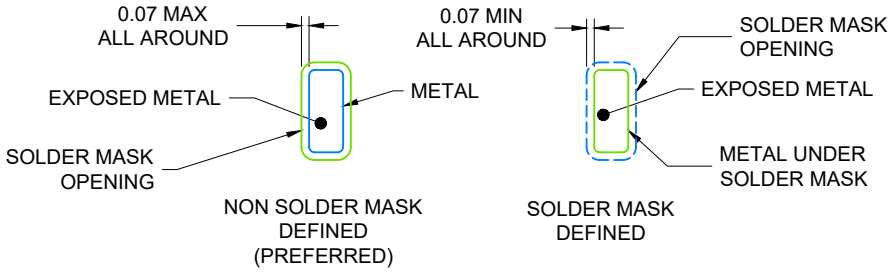
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 15X

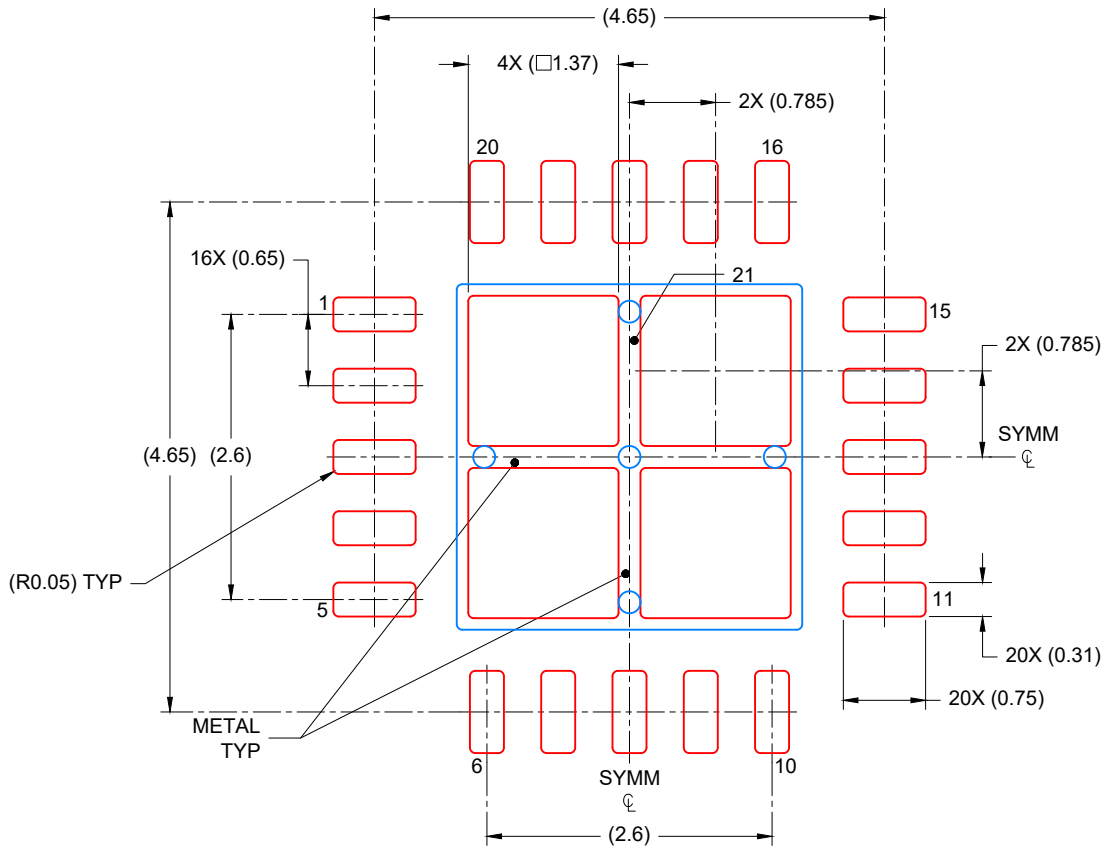


SOLDER MASK DETAILS

4219039/A 06/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 15X

4219039/A 06/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月