OPA561 大電流、高速オペアンプ

1 特長

- 1.2A の出力電流
- $12V_{PP}$ の出力電圧
- 広い電力範囲
  - シングル電源:7V～15V
  - デュアル電源:±3.5V～±7.5V
- 包括的な保護
  - サーマル・シャットダウン
  - 可変電流制限
- 出力ディセーブル制御
- 17MHz のゲイン帯域幅積
- 50V/µs のスルーレート
- 1MHz の フルパワー帯域幅
- 熱強化された HTSSOP-20 PowerPAD™ IC パッケージ
- 温度範囲:0℃～125℃

2 アプリケーション

- 電力線通信
- バルブ アクチュエータドライバ
- 電源
- 試験用機器
- TEC ドライバ
- レーザー ダイオード ドライバ

3 概要

OPA561 は、リアクティブな負荷に最大 1.2A のパルスを駆動できる、低コストでありながら大電流を制御できるオペアンプです。このモノリシック IC は、厳しい条件が要求される電力線搬送通信、レーザー ダイオード ドライバ、モーター制御アプリケーションで高い信頼性を実現します。また、高いスルーレートが、1MHz のフルパワー帯域幅と優れた直線性を提供しています。

設計の柔軟性を高めるため、OPA561 は 7V～15V の範囲のシングル電源、または ±3.5V～±7.5V のデュアル電源のいずれかで動作しており、シングル電源動作では入力同相範囲が接地よりも低い電位に対応できます。最大出力電流では、公称 15V 電源で出力信号の振幅が $12V_{PP}$ まで拡張できます。

OPA561 は、過熱状態および電流過負荷に対する保護回路を内蔵しており、その上、ユーザーが選択可能な高精度の電流制限機能を備えています。電流制限は、低消費電力の抵抗器やポテンショメータ、または DAC (D/A コンバータ) を使用して、0.2A～1.2A の範囲で調整できます。電流制御ループの高速特性により、パルス負荷の条件下でも高い精度を実現することができます。

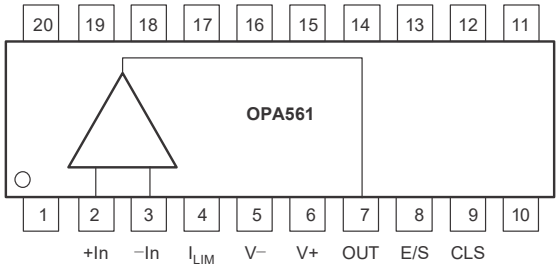
イネーブル / ステータス (E/S) ピンは、ピンを監視してデバイスがサーマル シャットダウン (アクティブ "Low") 状態にあるかどうかを判定する機能、強制的に "Low" 状態にして出力をディスエーブルにし負荷を切り離す機能の 2 つの機能を備えています。

OPA561 は小型の HTSSOP-20 PowerPAD IC パッケージで供給され、表面実装パッケージは熱強化されて、熱抵抗が非常に低くなっています。動作は産業用温度範囲に対応した 0℃～125℃ です。

パッケージ情報

部品番号	パッケージ(1)	パッケージ・サイズ(2)
OPA561	PWP (HTSSOP、20)	6.5mm × 6.4mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



HTSSOP−20

NOTE: Pins 1, 10, and 11−20 are not connected.
Flag must be connected to V−.

ピン配置図

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4 Pin Configuration and Functions

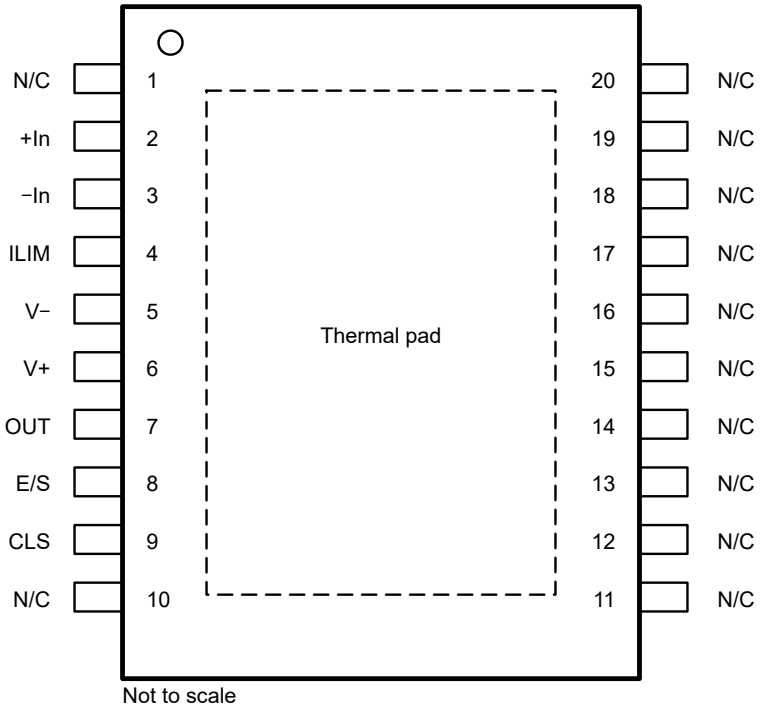


図 4-1. PWP Package, 20-Pin HTSSOP (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1	N/C	—	No electrical connection. Solder this pin to the printed circuit board (PCB).
2	+In	I	Noninverting input
3	–In	I	Inverting input
4	I_{LIM}	I	Adjustable current limit pin
5	V–	G	Negative supply
6	V+	P	Positive supply
7	OUT	O	Output
8	E/S	I/O	Enable and status pin
9	CLS	O	Overcurrent status flag
10-20	N/C	—	No electrical connection. Solder this pin to the printed circuit board (PCB).
Pad	Thermal pad	—	Connect the thermal pad to the most negative supply of the device, V–.

(1) I = input, O = output, G = ground, P = power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Supply voltage, V− to V+		16	V
	Input voltage	(V–) − 0.4	(V+) + 0.5	V
	Input shutdown voltage	(V–) − 0.4	(V–) + 0.5	V
	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Specified voltage	7	15	16	V
T_J	Specified junction temperature	0		125	°C

5.4 Thermal Information

THERMAL METRIC(1)			OPA561 PWP (HTSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	2-oz trace and 9-in^2 copper pad with solder	32	°C/W
		Without heat sink	100	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		1.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

at T_{CASE} = 25°C, V_S = 15 V, load connected to V/2, and E/S enabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE, V_S = 12 V						
V_{OS}	Input offset voltage	V_{CM} = 0 V		–3	±20	mV
dV_{OS}/dT	Input offset voltage vs temperature	T_A = 0°C to 125°C		±50		µV/°C
PSRR	Input Offset Voltage vs Power Supply	V_{CM} = 0 V, V_S = 7 V to 16 V		25	150	µV/V
INPUT BIAS CURRENT(1)						
I_B	Input bias current	V_{CM} = 0 V		10	100	pA
I_{OS}	Input offset current	V_{CM} = 0 V		10	100	pA
NOISE						
e_n	Input voltage noise density	f = 1 kHz		83		nV/√Hz
		f = 10 kHz		32		
		f = 100 kHz		14		
i_n	Current noise	f = 1 kHz		4		fA/√Hz
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage	Linear operation	(V–) – 0.1		(V+) – 3	V
CMRR	Common-mode rejection ratio	V_S = 15 V, V_{CM} = (V–) − 0.1 V to (V+) − 3 V	70	80		dB
INPUT IMPEDANCE						
	Differential			1.8×10^{11} || 10		Ω || pF
	Common-mode			1.8×10^{11} || 18.5		Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage Gain	V_O = 10 V_{PP}, R_L = 5 Ω	80	100		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	R_L = 5 Ω		17		MHz
SR	Slew Rate	G = 1, 10-V step, R_L = 5 Ω		50		V/µs
	Full-power bandwidth	G = +2, V_{OUT} = 10 Vp-p		1		MHz
	Settling time: ±0.1%	G = −1, 10-V step		1		µs
THD+N	Total harmonic distortion + noise	f = 1 kHz, R_L = 5 Ω, G = +2, V_O= 10 V_{PP}		0.02		%
		f = 1 MHz		3		
OUTPUT						
	Voltage output	Positive, I_O = 0.5 A	(V+) – 1	(V+) – 0.7		V
		Negative, I_O = –0.5 A	(V–) + 1	(V–) + 0.7		
		Positive, I_O = 1 A	(V+) – 1.5	(V+) – 1.2		
		Negative, I_O = –1 A	(V–) + 1.5	(V–) + 1.2		
	Maximum continuous current output, dc			1.2		A
Z_O	Output impedance	G = +2, f = 100 kHz		0.05		Ω
	Output current limit Range			±0.2 to ±1.2		A
	Current limit tolerance(2)	R_{CL} = 2 kΩ (I_{LIM} = ±1 A)		±50		mA
	Asymmetry	Comparing positive and negative limits		10		%

5.5 Electrical Characteristics (続き)

at T_{CASE} = 25°C, V_S = 15 V, load connected to V/2, and E/S enabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Current limit overshoot(3)	V = 5-V pulse (200 ns t_r), G = +2		50		%
	Output disabled	Output resistance		10		MΩ
		Output capacitance		140		pF
OUTPUT ENABLE/STATUS AND FLAG PINS						
	Shutdown input mode, $V_{E/S}$ high (output enabled)(4)	E/S pin open or forced high	(V−) + 2		(V−) + 5	V
	Shutdown input mode, $V_{E/S}$ low (output disabled)	E/S pin forced low	(V−) – 0.4		(V–) + 0.8	V
	Shutdown input mode, $I_{E/S}$ high (output enabled)	E/S pin indicates high		20		µA
	Shutdown input mode, $I_{E/S}$ low (output disabled)	E/S pin indicates low		0.1		µA
	Output disable time			50		ns
	Output enable time			3		µs
	Thermal shutdown status	Normal operation, sourcing 20 µA	(V–) + 2			V
		Thermally shutdown			(V–) + 0.8	
	Current limit status	Normal operation, sourcing 20 µA	(V–) + 0.8			V
		Current limit flagged			(V–) + 2	
	Junction temperature at shutdown			160		°C
	Reset temperature from shutdown			140		°C
POWER SUPPLY						
I_Q	Quiescent current	I_{LIM} connected to V−, I_Q = 0		50	60	mA
	Quiescent current vs temperature	T_A = 0°C to 125°C		60	70	mA
	Quiescent current in shutdown mode	I_{LIM} connected to V−			250	µA

(1) High-speed test at T_J = +25°C.
(2) See text for more information on current limit accuracy.
(3) Transient load transition time must be ≥ 200 ns.
(4) 402-kΩ pullup resistor to V+ can be used to permanently enable the OPA561.

5.6 Typical Characteristics

at T_{CASE} = 25°C, V_S = 15 V, and E/S enabled (unless otherwise noted)

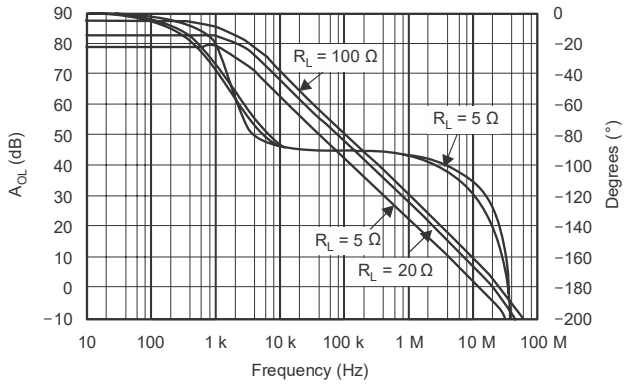


図 5-1. Gain and Phase vs Frequency

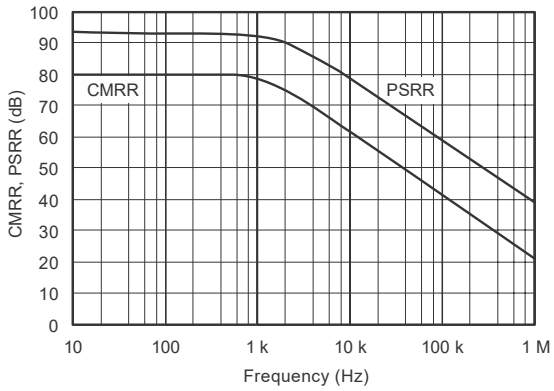


図 5-2. Common-Mode Rejection Ratio, Power-Supply Rejection Ratio vs Frequency

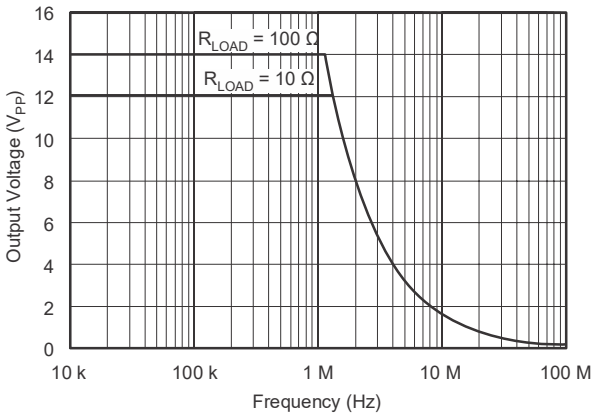
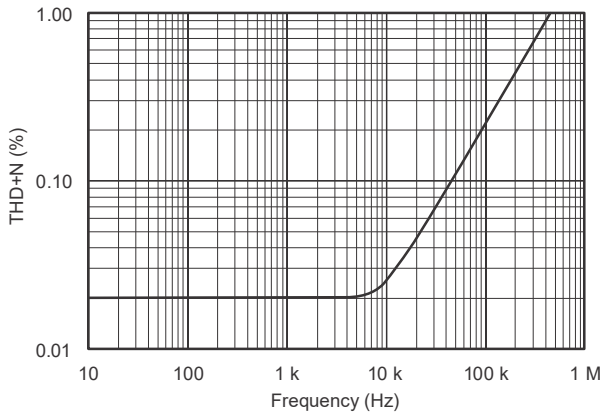


図 5-3. Maximum Output Amplitude vs Frequency



Unity gain follower, load = 5 Ω

図 5-4. Total Harmonic Distortion + Noise vs Frequency

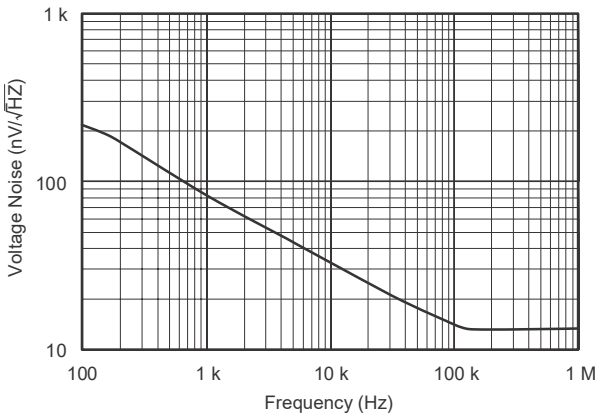


図 5-5. Input Voltage Spectral Noise vs Frequency

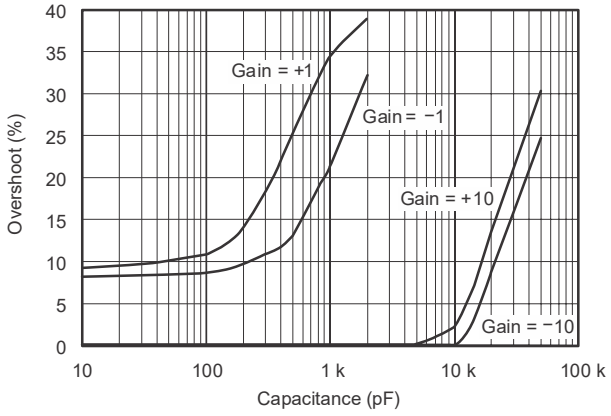


図 5-6. Small-Signal Overshoot vs Load Capacitance

5.6 Typical Characteristics (continued)

at T_{CASE} = 25°C, V_S = 15 V, and E/S enabled (unless otherwise noted)

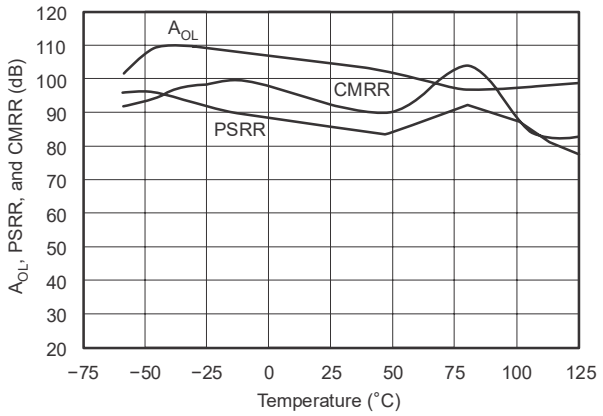


図 5-7. A_{OL}, PSRR, and CMRR vs Temperature

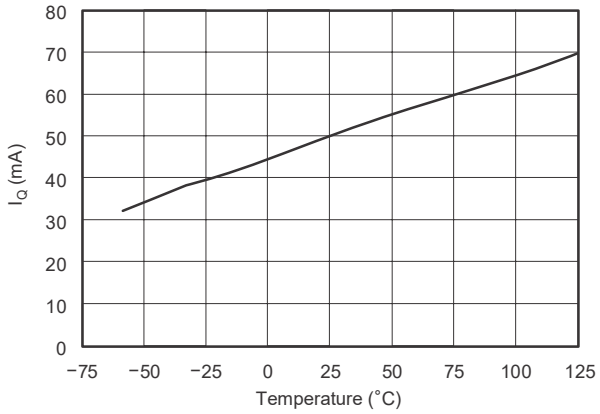


図 5-8. I_Q vs Temperature

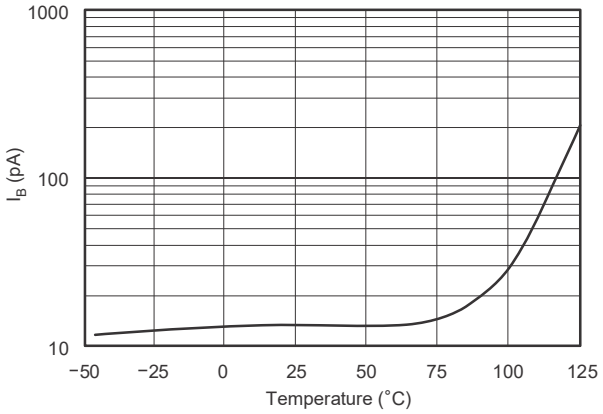


図 5-9. I_B vs Temperature

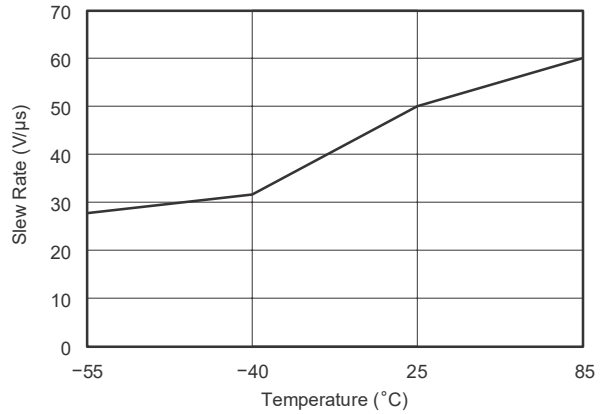


図 5-10. Slew Rate vs Temperature

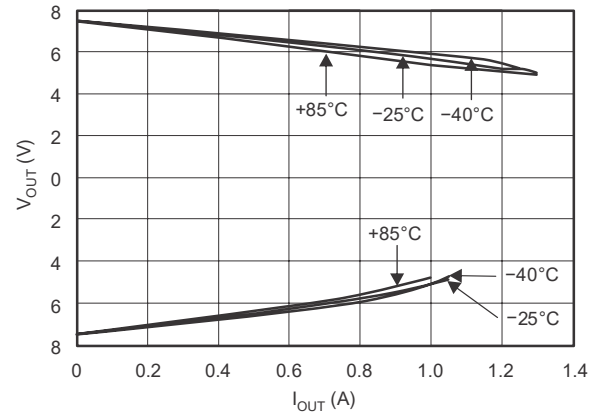


図 5-11. Output Voltage Swing vs Output Current

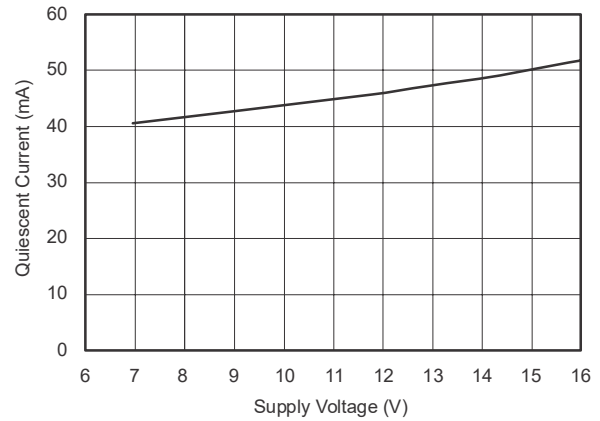


図 5-12. Quiescent Current vs Supply Voltage

5.6 Typical Characteristics (continued)

at T_{CASE} = 25°C, V_S = 15 V, and E/S enabled (unless otherwise noted)

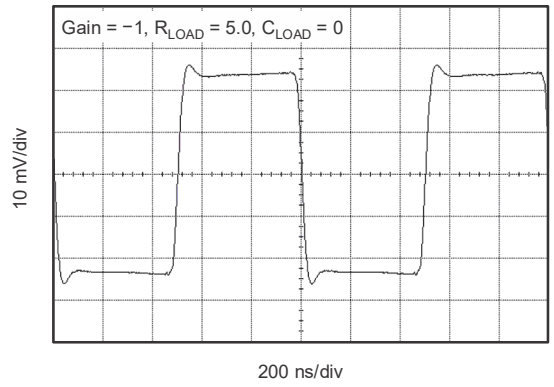


図 5-13. Small-Signal Step Response

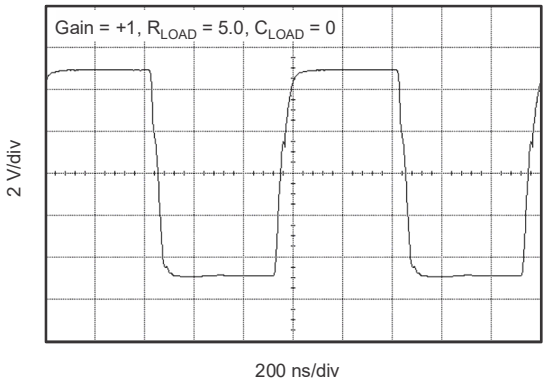
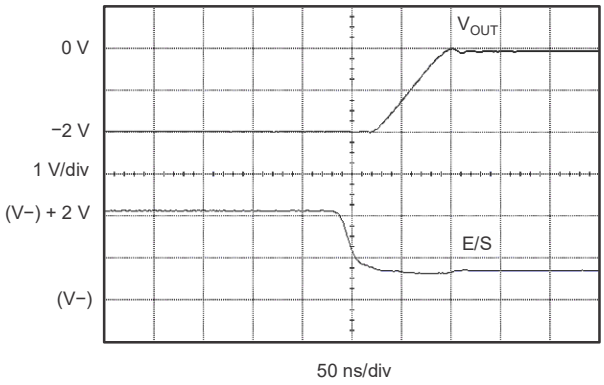
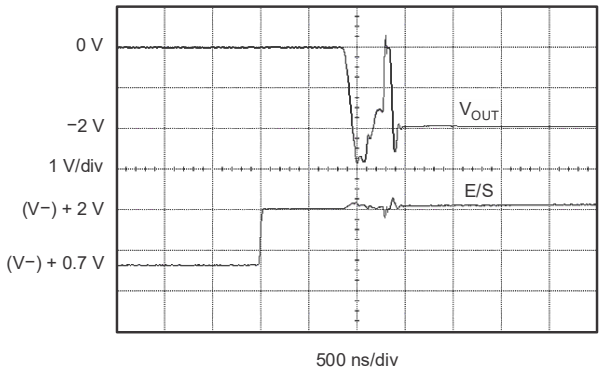


図 5-14. Large-Signal Step Response



R_L = 5 Ω

図 5-15. Shutdown Response



R_L = 5 Ω

図 5-16. Enable Response

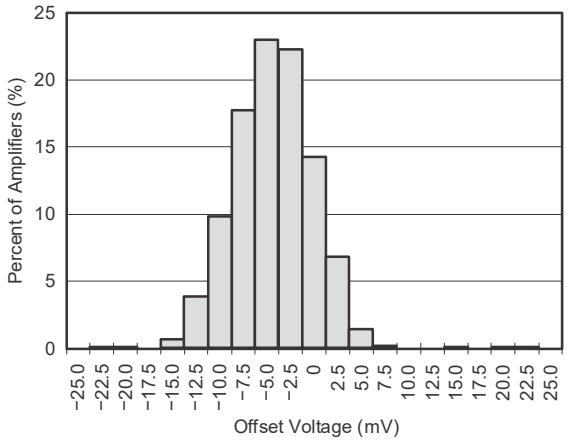


図 5-17. Offset Voltage Production Distribution

6 Detailed Description

6.1 Overview

The OPA561 is a monolithic low-cost, high-current operational amplifier capable of driving up to 1.2 A pulses into reactive loads. The amplifier is designed to provide high slew rate, which results in 1-MHz full-power bandwidth and excellent linearity. The OPA561 operates from either a single supply in the range of 7 V to 15 V or dual power supplies of ±3.5 V to ±7.5 V for design flexibility.

6.2 Feature Description

6.2.1 Adjustable Current Limit

The OPA561 has an accurate, user-defined, current limit which can be set from 0.2 A to 1.2 A by controlling the input to the I_{LIM} pin. Unlike other designs that use a power resistor in series with the output current path, the OPA561 senses the load internally. This allows the current limit to be set with low-power components. In contrast, other designs require one or two expensive power resistors that can handle the full output current (1.2 A in this case).

6.2.1.1 Current Limit Accuracy

The OPA561 has separate circuits to monitor the positive and negative currents. Each output is compared to a single internal reference that is set by the external current limit resistor (or voltage). The OPA561 employs a patented circuit technique to achieve an accurate and stable current limit. The output current limit has an accuracy of up to 5% on the 1-A current limit. Due to internal matching limitations, the positive and negative current limits can be slightly different. However, the values are typically within 10% of each other.

6.2.1.2 Setting the Current Limit

Do not float the I_{LIM} pin or damage to the device is possible. Connect I_{LIM} directly to V− to program the maximum output current limit, typically 1.2 A. The simplest method for adjusting the current limit (I_{LIM}) uses a resistor or potentiometer connected between the ILIM pin and V− according to the following equation:

$$I_{LIM} = \left(\frac{1.2V}{R_{CL} + 10k\Omega}\right) \times 10{,}000 \quad (1)$$

This external resistor determines a small internal current which sets the desired output current limit. Alternatively, the output current limit can be set by applying a voltage to the I_{LIM} pin. 図 6-1 shows a simplified schematic of the OPA561 current limit.

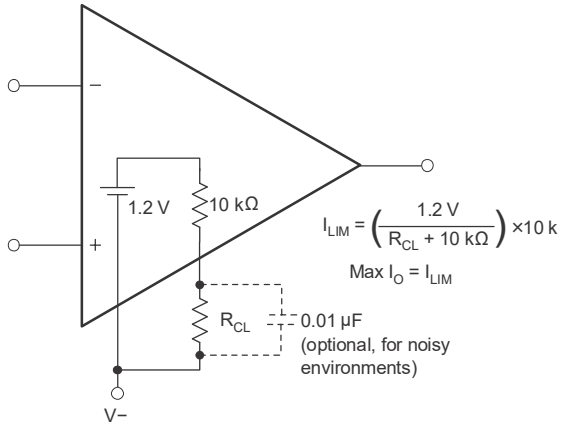


図 6-1. Adjustable Current Limit — Resistor Method

6.2.2 Enable-Status (E/S) Pin

The enable-status (E/S) pin provides two unique functions:

1. Output disable by forcing the pin LOW
2. Thermal shutdown indication by monitoring the voltage level at the pin

One or both of these functions can be used on the same device. For normal operation (output enabled), pull the E/S pin high (at least 2 V greater than V−). A small-value capacitor can be connected between the E/S pin and V− for noisy applications. To enable the OPA561 permanently, tie the E/S pin to V+ through a 402-kΩ pullup resistor.

6.2.2.1 Output Disable

The shutdown pin is referenced to the negative supply (V−). Therefore, shutdown operation is slightly different in single-supply and dual-supply applications. In single-supply operation, V− typically equals common ground. Therefore, the shutdown logic signal and the OPA561's shutdown pin are referenced to the same potential. In this configuration, the logic pin and the OPA561 enable can simply be tied together. Shutdown occurs for voltage levels of < 0.8 V. The OPA561 is enabled at logic levels > 2 V. In dual-supply operation, the logic pin is still referenced to a logic ground. However, the shutdown pin of the OPA561 is still referenced to V−. To shutdown the OPA561, the voltage level of the logic signal needs to be level shifted using an optocoupler, as shown in 図 6-2.

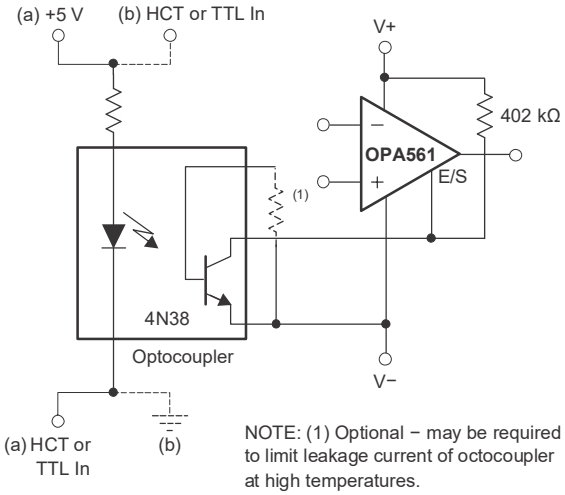


図 6-2. Shutdown Configuration for Dual Supplies

To disable the output, the E/S pin is pulled LOW, to no greater than 0.8 V above V−. This function can be used to conserve power during idle periods. The typical time required to shut down the output is 50 ns. To return the output to an enabled state, the E/S pin can be pulled to at least 2.0 V above V−. Typically, the output is enabled within 3 µs. Note that pulling the E/S pin HIGH (output enabled) does not disable the internal thermal shutdown.

6.2.2.2 Maintaining Microcontroller Compatibility

Not all microcontrollers output the same logic state after power-up or reset. 8051-type microcontrollers, for example, output logic-high levels on the ports, whereas other models power up with logic low levels after reset. In 図 6-2, configuration (a) the shutdown signal is applied on the cathode side of the photodiode within the optocoupler. A high logic level causes the OPA561 to be enabled, and a low logic level shuts down the OPA561. In 図 6-2, configuration (b), with the logic signal applied on the anode side, a high level causes the OPA561 to shut down, and a low level enables the op amp.

6.2.3 Overcurrent Flag

The OPA561 features an overcurrent status flag (CLS, pin 9) that can be monitored to see if the load exceeds the current limit. The output signal of the overcurrent limit flag is compatible to standard logic. The CLS signal is referenced to V−. A voltage level less than (V−) + 0.8 V indicates normal operation, and a level greater than (V−) + 2 V indicates that the OPA561 is current limited. The flag remains high as long as the output of the OPA561 current limited. At very low signal frequencies (typically < 1 kHz), both the upper (sourcing current) and lower (sinking current) current limits are monitored. At frequencies > 1 kHz, as a result of internal circuit limitations, the flag output signal for the upper current limit becomes delayed and shortened. The flag signal for the lower current limit is unaffected by this behavior. As the signal frequency increases further, only the lower current limit (sinking current) is output on pin 9.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

図 7-1 shows the OPA561 connected as a basic noninverting amplifier. However, the OPA561 can be used in virtually any op amp configuration. Reinforce power supply terminals with low series impedance capacitors. The technique of using a ceramic and tantalum type in parallel is recommended. Low series impedance power supply wiring is recommended.

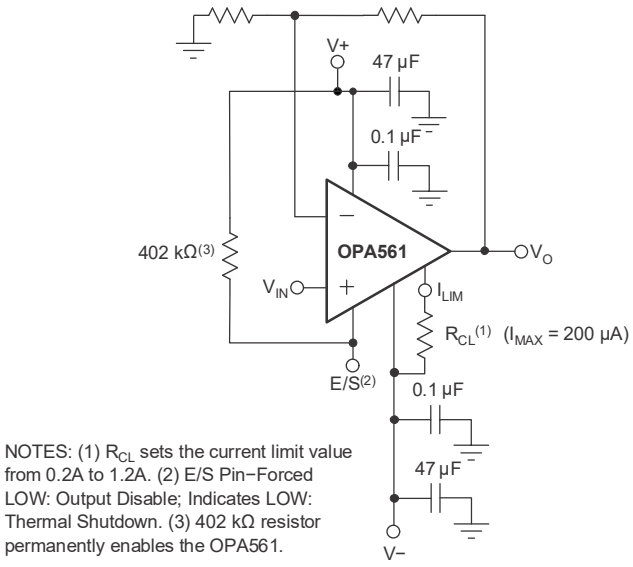


図 7-1. Basic Circuit Connections

7.1.1 Output Stage Compensation

The complex load impedances common in power op amp applications can cause output stage instability. For normal operation, output compensation circuitry is typically not required. However, if the OPA561 is intended to be driven into current limit, implementing an R/C network (snubber) is recommended. A snubber circuit also helps to enhance stability when driving large capacitive loads (> 1000 pF) or inductive loads (motors, loads separated from the amplifier by long cables). Typically, 3 Ω to 10 Ω in series with 0.01 µF to 0.1 µF is adequate. Varying the component values can help with challenging load conditions.

7.1.2 Output Protection

Reactive and EMF-generation loads can return load current to the amplifier, causing the output voltage to exceed the power-supply voltage. This damaging condition can be avoided with clamp diodes from the output terminal to the power supplies, as shown in 図 7-2. Schottky rectifier diodes with a 3 A or greater continuous rating are recommended.

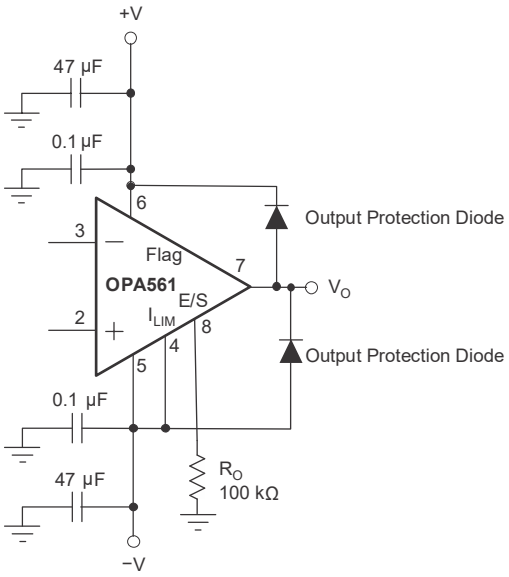


図 7-2. Output Protection Diode

7.1.3 Thermal Protection

The OPA561 has thermal sensing circuitry that helps protect the amplifier from exceeding temperature limits. Power dissipated in the OPA561 causes the junction temperature to rise. Internal thermal shutdown circuitry shuts down the output when the die temperature reaches approximately 160°C, resetting when the die has cooled to approximately 140°C. Depending on load and signal conditions, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the amplifier, but can have an undesirable effect on the load. Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable, long-term, continuous operation, limit the junction temperature to 125°C, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case loading and signal conditions. For good, long-term reliability, set the thermal protection to trigger at more than 35°C greater than the maximum expected ambient condition of your application. This configuration produces a junction temperature of 125°C at the maximum expected ambient condition. The internal protection circuitry of the OPA561 is designed to protect against overload conditions, and is not intended to replace a proper heat sink. Continuously running the OPA561 into thermal shutdown can degrade reliability. The E/S pin can be monitored to determine if shutdown has occurred. During normal operation the voltage on the E/S pin is typically greater than (V−) + 2 V. During shutdown, the voltage drops to less than (V−) + 0.8 V.

7.1.4 Power Dissipation

Power dissipation depends on power supply, signal, and load conditions. For DC signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor. Dissipation with ac signals is lower. The *Power Amplifier Stress and Power Handling Limitations* application bulletin explains how to calculate or measure power dissipation with unusual signals and loads, and can be downloaded from www.ti.com.

7.1.5 Heat-Sink Area

The relationship between thermal resistance and power dissipation can be expressed as:

$$\theta_{JA} = \frac{T_J - T_A}{P_D} \quad (2)$$

Where:

- T_J = Junction temperature (°C)
- T_A = Ambient temperature (°C)
- θ_{JA} = Junction-to-ambient thermal resistance (°C/W)
- P_D = Power dissipation (W)

Calculate the appropriate power dissipation to determine required heat-sink area. At the same time, consider the relationship between power dissipation and thermal resistance to minimize shutdown conditions and allow for proper long-term operation (junction temperature of 125 °C). After the heat-sink area has been selected, verify proper thermal protection by testing worst-case load conditions. For applications with limited board size, refer to 図 7-3 for the approximate thermal resistance relative to heat-sink area. Increasing heat-sink area beyond 2 in^2 provides little improvement in thermal resistance. To achieve the 32 °C/W stated in the *Electrical Characteristics*, a copper plane size of 9 in^2 was used. The HTSSOP-20 PowerPAD integrated circuit package is a good choice for continuous power levels from 2 W to 4 W, depending on ambient temperature and heat-sink area. Higher power levels can be achieved in applications with a low on-off duty cycle, such as remote meter reading.

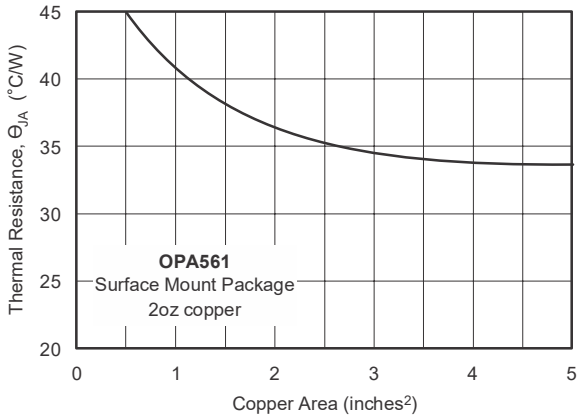


図 7-3. Thermal Resistance vs Circuit Board Copper Area

7.1.6 Amplifier Mounting

7.1.6.1 What is the PowerPAD™ Integrated Circuit Package?

The OPA561 uses the HTSSOP-20 PowerPAD integrated circuit package, a thermally enhanced, standard-size IC package designed to eliminate the use of bulky heat sinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard PCB assembly techniques, and can be removed and replaced using standard repair procedures.

The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC, as shown in 図 7-4. This provides an extremely low thermal resistance (θ_{JC}) path between the die and the exterior of the package. The thermal pad on the bottom of the IC must be soldered directly to the PCB, using the PCB as a heat sink. In addition, through the use of thermal vias, the thermal pad can be directly connected to a ground plane or special heat sink structure designed into the PCB.

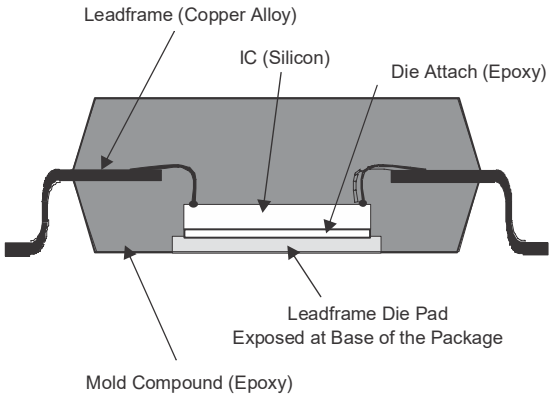


図 7-4. Section View of a PowerPAD Package

Soldering the thermal pad to the PCB is always recommended, even with applications that have low power dissipation. Soldering provides the necessary connection between the leadframe die and the PCB. Connect the thermal pad to the most negative supply of the device.

7.1.6.2 PowerPAD™ Integrated Circuit Package Assembly Process

1. Prepare the PCB with a top-side etch pattern, as shown in the attached *Thermal Land Pattern* mechanical drawing. Use etch for the leads as well as etch for the thermal land.
2. Place the recommended number of holes (or thermal vias) in the area of the thermal pad as shown on the attached *Land Pattern* mechanical. Use holes that are 13 mils in diameter. Keep the holes small so that solder wicking through the holes is not a problem during reflow.
3. Best practice is to place a small number of the holes under the package and outside the thermal pad area. These holes provide additional heat path between the copper land and ground plane and are 25 mils in diameter. The holes can be larger because the holes are not in the area to be soldered, so wicking is not a problem.
4. Connect all holes, including those within the thermal pad area and outside the pad area, to the internal ground plane or other internal copper plane.
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology; see 図 7-5. Web connections have a high thermal resistance that is useful for slowing the heat transfer during soldering operations. This heat-transfer slowing makes the soldering of vias that have plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, connect the holes under the PowerPAD package to the internal ground plane with a complete connection around the entire circumference of the plated through hole.
6. On the top-side solder mask, leave exposed the terminals of the package and the thermal pad area. On the thermal pad area, leave the 13 mil holes exposed. Cover the larger 25 mil holes outside the thermal pad area with solder mask.
7. Apply solder paste to the exposed thermal pad area and all of the package pins.
8. With these preparatory steps in place, the PowerPAD IC package is simply placed in position and run through the solder reflow operation, as with any standard surface-mount component. This procedure results in a part that is properly installed.

For detailed information on the PowerPAD IC package, including thermal modeling considerations and repair procedures, see the *PowerPAD Thermally Enhanced Package* technical brief, available at www.ti.com.

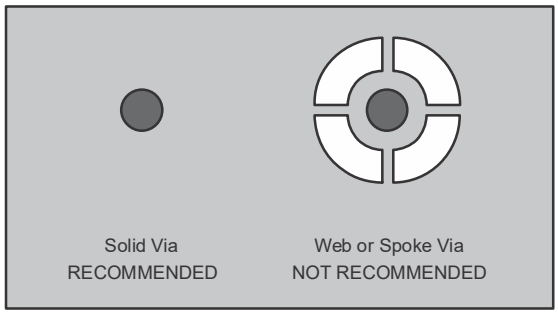


図 7-5. Via Connection

7.2 Typical Application

7.2.1 Laser Diode Driver

The high output current and low supply of the OPA561 makes this device a good candidate for driving laser diodes and thermoelectric coolers. 図 7-6 shows the OPA561 configured as a laser diode driver.

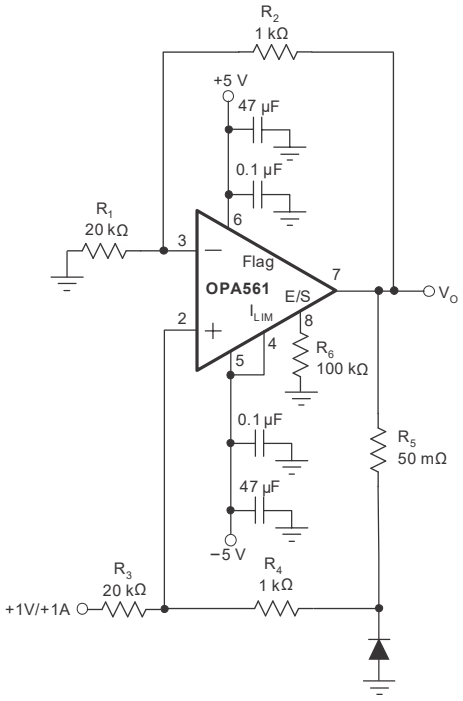


図 7-6. Laser Diode Driver

7.2.2 Programmable Power Supply

図 7-7 shows the OPA561 configured with the MSP430™ MCU, REF3030, and DAC7513 as a space-saving, low-cost, programmable power-supply design. This design features low-voltage operation, small-size packages, (DAC7513 in SOT23-8, REF3030 in SOT23-3) and low cost.

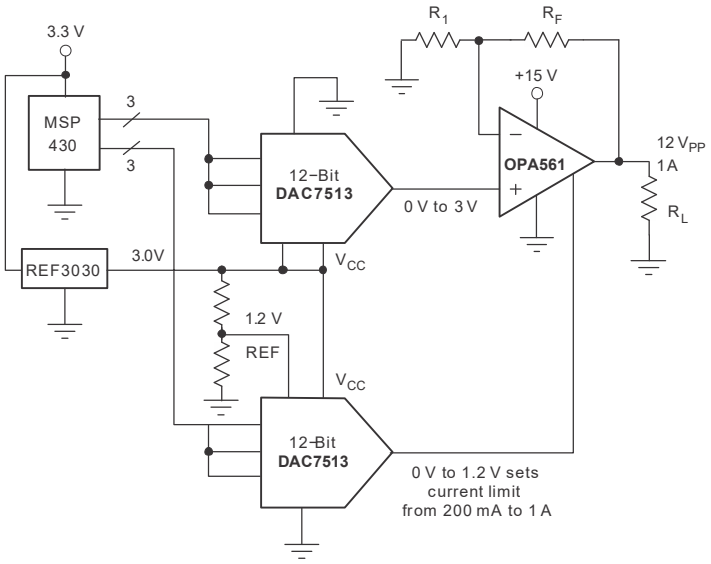


図 7-7. Programmable Power Supply

7.2.3 Power-Line Communication Modem

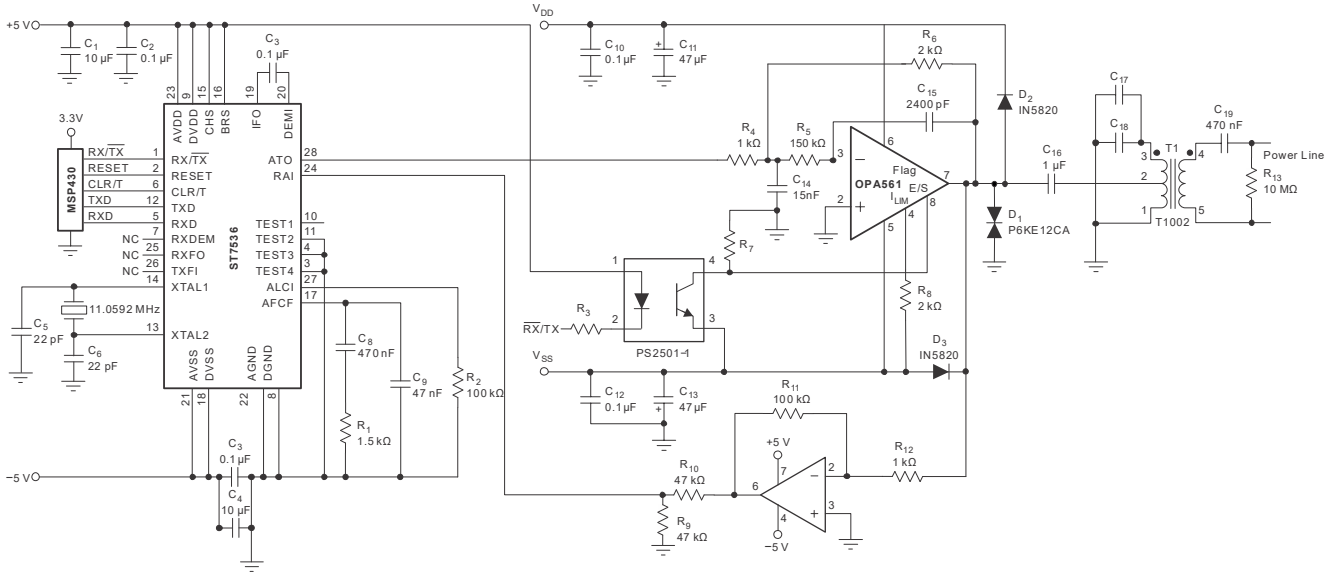


図 7-8. Power-Line Communication Driver

The OPA561 is an excellent choice to drive ac power lines for low-speed communication applications. The device provides an easily implemented, reliable option that is superior to discrete power transistor circuits. Advantages include:

1. Fully integrated device
2. Integrated shutdown circuitry for send-and-receive switching
3. Thermal shutdown
4. Adjustable current limit
5. Shutdown flag
6. Power savings
7. Small PowerPAD integrated circuit package

Typically such a system consists of a microcontroller, a modem IC and the power-line interface circuitry. See 図 7-8 for the half-duplex power line communication system.

The system uses a synchronous FSK-modem, capable of 600-baud and 1200-baud data rates, and supports two different FSK channels in the 60-kHz to 80-kHz range. A microcontroller such as the MSP430™ MCU is used to control the modem IC.

The OPA561 analog interface circuitry drives the FSK modem signals on the ac power line. The circuitry filters the transmit signal (ATO) from the ST7536 to suppress the 2nd-harmonic distortion of the transmit signal. The circuitry also amplifies the ATO signal and provides the very low output impedance necessary to properly drive the line. The impedance of a typical power line at 70-kHz ranges from 1 Ω to 100 Ω. The OPA561 is an excellent choice for this type of load. The transformer provides isolation and additional filtering. C9 prevents 50-Hz to 60-Hz current from flowing in the transformer. Choose this capacitor carefully for proper voltage rating and safety characteristics.

The receive input signal is amplified (G = 100) and applied to the modem IC. The OPA561 is disabled in receive mode to avoid loading the line.

7.3 Power Supply Recommendations

The OPA561 operates from single (7 V to 15 V) or dual (±3.5 V to ±7.5 V) supplies with excellent performance. Power-supply voltages do not need to be equal. For example, the positive supply can be set to 10 V with the negative supply at –5 V, or vice-versa. Most behaviors remain unchanged throughout the operating voltage range. Parameters that vary significantly with operating voltage are shown in the *Typical Characteristics*.

7.4 Layout

7.4.1 Layout Guidelines

The OPA561 is a high-speed power amplifier that requires proper layout for best performance. 図 7-9 shows an example of proper layout.

Keep power-supply leads as short as possible, which keeps inductance low and resistive losses at a minimum. A minimum 18-gauge wire thickness is recommended for power-supply leads. Use a wire length < 8 inches.

Proper power-supply bypassing with low-ESR capacitors is essential to achieve good performance. A parallel combination of small ceramic (around 100 nF) and larger (47 µF) nonceramic bypass capacitors provide low impedance over a wide frequency range. Place bypass capacitors as close as practical to the power-supply pins of the OPA561.

Keep PCB traces conducting high currents, such as from output to load or from the power-supply connector to the power-supply pins of the OPA561, as wide and as short as possible. This guideline helps keep inductance low and resistive losses to a minimum.

The holes in the landing pattern for the OPA561 are for the thermal vias that connect the thermal pad of the OPA561 to the heat sink area on the printed circuit board (see attached *Land Pattern* mechanical drawing). The additional larger vias further enhance the heat conduction into the heat-sink area. All traces conducting high currents are very wide for lowest inductance and minimal resistive losses. The negative supply (V−) pin on the OPA561 is connected through the thermal pad. This connection allows for maximum trace width for VOUT and the positive power supply (V+).

7.4.2 Layout Example

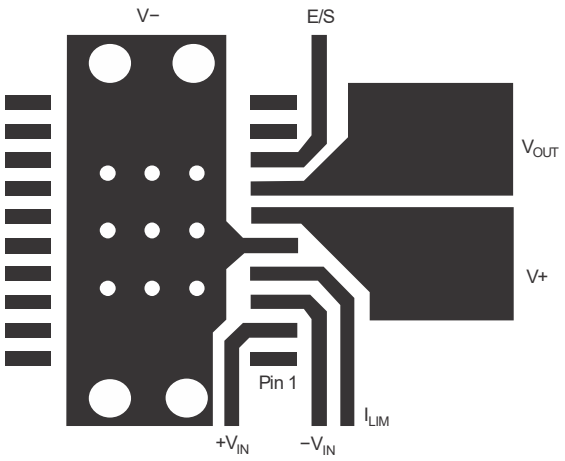


図 7-9. OPA561 Example Layout

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device Support

8.1.1 サード・パーティ製品に関する免責事項

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8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

8.4 Trademarks

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8.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (February 2007) to Revision F (October 2023)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• 「パッケージ情報」の表、「ピン構成および機能」セクション、「仕様」セクション、「ESD 定格」セクション、「推奨動作条件」セクション、「熱に関する情報」セクション、「詳細説明」セクション、「概要」セクション、「機能説明」セクション、「アプリケーションと実装」セクション、「代表的なアプリケーション」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1
• データシート全体にわたって最低動作温度を -40℃ から 0℃ に変更	1
• Updated input offset voltage typical value in *Electrical Characteristics*	5
• Updated to correct unit in Figure 6-11, *Output Voltage Swing vs Output Current*	7
• Updated to correct unit in Figure 6-17, *Offset Voltage Production Distribution*	7
• Added "approximately" to text referring to thermal protection behavior	14
• Added missing Equation 2	15

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA561PWP	Last Time Buy	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	OPA561
OPA561PWP.B	Last Time Buy	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	OPA561
OPA561PWP/2K	Last Time Buy	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	OPA561
OPA561PWP/2K.B	Last Time Buy	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	OPA561

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

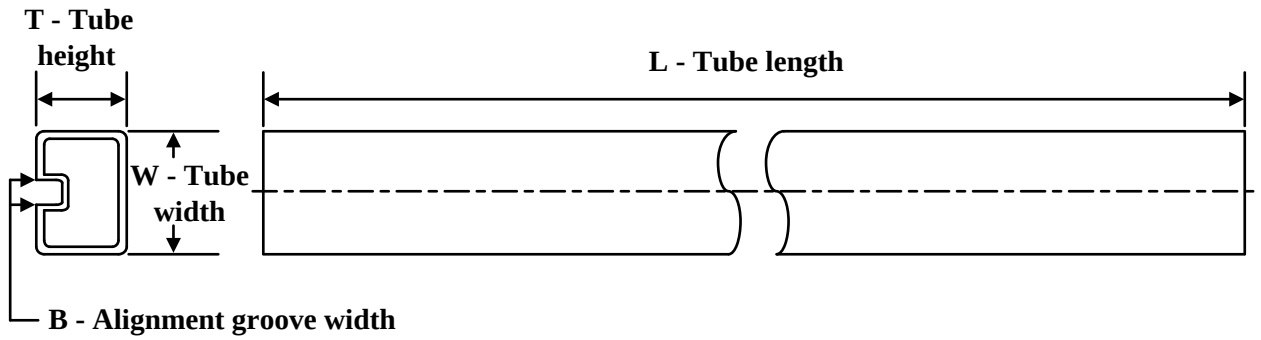
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA561PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
OPA561PWP.B	PWP	HTSSOP	20	70	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

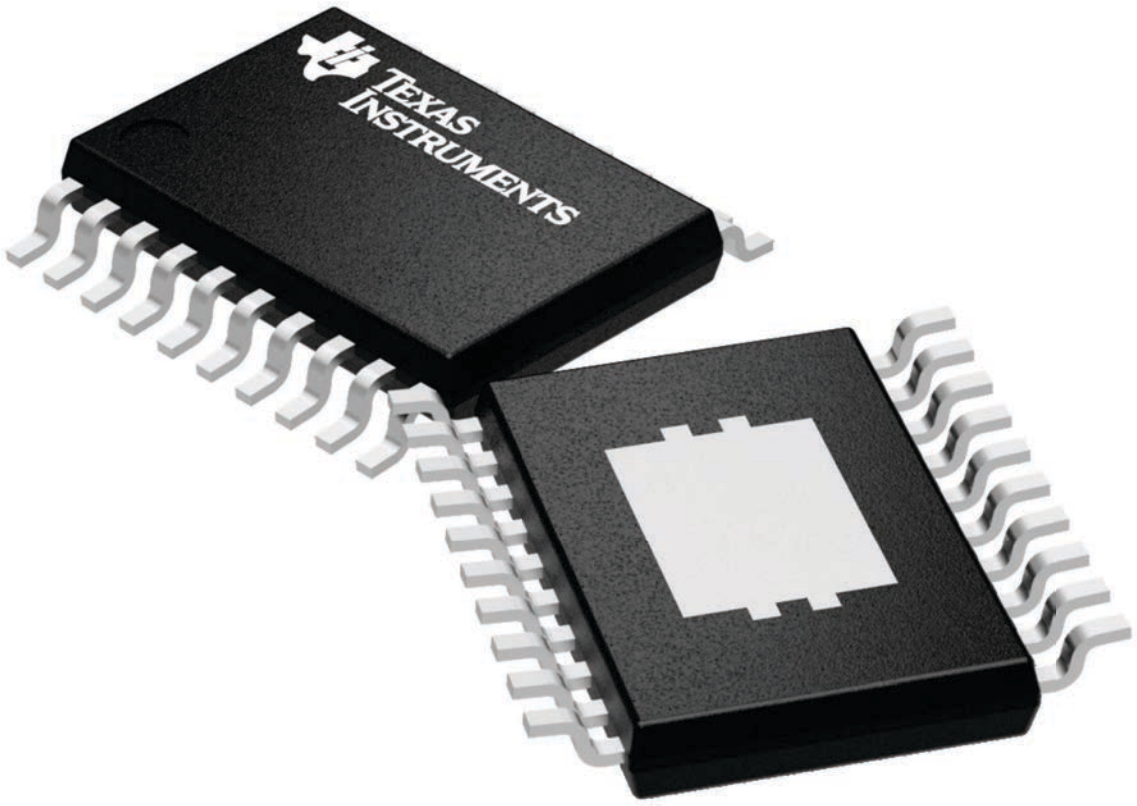
PWP 20

HTSSOP - 1.2 mm max height

6.5 x 4.4, 0.65 mm pitch

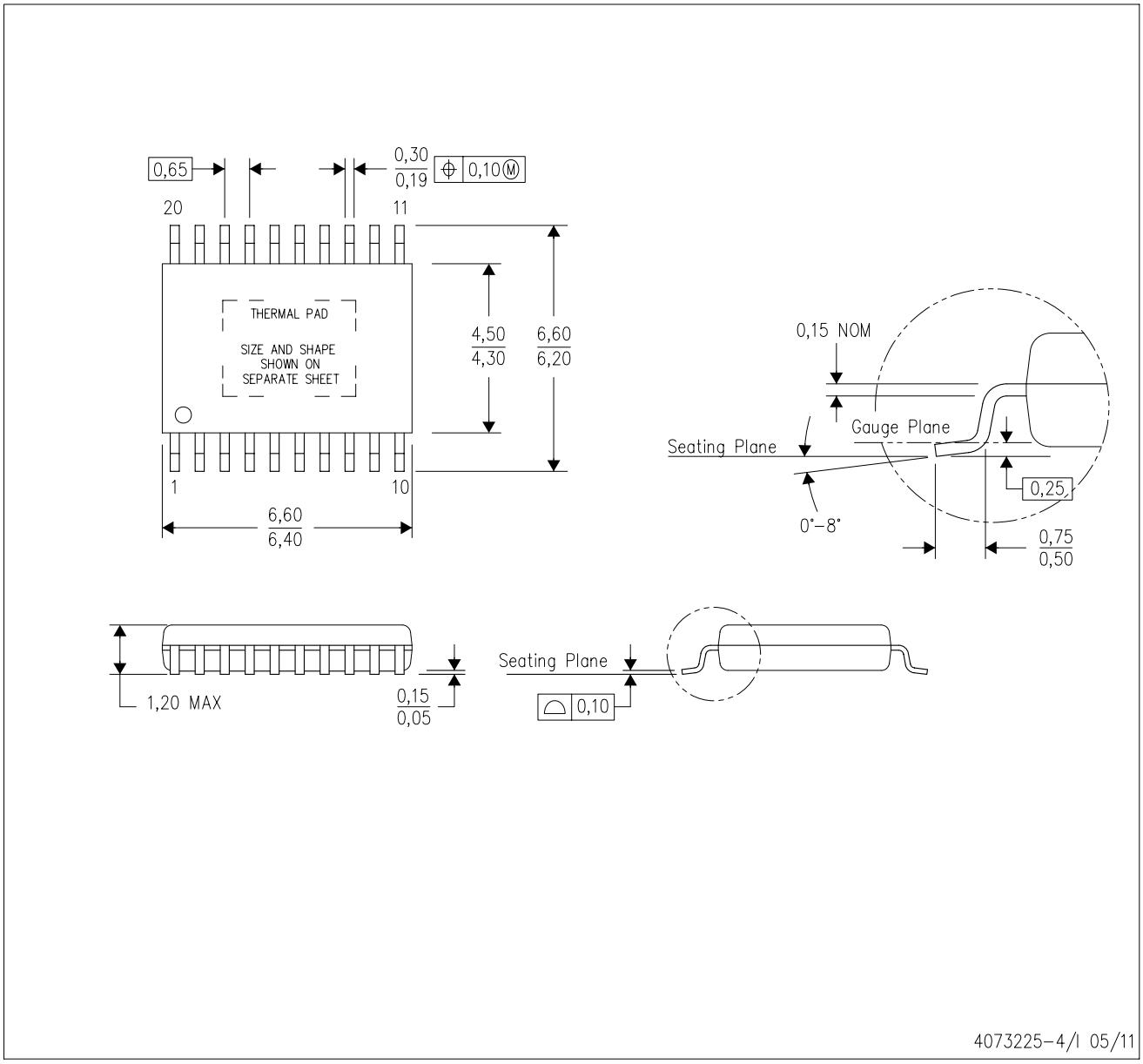
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

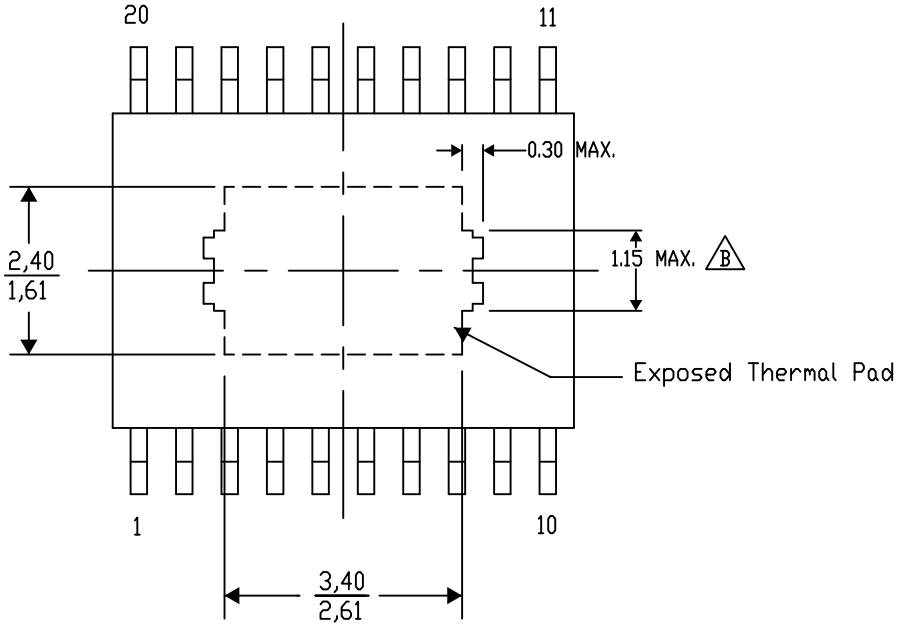
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

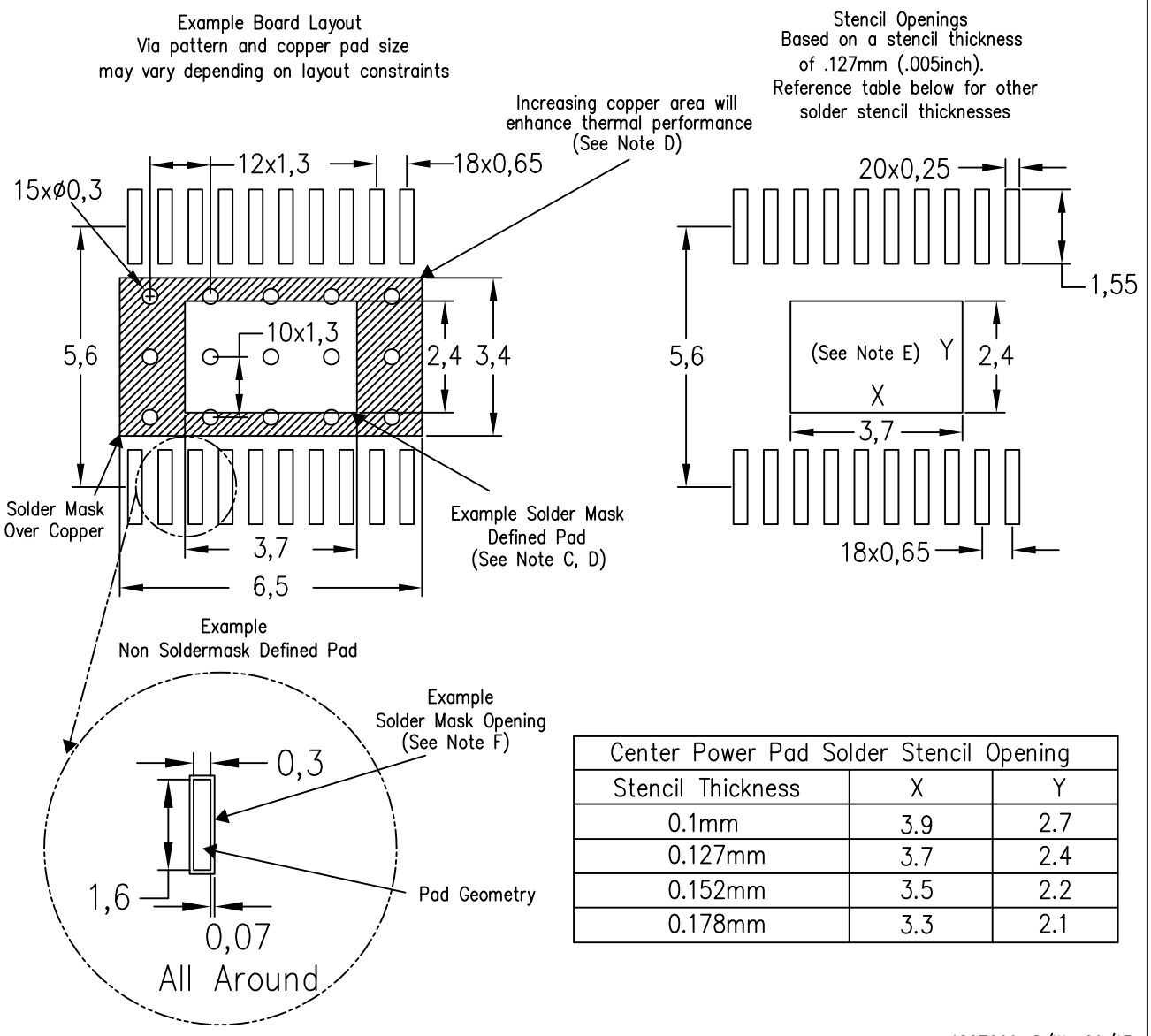
4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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