TEXAS INSTRUMENTS
PCA9539
JAJSLF4H – AUGUST 2005 – REVISED MARCH 2021

PCA9539 割り込み出力 / リセット / コンフィギュレーション・レジスタ付き、リモート 16 ビット I²C/SMBus 低消費電力 I/O エクスパンダ

1 特長

- 低いスタンバイ時消費電流：1μA 以下
- I²C からパラレル・ポートへのエクスパンダ
- オープン・ドレインのアクティブ LOW 割り込み出力
- アクティブ LOW のリセット入力
- 5V 許容の I/O ポート
- ほとんどのマイクロコントローラと互換
- 400kHz の高速 I²C バス
- 極性反転レジスタ
- 2 本のハードウェア・アドレス・ピンにより、4 つまでのデバイスをアドレス指定可能
- 大電流の駆動能力を持つラッチ付き出力により、LED を直接駆動
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を超える ESD 保護
  - 2000V、人体モデル (A114-A)
  - 1000V、デバイス帯電モデル (C101)

2 概要

この 2 線式双方向バス (I²C) 用 16 ビット I/O エクスパンダは、2.3V～5.5V の V_{CC} で動作するように設計されています。I²C インターフェイス [シリアル・クロック (SCL)、シリアル・データ (SDA)] により、ほとんどのマイクロコントローラ・ファミリの汎用リモート I/O 拡張に使用できます。

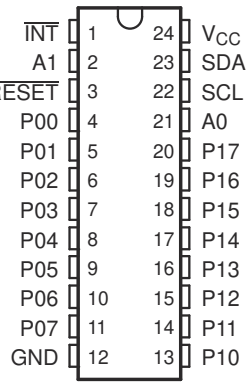
PCA9539 は、構成 (入力 / 出力選択)、入力ポート、出力ポート、極性反転 (アクティブ HIGH またはアクティブ LOW 動作) 用の 8 ビット・レジスタをそれぞれ 2 個ずつ搭載しています。電源オン時に、I/O は入力として構成されます。システム・マスタは、I/O 構成ビットに書き込むことで、I/O を入力または出力として有効にできます。それぞれの入力または出力のデータは、対応する入力または出力レジスタに保持されます。入力ポート・レジスタの極性は、極性反転レジスタで反転できます。すべてのレジスタをシステム・マスタで読み出すことができます。

製品情報

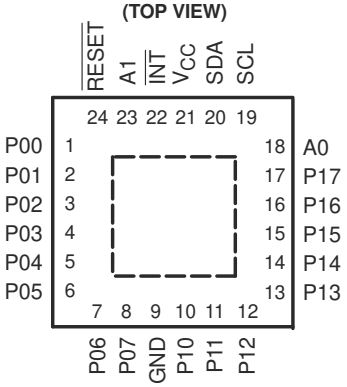
部品番号	パッケージ(1)	本体サイズ (公称)
PCA9539	SSOP (24)	8.20mm × 5.30mm
	TVSOP (24)	5.00mm × 4.40mm
	SOIC (24)	15.40mm × 7.50mm
	TSSOP (24)	7.80mm × 4.40mm
	VQFN (24)	4.00mm × 4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



RGE PACKAGE
(TOP VIEW)



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3 Revision History

Changes from Revision G (May 2014) to Revision H (March 2021) **Page**

- Moved the "Storage temperature range" to the *Absolute Maximum Ratings* 5
- Moved the "Package thermal impedance" to the *Thermal Resistance Characteristic* 5
- Changed the V_{CC} Supply voltage Max value From: 5.5 V To: V_{CC} in the *Recommended Operating Conditions* 5
- Added the *Thermal Resistance Characteristics* 6
- Changed the V_{PORR} Typ value From: 1.5 V To 1.2 V in the *Electrical Characteristics* 6
- Added V_{PORF} to the *Electrical Characteristics* 6
- Changed the I_{CC} Standby mode values in the *Electrical Characteristics* 6
- Changed the C_i SCL Max value From: 7 pF To: 8 pF in the *Electrical Characteristics* 6
- Changed the C_{io} SDA Max value From: 7 pF To: 9.5 pF in the *Electrical Characteristics* 6
- Updated the *Typical Characteristics* graphs.....8
- Changed the *Power Supply Recommendations* 27

Changes from Revision F (January 2011) to Revision G (May 2014) **Page**

- Added $\overline{RESET}$ Errata section.....17
- Added Interrupt Errata section.....18

4 概要 (続き)

システム・マスタは、タイムアウトまたはその他の不適切な動作の場合、$\overline{\text{RESET}}$ 入力を LOW にアサートすることで PCA9539 をリセットできます。パワーオン・リセットにより、レジスタはデフォルト状態に戻り、I^2C/SMBus ステート・マシンが初期化されます。$\overline{\text{RESET}}$ をアサートしても同じリセットと初期化が行われ、デバイスの電源はオフになりません。

PCA9539 のオープン・ドレイン割り込み ($\overline{\text{INT}}$) 出力は、いずれかの入力の状態が、対応する入力ポート・レジスタの状態と異なっている場合にアクティブになるため、入力状態が変化したことをシステム・マスタに示すために使用されます。

$\overline{\text{INT}}$ はマイクロコントローラの割り込み入力に接続できます。この配線で割り込み信号を送ることでリモート I/O は、I^2C バス経由で通信しなくてもポート上に受信データが存在するかどうかをマイクロコントローラに通知できます。そのため、PCA9539 はシンプル・スレーブ・デバイスとして機能できます。

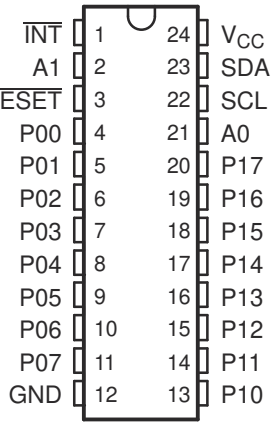
本デバイスの出力 (ラッチ付き) は大電流駆動能力を備えているため、LED を直接駆動できます。本デバイスは低消費電流です。

PCA9539 は、内部 I/O プルアップ抵抗が除去されていること、A2 が $\overline{\text{RESET}}$ に置き換わっていること、アドレス範囲が異なることを除いて PCA9555 と同じです。内部 I/O プルアップ抵抗の除去により、I/O を LOW に保持する際の消費電力が大幅に低減されています。

2 本のハードウェア・ピン (A0、A1) を使って固定 I^2C アドレスをプログラムおよび変更することで、最大 4 つのデバイスが同じ I^2C バスまたは SMBus を共有できます。

5 Pin Configuration and Functions

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



RGE PACKAGE
(TOP VIEW)

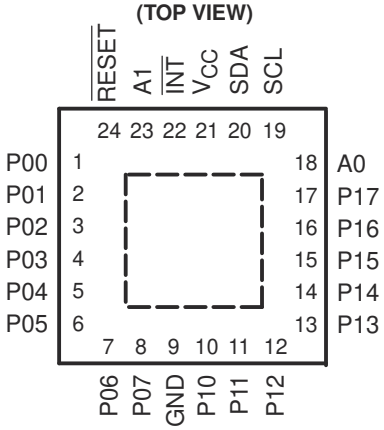


表 5-1. Pin Functions

PIN			DESCRIPTION
NAME	NO.		
	SOIC (DW), SSOP (DB), QSOP (DBQ), TSSOP (PW), AND TVSOP (DGV)	QFN (RGE)	
$\overline{INT}$	1	22	Interrupt output. Connect to V_{CC} through a pullup resistor.
A1	2	23	Address input. Connect directly to V_{CC} or ground.
$\overline{RESET}$	3	24	Active-low reset input. Connect to V_{CC} through a pullup resistor if no active connection is used.
P00	4	1	P-port input/output. Push-pull design structure.
P01	5	2	P-port input/output. Push-pull design structure.
P02	6	3	P-port input/output. Push-pull design structure.
P03	7	4	P-port input/output. Push-pull design structure.
P04	8	5	P-port input/output. Push-pull design structure.
P05	9	6	P-port input/output. Push-pull design structure.
P06	10	7	P-port input/output. Push-pull design structure.
P07	11	8	P-port input/output. Push-pull design structure.
GND	12	9	Ground
P10	13	10	P-port input/output. Push-pull design structure.
P11	14	11	P-port input/output. Push-pull design structure.
P12	15	12	P-port input/output. Push-pull design structure.
P13	16	13	P-port input/output. Push-pull design structure.
P14	17	14	P-port input/output. Push-pull design structure.
P15	18	15	P-port input/output. Push-pull design structure.
P16	19	16	P-port input/output. Push-pull design structure.
P17	20	17	P-port input/output. Push-pull design structure.
A0	21	18	Address input. Connect directly to V_{CC} or ground.
SCL	22	19	Serial clock bus. Connect to V_{CC} through a pullup resistor.
SDA	23	20	Serial data bus. Connect to V_{CC} through a pullup resistor.
V_{CC}	24	21	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6	V
V_I	Input voltage range(2)		–0.5	6	V
V_O	Output voltage range(2)		–0.5	6	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0		–20	mA
I_{IOK}	Input/output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_{OL}	Continuous output low current	V_O = 0 to V_{CC}		50	mA
I_{OH}	Continuous output high current	V_O = 0 to V_{CC}		–50	mA
I_{CC}	Continuous current through GND			–250	mA
	Continuous current through V_{CC}			160	
T_{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	V_{CC}	V
V_{IH}	High-level input voltage	SCL, SDA	0.7 × V_{CC}	V_{CC}	V
		A0, A1, $\overline{RESET}$, P07–P00, P17–P10	0.7 × V_{CC}	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	0.3 × V_{CC}	V
		A0, A1, $\overline{RESET}$, P07–P00, P17–P10	–0.5	0.3 × V_{CC}	
I_{OH}	High-level output current	P07–P00, P17–P10		–10	mA
I_{OL}	Low-level output current	P07–P00, P17–P00		25	mA
T_A	Operating free-air temperature		–40	85	°C

6.4 Thermal Resistance Characteristics

THERMAL METRIC[1]		PCA9539						UNIT
		DB (SSOP)	DBQ (SSOP)	DVG (TVSOP)	DW (SOIC)	PW (TSSOP)	RGE (VQFN)	
		24 Pins	24 Pins	24 Pins	24 Pins	24 Pins	24 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63	61	86	46	108.8	48.4	°C/W
θ_{JP}	Junction-to-pad characterization parameter						1.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA	2.3 V to 5.5 V	–1.2			V
V_{PORR}	Power-on reset voltage, V_{CC} rising	V_I = V_{CC} or GND, I_O = 0	2.3 V to 5.5 V		1.2	1.5	V
V_{PORF}	Power-on reset voltage, V_{CC} falling	V_I = V_{CC} or GND, I_O = 0	2.3 V to 5.5 V	0.75	1		V
V_{OH}	P-port high-level output voltage[2]	I_{OH} = –8 mA	2.3 V	1.8			V
			3 V	2.6			
			4.75 V	4.1			
		I_{OH} = –10 mA	2.3 V	1.7			
			3 V	2.5			
			4.75 V	4			
I_{OL}	SDA	V_{OL} = 0.4 V	2.3 V to 5.5 V	3			mA
	P port[3]	V_{OL} = 0.5 V		8	20		
		V_{OL} = 0.7 V		10	24		
	$\overline{INT}$	V_{OL} = 0.4 V		3			
I_I	SCL, SDA	V_I = V_{CC} or GND	2.3 V to 5.5 V			±1	µA
	A0, A1, $\overline{RESET}$ [4]					±1	
I_{IH}	P port	V_I = V_{CC}	2.3 V to 5.5 V			1	µA
I_{IL}	P port	V_I = GND	2.3 V to 5.5 V			–1	µA
I_{CC}	Operating mode	V_I = V_{CC} or GND, I_O = 0, I/O = inputs, f_{SCL} = 400 kHz	5.5 V		100	200	µA
			3.6 V		30	75	
			2.7 V		20	50	
	Standby mode	V_I = GND, I_O = 0, I/O = inputs, f_{SCL} = 0 kHz	5.5 V		1.5	8.7	
			3.6 V		0.9	4	
			2.7 V		0.6	3	
ΔI_{CC}	Additional current in standby mode	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V			200	µA
C_i	SCL	V_I = V_{CC} or GND	2.3 V to 5.5 V		3	8	pF
C_{io}	SDA	V_{IO} = V_{CC} or GND	2.3 V to 5.5 V		3	9.5	pF
	P port				3.7	9.5	

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}) and T_A = 25°C.
(2) Each I/O must be externally limited to a maximum of 25 mA, and each octal (P07–P00 and P17–P10) must be limited to a maximum current of 100 mA, for a device total of 200 mA.
(3) The total current sourced by all I/Os must be limited to 160 mA (80 mA for P07–P00 and 80 mA for P17–P10).
(4) $\overline{RESET}$ = V_{CC} (held high) when all other input voltages, V_I = GND.

6.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1)

			MIN	MAX	UNIT
f_{scl}	I²C clock frequency		0	400	kHz
t_{sch}	I²C clock high time		0.6		µs
t_{scl}	I²C clock low time		1.3		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		100		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time		20 + 0.1C_b (1)	300	ns
t_{icf}	I²C input fall time		20 + 0.1C_b (1)	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus	20 + 0.1C_b (1)	300	ns
t_{buf}	I²C bus free time between Stop and Start		1.3		µs
t_{sts}	I²C Start or repeated Start condition setup		0.6		µs
t_{sth}	I²C Start or repeated Start condition hold		0.6		µs
t_{sps}	I²C Stop condition setup		0.6		µs
$t_{vd(data)}$	Valid-data time	SCL low to SDA output valid	50		ns
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA (out) low	0.1	0.9	µs
C_b	I²C bus capacitive load			400	pF

(1) C_b = total capacitance of one bus line in pF

6.7 $\overline{\text{RESET}}$ Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-4)

		MIN	MAX	UNIT
t_W	Reset pulse duration	6		ns
t_{REC}	Reset recovery time	0		ns
t_{RESET}	Time to reset	400		ns

6.8 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (see 図 7-2 and 図 7-3)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{iv}	Interrupt valid time	P port	$\overline{\text{INT}}$		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{\text{INT}}$		4	µs
t_{pv}	Output data valid	SCL	P port		200	ns
t_{ps}	Input data setup time	P port	SCL	150		ns
t_{ph}	Input data hold time	P port	SCL	1		µs

6.9 Typical Characteristics

T_A = 25°C (unless otherwise noted)

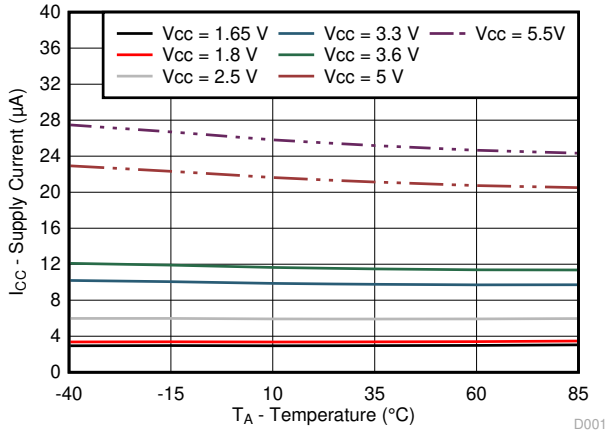


図 6-1. Supply Current vs Temperature for Different Supply Voltage (V_{CC})

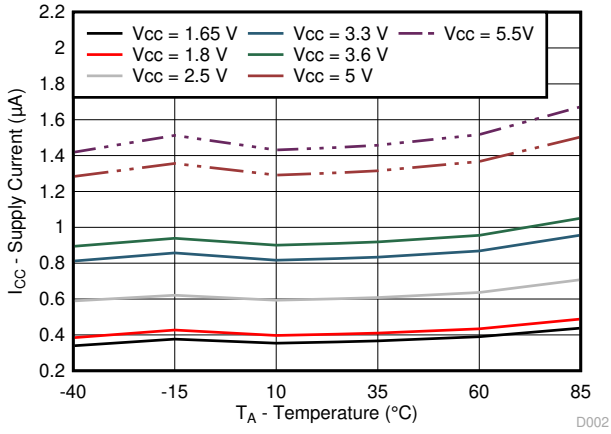


図 6-2. Standby Supply Current vs Temperature for Different Supply Voltage (V_{CC})

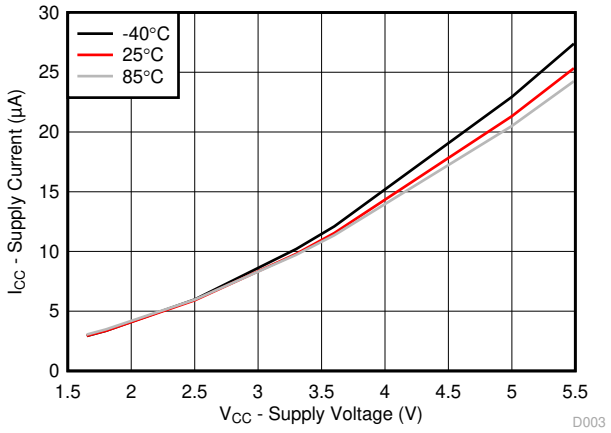


図 6-3. Supply Current vs Supply Voltage for Different Temperature (T_A)

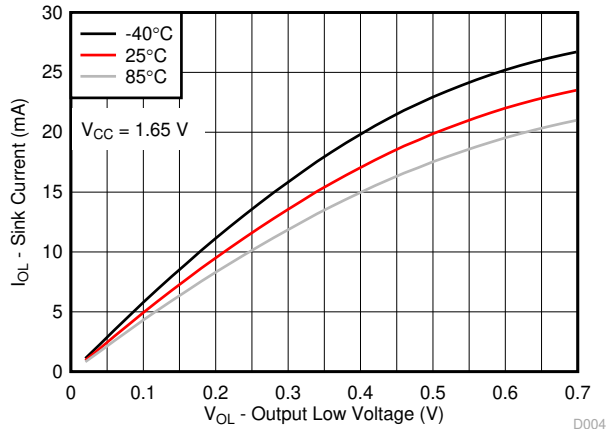


図 6-4. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 1.65 V

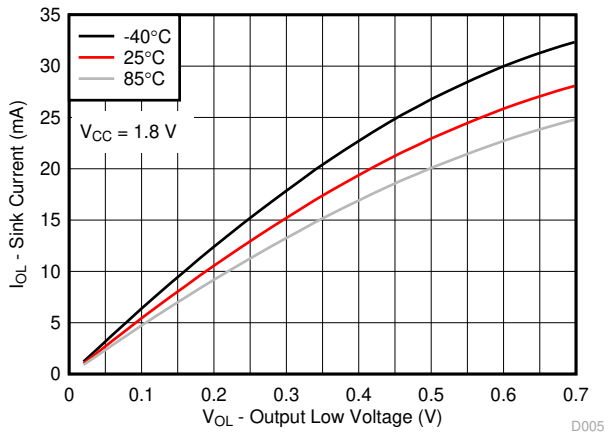


図 6-5. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 1.8 V

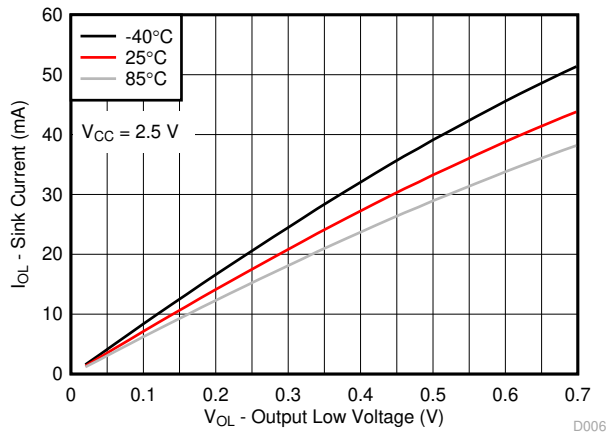


図 6-6. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 2.5 V

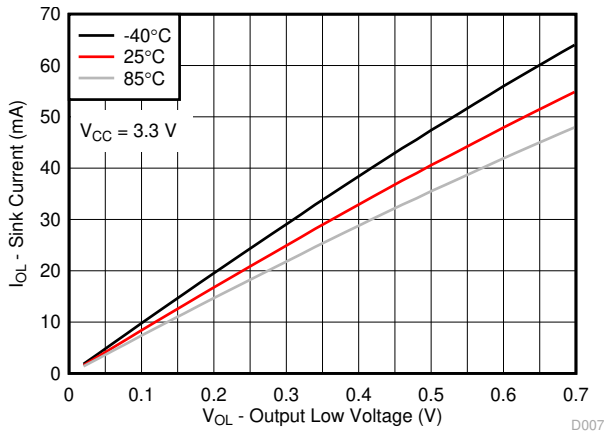


図 6-7. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 3.3 V

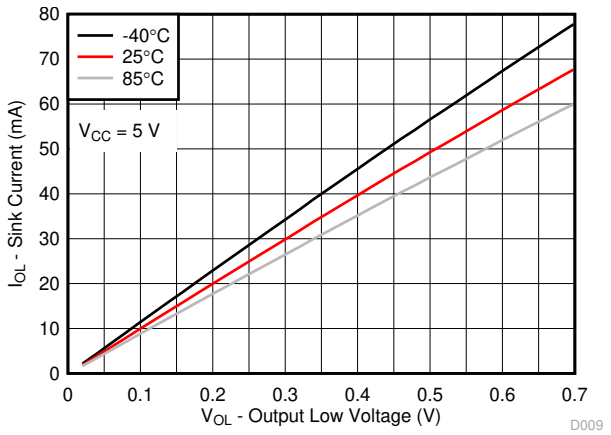


図 6-8. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 5 V

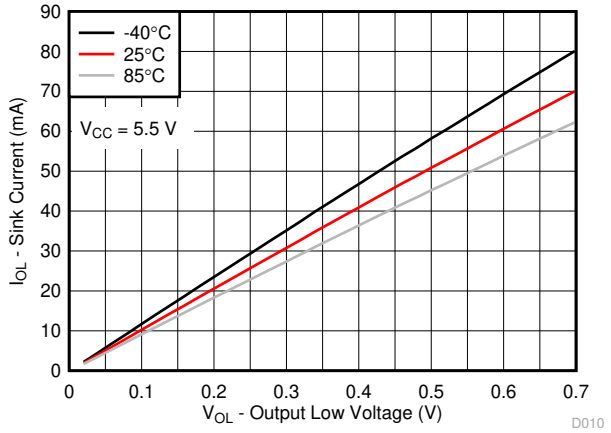


図 6-9. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 5.5 V

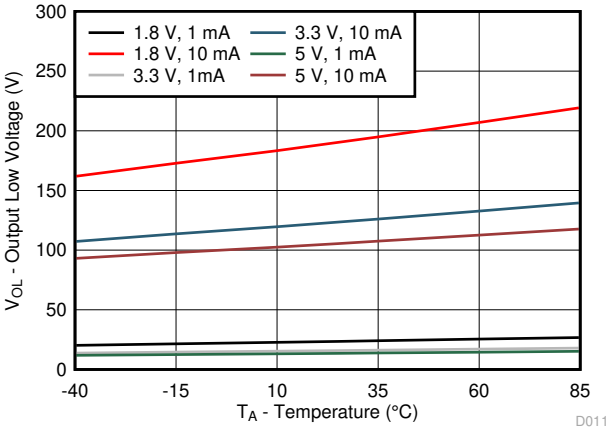


図 6-10. II/O Low Voltage vs Temperature for Different V_{CC} and I_{OL}

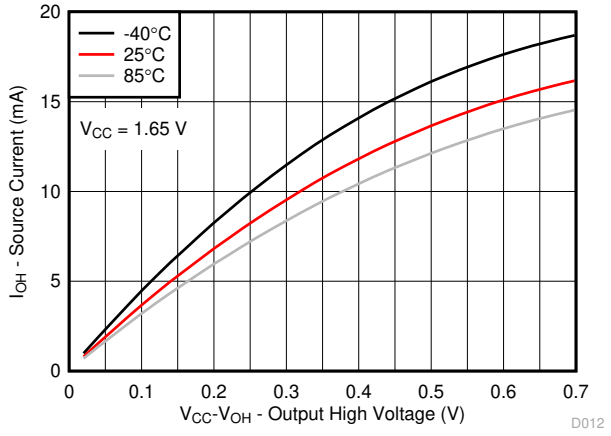


図 6-11. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 1.65 V

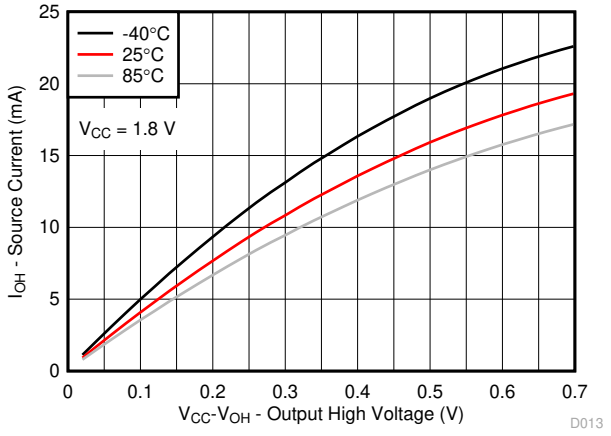


図 6-12. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 1.8 V

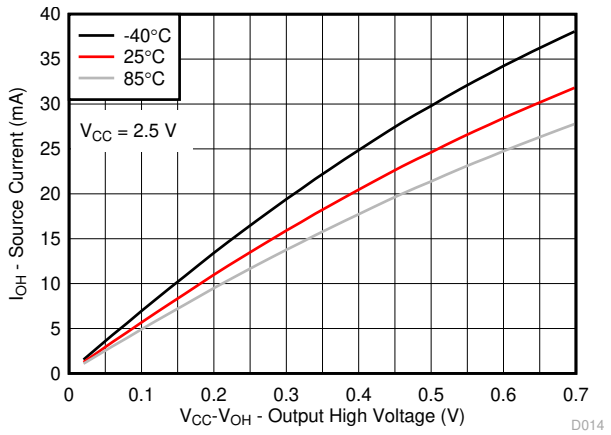


図 6-13. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 2.5 V

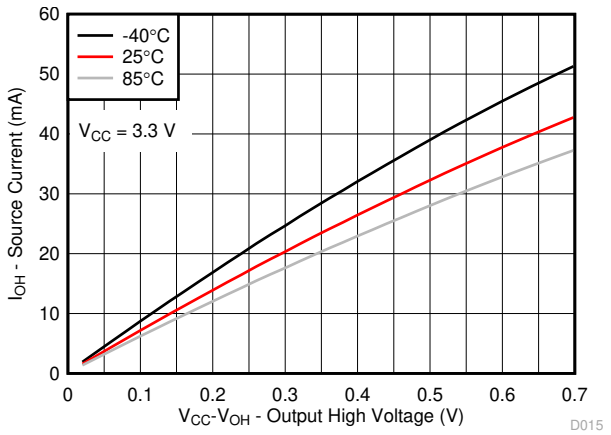


図 6-14. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 3.3 V

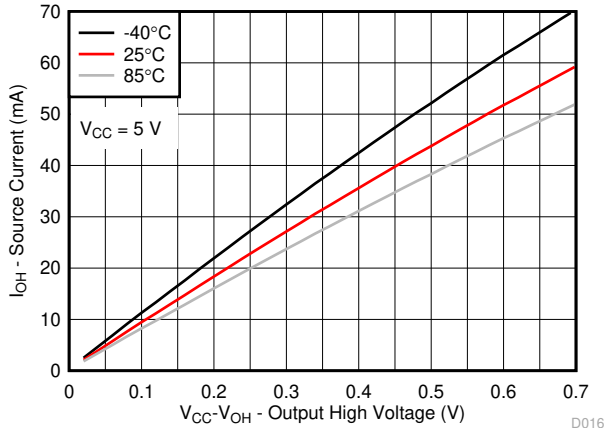


図 6-15. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 5 V

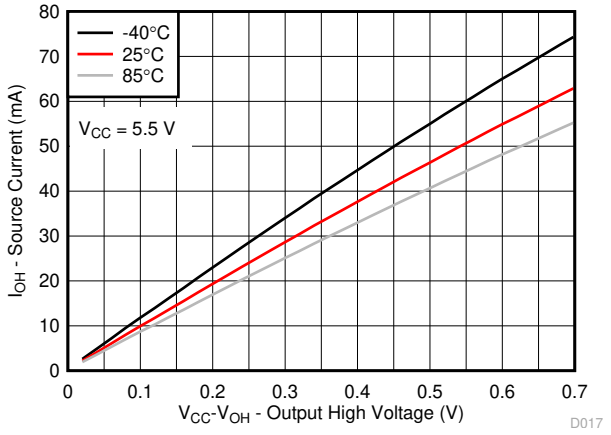


図 6-16. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 5.5 V

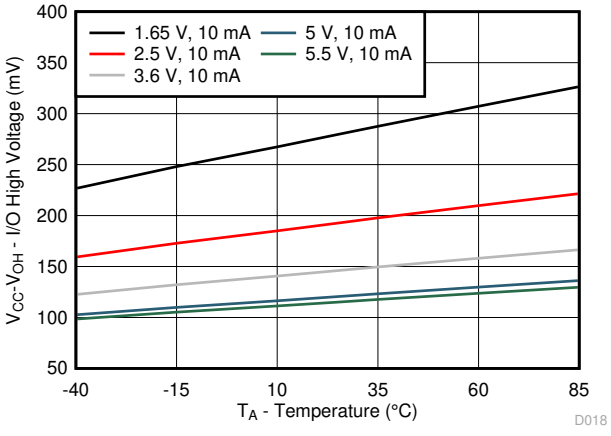


図 6-17. V_{CC} – V_{OH} Voltage vs Temperature for Different V_{CC}

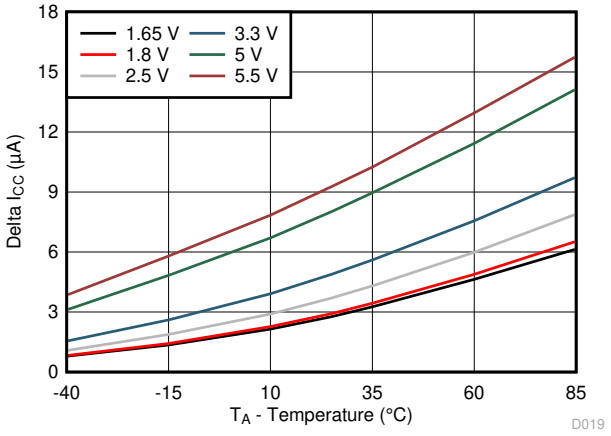
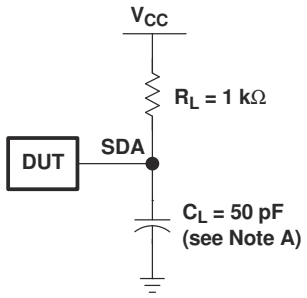
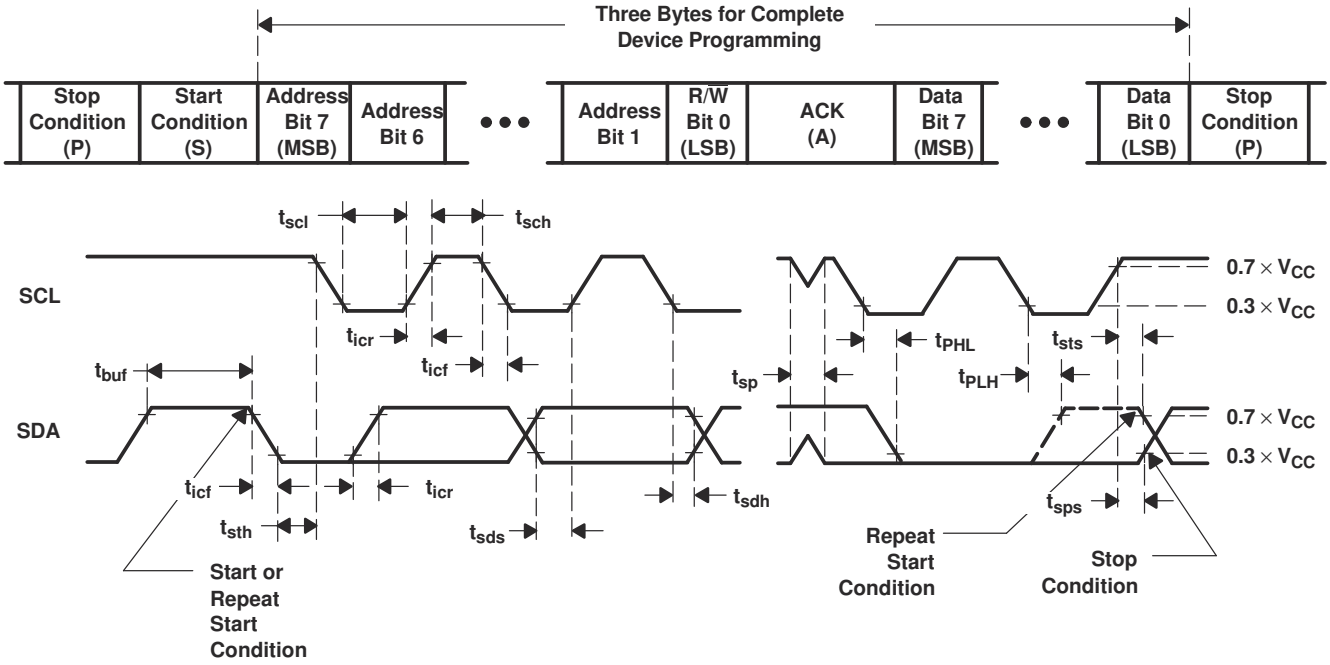


図 6-18. Δ I_{CC} vs Temperature for Different V_{CC} (V_I = V_{CC} – 0.6 V)

7 Parameter Measurement Information



SDA LOAD CONFIGURATION

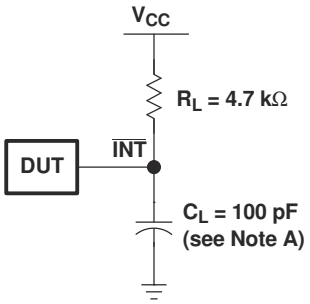


VOLTAGE WAVEFORMS

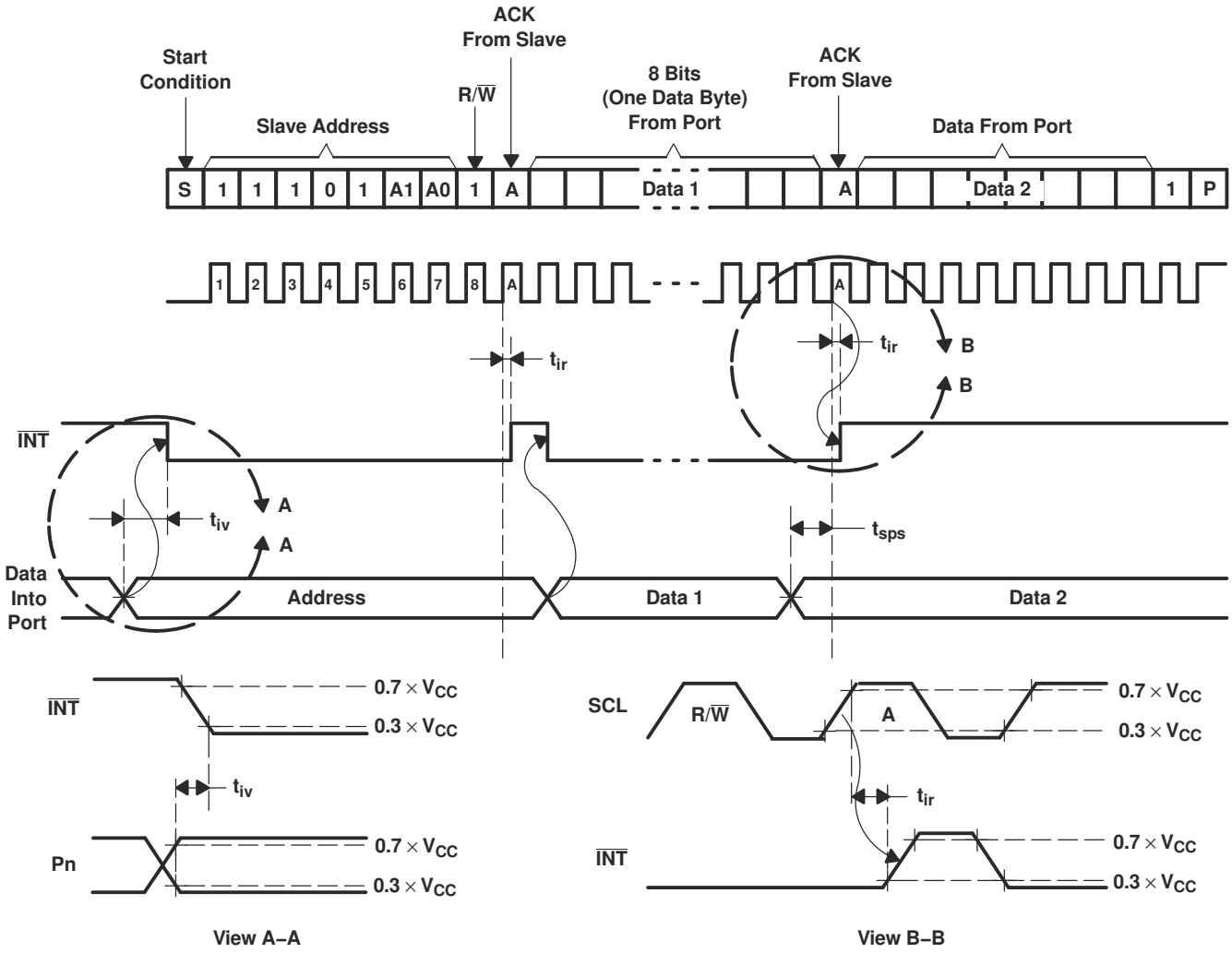
BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
C. All parameters and waveforms are not applicable to all devices.

図 7-1. I^2C Interface Load Circuit And Voltage Waveforms

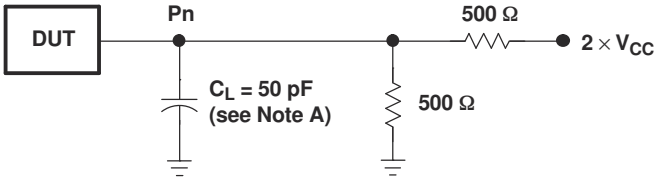


INTERRUPT LOAD CONFIGURATION

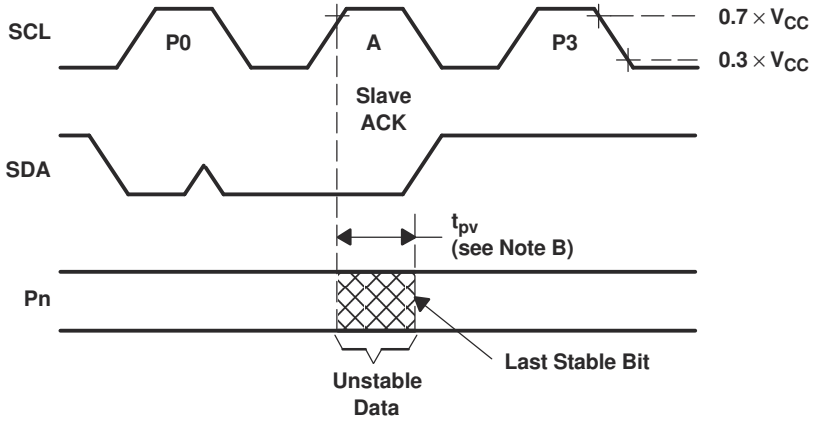


A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
C. All parameters and waveforms are not applicable to all devices.

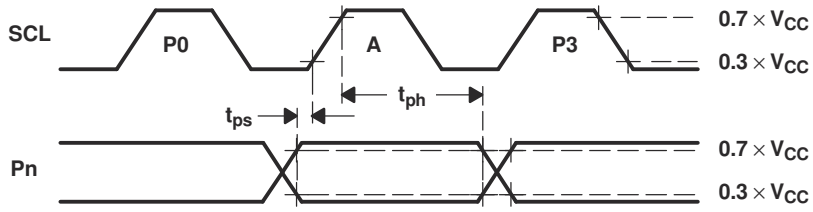
図 7-2. Interrupt Load Circuit And Voltage Waveforms



P-PORT LOAD CONFIGURATION



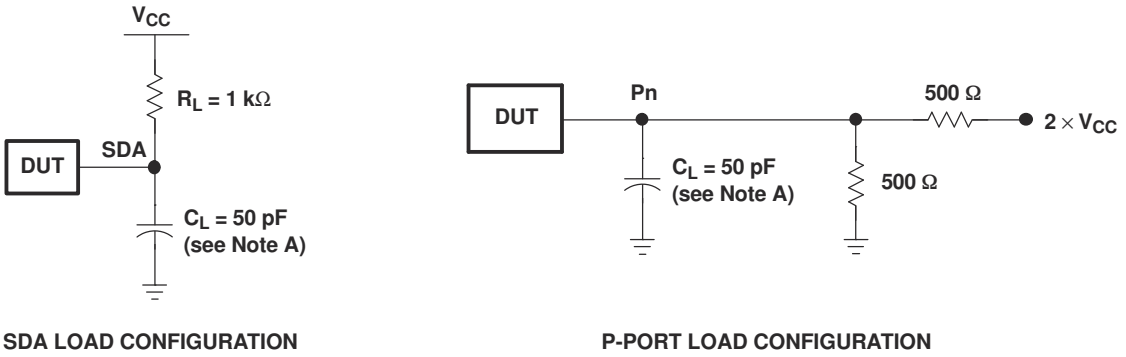
WRITE MODE (R/$\overline{W}$ = 0)



READ MODE (R/$\overline{W}$ = 1)

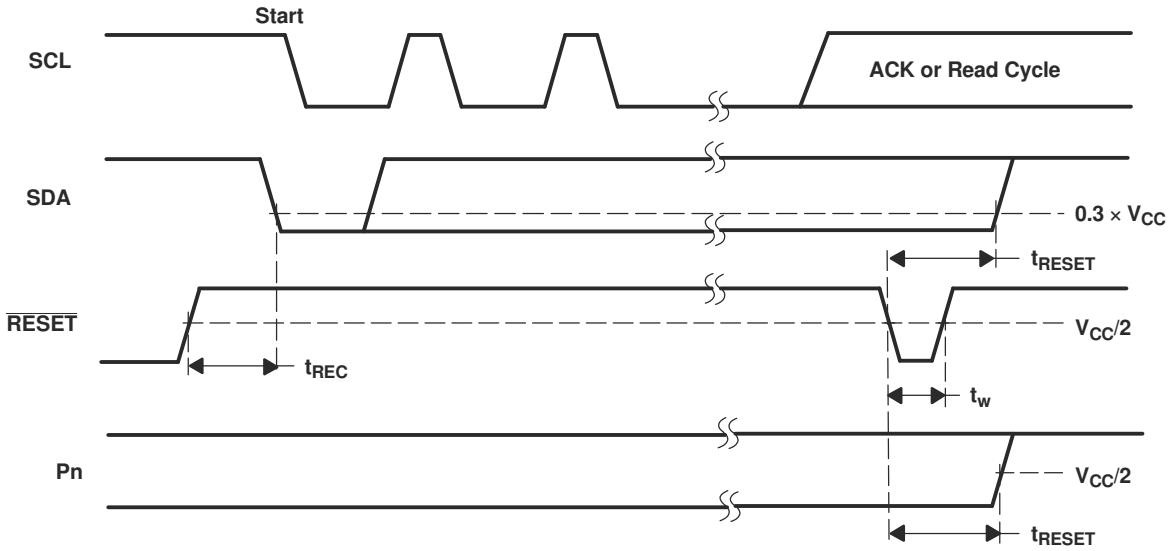
A. C_L includes probe and jig capacitance.
B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output.
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

図 7-3. P-Port Load Circuit And Voltage Waveforms



SDA LOAD CONFIGURATION

P-PORT LOAD CONFIGURATION

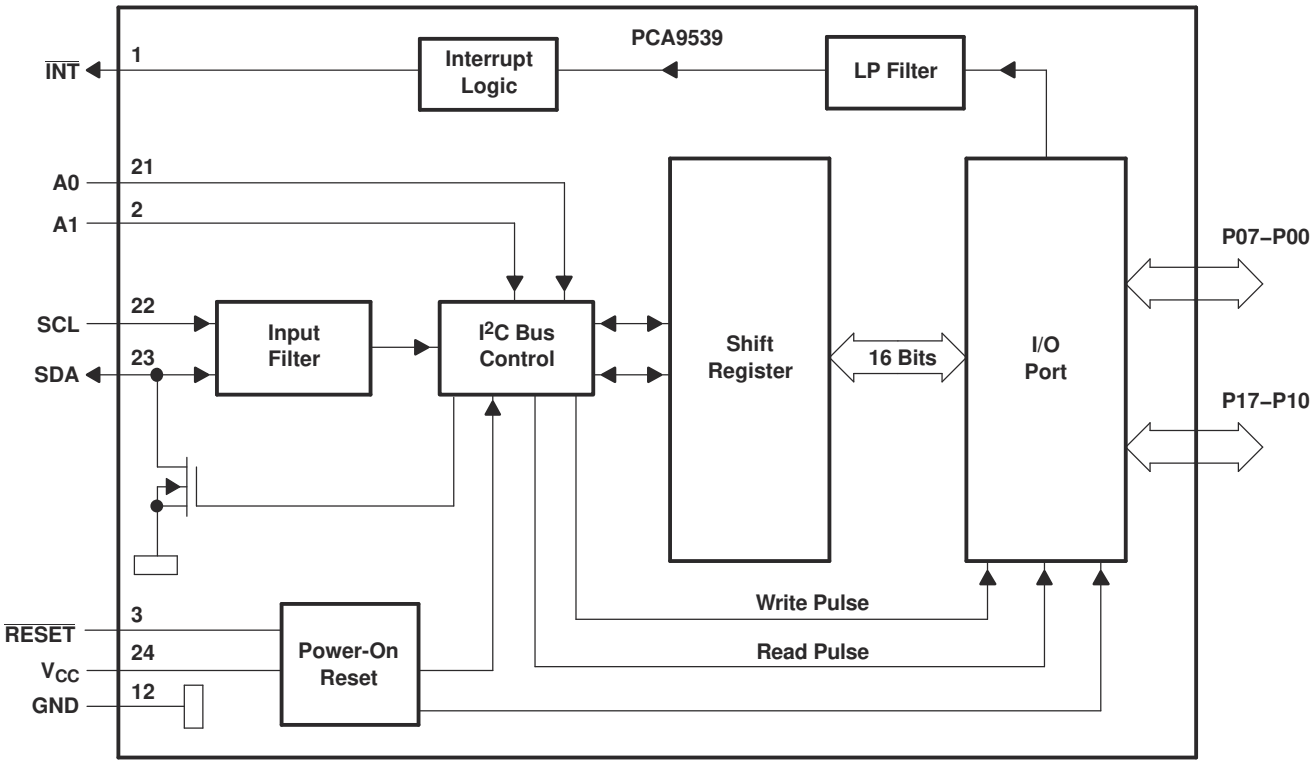


A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. I/Os are configured as inputs.
E. All parameters and waveforms are not applicable to all devices.

図 7-4. Reset Load Circuits And Voltage Waveforms

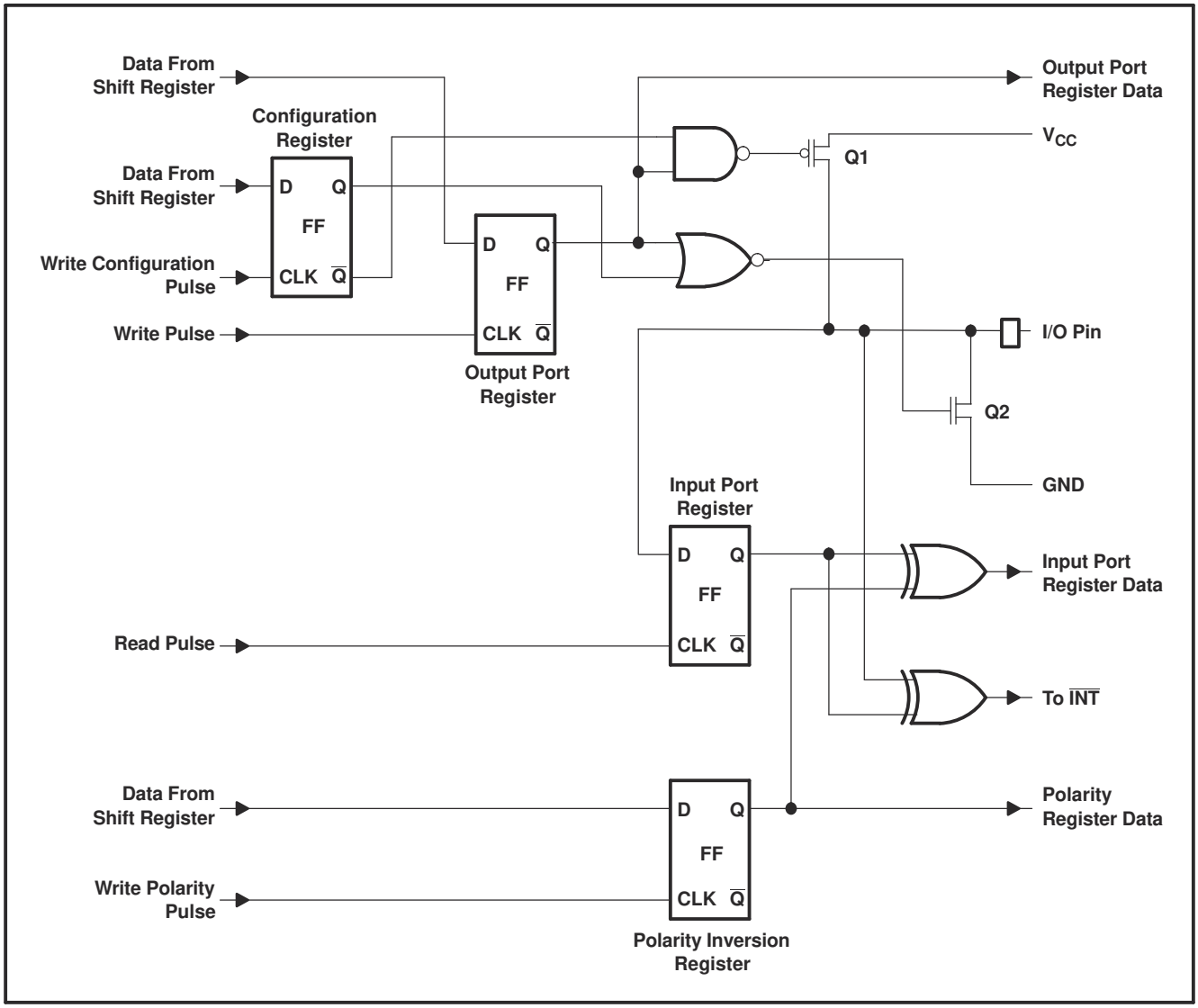
8 Detailed Description

8.1 Functional Block Diagram



A. Pin numbers shown are for DB, DBQ, DGV, DW, and PW packages.
B. All I/Os are set to inputs at reset.

図 8-1. Logic Diagram (Positive Logic)



A. At power-on reset, all registers return to default values.

図 8-2. Simplified Schematic Of P-Port I/Os

8.2 Device Functional Modes

8.2.1 $\overline{\text{RESET}}$ Input

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of t_W. The PCA9539 registers and I^2C/SMBus state machine are held in their default states until $\overline{\text{RESET}}$ is once again high. This input requires a pullup resistor to V_{CC}, if no active connection is used.

8.2.1.1 $\overline{\text{RESET}}$ Errata

If $\overline{\text{RESET}}$ voltage set higher than VCC, current will flow from $\overline{\text{RESET}}$ pin to VCC pin.

8.2.1.1.1 System Impact

VCC will be pulled above its regular voltage level

8.2.1.1.2 System Workaround

Design such that $\overline{\text{RESET}}$ voltage is same or lower than VCC

8.2.2 Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the PCA9539 in a reset condition until V_{CC} has reached V_{POR}. At that point, the reset condition is released and the PCA9539 registers and I^2C/SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

8.2.3 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 (in 図 8-2) are off, which creates a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output Port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

8.2.4 Interrupt ($\overline{\text{INT}}$) Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, the signal $\overline{\text{INT}}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting, data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{\text{INT}}$. Writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register. Because each 8-pin port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1 or vice versa.

The $\overline{\text{INT}}$ output has an open-drain structure and requires pullup resistor to V_{CC}.

8.2.4.1 Interrupt Errata

The INT will be improperly de-asserted if the following two conditions occur:

1. The last I²C command byte (register pointer) written to the device was 00h.

Note

This generally means the last operation with the device was a Read of the input register. However, the command byte may have been written with 00h without ever going on to read the input register. After reading from the device, if no other command byte written, it will remain 00h.

2. Any other slave device on the I²C bus acknowledges an address byte with the R/W bit set high

8.2.4.1.1 System Impact

Can cause improper interrupt handling as the Master will see the interrupt as being cleared.

8.2.4.1.2 System Workaround

Minor software change: User must change command byte to something besides 00h after a Read operation to the PCA9539 device or before reading from another slave device.

Note

Software change will be compatible with other versions (competition and TI redesigns) of this device.

8.3 Programming

8.3.1 I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see 図 8-3). After the Start condition, the device address byte is sent, MSB first, including the data direction bit (R/ $\overline{W}$). This device does not respond to the general call address.

After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0 and A1) of the slave device must not be changed between the Start and Stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see 図 8-4).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see 図 8-3).

Any number of data bytes can be transferred from the transmitter to the receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see 図 8-5). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

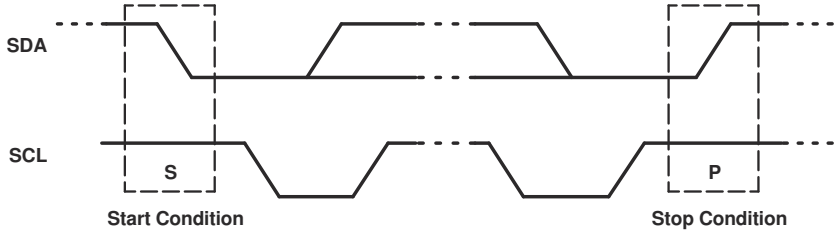


図 8-3. Definition Of Start And Stop Conditions

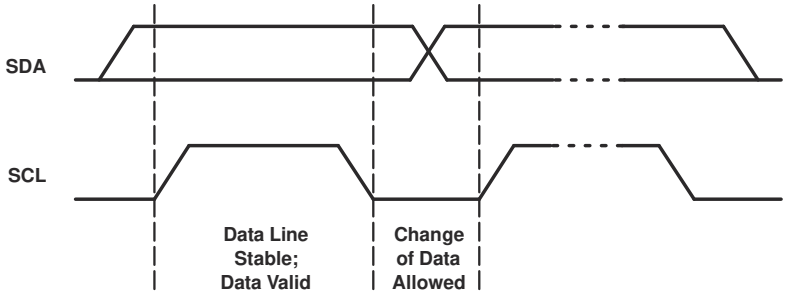


図 8-4. Bit Transfer

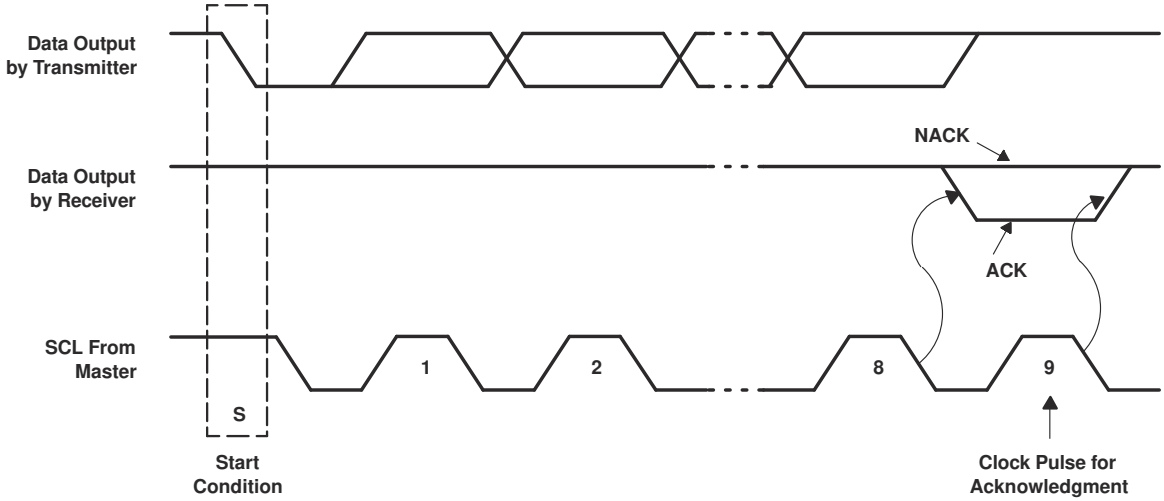


図 8-5. Acknowledgment On I²C Bus

8.3.2 Register Map

表 8-1. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C slave address	H	H	H	L	H	A1	A0	R/ $\overline{W}$
P0x I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
P1x I/O data bus	P17	P16	P15	P14	P13	P12	P11	P10

8.3.2.1 Device Address

図 8-6 shows the address byte of the PCA9539.

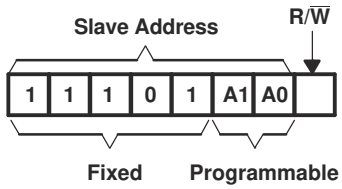


図 8-6. Pca9539 Address

表 8-2. Address Reference

INPUTS		I²C BUS SLAVE ADDRESS
A1	A0	
L	L	116 (decimal), 74 (hexadecimal)
L	H	117 (decimal), 75 (hexadecimal)
H	L	118 (decimal), 76 (hexadecimal)
H	H	119 (decimal), 77 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

8.3.2.2 Control Register And Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the PCA9539. Three bits of this data byte state the operation (read or write) and the internal register (input, output, Polarity Inversion or Configuration) that will be affected. This register can be written or read through the I²C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

0	0	0	0	0	B2	B1	B0

図 8-7. Control Register Bits

表 8-3. Command Byte

CONTROL REGISTER BITS			COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B2	B1	B0				
0	0	0	0x00	Input Port 0	Read byte	xxxx xxxx
0	0	1	0x01	Input Port 1	Read byte	xxxx xxxx
0	1	0	0x02	Output Port 0	Read/write byte	1111 1111
0	1	1	0x03	Output Port 1	Read/write byte	1111 1111
1	0	0	0x04	Polarity Inversion Port 0	Read/write byte	0000 0000
1	0	1	0x05	Polarity Inversion Port 1	Read/write byte	0000 0000
1	1	0	0x06	Configuration Port 0	Read/write byte	1111 1111
1	1	1	0x07	Configuration Port 1	Read/write byte	1111 1111

8.3.2.3 Register Descriptions

The Input Port registers (registers 0 and 1) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to indicate to the I^2C device that the Input Port register will be accessed next.

表 8-4. Registers 0 And 1 (Input Port Registers)

Bit	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X
Bit	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

The Output Port registers (registers 2 and 3) show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

表 8-5. Registers 2 And 3 (Output Port Registers)

Bit	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1
Bit	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

The Polarity Inversion registers (registers 4 and 5) allow Polarity Inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin's original polarity is retained.

表 8-6. Registers 4 And 5 (Polarity Inversion Registers)

Bit	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0
Bit	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

The Configuration registers (registers 6 and 7) configure the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

表 8-7. Registers 6 And 7 (Configuration Registers)

Bit	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1
Bit	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

8.3.2.4 Bus Transactions

Data is exchanged between the master and PCA9539 through write and read commands.

8.3.2.4.1 Writes

Data is transmitted to the PCA9539 by sending the device address and setting the least-significant bit to a logic 0 (see 図 8-6 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte.

The eight registers within the PCA9539 are configured to operate as four register pairs. The four pairs are Input Ports, Output Ports, Polarity Inversion ports, and Configuration ports. After sending data to one register, the next data byte is sent to the other register in the pair (see 図 8-8 and 図 8-9). For example, if the first byte is sent to Output Port 1 (register 3), the next byte is stored in Output Port 0 (register 2).

There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

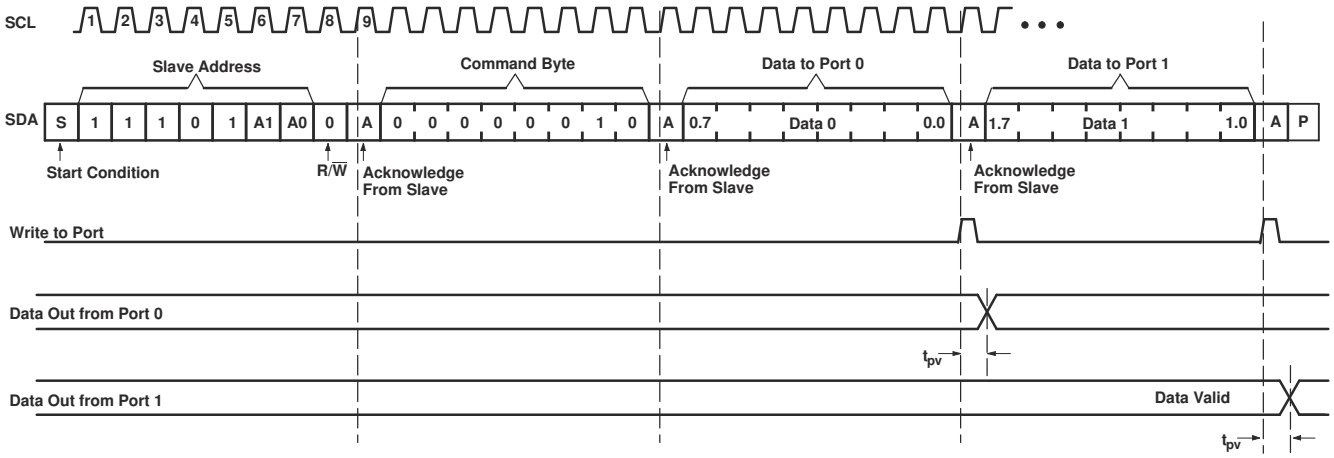


図 8-8. Write To Output Port Registers

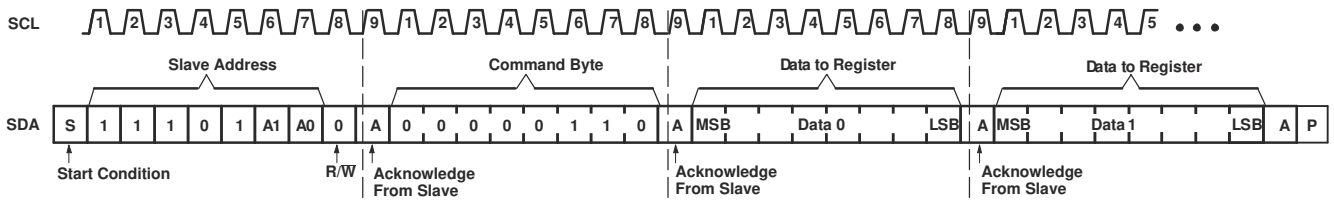


図 8-9. Write To Configuration Registers

8.3.2.4.2 Reads

The bus master first must send the PCA9539 address with the least-significant bit set to a logic 0 (see 図 8-6 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again, but this time, the least-significant bit is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9539 (see 図 8-10 through 図 8-12).

After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. For example, if the command byte references Input Port 1 before the restart, and the restart occurs when Input Port 0 is being read, the stored command byte changes to reference Input Port 0. The original command byte is forgotten. If a subsequent restart occurs, Input Port 0 is read first. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflect the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0.

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

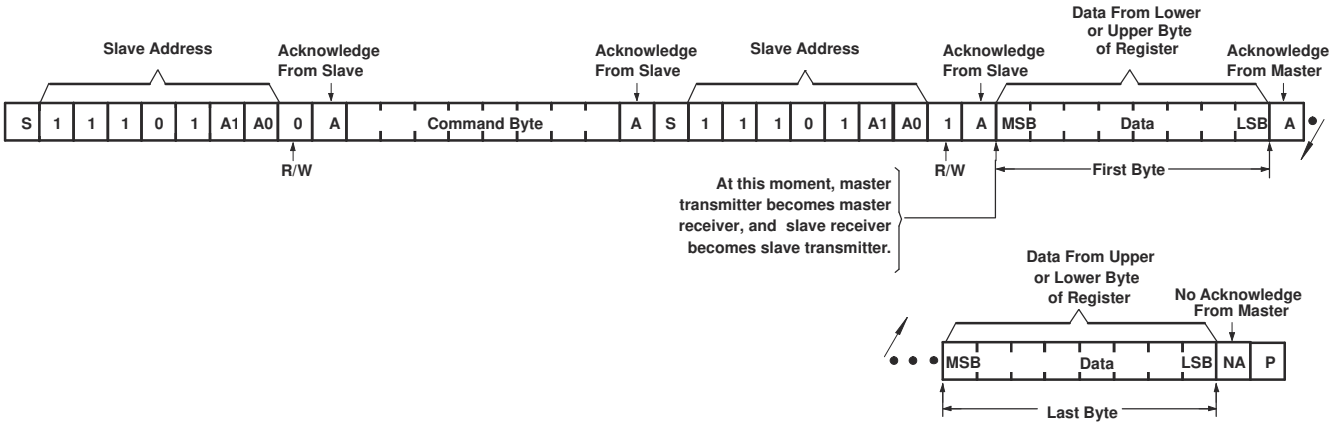
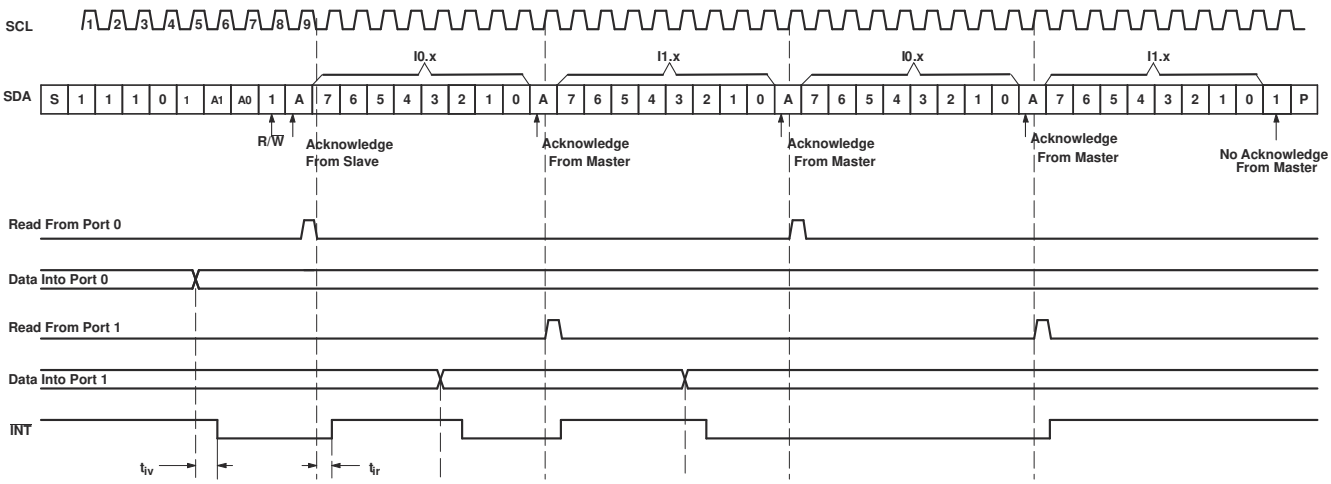


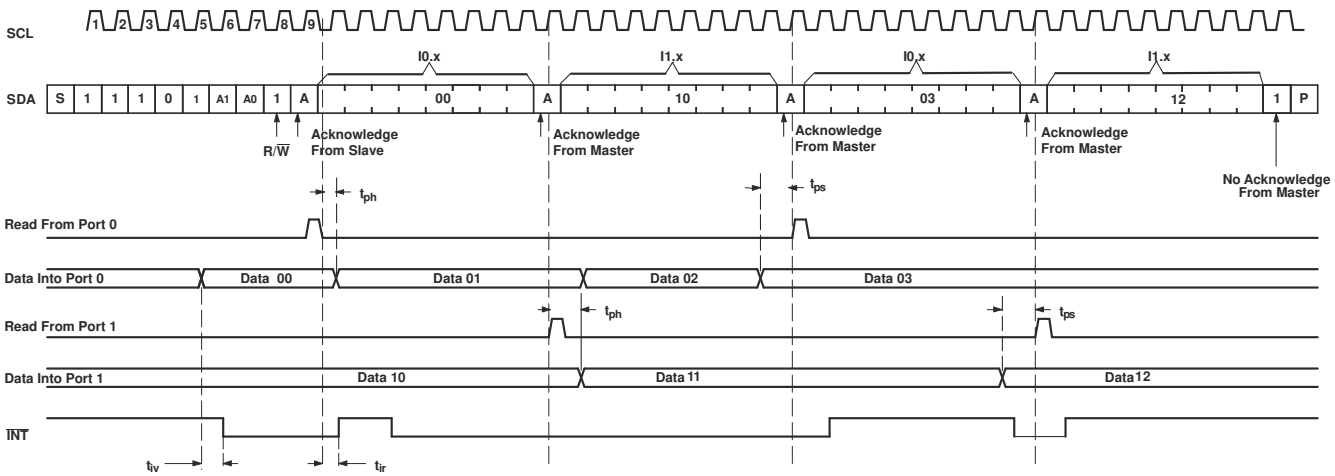
図 8-10. Read From Register



A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (Read Input Port register).

B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see 図 8-10 for these details).

図 8-11. Read Input Port Register, Scenario 1



A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (Read Input Port register).

B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see 図 8-10 for these details).

図 8-12. Read Input Port Register, Scenario 2

9 Application Information Disclaimer

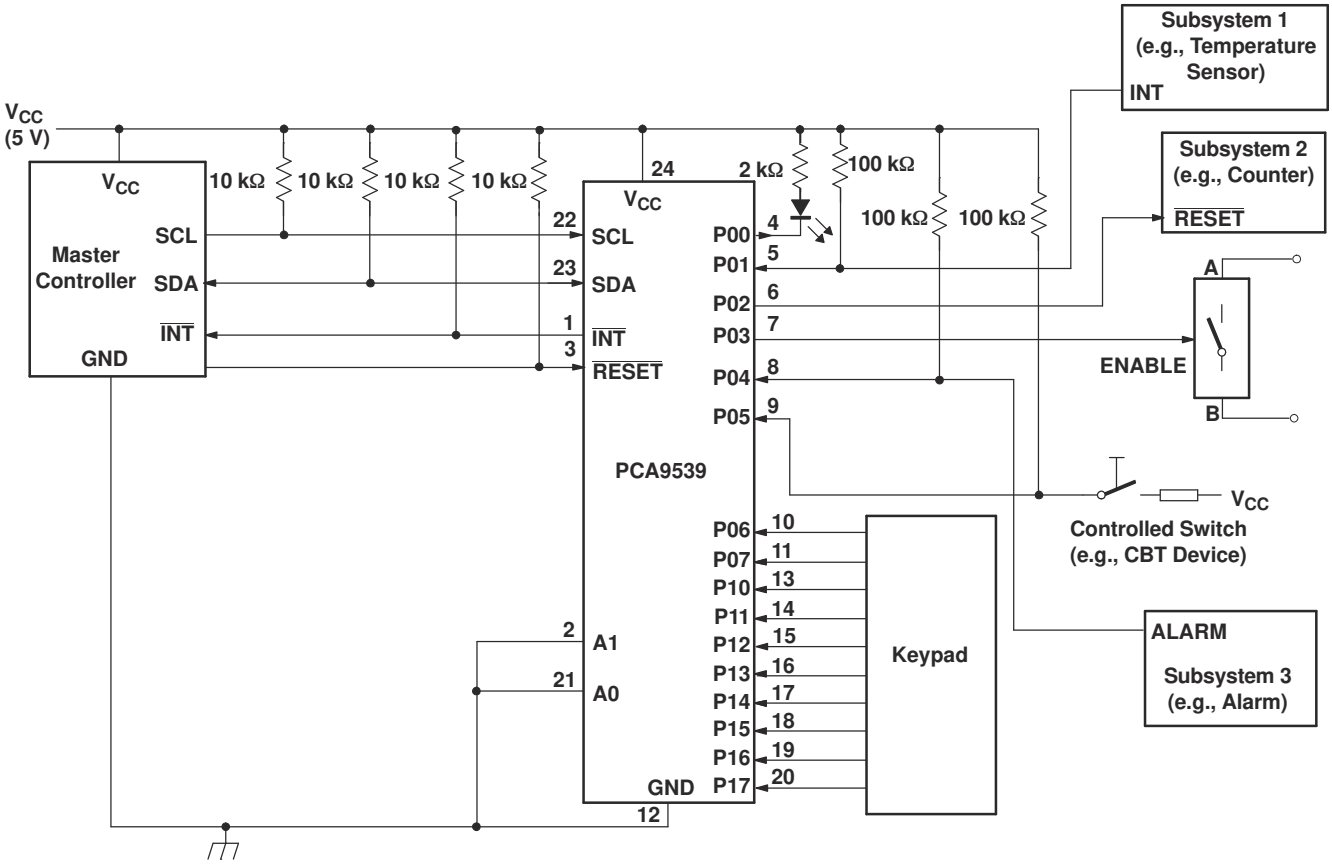
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

図 9-1 shows an application in which the PCA9539 can be used.

9.2 Typical Application



A. Device address is configured as 1110100 for this example.
B. P00, P02, and P03 are configured as outputs.
C. P01 and P04 to P17 are configured as inputs.
D. Pin numbers shown are for DB, DBQ, DGV, DW, and PW packages.

図 9-1. Typical Application

9.2.1 Detailed Design Procedure

9.2.1.1 Minimizing I_{CC} When I/O Is Used To Control Led

When an I/O is used to control an LED, normally it is connected to V_{CC} through a resistor (see 図 9-1). Because the LED acts as a diode, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The ΔI_{CC} parameter in Electrical Characteristics shows how I_{CC} increases as V_{IN} becomes lower than V_{CC}. For battery-powered applications, it is essential that the voltage of I/O pins is greater than or equal to V_{CC}, when the LED is off, to minimize current consumption.

図 9-2 shows a high-value resistor in parallel with the LED. 図 9-3 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{CC} at or above V_{CC} and prevent additional supply-current consumption when the LED is off.

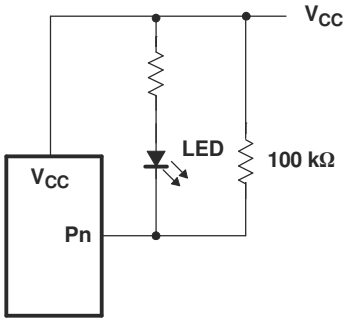


図 9-2. High-Value Resistor In Parallel With Led

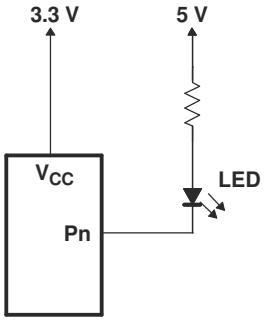


図 9-3. Device Supplied By Lower Voltage

10 Power Supply Recommendations

10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, PCA9539 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in 図 10-1 and 図 10-2.

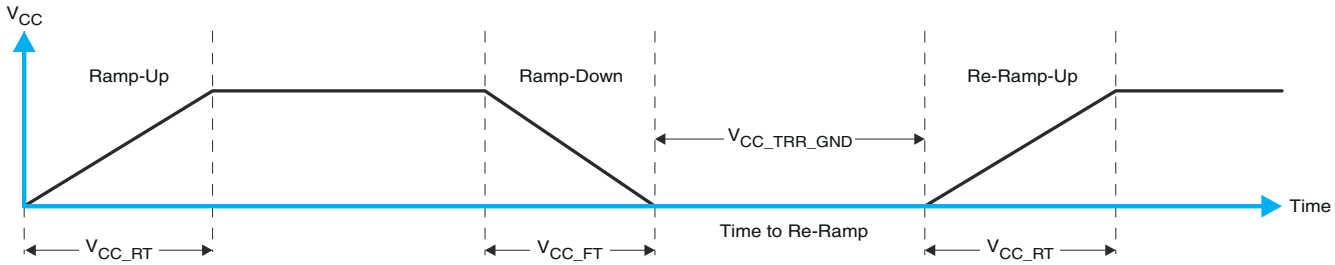


図 10-1. V_{CC} Is Lowered Below 0.2 V Or 0 V And Then Ramped Up To V_{CC}

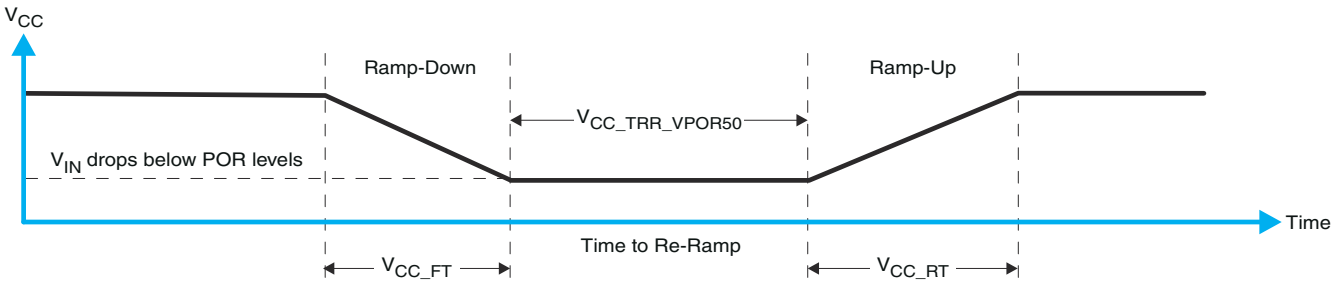


図 10-2. V_{CC} Is Lowered Below The Por Threshold, Then Ramped Back Up To V_{CC}

表 10-1 specifies the performance of the power-on reset feature for PCA9539 for both types of power-on reset.

表 10-1. Recommended Supply Sequencing And Ramp Rates(1)

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See 図 10-1	1		100	ms
V_{CC_RT}	Rise rate	See 図 10-1	0.01		100	ms
$V_{CC\_TRR\_GND}$	Time to re-ramp (when V_{CC} drops to GND)	See 図 10-1	0.001			ms
$V_{CC\_TRR\_POR50}$	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV)	See 図 10-2	0.001			ms
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCX_GW} = 1 µs	See 図 10-3			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when V_{CCX_GH} = 0.5 × V_{CCx}	See 図 10-3				µs
V_{PORF}	Voltage trip point of POR on falling V_{CC}		0.767		1.144	V
V_{PORR}	Voltage trip point of POR on rising V_{CC}		1.033		1.428	V

(1) T_A = –40°C to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and the device impedance are factors that affect power-on reset performance. 図 10-3 and 表 10-1 provide more information on how to measure these specifications.

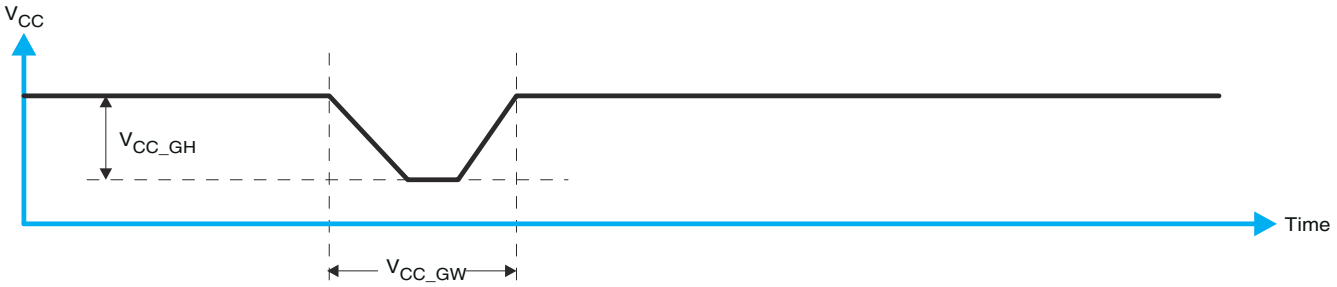


図 10-3. Glitch Width And Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. 図 10-4 and 表 10-1 provide more details on this specification.

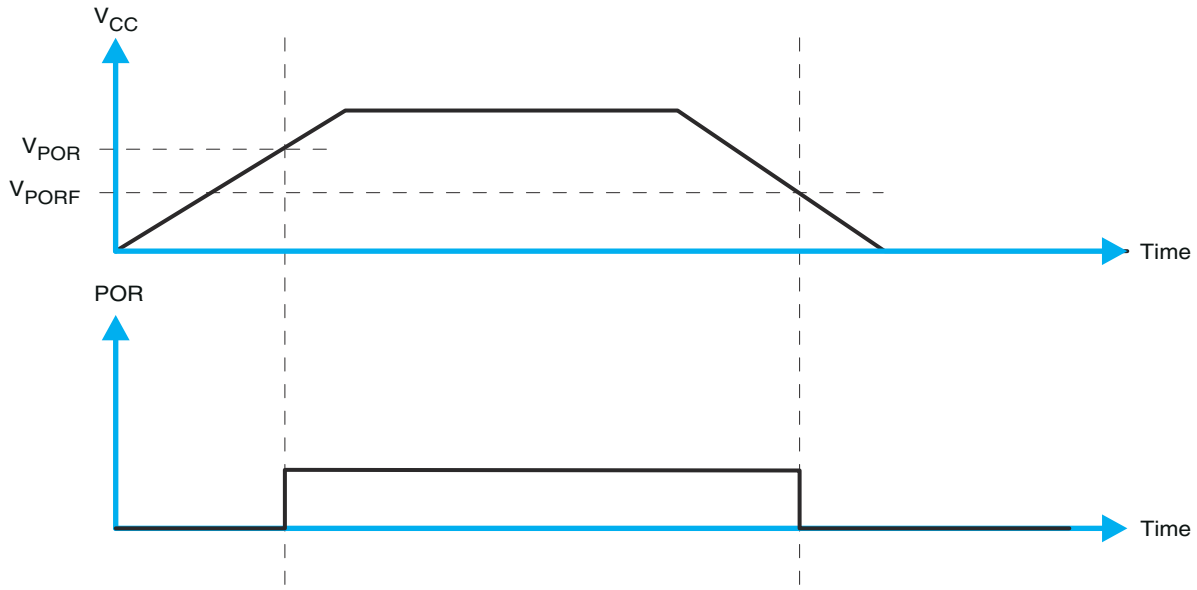


図 10-4. V_{POR}

11 Device and Documentation Support

11.1 Trademarks

すべての商標は、それぞれの所有者に帰属します。

11.2 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.3 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCA9539DB	Active	Production	SSOP (DB) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539
PCA9539DB.A	Active	Production	SSOP (DB) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539
PCA9539DBQR	Active	Production	SSOP (DBQ) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PCA9539
PCA9539DBQR.A	Active	Production	SSOP (DBQ) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PCA9539
PCA9539DBR	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539
PCA9539DBR.A	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539
PCA9539DGVR	Active	Production	TVSOP (DGV) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539
PCA9539DGVR.A	Active	Production	TVSOP (DGV) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539
PCA9539DW	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9539
PCA9539DW.A	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9539
PCA9539DWR	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9539
PCA9539DWR.A	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9539
PCA9539PWR	NRND	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539
PCA9539PWR.A	NRND	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539
PCA9539PWR.B	NRND	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539
PCA9539PWRG4	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539
PCA9539RGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539
PCA9539RGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539
PCA9539RGER.B	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539
PCA9539RGERG4	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539
PCA9539RGERG4.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539
PCA9539RGERG4.B	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9539

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

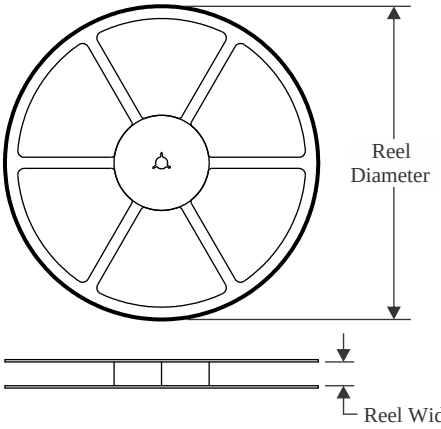
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

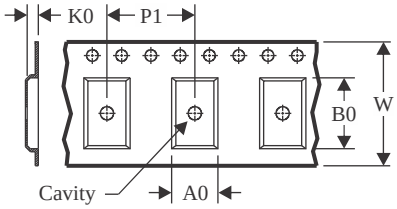
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

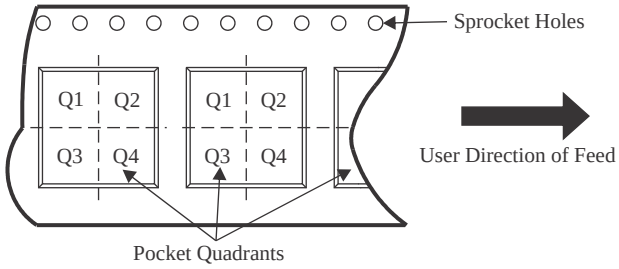


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

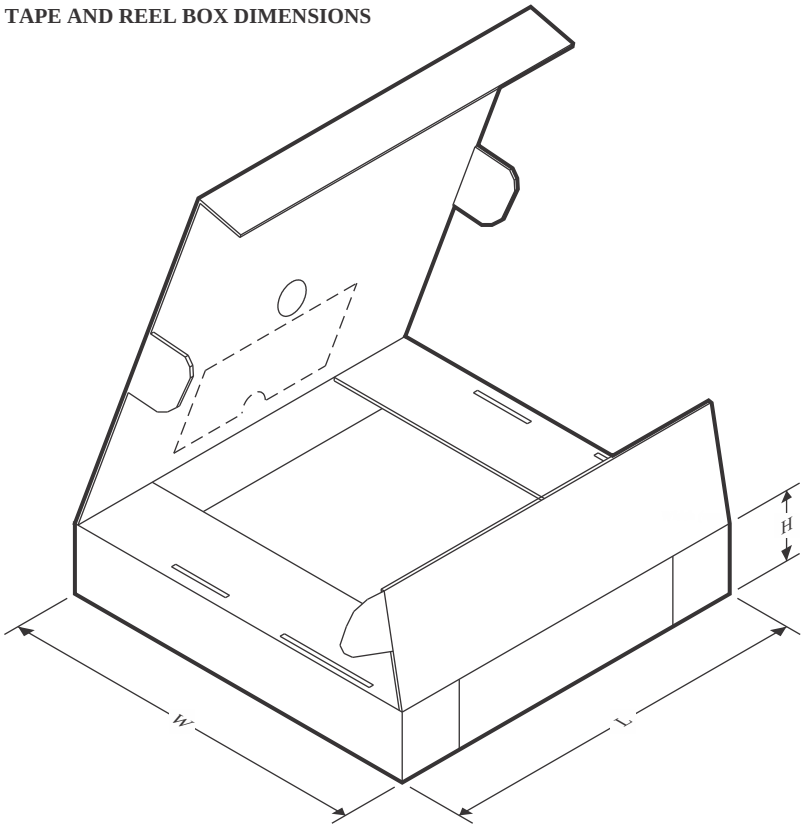
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9539DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
PCA9539DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
PCA9539DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9539DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
PCA9539PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
PCA9539RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
PCA9539RGERG4	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

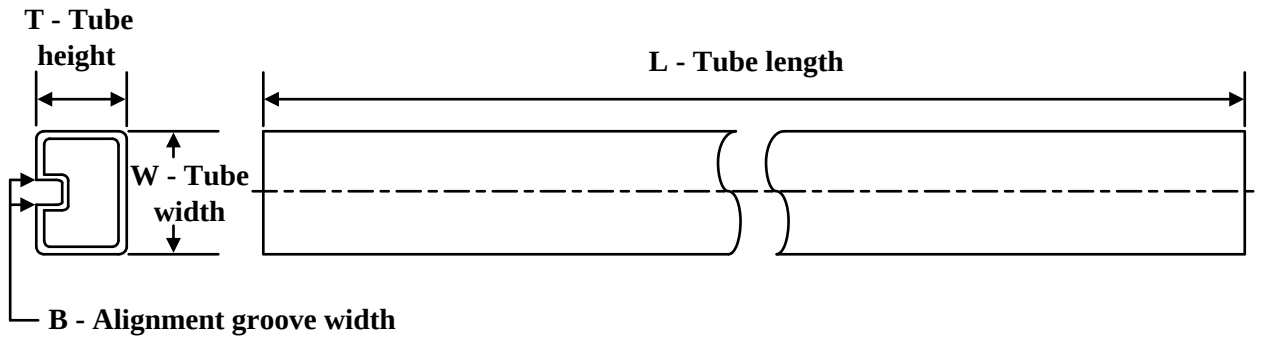
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9539DBQR	SSOP	DBQ	24	2500	353.0	353.0	32.0
PCA9539DBR	SSOP	DB	24	2000	353.0	353.0	32.0
PCA9539DGVR	TVSOP	DGV	24	2000	353.0	353.0	32.0
PCA9539DWR	SOIC	DW	24	2000	350.0	350.0	43.0
PCA9539PWR	TSSOP	PW	24	2000	353.0	353.0	32.0
PCA9539RGER	VQFN	RGE	24	3000	346.0	346.0	33.0
PCA9539RGERG4	VQFN	RGE	24	3000	346.0	346.0	33.0

TUBE



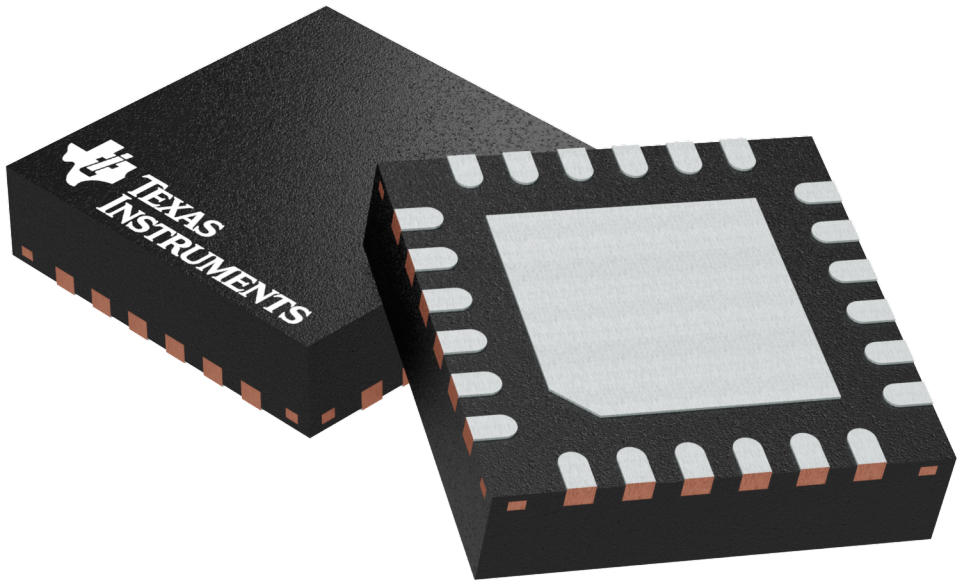
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PCA9539DB	DB	SSOP	24	60	530	10.5	4000	4.1
PCA9539DB.A	DB	SSOP	24	60	530	10.5	4000	4.1
PCA9539DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
PCA9539DW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

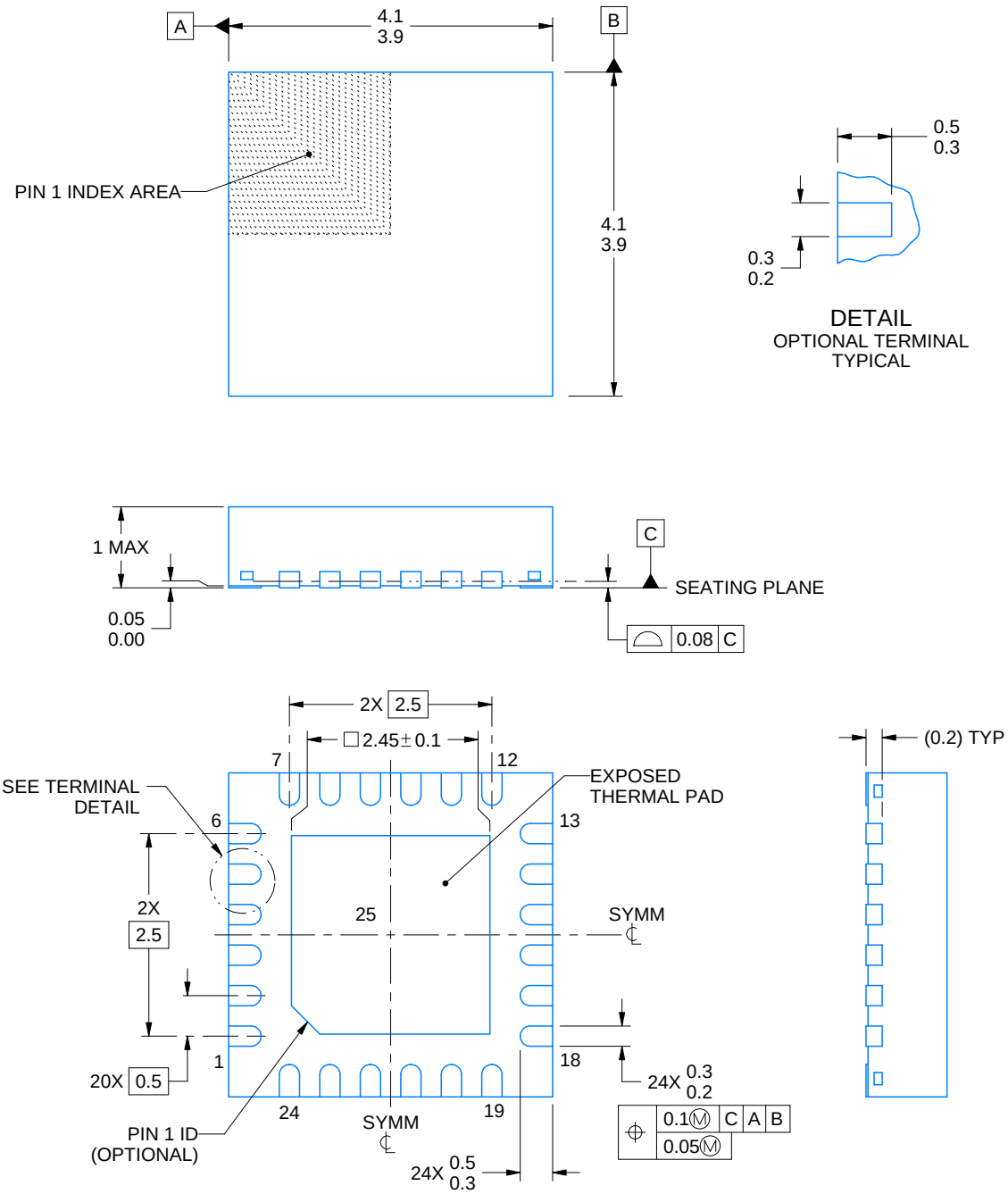
4204104/H

PACKAGE OUTLINE

RGE0024B

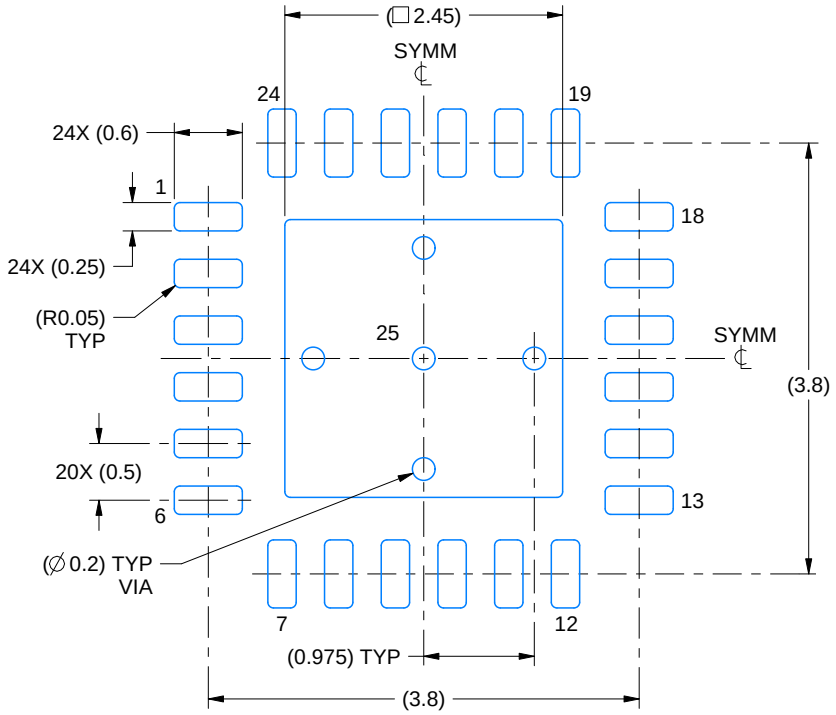
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

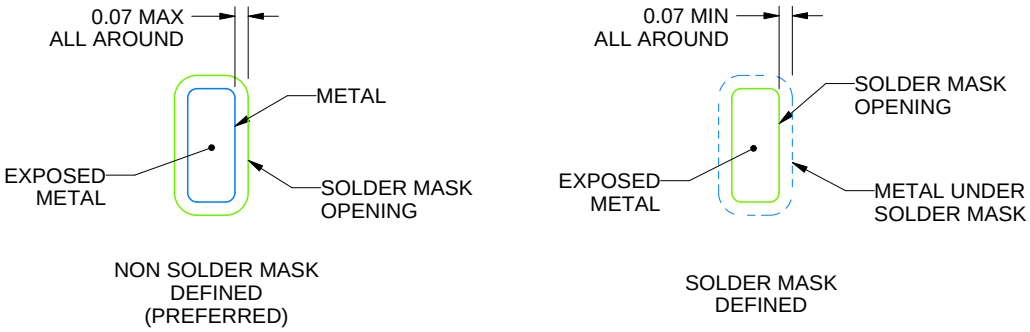


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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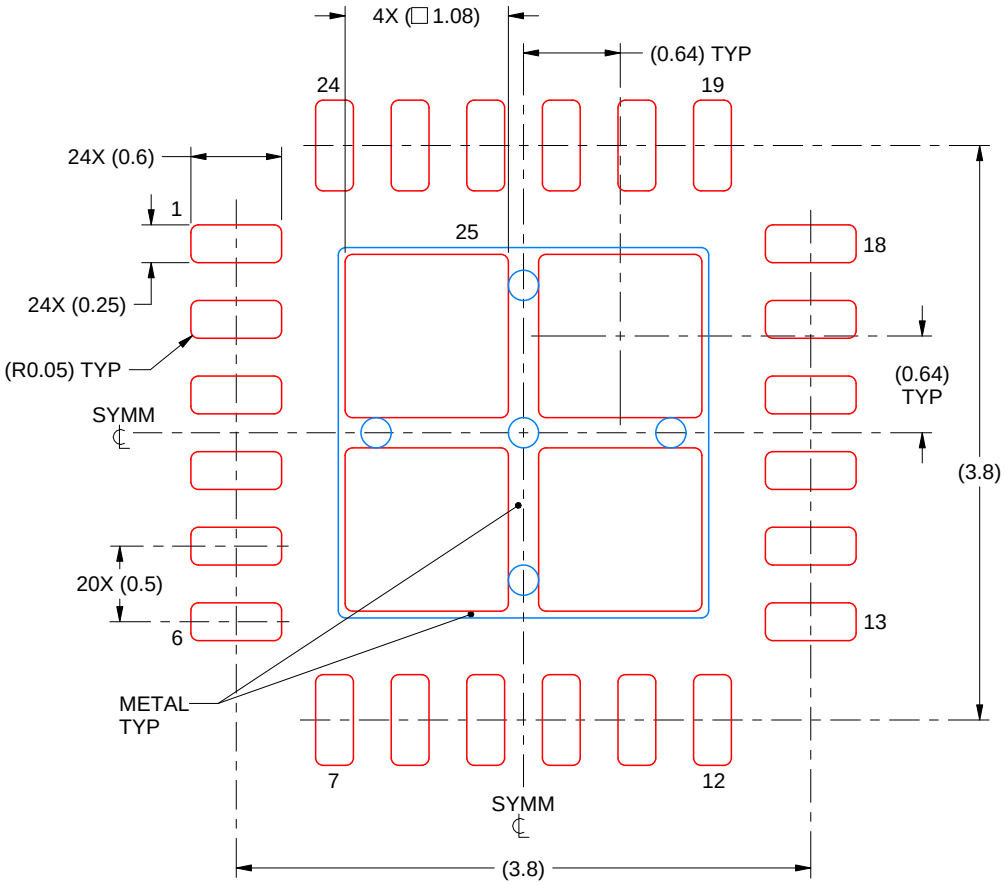
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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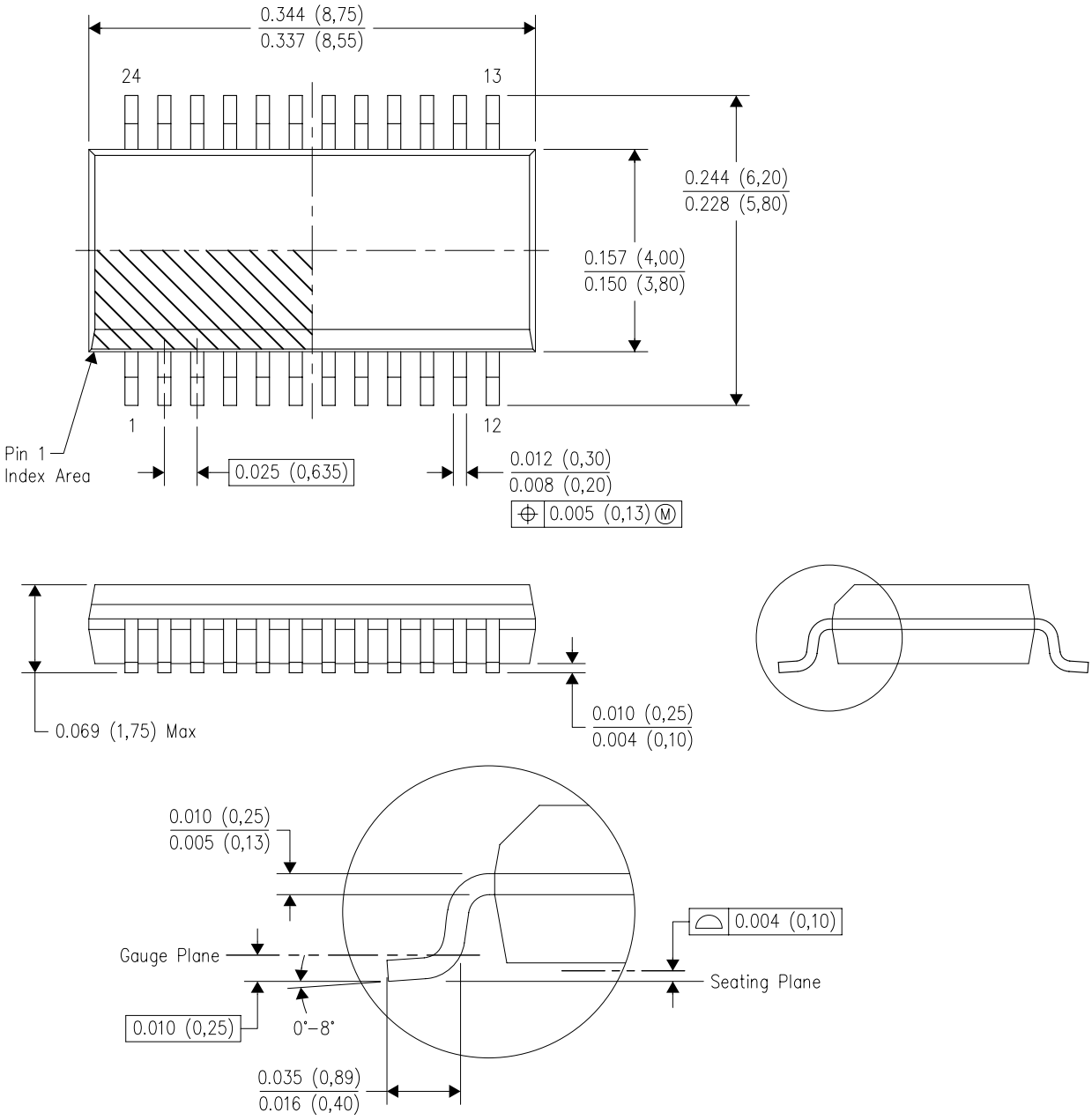
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



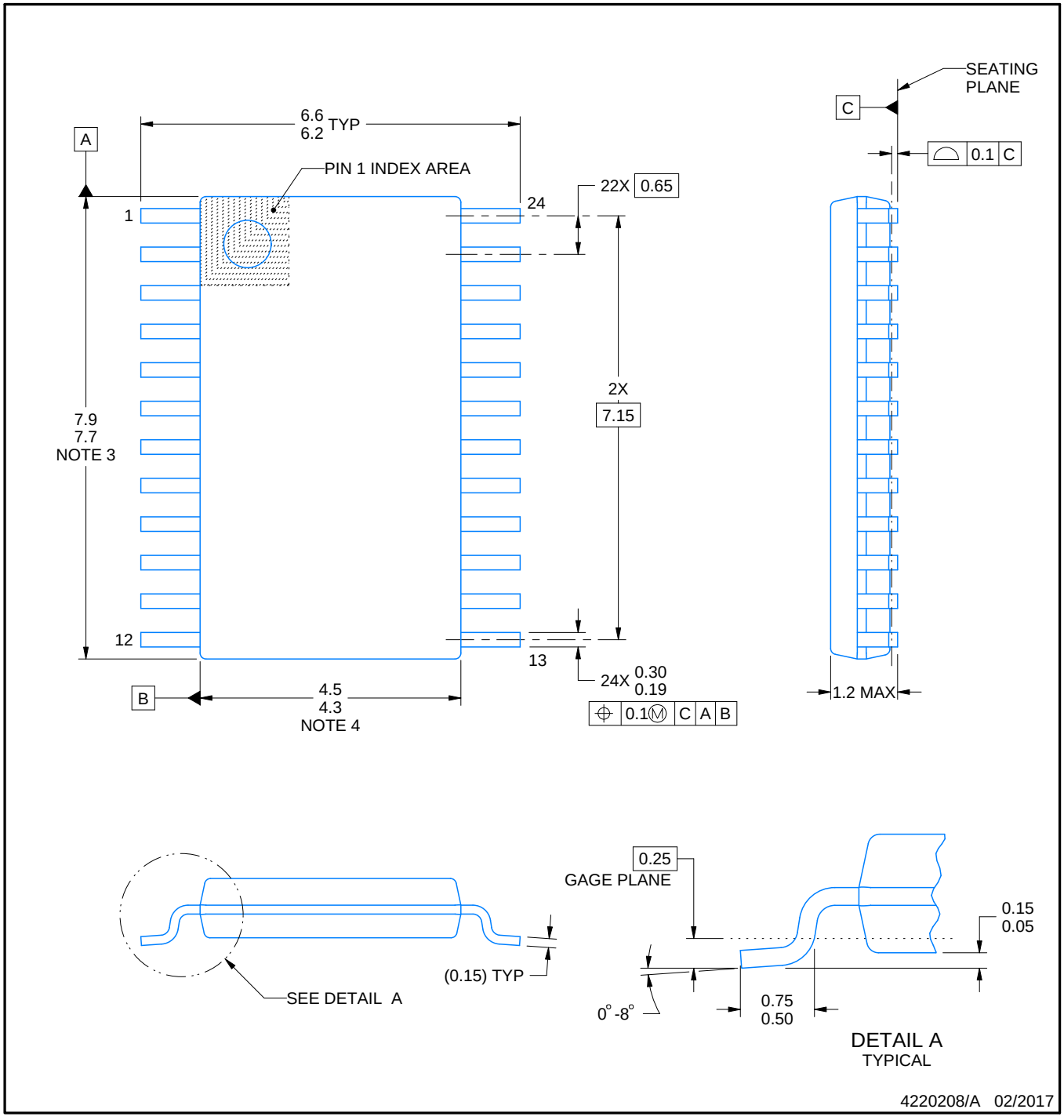
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

PACKAGE OUTLINE

PW0024A

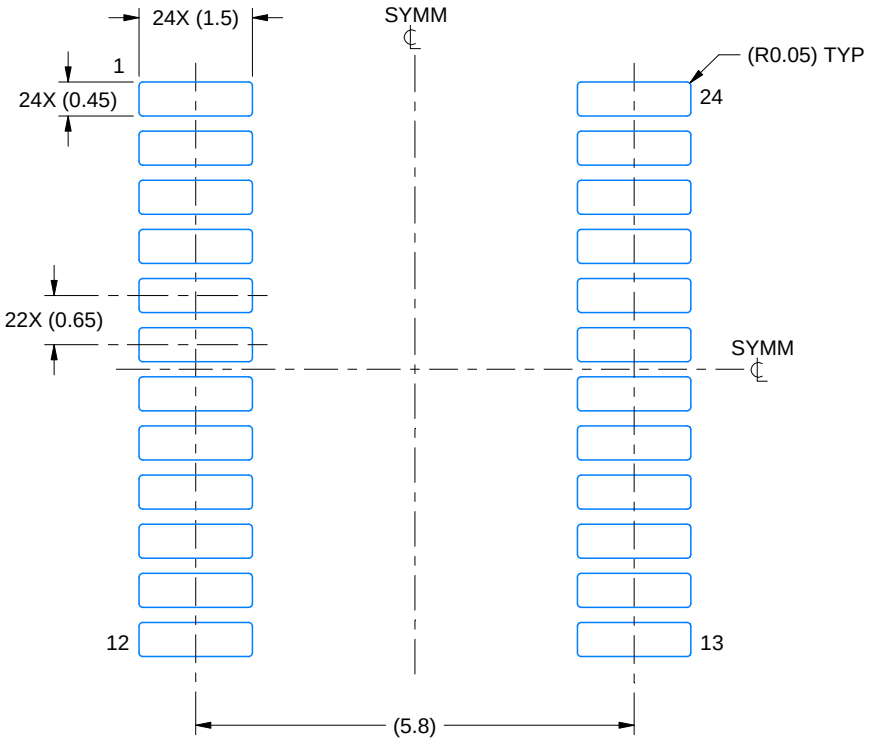
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

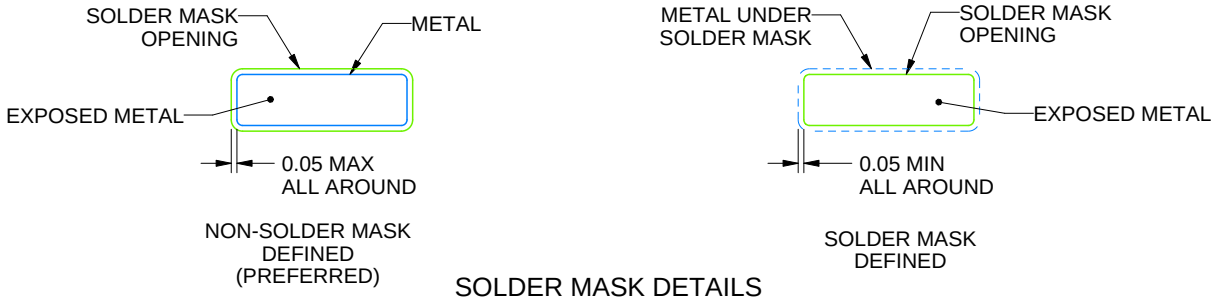


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

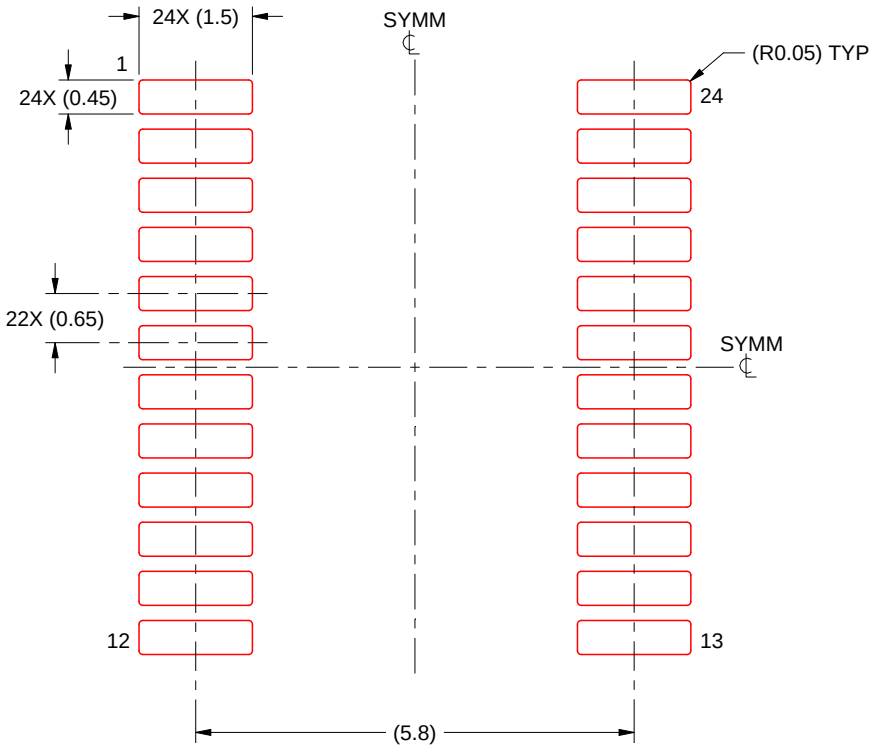


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



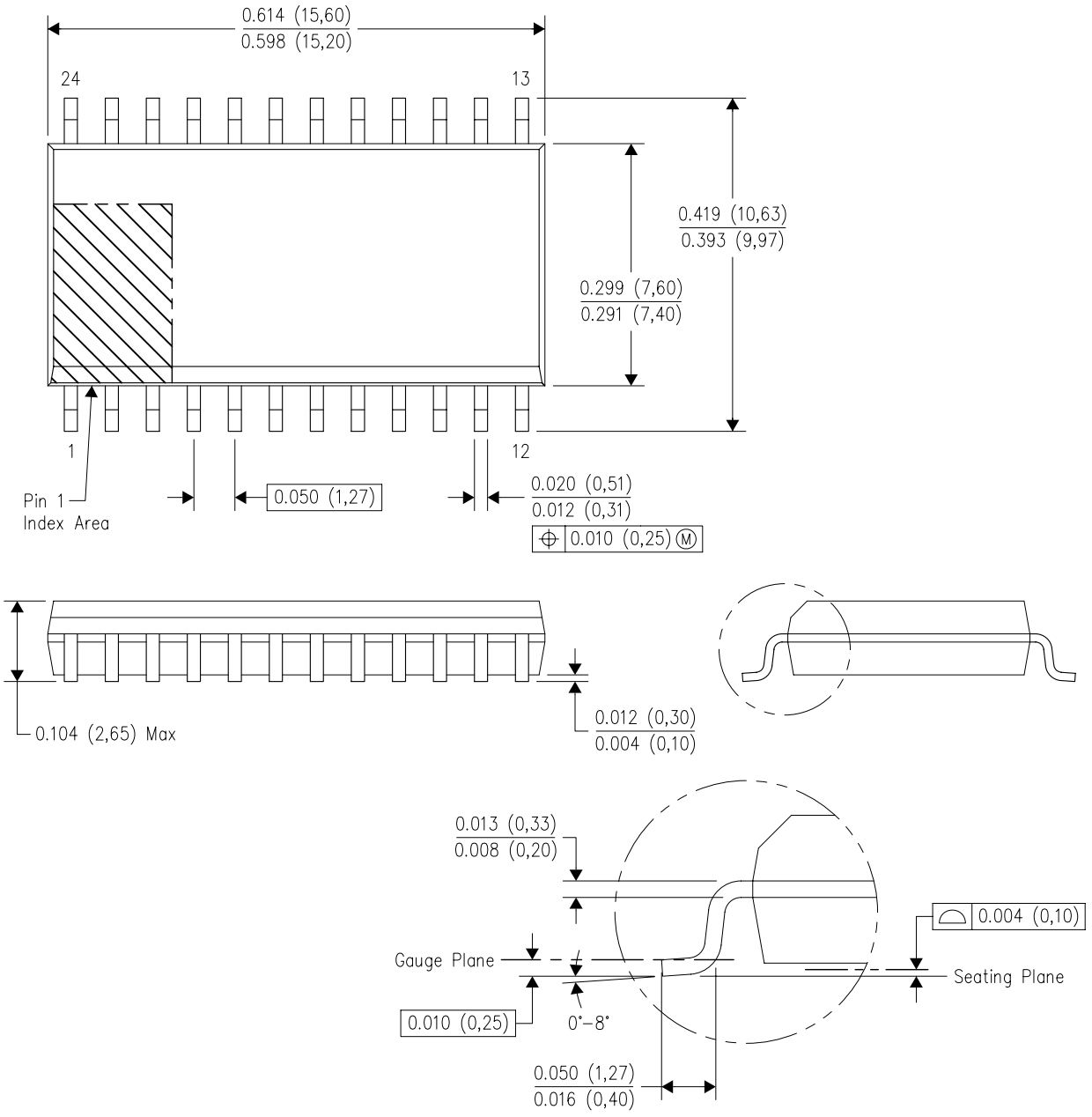
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



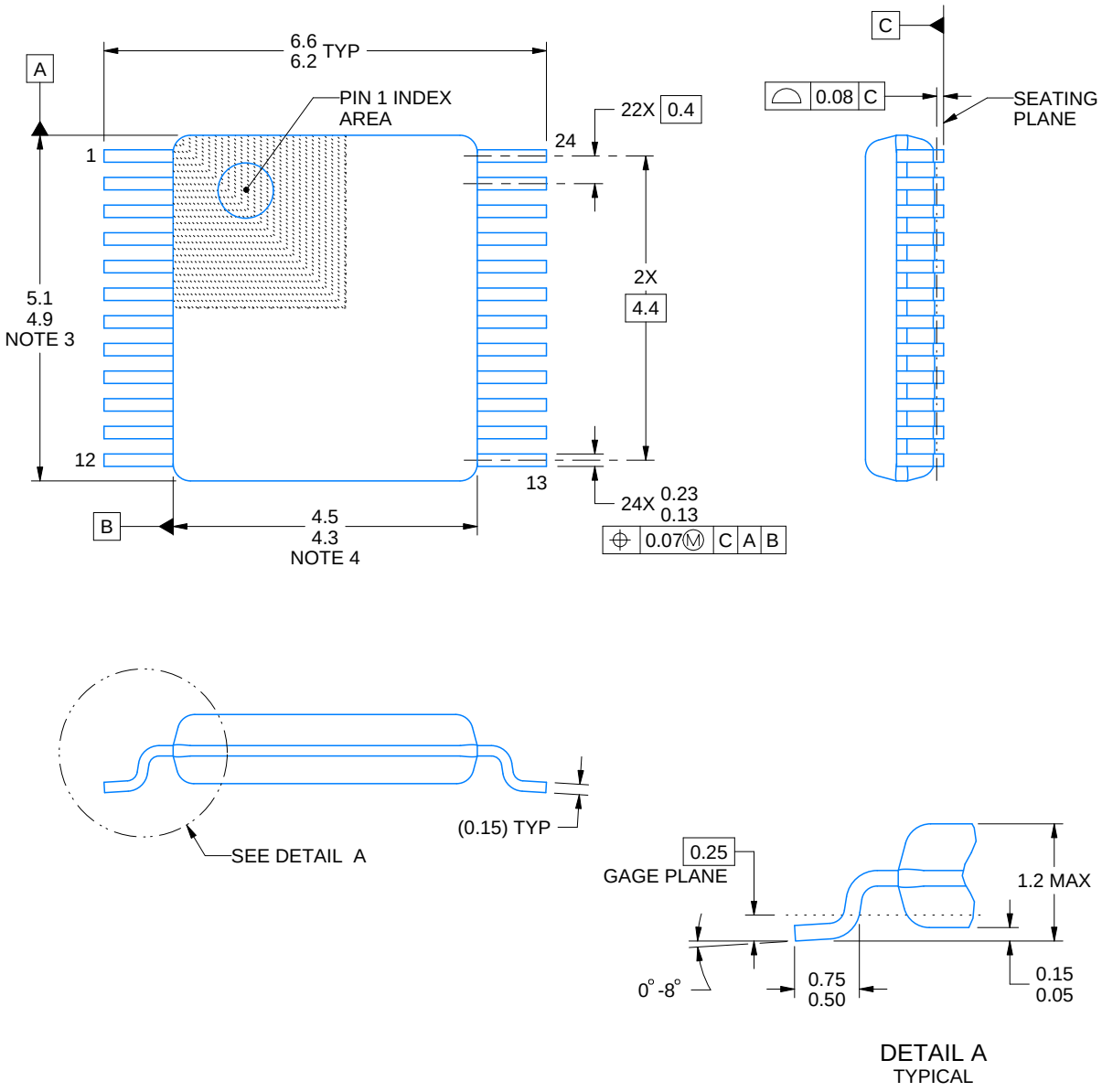
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

PACKAGE OUTLINE

DGV0024A

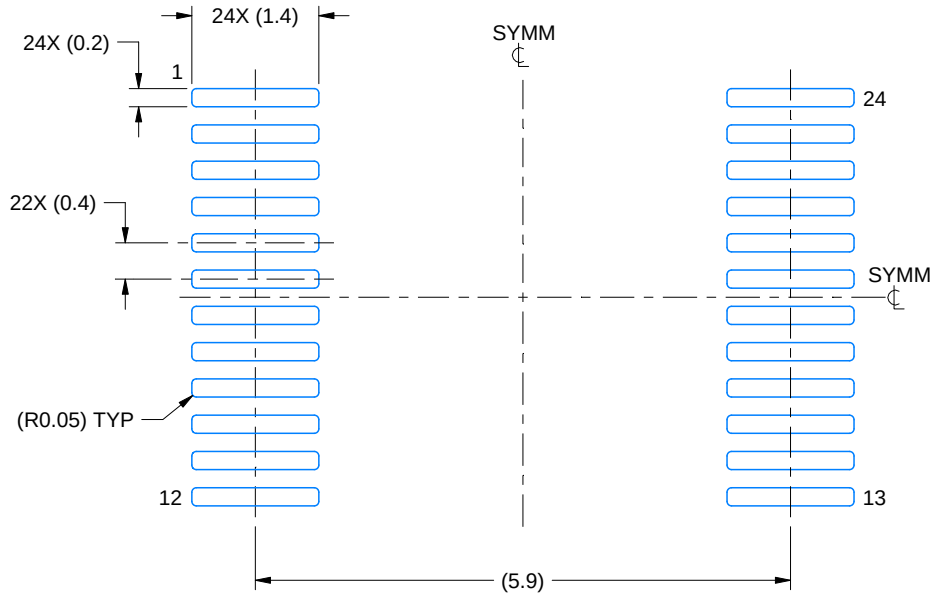
TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

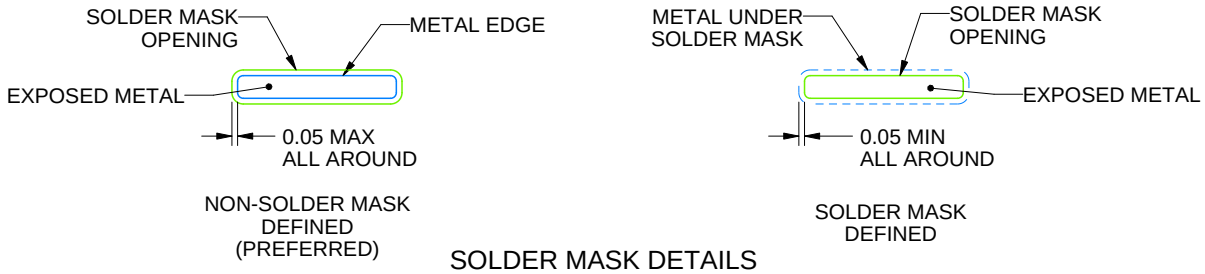


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

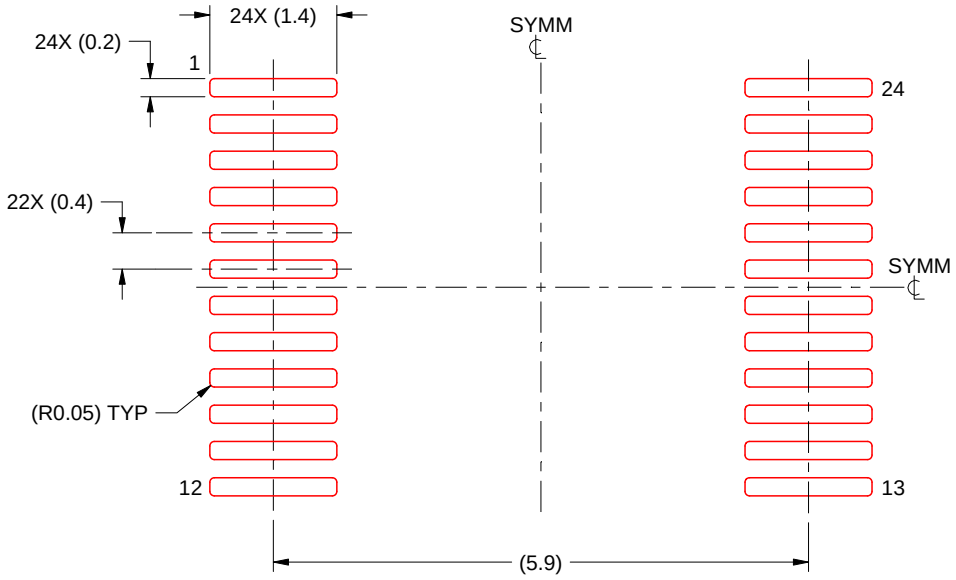


SOLDER MASK DETAILS

4229221/A 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

4229221/A 12/2022

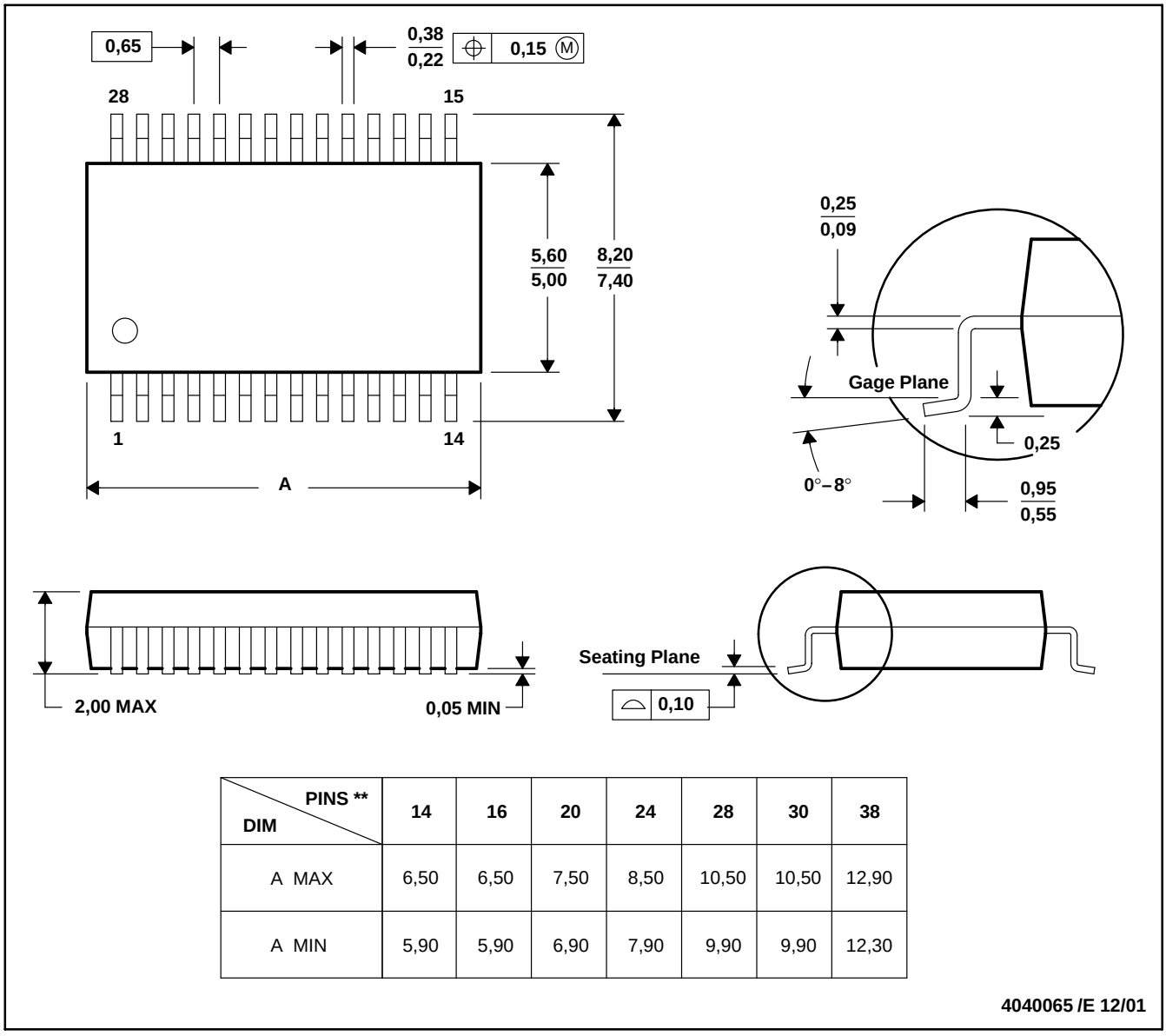
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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最終更新日：2025 年 10 月