TEXAS INSTRUMENTS
PCA9554A
JAJSLI6F – SEPTEMBER 2006 – REVISED MARCH 2021

PCA9554A 割り込み出力および構成レジスタ付き、リモート 8 ビット I²C/SMBus I/O エクスパンダ

1 特長

- I²C からパラレル・ポートへのエクスパンダ
- オープン・ドレインのアクティブ LOW 割り込み出力
- 2.3V～5.5V の動作電源電圧範囲
- 5V 対応の I/O
- 400kHz の高速 I²C バス
- 3 本のハードウェア・アドレス・ピンにより、最大 8 個のデバイスを I²C/SMBus に接続可能
- 入力 / 出力構成レジスタ
- 極性反転レジスタ
- パワーオン・リセット機能を内蔵
- 電源投入時はすべてのチャネルが入力に構成された状態
- 電源オン時のグリッチなし
- 大電流の最大駆動能力を持つラッチ付き出力により、LED を直接駆動
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を超える ESD 保護
  - 2000V、人体モデル (A114-A)
  - 200V、マシン・モデル (A115-A)
  - 1000V、デバイス帯電モデル (C101)

2 概要

この 2 線式双方向バス (I²C) 用 8 ビット I/O エクスパンダは、2.3V～5.5V の V_{CC} で動作するように設計されています。I²C インターフェイス [シリアル・クロック (SCL)、シリアル・データ (SDA)] により、ほとんどのマイクロコントローラ・ファミリの汎用リモート I/O 拡張に使用できます。

PCA9554A は、構成 (入力 / 出力選択)、入力、出力、極性反転 (アクティブ HIGH またはアクティブ LOW) 用の 8 ビット・レジスタをそれぞれ 1 個ずつ搭載しています。電源オン時、I/O は V_{CC} への弱いプルアップを備えた入力として構成されます。しかし、システム・マスタは、I/O 構成ビットに書き込むことで、I/O を入力または出力としてイネーブルできます。それぞれの入力または出力のデータは、対応する入力または出力レジスタに保持されます。入力ポート・レジスタの極性は、極性反転レジスタで反転できます。すべてのレジスタをシステム・マスタで読み出すことができます。

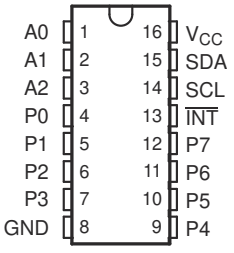
タイムアウトまたはその他の不適切な動作が発生した場合、システム・マスタはパワーオン・リセット機能を利用して PCA9554A をリセットできます。これにより、レジスタはデフォルト状態になり、I²C/SMBus ステート・マシンは初期化されます。

製品情報

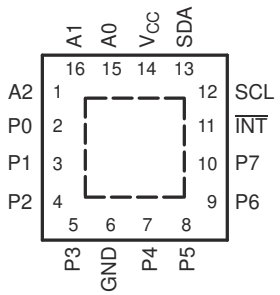
部品番号	パッケージ(1)	本体サイズ (公称)
PCA9554A	DB (SSOP) (16)	6.20mm × 5.30mm
	DBQ (VQFN) (16)	4.90mm × 3.90mm
	DGV (TSSOP) (16)	3.60mm × 4.40mm
	DW (SOIC)	10.3mm × 7.50mm
	PW (TSSOP)	5.00mm × 4.40mm
	RGT (VQFN)	3.00mm × 3.00mm
	RGV (VQFN)	4.00mm × 4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

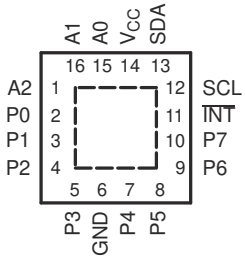
DB, DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)



RGV PACKAGE (TOP VIEW)



RGT PACKAGE (TOP VIEW)



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3 Revision History

Changes from Revision E (May 2014) to Revision F (March 2021) — **Page**

- 「*製品情報*」表を変更 ... 1
- Moved the Storage temperature range from the Handling Ratings table to the *Absolute Maximum Ratings* table ... 5
- Moved the Package thermal impedance to the *Thermal Information* table ... 5
- Changed the V_{IH} High-level input voltage (SDL, SDA) Max value From: 5.5 V To: V_{CC} in the *Recommended Operating Conditions* ... 5
- Changed the V_{IL} Low-level input voltage (A2–A0, P7–P0) Max value From: 0.8 V To: 0.3 x V_{CC} in the *Recommended Operating Conditions* ... 5
- Added the *Thermal Information* table ... 5
- Changed the V_{PORR} row in the *Electrical Characteristics* ... 6
- Added the V_{PORF} row in the *Electrical Characteristics* ... 6
- Changed the I_{CC} Standby mode values in the *Electrical Characteristics* ... 6
- Changed the C_i SCL Max value From: 5 pF To: 8 pF in the *Electrical Characteristics* ... 6
- Changed the C_{io} SDA Max value From: 6.5 pF To: 9.5 pF in the *Electrical Characteristics* ... 6
- Changed the t_{pv} Output data valid MAX values From: 200 ns To 350 ns in the *Switching Characteristics* ... 7
- Changed the *Typical Characteristics* graphs ... 8
- Changed the *Power Supply Recommendations* ... 23

Changes from Revision D (August 2008) to Revision E (May 2014) — **Page**

- Added Interrupt Errata section. ... 15
- Added the *Power-On Reset Errata* section ... 23

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4 概要 (続き)

PCA9554A のオープン・ドレイン割り込み ($\overline{INT}$) 出力は、いずれかの入力の状態が、対応する入力ポート・レジスタの状態と異なっている場合にアクティブになるため、入力状態が変化したことをシステム・マスタに示すために使用されます。

$\overline{INT}$ はマイクロコントローラの割り込み入力に接続できます。この配線で割り込み信号を送ることでリモート I/O は、I^2C バス経由で通信しなくてもポート上に受信データが存在するかどうかをマイクロコントローラに通知できます。そのため、PCA9554A はシンプル・スレーブ・デバイスとして機能できます。

本デバイスの出力 (ラッチ付き) は大電流駆動能力を備えているため LED を直接駆動でき、低消費電流です。

3 本のハードウェア・ピン (A0、A1、A2) を使って固定 I^2C アドレスをプログラムおよび変更することで、最大 8 つのデバイスが同じ I^2C バスまたは SMBus を共有できます。

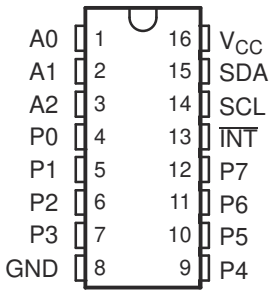
PCA9554A は PCF8574A とピン互換、I^2C アドレス互換です。しかし PCA9554A では、PCF8574A に対して機能が拡張されているため、ソフトウェアを変更する必要があります。

PCA9554A と PCA9554 は、固定 I^2C アドレスを除くと同じです。そのため、これらのデバイス最大 16 個 (各 8 個) を同じ I^2C/SMBus に接続できます。

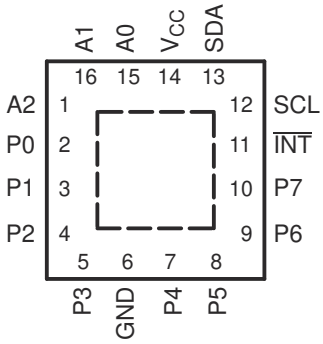
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5 Pin Configuration And Functions

DB, DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)



RGV PACKAGE (TOP VIEW)



RGT PACKAGE (TOP VIEW)

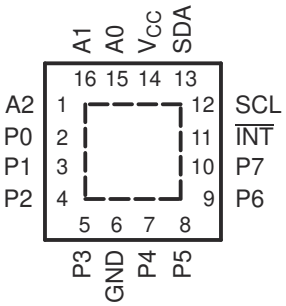


表 5-1. Pin Functions

PIN			DESCRIPTION
NAME	QSOP (DBQ) SOIC (DW), SSOP (DB), TSSOP (PW), AND TVSOP (DGV)	QFN (RGT AND RGV)	
A0	1	15	Address input. Connect directly to V_{CC} or ground.
A1	2	16	Address input. Connect directly to V_{CC} or ground.
A2	3	1	Address input. Connect directly to V_{CC} or ground.
P0	4	2	P-port input/output. Push-pull design structure.
P1	5	3	P-port input/output. Push-pull design structure.
P2	6	4	P-port input/output. Push-pull design structure.
P3	7	5	P-port input/output. Push-pull design structure.
GND	8	6	Ground
P4	9	7	P-port input/output. Push-pull design structure.
P5	10	8	P-port input/output. Push-pull design structure.
P6	11	9	P-port input/output. Push-pull design structure.
P7	12	10	P-port input/output. Push-pull design structure.
$\overline{INT}$	13	11	Interrupt output. Connect to V_{CC} through a pullup resistor.
SCL	14	12	Serial clock bus. Connect to V_{CC} through a pullup resistor.
SDA	15	13	Serial data bus. Connect to V_{CC} through a pullup resistor.
V_{CC}	16	14	Supply voltage

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6	V
V_I	Input voltage range(2)		–0.5	6	V
V_O	Output voltage range(2)		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_{IOK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	V_O = 0 to V_{CC}		50	mA
I_{OH}	Continuous output high current	V_O = 0 to V_{CC}		–50	mA
I_{CC}	Continuous current through GND			–250	mA
	Continuous current through V_{CC}			160	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	0.7 × V_{CC}	V_{CC}	V
		A2–A0, P7–P0	2	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	0.3 × V_{CC}	V
		A2–A0, P7–P0	–0.5	0.3 × V_{CC}	
I_{OH}	High-level output current	P7–P0		–10	mA
I_{OL}	Low-level output current	P7–P0		25	mA
T_A	Operating free-air temperature		–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		PCA9554A							UNIT
		DB (SSOP)	DBQ (SSOP)	DGV (TVSOP)	DW (SOIC)	PW (TSSOP)	RGT (TSSOP)	RGV (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113.2	121.7	120	84.7	122	63.2	51	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA	2.3 V to 5.5 V	–1.2			V
V_{PORR}	Power-onreset voltage,V_{CC} rising	V_I = V_{CC} or GND, I_O = 0			1.2	1.5	V
V_{PORF}	Power-onreset voltage,V_{CC} falling	V_I = V_{CC} or GND, I_O = 0		0.75	1		V
V_{OH}	P-port high-level output voltage(2)	I_{OH} = –8 mA	2.3 V	1.8			V
			3 V	2.6			
			4.5 V	3.1			
			4.75 V	4.1			
		I_{OH} = –10 mA	2.3 V	1.7			
			3 V	2.5			
			4.5 V	3			
			4.75 V	4			
I_{OL}	SDA	V_{OL} = 0.4 V	2.3 V to 5.5 V	3	8		mA
	P port(3)	V_{OL} = 0.5 V	2.3 V	8	10		
			3 V	8	14		
			4.5 V	8	17		
			4.75 V	8	35		
		V_{OL} = 0.7 V	2.3 V	10	13		
			3 V	10	19		
			4.5 V	10	24		
			4.75 V	10	45		
	$\overline{INT}$	V_{OL} = 0.4 V	2.3 V to 5.5 V	3	10		
I_I	SCL, SDA	V_I = V_{CC} or GND	2.3 V to 5.5 V			±1	µA
	A2–A0					±1	
I_{IH}	P port	V_I = V_{CC}	2.3 V to 5.5 V			1	µA
I_{IL}	P port	V_I = GND	2.3 V to 5.5 V			–100	µA
I_{CC}	Operating mode	V_I = V_{CC}, I_O = 0, I/O = inputs, f_{scl} = 400 kHz, No load	5.5 V		104	175	µA
			3.6 V		50	90	
			2.7 V		20	65	
		V_I = V_{CC}, I_O = 0, I/O = inputs, f_{scl} = 100 kHz, No load	5.5 V		60	150	
			3.6 V		15	40	
			2.7 V		8	20	
	Standby mode	V_I = GND, I_O = 0, I/O = inputs, f_{scl} = 0 kHz, No load	5.5 V		450	700	
			3.6 V		300	600	
			2.7 V		230	500	
		V_I = V_{CC}, I_O = 0, I/O = inputs, f_{scl} = 0 kHz, No load	5.5 V		1.9	3.5	
			3.6 V		1.1	1.8	
			2.7 V		1	1.6	
ΔI_{CC}	Additional current in standby mode	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V			1.5	mA
		Every LED I/O at V_I = 4.3 V; f_{scl} = 0 kHz	5.5 V			1	
C_I	SCL	V_I = V_{CC} or GND	2.3 V to 5.5 V		4	8	pF
C_{io}	SDA	V_{IO} = V_{CC} or GND	2.3 V to 5.5 V		5.5	9.5	pF
	P port				8	9.5	

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}) and T_A = 25°C.
(2) The total current sourced by all I/Os must be limited to 85 mA.
(3) Each I/O must be externally limited to a maximum of 25 mA, and the P port (P0 to P7) must be limited to a maximum current of 200 mA.

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6.6 I²C Interface Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see 図 7-1)

			STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
			MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency		0	100	0	400	kHz
t_{sch}	I²C clock high time		4		0.6		µs
t_{scl}	I²C clock low time		4.7		1.3		µs
t_{sp}	I²C spike time			50		50	ns
t_{sds}	I²C serial-data setup time		250		100		ns
t_{sdh}	I²C serial-data hold time		0		0		ns
t_{icr}	I²C input rise time			1000	$20 + 0.1C_b$ (1)	300	ns
t_{icf}	I²C input fall time			300	$20 + 0.1C_b$ (1)	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	$20 + 0.1C_b$ (1)	300	ns
t_{buf}	I²C bus free time between Stop and Start		4.7		1.3		µs
t_{sts}	I²C Start or repeated Start condition setup		4.7		0.6		µs
t_{sth}	I²C Start or repeated Start condition hold		4		0.6		µs
t_{sps}	I²C Stop condition setup		4		0.6		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid	300		50		ns
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low	0.3	3.45	0.1	0.9	µs
C_b	I²C bus capacitive load			400		400	ns

(1) C_b = Total capacitive load of one bus in pF

6.7 Switching Characteristics

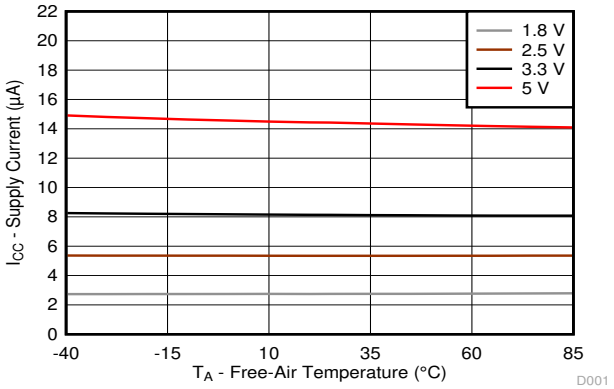
over operating free-air temperature range (unless otherwise noted) (see 図 7-2 and 図 7-3)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
				MIN	MAX	MIN	MAX	
t_{iv}	Interrupt valid time	P port	$\overline{INT}$		4		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$		4		4	µs
t_{pv}	Output data valid	SCL	P7–P0		350		350	ns
t_{ps}	Input data setup time	P port	SCL	100		100		ns
t_{ph}	Input data hold time	P port	SCL	1		1		µs

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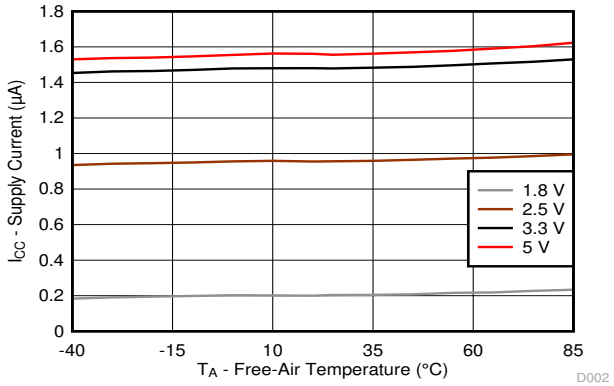
6.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)



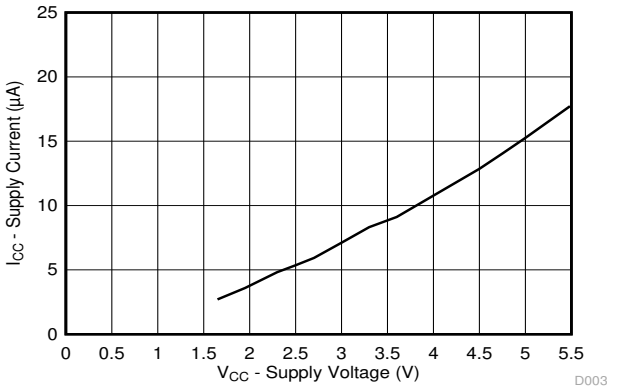
f_{SCL} = 400 kHz I/Os = High or Low Inputs

図 6-1. Supply Current (I_{CC}, Operating Mode) vs Temperature (T_A) at Four Supply Voltages



f_{SCL} = 0 kHz I/Os = High Inputs

図 6-2. Supply Current (ICC, Standby Mode) vs Temperature (T_A) at Four Supply Voltages



f_{SCL} = 400 kHz I/Os = High or Low Inputs T_A = 25°C

図 6-3. Supply Current (I_{CC}, Operating Mode) vs Supply Voltage (V_{CC})

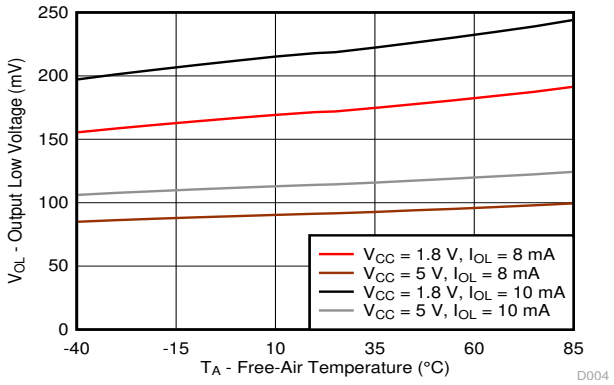
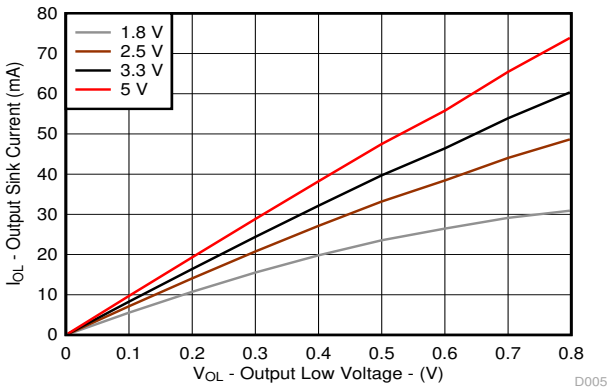


図 6-4. Output Low Voltage (V_{OL}) vs Temperature (T_A) for P-Port I/Os



T_A = 25°C

図 6-5. Sink Current (I_{OL}) vs Output Low Voltage (V_{OL}) for P-Ports at Four Supply Voltages

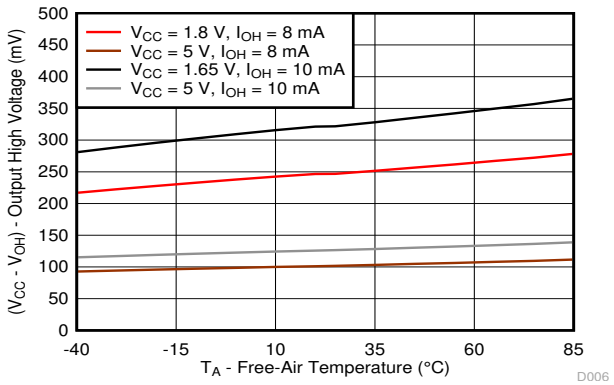
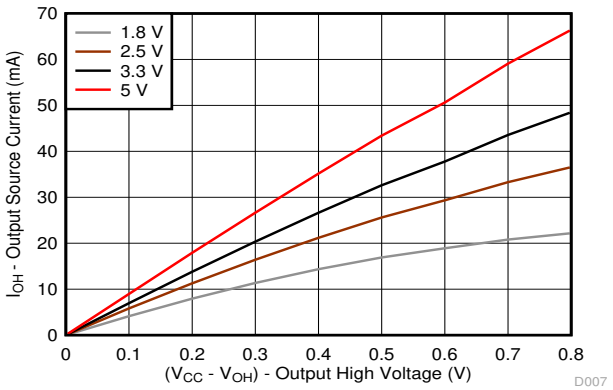


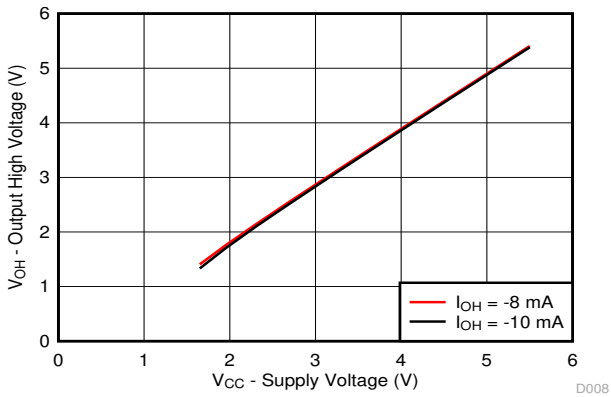
図 6-6. Output High Voltage (V_{CC} – V_{OH}) vs Temperature (T_A) for P-Ports

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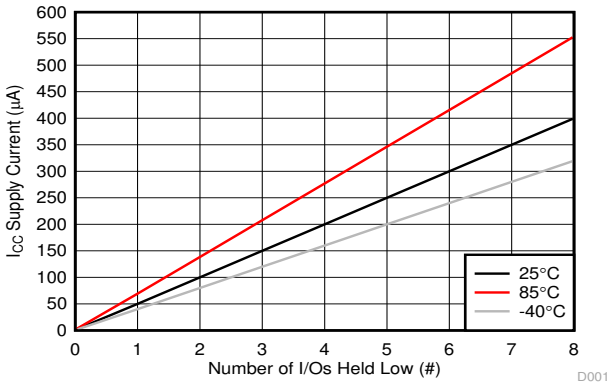
T_A = 25°C

図 6-7. Source Current (I_{OH}) vs Output High Voltage (V_{OH}) for P-Ports at Four Supply Voltages



T_A = 25°C

図 6-8. Output High Voltage (V_{OH}) vs Supply Voltage (V_{CC}) for P-Ports



V_{CC} = 5 V

図 6-9. Supply Current (I_{CC}) vs Number of I/Os Held Low (#)

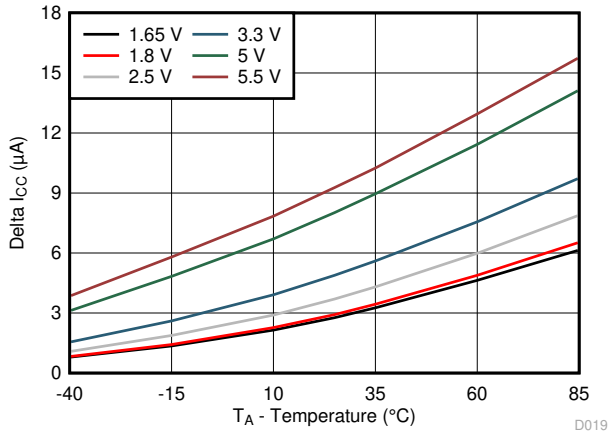
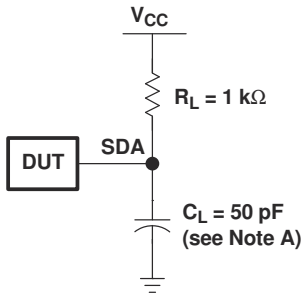
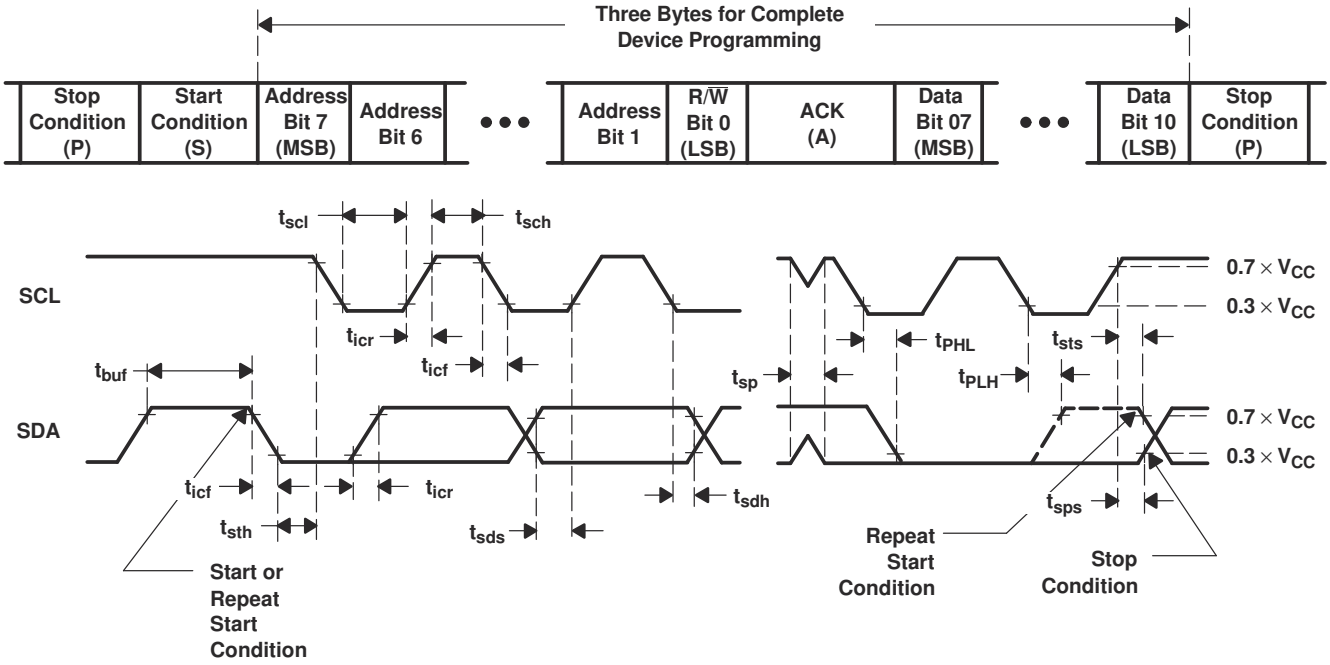


図 6-10. Δ I_{CC} vs Temperature for Different V_{CC} (V_I = V_{CC} – 0.6 V)

7 Parameter Measurement Information



SDA LOAD CONFIGURATION



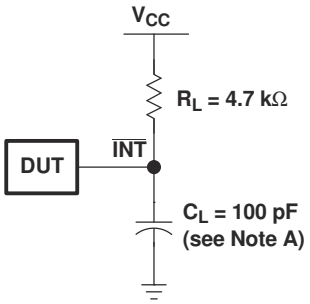
VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

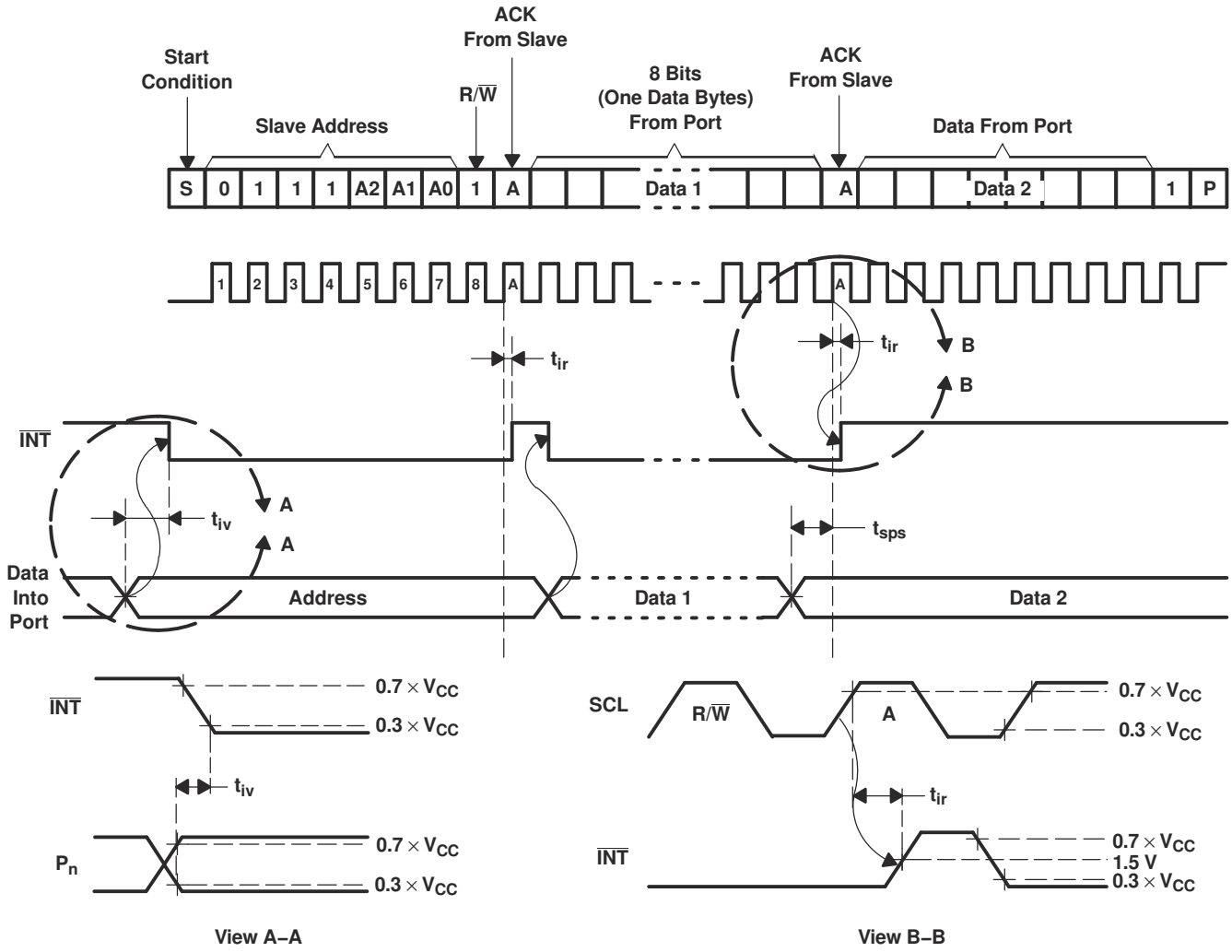
A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
C. All parameters and waveforms are not applicable to all devices.

図 7-1. I^2C Interface Load Circuit And Voltage Waveforms

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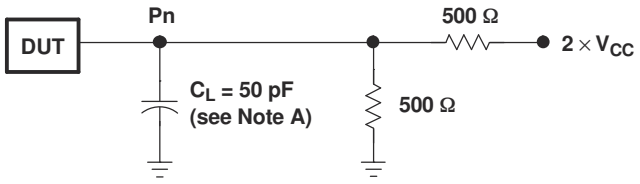
INTERRUPT LOAD CONFIGURATION



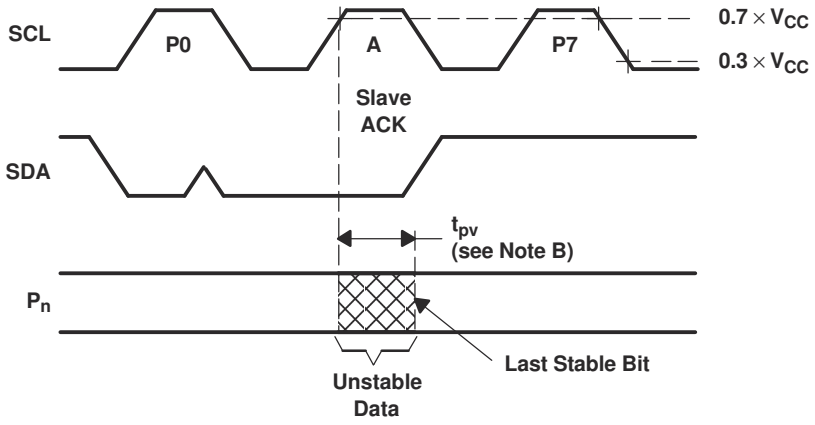
A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
C. All parameters and waveforms are not applicable to all devices.

図 7-2. Interrupt Load Circuit And Voltage Waveforms

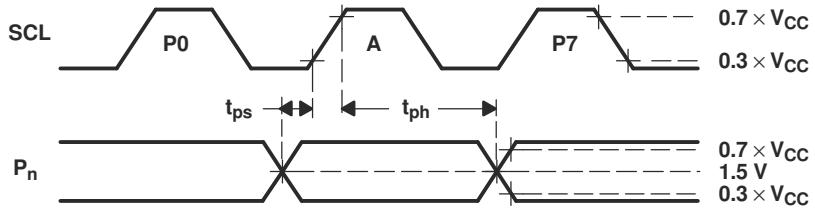
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P-PORT LOAD CONFIGURATION



WRITE MODE (R/$\overline{W}$ = 0)



READ MODE (R/$\overline{W}$ = 1)

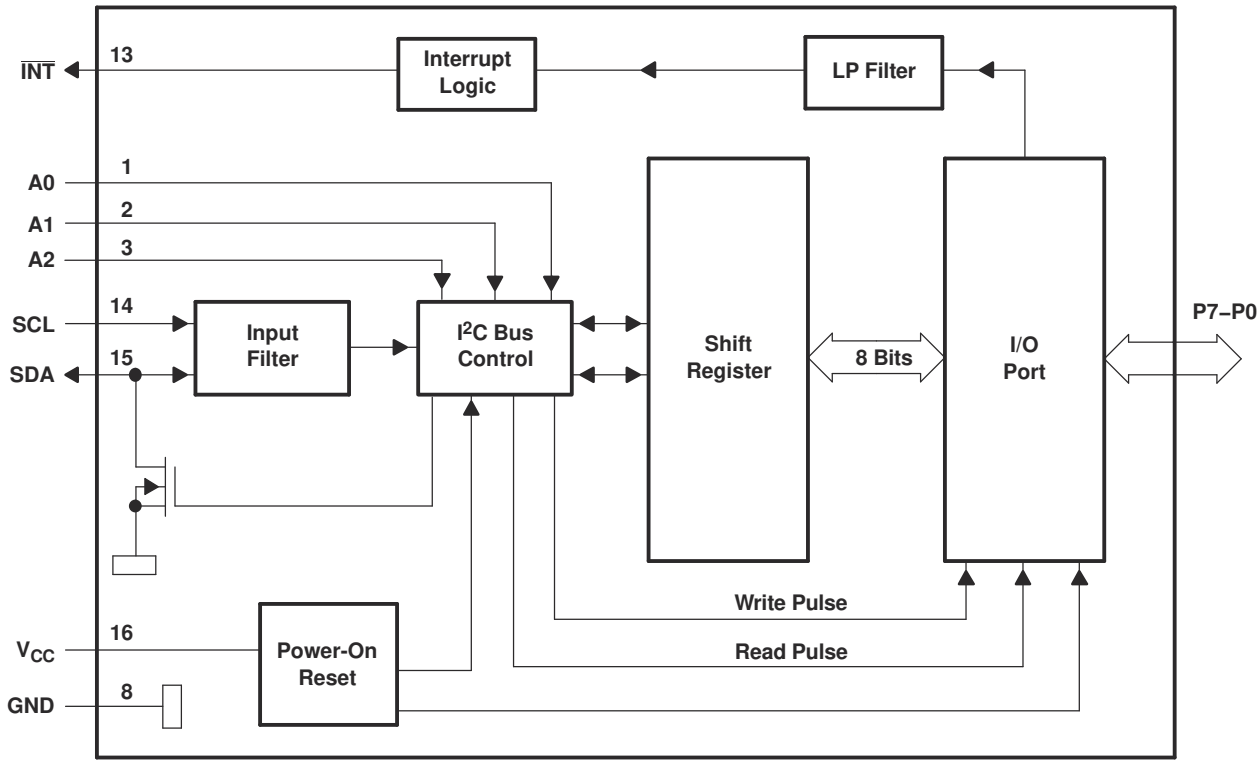
A. C_L includes probe and jig capacitance.
B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O pin output.
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

図 7-3. P-Port Load Circuit And Voltage Waveforms

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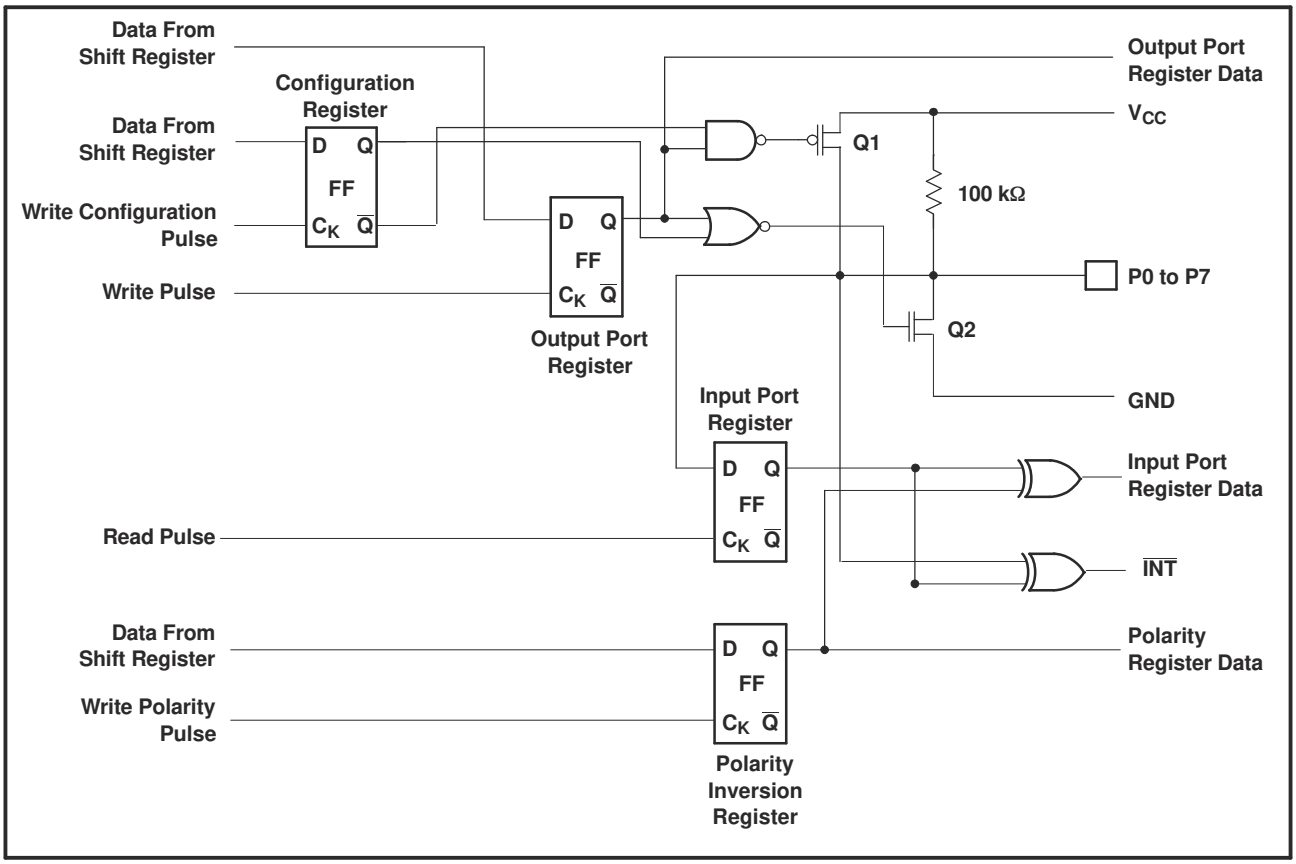
8 Detailed Description

8.1 Functional Block Diagram



A. Pin numbers shown are for the DB, DBQ, DGV, DW, or PW package.
B. All I/Os are set to inputs at reset.

図 8-1. Logic Diagram



A. At power-on reset, all registers return to default values.

図 8-2. Simplified Schematic Of P0 To P7

8.2 Device Functional Modes

8.2.1 Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the PCA9554A in a reset condition until V_{CC} has reached V_{PORR}. At that point, the reset condition is released and the PCA9554A registers and I^2C/SMBus state machine will initialize to their default states. After that, V_{CC} must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

8.2.2 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 (in 図 8-2) are off, which creates a high impedance input with a weak pullup (100 kΩ typ) to V_{CC}. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

8.2.3 Interrupt Output ($\overline{INT}$)

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting, data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$. Writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an

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interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register. Because each 8-pin port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1 or vice versa.

The $\overline{INT}$ output has an open-drain structure and requires pull-up resistor to V_{CC}.

8.2.3.1 Interrupt Errata

8.2.3.1.1 Description

The INT will be improperly de-asserted if the following two conditions occur:

1. The last I²C command byte (register pointer) written to the device was 00h.

Note

This generally means the last operation with the device was a Read of the input register. However, the command byte may have been written with 00h without ever going on to read the input register. After reading from the device, if no other command byte written, it will remain 00h.

2. Any other slave device on the I²C bus acknowledges an address byte with the R/W bit set high

8.2.3.1.2 System Impact

Can cause improper interrupt handling as the Master will see the interrupt as being cleared.

8.2.3.1.3 System Workaround

Minor software change: User must change command byte to something besides 00h after a Read operation to the PCA9554A device or before reading from another slave device.

Note

Software change will be compatible with other versions (competition and TI redesigns) of this device.

8.3 Programming

8.3.1 I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see 図 8-3). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/ $\overline{W}$).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the Start and Stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see 図 8-4).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see 図 8-3).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see 図 8-5). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

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A master receiver will signal an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

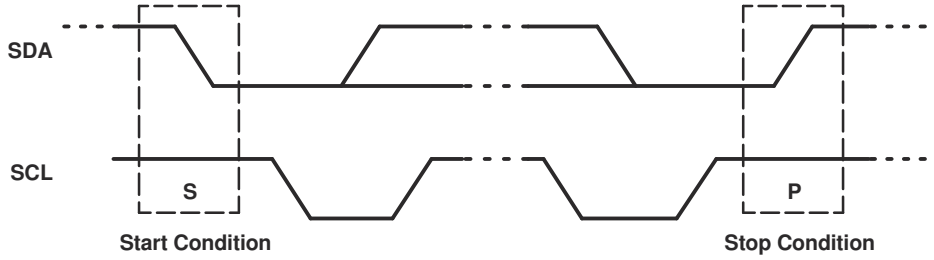


図 8-3. Definition Of Start And Stop Conditions

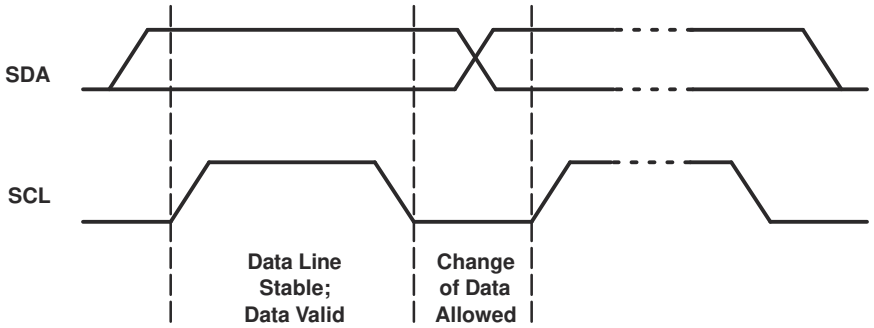


図 8-4. Bit Transfer

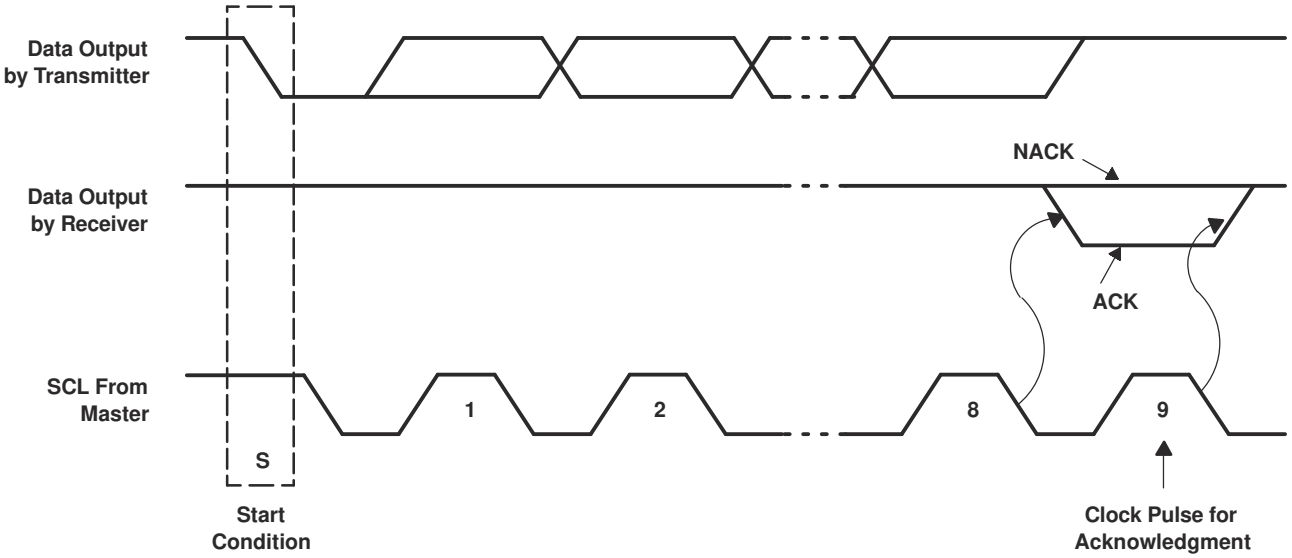


図 8-5. Acknowledgment On The I²C Bus

8.3.2 Register Map

表 8-1. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I^2C slave address	L	H	H	H	A2	A1	A0	R/ $\overline{W}$
Px I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

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8.3.2.1 Device Address

図 8-6 shows the address byte for the PCA9554A.

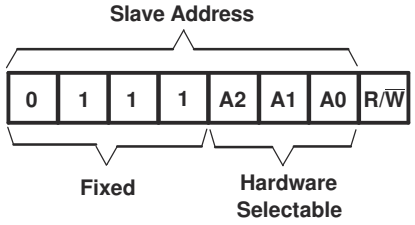


図 8-6. Pca9554a Address

表 8-2. Address Reference

INPUTS			I²C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	56 (decimal), 38 (hexadecimal)
L	L	H	57 (decimal), 39 (hexadecimal)
L	H	L	58 (decimal), 3A (hexadecimal)
L	H	H	59 (decimal), 3B (hexadecimal)
H	L	L	60 (decimal), 3C (hexadecimal)
H	L	H	61 (decimal), 3D (hexadecimal)
H	H	L	62 (decimal), 3E (hexadecimal)
H	H	H	63 (decimal), 3F (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected. A low (0) selects a write operation.

8.3.2.2 Control Register And Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the PCA9554A. Two bits of this command byte state the operation (read or write) and the internal register (input, output, polarity inversion or configuration) that will be affected. This register can be written or read through the I²C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

0	0	0	0	0	0	B1	B0

図 8-7. Control Register Bits

表 8-3. Command Byte

CONTROL REGISTER BITS		COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B1	B0				
0	0	0x00	Input Port	Read byte	XXXX XXXX
0	1	0x01	Output Port	Read/write byte	1111 1111
1	0	0x02	Polarity Inversion	Read/write byte	0000 0000
1	1	0x03	Configuration	Read/write byte	1111 1111

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8.3.2.3 Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to let the I^2C device know that the Input Port register will be accessed next.

表 8-4. Register 0 (Input Port Register)

BIT	I7	I6	I5	I4	I3	I2	I1	I0
DEFAULT	X	X	X	X	X	X	X	X

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

表 8-5. Register 1 (Output Port Register)

BIT	O7	O6	O5	O4	O3	O2	O1	O0
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin original polarity is retained.

表 8-6. Register 2 (Polarity Inversion Register)

BIT	N7	N6	N5	N4	N3	N2	N1	N0
DEFAULT	0	0	0	0	0	0	0	0

The Configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with high impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

表 8-7. Register 3 (Configuration Register)

BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	1	1	1	1	1	1	1	1

8.3.2.4 Bus Transactions

Data is exchanged between the master and PCA9554A through write and read commands.

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8.3.2.4.1 Writes

Data is transmitted to the PCA9554A by sending the device address and setting the least-significant bit to a logic 0 (see 図 8-6 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte (see 図 8-8 and 図 8-9). There is no limitation on the number of data bytes sent in one write transmission.

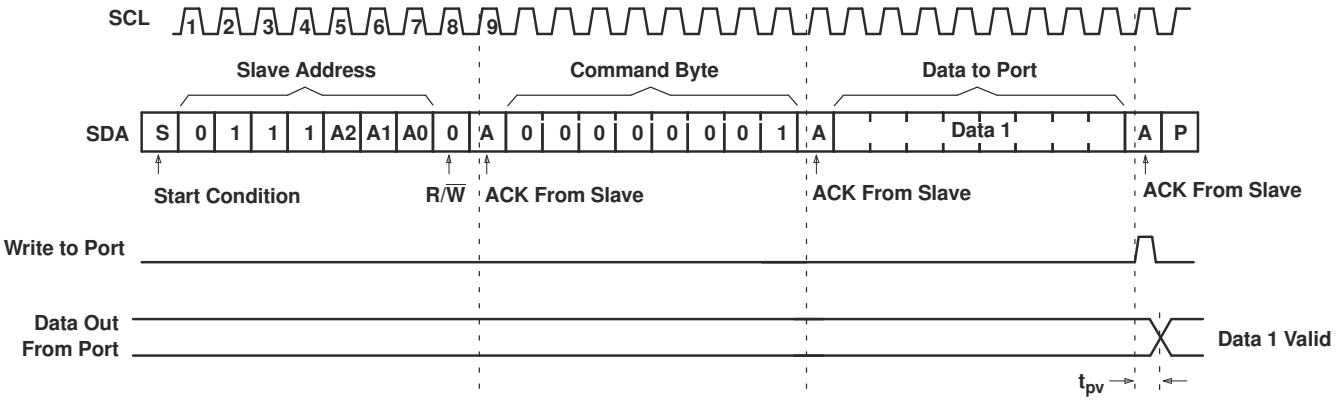


図 8-8. Write To Output Port Register

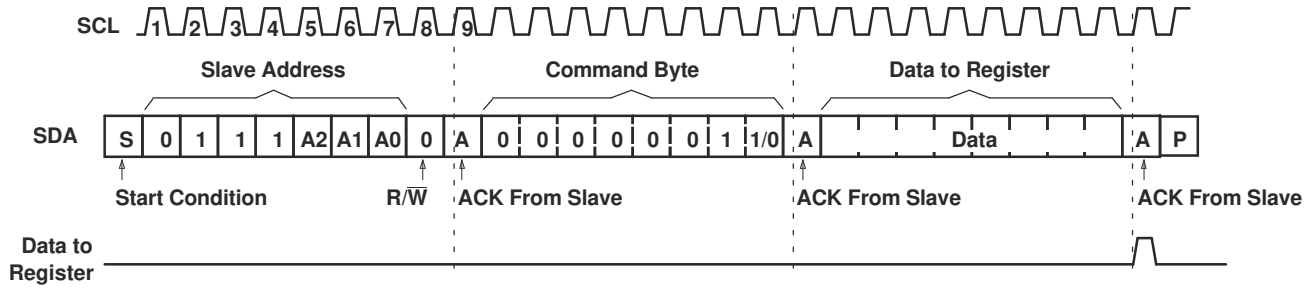


図 8-9. Write To Configuration Or Polarity Inversion Registers

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8.3.2.4.2 Reads

The bus master first must send the PCA9554A address with the least significant bit (LSB) set to a logic 0 (see 図 8-6 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again, but this time the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9554A (see 図 8-10 and 図 8-11). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

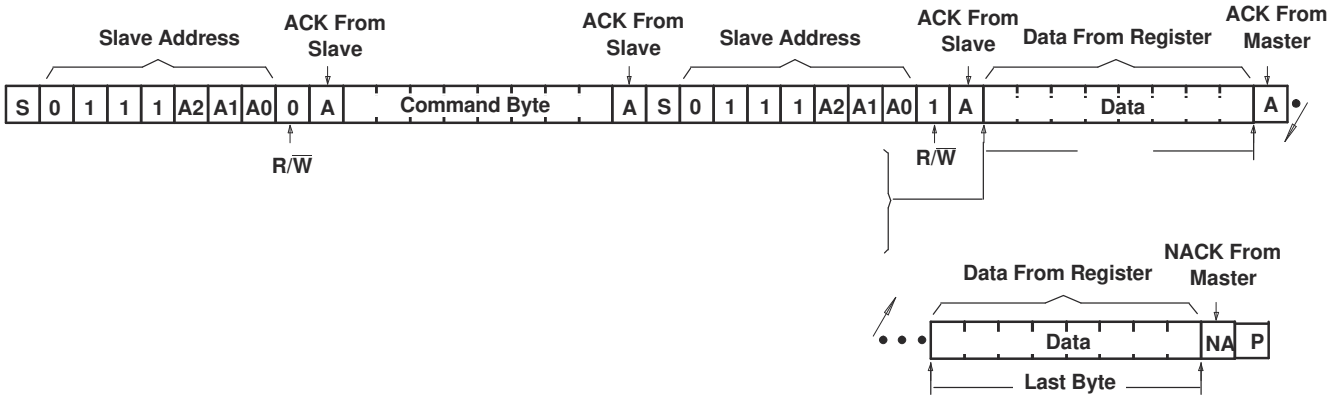
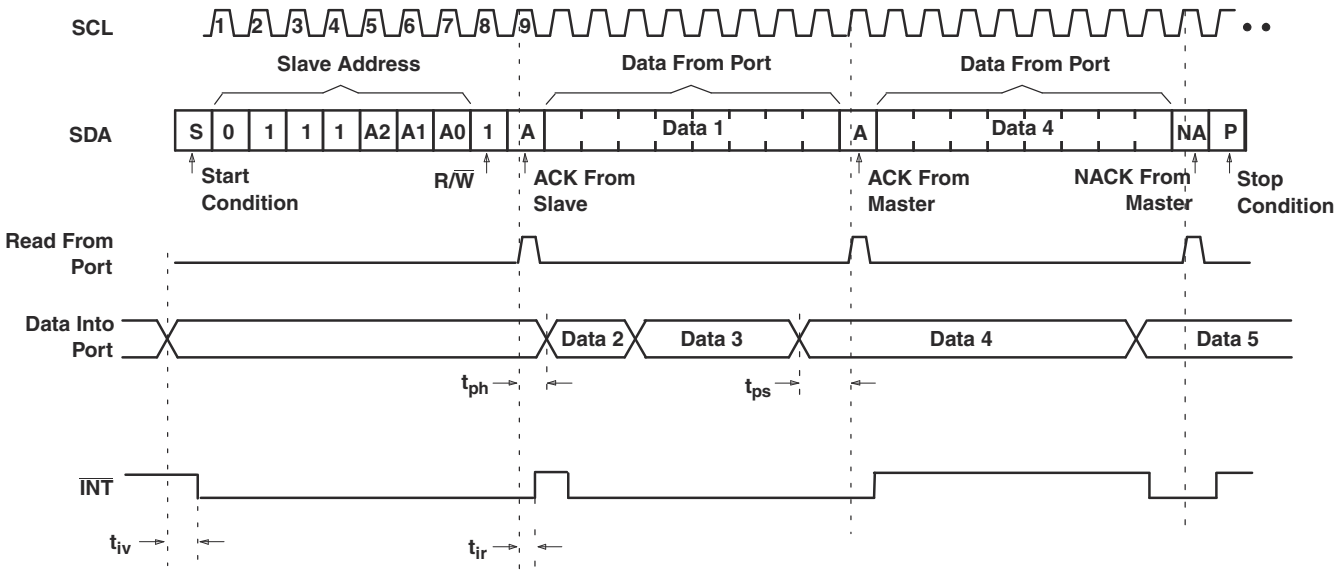


図 8-10. Read From Register



A. This figure assumes the command byte has previously been programmed with 00h.
B. Transfer of data can be stopped at any moment by a Stop condition.
C. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port. See 図 8-10 for these details.

図 8-11. Read From Input Port Register

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9 Application Information Disclaimer

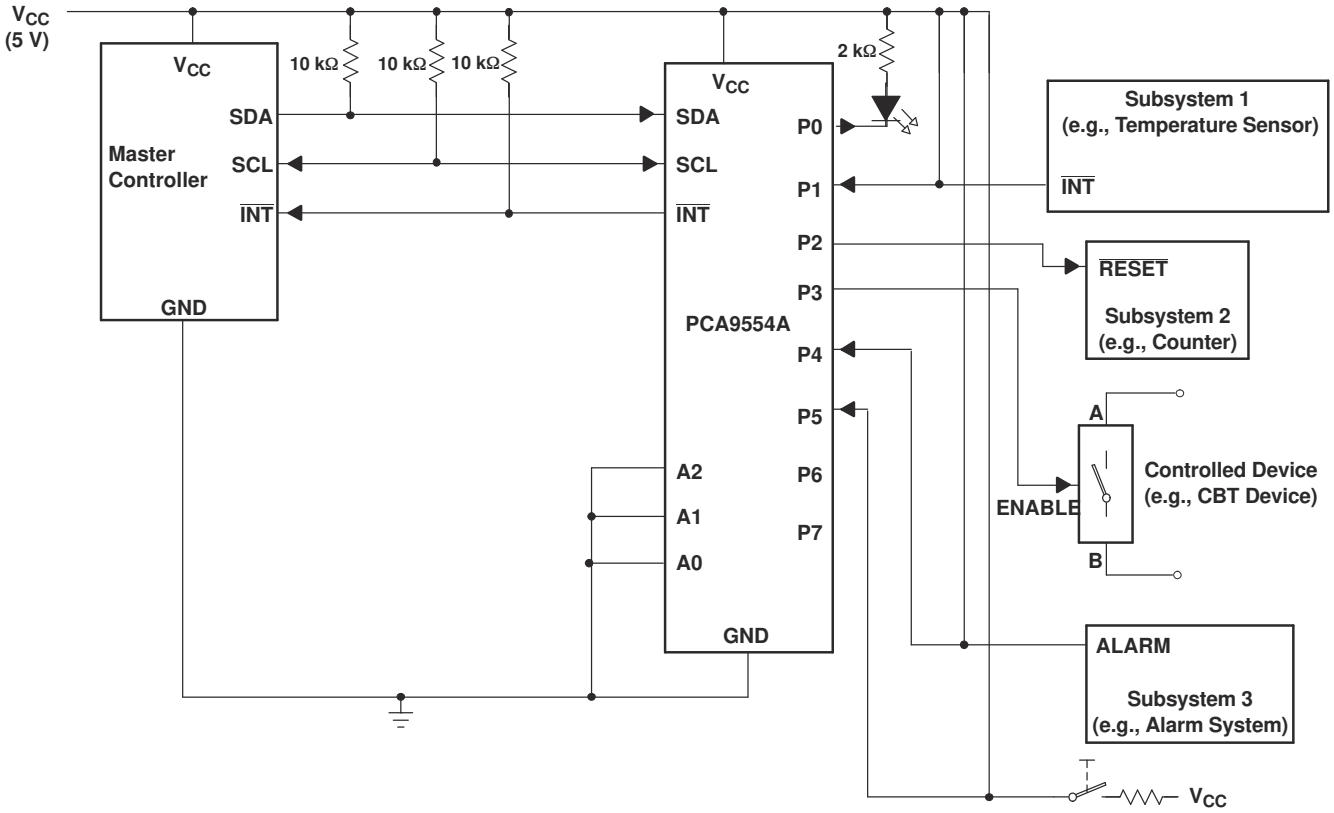
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Typical Application

図 9-1 shows an application in which the PCA9554A can be used.



A. Device address is configured as 0111000 for this example.
B. P0, P2, and P3 are configured as outputs.
C. P1, P4, and P5 are configured as inputs.
D. P6 and P7 are not used and have internal 100-kΩ pullup resistors to protect them from floating.

図 9-1. Typical Application

9.1.1.1 Detailed Design Procedure

9.1.1.1.1 Minimizing I_{CC} When I/Os Control Leds

When the I/Os are used to control LEDs, they are normally connected to V_{CC} through a resistor as shown in 図 9-1. Because the LED acts as a diode, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The supply current, I_{CC}, increases as V_{IN} becomes lower than V_{CC} and is specified as ΔI_{CC} in *Electrical Characteristics*.

For battery-powered applications, it is essential that the voltage of I/O pins is greater than or equal to V_{CC} when the LED is off to minimize current consumption. 図 9-2 shows a high-value resistor in parallel with the LED. 図 9-3 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevents additional supply-current consumption when the LED is off.

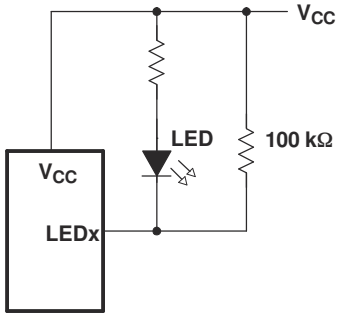


図 9-2. High-Value Resistor In Parallel With The Led

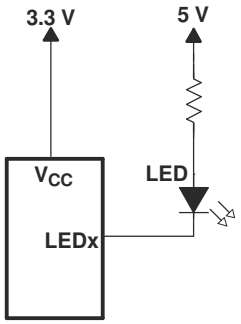


図 9-3. Device Supplied By A Lower Voltage

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10 Power Supply Recommendations

10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, PCA9554A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in 図 10-1 and 図 10-2.

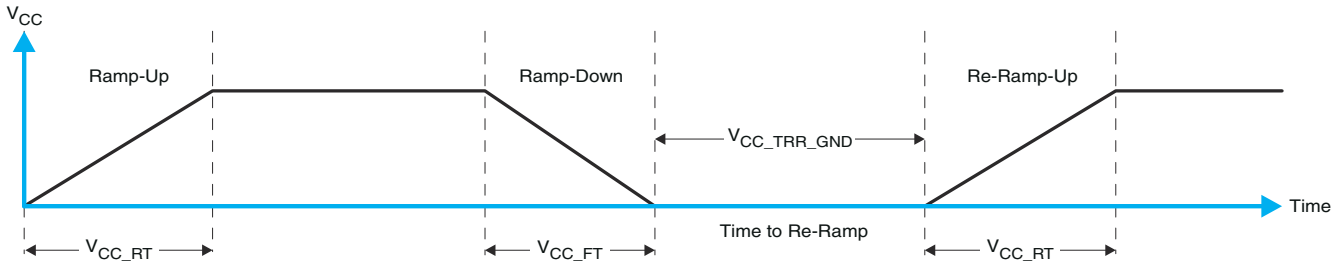


図 10-1. V_{CC} Is Lowered Below 0.2 V Or 0 V And Then Ramped Up To V_{CC}

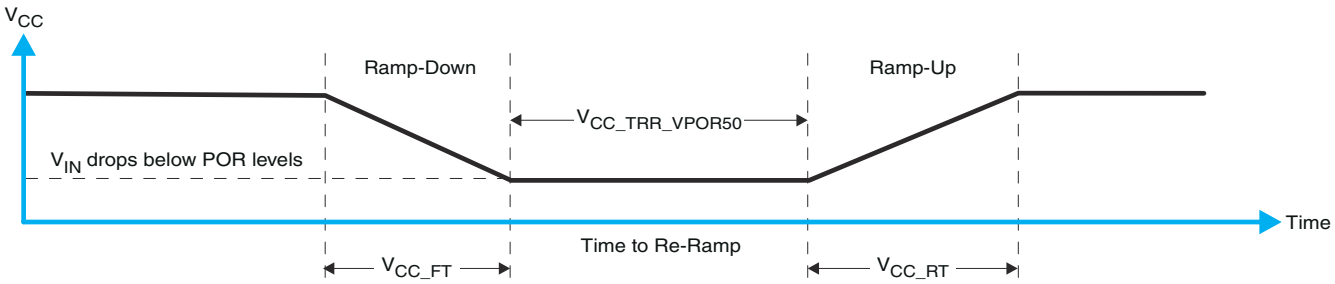


図 10-2. V_{CC} Is Lowered Below The Por Threshold, Then Ramped Back Up To V_{CC}

表 10-1 specifies the performance of the power-on reset feature for PCA9554A for both types of power-on reset.

表 10-1. Recommended Supply Sequencing And Ramp Rates(1)

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See 図 10-1	1		100	ms
V_{CC_RT}	Rise rate	See 図 10-1	0.01		100	ms
$V_{CC_TRR_GND}$	Time to re-ramp (when V_{CC} drops to GND)	See 図 10-1	0.001			ms
$V_{CC_TRR_POR50}$	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV)	See 図 10-2	0.001			ms
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCX_GW} = 1 µs	See 図 10-3			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when V_{CCX_GH} = 0.5 × V_{CCx}	See 図 10-3				µs
V_{PORF}	Voltage trip point of POR on falling V_{CC}		0.767		1.144	V
V_{PORR}	Voltage trip point of POR on rising V_{CC}		1.033		1.428	V

(1) T_A = –40°C to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and the device impedance are factors that affect power-on reset performance. 図 10-3 and 表 10-1 provide more information on how to measure these specifications.

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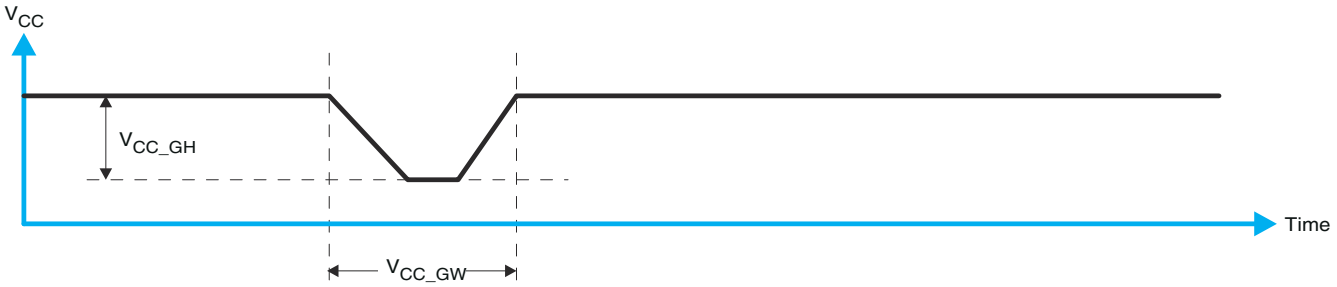


図 10-3. Glitch Width And Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. 図 10-4 and 表 10-1 provide more details on this specification.

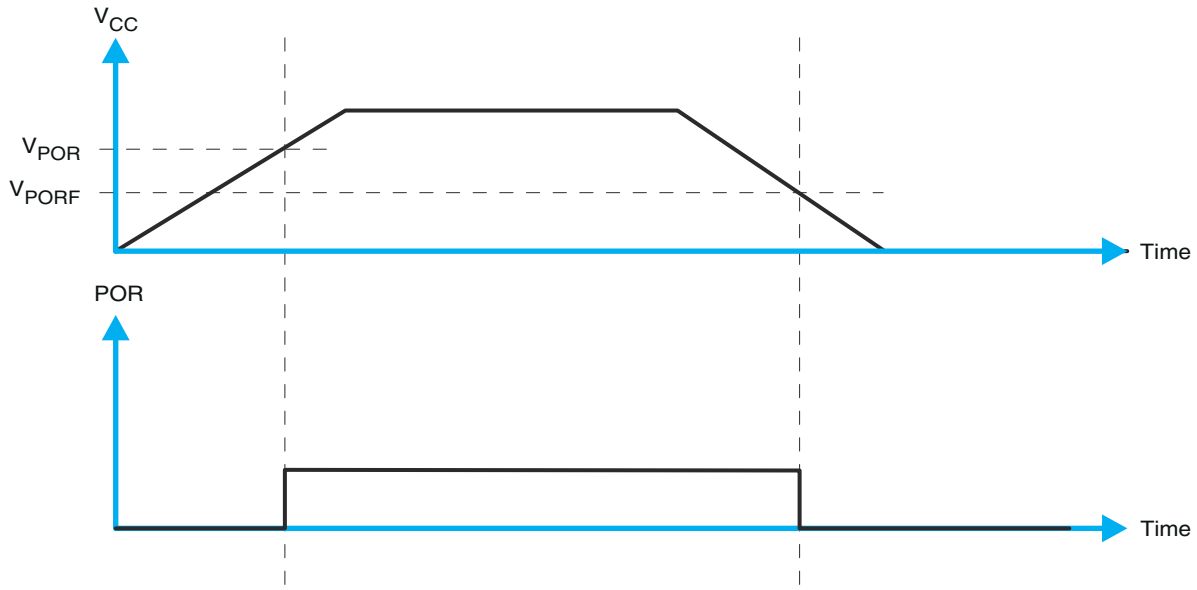


図 10-4. V_{POR}

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11 Device and Documentation Support

11.1 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

11.2 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.3 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.4 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCA9554ADB	Obsolete	Production	SSOP (DB) | 16	-	-	Call TI	Call TI	-40 to 85	PD554A
PCA9554ADBQR	NRND	Production	SSOP (DBQ) | 16	-	-	Call TI	Call TI	-40 to 85	
PCA9554ADGV	NRND	Production	TVSOP (DGV) | 16	-	-	Call TI	Call TI	-40 to 85	
PCA9554ADGVR	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD554A
PCA9554ADGVR.A	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD554A
PCA9554ADW	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	-40 to 85	PCA9554A
PCA9554ADWR	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	-40 to 85	PCA9554A
PCA9554ARGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	ZVH
PCA9554ARGTR.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	ZVH
PCA9554ARGTR.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	ZVH
PCA9554ARGTRG4	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVH
PCA9554ARGTRG4.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVH
PCA9554ARGTRG4.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVH
PCA9554ARGVR	Active	Production	VQFN (RGV) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD554A
PCA9554ARGVR.A	Active	Production	VQFN (RGV) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD554A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

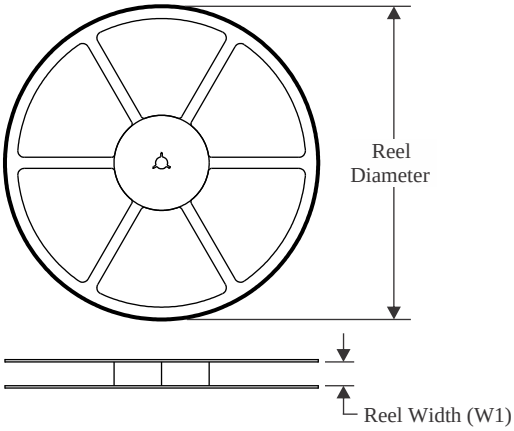
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

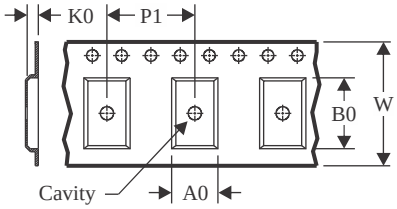
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

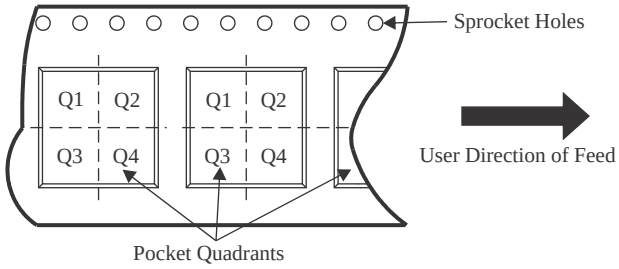


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

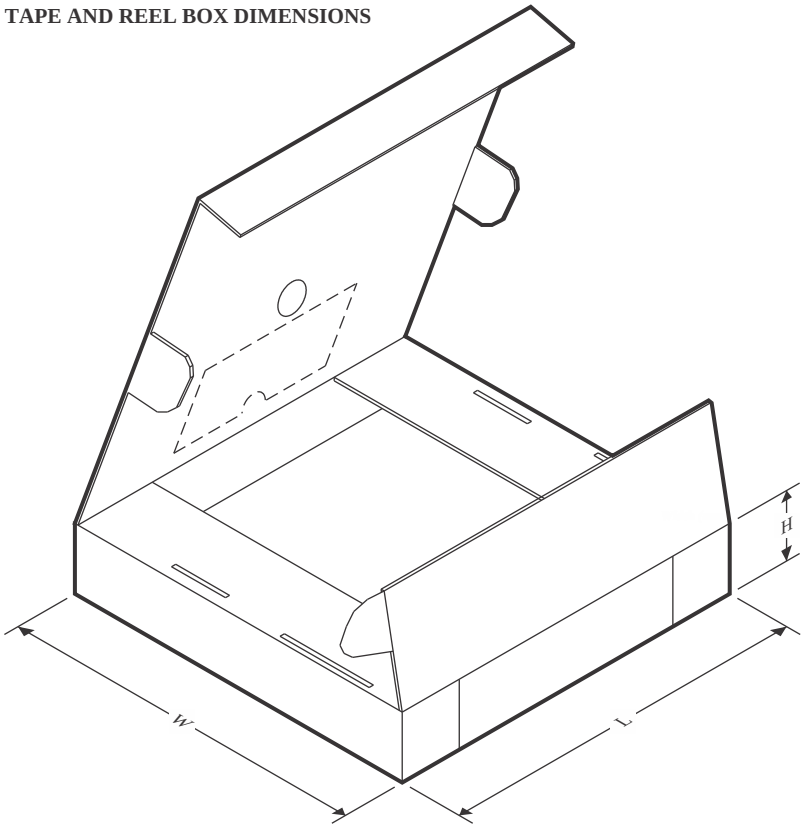
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9554ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
PCA9554ARGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
PCA9554ARGTRG4	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
PCA9554ARGVR	VQFN	RGV	16	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9554ADGVR	TVSOP	DGV	16	2000	353.0	353.0	32.0
PCA9554ARGTR	VQFN	RGT	16	3000	360.0	360.0	36.0
PCA9554ARGTRG4	VQFN	RGT	16	3000	367.0	367.0	35.0
PCA9554ARGVR	VQFN	RGV	16	2500	353.0	353.0	32.0

GENERIC PACKAGE VIEW

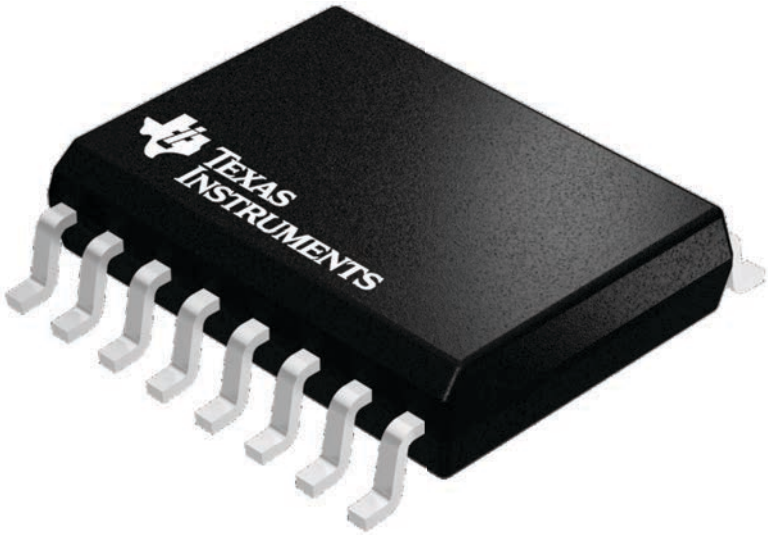
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

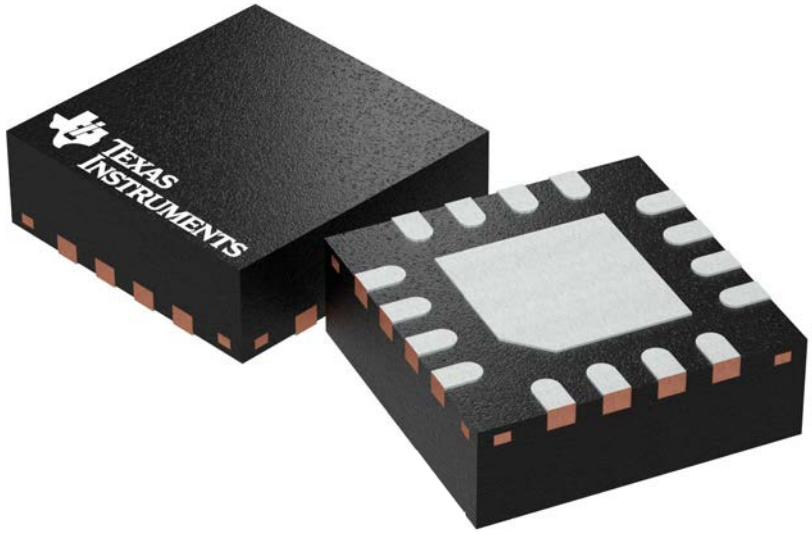
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



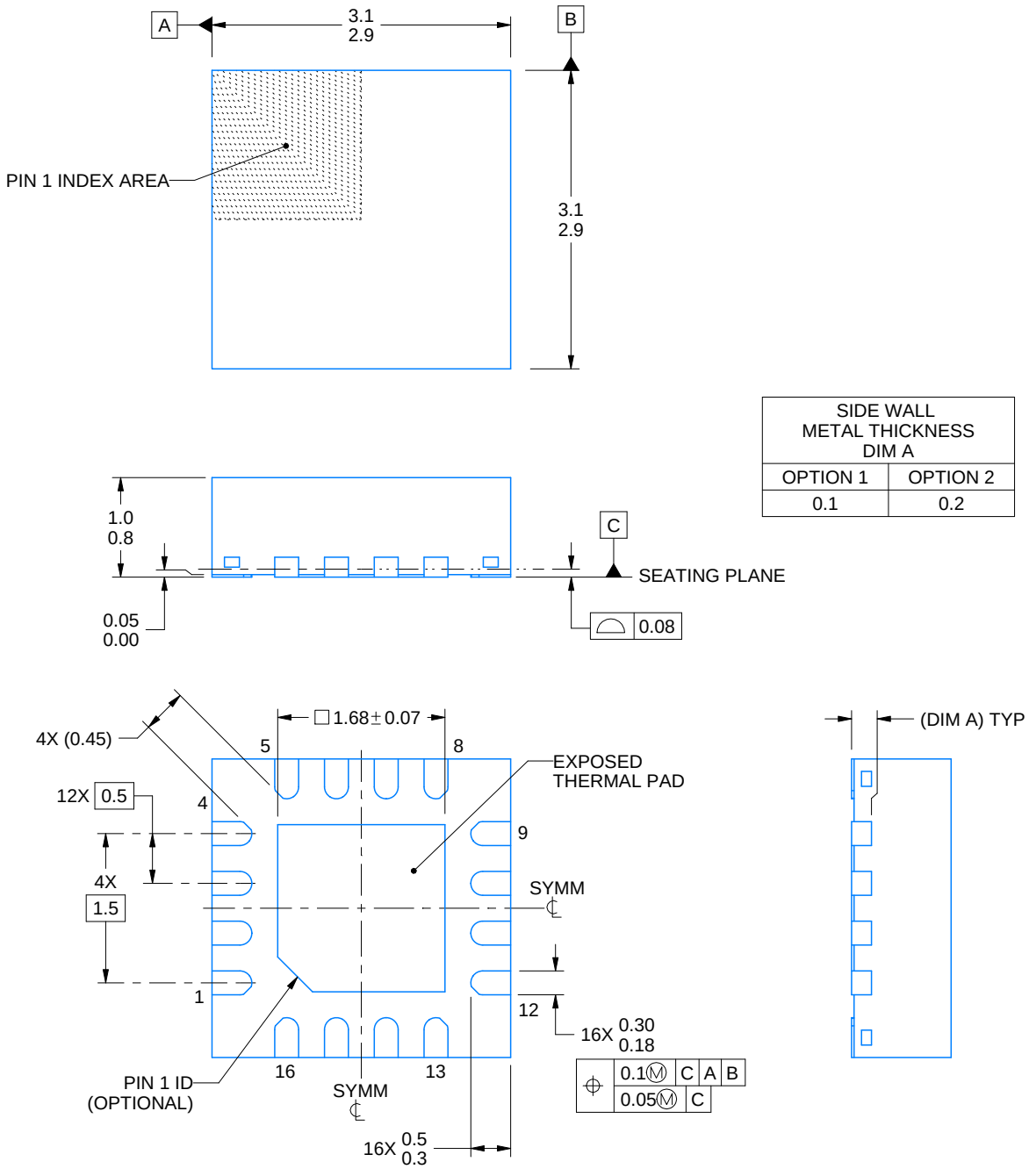
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

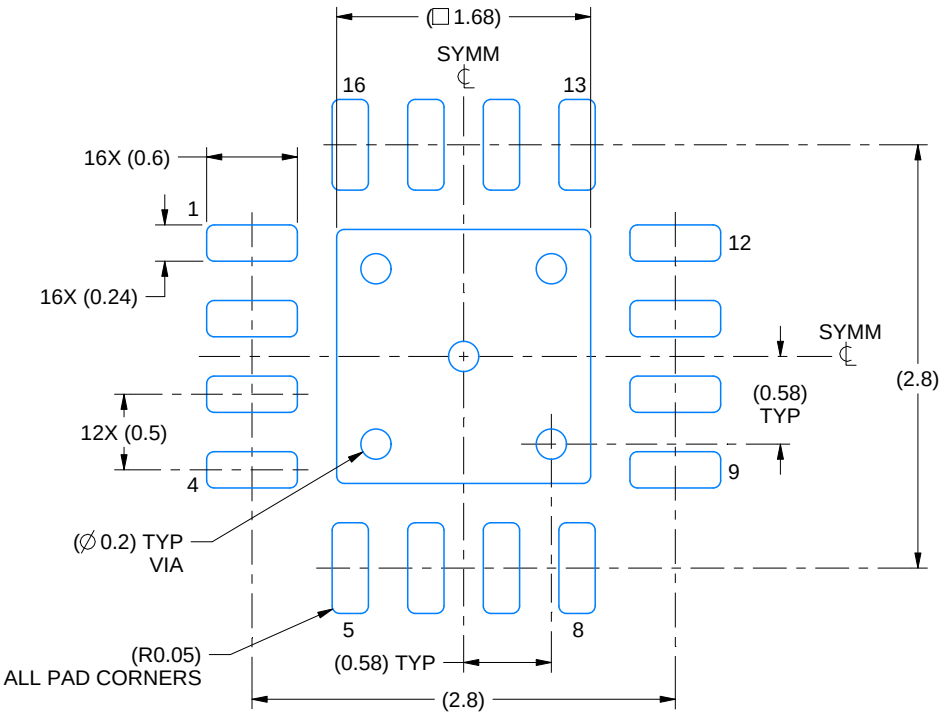
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

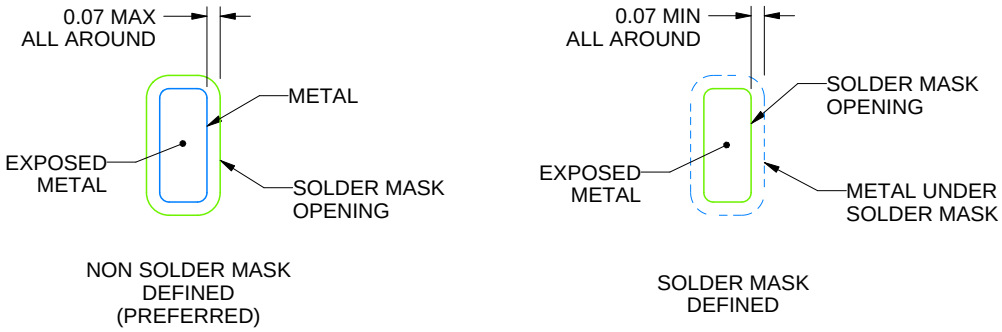


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

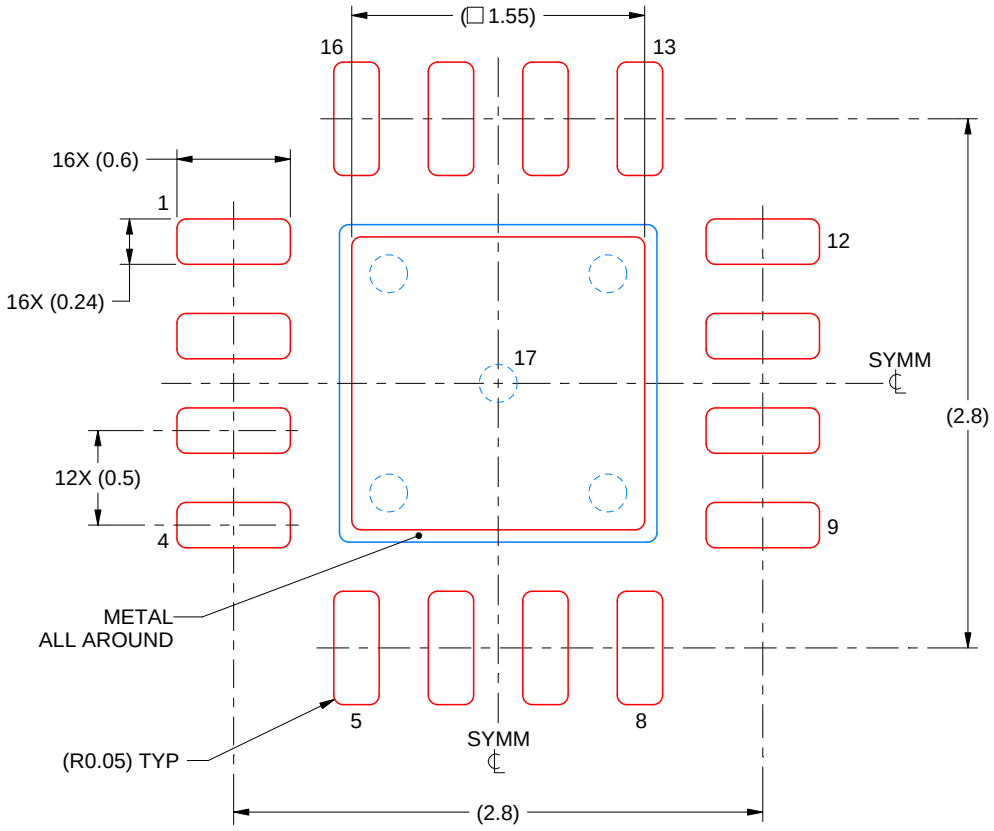


SOLDER MASK DETAILS

4222419/E 07/2025

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/E 07/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

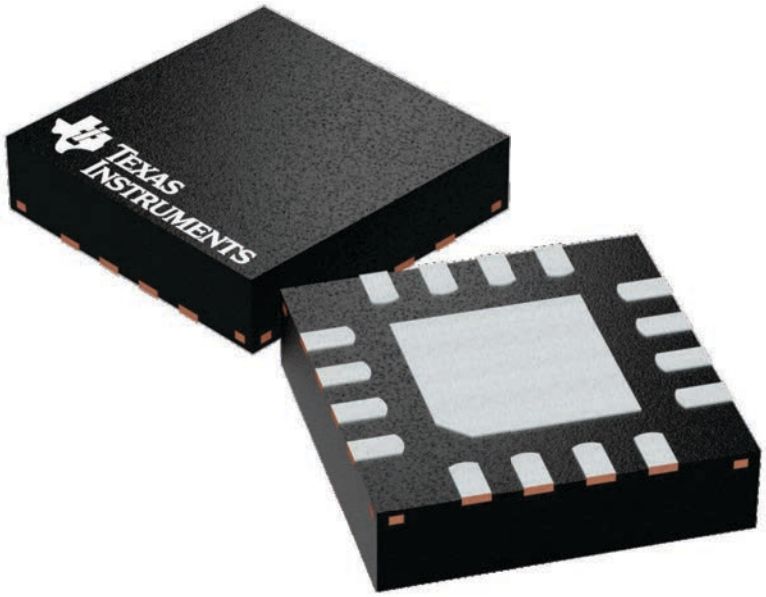
GENERIC PACKAGE VIEW

RGV 16

VQFN - 1 mm max height

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

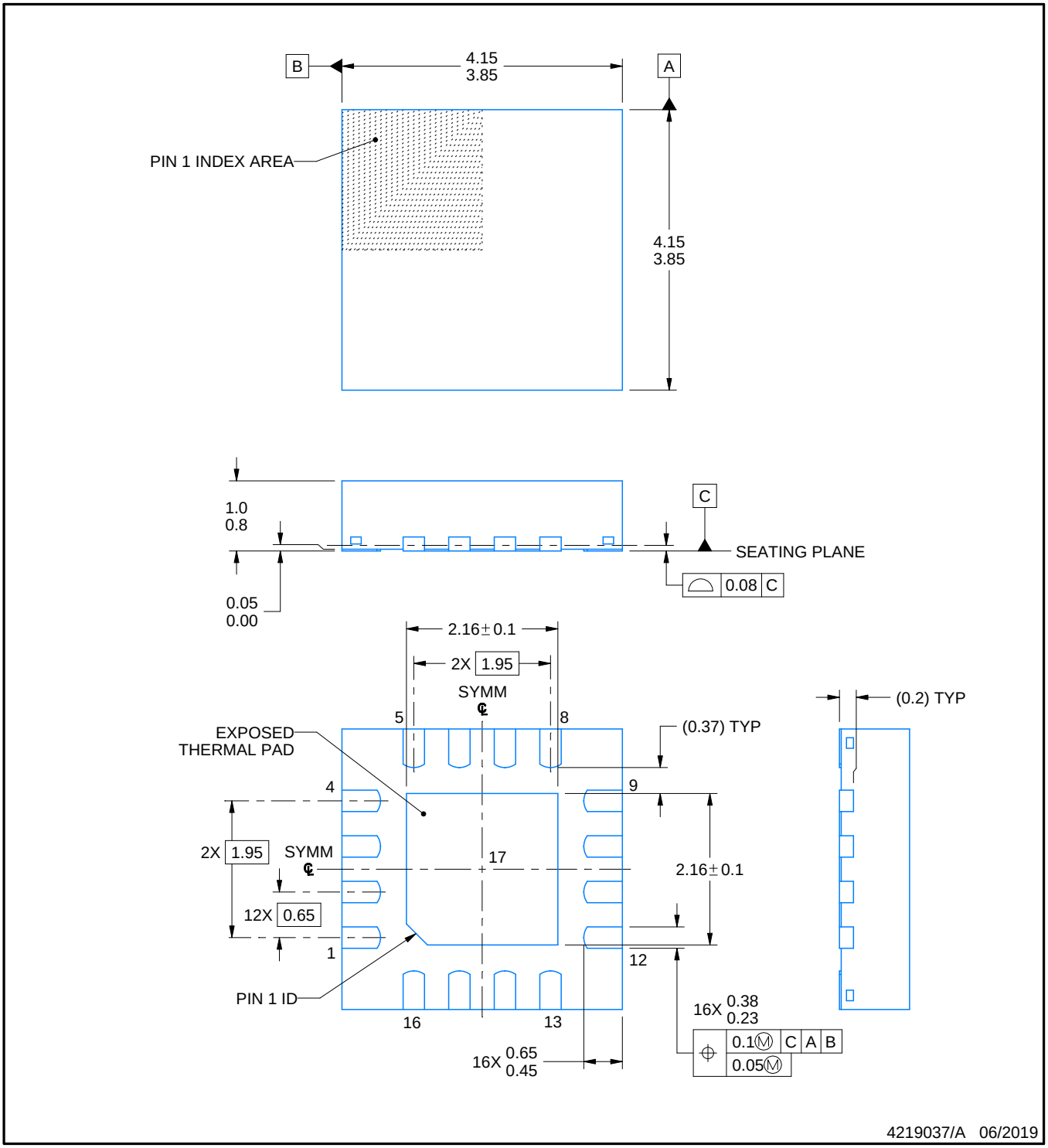
4224748/A

RGV0016A

PACKAGE OUTLINE

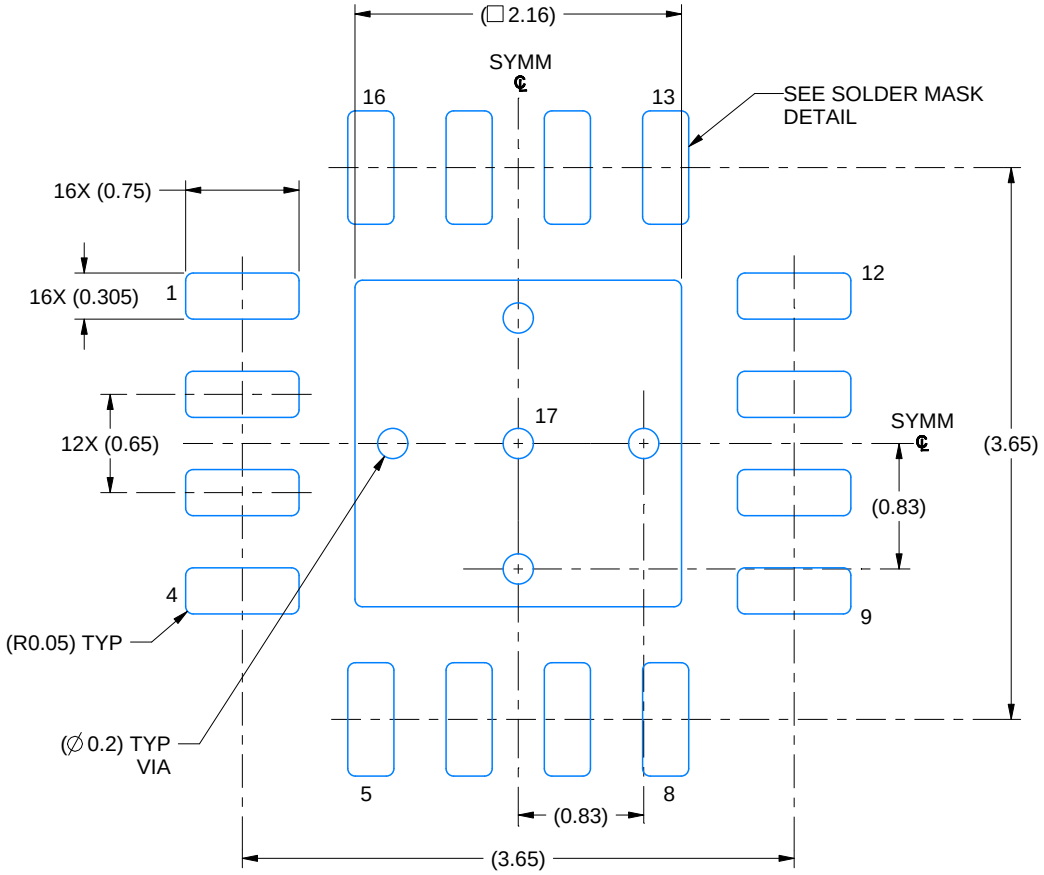
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

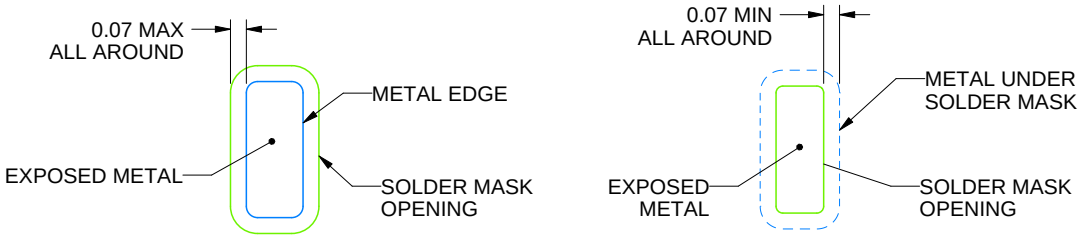


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

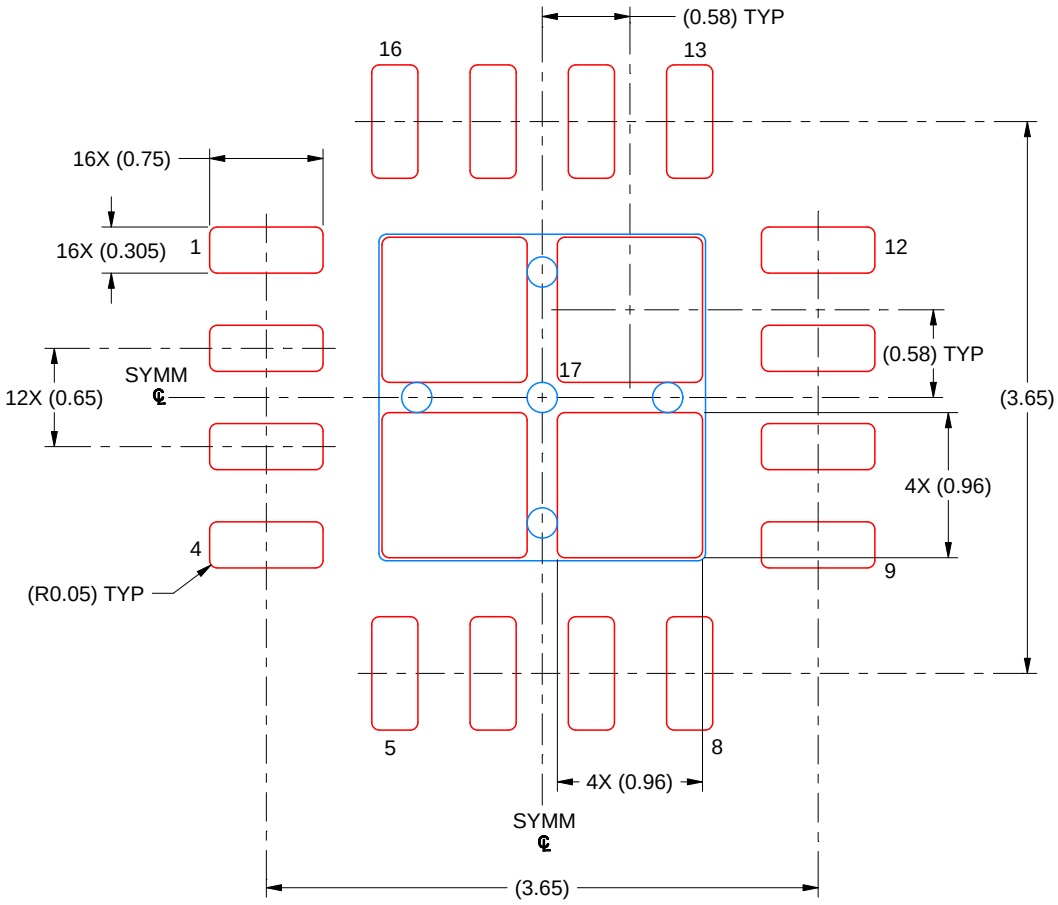
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219037/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219037/A 06/2019

NOTES: (continued)

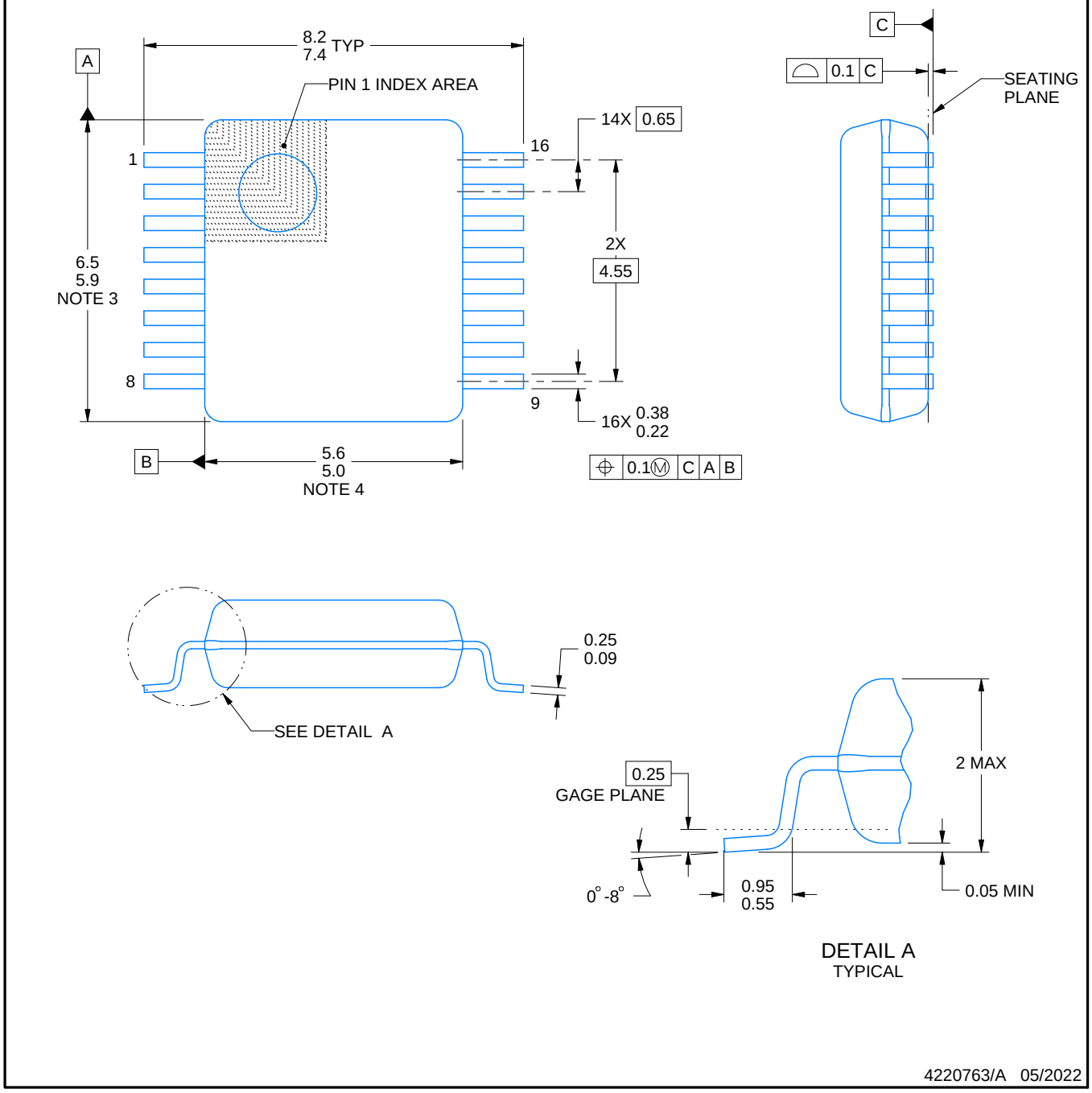
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DB0016A

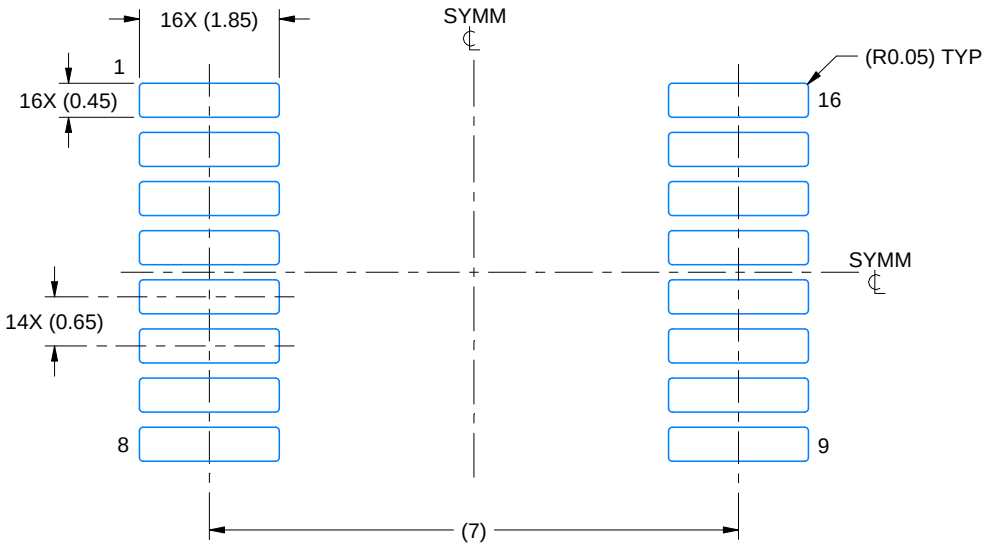
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

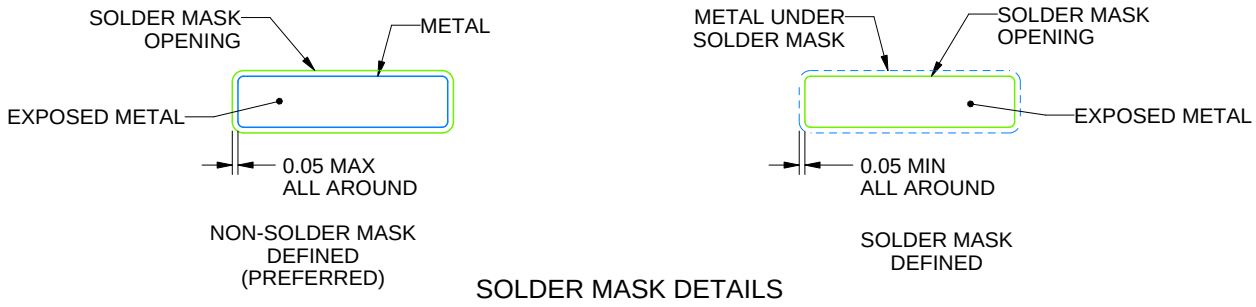


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

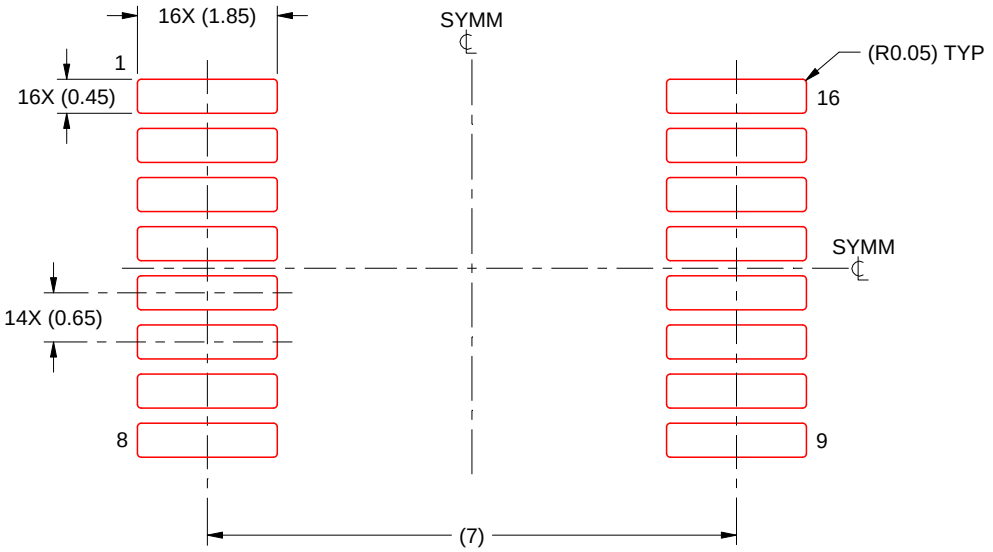


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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