PCM9211 ステレオ ADC およびルーティング機能搭載、216kHz デジタル・オーディオ・インターフェイス・トランシーバ (DIX)

1 特長

- DIX、ADC、信号ルーティングを統合:
  - 非同期動作 (DIR、DIT、ADC)
  - PCM データの多重化とルーティング:
    - I^2S、左揃え、右揃え
  - 汎用入出力ピン
- デジタル・オーディオ I/F レシーバ (DIR):
  - 24 ビット、216kHz に対応
  - 50ps の超低ジッタ
  - 非 PCM の検出 (IEC61937、DTS-CD/LD)
  - 12 個の S/PDIF 入力ポート:
    - 2 個の同軸 S/PDIF 入力
    - 10 個の光 S/PDIF 入力
- デジタル・オーディオ I/F トランスミッタ (DIT):
  - 24 ビット、216kHz に対応
  - 24 ビットのデータ長
  - 48 ビットのチャネル・ステータス・バッファ
  - 同期 / 非同期動作
- A/D コンバータ (ADC):
  - 24 ビット、96kHz に対応
  - ダイナミック・レンジ:101dB (f_S = 96kHz)
  - 同期 / 非同期動作
- ルーティング機能:
  - 入力:3x PCM、1x DIR、1x ADC
  - 出力:メイン OUT、補助 OUT、DIT
  - マルチチャネル (8 チャネル) PCM ルーティング
- その他の機能的な特長:
  - パワー・ダウン (ピンまたはレジスタ制御)
  - PCM ポートのサンプリング周波数カウンタ
  - GPIO と GPO
  - 外付け水晶振動子用の OSC (24.576MHz)
  - SPI、I^2C、またはハードウェア制御モード
- 電源:
  - 3.3V (2.9V～3.6V):DIX、全デジタル用
  - 5V (4.5V～5.5V):ADC アナログ用
- 動作温度:–40℃～+85℃
- パッケージ:48 ピン LQFP

2 アプリケーション

- ホームシアター、AVR 機器
- テレビ、スマート・サウンドバー
- 高性能サウンドカード

3 概要

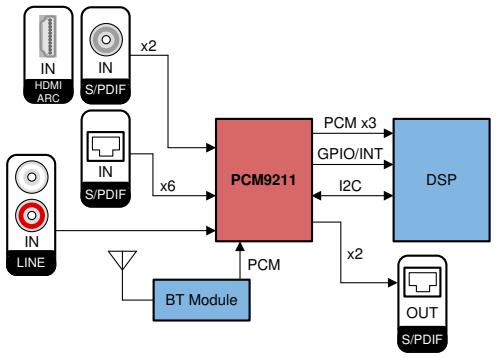
PCM9211 は、今日のマルチメディア・プレーヤー、サウンド・バー、レコーダー向けの完備したアナログおよびデジタル・フロントエンドです。

PCM9211 にはステレオ ADC、最大 12 の多重化された入力を持つ S/PDIF トランシーバ、3 つの PCM 入力が内蔵されており、デジタル信号プロセッサ (DSP) へのアナログおよび S/PDIF 信号とともに他のオーディオ・レシーバを多重化できます。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
PCM9211	LQFP (48)	7.00mm × 7.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。



アプリケーション概略図

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (February 2020) to Revision D (August 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• Changed *AUTO Source Selector Cause Setting Register* to match *Register Map* table	69

Changes from Revision B (August 2018) to Revision C (February 2020)	Page
• ドキュメントから HDMI 2.1 eARC 互換機能を削除	1
• *アプリケーション*のセクションにリンクを追加	1
• Changed bit 0 from RSV to MADLVL1 in bit register of *INT1 Output Cause Mask Setting Register* section	74
• Changed AUXIN2 bit setting from 100 to 101 in *DIT Function Control Register 1/3* section	95
• Changed title of bit register from *MPIO_C1, MPIO_C0 Output Flag Select Register* to *MPIO_C3, MPIO_C2 Output Flag Select Register* in *MPIO_C3, MPIO_C2 Output Flag Select Register* section	112
• Changed title of bit register from *MPIO_C1, MPIO_C0 Output Flag Select Register* to *MPO1, MPO0 Output Flag Select Register* in *MPO1, MPO0 Function Assign Setting Register* section	113

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5 Pin Configuration and Functions

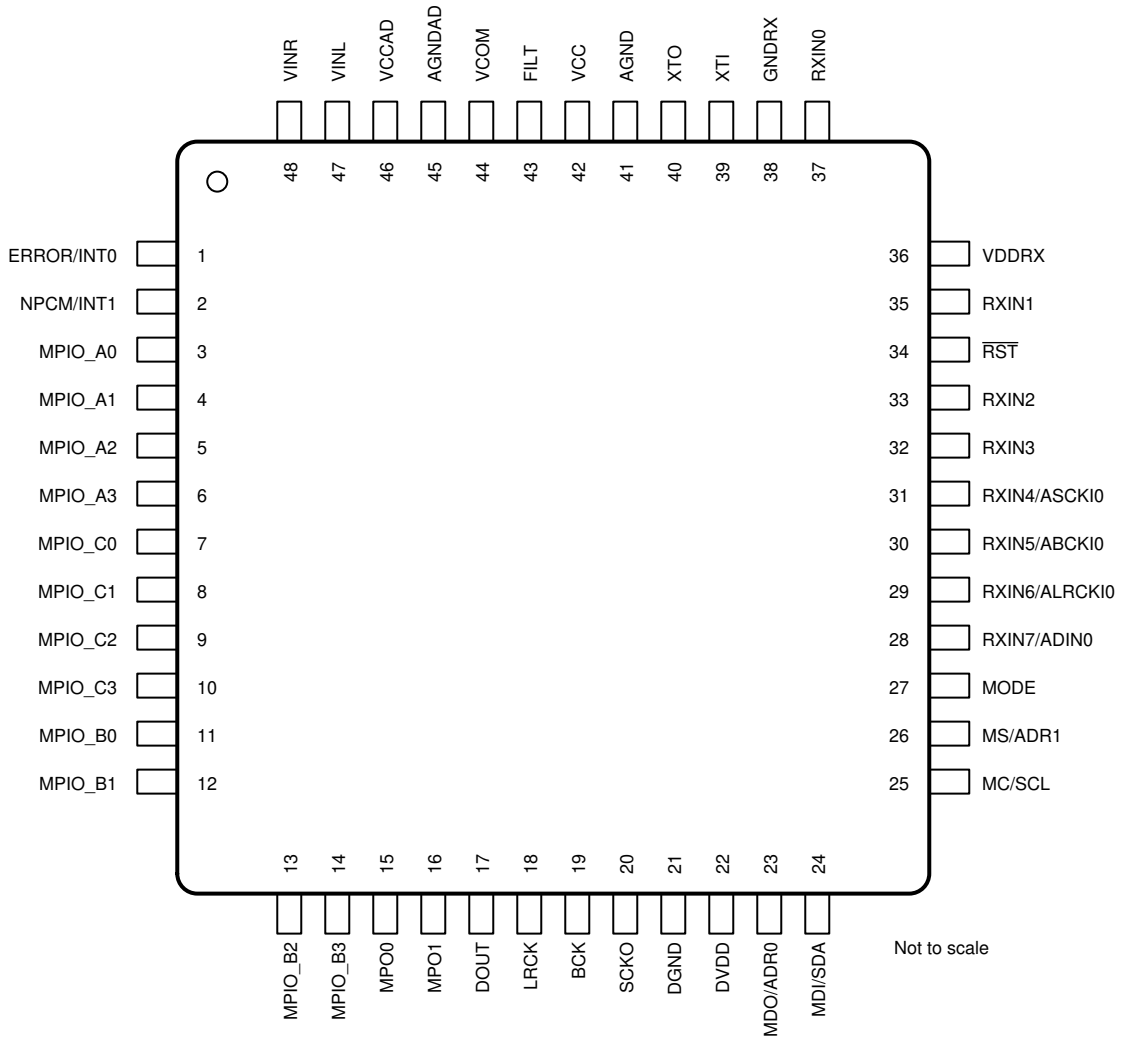

図 5-1. PT Package, 48-Pin LQFP (Top View)

表 5-1. Pin Functions

PIN		I/O	5-V TOLERANT	DESCRIPTION
NO.	NAME			
1	ERROR/INT0	O	No	DIR error detection output / interrupt 0 output
2	NPCM/INT1	O	No	DIR non-PCM detection output / interrupt 1 output
3	MPIO_A0	I/O	Yes	Multipurpose I/O, group A(1)
4	MPIO_A1	I/O	Yes	Multipurpose I/O, group A(1)
5	MPIO_A2	I/O	Yes	Multipurpose I/O, group A(1)
6	MPIO_A3	I/O	Yes	Multipurpose I/O, group A(1)
7	MPIO_C0	I/O	Yes	Multipurpose I/O, group C(1)
8	MPIO_C1	I/O	Yes	Multipurpose I/O, group C(1)
9	MPIO_C2	I/O	Yes	Multipurpose I/O, group C(1)
10	MPIO_C3	I/O	Yes	Multipurpose I/O, group C(1)
11	MPIO_B0	I/O	Yes	Multipurpose I/O, group B(1)
12	MPIO_B1	I/O	Yes	Multipurpose I/O, group B(1)
13	MPIO_B2	I/O	Yes	Multipurpose I/O, group B(1)

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表 5-1. Pin Functions (continued)

PIN		I/O	5-V TOLERANT	DESCRIPTION
NO.	NAME			
14	MPIO_B3	I/O	Yes	Multipurpose I/O, group B(1)
15	MPO0	O	No	Multipurpose output 0
16	MPO1	O	No	Multipurpose output 1
17	DOUT	O	No	Main output port, serial digital audio data output
18	LRCK	O	No	Main output port, LR clock output
19	BCK	O	No	Main output port, bit clock output
20	SCKO	O	No	Main output port, system clock output
21	DGND	–	–	Ground, for digital
22	DVDD	–	–	Power supply, 3.3 V (typ), for digital
23	MDO/ADR0	I/O	Yes	Software control I/F, SPI data output / I^{2}C slave address setting 0(1)
24	MDI/SDA	I/O	Yes	Software control I/F, SPI data input / I^{2}C data input/output(1) (4)
25	MC/SCL	I	Yes	Software control I/F, SPI clock input / I^{2}C clock input(1)
26	MS/ADR1	I	Yes	Software control I/F, SPI chip select / I^{2}C slave address setting 1(1)
27	MODE	I	No	Control mode setting, (see the *Serial Control Mode* section, control mode pin setting)
28	RXIN7/ADIN0	I	Yes	Biphase signal, input 7 / AUXIN0, serial audio data input(1)
29	RXIN6/ALRCKI0	I	Yes	Biphase signal, input 6 / AUXIN0, LR clock input(1)
30	RXIN5/ABCKI0	I	Yes	Biphase signal, input 5 / AUXIN0, bit clock input(1)
31	RXIN4/ASCKI0	I	Yes	Biphase signal, input 4 / AUXIN0, system clock input(1)
32	RXIN3	I	Yes	Biphase signal, input 3(1)
33	RXIN2	I	Yes	Biphase signal, input 2(1)
34	$\overline{\text{RST}}$	I	Yes	Reset input, active low(1) (2)
35	RXIN1	I	Yes	Biphase signal, input 1, built-in coaxial amplifier
36	VDDRX	–	–	Power supply, 3.3 V (typ.), for RXIN0 and RXIN1.
37	RXIN0	I	Yes	Biphase signal, input 0, built-in coaxial amplifier
38	GNDRX	-	-	Ground, for RXIN
39	XTI	I	No	Oscillation circuit input for crystal resonator or external XTI clock source input(3)
40	XTO	O	No	Oscillation circuit output for crystal resonator
41	AGND	–	–	Ground, for PLL analog
42	VCC	–	–	Power supply, 3.3 V (typ), for PLL analog
43	FILT	O	No	External PLL loop filter connection terminal; must connect recommended filter
44	VCOM	O	No	ADC common voltage output; must connect external decoupling capacitor
45	AGNDAD	–	–	Ground, for ADC analog
46	VCCAD	–	–	Power supply, 5.0 V (typ), for ADC analog
47	VINL	I	No	ADC analog voltage input, left channel
48	VINR	I	No	ADC analog voltage input, right channel

(1) Schmitt trigger input.
(2) Onboard pulldown resistor (50 kΩ, typical).
(3) CMOS Schmitt trigger input.
(4) Open-drain configuration in I^{2}C mode.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Supply voltage	VCC, VDD, VDDRX	–0.3	4.0	V
	VCCAD	–0.3	6.5	
Supply voltage differences: VCC, VDD			±0.1	V
Ground voltage differences: AGND, DGND, GNDRX			±0.1	V
Digital input voltage	RXIN2, RXIN3, RXIN4/ASCKI0, RXIN5/ABCKI0, RXIN6/ALRCKI0, RXIN7/ADIN0, MC/SCL, MDI/SDA, MDO/ADR, MS/ADR1, $\overline{RST}$	–0.3	6.5	V
	MPIO_A0-A3, MPIO_B0-B3, MPIO_C0-C3	–0.3	6.5	
	RXIN0, RXIN1 (For S/PDIF TTL / OPTICAL input)	–0.3	6.5	
	MODE	–0.3	4.0	
Analog input voltage	RXIN0, RXIN1 (For S/PDIF Coaxial Input Only)	–0.3	(VDDRX + 0.3) < 4.0	V
	XTI, XTO	–0.3	(VDD + 0.3) < 4.0	
	FILT	–0.3	(VCC + 0.3) < 4.0	
	VINL, VINR, VCOM	–0.3	(VCCAD + 0.3) < 6.5	
Input current (any pins except supplies)			±10	mA
Ambient temperature under bias		–40	125	°C
Package temperature (reflow, peak)			260	°C
Operating Junction temperature, T_J			150	°C
Storage temperature range, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DIR analog supply voltage, V_{CC}		2.9	3.3	3.6	V
ALL digital supply voltage, V_{DD}		2.9	3.3	3.6	V
ADC analog supply voltage, V_{CCAD}		4.5	5.0	5.5	V
Coaxial amplifier supply voltage, V_{DDRX}		2.9	3.3	3.6	V
Digital input interface level			TTL-compatible		
Digital input/output clock frequency	DIR, DIT, and Routing sampling frequency	7		216	kHz
	DIR, DIT, and Routing system clock frequency	0.896		55.296	MHz
	ADC sampling frequency	16		96	kHz
	ADC system clock frequency	2.048		24.576	MHz
	XTI input clock frequency		24.576		MHz
Analog input level	VINL, VINR		3		V_{PP}
Digital output load capacitance	Except SCKO			20	pF
Digital output load capacitance	SCKO			10	pF
MODE pin capacitance				10	pF
Operating free-air temperature		–40	25	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		PCM9211 PT (LQFP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics: General

All specifications at T_A = 25°C, V_{CC} = V_{DD} = V_{DDRX} = 3.3 V, and V_{CCAD} = 5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
DIGITAL I/O—DATA FORMAT						
	Audio data interface format			I^2S, left-justified, right-justified		
	Audio data word length			16, 24		Bits
	Audio data format			MSB first, twos complement		
f_S	Sampling frequency	DIR	7		216	kHz
		DIT	7		216	
		Routing	7		216	
		ADC	16		96	
DIGITAL I/O—INPUT LOGIC						
V_{IH}	Input logic level, high(2) (3)		2.0		5.5	VDC
V_{IL}	Input logic level, low(2) (3)				0.8	VDC
V_{IH}	Input logic level, high (XTI pin)(4)		0.7 V_{CC}		V_{CC}	VDC
V_{IL}	Input logic level, low (XTI pin)(4)				0.3 V_{CC}	VDC
V_{IH}	Input logic level, high (RXIN0/1 pins) (5)		0.7 V_{DDRX}		V_{DDRX}	VDC

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6.5 Electrical Characteristics: General (continued)

All specifications at T_A = 25°C, V_{CC} = V_{DD} = V_{DDRX} = 3.3 V, and V_{CCAD} = 5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
V_{IL}	Input logic level, low (RXIN0/1 pins) (5)				0.3 V_{DDRX}	VDC
I_{IH}	Input logic current, high(2) (4)	V_{IN} = V_{DD} or V_{CC}			±10	µA
I_{IL}	Input logic current, low(2) (4)	V_{IN} = 0 V			±10	µA
I_{IH}	Input logic current, high ($\overline{RST}$ pin)(3)	V_{IN} = V_{DD}		65	100	µA
I_{IL}	Input logic current, low ($\overline{RST}$ pin)(3)	V_{IN} = 0 V			±10	µA
I_{IH}	Input logic current, high (RXIN0/1 pins)(5)	V_{IN} = V_{DDRX}		165	300	µA
I_{IL}	Input logic current, low (RXIN0/1 pins)(5)	V_{IN} = 0 V		–165	–300	µA
DIGITAL I/O—OUTPUT LOGIC						
V_{OH}	Output logic level, high(6)	I_{OUT} = –4 mA	2.8			VDC
V_{OL}	Output logic level, low(6)	I_{OUT} = 4 mA			0.5	VDC
V_{OH}	Output logic level, high(7)	I_{OUT} = –4 mA	0.85 V_{CC}			VDC
V_{OL}	Output logic level, low(7)	I_{OUT} = 4 mA			0.15 V_{CC}	VDC
POWER-SUPPLY REQUIREMENTS						
V_{CC}	Voltage range		2.9	3.3	3.6	VDC
V_{DD}	Voltage range		2.9	3.3	3.6	VDC
V_{CCAD}	Voltage range		4.5	5.0	5.5	VDC
V_{DDRX}	Voltage range		2.9	3.3	3.6	VDC
I_{CC}	Supply current	f_S = 48 kHz / DIR, f_S = 48 kHz / ADC, f_S = 48 kHz / DIT		4.5		mA
		f_S = 192 kHz / DIR, f_S = 96 kHz / ADC, f_S = 192 kHz / DIT		7	13	
		Full power down, $\overline{RST}$ = low		150	350	µA
I_{DD}	Supply current	f_S = 48 kHz / DIR, f_S = 48 kHz / ADC, f_S = 48 kHz / DIT		12		mA
		f_S = 192 kHz / DIR, f_S = 96 kHz / ADC, f_S = 192 kHz / DIT		26	38	
		Full power down, $\overline{RST}$ = low		150	350	µA
I_{CCAD}	Supply current	f_S = 48 kHz / DIR, f_S = 48 kHz / ADC, f_S = 48 kHz / DIT		12		mA
		f_S = 192 kHz / DIR, f_S = 96 kHz / ADC, f_S = 192 kHz / DIT		12		
		Full power down, $\overline{RST}$ = low		110	250	µA
I_{DDRX} (8)	Supply current	f_S = 48 kHz / DIR, f_S = 48 kHz / ADC, f_S = 48 kHz / DIT		3.2		mA
		f_S = 192 kHz / DIR, f_S = 96 kHz / ADC, f_S = 192 kHz / DIT		3.2	4.8	
		Full power down, $\overline{RST}$ = low		0	30	µA
	Power dissipation	f_S = 48 kHz / DIR, f_S = 48 kHz / ADC, f_S = 48 kHz / DIT		135		mW
		f_S = 192 kHz / DIR, f_S = 96 kHz / ADC, f_S = 192 kHz / DIT		180		
		Full power down, $\overline{RST}$ = low		0.85		
TEMPERATURE						
	Operating temperature		–40		85	°C
$R_{\theta JA}$	Thermal resistance			100		°C/W

(1) PLL lock-up time varies with *ERROR release wait time* setting (Register 23h/ERRWT). Therefore, lock-up time in this table shows the value at ERRWT = 11 as the shortest time setting.
(2) Pins: MPIO_A0-A3, MPIO_B0-B3, MPIOC0-C3, RXIN2-RXIN7, MC/SCL, MDI/SDA, MDO/ADR0, MS/ADR1.
(3) Pin: $\overline{RST}$.
(4) Pin: XTI.
(5) Pins: RXIN0, RXIN1. Input impedance of RXIN0 and RXIN1 is 20 kΩ (typical). COAX amplifiers are powered on by Register 34h/RX0DIS and RX1DIS = 0. At power down by Register 34h/RX0DIS and RX1DIS= 1 (default), RXIN0 and RXIN1 are internally tied high.
(6) Pins: MPIO_A0-A3, MPIO_B0-B3, MPIO_C0-C3, SCKO, BCK, LRCK, DOUT, MPO0-1, ERROR/INT0, NPCM/INT1.
(7) Pin: XTO.
(8) Two coaxial amplifiers are powered on by Register 34h/RX1DIS and Register 34h, RX0DIS.

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6.6 Electrical Characteristics: Analog-to-Digital Converter (ADC)

All specifications at T_A = 25°C, V_{CC} = V_{DD} = V_{DDRX} = 3.3 V, and V_{CCAD} = 5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC, CHARACTERISTICS						
	Resolution		16	24		Bits
f_S	Sampling frequency		16		96	kHz
	Bit clock frequency	$64f_S$	1.024		6.144	MHz
	System clock frequency	$256f_S$	4.096		24.576	MHz
		$512f_S$	8.192		24.576	
ADC, ANALOG INPUT						
	Full-scale input voltage	$V_{IN}L$, $V_{IN}R$ = 0 dB		0.6 V_{CCAD}		V_{PP}
	Center voltage			0.5 V_{CCAD}		V
	Input Impedance			10		kΩ
	Antialiasing filter response	–3 dB		300		kHz
ADC, DC ACCURACY						
	Gain mismatch, channel to channel	Full-scale input, $V_{IN}L$, $V_{IN}R$		2.0	±8.0	% of FSR
	Gain error	Full-scale input, $V_{IN}L$, $V_{IN}R$		±2.0	±8.0	% of FSR
	Bipolar zero error	HPF bypass, $V_{IN}L$, $V_{IN}R$		±0.5	±2.0	% of FSR
ADC, DYNAMIC PERFORMANCE						
	THD+N V_{IN} = –1 dB	f_S = 48 kHz		–93	–85	dB
		f_S = 96 kHz		–93		
	Dynamic range	f_S = 48 kHz, A-weighted	95	99		dB
		f_S = 96 kHz, A-weighted		101		
	S/N ratio	f_S = 48 kHz, A-weighted	95	99		dB
		f_S = 96 kHz, A-weighted		101		
	Channel separation (between L-ch and R-ch)	f_S = 48 kHz	92	96		dB
		f_S = 96 kHz		98		
ADC, DIGITAL FILTER PERFORMANCE						
	Passband				0.454 f_S	Hz
	Stop band		0.583 f_S			Hz
	Passband ripple	< 0.454 f_S			±0.05	dB
	Stop band attenuation	> 0.583 f_S	–65			dB
	Group delay time			17.4 / f_S		sec
	HPF frequency response	–3 dB		0.019 f_S/1000		Hz
ADC, COMMON VOLTAGE OUTPUT						
	V_{COM} output voltage			0.5 V_{CCAD}		V
	V_{COM} output impedance		7	12.5	18	kΩ
	Allowable V_{COM} output source/sink current				±1	µA

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6.7 Electrical Characteristics: Digital Audio I/F Receiver (DIR)

All specifications at T_A = 25°C, V_{CC} = V_{DD} = V_{DDRX} = 3.3 V, and V_{CCAD} = 5 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIR, COAXIAL INPUT AMPLIFIER (RXIN0 and RXIN1)					
Input resistance			20		kΩ
Input voltage		0.15			V_{PP}
Input hysteresis			50		mV
Input sampling frequency		7		216	kHz
DIR, BIPHASE SIGNAL INPUT and PLL					
Input biphase sampling frequency range	Normal mode	28		108	kHz
	Wide mode	7		216	
Input sampling frequency accuracy	IEC60958-3 (2003-01)	Level III (±12.5%)			
Jitter tolerance	IEC60958-3 (2003-01)	IEC60958-3			
PLL lock up time(1)	From biphase signal detection to error out release (ERROR = L)			100	ms
DIR, RECOVERED CLOCK and DATA					
Serial audio data width		16		24	Bits
System clock frequency	128f_S	0.896		27.648	MHz
	256f_S	1.792		55.296	
	512f_S	3.584		55.296	
Bit clock frequency	64f_S	0.448		13.824	MHz
LR clock frequency	f_S	7		216	kHz
System clock jitter	f_S = 48 kHz, SCKO = 256f_S, measured period jitter		50	100	ps, rms
System clock duty cycle	50% reference	±5%		±5%	
DIT					
Output biphase sampling frequency		7		216	kHz
Input system clock frequency	128f_S	0.896		27.648	MHz
	256f_S	1.792		55.296	
	512f_S	3.584		55.296	
Input bit clock frequency	64f_S	0.448		13.824	MHz
Input LR clock frequency	f_S	7		216	kHz
OSCILLATOR CIRCUIT, XTI and XMCKO CLOCK					
XTI source clock frequency			24.576		MHz
Frequency accuracy		–100		100	ppm
XTI input clock duty cycle		45%		55%	
XMCKO frequency			24.576		MHz
XMCKO output duty cycle	50% reference	±5%		±5%	
PCM OUTPUT PORT (SCKO, BCK, LRCK, DOUT)					
System clock frequency	128f_S / 256f_S / 512f_S	0.896		55.296	MHz
Bit clock output frequency	64f_S	0.448		13.824	MHz
LR clock output frequency	f_S	7		216	kHz
ROUTING					
System clock frequency	128f_S / 256f_S / 512f_S	0.896		55.296	MHz
Bit clock output Frequency	64f_S	0.448		13.824	MHz
LR clock output frequency	f_S	7		216	kHz

(1) PLL lock-up time varies with *ERROR release wait time* setting (Register 23h/ERRWT). Therefore, lock-up time in this table shows the value at ERRWT = 11 as the shortest time setting.

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6.8 Timing Requirements

		MIN	NOM	MAX	UNIT
$\overline{RST}$ PIN DEVICE RESET REQUIREMENTS, 図 7-1					
t_{RSTL}	$\overline{RST}$ pulse width ($\overline{RST}$ pin = low)	1			µs
ADC SYSTEM CLOCK INPUT(1), 図 7-3					
t_{SCY}	System clock cycle time	30			ns
t_{SCH}	System clock high time	0.4 t_{SCY}			ns
t_{SCL}	System clock low time	0.4 t_{SCY}			ns
	System clock duty cycle	40%		60%	
AUDIO DATA INTERFACE, SLAVE MODE(2), 図 7-5					
t_{BCY}	BCK cycle time	75			ns
t_{BCH}	BCK high time	35			ns
t_{BCL}	BCK low time	35			ns
t_{LRS}	LRCK setup time to BCK rising edge	10			ns
t_{LRH}	LRCK hold time to BCK rising edge	10			ns
t_{DOD}	DOUT delay time from BCK falling edge	10		70	ns
AUDIO DATA INTERFACE, MASTER MODE(2), 図 7-6					
t_{BCY}	BCK cycle time		1/64f_S		
t_{BCH}	BCK high time	0.4 t_{BCY}	0.5 t_{BCY}	0.6 t_{BCY}	
t_{BCL}	BCK low time	0.4 t_{BCY}	0.5 t_{BCY}	0.6 t_{BCY}	
t_{LRD}	LRCK delay time to BCK falling edge	0		30	ns
t_{DOD}	DOUT delay time from BCK falling edge	0		30	ns
LATENCY BETWEEN INPUT BIPHASE AND LRCKO/DOUT, 図 7-12					
t_{LATE}	LRCKO/DOUT latency		4/f_S		s
DIR DECODED AUDIO DATA OUTPUT(3), 図 7-13					
t_{SCY}	System clock pulse cycle time	18			ns
t_{CKLR}	Delay time of BCKO falling edge to LRCKO valid	–10		10	ns
t_{BCY}	BCKO pulse cycle time		1/64f_S		s
t_{BCH}	BCKO pulse width high	60			ns
t_{BCL}	BCKO pulse width low	60			ns
t_{BCDO}	Delay time of BCKO falling edge to DOUT valid	–10		10	ns
t_R	Rising time of all signals		5		ns
t_F	Falling time of all signals		5		ns
CONTROL INTERFACE REQUIREMENTS, FOUR WIRE SCI, 図 7-29					
t_{MCY}	MC Pulse cycle time	100			ns
t_{MCL}	MC Low level time	40			ns
t_{MCH}	MC High level time	40			ns
t_{MHH}	MS High level time	t_{MCY}			ns
t_{MSS}	MS Falling edge to MC rising edge	30			ns
t_{MSH}	MS Rising edge from MC rising edge for LSB	15			ns
t_{MDH}	MDI Hold time	15			ns
t_{MDS}	MDI Set-up time	15			ns
t_{MDD}	MDO Enable or delay time from MC falling edge	0		30	ns
t_{MDR}	MDO Disable time from MS rising edge	0		30	ns

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6.8 Timing Requirements (continued)

		MIN	NOM	MAX	UNIT
CONTROL INTERFACE, SCL AND SDA, STANDARD MODE, 図 7-33					
f_{SCL}	SCL clock frequency			100	kHz
t_{BUF}	Bus free time between STOP and START condition	4.7			µs
t_{LOW}	Low period of the SCL clock	4.7			µs
t_{HI}	High period of the SCL clock	4			µs
t_{S-SU}	Setup time for START/Repeated START condition	4.7			µs
t_{S-HD}	Hold time for START/Repeated START condition	4			µs
t_{D-SU}	Data setup time	250			ns
t_{D-HD}	Data hold time	0		3450	ns
t_{SCL-R}	Rise time of SCL signal			1000	ns
t_{SCL-F}	Fall time of SCL signal			1000	ns
t_{SDA-R}	Rise time of SDA signal			1000	ns
t_{SDA-F}	Fall time of SDA signal			1000	ns
t_{P-SU}	Setup time for STOP condition	4			µs
t_{GW}	Allowable glitch width			NA	ns
C_B	Capacitive load for SDA and SCL line			400	pF
V_{NH}	Noise margin at High level for each connected device (including hysteresis)	0.2 × V_{DD}			V
V_{NL}	Noise margin at Low level for each connected device (including hysteresis)	0.1 × V_{DD}			V
V_{HYS}	Hysteresis of Schmitt-trigger input	NA			V
CONTROL INTERFACE, SCL AND SDA, FAST MODE, 図 7-33					
f_{SCL}	SCL clock frequency			400	
t_{BUF}	Bus free time between STOP and START condition	1.3			
t_{LOW}	Low period of the SCL clock	1.3			
t_{HI}	High period of the SCL clock	0.6			
t_{S-SU}	Setup time for START/Repeated START condition	0.6			
t_{S-HD}	Hold time for START/Repeated START condition	0.6			
t_{D-SU}	Data setup time	100			
t_{D-HD}	Data hold time	0		900	
t_{SCL-R}	Rise time of SCL signal	20 + 0.1 C_B		300	
t_{SCL-F}	Fall time of SCL signal	20 + 0.1 C_B		300	
t_{SDA-R}	Rise time of SDA signal	20 + 0.1 C_B		300	
t_{SDA-F}	Fall time of SDA signal	20 + 0.1 C_B		300	
t_{P-SU}	Setup time for STOP condition	0.6			
t_{GW}	Allowable glitch width			50	
C_B	Capacitive load for SDA and SCL line			100	
V_{NH}	Noise margin at High level for each connected device (including hysteresis)	0.2 × V_{DD}			
V_{NL}	Noise margin at Low level for each connected device (including hysteresis)	0.1 × V_{DD}			
V_{HYS}	Hysteresis of Schmitt-trigger input	0.05 × V_{DD}			

(1) This timing requirement is applied when ADC clock source (register 42h, ADCLK) is AUXIN0, AUXIN1 or AUXIN2.
(2) Load capacitance of output is 20 pF. This timing requirement is applied when ADC clock source (register 42h, ADCLK) is AUXIN0, AUXIN1 or AUXIN2. This specification is applied for SCK with a frequency less than 25 MHz.
(3) Load capacitance of LRCKO, BCKO, and DOUT pin is 20 pF. DOUT, LRCKO, and BCKO are synchronized with SCKO.

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6.9 Typical Characteristics: ADC

All specifications at T_A = 25°C, VCCAD = 5 V, VDD = 3.3 V, f_S = 48 kHz, SCK = 512f_S, and 24-bit data, unless otherwise noted.

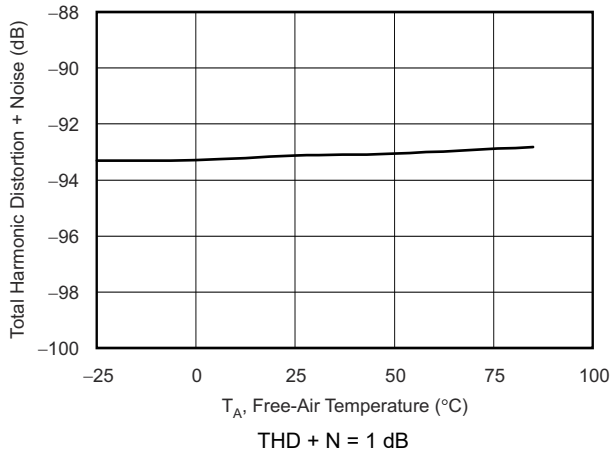

図 6-1. Total Harmonic Distortion + Noise vs Temperature

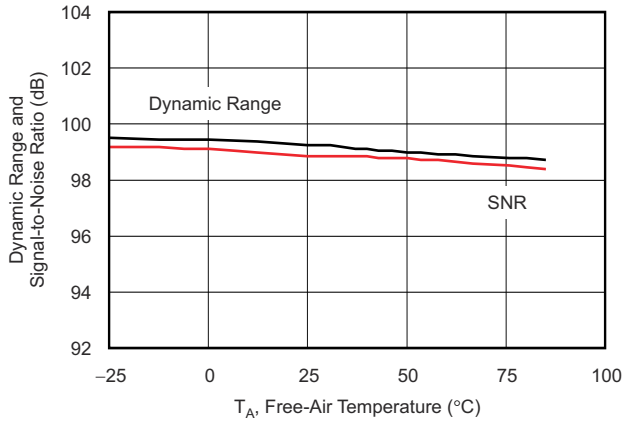

図 6-2. Dynamic Range and SNR vs Temperature

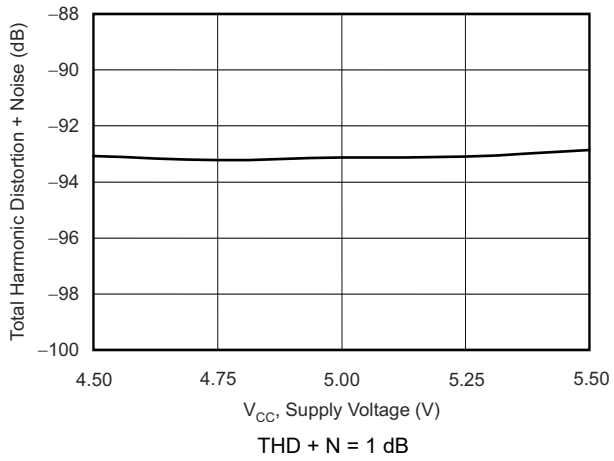

図 6-3. Total Harmonic Distortion + Noise vs Supply Voltage

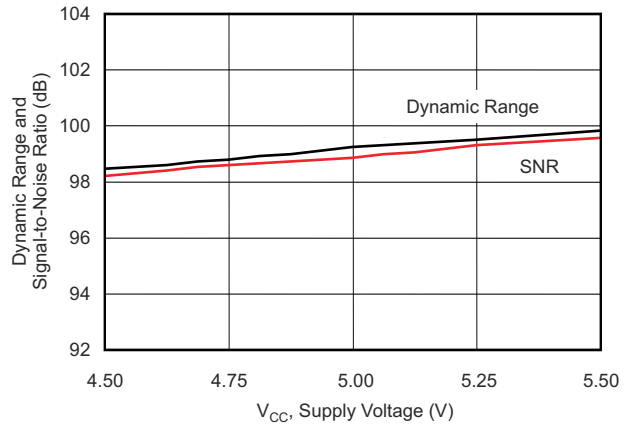

図 6-4. Dynamic Range and SNR vs Supply Voltage

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6.10 Typical Characteristics: ADC Internal Filter

All specifications at T_A = 25°C, VCCAD = 5 V, VDD = 3.3 V, f_S = 48 kHz, SCK = 512f_S, and 24-bit data, unless otherwise noted.

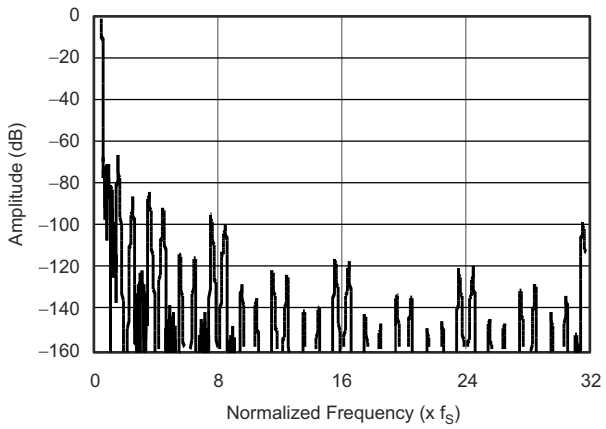

図 6-5. Decimation Filter Stop Band Characteristic

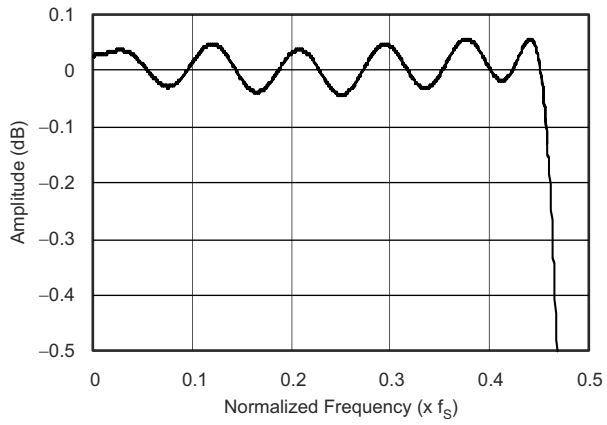

図 6-6. Decimation Filter Passband Characteristic

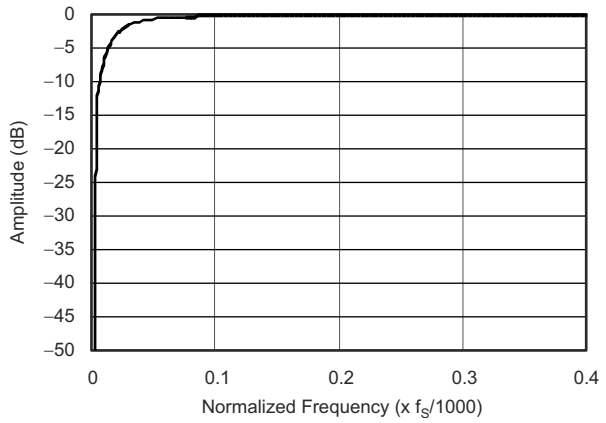

図 6-7. High-Pass Filter Characteristic

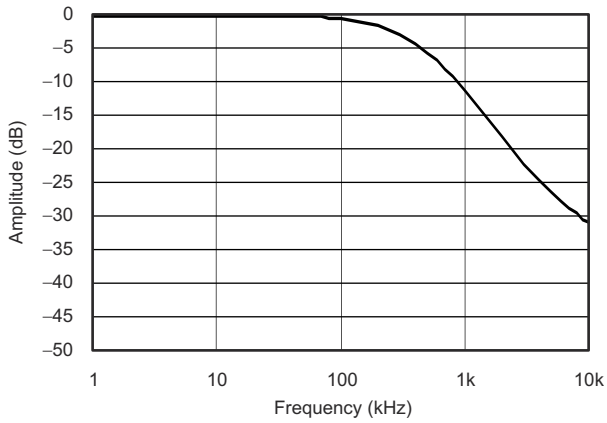

図 6-8. Antialiasing Filter Characteristic

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6.11 Typical Characteristics: ADC Output Spectrum

All specifications at T_A = 25°C, VCCAD = 5 V, VDD = 3.3 V, f_S = 48 kHz, SCK = 512f_S, and 24-bit data, unless otherwise noted.

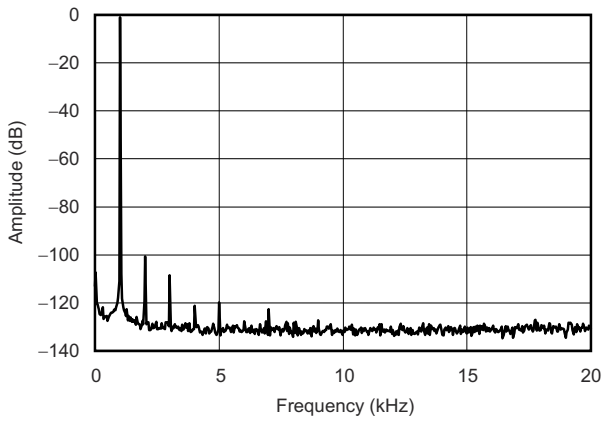
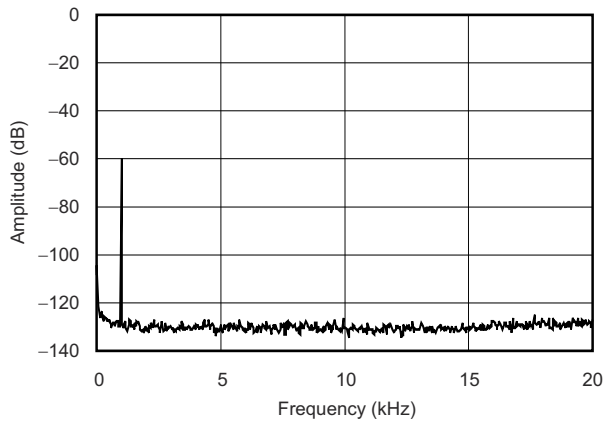


図 6-9. Output Spectrum



–60 dB, N = 32,768

図 6-10. Output Spectrum

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Parameter Measurement Information

All *Typical Characteristics* for the devices are measured using the EVM and an Audio Precision SYS-2722 Audio Analyzer. 図 7-1 shows the PCM9211 parameter measurement circuit.

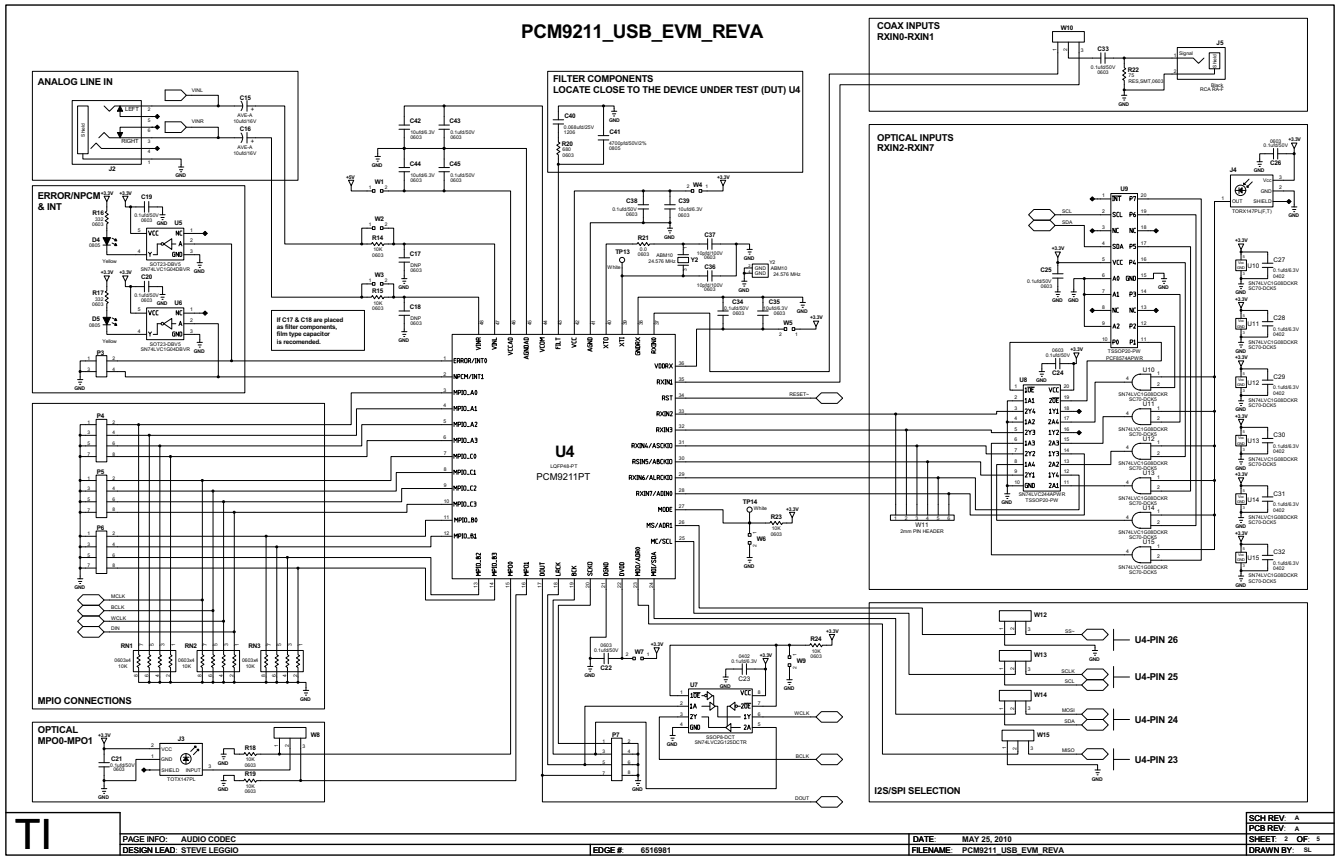

図 7-1. PCM9211 Parameter Measurement Circuit

7 Detailed Description

7.1 Overview

The PCM9211 is an analog and digital front-end device for any media player and recorder. It integrates a 216-kHz digital audio transceiver (DIX), a 96-kHz stereo ADC, and multiple PCM (I^2S, left-justified, right-justified) interfaces. Additionally, the device integrates a router that allows any source (ADC, DIR, or PCM) to be routed to one of three outputs (2x PCM and DIT), thus significantly reducing the number of external components required to route sources to the core DSP.

Each audio interface of the PCM9211 (that is, the ADC, DIT, and DIR) can operate asynchronously at different sampling rates, allowing an analog source to be sampled at 96 kHz and to be switched over to an S/PDIF source driving encoded data at 48 kHz.

The PCM9211 also features a power down function that can be set using hardware pins and registers, ensuring that the system minimizes power consumption during standby.

7.1.1 Device Comparison

表 7-1. Device Comparison

PART NUMBER	ADC	PCM PORTS	S/PDIF PORTS
PCM9211	Yes	Up to 3 IN and Up to 3 OUT	Up to 12 IN and Up to 2 OUT
DIX9211	No	Up to 3 IN and Up to 3 OUT	Up to 12 IN and Up to 2 OUT

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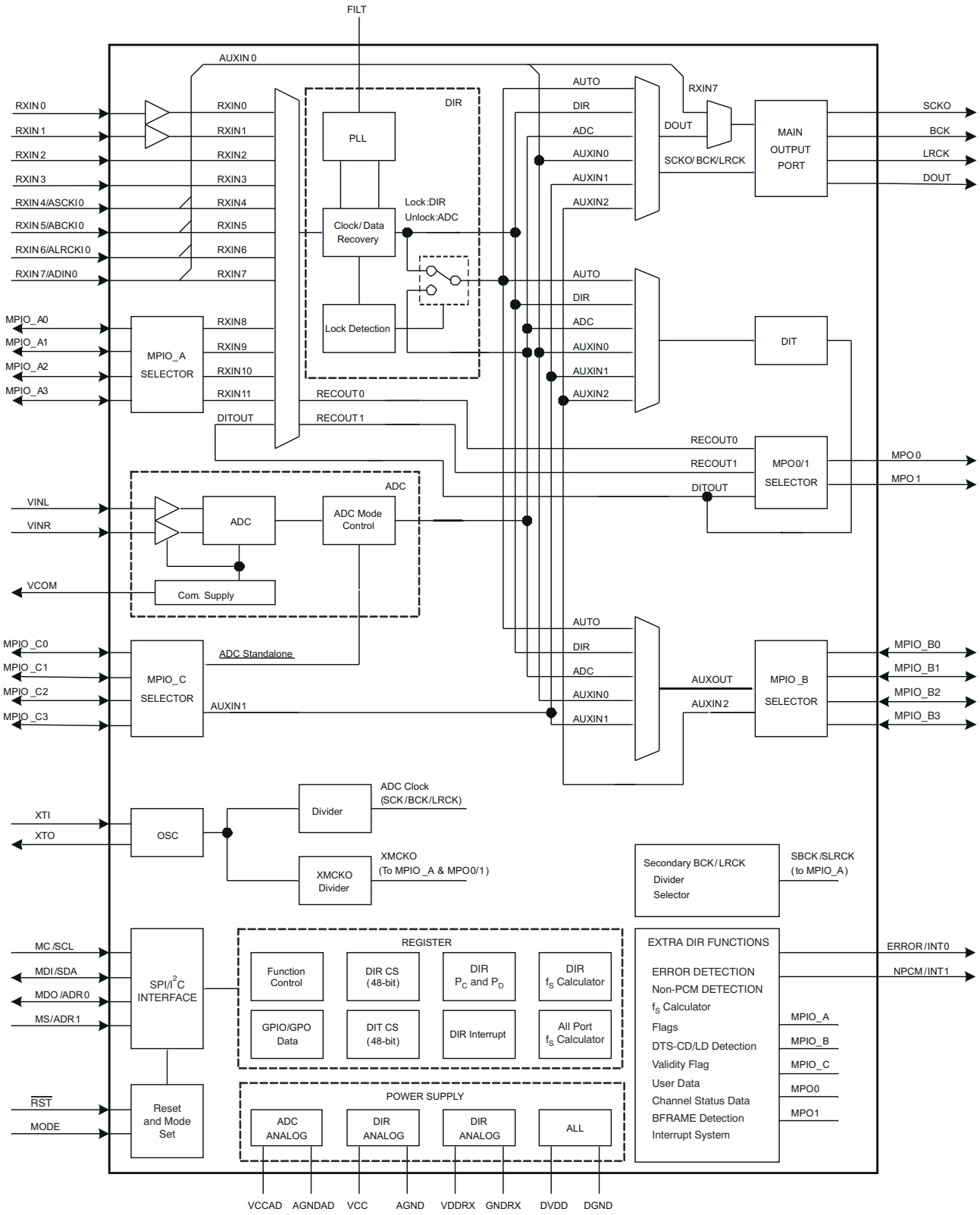
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Digital Audio Interface Receiver (DIR)

Up to 12 single-ended S/PDIF input pins are available on the PCM9211 DIR module. Two of the 12 S/PDIF inputs integrate coaxial amplifiers; the other inputs are designed to be directly connected to CMOS sources (up to 5 V), or standard S/PDIF optical modules.

The DIR module outputs the first 48 bits of channel status data from each frame into specific registers that can be read via the control interface. In addition, the DIR can detect non-PCM data (such as compressed multi-channel data) by looking at channel status bits, burst preambles and DTS-CD/LD. When the DIR detects non-PCM audio data, its status can be configured to the NPCM pin (pin 2). Control of pin 2 (NPCM or INT1) is set by register 2Bh.

When the DIR encounters an error (for example, when it loses a lock), an error signal can be configured and sent to the ERROR pin (pin 1). Control of pin 1 (ERROR or Int0) is set by Register 20h. Preamble data P_C and P_D (typically used to transmit format information such as Digital Theater Sound, or DTS, or AC-3™ data) can be read from registers Register 3Ah through Register 3Dh. For more information, see the audio data standard IEC61937.

The PCM9211 has two interrupt pins (INT0 and INT1) that are shared with other functions (NPCM and ERROR). The interrupt pins, when configured, can be used for operations such as interrupt transmissions to the DSP (for example, instructing the DSP where the start of the frame is, etc.). Eight different factors can drive the interrupt. For more details, see Register 2Ch and Register 2Dh. The interrupt source can also be stored in a register to be read by a DSP, if required.

When switching from one source to the DIR and vice-versa, additional circuitry in the DIR helps continuity between the crystal clock source and an internal phase-locked loop (PLL). During a clock source switch, a clock transition signal can be output that can then be used by the processor to respond accordingly (such as temporarily muting the output).

An integrated sample rate calculator in the DIR can read and detect both the incoming data rate of the S/PDIF input as well as the sample rate information bits that are within the channel status data.

The PCM9211 has an internal clock divider that changes its system clock (SCK) output rate in order to maintain synchronization between the incoming clock and the receiver (based on the autodetector of the incoming data rate). For example, if the user switches from a 96-kHz source to a 48-kHz source, the divider automatically detects the switch and changes the clock dividing ratio to make sure that the subsequent DSP continues to receive the same system clock.

The PCM9211 also has two output ports for the DIR output. The primary output is available from the Main Port and/or MPIO_B; the secondary port is available through MPIO_A. The dividing ratio of BCK and LRCK for the primary output is defined by the DIR. The dividing ratio for the second output (normally taken from MPIO_A) is defined by Register 32h and Register 33h.

When the PLL is locked, the secondary clock source automatically selects the PLL clock ($256f_S$). Otherwise, the XTI clock source is selected. Register 32h should be used for dividing in the lock status (that is, the PLL source). When unlocked, Register 33h should be used (the XTI source).

The PCM9211 has two RECOUT signals that can be routed to the MPO port. The respective sources can be drawn from one of the 12 S/PDIF inputs, or the DIT module.

Channel status, user data, and valid audio data from the S/PDIF stream can be found in various registers or routed to MPIO pins. In addition, the *block start* signal can be routed to an I/O pin, so that any postprocessing DSP can be informed of the start of a frame for decoding data and so forth.

The DIR module in the PCM9211 complies with these digital audio I/F standards:

- S/PDIF
- IEC60958 (formerly IEC958)
- JEITA CPR-1205 (formerly EIAJ CP-1201/340)
- AES3

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- EBU Tech 3250 (also known as AES/EBU)

In addition, the DIR Module within the PCM9211 also meets and exceeds jitter tolerance specifications defined by IEC60958-3 for sampling frequencies between 28 kHz and 216 kHz.

7.3.2 Digital Audio Interface Transmitter (DIT)

The DIT (S/PDIF transmitter) is a relatively simple module. The DIT integrated in the PCM9211 is able to transmit control status and user bits in the data stream, as well as standard 24-bit audio. Channel status, user data, and Audio Valid bits in the stream are configured on incoming MPIO pins.

The DIT complies with the following audio standards:

- S/PDIF
- IEC60958 (formerly IEC958)
- JEITA CPR-1205 (formerly EIAJ CP-1201/340)
- AES3
- EBU Tech 3250 (also known as AES/EBU)

7.3.3 Analog-to-Digital Converter (ADC)

The integrated ADC within the PCM9211 is capable of supporting 24-bit data from 16 kHz up to 96 kHz. The signal-to-noise ratio (SNR) of the ADC module at 96 kHz is 101 dB.

The PCM9211 contains integrated front-end buffer amplifiers for the ADC, thereby reducing the need for external amplifiers. The ADC also has several digital features, including digital volume control (adjustable from –100 dB to 20 dB in 0.5-dB steps), digital mute, and the ability to phase-invert the digital output.

Additionally, interrupts can be generated based on the ADC inputs being larger than user-defined threshold levels.

In standalone mode, the ADC can be either a clock master or a clock slave.

7.3.4 Auxiliary PCM Audio Input and Output (I/O)

There are up to 3x digital auxiliary (AUX) inputs and one AUX output on the PCM9211. These I/Os are multiplexed and shared with RXIN4 through RXIN7, MPIOB, and MPIOC. Each input and output supports a four-wire digital audio interface that is similar to the I^2S protocol. Each I/O can support SCK (system clock), BCK (bit clock), LRCK (left/right clock, or word clock) and data transmissions. The audio format supported through the Aux I/O can be configured for I^2S, 24-bit left-justified (LJ), 24-bit right-justified (RJ), and 16-bit RJ output.

The AUX inputs are designed to be driven in Clock Slave mode. The Aux Output can only operate in Master mode. The system clock can be run from $128f_S$, $256f_S$, and $512f_S$. However, the ADC cannot run from $128f_S$.

7.3.5 Routing

All 3x AUXIN data and clocks, in addition to data and clocks from the ADC and DIR modules, are routed to three output ports. The Main Output Port and Aux Output Port (that can be output through MPIO_B) are both PCM outputs capable of I^2S, RJ, and LJ. The DIT output is an S/PDIF signal output.

All three outputs have individual multiplexers that can select between the AUXINs, DIR, or ADC.

7.3.6 Control Interface

The PCM9211 can be controlled by either SPI or I^2C (up to a 400-kHz I^2C bus). However, on startup, the device goes into a default routing mode. Details of this mode are discussed in the *Serial Control Mode* section. For certain applications, the default configuration may be suitable, and therefore does not require external programming.

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7.3.7 Multipurpose I/O

The PCM9211 includes 12 MPIO (Multi-Purpose Inputs/Outputs) and two MPO (Multi-Purpose Output) pins. These MPIO/MPO pins can be easily set to different configurations through registers to allow different routing and provide data outputs based on the specific application.

The 12 MPIO pins are divided into three groups (A, B, and C); each group has four pins (MPIO_Ax, MPIO_Bx, and MPIO_Cx).

For example, to access all 12 S/PDIF inputs, the MPIO_Ax pins can be configured to support S/PDIF RXIN8 and RXIN11. However, if the application requires an additional I^2S input, then the MPIO_Ax pins can be configured for an Aux In instead of RXIN8 and RXIN11.

7.3.8 PCM9211 Module Descriptions

7.3.8.1 Power Supply

The PCM9211 has four power-supply pins and four ground pins. All ground pins (AGND, AGNDAD, DGND, and GNDRX) must be connected as closely as possible to the PCM9211. The PCM9211 DVDD and DGND pins are power-supply pins that support all the onboard digital circuitry for the PCM9211. DVDD should be connected to a 3.3-V supply. DVDD drives the internal power-on reset circuit, making it a startup requirement.

VCC and AGND are analog power-supply power pins that support the DIR analog supply rails.

VDDAD and AGNDAD are dedicated power-supply pins for the onboard ADC. VDDAD should be connected to a 5.0-V power rail.

VDDRX is a dedicated power supply for the coaxial input amplifiers on pins RXIN0 and RXIN1. It should be connected to a 3.3-V pin. The relative GND pin for this supply is GNDRX. If the coaxial amplifiers are not used (for example, the application only uses optical inputs), then no power supply is required for the VDDRX.

If the onboard ADC is not used (such as when the application uses an external ADC) then no power supply is required for the VCCAD pin. This option means that a 5-V rail is not required when the internal ADC is not used. In such situations, VCCAD should be connected to AGND OR AGNDAD.

Because VCC (3.3 V) is an analog supply (used as part of the power supply for the DIR PLL), make sure that minimum noise and ripple are present. 0.1-µF ceramic capacitors and 10-µF electrolytic capacitors should be used to decouple each supply pin to the respective relative GND (for example, to decouple VCCAD and AGNDAD).

7.3.8.2 Power-Down Function

The PCM9211 has a power-down function that is controlled by the external $\overline{\text{RST}}$ pin or a power control register.

When the $\overline{\text{RST}}$ pin is held at GND, the PCM9211 powers down.

When the device is powered down (that is, $\overline{\text{RST}}$ = GND), all register values are cleared and reset to the respective default values. By default, all modules are powered on except for the coaxial amplifier.

The other option for powering down the device is to use the Power Control Register (Register 40h). The Power Control Register allows selective power down of the DIR, ADC, DIT, Coax Amp, and Oscillator circuit without resetting other registers to the respective default modes.

The advantage of using the registers to power down individual modules of the PCM9211 is that the registers retain the respective settings rather than resetting to default.

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7.3.8.3 System Reset

The PCM9211 has two sources for reset: the internal power-on reset circuit (hereafter called *POR*) and the external reset circuit. See 図 7-4 for an illustration of the timing sequence during an internal power-on reset event. Initialization (reset) is done automatically when V_{DD} exceeds 2.2 V (typ).

When only the onboard POR is to be used, the $\overline{RST}$ pin should be connected to V_{DD} directly. An external pull-up resistor should not be used, because the $\overline{RST}$ pin has an internal pull-down resistor (typ 50 kΩ). If an external resistor is used, then the reset is not released. The reset sequence is shown in 図 7-1. The *Timing Requirements* table lists the timing requirements to reset the device using the $\overline{RST}$ pin.

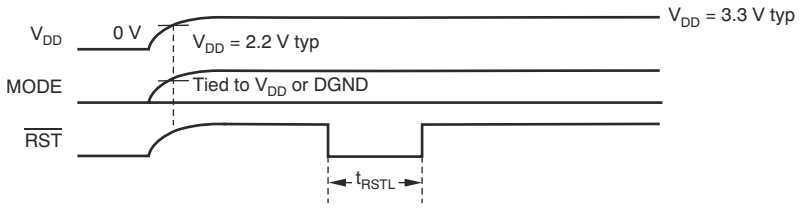

図 7-1. Required System Reset Timing

The condition of each output pins during the device reset is shown in 表 7-2.

表 7-2. Output Pin Condition During Reset

CLASSIFICATION	PIN NAME	AT $\overline{RST}$ = L(1)
Main output port	SCKO	L
	BCK	L
	LRCK	L
	DOUT	L
Flag and status	ERROR/INT0	H
	NPCM/INT1	L
MPIOs and MPOs	MPIO_A0 through MPIO_A3	Hi-Z
	MPIO_B0 through MPIO_B3	Hi-Z
	MPIO_C0 through MPIO_C3	Hi-Z
	MPO0, MPO1	L
Serial I/F	MDI/SDA	Hi-Z
	MDO/ADR0	Hi-Z
Oscillation circuit	XTO	Output
Common supply for ADC	VCOM	Output
Coax input	RXIN0, RXIN1	H

(1) L = low, H = high, Hi-Z = high impedance.

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7.3.8.4 PCM Audio Interface Format

Each of the modules in the PCM9211 (DIR, DIT, ADC, Aux I/Os) supports these four interface formats:

- 24-bit I^{2}S format
- 24-bits Left-Justified format
- 24-bit Right-Justified format
- 16-bit Right-Justified format

32-bit interfaces are supported for the paths from AUXIN0/1/2 to MainPort/AUXOUT.

All formats are provided twos complement, MSB first. They are selectable through SPI-/I^{2}C-accessible registers. The specific control registers are:

- DIR: RXFMT[2:0]
- ADC: ADFMT[1:0]
- DIT: TXFMT[1:0]

図 7-2 shows these formats.

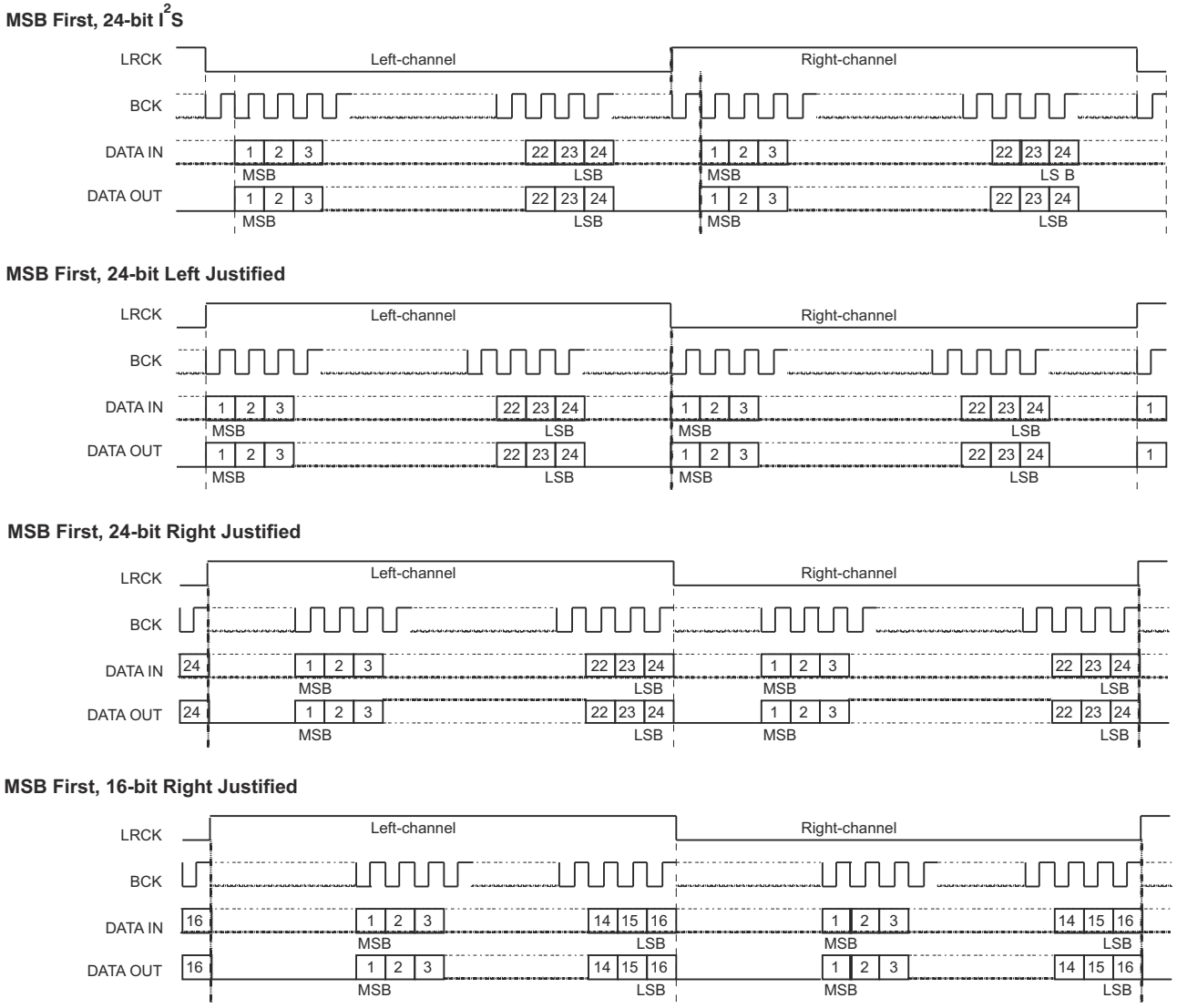

図 7-2. Audio Data Input/Output Format

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7.3.8.5 ADC Details

7.3.8.5.1 System Clock

The system clock for the ADC of the PCM9211 must be either $256f_S$ or $512f_S$, where f_S is the audio sampling rate for the ADC (16 kHz to 96 kHz).

表 7-3 lists the typical system clock frequencies f_{SCK} for common audio sampling rates. 図 7-3 shows the timing requirements for the system clock inputs. The *Timing Requirements* table the timing requirements.

表 7-3. ADC Clock Requirements

SAMPLING FREQUENCY	BIT CLOCK FREQUENCY	SYSTEM CLOCK FREQUENCY	
	$64f_S$	$256f_S$	$512f_S$
16 kHz	1.024 MHz	4.0960 MHz	8.1920 MHz
32 kHz	2.048 MHz	8.1920 MHz	16.3840 MHz
44.1 kHz	2.8224 MHz	11.2896 MHz	22.5792 MHz
48 kHz	3.072 MHz	12.2880 MHz	24.5760 MHz
88.2 kHz	5.6448 MHz	22.5792 MHz	See (1)
96 kHz	6.144 MHz	24.5760 MHz	See (1)

(1) This system clock frequency is not supported for the given sampling clock frequency

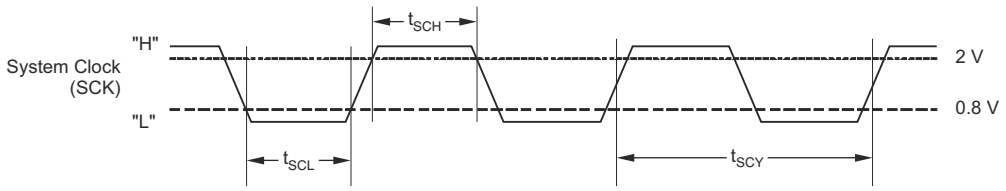

図 7-3. ADC System Clock Input Timing

7.3.8.5.2 ADC: Clock Source Configuration

A number of clock sources for the ADC are provided. Clock source selection is done using the ADCLK[2:0] register (Register 42h). In most applications, the onboard clock (XTI) is used, but using another clock source (such as a DIR recovered clock or AUXIN clock) is also possible. The ADC can only be used in a slave mode unless it is set to run in standalone mode.

1. **Driving the ADC From an XTI (External) Clock**

   The dividing ratio for the incoming clock (XTI) is set by using the registers XSCK[1:0], XBCL[1:0], and XLRCL[1:0] (Register 31h). These registers provide the ability to drive the device up to 192 kHz; however, the integrated ADC sample rate is only supported in the range of 16 kHz to 96 kHz.

   Keep this limitation in mind when setting the registers.

2. **Driving the ADC From the DIR Clock**

   The ADC maximum specified sampling frequency is 96 kHz. The maximum supported frequency of the DIR is 216 kHz. Therefore, special care must be taken when driving the ADC clock from the DIR receiver clock.

   Driving the ADC clock from the DIR is done by setting Register 42h/ADCLK-001. An ADC clock limiter is set in Register 42h/ADFSLMT. This limiter only functions when the DIR is selected as the clock source.

   If the DIR receives data that are over 96 kHz and generates a clock for the ADC that exceeds its specifications, then the ADC is forced into a power-down state. If the limiter is not set, the ADC will run beyond its specified limits and generate erroneous data.

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7.3.8.5.3 ADC: Standalone Operation

This configuration allows separate use of the ADC from the rest of the device. In this configuration, PCM data (SCK, BCK, LRCK, and Data) are routed directly out to MPIO_C.

This mode is the only state where the ADC can act as the master (set in register ADIFMD). In master mode, the ADC can output SCK clocks at $256f_S$ or $512f_S$.

During normal ADC operation, the system clock (SCK) is sourced within the PCM9211 (that is, either the DIR SCK, or the oscillator circuit SCK). By running the ADC in Master mode, the ADC can operate from an external SCK source (such as a DSP or PLL circuit), and provide BCK and LRCK to the rest of the PCM9211 circuitry and external components.

To configure the ADC for standalone operation, set MPCSEL[2:0] to *001*. ADIFMD should also be set to *010* or *100*.

7.3.8.5.4 Additional ADC Functions

The onboard ADC has some additional functions. Control of these functions is done using several registers (Register 40h through Register 49h).

Each ADC channel has a digital attenuator function. The level of attenuation can be set from 20 dB to –100 dB in 0.5-dB steps, and also set to infinite attenuation (mute). By default, the digital gain/attenuation is moved 0.5-dB steps closer from its current level to its new setting only when the sampled output crosses zero (zero crossing). Changing gain or attenuation at zero crossing points in the audio minimizes zipper noise.

If zero crossing is disabled, then the gain steps ±0.5 dB towards its target every $8/f_S$. Zero crossing detection is modified using the ADZCDD register. If zero crossing is not detected for $512/f_S$ (for example, if there is a significant dc bias on the signal), then the level change is done on every samples ($1/f_S$) until zero crossing is detected again.

If updated volume change instructions are received during a volume change, they will be ignored until the current change is complete.

The attenuation level for each channel can be set individually using the following formula:

Attenuation Level (dB) = 0.5 ● ($AT1x[7:0]_{DEC}$ – 215), where $AT1x[7:0]_{DEC}$ = 0 through 255

For $ADATTL[7:0]_{DEC}$ = 0 through 14, attenuation is set to infinite attenuation (mute).

For $ADATTR[7:0]_{DEC}$ = 0 through 14, attenuation is set to infinite attenuation (mute).

7.3.8.5.5 ADC: Power Down and Power Up

If synchronization is maintained among SCKI, BCK, and LRCK, the DOUT from the ADC is enabled and a *fade-in* begins $t_{ADCDLY1} = 2048/f_S$ after the internal reset is released. DOUT then starts to output data corresponding to $V_{IN}L$ and $V_{IN}R$ after $t_{ADCDLY2} = 1936/f_S$ from the start of fade-in. If synchronization is not maintained, the internal reset is not released, and the ADC is held in reset. After resynchronization, the ADC begins its fade-in operation after internal initialization and an initial delay. During fade-in ($t_{ADCDLY1}$ + $t_{ADCDLY2}$) and fade-out ($t_{ADCDLY2}$), SCKI, BCK, and LRCK must be provided. 図 7-4 illustrates the ADC output sequence at power up and power down.

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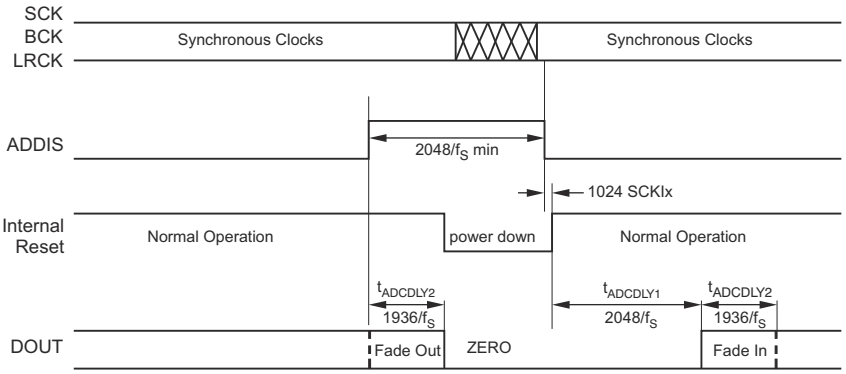

図 7-4. ADC Output At Power Up And Power Down

7.3.8.5.6 ADC: Audio Interface Mode and Timing

The digital audio data can be interfaced in either slave or master mode. The interface mode is selected by using the serial mode control described in the *Serial Control Mode* section. The default mode is slave mode. Master mode is available only for ADC standalone operation by setting Register 6Fh/MPCSEL. In slave mode, BCK and LRCK are inputs to the ADC. BCK must be $64f_S$. DOUT changes on the falling edge of BCK. The default timing specification is shown in 図 7-5. *Timing Requirements* lists the timing descriptions.

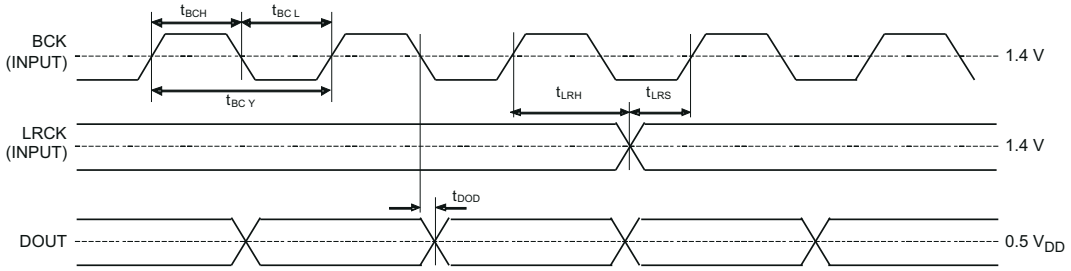

図 7-5. Audio Data Interface Timing (Slave Mode: BCK and LRCK Work as Inputs)

In master mode, BCK and LRCK are output from the ADC of PCM9211. BCK and LRCK are generated by the internal ADC from SCKI, and BCK is fixed as $64f_S$. DOUT changes on the falling edge of BCK. The detailed timing specification is shown in 図 7-6. *Timing Requirements* lists the timing descriptions.

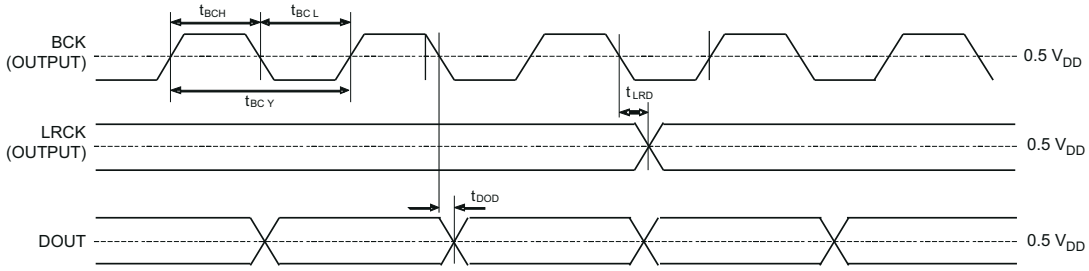

図 7-6. Audio Data Interface Timing (Master Mode: BCK and LRCK Work as Outputs)

7.3.8.5.7 Audio Interface Format

The ADC of the PCM9211 supports the following interface formats in both slave and master modes:

- 24-bit I^2S format
- 24-bit Left-Justified format
- 24-bit Right-Justified format
- 16-bit Right-Justified format

All formats are provided twos complement, MSB first. ADC interface formats are set using register 48h.

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7.3.8.5.8 ADC and Synchronization with Other Clocks

The PCM9211 operates under the system clock (SCKI) and the audio sampling clock (LRCK). The PCM9211 does not require a specific phase relationship between audio interface clocks (LRCK, BCK) and the system clock (SCKI), but does require the synchronization in the frequency of LRCK, BCK and SCKI. This requirement allows SCKI to be provided elsewhere than from LRCK and BCK.

LRCK and BCK require synchronization at all times.

If the relationship between SCKI and LRCK changes more than ±6 BCKs as a result of jitter, a frequency change, and so forth, the internal operation of the ADC stops within $2/f_S$, and the digital output will be ZERO codes until resynchronization between SCKI and LRCK and BCK is completed. Real data begin to be generated a period of $t_{ADCDLY3}$ later.

Changes or drift less than ±5 BCKs do not cause any issues with the device. 図 7-7 shows the ADC digital output when synchronization is lost.

The ADC output, DOUT, maintains its previous state if the system clock stops.

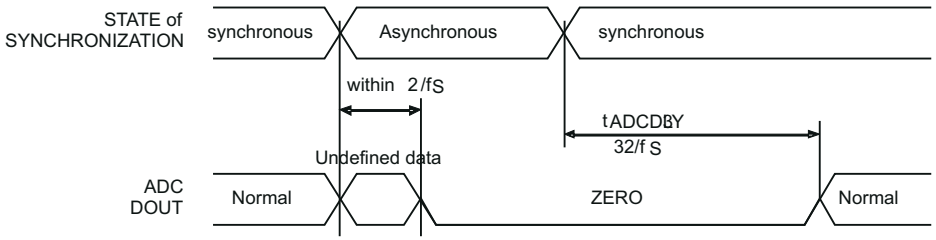

図 7-7. ADC Output for Lost Synchronization

7.3.8.5.9 Setting the ADC Sampling Frequency with XTI as Clock Source

Register 31h holds the bytes that control the dividers used to bring the high-speed, 24.567-MHz clock down to SCK, BCK, and LRCK as used by the ADC.

Note

While the registers allow operation beyond 96 kHz, the ADC itself does not.

7.3.8.5.10 Analog Inputs to the ADC

The ADC module of the PCM9211 has two independent input channels: $V_{IN}L$ and $V_{IN}R$. These are single-ended, unbalanced inputs, each capable of 0.6 V_{CC} V_{PP} input with 10-kΩ input resistance (typ). The ADC also integrates a buffering operational amplifier and a low-pass filter.

7.3.8.5.11 V_{COM} Output

One unbuffered common voltage output pin, V_{COM} (pin 44) is brought out for decoupling purposes. This pin is internally biased to a dc voltage level of 0.5 V_{CCAD} (nominal), and is used as internal reference voltage for the ADC. This pin may be used to bias external circuitry (such as an ADC driver op amp), but the load impedance must be high enough because the output impedance of this pin is typically 12.5 kΩ.

7.3.8.5.12 Oversampling Rate

The oversampling rate of the PCM9211 ADC is fixed at $64f_S$.

7.3.8.5.13 External ADC Mode

To use an external ADC instead of the integrated ADC, the PCM9211 supports *External ADC Mode*. This option enables a connection with an external, 192-kHz capable ADC via the MPIO_B ports. The external ADC must be a clock slave to the PCM9211. The clock source for the external ADC can be selected using Register 42h/ ADCLK (the same register that controls the clock source for the internal ADC).

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To lower power consumption in the PCM9211, the onboard ADC can be set to power-down state using Register 40h/ADDIS.

To use the external ADC mode, Register 6Fh/MPBSEL must be set to '101' (External Slave ADC Input). Then, each MPIO_B port is assigned for MPIO_B0 = EASCKO (output), MPIO_B1 = EABCKO (output), MPIO_B2 = EALRCKO (output), and MPIO_B3 = EADIN (input). The MPIO_B pins should be connected according to this configuration:

- MPIO_B0 to ADC system clock input
- MPIO_B1 to ADC bit clock input
- MPIO_B2 to ADC LR clock input
- MPIO_B3 to ADC data output

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7.3.8.5.14 ADC Level Detect and Interrupt

The PCM9211 has the ability to monitor audio inputs, which can be used to trigger interrupt outputs on port INT1. The ADC has a level monitor that can be set so that INT1 can be triggered whenever a specific level (referenced to 0dBFS) is crossed. A block diagram for this function is shown in 図 7-8.

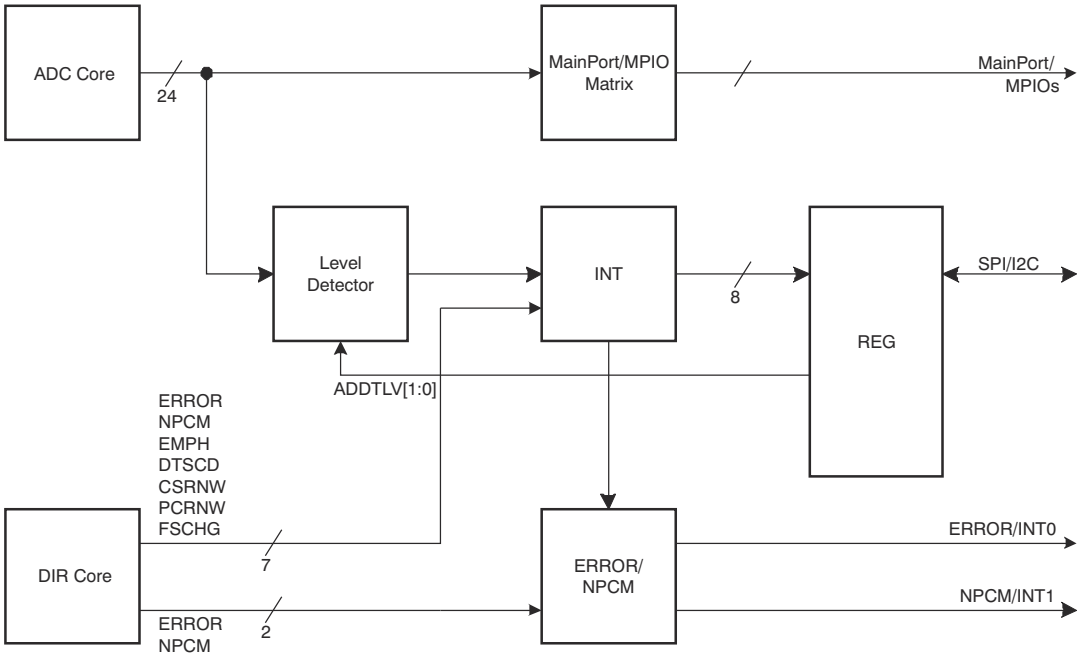

図 7-8. Block Diagram for ADC Level Detection

Operation of the level detect circuitry is shown in 図 7-9. The ADC level detect is flagged when either ADC channel goes high. The flag is cleared when Register 2Dh is read.

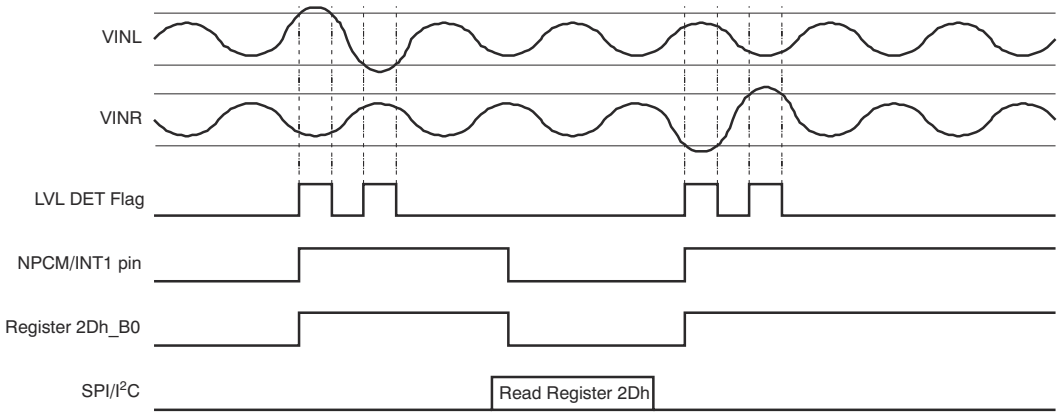

図 7-9. Operation of the ADC Level Detect Circuitry

The trigger threshold for the ADC can be configured at four different levels below full scale using the ADLVLTH[1:0] bits in Register 2Eh. The output is post-ADC volume control, allowing finer gain steps to be configured by changing the ADC volume control.

In a typical application, this level change is done as the system moves into standby, and reset back to 0dB attenuation when the system wakes up.

The output of this comparator circuit can be ORed along with the INT1 interrupt that is sourced. When the INT1 interrupt is flagged, then the INT1 output register can be read by the host controller.

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7.3.8.5.15 Real World Application

By using both the S/PDIF lock status on INT0 and the analog level detect output on INT1, a system controller can place the rest of the system to sleep (such as the Class D amplifier stage, etc). Upon S/PDIF lock, or an ADC input that is above the preset threshold, the controller can wake up and wake up the rest of the system.

In most implementations, it is suggested that as the system goes into standby, only INT1 be used for the ADC level detect function. (that is, mask all other INT1 sources). In addition, it is recommended that this function be implemented one second after startup, in order to allow the internal high-pass filter to settle.

Using such a system allows auto-shutdown, provided that the source moves into its own standby mode (for example, a TV or a set-top box).

7.3.8.6 Digital Audio Interface Receiver (Rxin0 To Rxin11)

7.3.8.6.1 Input Details for Pins Rxin0 through Rxin11

Up to 12 single-ended S/PDIF input pins are available. Two of the S/PDIF input pins integrate coaxial amplifiers. The other 10 pins are designed to be directly connected to CMOS sources or standard S/PDIF optical modules. Each of the inputs can tolerate 5-V inputs.

The DIR module in the PCM9211 complies with these Digital Audio I/F standards:

- S/PDIF
- IEC60958 (formerly IEC958)
- JEITA CPR-1205 (formerly EIAJ CP-1201/340)
- AES3
- EBU Tech 3250 (also known as AES/EBU)

In addition, the DIR module within the PCM9211 also meets and exceeds jitter tolerance limits as specified by IEC60958-3 for sampling frequencies between 28 kHz and 216 kHz.

Each of the physical connections used for these standards (optical, differential, and single-ended) have different signal levels. Take care to make sure that each of the RXIN pins is not overdriven or underdriven, such as driving a coaxial 0.2-V_{PP} signal into a CMOS 3.3-V input.

RXIN0 and RXIN1 integrate coaxial input amplifiers. This architecture means that they can be directly connected to either coaxial input (or RCA/Phono) S/PDIF sources. They can accept a minimum of 0.2V_{PP}. They can also be connected to maximum 5-V TTL sources, such as optical receivers.

Note

Consideration should be made for electrostatic discharge, or ESD, on the input connectors.

RXIN2 to RXIN11 are 5-V tolerant TTL level inputs. These inputs are typically used as connections to optical receiver modules (known as TOSLINK™ connectors).

RXIN8 through RXIN11 are also part of the MPIO_A (Multipurpose Input/Output *A*) group. These I/O pins can either be set as S/PDIF inputs, or reassigned to other functions (see the *MPIO Description* section). To configure MPIO_A as S/PDIF inputs, set Register MPASEL[1:0] to 00.

Typically, no additional components are required to connect an optical receiver to any RXIN pin. However, consideration should be given to the output characteristics of the specific receiver modules used, especially if there is a long printed circuit board (PCB) trace between the receiver and the PCM9211 itself.

For differential inputs (such as the AES/EBU standard), differential to single-ended circuitry is required.

7.3.8.6.2 PLL Clock Source (Built-In PLL and VCO) Details

The PCM9211 an has on-chip PLL (including a voltage-controlled oscillator, or VCO) for recovering the clock from the S/PDIF input signal.

The VCO-derived clock is identified as the PLL clock source.

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When locked, the onboard PLL generates a system clock that synchronizes with the input biphase signal. When unlocked, the PLL generates its own free-run clock (from the VCO).

The generated system clocks from the PLL can be set to fixed multiples of the input S/PDIF frequency. Register 30h/PSCK[2:0] can configure the output clock to $128f_S$, $256f_S$ or $512f_S$.

The PCM9211 also has an automatic default output rate that is calculated based on the incoming S/PDIF frequency. This calculation and rate are controlled by Register 30h/PSCKAUTO. In its default mode, the SCK dividing ratio is configured according to these parameters:

- $512f_S$: 54 kHz and below.
- $256f_S$: 54 kHz to 108 kHz
- $128f_S$: 108 kHz and above (or unlocked)

PSCKAUTO takes priority over any settings in PSCK[2:0]. PSCK[2:0] only becomes relevant in the system when the PSCKAUTO Register is set to 0.

The PCM9211 can decode S/PDIF input signals between sampling frequencies of 7 kHz and 216 kHz for all PSCK[2:0] settings. The relationship between the output clock (SCKO, BCKO, LRCKO) at the PLL source and PSCK[2:0] selection is shown in 表 7-4.

表 7-4. SCKO, BCKO and LRCKO Frequency Set by PSCK[2:0]

OUTPUT CLOCK AT PLL SOURCE			PSCK[2:0] SETTING		
SCKO	BCKO	LRCKO	PSCK2	PSCK1	PSCK0
$128f_S$	$64f_S$	f_S	0	0	0
$256f_S$	$64f_S$	f_S	0	1	0
$512f_S$ (1)	$64f_S$	f_S	1	0	0

(1) $512f_S$ SCK is only supported at 108 kHz or lower sampling frequency of incoming biphase signal.

In PLL mode, the output clocks (SCKO, BCKO, LRCKO) are generated from the PLL source clock.

The relationship between the sampling frequencies (f_S) of the input S/PDIF signal and the frequency of LRCKO, BCKO, and SCKO are shown in 表 7-5.

表 7-5. Output Clock Frequency at PLL Lock State

LRCK	BCK	SCK(1)		
f_S	$64f_S$	$128f_S$	$256f_S$	$512f_S$
8 kHz	0.512 MHz	1.024MHz	2.048 MHz	4.096 MHz
11.025 kHz	0.7056 MHz	1.4112 MHz	2.8224 MHz	5.6448 MHz
12 kHz	0.768 MHz	1.536 MHz	3.072 MHz	6.144 MHz
16 kHz	1.024 MHz	2.048 MHz	4.096 MHz	8.192 MHz
22.05 kHz	1.4112 MHz	2.8224 MHz	5.6448 MHz	11.2896 MHz
24 kHz	1.536 MHz	3.072 MHz	6.144 MHz	12.288 MHz
32 kHz	2.048 MHz	4.096 MHz	8.192 MHz	16.384 MHz
44.1 kHz	2.8224 MHz	5.6448 MHz	11.2896 MHz	22.5792 MHz
48 kHz	3.072 MHz	6.144 MHz	12.288 MHz	24.576 MHz
64 kHz	4.096 MHz	8.192 MHz	16.384 MHz	32.768 MHz
88.2 kHz	5.6448 MHz	11.2896 MHz	22.5792 MHz	45.1584 MHz
96 kHz	6.144 MHz	12.288 MHz	24.576 MHz	49.152 MHz
128 kHz	8.192 MHz	16.384 MHz	32.768 MHz	N/A
176.4 kHz	11.2896 MHz	22.5792 MHz	45.1584 MHz	N/A
192 kHz	12.288 MHz	24.576 MHz	49.152 MHz	N/A

(1) Depending on PSCK[2:0] setting.

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7.3.8.6.3 DIR and PLL Loop Filter Details

The PCM9211 incorporates a PLL for generating clocks synchronized with the input biphase signal (S/PDIF). The onboard PLL requires an external loop filter. The components and configuration shown in 図 7-10 and 表 7-6 are recommended for optimal performance, with these considerations:

- The resistor and capacitors that configure the filter should be located and routed as close as possible to the PCM9211. The external loop filter must be placed on the FILT pins.
- The GND node of the external loop filter must be directly connected with AGND pin of the PCM9211; it must be not combined with other signals.

図 7-10 shows the configuration of the external loop filter and the connection with the PCM9211.

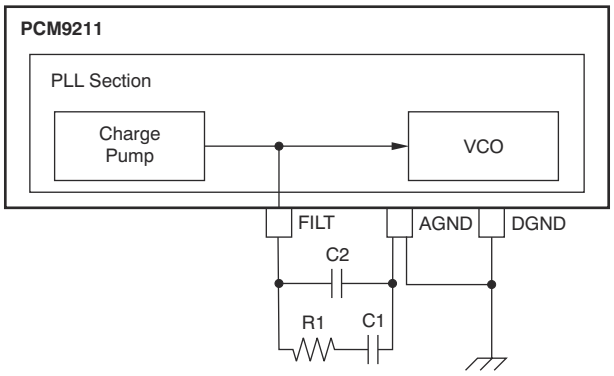

図 7-10. Loop Filter Connection

The recommended value of loop filter components is shown in 表 7-6.

表 7-6. Recommended Value of Loop Filter Components

REF. NO.	RECOMMENDED VALUE	TYPE	TOLERANCE
R_1	680 Ω	Metal film or carbon	≤ 5%
C_1	0.068 µF	Film or ceramic (CH or C0G)	≤ 5%
C_2	0.0047 µF	Film or ceramic (CH or C0G)	≤ 5%

7.3.8.6.4 External (XTI) Clocks, Oscillators, and Supporting Circuitry

An external clock source (CMOS or crystal/resonator) is known as the *XTI source*. The XTI source can be either a CMOS logic source, or a crystal resonator (internal circuitry in the PCM9211 can start the crystal resonating). Whichever clock source is used, it must be 24.576 MHz.

The PCM9211 uses the XTI source as a reference clock in order to calculate the sampling frequency of the incoming S/PDIF stream. It is also used as the clock source in XTI clock source mode.

When using a resonator as an XTI source, the following points should be considered:

- The 24.576-MHz resonator should be connected between the XTI and XTO pins
- The resonator should be a fundamental mode type
- A crystal or ceramic resonator can be used as the XTI source
- The values of the load capacitors C_{L1} and C_{L2} and the current limiting resistor R_d all depend on the characteristics of the resonator
- No external feedback resistor between the XTI and XTO pins is required, because the resistor is integrated into the device
- No loads other than the resonator should be used on the XTO pin

When using an external oscillation circuit with a CMOS output, the following points should be considered:

- Always supply a 24.576-MHz clock on the XTI pin
- Only 3.3 V is supported on the XTI pin; 5 V is not supported

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- XTO should be left floating

図 7-11 shows the connections for the XTI and XTO pins for both a resonator connection and an external clock input connection.

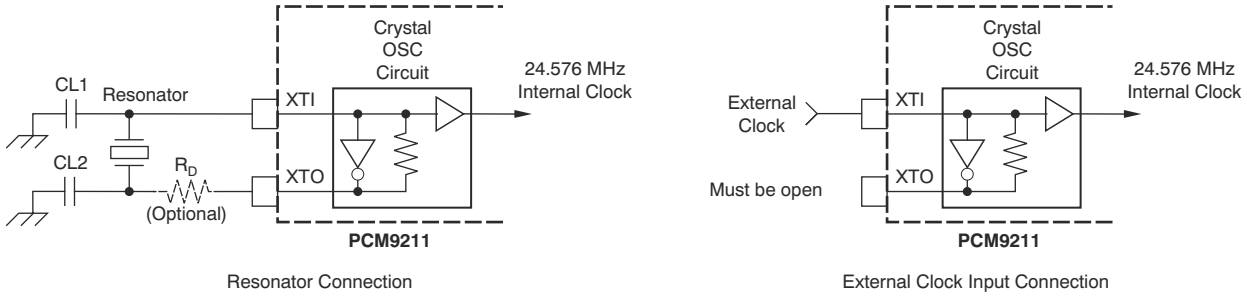

図 7-11. XTI and XTO Connection Diagram

In XTI mode, the output clocks (SCKO, BCKO, and LRCKO) are generated from the XTI source clock.

Register 24h/OSCAUTO controls whether or not the internal oscillator functions while it is not required. When using the DIR as a clock source, the XTI source is not required; thus, the internal oscillator can be switched off. There is a constraint, however, that when the DIR wide mode is being set (for example, in 192-kHz support), the XTI is always used. The sampling frequency calculator also requires the XTI source.

XMCKO (the XTI clock buffered output) provides a buffered (and divided) XTI clock that can be output to MPIO_A. Register 24h/XMCKEN controls whether the XMCKO should be muted or not, and Register 24h/XMCKDIV controls the division factor.

7.3.8.6.5 DIR Data Description

Decoded Serial Audio Data Output and Interface Format

The PCM9211 supports the following four data formats for the decoded data:

- 16-bit MSB First, Right-Justified
- 24-bit MSB First, Right-Justified
- 24-bit MSB First, Left-Justified
- 24-bit MSB First, I^2S

Decoded data are MSB first and twos complement in all formats.

The format of the decoded data is selected by the RXFMT[2:0] register. 表 7-7 lists the possible data formats.

表 7-7. DIR Serial Audio Data Output Format Set by RXFMT[2:0]

DIR SERIAL AUDIO DATA OUTPUT FORMAT	RXFMT[2:0] SETTING		
	RXFMT2	RXFMT1	RXFMT0
24-bit MSB First, Right-Justified	0	0	0
16-bit MSB First, Right-Justified	0	1	1
24-bit MSB First, I^2S (Default)	1	0	0
24-bit MSB First, Left-Justified	1	0	1

図 7-12 depicts the latency time between the input biphase signal and LRCKO/DOUT. 図 7-13 illustrates the DIR decoded audio data output timing. *Timing Requirements* lists the timing requirements.

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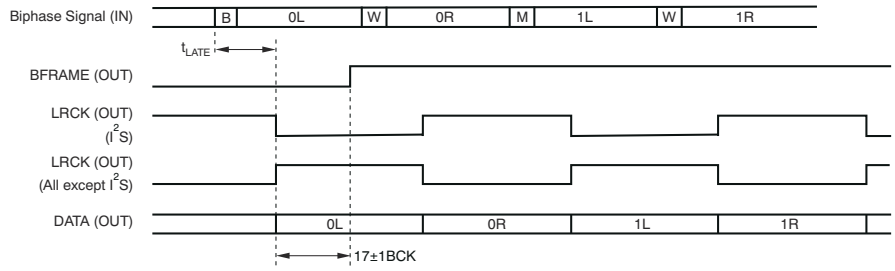

図 7-12. Latency Time Between Input Biphase and LRCKO/DOUT

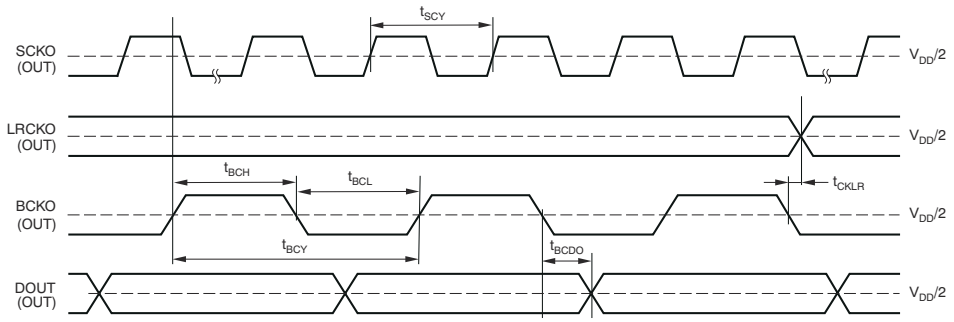

図 7-13. DIR Decoded Audio Data Output Timing

7.3.8.6.6 Channel Status Data, User Data, and Validity Flag

The PCM9211 can output decoded channel status data, user data, and a validity flag synchronized with audio data from the input S/PDIF signal. These signals can be transmitted from any of the three MPIOs (MPIO_A, MPIO_B, or MPIO_C). To assign this function to the MPIOs, see the *MPIO Description* section.

Each type of output data has own dedicated output pin:

- Channel status data (***C***) are output through MPIOs assigned as COUT.
- User data (***U***) are output through MPIOs assigned as UOUT.
- Validity flag (***V***) is output through MPIOs assigned as VOUT
- Data (left and right) are identified as DOUT.

C, U, and V output data are synchronized with the recovered LRCKO (left-right clock output) from the S/PDIF input signal.

The polarity of the recovered LRCKO from the S/PDIF input depends on the Register 2Fh/RXFMT[2:0] setting.

The beginning of each S/PDIF frame (BFRAME) is provided as one of the outputs on the MPIO. It can be used to indicate the start of the frame to the decoding DSP. If the DIR decodes a start-of-frame preamble on the decoded data, then it sets BFRAME high for 8xLRCK periods to signify the start of the frame.

LRCKO can be used as a reference clock for each of the data outputs, BFRAME, DOUT, COUT, UOUT, and VOUT. The relationship between each output is shown in 図 7-14.

Numbers 0 to 191 of DOUT, COUT, UOUT, and VOUT in 図 7-14 indicate the frame number of the input biphase signal.

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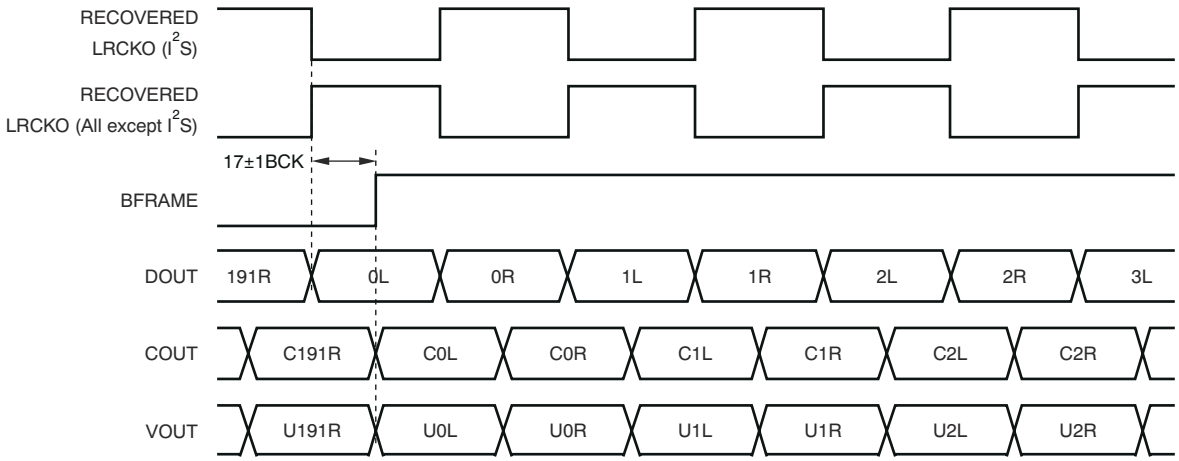

図 7-14. LRCKO, DOUT, BFRAME, COUT, UOUT, and VOUT Output Timing

The RXVDLY Register in Register 22h controls when the VOUT pin goes high (either immediately, or at the start of the sample/frame). 図 7-15 shows these timing sequences.



図 7-15. RXVDLY and VOUT Timing

7.3.8.6.7 DIR: Parity Error Processing

Error detection and processing for parity errors behave in the following manner:

- For PCM data, when an error is detected (for example, a parity error), then the data from the previous sample are repeated. This sequence is shown in 図 7-16, where sample L_{n+1} is repeated because the incoming data (L_{n+2}) had an error.
- For non-PCM data, the data are output *as is* with no changes. (Non-PCM data implies data which has Channel Status bit 1 = 1.)

図 7-16 shows the processing for parity error occurrence.

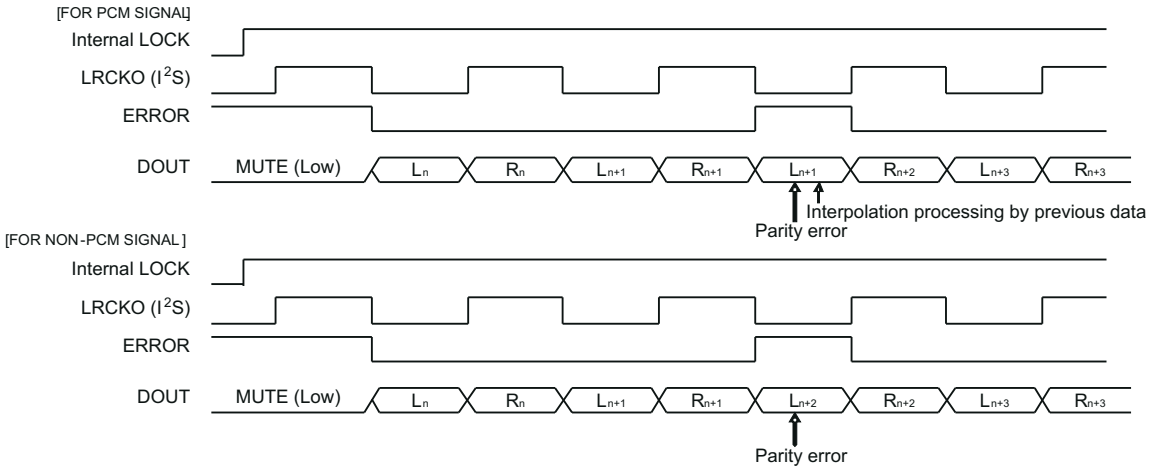

図 7-16. Processing for Parity Error Occurrence

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The PCM9211 handles parity errors as directed by the 23h/PRTPRO[1:0] registers.

When set to 01, if the error is received eight times sequentially, the DIR output is muted on the next error. Until the mute is enabled, the previously *accurate* sample is repeated. This function is only valid for PCM data.

When set to 10, the device behaves in exactly the same way as it does when set to 01. However, this function is enabled for both PCM and non-PCM data.

When set to 00, the device ignores parity errors and continues to output whatever data comes into the device.

The setting on 11 is reserved.

7.3.8.6.8 DIR: Errors and Interrupts

The PCM9211 has two pins that are used to inform the system DSP or controller that there is an error, or an interrupt that it should be aware of.

The ERR/INT0 and NPCM/INT1 pins can be configured in these ways:

HARDWARE PIN	OPTIONS
ERR/INTO0	DIR Error (default), INT0 or Hi-Z
NPCM/INT1	DIR NPCM (default), INT1 or Hi-Z

When configured as direct DIR error connections (ERR, NPCM), the system audio processor typically treats them as dedicated interrupt pins to change or control audio processing software. An example would be that the system may mute if an ERR signal is detected. Another example is that if the DSP receives an NPCM interrupt, it begins looking for AC-3 or DTS preambles in the incoming encoded S/PDIF stream.

For more advanced users, the two pins can be set up as interrupt sources. The seven interrupt sources (ERROR, NPCM, DTS-CD/LD, Emphasis, Channel Status Start, Burst Preamble Start, f_S Calculator Complete) can be masked into Registers INT0 and INT1.

Upon receipt of an interrupt source (such as f_S Calculator Complete), INT0 or INT1 performs a bitwise evaluation of *AND* (&) with an inverted mask [Register 2Ah (INT0) and Register 2Bh (INT1)], then perform an eight-way *OR* of the data. If the output is 1, then INTx is set to 1, which can be used to trigger an interrupt in the host DSP. The host can then poll the INTx register to determine the interrupt source. 図 7-17 shows the logic that the device uses to mask the DIR interrupts from the INTx register.

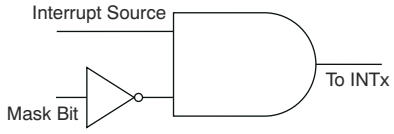

図 7-17. DIR Interrupt Mask Logic

Once the register is read, each of the bits in the register (INT0 and INT1) are cleared. If the signal is routed to ERR/INT0 or NPCM/INT1, the output pin is also cleared.

By default, the mask registers are set to mask all inputs; that is, all inputs are rejected, in which case no interrupt can be seen on the output until the mask is changed.

A block diagram for the error output and interrupt output is shown in 図 7-18.

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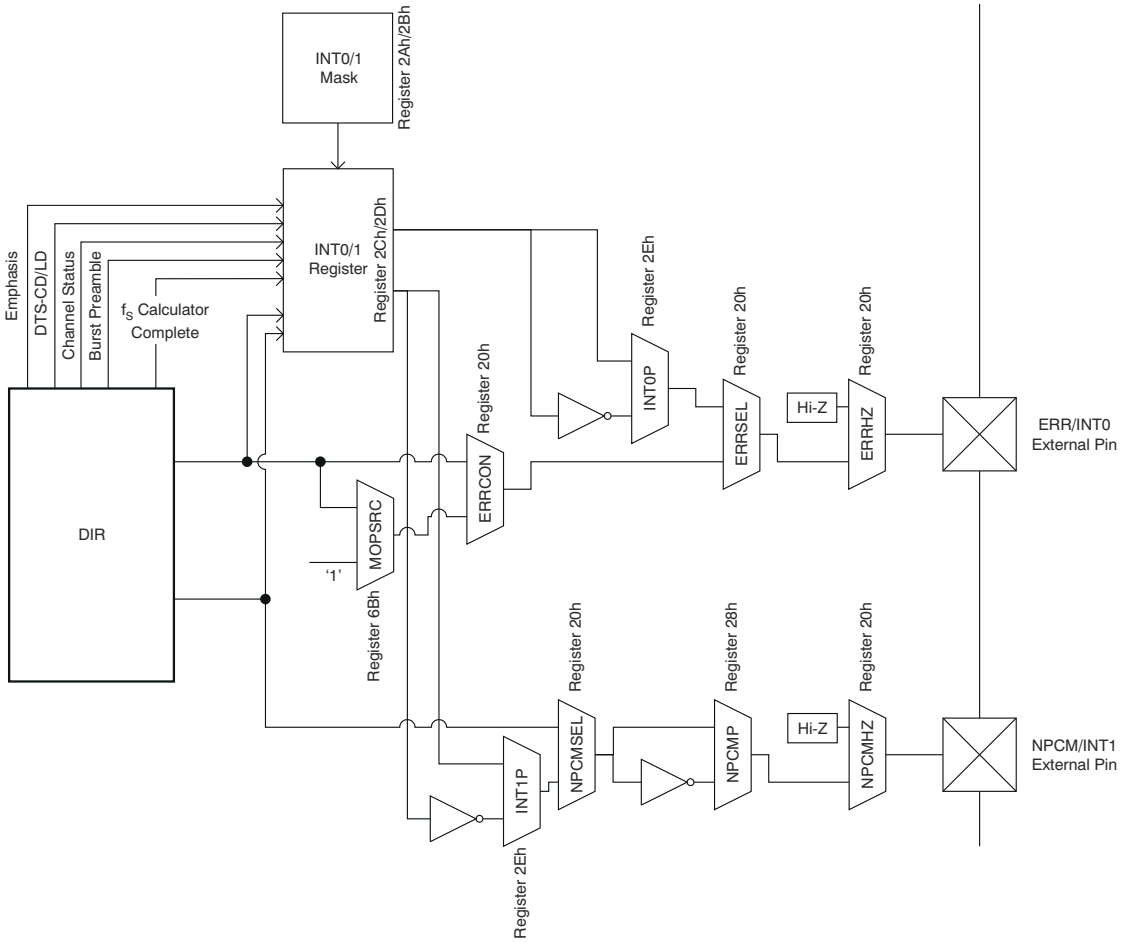

図 7-18. Error Output and Interrupt Output Block Diagram

There are several allowable error sources from the DIR:

- Change of incoming S/PDIF sample frequency (Register 25h / EFSCHG)
- *Out-of-range* incoming S/PDIF signal (Register 25h / EFSLMT)
- Non-PCM data (Register 25h / ENPCM)
- Data invalid flag is the stream (Validity bit = 1) (Register 25h / EVALID)
- Parity error (Register 25h / EPARITY)
- PLL unlock (default) (Register 25h / EUNLOCK)

The error sources can be selected using Register 25h.

There are also several interrupts within the device that can be masked:

- Error in DIR (this error is selectable from the list above in Register 25h)
- When the device detects non-PCM data
- When the Emphasis flag in the channel status of the incoming data has been set
- When DTS-CD data have been detected by the device
- When the Channel Status (CS) is updated
- When Burst Preamble (P_C) is updated
- When the sampling frequency is changed.
- When the analog input crosses the Analog Input Detect level (available only on INT1).

Each interrupt source can be masked by Register 2Ah (INT0) and Register 2Bh (INT1).

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7.3.8.6.9 DIR: Sampling Frequency Calculator for Incoming S/PDIF Inputs

The PCM9211 has two integrated sampling frequency calculators. The first calculator is always connected to the output of the DIR. It calculates the actual sampling frequency of the incoming S/PDIF signal. The result can be read from a register, or output through the MPIO pins. Note that this process is not the same as reading the Channel Status value for the sample rate that the transmitting equipment may be sending.

To use this function, a 24.576-MHz clock source must be supplied to the XTI pin. The 24.576-MHz clock is used as a reference clock to calculate the incoming S/PDIF sampling frequency. If the XTI pin is connected to DGND, the function is disabled and the calculation is not performed. If there is an error in the XTI clock frequency, the calculation result and range will be incorrect.

The result is decoded into 4-bit data and stored in Register 39h/SFSOUT[3:0]; the MPIO pins are then assigned to the SFSOUT[3:0] function.

The data in the SFSOUT[3:0] register (and available as a signal for the MPIO section) are the calculated sampling frequency based on the incoming S/PDIF stream, and not what is reported in Channel Status bits 24 to 27. If the PLL becomes unlocked, or attempts to run out of range, SFSOUT[3:0] = '0000' is output, and indicates abnormal operation.

If the XTI source clock is not supplied before the PCM9211 powers up, SFSOUT [3:0] outputs '0000'. If the XTI source clock is stopped, the f_S calculator holds its most recent calculated result. Once the XTI source clock is restored, the f_S calculator resumes operation.

Register 39h/SFSST indicates the calculator status. Before reading SFSOUT[3:0], it is recommended that the user verify that the SFSST status is 0.

The relationship between SFSOUT[3:0] outputs and the range of sampling frequency f_S is shown in 表 7-8.

表 7-8. Calculated Biphase Sampling Frequency Output

NOMINAL f_S	ACTUAL SAMPLING FREQUENCY RANGE	CALCULATED SAMPLING FREQUENCY OUTPUT(1)			
		SFSOUT3	SFSOUT2	SFSOUT1	SFSOUT0
Out of range	Out of range	0	0	0	0
8 kHz	7.84 kHz to 8.16 kHz	0	0	0	1
11.025 kHz	10.8045 kHz to 11.2455 kHz	0	0	1	0
12 kHz	11.76 kHz to 12.24 kHz	0	0	1	1
16 kHz	15.68 kHz to 16.32 kHz	0	1	0	0
22.05 kHz	21.609 kHz to 22.491 kHz	0	1	0	1
24 kHz	23.52 kHz to 24.48 kHz	0	1	1	0
32 kHz	31.36 kHz to 32.64 kHz	0	1	1	1
44.1 kHz	43.218 kHz to 44.982 kHz	1	0	0	0
48 kHz	47.04 kHz to 48.96 kHz	1	0	0	1
64 kHz	62.72 kHz to 65.28 kHz	1	0	1	0
88.2 kHz	86.436 kHz to 89.964 kHz	1	0	1	1
96 kHz	94.08 kHz to 97.92 kHz	1	1	0	0
128 kHz	125.44 kHz to 130.56 kHz	1	1	0	1
176.4 kHz	172.872 kHz to 179.928 kHz	1	1	1	0
192 kHz	188.16 kHz to 195.84 kHz	1	1	1	1

(1) The flag SFSOUT[3:0] is output from the register and MPIOs are assigned as SFSOUT[3:0].
0 or 1 indicates the register output data. The symbol 'H' or 'L' refers to the MPIO output electrical signal.

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The Biphase Sampling Frequency Calculator is also used for restricting the type of data that can be received.

1. If Register 27h/MSK128 is set to 1, the PCM9211 does not accept 128-kHz sampling frequency data
2. If Register 27h/MSK64 is set to 1, the PCM9211 does not accept 64-kHz sampling frequency data.
3. If Register 27h/NOMLMT is set to 1, the PCM9211 only accepts the nominal audio sampling frequency within ±2%.The nominal audio sampling frequencies are 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz,32 kHz, 44.1 kHz, 48 kHz, 64 kHz, 88.2 kHz, 96 kHz, 128 kHz, 176.4 kHz, and 192 kHz.
4. For Register 27h/HILMT[1:0] and Register 27h/LOLMT[1:0]: These registers are used for setting a higher or lower limit to the acceptable sampling frequency.

Register 21h/RXFSRNG is used for global control of the acceptable sampling frequencies. If normal mode is selected, the range of acceptable sampling frequency is restricted from 28 kHz to 108 kHz. If wide mode is selected, the range is from 7 kHz to 216 kHz.

7.3.8.6.10 DIR: Audio Port Sampling Frequency Calculator

The second sampling frequency calculator can be used to calculate the sampling frequency of DIR, ADC, AUXIN0, AUXIN1, AUXIN2, Main Output Port, AUX Output Port, and DIT Input. 図 7-19 illustrates the sampling frequency calculator sources.

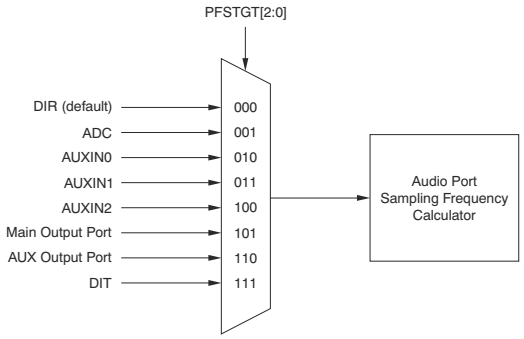

図 7-19. Sampling Frequency Calculator Sources

The calculated sampling frequency f_S is decoded to 4-bit data and stored in the PFSOUT[3:0] register. The input source of this counter is selectable from AUXIN0, AUXIN1, AUXIN2, DIR, ADC, Main Output Port, AUX Output Port, and DIT by using the Register 37h/PFSTGT[3:0].

To use this function, a 24.576-MHz clock source must be supplied to the XTI pin. The 24.576-MHz clock is used as a reference clock. If the XTI pin is connected to DGND, the calculation is not performed. If there is an error in the XTI clock frequency, the calculation result and range will be incorrect.

Register 38h/PFSST indicates the calculator status. It is recommended that PFSST is checked (for *complete* status) before reading PFSOUT[3:0].

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7.3.8.6.11 Output Register Construction

The output 8-bit register is subdivided into three sections. The first four bits show the decoded result. The next three bits signify the source; the final bit signifies the calculator status (finished or not).

The lock range of the counter (to the specified f_S given in 表 7-9) are any clock rate within ±2%. The relation between the nominal f_S and actual measured f_S range is shown in 表 7-9.

表 7-9. Calculated Port Sampling Frequency Output

NOMINAL f_S	ACTUAL SAMPLING FREQUENCY RANGE (MIN)	CALCULATED SAMPLING FREQUENCY OUTPUT			
		PFSOUT3	PFSOUT2	PFSOUT1	PFSOUT0
Out of range	Out of range	0	0	0	0
8 kHz	7.84 kHz to 8.16 kHz	0	0	0	1
11.025 kHz	10.8045 kHz to 11.2455 kHz	0	0	1	0
12 kHz	11.76 kHz to 12.24 kHz	0	0	1	1
16 kHz	15.68 kHz to 16.32 kHz	0	1	0	0
22.05 kHz	21.609 kHz to 22.491 kHz	0	1	0	1
24 kHz	23.52 kHz to 24.48 kHz	0	1	1	0
32 kHz	31.36 kHz to 32.64 kHz	0	1	1	1
44.1 kHz	43.218 kHz to 44.982 kHz	1	0	0	0
48 kHz	47.04 kHz to 48.96 kHz	1	0	0	1
64 kHz	62.72 kHz to 65.28 kHz	1	0	1	0
88.2 kHz	86.436 kHz to 89.964 kHz	1	0	1	1
96 kHz	94.08 kHz to 97.92 kHz	1	1	0	0
128 kHz	125.44 kHz to 130.56 kHz	1	1	0	1
176.4 kHz	172.872 kHz to 179.928 kHz	1	1	1	0
192 kHz	188.16 kHz to 195.84 kHz	1	1	1	1

7.3.8.6.12 DIR: Auto Source Selector for Main Output and AUX Output

The AUTO source selector is an automatic system that selects the DIR or ADC output based on specific DIR conditions set by Register 26h. The AUTO source selector is integrated in both the Main Port and the AUX output separately.

The typical behavior for the AUTO source selector is shown in 図 7-20. This example is the default register setting for Register 26h. In this case, only Register 26h/AUNLOCK is selected.

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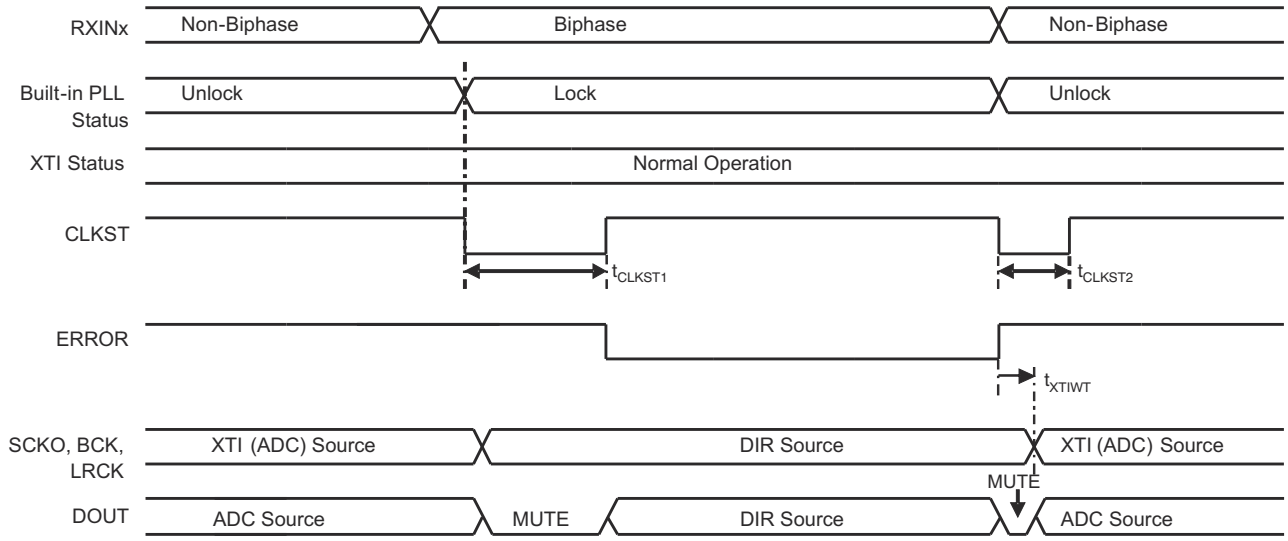

図 7-20. Typical Behavior for Auto Source Selector

When the DIR is unlocked, the ADC output is automatically routed to the Main Output Port.

Polarity of the CLKST signal is configured by Register 22h/CLKSTP. The default is active low, which means that clock source either changes from DIR to ADC, or from ADC to DIR.

If the DIR is locked, then the DIR output is routed to the Main Output Port automatically after t_{CLKST1}. During that period, the output port is muted. t_{CLKST1} can be configured using Register 23h/ERRWT[1:0]. t_{CLKST2} is 50 ms, providing that an XTI clock of 24.576 MHz is applied.

If the DIR loses its lock a subsequent time, the ADC output is routed to the Main Output Port automatically after t_{XTIWT}. Once again, the output port is muted during this time. t_{XTIWT} can be configured using Register 23h/XTIWT[1:0].

The auto source selector can be triggered by the following changes in the DIR (Register 26h is used to select which variable to use as the trigger):

- DIR error (discussed earlier in *DIR: Errors and Interrupts*; configured by Register 25h)
- Out-of-range sampling frequency
- Non-PCM data
- When the Validity flag in the S/PDIF stream is 1
- When the PLL is unlocked (default)

図 7-21 shows the Clock Tree Diagram for the AUTO source selector.

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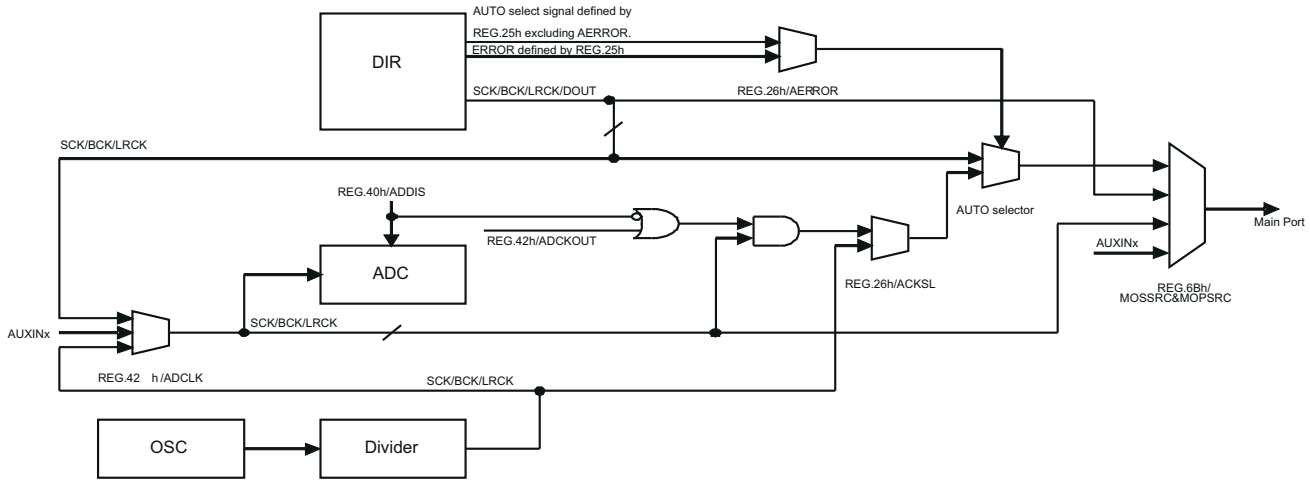

図 7-21. Clock Tree Diagram for Auto Source Selector

7.3.8.6.13 Non-PCM Data Detection

The PCM9211 can also detect Non-PCM data (AC-3, DTS-CD, and so forth) using one of these two methods:

1. Channel Status Bit 1 is 1.

   If Register 28h/CSBIT is set to 1, this function is enabled. Register 39h/SCSBIT1 always indicates Channel Status Bit 1 status even if CSBIT1 is disabled.
2. A Burst Preamble (P_A/P_B) is found in the S/PDIF stream.

   If Register 28h/PAPB or Register 28h/DTSCD is set to 1, this function is enabled. If DTS-CD detection is active, it uses DTSCD, and can also be set in Register 29h/DTS16, 29h/DTS14, and Register 29h/DTSPRD[1:0].

If the PCM9211 detects a Burst Preamble when Non-PCM detection is enabled, an error signal and BPSYNC signal are generated. The BPSYNC signal can be monitored through MPIO_A/MPIO_B/MPIO_C. For more details, see the *MPIO Description* section of this document. The error signal can be monitored from either the ERR_INT0 pin or the NPCM_INT1 pin.

7.3.8.6.14 P_C/P_D Monitor

The PCM9211 has a P_C and P_D buffer for monitoring the latest P_C or P_D. Registers 3Ah and 3Bh are assigned for the P_C buffer; Registers 3Ch and 3Dh are assigned for the $P_D$buffer.

The following sequence is an example of reading P_C/P_D buffers. This example is based on using the INT0 function.

1. Set Register 2Ah/MPCRNW0 to 0.
2. Check that Register 2Ch/OPCRNW0 is 1.
3. Read the P_C and P_D buffers.

7.3.8.7 Digital Audio Interface Transmitter

7.3.8.7.1 Overview

The PCM9211 has an onboard Digital Audio Interface Transmitter (DIT) that transmits S/PDIF data from 7 kHz to 216 kHz, up to 24-bit audio data. The first 48 bits of the channel status buffer are programmable. The source for the DIT is selectable from the built-in routing function of the PCM9211 as well as the dedicated inputs assigned to the MPIOs.

7.3.8.7.2 Selection of DIT Input Source

Selection of the DIT audio and clock sources is done using the Registers 60h/TXSSRC[2:0] and 60h/TXPSRC[2:0]. The system clock source for the DIT is selected using the Register 60h/TXSSRC[2:0]. The PCM audio data source for the DIT (BCK. LRCK, and Data) is selected using the Register 60h/TXPSRC[2:0].

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The DIT can also be operated in a standalone mode. In standalone mode, the data source is provided through MPIO_C. See the *Standalone Operation* section for more details.

7.3.8.7.3 DIT Output Biphase

The S/PDIF-encoded signal generated by the DIT module is available through the MPO0 and MPO1 pins. The MPO selection registers (Register 78h/MPOxSEL[3:0]) can be set to '1101' to determine the DIT output through one of these two pins.

In addition to the standard MPOx pins, the DIT output can also be multiplexed to the RECOUT pin, or back into the DIR. An example of where this multiplexing might occur is in a jitter cleaner application. The DIR in the PCM9211 has excellent jitter reduction. Data can be brought in from an auxiliary source, transmitted through the DIT internally, then routed to the DIR. This process, in turn, cleans the clocks and provides a stable, well-clocked PCM source. This feature is especially useful for jittery sources, such as HDMI.

7.3.8.7.4 Audio Data and Clock

The DIT can accept a $128f_S$, $256f_S$, or $512f_S$ system clock. The clock ratio selection is set by using the Register TXSCK[2:0]. A 216-kHz sampling frequency is supported by using the $128f_S$ or $256f_S$ system clock ratio. A 108-kHz sampling frequency can be supported up to a $512f_S$ clock ratio.

I^2S, 24-bit left-justified, 24-bit right-justified, and 16-bit right-justified serial audio interface formats can be used. Only slave mode is supported. 表 7-10 shows the relationship between typical audio sampling frequencies and the respective BCK and SCK frequencies

表 7-10. Typical Audio Sampling, BCK, and SCK Frequencies

LRCK	BCK	SCK		
f_S	$64f_S$	$128f_S$	$256f_S$	$512f_S$
8 kHz	0.512 MHz	1.024MHz	2.048 MHz	4.096 MHz
11.025 kHz	0.7056 MHz	1.4112 MHz	2.8224 MHz	5.6448 MHz
12 kHz	0.768 MHz	1.536 MHz	3.072 MHz	6.144 MHz
16 kHz	1.024 MHz	2.048 MHz	4.096 MHz	8.192 MHz
22.05 kHz	1.4112 MHz	2.8224 MHz	5.6448 MHz	11.2896 MHz
24 kHz	1.536 MHz	3.072 MHz	6.144 MHz	12.288 MHz
32 kHz	2.048 MHz	4.096 MHz	8.192 MHz	16.384 MHz
44.1 kHz	2.8224 MHz	5.6448 MHz	11.2896 MHz	22.5792 MHz
48 kHz	3.072 MHz	6.144 MHz	12.288 MHz	24.576 MHz
64 kHz	4.096 MHz	8.192 MHz	16.384 MHz	32.768 MHz
88.2 kHz	5.6448 MHz	11.2896 MHz	22.5792 MHz	45.1584 MHz
96 kHz	6.144 MHz	12.288 MHz	24.576 MHz	49.152 MHz
128 kHz	8.192 MHz	16.384 MHz	32.768 MHz	N/A
176.4 kHz	11.2896 MHz	22.5792 MHz	45.1584 MHz	N/A
192 kHz	12.288 MHz	24.576 MHz	49.152 MHz	N/A

7.3.8.7.5 Data Mute Function

The PCM9211 has the ability to mute the audio data on its DIT output. This option is set using Register 62h/ TXDMUT. During a mute state (TXDMUT = 1), the biphase stream continues to flow, but all audio data are zeroed.

The channel status data and validity flag are not zeroed. Mute is done at the LRCK edge for both L-ch and R-ch data at the same time.

7.3.8.7.6 Channel Status Data

The DIT has the ability to transmit channel status (CS) data for the first 48 bits of the 128-bit stream. These 48 bits cover the standards for both S/PDIF and AES/EBU. These bits are set in Registers TXCS0 through TXCS47. These values are used on both the Left and Right channels of the output stream.

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Upon reset, these registers are all 0 by default.

7.3.8.7.7 User Data

This DIT does not have the ability to transmit custom user data (known as "U Bits" in the stream).

7.3.8.7.8 Validity Flag

Setting the valid flag is possible in the DIT by using Register 62h/TXVFLG. The same value is used for both left and right channels.

7.3.8.7.9 Standalone Operation

Standalone operation for the DIT module is provided by supplying external clocks and data (SCK, BCK, LRCK, and Data). In standalone mode, the audio and clock data must be brought into the device through MPIO_C. To enable standalone mode, set Register 6Fh/MPCSEL[2:0] to '101'. This configuration then bypasses the standard DIT connections through the device and connects them directly to MPIO_C.

Channel Status and Validity flags continue to be sourced from the same registers as they would during normal DIT operation.

7.3.8.8 MPIO Description

7.3.8.8.1 Overview

The PCM9211 offers significant flexibility through its MPIO pins. Depending on the system partitioning of the specific end product, the pins can be reconfigured to offer various I/Os that complement the design.

There are 14 flexible pins: 12 are Input/Output pins, and two pins that are output only.

The 12 multi-purpose I/O (MPIO) pins are grouped into three banks, each with four pins: MPIO_A, MPIO_B, and MPIO_C.

The two multi-purpose outputs (MPO) pins are assigned as MPO0 and MPO1.

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7.3.8.8.2 Assignable Signals for MPIO Pins

The PCM9211 has the following signals that can be brought out to MPIOs. Not all MPIOs are equal; be sure to review subsequent sections in this document to see which signals can be brought out to which MPIO. The possible signals are summarized in 表 7-11.

表 7-11. Allowable MPIO Signals

MODULE	ALLOWABLE SIGNALS
DIR	Extended biphase input pins for DIR: RXIN8/RXIN9/RXIN10/RXIN11
	DIR Flags Output: The details of each signal are described in the *Channel Status Data, User Data, and Validity Flag* section.
	DIR Interrupt Output: INT0 and INT1
	DIR, B frame, serial output of channel status, user data, validity flag
	DIR, decoded result of sampling frequency calculated by built-in f_S counter
Auxiliary I/O	AUXIN0, external serial audio data input (SCK/BCK/LRCK/Data)
	AUXIN1, external serial audio data input (SCK/BCK/LRCK/Data)
	AUXIN2, external serial audio data input (SCK/BCK/LRCK/Data)
	AUXOUT, external serial audio data output (SCK/BCK/LRCK/Data)
ADC	Serial audio data output for ADC Standalone Operation
DIT	Serial audio data input for DIT Standalone Operation
Application-Specific	AVR Application1: Clock Transition Output, Validity Output, XTI buffered Output, Interrupt Output
	AVR Application2: Secondary BCK/LRCK Output, XTI buffered Output, Interrupt Output
Digital Logic Specific	GPIO (General Purpose I/O), Logical high or low I/O, selectable I/O direction for each pin
	Hi-Z status, selectable for each pin

7.3.8.8.3 How to Assign Functions to MPIO

Both MPO0 and MPO1 have a function assignment register. The output of MPO0 can be selected using the MPO0SEL[3:0] register; in the same way, the output of MPO1 can be selected using the MPO1SEL[3:0] register. Selecting the biphase source can be done using Register 35h/RO0SEL and Register 36h/RO1SEL. Muting the MPO can be done using Registers MPO0MUT and MPO1MUT.

7.3.8.8.4 Selection of Output Source

The PCM9211 also has a routing function for serial digital audio clocks and data. This function routes between all input sources (DIR, ADC, AUXIN0, AUXIN1, AUXIN2) and Main Out, AUXOUT, and DIT. The selection for Main Out and AUXOUT is set with these registers:

- **Main Out:** Registers 6Bh, MOSSRC[2:0], and MOPSRC[2:0]
- **AUXOUT:** Register 6Ch, AOSSRC[2:0], and AOPSC[2:0]

Muting Main Out and AUXOUT is done using Register 6Ah. Hi-Z control for Main Out is set with Register 6Dh.

7.3.8.8.5 Assignable Signals to MPO Pins

Both MPO pins have the same function. The following signals can be routed to the MPOs:

- DIR flags output (details of signals are described in the *Channel Status Data, User Data, and Validity Flag* section)
- DIR Interrupt Output: INT0 and INT1
- B frame, serial output of channel status, user data and validity flag of DIR
- GPO (general-purpose output), Hi-Z / Logical high or low
- DIT biphase Output
- XTI buffered Output

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- RECOUT0 or RECOUT1, two independent multiplexers, are provided

To use the limited pins of the PCM9211 economically, the DIR flag outputs and the GPIO are used at same time within the number of MPIO pins assigned to DIR flags or to GPIO functions. *DIR flags* or *GPIO* can be selected for each MPIO zone by using Registers MPASEL[1:0], MPBSEL[2:0], and MPCSEL[2:0]

Note

To identify the pins in each MPIO group, the convention * represents 0 to 3.

When DIR flags are required on hardware pins, users should select the desired signals with Registers MPA*FLG, MPB*FLG, and MPC*FLG.

When GPIOs are required, set the I/O direction with GIOA*DIR, GIOB*DIR, and GIOC*DIR registers. When a GPO (general-purpose output) function is required, set the output data with Registers GPOA*, GPOB*, and GPOC*. When a GPI (general-purpose input) function is required, the status of the pins with an assigned GPI function is stored in the GPIA*, GPIB*, and GPIC* registers (these registers are read-only).

7.3.8.8.6 MPIO and MPO Assignments

The I/O function of the MPIOs and MPOs are assigned by Registers MPASEL[1:0], MPBSEL[2:0], MPCSEL[2:0], MPO0SEL[3:0], and MPO1SEL[3:0]. The available functions are shown in 表 7-12 through 表 7-16.

表 7-12. MPIO Group A (Pin: MPIO_A0 – MPIO_A3)

MPASEL[1:0]	DIRECTION	MPIO GROUP A FUNCTION
00	IN	Biphase input (RXIN8/RXIN9/RXIN10/RXIN11)
01	OUT	AVR Application 1 (CLKST, VOUT, XMCKO, INT0) (default)(1)
10	OUT	AVR Application 2 (SBCK, SLRCK, XMCKO, INT0)
11	IN/ OUT	DIR Flags output or GPIOs

(1) MPIO_A0 to MPIO_A3 are set to *Hi-Z* by the MPA0HZ to MPA3HZ registers as default.

表 7-13. MPIO Group B (Pin: MPIO_B0 – MPIO_B3)

MPBSEL[2:0]	DIRECTION	MPIO GROUP B FUNCTION
000	IN	AUXIN2, ASCKI2/ABCKI2/ALRCKI2/ADIN2 (default)
001	OUT	AUXOUT, ASCKO/ABCKO/ALRCKO/ADOUT
010	OUT	Sampling frequency calculated result output, SFSOUT[3:0]
011	IN/OUT	DIR Flags Output or GPIO
100	OUT	DIR BCU_{V_Output} (BFRAME/COUT/UOUT/VOUT)
101	IN/OUT	External slave ADC input (EASCKO/EABCKO/EALRCKO/EADIN)
110	N/A	Reserved
111	N/A	Reserved

表 7-14. MPIO Group C (Pin: MPIO_C0 – MPIO_C3)

MPCSEL[2:0]	DIRECTION	MPIO GROUP C FUNCTION
000	IN	AUXIN1 (ASCKI1/ABCKI1/ALRCKI1/ADIN1) (default)
001	IN/OUT	ADC Standalone, clock, and data (ADSCK/ADBCK/ADLRCK/ADDOUT)
010	OUT	Sampling frequency calculated result output, SFSOUT[3:0]
011	IN/OUT	DIR Flags output or GPIO
100	OUT	DIR BCUV output (BFRAME/COUT/UOUT/VOUT)
101	IN	DIT Standalone, clock, and data (TXSCK/TXBCK/TXLRCK/TXDIN)
110	N/A	Reserved
111	N/A	Reserved

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表 7-15. MPO0 Pin

MPO0SEL[3:0]	DIRECTION	MPO0 FUNCTION
0000	OUT	Hi-Z
0001	OUT	GPO0, Output data = Logic high level
0010	OUT	GPO0, Output data = Logic low level
0011	OUT	VOUT
0100	OUT	INT0
0101	OUT	INT1
0110	OUT	CLKST
0111	OUT	EMPH
1000	OUT	BPSYNC
1001	OUT	DTSCD
1010	OUT	PARITY
1011	OUT	LOCK
1100	OUT	XMCKO
1101	OUT	TXOUT (default)
1110	OUT	RECOUT0
1111	OUT	RECOUT1

表 7-16. MPO1 Pin

MPO1SEL[3:0]	DIRECTION	MPO1 FUNCTION
0000	OUT	Hi-Z
0001	OUT	GPO1, Output data = Logic high level
0010	OUT	GPO1, Output data = Logic low level
0011	OUT	VOUT (default)
0100	OUT	INT0
0101	OUT	INT1
0110	OUT	CLKST
0111	OUT	EMPH
1000	OUT	BPSYNC
1001	OUT	DTSCD
1010	OUT	PARITY
1011	OUT	LOCK
1100	OUT	XMCKO
1101	OUT	TXOUT
1110	OUT	RECOUT0
1111	OUT	RECOUT1

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7.3.8.8.7 MPIO Description

Description for Signal Name Assigned to MPIO

表 7-17 through 表 7-25 list the details of where each of the internal PCM9211 signals can be routed to. For instance, DIR LOCK can be output to any of the MPIO and MPO pins, while SBCK (Secondary Clock Output) can only be brought out through MPIO_A0.

表 7-17. DIR Flags Output

SIGNAL NAME	MPIO GROUP / PIN	DESCRIPTION
CLKST	All MPIOs, MPO0/1	Clock transient status signal output
INT0	All MPIOs, MPO0/1	Interrupt system 0, Interrupt event detection output
INT1	All MPIOs, MPO0/1	Interrupt system 1, Interrupt event detection output
EMPH	All MPIOs, MPO0/1	Channel status, emphasis detection output
BPSYNC	All MPIOs, MPO0/1	Burst preamble sync signal output
DTSCD	All MPIOs, MPO0/1	DTS-CD/LD detection output
PARITY	All MPIOs, MPO0/1	Biphase parity error detection output
LOCK	All MPIOs, MPO0/1	PLL lock detection output

表 7-18. DIR B Frame, Channel Status, User Data, Validity Flag Output

SIGNAL NAME	MPIO GROUP / PIN	DESCRIPTION
BFRAME	All MPIOs, MPO0/1	B frame output
COUT	All MPIOs	Channel status data
UOUT	All MPIOs	User data
VOUT	All MPIOs	Validity flag

表 7-19. DIR Calculated Sampling Frequency Output

SIGNAL NAME	MPIO GROUP / PIN	DESCRIPTION
SFSOUT0	All MPIOs	Calculated f_S, decoded output, bit0
SFSOUT1	All MPIOs	Calculated f_S, decoded output, bit1
SFSOUT2	All MPIOs	Calculated f_S, decoded output, bit2
SFSOUT3	All MPIOs	Calculated f_S, decoded output, bit3

表 7-20. Biphase Input

SIGNAL NAME	MPIO GROUP / PIN	DESCRIPTION
RXIN8	MPIO_A0	Biphase signal input 8
RXIN9	MPIO_A1	Biphase signal input 9
RXIN10	MPIO_A2	Biphase signal input 10
RXIN11	MPIO_A3	Biphase signal input 11

表 7-21. Biphase Output

SIGNAL NAME	MPIO GROUP / PIN	DESCRIPTION
RECOUT0	MPO0/1	Independent biphase selector 0, output0
RECOUT1	MPO0/1	Independent biphase selector 1, output1
TXOUT	MPO0/1	Built-in DIT, biphase output

表 7-22. AUX Clocks Output

SIGNAL NAME	MPIO GROUP / PIN	DESCRIPTION
SBCK	MPIO_A0	Secondary bit clock output
SLRCK	MPIO_A1	Secondary LR clock output
XMCKO	MPIO_A2, MPO0/1	XTI pin input clock buffered output

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表 7-23. Audio Clock and Data I/O

SIGNAL NAME	MPIO GROUP / PIN	DESCRIPTION
ASCKI1	MPIO_C0	AUXIN1, system clock input
ABCKI1	MPIO_C1	AUXIN1, bit clock input
ALRCKI1	MPIO_C2	AUXIN1, LR clock input
ADIN1	MPIO_C3	AUXIN1, data input
ASCKI2	MPIO_B0	AUXIN2, system clock input
ABCKI2	MPIO_B1	AUXIN2, bit clock input
ALRCKI2	MPIO_B2	AUXIN2, LR clock input
ADIN2	MPIO_B3	AUXIN2, data input
ASCKO	MPIO_B0	AUXOUT, system clock output
ABCKO	MPIO_B1	AUXOUT, bit clock output
ALRCKO	MPIO_B2	AUXOUT, LR clock output
ADOUT	MPIO_B3	AUXOUT, data output
EASCKO	MPIO_B0	External Slave ADC Input, system clock output
EABCKO	MPIO_B1	External Slave ADC Input, bit clock output
EALRCKO	MPIO_B2	External Slave ADC Input, LR clock output
EADIN	MPIO_B3	External Slave ADC Input, data input
TXSCK	MPIO_C0	DIT Standalone, system clock input
TXBCK	MPIO_C1	DIT Standalone, bit clock input
TXLRCK	MPIO_C2	DIT Standalone, LR clock input
TXDIN	MPIO_C3	DIT Standalone, data input
ADSCK	MPIO_C0	ADC Standalone, system clock input
ADBCK	MPIO_C1	ADC Standalone, bit clock input/output
ADLRCK	MPIO_C2	ADC Standalone, LR clock input/output
ADDOUT	MPIO_C3	ADC Standalone, data output

表 7-24. GPIO (General-Purpose Input/Output)

SIGNAL NAME	MPIO GROUP / PIN	DESCRIPTION
GPIA0	MPIO_A0	General-purpose input
GPIA1	MPIO_A1	General-purpose input
GPIA2	MPIO_A2	General-purpose input
GPIA3	MPIO_A3	General-purpose input
GPOA0	MPIO_A0	General-purpose output
GPOA1	MPIO_A1	General-purpose output
GPOA2	MPIO_A2	General-purpose output
GPOA3	MPIO_A3	General-purpose output
GPIB0	MPIO_B0	General-purpose input
GPIB1	MPIO_B1	General-purpose input
GPIB2	MPIO_B2	General-purpose input
GPIB3	MPIO_B3	General-purpose input
GPOB0	MPIO_B0	General-purpose output
GPOB1	MPIO_B1	General-purpose output
GPOB2	MPIO_B2	General-purpose output
GPOB3	MPIO_B3	General-purpose output
GPIC0	MPIO_C0	General-purpose input
GPIC1	MPIO_C1	General-purpose input
GPIC2	MPIO_C2	General-purpose input

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表 7-24. GPIO (General-Purpose Input/Output) (continued)

SIGNAL NAME	MPIO GROUP / PIN	DESCRIPTION
GPIC3	MPIO_C3	General-purpose input
GPOC0	MPIO_C0	General-purpose output
GPOC1	MPIO_C1	General-purpose output
GPOC2	MPIO_C2	General-purpose output
GPOC3	MPIO_C3	General-purpose output

表 7-25. GPO (General-Purpose Output)

SIGNAL NAME	MPIO GROUP / PIN	DESCRIPTION
GPO0	MPO0	General-purpose output
GPO1	MPO1	General-purpose output

7.3.8.8.8 MPIO And MPO Assignment: Pin Assignment Details

Each MPIO group has four pins. 表 7-26 through 表 7-28 describe the signals assigned to each group.

表 7-26. MPIO Group A

MPASEL[1:0]	ASSIGNED PIN FUNCTION			
	MPIO_A0	MPIO_A1	MPIO_A2	MPIO_A3
00	RXIN8	RXIN9	RXIN10	RXIN11
01 (Default)	CLKST	VOUT	XMCKO	INT0
10	SBCK	SLRCK	XMCKO	INT0
11	DIR Flag / GPIO(1)	DIR Flag / GPIO(1)	DIR Flag / GPIO (1)	DIR Flag / GPIO(1)

(1) This function, DIR Flag Output or GPIO, is set for each pin by Registers MPA0FLG, MPA1FLG, MPA2FLG, and MPA3FLG.

表 7-27. MPIO Group B

MPBSEL[1:0]	ASSIGNED PIN FUNCTION			
	MPIO_B0	MPIO_B1	MPIO_B2	MPIO_B3
000 (Default)	ASCKI2	ABCKI2	ALRCKI2	ADIN2
001	ASCKO	ABCKO	ALRCKO	ADOUT
010	SFSOUT3	SFSOUT2	SFSOUT1	SFSOUT0
011	DIR Flag / GPIO(1)	DIR Flag / GPIO (1)	DIR Flag / GPIO(1)	DIR Flag / GPIO(1)
100	BFRAME	COUT	UOUT	VOUT
101	EASCKO	EABCKO	EALRCKO	EADIN
110	Reserved	Reserved	Reserved	Reserved
111	Test Mode	Test Mode	Test Mode	Test Mode

(1) This function, DIR Flag Output or GPIO, is set for each pin by Registers MPB0FLG, MPB1FLG, MPB2FLG, and MPB3FLG.

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表 7-28. MPIO Group C

MPCSEL[1:0]	ASSIGNED PIN FUNCTION			
	MPIO_C0	MPIO_C1	MPIO_C2	MPIO_C3
000 (Default)	ASCKI1	ABCKI1	ALRCKI1	ADIN1
001	ADSCK	ADBCK	ADLRCK	ADDOUT
010	SFSOUT3	SFSOUT2	SFSOUT1	SFSOUT0
011	DIR Flag / GPIO(1)	DIR Flag / GPIO (1)	DIR Flag / GPIO(1)	DIR Flag / GPIO(1)
100	BFRAME	COUT	UOUT	VOUT
101	TXSCK	TXBCK	TXLRCK	TXDIN
110	Reserved	Reserved	Reserved	Reserved
111	Reserved	Reserved	Reserved	Reserved

(1) This function, DIR Flag Output or GPIO, is set for each pin by Registers MPC0FLG, MPC1FLG, MPC2FLG, and MPC3FLG.

7.3.8.9 Default Routing Function (After Reset)

The default routing paths are shown in 図 7-22. MPIO_A0-A3 are selected by CLKST, VOUT, XMCKO, and INT0. Note that by default, MPIO_A0-A3 pins are *Hi-Z*as set by Registers MPA0HZ, MPA1HZ, MPA2HZ, and MPA3HZ.

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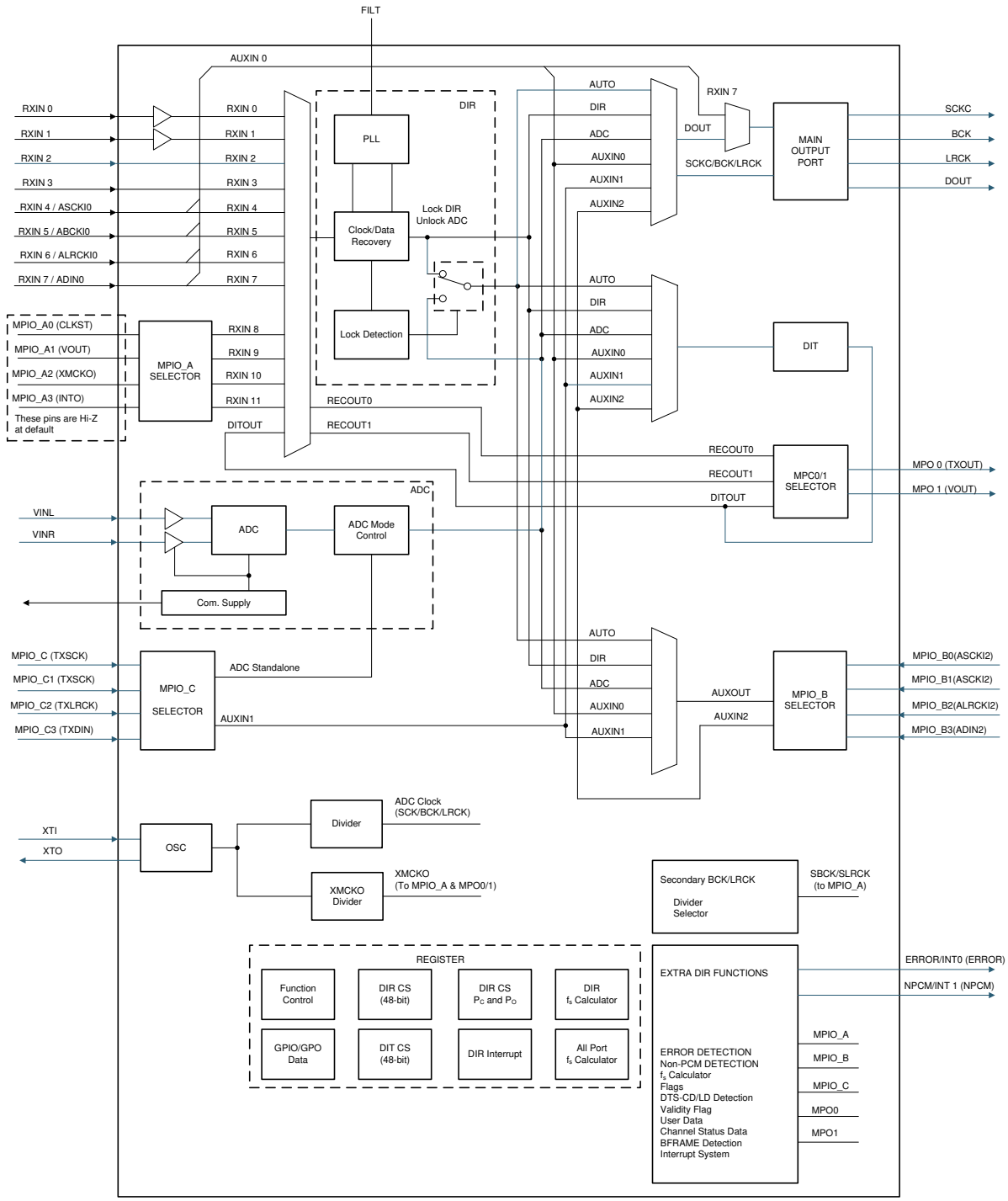

図 7-22. Default Routing Block Diagram

By default, the ADC starts up as a clock slave to the crystal that is connected to the PCM9211. The DIR receives data on RXIN2. When the DIR is unlocked, the ADC has priority, and uses the Main port. When the DIR is locked, data from the MAIN PORT are DIR data.

7.3.8.10 Multichannel PCM Routing Function

7.3.8.10.1 Overview

The PCM9211 has a multi-channel PCM routing function (maximum of eight channels) that can route multi-channel PCM signals easily. This function is enabled by using all the MPIOs.

MPIO_A and MPIO_C are assigned as multi-channel PCM input ports and clock transition outputs (CLKST).

MPIO_B and the Main audio port are assigned as multi-channel PCM output ports. For some applications, these multi-channel PCM output ports have five data pins. The DOUT pin and the MDOUT pin share the same data.

A detailed block diagram is shown in 図 7-23.

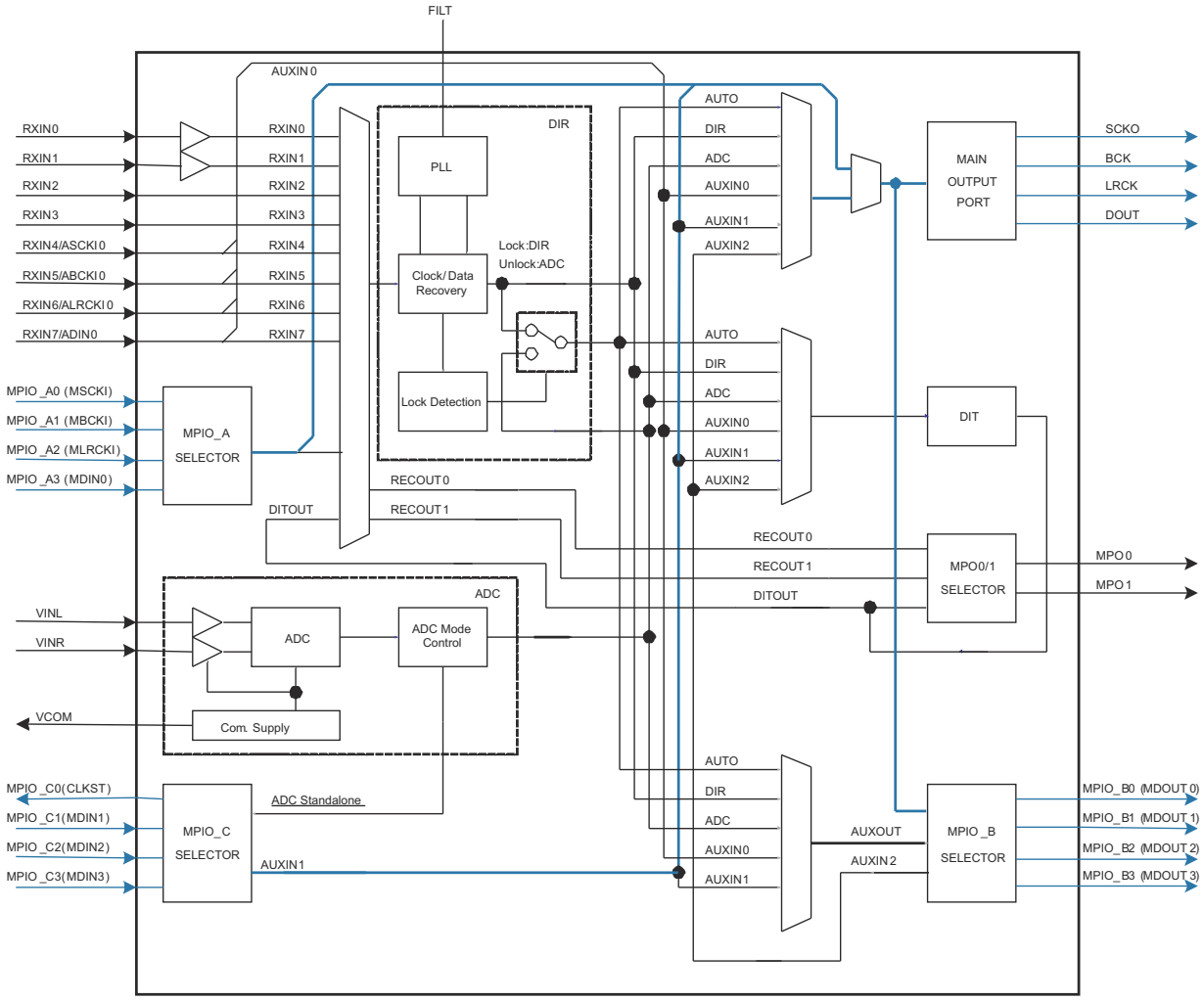

図 7-23. Multichannel PCM Routing Block Diagram

7.3.8.10.2 Initial Setting

To use the multi-channel function, set Register MCHR to 1. In the multi-channel function, the assigned MPIO function for Registers MPASEL[1:0], MPBSEL[2:0], and MPCSEL[2:0], are invalid; in other words, Register MCHR has greater priority than Registers MPASEL[1:0], MPBSLE[2:0], and MPCSEL[2:0].

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Note

In multi-channel PCM mode, Register MCHR (20h) and Register MPAxHz (6Eh) must be set to 0 in order to get the outputs from the main port.

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7.3.8.10.3 Output Source Selection

The output source for Multi-Channel PCM Output (the Main output port and MPIO_B) is selected by a register. 表 7-29 describes the relationship between the output source and the register (MCHRSRC) setting.

表 7-29. Multichannel PCM Output Source and Register Setting

MULTI-CHANNEL MODE OUTPUT SOURCE SELECT	MCHRSRC	
	00 or 10	01 or 11
CLOCK SOURCE	MAIN OUT (1)	MULTI-CH INPUT
DOUT	MAIN OUT (1)	MDIN0
MDOUT0	MAIN OUT (1)	MDIN0
MDOUT1	Logic low	MDIN1
MDOUT2	Logic low	MDIN2
MDOUT3	Logic low	MDIN3

(1) The *Main OUT* data source is discussed in the *Digital Audio Interface Receiver (Rxin0 To Rxin11)* section of this data sheet. It can either be the DIR recovered clock and data, or the ADC DATA and the ADC clock source.

7.4 Device Functional Modes

7.4.1 DSD Input Mode

The PCM9211 can also be used to suppress the jitter of the DSCKI signals, typically generated by an HDMI receiver. DSD signals (DBCKI, DSDRI, DSDLI) are routed to the Main Port as DBCKO, DSDRO, and DSDLO, respectively.

The DIT works with DSCKI for SCK, DBCKI for BCK, internally-created LRCK, DBCKI divided by 64, and 0 data for DIN.

MOLRMTEN (Register 6Ah) can be used to mute/unmute DSDRO from the LRCK port. When MOLRMTEN is set to 1, mute/unmute of DSDRO from LRCK is available by MODMUT = 1/0.

表 7-30 summarizes the DSD input mode configuration. 図 7-24 illustrates the DSD format.

表 7-30. DSD Input Mode Summary

SIGNAL NAME	MPIO GROUP / PIN	DESCRIPTION
DSCKI	MPIO_C0 or MPIO_B0	SCK input ($256f_S$)
DBCKI	MPIO_C1 or MPIO_B1	DBCK input for DSD format ($64f_S$)
DSDRI	MPIO_C2 or MPIO_B2	R-channel DSD data input for DSD format
DSDLI	MPIO_C3 or MPIO_B3	L-channel DSD data input for DSD format
DSCKO	SCKO	SCK output generated by DIR from DIT output
DBCKO	BCK	DBCK output for DSD format (the same signal as DBCKI)
DSDRO	LRCK	R-channel DSD data output for DSD format (the same signal as DSDRI)
DSDLO	DOUT	L-channel DSD data output for DSD format(the same signal as DSDLI)



図 7-24. DSD Format

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7.4.1.1 Typical Register Settings

表 7-31 and 表 7-32 show the typical register settings for DSD format.

表 7-31. DSD Inputs From MPIO_CX Ports

REGISTER SETTINGS	DESCRIPTIONS
34h = CFh	RXSEL = TXOUT
61h = 14h	TXDSD = Enable
6Bh = 14h	MOSSRC = DIR MOPSRC = AUXIN1

表 7-32. DSD Inputs From MPIO_BX Ports

REGISTER SETTINGS	DESCRIPTIONS
34h = CFh	RXSEL = TXOUT
60h = 55h	TXSSRC = AUXIN2 TXPSRC = AUXIN2
61h = 14h	TXDSD = Enable
6Bh = 14h	MOSSRC = DIR MOPSRC = AUXIN1

図 7-25 shows a block diagram of DSD Input Mode (this illustration includes an example of DSD input = MPIO_Cx pins).

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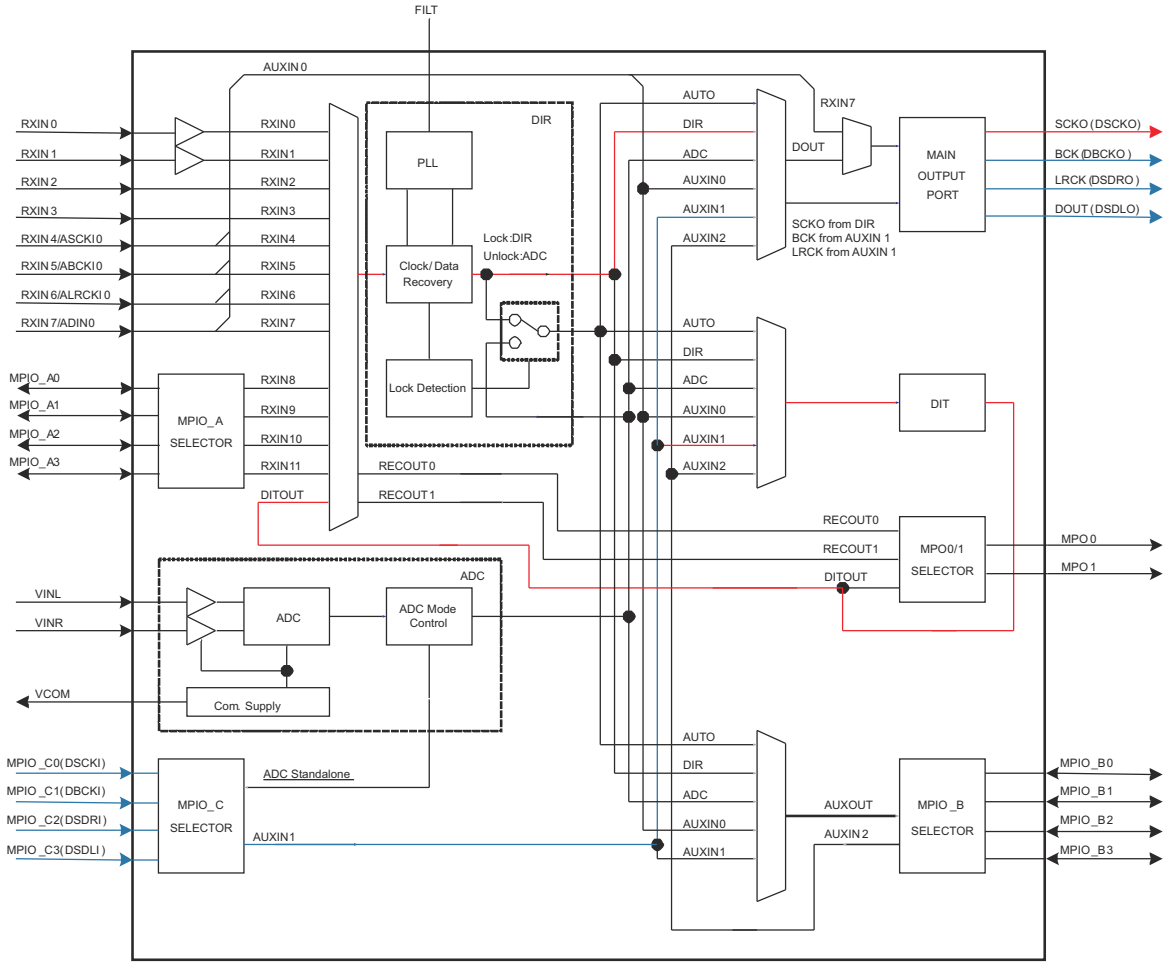

Blue lines are through-paths for DBCKI, DSDRI, and DSDLI. Red lines are DSCKO generation paths.

図 7-25. DSD Input Mode Block Diagram

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7.4.2 Serial Control Mode

The PCM9211 supports two types of control interface, which are set using the MODE pin (pin 27), as defined in 表 7-33.

表 7-33. Mode Control Interface Types

MODE	MODE CONTROL INTERFACE
Tied to DGND	Two-wire (I^2C) serial control
Tied to VDD	Four-wire (SPI) serial control

The input state of the MODE pin is only sampled during a power-on reset or external reset event. Therefore, any change after device power on or external reset is ignored.

表 7-34 shows the pin assignments based on the control interface selected.

表 7-34. Pin Assignments for SPI And I^2C Control Interfaces

PIN	DEFINITION	
	SPI MODE	I^2C MODE
23	MDO	ADR0
24	MDI	SDA
25	MC	SCL
26	MS	ADR1

7.4.3 Four-Wire (SPI) Serial Control

The PCM9211 includes an SPI-compatible serial port, which operates asynchronously to the audio serial interface. The control interface consists of these data sources: MDI/SDA, MS/ADR1, MC/SCL, and MDO/ADR0.

- MDI is the serial data input to program the mode control registers. In other applications, this source may be known as *MOSI*.
- MDO is the serial data output to read back register settings and some flags. In other applications, this source may be known as *MISO*.
- MC is the serial bit clock to shift the data into the control port. In other applications, this clock may be known as *SCK*.
- MS is the select input to enable the mode control port. In other applications, this control may be known as an *active-low Chip Select* ($\overline{CS}$).

7.4.3.1 Control Data Word Format

All single write/read operations via the serial control port use 16-bit data words. 図 7-26 shows the control data word format. The first bit is for read/write control, where 0 indicates a write operation and 1 shows a read operation. The next seven bits, labeled ADR[6:0], set the register address for the write/read operation. The least significant eight bits, D[7:0] on MDI or MDO, contain the data to be written to (or read from) the register specified by ADR[6:0].



図 7-26. Control Data Word Format for MDI

7.4.3.2 Register Write Operation

図 7-27 shows the functional timing diagram for a single write operation on the serial control port. MS is held at 1 until a register must be written. To start the register write cycle, MS should be set to 0. 16 clocks are then provided on MC, corresponding to the 16 bits of the control data word on MDI. After the 16th clock cycle has been completed, MS is set to 1 to latch the data into the indexed mode control register.

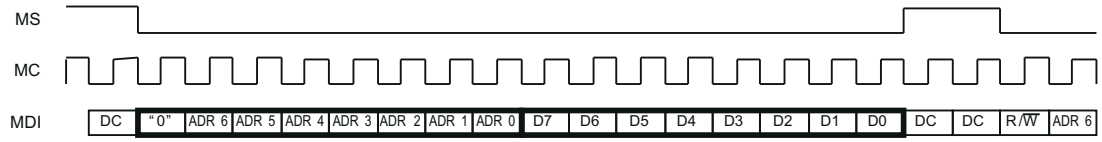

図 7-27. Register Write Operation

Channel status data are available from the Channel Status registers. To read the first 48 bits of the Channel Status registers accurately, the read should be started $48f_S$ after the start of the block. However, once MS is pulled to 0, there are no time requirements in which to read the data because the registers are locked.

Both INT0 and INT1 can also be masked to highlight when the Channel Status has been updated. In many cases, Channel Status does not change during playback (of a movie or music). Once the source changes, though, the Channel Status changes. This change causes an interrupt, which can then be used to trigger the DSP to read the Channel Status registers. The interrupt source is called *OCSRNWx* (Output Channel Status Renewal).

The OCSRNWx flag can be held in the INTx register, or masked and brought out to the ERR/INT0 or NPCM/INT1 pin.

7.4.3.3 Register Read Operation

図 7-28 shows the functional timing diagram for single read operations on the SPI serial control port. MS is held high until a register is to be read. To start the register read cycle, MS is set to a *low* state. 16 clocks are then provided on MC, corresponding to the first eight bits of the control data word on MDI, and second eight bits of the read-back data word from MDO. After the 16th clock cycle has been completed, MS is set to *high* for next write or read operation. MDO remains in a *Hi-Z* (or high impedance) state except for a period of eight MC clocks for actual data transfer.

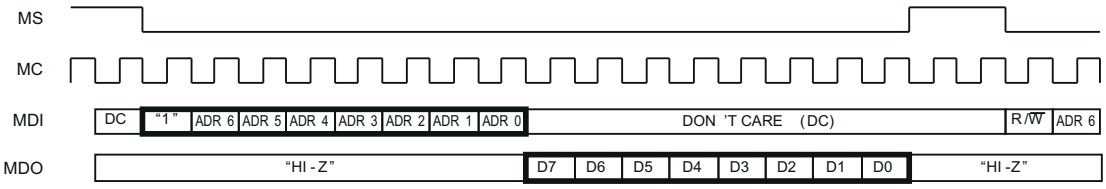

図 7-28. Register Read Operation

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7.4.3.4 Control Interface Timing Requirements

図 7-29 shows a detailed timing diagram for the four-wire serial control interface. These timing parameters are critical for proper control port operation. Timing Requirements lists the timing requirements.

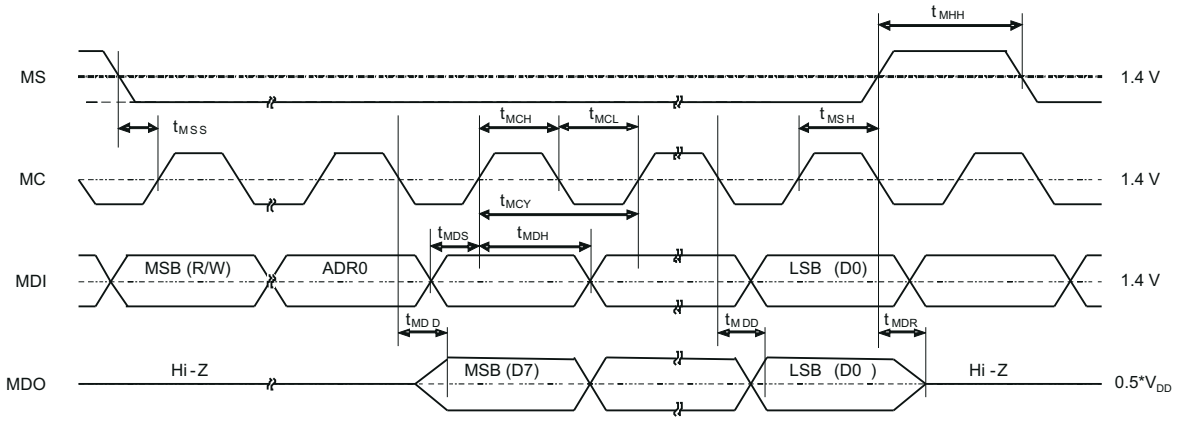

図 7-29. Control Interface Timing Requirements

7.4.4 Two-Wire (I^2C) Serial Control

The PCM9211 also supports the I^2C serial bus and data transmission protocol. It can be configured for fast mode as a slave device.

7.4.4.1 Slave Address

MSB							LSB
1	0	0	0	0	ADR1	ADR0	R/ $\overline{W}$

The PCM9211 has seven bits for its own slave address. The first five bits (MSB) of the slave address are factory-preset to '10000'. The next two bits of the address byte are selectable bits that can be set by MDO/ADR0 and MS/ADR1. A maximum of four PCM9211s can be connected on the same bus at one time. Each PCM9211 responds when it receives its own slave address.

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7.4.4.2 Packet Protocol

A master device must control the packet protocol, which consists of a start condition, slave address with read/write bit, data if a write procedure is desired, or an acknowledgment if read and stop conditions exist. The PCM9211 supports both slave receiver and transmitter functions. Details of the DATA pulse for both write and read operations are described in 図 7-30.

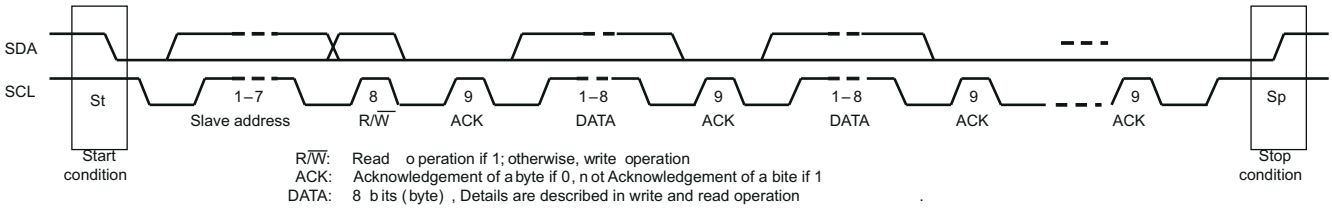

図 7-30. I²C Packet Protocol

7.4.4.3 Write Operation

The PCM9211 can only function as an I²C slave. A master can write to any PCM9211 registers using either single or multiple accesses. The master sends a PCM9211 slave address with a write bit, a register address, and the data. When undefined registers are accessed, the PCM9211 does not send an acknowledgment. 図 7-30 illustrates the write operation. The register address and the write data are 8-bit, MSB-first format.

図 7-30. Framework for Write Operation

Transmitter	*M*	*M*	*M*	*S*	*M*	*S*	*M*	*S*	*M*	*S*		*S*	*M*
Data Type	St	slave address	$\overline{W}$	ACK	reg address	ACK	write data 1	ACK	write data 2	ACK		ACK	Sp

M: Master Device, *S*: Slave Device, St: Start Condition, $\overline{W}$: Write, ACK: Acknowledge, Sp: Stop Condition

7.4.4.4 Read Operation

A master can read the PCM9211 registers. The value of the register address is stored in an indirect index register in advance. The master sends the PCM9211 slave address with a read bit after storing the register address. The PCM9211 then transfers the data to which the index register points. 図 7-31 shows the read operation.

図 7-31. Framework for Read Operation

Transmitter	*M*	*M*	*M*	*S*	*M*	*S*	*M*	*M*	*M*	*S*	*S*	*M*	*M*
Data Type	St	slave address	$\overline{W}$	ACK	reg address	ACK	Sr	slave address	R	ACK	read data	NACK	Sp

M: Master Device, *S*: Slave Device, St: Start Condition, Sr: Repeated Start Condition, $\overline{W}$: Write, R: Read,
ACK: Acknowledge, NACK: Not Acknowledge, Sp: Stop Condition

The slave address after the repeated start condition must be the same as the previous slave address.

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7.4.4.5 Timing Diagram

図 7-33 shows the detailed timing diagram for SCL and SDA. Timing Requirements lists the timing requirements.

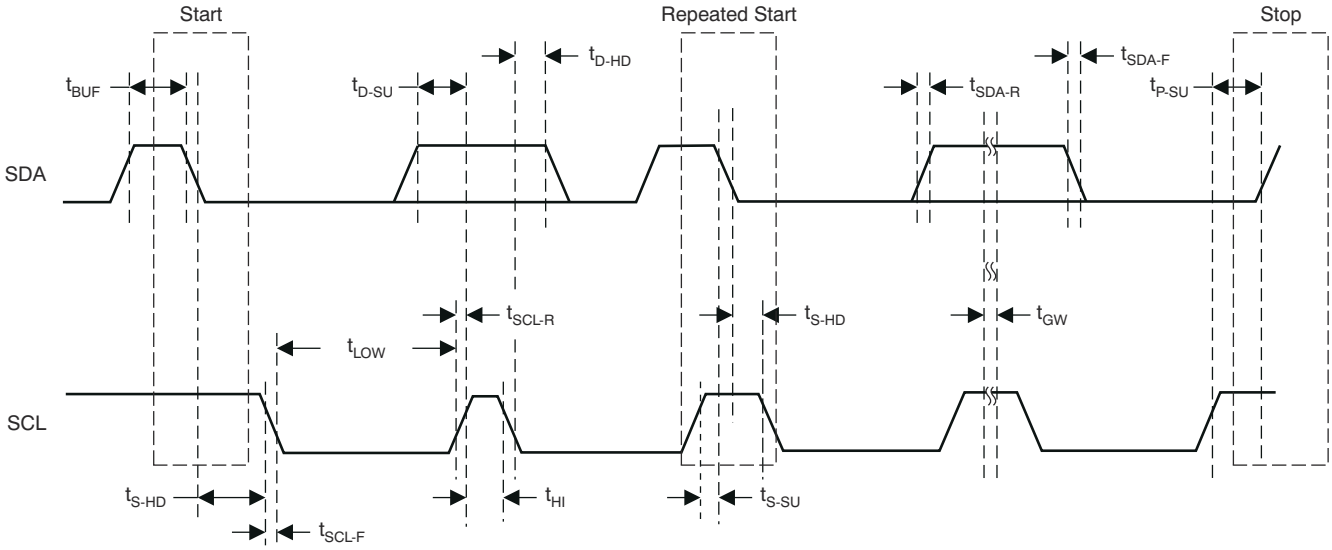

図 7-33. Control Interface Timing

7.5 Register Maps

表 7-35 shows the PCM9211 register map that lists all the registers available in this device.

表 7-35. Register Map

ADR	REGISTER DESCRIPTION	R/W	B7	B6	B5	B4	B3	B2	B1	B0
20h	ERROR Output Condition and Shared Port Settings	R/W	RSV	ERRCON	MCHR	RSV	ERRHZ	ERRSEL	NPCMHZ	NPCMSEL
21h	DIR Initial Settings 1/3	R/W	RSV	RSV	RSV	RXFSRNG	RSV	RSV	RSV	RSV
22h	DIR Initial Settings 2/3	R/W	RSV	CLKSTCON	RSV	CLKSTP	RSV	RSV	RSV	RXVDLY
23h	DIR Initial Settings 3/3	R/W	RSV	RSV	XTIWT1	XTIWT0	PRTPRO1	PRTPRO0	ERRWT1	ERRWT0
24h	Oscillation Circuit Control	R/W	OSCAUTO	RSV	RSV	XMCKEN	XMCKDIV1	XMCKDIV0	RSV	RSV
25h	ERROR Cause Setting	R/W	RSV	RSV	EFSCHG	EFSLMT	ENPCM	EVALID	EPARITY	EUNLOCK
26h	AUTO Source Selector Cause Setting	R/W	ACKSL	AERROR	RSV	AFSLMT	ANPCM	AVALID	RSV	AUNLOCK
27h	DIR Acceptable f_S Range Setting and Mask	R/W	MSK128	MSK64	RSV	NOMLMT	HILMT1	HILMT0	LOLMT1	LOLMT0
28h	Non-PCM Definition Setting	R/W	RSV	RSV	CS1BPLS	NPCMP	RSV	DTSCD	PAPB	CSBIT1
29h	DTS CD/LD Detection Setting	R/W	RSV	RSV	RSV	RSV	DTS16	DTS14	DTSPRD1	DTSPRD0
2Ah	INT0 Output Cause Mask Setting	R/W	MERROR0	MNPCM0	MEMPHF0	MDTSCD0	MCSRNW0	MPCRNW0	MFSCHG0	RSV
2Bh	INT1 Output Cause Mask Setting	R/W	MERROR1	MNPCM1	MEMPHF1	MDTSCD1	MCSRNW1	MPCRNW1	MFSCHG1	MADLVL1
2Ch	INT0 Output Register	R	OERROR0	ONPCM0	OEMPHF0	ODTSCD0	OCSRNW0	OPCRNW0	OFSCHG0	RSV
2Dh	INT1 Output Register	R	OERROR1	ONPCM1	OEMPHF1	ODTSCD1	OCSRNW1	OPCRNW1	OFSCHG1	OADLVL1
2Eh	INT0, INT1 Output Polarity Setting	R/W	RSV	INT1P	RSV	ADLVLTH1	ADLVLTH0	INT0P	RSV	RSV
2Fh	DIR Output Data Format	R/W	RSV	RSV	RSV	RSV	RSV	RXFMT2	RXFMT1	RXFMT0
30h	DIR Recovered System Clock Ratio Setting	R/W	RSV	RSV	RSV	PSCKAUTO	RSV	PSCK2	PSCK1	PSCK0
31h	XTI Source Clock Frequency Setting	R/W	RSV	RSV	XSCK1	XSCK0	XBCK1	XBCK0	XLRCK1	XLRCK0
32h	DIR Source, Sec. Bit/LR Clock Frequency Setting	R/W	RSV	PSBCK2	PSBCK1	PSBCK0	RSV	PSLRCK2	PSLRCK1	PSLRCK0
33h	XTI Source, Sec. Bit/LR Clock Frequency Setting	R/W	RSV	XSBCK2	XSBCK1	XSBCK0	RSV	XSLRCK2	XSLRCK1	XSLRCK0
34h	DIR Input Biphase Source Select, Coax Amp. Control	R/W	RX0DIS	RX1DIS	RSV	RSV	RXSEL3	RXSEL2	RXSEL1	RXSEL0
35h	RECOUT0 Output Biphase Source Select	R/W	RSV	RSV	RSV	MPO0MUT	RO0SEL3	RO0SEL2	RO0SEL1	RO0SEL0
36h	RECOUT1 Output Biphase Source Select	R/W	RSV	RSV	RSV	MPO1MUT	RO1SEL3	RO1SEL2	RO1SEL1	RO1SEL0
37h	Port f_S Calculator Measurement Target Setting	R/W	RSV	RSV	RSV	RSV	RSV	PFSTGT2	PFSTGT1	PFSTGT0
38h	Port f_S Calculator Result Output	R	PFSST	PFSPO2	PFSPO1	PFSPO0	PFSOUT3	PFSOUT2	PFSOUT1	PFSOUT0
39h	Incoming Biphase Information and Calculated f_S Output	R	SFSST	SCSBIT1	RSV	RSV	SFSOUT3	SFSOUT2	SFSOUT1	SFSOUT0
3Ah	P_C Buffer Byte0 (Burst Preamble P_C Output Register)	R	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
3Bh	P_C Buffer Byte1 (Burst Preamble P_C Output Register)	R	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
3Ch	P_D Buffer Byte0 (Burst Preamble PD Output Register)	R	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
3Dh	P_D Buffer Byte1 (Burst Preamble P_D Output Register)	R	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8
40h	System Reset Control	R/W	MRST	SRST	ADDIS	RXDIS	RSV	RSV	TXDIS	XODIS
42h	ADC Function Control 1/3	R/W	RSV	RSV	ADCKOUT	ADDTRX7	ADFSLMT	ADCLK2	ADCLK1	ADCLK0
46h	ADC L-ch, digital ATT control	R/W	ADATTL7	ADATTL6	ADATTL5	ADATTL4	ADATTL3	ADATTL2	ADATTL1	ADATTL0
47h	ADC R-ch, digital ATT control	R/W	ADATTR7	ADATTR6	ADATTR5	ADATTR4	ADATTR3	ADATTR2	ADATTR1	ADATTR0
48h	ADC Function Control 2/3	R/W	RSV	ADIFMD2	ADIFMD1	ADIFMD0	RSV	RSV	ADFMT1	ADFMT0
49h	ADC Function Control 3/3	R/W	RSV	RSV	RSV	ADZCDD	ADBYP	ADPHSE	ADMUTR	ADMUTL
5Ah	DIR Channel Status Data Buffer 1/6	R	RXCS7	RXCS6	RXCS5	RXCS4	RXCS3	RXCS2	RXCS1	RXCS0
5Bh	DIR Channel Status Data Buffer 2/6	R	RXCS15	RXCS14	RXCS13	RXCS12	RXCS11	RXCS10	RXCS9	RXCS8
5Ch	DIR Channel Status Data Buffer 3/6	R	RXCS23	RXCS22	RXCS21	RXCS20	RXCS19	RXCS18	RXCS17	RXCS16
5Dh	DIR Channel Status Data Buffer 4/6	R	RXCS31	RXCS30	RXCS29	RXCS28	EXCS27	RXCS26	RXCS25	RXCS24
5Eh	DIR Channel Status Data Buffer 5/6	R	RXCS39	RXCS38	RXCS37	RXCS36	RXCS35	RXCS34	RXCS33	RXCS32
5Fh	DIR Channel Status Data Buffer 6/6	R	RXCS47	RXCS46	RXCS45	RXCS44	RXCS43	RXCS42	RXCS41	RXCS40
60h	DIT Function Control 1/3	R/W	RSV	TXSSRC2	TXSSRC1	TXSSRC0	RSV	TXPSRC2	TXPSRC1	TXPSRC0
61h	DIT Function Control 2/3	R/W	RSV	TXSCK2	TXSCK1	TXSCK0	RSV	RSV	TXFMT1	TXFMT0
62h	DIT Function Control 3/3	R/W	RSV	RSV	TXDMUT	RSV	TXVFLG	RSV	RSV	RSV
63h	DIT Channel Status Data Buffer 1/6	R/W	TXCS7	TXCS6	TXCS5	TXCS4	TXCS3	TXCS2	TXCS1	TXCS0
64h	DIT Channel Status Data Buffer 2/6	R/W	TXCS15	TXCS14	TXCS13	TXCS12	TXCS11	TXCS10	TXCS9	TXCS8
65h	DIT Channel Status Data Buffer 3/6	R/W	TXCS23	TXCS22	TXCS21	TXCS20	TXCS19	TXCS18	TXCS17	TXCS16
66h	DIT Channel Status Data Buffer 4/6	R/W	TXCS31	TXCS30	TXCS29	TXCS28	TXCS27	TXCS26	TXCS25	TXCS24
67h	DIT Channel Status Data Buffer 5/6	R/W	TXCS39	TXCS38	TXCS37	TXCS36	TXCS35	TXCS34	TXCS33	TXCS32

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表 7-35. Register Map (continued)

ADR	REGISTER DESCRIPTION	R/W	B7	B6	B5	B4	B3	B2	B1	B0
68h	DIT Channel Status Data Buffer 6/6	R/W	TXCS47	TXCS46	TXCS45	TXCS44	TXCS43	TXCS42	TXCS41	TXCS40
6Ah	Main Output and AUXOUT Port Data Mute Control	R/W	AOMUTAS	MOMUTAS	RSV	RSV	AOLRMTEN	AODMUT	MOLRMTEN	MODMUT
6Bh	Main Output Port, Output Source Setting	R/W	RSV	MOSSRC2	MOSSRC1	MOSSRC0	RSV	MOPSRC2	MOPSRC1	MOPSRC0
6Ch	AUX Output Port, Output Source Setting	R/W	RSV	AOSSRC2	AOSSRC1	AOSSRC0	RSV	AOPSRC2	AOPSRC1	AOPSRC0
6Dh	MPIO_B & Main Output Port Hi-Z Control	R/W	MPB3HZ	MPB2HZ	MPB1HZ	MPB0HZ	SCKOHZ	BCKHZ	LRCKHZ	DOUTHZ
6Eh	MPIO_C and MPIO_A Hi-Z Control	R/W	MPC3HZ	MPC2HZ	MPC1HZ	MPC0HZ	MPA3HZ	MPA2HZ	MPA1HZ	MPA0HZ
6Fh	MPIO_A, MPIO_B, MPIO_C Group Function Assign	R/W	MPASEL1	MPASEL0	MPBSEL2	MPBSEL1	MPBSEL0	MPCSEL2	MPCSEL1	MPCSEL0
70h	MPIO_A, Flags/GPIO Assign Setting	R/W	RSV	RSV	MCHSRC1	MCHSRC0	MPA3SEL	MPA2SEL	MPA1SEL	MPA0SEL
71h	MPIO_B, MPIO_C, Flags/GPIO Assign Setting	R/W	MPB3SEL	MPB2SEL	MPB1SEL	MPB0SEL	MPC3SEL	MPC2SEL	MPC1SEL	MPC0SEL
72h	MPIO_A1, MPIO_A0 Output Flag Select	R/W	MPA1FLG3	MPA1FLG2	MPA1FLG1	MPA1FLG0	MPA0FLG3	MPA0FLG2	MPA0FLG1	MPA0FLG0
73h	MPIO_A3, MPIO_A2 Output Flag Select	R/W	MPA3FLG3	MPA3FLG2	MPA3FLG1	MPA3FLG0	MPA2FLG3	MPA2FLG2	MPA2FLG1	MPA2FLG0
74h	MPIO_B1, MPIO_B0 Output Flag Select	R/W	MPB1FLG3	MPB1FLG2	MPB1FLG1	MPB1FLG0	MPB0FLG3	MPB0FLG2	MPB0FLG1	MPB0FLG0
75h	MPIO_B3, MPIO_B2 Output Flag Select	R/W	MPB3FLG3	MPB3FLG2	MPB3FLG1	MPB3FLG0	MPB2FLG3	MPB2FLG2	MPB2FLG1	MPB2FLG0
76h	MPIO_C1, MPIO_C0 Output Flag Select	R/W	MPC1FLG3	MPC1FLG2	MPC1FLG1	MPC1FLG0	MPC0FLG3	MPC0FLG2	MPC0FLG1	MPC0FLG0
77h	MPIO_C3, MPIO_C2 Output Flag Select	R/W	MPC3FLG3	MPC3FLG2	MPC3FLG1	MPC3FLG0	MPC2FLG3	MPC2FLG2	MPC2FLG1	MPB2FLG0
78h	MPO1, MPO0 Function Assign Setting	R/W	MPO1SEL3	MPO1SEL2	MPO1SEL1	MPO1SEL0	MPO0SEL3	MPO0SEL2	MPO0SEL1	MPO0SEL0
79h	GPIO I/O Direction control for MPIO_A, MPIO_B	R/W	GIOB3DIR	GIOB2DIR	GIOB1DIR	GIOB0DIR	GIOA3DIR	GIOA2DIR	GIOA1DIR	GIOA0DIR
7Ah	GPIO I/O Direction control for MPIO_C	R/W	RSV	RSV	RSV	RSV	GIOC3DIR	GIOC2DIR	GIOC1DIR	GIOC0DIR
7Bh	GPIO Output Data Setting for MPIO_A, MPIO_B	R/W	GPOB3	GPOB2	GPOB1	GPOB0	GPOA3	GPOA2	GPOA1	GPOA0
7Ch	GPIO Output Data Setting for MPIO_C	R/W	RSV	RSV	RSV	RSV	GPOC3	GPOC2	GPOC1	GPOC0
7Dh	GPIO Input Data Register for MPIO_A, MPIO_B	R	GPIB3	GPIB2	GPIB1	GPIB0	GPIA3	GPIA2	GPIA1	GPIA0
7Eh	GPIO Input Data Register for MPIO_C	R	RSV	RSV	RSV	RSV	GPIC3	GPIC2	GPIC1	GPIC0

Note

Blank spaces are provided to aid in development. Record your register settings for future reference.

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7.5.1 Error Output Condition and Shared Port Settings Register (address = 20h) [reset = 00000000]

図 7-33. Error Output Condition and Shared Port Settings Register

7	6	5	4	3	2	1	0
RSV	ERRCON	MCHR	RSV	ERRHZ	ERRSEL	NPCMHZ	NPCMSEL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

ERRCON: ERROR Output Condition Setting

0: ERROR pin output is always DIR status (default)

1: ERROR output depends on source control MOPSRC[2:0]

DIR/AUTO: Output DIR status

Except DIR: ERROR outputs *high* (error status).

MCHR: MPIO/Multi-Channel PCM Routing Select

0: All MPIOs are controlled by MPASEL[1:0], MPBSEL[1:0], MPCSEL[2:0] (Default)

1: All MPIOs are assigned for Multichannel PCM Routing I/O.

ERRHZ: ERROR/INT0 Port Output Hi-Z Control

0: Output (default)

1: Hi-Z

ERRSEL: ERROR/INT0 Port Output Source Select

0: ERROR (default)

1: INT0

NOTE: ERRSEL must be 0 when Register 26h/AERROR = 1 or Register 42h/ADFSLMT = 1, or if the signal CLKST is used.

NPCMHZ: NPCM/INT1 Port Output Hi-Z Control

0: Output (default)

1: Hi-Z

NPCMSEL: NPCM/INT1 Port Output Source Select

0: NPCM (default)

1: INT1

7.5.2 DIR Initial Settings Register 1/3 (address: 21h) [reset = 00000000]

図 7-34. DIR Initial Settings Register 1/3

7	6	5	4	3	2	1	0
RSV	RSV	RSV	RXFSRNG	RSV	RSV	RSV	RSV
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

RXFSRNG: DIR Receivable Incoming Biphase Sampling Frequency Range Setting

0: Wide mode (7 kHz to 216 kHz) (default)

1: Normal mode (28 kHz to 108 kHz)

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7.5.3 DIR Initial Settings Register 2/3 (address: 22h) [reset = 00000001]

図 7-35. DIR Initial Settings Register 2/3

7	6	5	4	3	2	1	0
RSV	CLKSTCON	RSV	CLKSTP	RSV	RSV	RSV	RXVDLY
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

CLKSTCON: CLKST Output Condition Setting

0: Only PLL Lock status change (default)

1: All events where the Main port output clock condition changes, as well as these cases:

1. MOSSRC/MOPSRC register is updated to ADC, AUXIN0, AUXIN1, or AUXIN2
2. DIR and ADC are switched by DIR status when MOSSRC = 000(AUTO) and MOPSRC = 000(AUTO)
3. Main port sampling frequency changes when PFSTGT = 101(Main output port)

NOTES:

CLKST never outputs when updating MOSSRC and MOPSRC to AUTO or DIR.

OSCAUTO must be 0 when CLKST is used because CLKST is generated by frequency counting of built-in oscillator circuit.

To output CLKST, MOSSRC and MOPSRC are set simultaneously.

CLKSTP: CLKST Polarity Setting

0: Active low (default)

1: Active high

RXVDLY: VOUT Delay Setting

0: VOUT is active immediately after validity flag is detected

1: VOUT is active after synchronization with DOUT data (default)

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7.5.4 DIR Initial Settings Register 3/3 (address: 23h) [reset = 00000100]

図 7-36. DIR Initial Settings Register 3/3

7	6	5	4	3	2	1	0
RSV	RSV	XTIWT1	XTIWT0	PRTPRO1	PRTPRO0	ERRWT1	ERRWT0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

XTIWT[1:0]: Crystal OSC, Oscillation Start-up Wait Time Setting

00: 25 ms

01: 50 ms

10: 100 ms

11: 200 ms

XTIWT is counted by the PLL generated clock.

These are the resulting values when the PLL is running with a free-run clock because of no S/PDIF input.

After these delay times, the Main Port source changes from DIR to ADC when DIR is unlocked.

PRTPRO[1:0]: Process for Parity Error Detection

00: No process

01: For PCM data only, an 8x continuous parity error is replaced by previous data and muted after ninth parity error at EPARITY = 1 (default)

10: For PCM and non-PCM data, an 8x continuous parity error is replaced by previous data and muted after ninth parity error at EPARITY = 1

11: Reserved (The definition of *Non-PCM* depends on the Non-PCM Definition Setting Register)

Validity flag, user bit, channel status, Non-PCM and DTS-CD detection should be refreshed by waiting more than $192/f_S$ without any parity error.

ERRWT[1:0]: ERROR Release Wait Time Setting

00: ERROR Release after 48 counts of preamble *B* (Default), 192 ms at f_S = 48 kHz

01: ERROR Release after 12 counts of preamble *B*

10: ERROR Release after six counts of preamble *B*

11: ERROR Release after three counts of preamble *B*

These counts are only available when DIR is unlocked or DIR sampling frequency is changed or exceeds limits defined by DIR Acceptable f_S Range Setting and Mask registers.

CLKST also uses ERRWT to release.

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7.5.5 Oscillation Circuit Control Register (address: 24h) [reset = 00000000]

図 7-37. Oscillation Circuit Control Register

7	6	5	4	3	2	1	0
OSCAUTO	RSV	RSV	XMCKEN	XMCKDIV1	XMCKDIV0	RSV	RSV
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

OSCAUTO: Oscillation Circuit Automatic Operation Control

0: Built-in oscillator circuit always operates (default)

1: Built-in oscillator circuit is stopped during lock state of DIR but is active when DIR locks and CLKST is active

NOTES:

The XODIS command has more priority than this OSCAUTO register.

If XODIS is set to power down, the XTI source is not output.

XMCKENX: MCKO (XTI Clock Buffered Output) Output Enable Control

0: MUTE (Logic low level) (default)

1: Output

XMCKDIV[1:0]: XMCKO (XTI Clock Buffered Output) Output Clock Dividing Ratio

00: XTI/1 (24.576 MHz) (default)

01: XTI/2 (12.288 MHz)

10: XTI/4 (6.144 MHz)

11: XTI/8 (3.072 MHz)

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7.5.6 Error Cause Setting Register (address = 25h) [reset = 00000001]

The following ERROR Cause Setting registers are independent of the AUTO Source Selector Cause Setting register (26h).

図 7-38. Error Cause Setting Register

7	6	5	4	3	2	1	0
RSV	RSV	EFSCHG	EFSLMT	ENPCM	EVALID	EPARITY	EUNLOCK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

EFSCHG: DIR Sampling Frequency Change

0: Not selected (default)

1: Selected

EFSLMT: DIR Limiting Acceptable Sampling Frequency

0: Not selected (default)

1: Selected

The definition of receivable sampling frequency range depends on the f_S Limit Setting Register.

ENPCM: Non-PCM

0: Not selected (default)

1: Selected

The definition of *non-PCM* depends on the Non-PCM Definition Setting Register.

EVALID: Validity Flag

0: Not selected (default)

1: Selected

EPARITY: Parity Error

0: Not selected (default)

1: Selected

EUNLOCK: PLL Lock Error

0: Not selected

1: Selected (default)

This register is used for setting the ERROR output factor.

The required factors of ERROR set to 1 are selected based on *OR* logic.

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7.5.7 AUTO Source Selector Cause Setting Register (address = 26h) [reset = 00000001]

図 7-39. AUTO Source Selector Cause Setting Register

7	6	5	4	3	2	1	0
ACKSL	AERROR	RSV	AFSLMT	ANPCM	AVALID	RSV	AUNLOCK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

The AUTO source selector is an automatic selector that outputs DIR or ADC output based on the following register settings. The following AUTO Source Selector Cause Setting registers are independent of the ERROR Cause Setting register (25h).

ACKSL: ADC Output Clock Select

0: ADC clock selected by the ADCLK[2:0] register (42h) (default)

1: XTI clock

AERROR: ERROR

0: Not selected (default)

1: Selected

ERROR condition is defined by the ERROR Cause Setting register (25h).

AFSLMT: Limiting Acceptable Sampling Frequency

0: Not selected (default)

1: Selected

The definition of receivable sampling frequency range depends on the f_S Limit Setting register.

ANPCM: Non-PCM

0: Not selected (default)

1: Selected

The definition of *non-PCM* depends on the Non-PCM Definition Setting register.

AVALID: Validity Flag

0: Not selected (default)

1: Selected

AUNLOCK: PLL Lock Error

0: Not selected

1: Selected (default)

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7.5.8 DIR Acceptable f_S Range Setting and Mask Register (address: 27h) [reset = 00000000]

図 7-40. DIR Acceptable f_S Range Setting and Mask Register

7	6	5	4	3	2	1	0
MSK128	MSK64	RSV	NOMLMT	HILMT1	HILMT0	LOLMT1	LOLMT0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

MSK128: Mask for f_S = 128 kHz

0: No mask (default)

1: Mask

PCM9211 does not receive 128-kHz sampling frequency.
This register setting is effective with NOMLMT = 1.

MSK64: Mask for f_S = 64 kHz

0: No mask (default)

1: Mask

PCM9211 does not receive 64-kHz sampling frequency.
This register setting is effective with NOMLMT = 1.

NOMLMT: Receive Nominal Audio f_S within ±2%

0: No limit (default)

1: Limit

PCM9211 receives the nominal audio sampling frequencies within ±2%.
The nominal audio sampling frequencies are: 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz, 64 kHz, 88.2 kHz, 96 kHz, 128 kHz, 176.4 kHz, 192 kHz

HILMT[1:0]: Acceptable f_S Higher Limit Setting

00: No limit (default)

01: f_S = 54 kHz

10: f_S = 108 kHz

11: f_S = 216 kHz

LOLMT[1:0]: Acceptable f_S Lower Limit Setting

00: No limit (default)

01: f_S = 7 kHz

10: f_S = 14 kHz

11: f_S = 28 kHz

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7.5.9 Non-PCM Definition Register (address = 28h) [reset = 00000011]

図 7-41. Non-PCM Definition Register

7	6	5	4	3	2	1	0
RSV	RSV	CS1BPLS	NPCMP	RSV	DTSCD	PAPB	CSBIT1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

CS1BPLS: CSBIT1 Detection Signal Select

0: Hold value (default)

1: Pulse

NPCMP: NPCM Pin Output Polarity

0: Active high (default)

1: Active low

DTSCD: DTS CD/LD Detection

0: Unselected (default)

1: Selected

PAPB: Burst Preamble P_A and P_B Detection

0: Unselected

1: Selected (default)

CSBIT1: Channel Status Bit1 = 1 Detection

0: Unselected

1: Selected (default)

This register is used to set the definition of non-PCM data. The NPCM pin output and NPCM register flag output follow this definition.

There are three types of non-PCM factors to be selected, based on *OR* logic.

Note

The DTSCD register (29h) must be 1 (that is, selected) in order to output the DTSCD flag from the MPIO, MPO, and INT pins as DIR Flag outputs.

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7.5.10 DTS-CD/LD Sync Word and Period Detection Setting Register (address: 29h) [reset = 00001100]

図 7-42. DTS-CD/LD Sync Word and Period Detection Setting Register

7	6	5	4	3	2	1	0
RSV	RSV	RSV	RSV	DTS16	DTS14	DTSPRD1	DTSPRD0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

DTS16: DTS-CD/LD 16-bit Sync Word Detection

0: Unselected

1: Selected (default)

DTS14: DTS-CD/LD 14-bit Sync Word Detection

0: Unselected

1: Selected (default)

DTSPRD[1:0]: DTS-CD/LD Sync Word Detection Period

00: No period, detect one sync word (default)

01: One period

10: Two periods

11: Four periods

Note

The DTSCD register (register 28h) must be 1 (that is, selected) in order to output the DTSCD flag from the MPIO, MPO, and INT pins as DIR Flag outputs.

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7.5.11 INT0 Output Cause Mask Setting Register (Address: 2Ah) [reset = 11111111]

図 7-43. INT0 Output Cause Mask Setting Register

7	6	5	4	3	2	1	0
MERROR0	MNPCM0	MEMPHF0	MDTSCD0	MCSRNW0	MPCRNW0	MFSCHG0	RSV
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

MERROR0: ERROR Port Output Status

0: Not masked

1: Masked (default)

MNPCM0: NPCM Port Output Status

0: Not masked

1: Masked (default)

This register setting follows the register setting of non-PCM data identification.

MEMPHF0: Emphasis Flag in Channel Status

0: Not masked

1: Masked (default)

MDTSCD0: DTS-CD/LD Sync Detection

0: Not masked

1: Masked (default)

This detection condition depends on the register setting for DTS-CD/LD detection conditions.

MCSRNW0: Channel Status Data of Beginning 48-bit Renewal

0: Not masked

1: Masked (default)

MPCRNW0: Burst Preamble P_C Renewal

0: Not masked

1: Masked (default)

MFSCHG0: Renewal Flag of f_S Calculator Result

0: Not masked

1: Masked (default)

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7.5.12 INT1 Output Cause Mask Setting Register (Address: 2Bh) [reset = 11111111]

図 7-44. INT1 Output Cause Mask Setting Register

7	6	5	4	3	2	1	0
MERROR1	MNPCM1	MEMPHF1	MDTSCD1	MCSRNW1	MPCRNW1	MFSCHG1	MADLVL1
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

MERROR1: ERROR Port Output Status

0: Not masked

1: Masked (default)

MNPCM1: NPCM Port Output Status

0: Not masked

1: Masked (default)

This register setting follows the register setting of non-PCM data identification.

MEMPHF1: Emphasis Flag in Channel Status

0: Not masked

1: Masked (default)

MDTSCD1: DTS-CD/LD Sync Detection

0: Not masked

1: Masked (default)

This detection condition depends on the register setting for DTS-CD/LD detection conditions.

MCSRNW1: Channel Status Data of Beginning 48-bit Renewal

0: Not masked

1: Masked (default)

MPCRNW1: Burst Preamble P_C Renewal

0: Not masked

1: Masked (default)

MFSCHG1: Renewal Flag of f_S Calculator Result

0: Not masked

1: Masked (default)

MADLVL1: ADC Input Level Detection Status

0: Not masked

1: Masked (default)

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7.5.13 INT0 Output Register (address = 2Ch) [reset = N/A]

図 7-45. INT0 Output Register

7	6	5	4	3	2	1	0
OERROR0	ONPCM0	OEMPHF0	ODTSCD0	OCSRNW0	OPCRNW0	OFSCHG0	RSV
R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

OERROR0: ERROR Port Output Status

0: No ERROR

1: Detect ERROR

This register setting follows the register setting of the ERROR factor.

ONPCM0: NPCM Port Output Status

0: PCM data

1: Non-PCM data

This register setting follows the register setting of non-PCM data identification.

OEMPHF0: Emphasis Flag in Channel Status

0: No emphasis

1: Emphasis

ODTSCD0: DTS-CD/LD Detection

0: No DTS-CD/LD

1: DTS-CD/LD

This register setting follows the register setting for DTS-CD/LD detection conditions.

OCSRNW0: Channel Status Data of Beginning 48-bit Renewal

0: Not detect renewal

1: Detect renewal

OPCRNW0: Burst Preamble P_C Renewal

0: Not detect renewal

1: Detect renewal

OFSCHG0: Renewal Flag of f_S Calculator Result

0: Not detect renewal

1: Detect renewal

When this register is read, the INT0 output is cleared.

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7.5.14 INT1 Output Register (address = 2Dh) [reset = N/A]

図 7-46. INT1 Output Register

7	6	5	4	3	2	1	0
OERROR1	ONPCM1	OEMPHF1	ODTSCD1	OCSRNW1	OPCRNW1	OFSCHG1	OADLVL1
R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

OERROR1: ERROR Port Output Status

0: No ERROR

1: Detect ERROR

This register setting follows the register setting of the ERROR factor.

ONPCM1: NPCM Port Output Status

0: PCM data

1: Non-PCM data

This register setting follows the register setting of non-PCM data identification.

OEMPHF1: Emphasis Flag in Channel Status

0: No emphasis

1: Emphasis

ODTSCD1: DTS-CD/LD Detection

0: No DTS-CD/LD

1: DTS-CD/LD

This register setting follows the register setting for DTS-CD/LD detection conditions.

OCSRNW1: Channel Status Data of Beginning 48-bit Renewal

0: Not detect renewal

1: Detect renewal

OPCRNW1:Burst Preamble P_C Renewal

0: Not detect renewal

1: Detect renewal

OFSCHG1: Renewal Flag of f_S Calculator Result

0: Not detect renewal

1: Detect renewal

OADLVL1: ADC Input Level Detection Status

0: Not detect the defined threshold input level

1: Detect the defined threshold input level

NOTE: The threshold input level is defined by Register 2Eh, ADLVLTH[1:0].

When this register is read, the INT1 output is cleared.

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7.5.15 INT0, INT1 Output Polarity Setting Register (address = 2Eh) [reset = 00000000]

図 7-47. INT0, INT1 Output Polarity Setting Register

7	6	5	4	3	2	1	0
RSV	INT1P	RSV	ADLVLTH1	ADLVLTH0	INT0P	RSV	RSV
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

INT1P: INT1 Port, Polarity Setting

0: Negative logic (default)

1: Positive logic

ADLVLTH[1:0]: ADC Input Level Detection Threshold for INT1

00: –12dB

01: –24dB

10: –36dB

11: –48dB

INT0P: INT0 Port, Polarity Setting

0: Negative logic (default)

1: Positive logic

When the INT0 or INT1 Information Register is read, Register INT0 or INT1 port output is cleared.

7.5.16 DIR Output Data Format Register (address = 2Fh) [reset = 00000100]

図 7-48. DIR Output Data Format Register

7	6	5	4	3	2	1	0
RSV	RSV	RSV	RSV	RSV	RXFMT2	RXFMT1	RXFMT0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

RXFMT[2:0]: DIR Output Data Format Setting

000: 24-bit MSB first, right-justified

001: Reserved

010: Reserved

011: 16-bit MSB first, right-justified

100: 24-bit MSB first, I^2S (default)

101: 24-bit MSB first, left-justified

110: Reserved

111: Reserved

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7.5.17 DIR Recovered System Clock (SCK) Ratio Setting Register (address = 30h) [reset = 00000010]

図 7-49. DIR Recovered System Clock (SCK) Ratio Setting Register

7	6	5	4	3	2	1	0
RSV	RSV	RSV	PSCKAUTO	RSV	PSCK2	PSCK1	PSCK0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

PSCKAUTO: PLL SCK Dividing Ratio Automatic Control Setting

0: Disable (default)

1: Enable

This register is used to set the PLL SCK dividing ratio automatic control function.
SCK setting is automatically set depending on the input sampling frequency.

$512f_S$: 54 kHz and below

$256f_S$: 54 kHz to 108 kHz

$128f_S$: 108 kHz and above or unlocked

The register setting of PSCKAUTO is prioritized higher than the PSCK[2:0] register setting.
For instance, if PSCKAUTO = 1, the PSCK[2:0] register setting is ignored.
To use this function, the XTI clock source is required.

PSCK[2:0]: DIR Recovered Clock Frequency Setting

000: $128f_S$

001: Reserved

010: $256f_S$ (default)

011: Reserved

100: $512f_S$

101: Reserved

110: Reserved

111: Reserved

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7.5.18 XTI Source, Clock (SCK, BCK, LRCK) Frequency Setting Register (address = 31h) [reset = 00011010]

図 7-50. XTI Source, Clock (SCK, BCK, LRCK) Frequency Setting Register

7	6	5	4	3	2	1	0
RSV	RSV	XSCK1	XSCK0	XBCK1	XBCK0	XLRCK1	XLRCK0
R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-0h	R/W-1h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

XSCK[1:0]: XTI Clock Source Frequency Setting

00: XTI/1 (24.576 MHz)
01: XTI/2 (12.288 MHz) (default)
10: XTI/4 (6.144 MHz)
11: XTI/8 (3.072 MHz)

XBCK[1:0]: XTI Clock Source BCK Frequency Setting

00: XTI/2 (12.288 MHz)
01: XTI/4 (6.144 MHz)
10: XTI/8 (3.072 MHz) (default)
11: XTI/16 (1.536 MHz)

XLRCK[1:0]: XTI Clock Source LRCK Frequency Setting

00: XTI/128 (192 kHz)
01: XTI/256 (96 kHz)
10: XTI/512 (48 kHz) (default)
11: XTI/1024 (24 kHz)

Note

The XTI clock source frequency is allowed to be set over the maximum limit of the ADC allowable clock frequency. However, setting the XTI clock source frequency at such a level is not recommended and may cause the device to exceed its stated operating and performance limits.

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7.5.19 DIR Source, Secondary Bit/LR Clock (SBCK/SLRCK) Frequency Setting Register (address = 32h) [reset = 00100010]

図 7-51. DIR Source, Secondary Bit/LR Clock (SBCK/SLRCK) Frequency Setting Register

7	6	5	4	3	2	1	0
RSV	PSBCK2	PSBCK1	PSBCK0	RSV	PSLRCK2	PSLRCK1	PSLRCK0
R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

PSBCK[2:0]: DIR Clock Source, Secondary BCK (SBCK) Frequency Setting

000: $16f_S$ (BCK/4)
001: $32f_S$ (BCK/2)
010: $64f_S$ (1x BCK) (default)
011: $128f_S$ (2x BCK)
100: $256f_S$ (4x BCK)
101: Reserved
110: Reserved
111: Reserved

PSLRCK[2:0]: DIR Clock Source, Secondary LRCK (SLRCK) Frequency Setting

000: $f_S/4$ (LRCK/4)
001: $f_S/2$ (LRCK/2)
010: f_S (1x LRCK) (default)
011: $2f_S$ (2x LRCK)
100: $4f_S$ (4x LRCK)
101: Reserved
110: Reserved
111: Reserved

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7.5.20 XTI Source, Secondary Bit/LR Clock (SBCK/SLRCK) Frequency Setting Register (address = 33h) [reset = 00100010]

図 7-52. DIR Source, Secondary Bit/LR Clock (SBCK/SLRCK) Frequency Setting Register

7	6	5	4	3	2	1	0
RSV	XSBCK2	XSBCK1	XSBCK0	RSV	XSLRCK2	XSLRCK1	XSLRCK0
R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

XSBCK[2:0]: XTI Clock Source, Secondary BCK (SBCK) Frequency Setting

000: XTI/2 (12.288 MHz)
001: XTI/4 (6.144 MHz)
010: XTI/8 (3.072 MHz) (default)
011: XTI/16 (1.536 MHz)
100: XTI/32 (0.768 MHz)
101: Reserved
110: Reserved
111: Reserved

XSLRCK[2:0]: XTI Clock Source, Secondary LRCK (SLRCK) Frequency Setting

000: XTI/128 (192 kHz)
001: XTI/256 (96 kHz)
010: XTI/512 (48 kHz) (default)
011: XTI/1024 (24 kHz)
100: XTI/2048 (12 kHz)
101: Reserved
110: Reserved
111: Reserved

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7.5.21 DIR Input Biphase Source Select, Coax Amplifier Control Register (address = 34h) [reset = 11000010]

図 7-53. DIR Input Biphase Source Select, Coax Amplifier Control Register

7	6	5	4	3	2	1	0
RX0DIS	RX1DIS	RSV	RSV	RXSEL3	RXSEL2	RXSEL1	RXSEL0
R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

RX0DIS: Power Down for RXIN0 Coaxial Amplifier

0: Normal operation

1: Power down (default)

RX1DIS: Power Down for RXIN1 Coaxial Amplifier

0: Normal operation

1: Power down (default)

RXSEL[3:0]: DIR Input Biphase Signal Source Select

0000: RXIN0

0001: RXIN1

0010: RXIN2 (default)

0011: RXIN3

0100: RXIN4

0101: RXIN5

0110: RXIN6

0111: RXIN7

1000: RXIN8

1001: RXIN9

1010: RXIN10

1011: RXIN11

1100: Reserved

1101: Reserved

1110: Reserved

1111: TXOUT (internal DIT output)

Note

RX0DIS or RX1DIS must be set to 0, even when an S/PDIF, TTL, or OPTICAL input is provided into RXIN0 or RXIN1, without use of the built-in COAX amplifier.

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7.5.22 RECOUT0 Output Biphase Source Settings Register (address = 35h) [reset = 00000010]

図 7-54. RECOUT0 Output Biphase Source Settings Register

7	6	5	4	3	2	1	0
RSV	RSV	RSV	MPO0MUT	RO0SEL3	RO0SEL2	RO0SEL1	RO0SEL0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

RO0SEL0[3:0]: RECOUT0 Output Biphase Source Select

0000: RXIN0
0001: RXIN1
0010: RXIN2 (default)
0011: RXIN3
0100: RXIN4
0101: RXIN5
0110: RXIN6
0111: RXIN7
1000: RXIN8
1001: RXIN9
1010: RXIN10
1011: RXIN11
1100: Reserved
1101: Reserved
1110: Reserved
1111: TXOUT (internal DIT output)

MPO0MUT: MPO0 Mute Control

0: Output (default)
1: MUTE (Logic low level)

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7.5.23 RECOUT1 Output Biphase Source Settings Register (address = 36h) [reset = 00000010]

図 7-55. RECOUT1 Output Biphase Source Settings Register

7	6	5	4	3	2	1	0
RSV	RSV	RSV	MPO1MUT	RO1SEL3	RO1SEL2	RO1SEL1	RO1SEL0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

RO1SEL0[3:0]: RECOUT1 Output Biphase Source Select

0000: RXIN0
0001: RXIN1
0010: RXIN2 (default)
0011: RXIN3
0100: RXIN4
0101: RXIN5
0110: RXIN6
0111: RXIN7
1000: RXIN8
1001: RXIN9
1010: RXIN10
1011: RXIN11
1100: Reserved
1101: Reserved
1110: Reserved
1111: TXOUT (internal DIT output)

MPO1MUT: MPO1 Mute Control

0: Output (default)
1: MUTE (Logic low level)

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7.5.24 Port Sampling Frequency Calculator Measurement Target Setting Register (address = 37h) [reset = 00000000]

図 7-56. RECOUT1 Output Biphase Source Settings Register

7	6	5	4	3	2	1	0
RSV	RSV	RSV	RSV	RSV	PFSTGT2	PFSTGT1	PFSTGT0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

PFSTGT[2:0]: Port f_S Calculator, Target Port Setting

000: DIR (default)
001: ADC
010: AUXIN0
011: AUXIN1
100: AUXIN2
101: Main output port
110: AUX output port
111: DIT

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7.5.25 Port Sampling Frequency Calculator Result Output Register (address = 38h) [reset = N/A]

図 7-57. Port Sampling Frequency Calculator Result Output Register

7	6	5	4	3	2	1	0
PFSST	PFSPO2	PFSPO1	PFSPO0	PFSOUT3	PFSOUT2	PFSOUT1	PFSOUT0
R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

PFSST: Port Sampling Frequency Calculate Status

0: Calculated

1: Calculating

PFSPO[2:0]: Calculated Port Information

000: DIR

001: ADC

010: AUXIN0

011: AUXIN1

100: AUXIN2

101: Main output port

110: AUX output port

111: DIT

PFSOUT[3:0]: Calculated Sampling Frequency

0000: Out of range

0001: 8 kHz

0010: 11.025 kHz

0011: 12 kHz

0100: 16 kHz

0101: 22.05 kHz

0110: 24 kHz

0111: 32 kHz

1000: 44.1 kHz

1001: 48 kHz

1010: 64 kHz

1011: 88.2 kHz

1100: 96 kHz

1101: 128 kHz

1110: 176.4 kHz

1111: 192 kHz

Note

PFSST, PFSPO, and PFSOUT always output the status when these registers are read.

The other registers do not have clear functions when these are read. To enable these registers, DIR must be powered on. For example, (Register 40h/RXDIS = 0) PFSST indicates *Calculating* and PFSOUT indicates the previous value when no source comes to the port that is selected by Register 37h/PFSTGT.

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7.5.26 Incoming Biphase Information and Sampling Frequency Register (address = 39h) [reset = N/A]

図 7-58. Port Sampling Frequency Calculator Result Output Register

7	6	5	4	3	2	1	0
SFSST	SCSBIT1	RSV	RSV	SESOUT3	SESOUT2	SESOUT1	SESOUT0
R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

SFSST: Incoming Biphase Signal, Sampling Frequency Calculate Status

0: SFSOUT[3:0] Output is calculated

1: In the process of calculating or unlocked

SCSBIT1: Detected Channel Status Bit1 Flag

0: CS Bit1 = 0 (Audio data)

1: CS Bit1 = 1 (Non-audio data)

SFSOUT[3:0]: Incoming Biphase Signal, Actual Sampling Frequency

0000: Out of range

0001: 8 kHz

0010: 11.025 kHz

0011: 12 kHz

0100: 16 kHz

0101: 22.05 kHz

0110: 24 kHz

0111: 32 kHz

1000: 44.1 kHz

1001: 48 kHz

1010: 64 kHz

1011: 88.2 kHz

1100: 96 kHz

1101: 128 kHz

1110: 176.4 kHz

1111: 192 kHz

Note

When SFSST becomes 1 (that is, in the process of calculating or unlocked), SFSOUT holds the previous data. SFSST and SFSOUT always output the status when these registers are read. The other registers do not have clear functions when these are read. To enable these registers, DIR must be powered on (register 40h/RXDIS = 0).

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7.5.27 P_C Buffer (Burst Preamble P_C Output) Register (address = 3Ah) [reset = N/A]

図 7-59. P_C Buffer (Burst Preamble P_C Output) Register

15	14	13	12	11	10	9	8
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A
7	6	5	4	3	2	1	0
PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

PC[4:0]: Burst Preamble P_C, data type
PC[6:5]: Burst Preamble P_C, reserved
PC7: Burst Preamble P_C, Error
PC[12:8]: Burst Preamble P_C, data type dependent information
PC[15:13]: Burst Preamble P_C, bit stream no.

Read P_C/P_D after ONPCM1/0 goes high by setting MNPCM1 = 1 or MNPCM0 = 1. Polling P_C/P_D [15:0] is not allowed.

7.5.28 P_D Buffer (Burst Preamble P_D Output) Register (address = 3Ch) [reset = N/A]

図 7-60. P_D Buffer (Burst Preamble P_D Output) Register

15	14	13	12	11	10	9	8
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A
7	6	5	4	3	2	1	0
PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8
R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A	R-N/A

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

PD[15:0]: Burst Preamble P_D, Length Code (Number of bits)

PD[15:0] is updated at the time when PC[15:0] is updated. PD[15:0] is never updated when only PC[15:0] is updated. Register 2Ch/OPCRNW0 or Register 2Dh/OPCRNW1 inform the system that PC[15:0] is updated.

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7.5.29 System Reset Control Register (address = 40h) [reset = 11000000]

図 7-61. System Reset Control Register

7	6	5	4	3	2	1	0
MRST	SRST	ADDIS	RXDIS	RSV	RSV	TXDIS	XODIS
R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

MRST: Mode Control Register Reset for All Functions

0: Set default value

1: Normal operation (default)

SRST: System Reset for ADC

0: Reset

1: Normal operation (default)

To return the MRST, SRST bit to 0 is not necessary because the MRST, SRST bit is automatically set to 1.

ADDIS: Power Down for ADC

0: Normal operation (default)

1: Power down

SCK must be provided to disable ADC by ADDIS = 1.

RXDIS: Power Down for DIR

0: Normal operation (default)

1: Power down

TXDIS: Power Down for DIT

0: Normal operation (default)

1: Power down

XODIS: Power Down for OSC

0: Normal operation (default)

1: Power down

XODIS is superior to OSCAUTO.

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7.5.30 ADC Function Control Register 1/3 (address = 42h) [reset = 00000010]

図 7-62. ADC Function Control Register 1/3

7	6	5	4	3	2	1	0
RSV	RSV	ADCKOUT	ADDTRX7	ADFSLMT	ADCLK2	ADCLK1	ADCLK0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

ADCKOUT: ADC Clock (SCK, BCK, LRCK) Output Select at ADC Power-Down

0: Output enable even at ADDIS = 1 (default)

1: Output disable at ADDIS = 0

ADDTRX7: ADC Output Data Select to Main Port, DOUT Pin

0: DOUT = ADC DOUT (default)

1: DOUT = RXIN7 (ADIN0)

This register can select an external ADC data from RXIN7 (ADIN0) to Main Port DOUT pin when an external ADC is used.

ADFSLMT: ADC Sampling Frequency Limiter for DIR Clock Source

0: Disable (default)

1: Enable

When ADFSLMT = 1, ADCLK[2:0] = 001(ADC clock is DIR output clock) and DIR locks at frequency from 14 kHz to 111 kHz, the ADC is forced into power down.

ADCLK[2:0]: ADC Clock Source (SCK/BCK/LRCK) Select

000: AUTO (DIR or XTI)

001: DIR

010: XTI (default)

011: AUXIN0

100: AUXIN1

100: AUXIN2

110: Reserved

111: Reserved

The ADC clock source must be normally set to XTI source with fixed frequency (the clocks at the XTI source select are generated by the SCK/BCK/LRCK dividers). Its frequency is set by the register of XSCK[1:0], XBCK[1:0], and XLRCK[1:0].).

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7.5.31 ADC L-Ch, Digital ATT Control Register (address = 46h) [reset = 11010111]

図 7-63. ADC L-Ch, Digital ATT Control Register

7	6	5	4	3	2	1	0
ADATTL7	ADATTL6	ADATTL5	ADATTL4	ADATTL3	ADATTL2	ADATTL1	ADATTL0
R/W-1h	R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

ADATTL[7:0]: ADC L-Ch, Digital ATT Setting

1111 1111: +20.0 dB
1111 1110: +19.5 dB
1101 0111: 0 dB (default)
1101 0110: –0.5 dB
0000 1111: –100 dB
Others: Mute

7.5.32 ADC R-Ch, Digital ATT Control Register (address = 47h) [reset = 11010111]

図 7-64. ADC L-Ch, Digital ATT Control Register

7	6	5	4	3	2	1	0
ADATTR7	ADATTR6	ADATTR5	ADATTR4	ADATTR3	ADATTR2	ADATTR1	ADATTR0
R/W-1h	R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

ADATTR[7:0]: ADC R-Ch, Digital ATT Setting

1111 1111: +20.0 dB
1111 1110: +19.5 dB
1101 0111: 0 dB (default)
1101 0110: –0.5 dB
0000 1111: –100 dB
Others: Mute

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7.5.33 ADC Function Control Register 2/3 (address = 48h) [reset = 00000000]

図 7-65. ADC Function Control Register 2/3

7	6	5	4	3	2	1	0
RSV	ADIFMD2	ADIFMD1	ADIFMD0	RSV	RSV	ADFMT1	ADFMT0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

ADIFMD[2:0]: ADC Interface Mode Setting

000: Slave mode (default)

001: Reserved

010: Master mode, $512f_S$

011: Reserved

100: Master mode, $256f_S$

101: Reserved

110: Reserved

111: Reserved

Master mode settings are available only in ADC standalone mode (MPCSEL[2:0] = '001').

ADFMT[1:0]: ADC Audio I/F Format Setting

00: 24-bit I^2S (default)

01: 24-bit left-justified

10: 24-bit right-justified

11: 16-bit right-justified

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7.5.34 ADC Function Control Register 3/3 (address = 49h) [reset = 00000000]

図 7-66. ADC Function Control Register 3/3

7	6	5	4	3	2	1	0
RSV	RSV	RSV	ADZCDD	ADBYP	ADPHSE	ADMUTR	ADMUTL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

ADZCDD: Zero-Crossing Detection Disable for Digital Attenuation

0: Enable (default)

1: Disable.

ADBYP: High-Pass Filter Bypass Control

0: Normal output, HPF enable (default)

1: Bypassed output, HPF disenable

ADPHSE: Input Phase Select

0: Normal input (default)

1: Invert Input

ADMUTR: Soft Mute Control, R-Ch

0: Mute disabled (default)

1: Mute enabled

ADMUTL: Soft Mute Control, L-Ch

0: Mute disabled (default)

1: Mute enabled

The mute bits, ADMUTL and ADMUTR, are used to enable or disenable the soft mute function for the corresponding ADC outputs, DOUT.

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7.5.35 DIR Channel Status Data Buffer Register (address = 5Ah) [reset = 00000000]

図 7-67. DIR Channel Status Data Buffer Register

47	46	45	44	43	42	41	40
RXCS7	RXCS6	RXCS5	RXCS4	RXCS3	RXCS2	RXCS1	RXCS0
CS Bit7	CS Bit6	CS Bit5	CS Bit4	CS Bit3	CS Bit2	CS Bit1	CS Bit0
R	R	R	R	R	R	R	R
39	38	37	36	35	34	33	32
RXCS15	RXCS14	RXCS13	RXCS12	RXCS11	RXCS10	RXCS9	RXCS8
CS Bit15	CS Bit14	CS Bit13	CS Bit12	CS Bit11	CS Bit10	CS Bit9	CS Bit8
R	R	R	R	R	R	R	R
31	30	29	28	27	26	25	24
RXCS23	RXCS22	RXCS21	RXCS20	RXCS19	RXCS18	RXCS17	RXCS16
CS Bit23	CS Bit22	CS Bit21	CS Bit20	CS Bit19	CS Bit18	CS Bit17	CS Bit16
R	R	R	R	R	R	R	R
23	22	21	20	19	18	17	16
RXCS31	RXCS30	RXCS29	RXCS28	RXCS27	RXCS26	RXCS25	RXCS24
CS Bit31	CS Bit30	CS Bit29	CS Bit28	CS Bit27	CS Bit26	CS Bit25	CS Bit24X
R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
RXCS39	RXCS38	RXCS37	RXCS36	RXCS35	RXCS34	RXCS33	RXCS32
CS Bit39	CS Bit38	CS Bit37	CS Bit36	CS Bit35	CS Bit34	CS Bit33	CS Bit32
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
RXCS47	RXCS46	RXCS45	RXCS44	RXCS43	RXCS42	RXCS41	RXCS40
CS Bit47	CS Bit46	CS Bit45	CS Bit44	CS Bit43	CS Bit42	CS Bit41	CS Bit40
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

RXCS0: Use of channel status block
RXCS1: Linear PCM information
RXCS2: Copyright information
RXCS5 – RXCS3: Additional format information
RXCS7– RXCS6: Channel status mode
RXCS15 – RXCS8: Category code
RXCS19 – RXCS16: Source number
RXCS23 – RXCS20: Channel number
RXCS27 – RXCS24: Sampling frequency
RXCS29 – RXCS28: Clock accuracy
RXCS31 – RXCS30: Not defined
RXCS32: Maximum audio sample word length
RXCS35 – RXCS33: Sample word length
RXCS39 – RXCS36: Original sampling frequency
RXCS47 – RXCS40: Not defined

xx of RXCSxx represents the serial number of the channel status data. L-channel data of the channel status is stored in this register. Its default value is not specified. Therefore, wait until the ERROR/INT0 port goes low and 192 samples pass to read RXCS. RXCS is cleared when DIR unlocks and an L-ch parity error is detected.

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7.5.36 DIT Function Control Register 1/3 (address = 60h) [reset = 01000100]

図 7-68. DIT Function Control Register 1/3

7	6	5	4	3	2	1	0
RSV	TXSSRC2	TXSSRC1	TXSSRC0	RSV	TXPSRC2	TXPSRC1	TXPSRC0
R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

TXSSRC[2:0]: DIT System Clock Source Select

000: DIR/ADC Automatic (DIR lock = DIR, DIR unlock = ADC)
001: DIR
010: ADC
011: AUXIN0
100: AUXIN1 (default)
101: AUXIN2
110: Reserved
111: Reserved

TXPSRC[2:0]: DIT Bit Clock, LR Clock, Data Source Select

000: DIR/ADC Automatic (DIR lock = DIR, DIR unlock = ADC)
001: DIR
010: ADC
011: AUXIN0
100: AUXIN1 (default)
101: AUXIN2
110: Reserved
111: Reserved

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7.5.37 DIT Function Control Register 2/3 (address = 61h) [reset = 00010000]

図 7-69. DIT Function Control Register 2/3

7	6	5	4	3	2	1	0
RSV	TXSCK2	TXSCK1	TXSCK0	RSV	TXDSD	TXFMT1	TXFMT0
R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

TXSCK[2:0]: DIT System Clock Control

000: $128f_S$
001: $256f_S$ (default)
010: $512f_S$
011: Reserved
100: Controlled by DIR system clock rate
100: Controlled by DIR system clock rate
110: Controlled by DIR system clock rate
111: Controlled by DIR system clock rate

TXDSD: DIT DSD Input Enable

0: DSD input disable (default)
1: DSD input enable

Note

When TXDSD is set to 1, the DIT LR clock is generated by the Bit Clock divided by 64. The DIT source data are forced to all 0s. Provide the DSD source to MPIO_B0 for the system clock ($256f_S$), MPIO_B1 for the DSD bit clock ($64f_S$), MPIO_B2 for L-ch data, and MPIO_B3 for R-ch data.

This function is useful when it is desired to suppress system clock jitter by using the path that is DIT to DIR. Jitter of the system clock generated by DIR is also reduced if the jitter is high frequency.

TXFMT[1:0]:DIT Audio I/F Format Setting

00: 24-bit I^2S (default)
01: 24-bit left-justified
10: 24-bit right-justified
11: 16-bit right-justified

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7.5.38 DIT Function Control Register 3/3 (address = 62h) [reset = 00000000]

図 7-70. DIT Function Control Register 3/3

7	6	5	4	3	2	1	0
RSV	RSV	TXDMUT	RSV	TXVFLG	RSV	RSV	RSV
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

TXDMUT: DIT Output Audio Data Mute Control

0: No mute (default)

1: Audio data on biphase signal is Mute (zero data)

TXVFLG: DIT Output Validity Flag Control

0: V = 0, Valid (default)

1: V = 1, Invalid

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7.5.39 DIT Channel Status Data Buffer Register (address = 63h) [reset = 00000000]

図 7-71. DIT Channel Status Data Buffer Register

47	46	45	44	43	42	41	40
TXCS7	TXCS6	TXCS5	TXCS4	TXCS3	TXCS2	TXCS1	TXCS0
CS Bit7	CS Bit6	CS Bit5	CS Bit4	CS Bit3	CS Bit2	CS Bit1	CS Bit0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
39	38	37	36	35	34	33	32
TXCS15	TXCS14	TXCS13	TXCS12	TXCS11	TXCS10	TXCS9	TXCS8
CS Bit15	CS Bit14	CS Bit13	CS Bit12	CS Bit11	CS Bit10	CS Bit9	CS Bit8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
31	30	29	28	27	26	25	24
TXCS23	TXCS22	TXCS21	TXCS20	TXCS19	TXCS18	TXCS17	TXCS16
CS Bit23	CS Bit22	CS Bit21	CS Bit20	CS Bit19	CS Bit18	CS Bit17	CS Bit16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
23	22	21	20	19	18	17	16
TXCS31	TXCS30	TXCS29	TXCS28	TXCS27	TXCS26	TXCS25	TXCS24
CS Bit31	CS Bit30	CS Bit29	CS Bit28	CS Bit27	CS Bit26	CS Bit25	CS Bit24X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
15	14	13	12	11	10	9	8
TXCS39	TXCS38	TXCS37	TXCS36	TXCS35	TXCS34	TXCS33	TXCS32
CS Bit39	CS Bit38	CS Bit37	CS Bit36	CS Bit35	CS Bit34	CS Bit33	CS Bit32
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
TXCS47	TXCS46	TXCS45	TXCS44	TXCS43	TXCS42	TXCS41	TXCS40
CS Bit47	CS Bit46	CS Bit45	CS Bit44	CS Bit43	CS Bit42	CS Bit41	CS Bit40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

TXCS0: Use of channel status block.
TXCS1: Linear PCM information.
TXCS2: Copyright information.
TXCS5 – TXCS3: Additional format information.
TXCS7 – TXCS6: Channel status mode.
TXCS15 – TXCS8: Category code.
TXCS19 – TXCS16: Source number.
TXCS23 – TXCS20: Channel number.
TXCS27 – TXCS24: Sampling frequency.
TXCS29 - TXCS28: Clock accuracy.
TXCS31 – TXCS30: Not defined.
TXCS32: Maximum audio sample word length.
TXCS35 – TXCS33: Sample word length.
TXCS39 – TXCS36: Original sampling frequency.
TXCS47 – TXCS40: Not defined.

The data in this register are used for both channels (L-ch and R-ch). When these register data are used for the DIT channel status data, a channel status data of bit 48 or later is all 0. All initial values of this register are all 0.

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7.5.40 Main Output and AUXOUT Port Control Register (address = 6A) [reset = 00000000]

図 7-72. Main Output and AUXOUT Port Control Register

7	6	5	4	3	2	1	0
AOMUTAS	MOMUTAS	RSV	RSV	AOLRMTEN	AODMUT	MOLRMTEN	MODMUT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

AOMUTAS: AUX Output Port, Mute Synchronization Select (MPIO_B2 and MPIO_B3)

0: AODMUT works with synchronization with LRCK edge. (default)

1: AODMUT works without synchronization with LRCK edge

MOMUTAS: Main Output Port, Mute Synchronization Select (LRCK and DOUT)

0: MODMUT works with synchronization with LRCK edge. (default)

1: MODMUT works without synchronization with LRCK edge

AOLRMTEN: AODMUT Signal Select (MPIO_B2)

0: Only DOUT (default)

1: Both of LRCK and DOUT

AODMUT: AUX Output Port, Data Mute Control

0: Output (default)

1: Mute (the affected signals are selected by Register 6Ah, AOLRMTEN)

MOLRMTEN : MODMUT signal select

0: Only DOUT (default)

1: Both LRCK and DOUT

MODMUT: Main Output Port, DOUT Mute Control

0: Output (default)

1: Mute (the affected signals are selected by Register 6Ah, MOLRMTEN)

Data mutes are done in synchronization with a LRCK edge.

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7.5.41 Main Output Port (SCKO/BCK/LRCK/DOUT) Source Setting Register (address = 6Bh) [reset = 00000000]

図 7-73. Main Output Port (SCKO/BCK/LRCK/DOUT) Source Setting Register

7	6	5	4	3	2	1	0
RSV	MOSSRC2	MOSSRC1	MOSSRC0	RSV	MOPSRC2	MOPSRC1	MOPSRC0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

MOSSRC[2:0]: Main Output Port, SCK Source Control

000: DIR/ADC Automatic (DIR lock:DIR, DIR unlock:ADC) (default)
001: DIR
010: ADC
011: AUXIN0
100: AUXIN1
101: AUXIN2
110: Reserved
111: Reserved

MOPSRC[2:0]: Main Output Port, BCK/LRCK/DATA Source Control

000: DIR/ADC Automatic (DIR lock:DIR, DIR unlock:ADC) (default)
001: DIR
010: ADC
011: AUXIN0
100: AUXIN1
101: AUXIN2
110: Reserved
111: Reserved

This source control register is divided into two parts (MOSSRC and MOPSRC). This architecture allows some additional functionality such as jitter cleaning. To clean the clock jitter of the HDMI receiver output, the HDMI receiver S/PDIF output is connected with the PCM9211 S/PDIF input, and the HDMI receiver I^2S outputs (BCK/LRCK/DATA) are connected with the PCM9211 PCM input port.

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7.5.42 AUX Output Port (AUXSCKO/AUXBCKO/AUXLRCKO/AUXDOUT) Source Setting Register (address = 6Ch) [reset = 00000000]

図 7-74. AUX Output Port (SCKO/BCK/LRCK/DOUT) Source Setting Register

7	6	5	4	3	2	1	0
RSV	AOSSRC2	AOSSRC1	AOSSRC0	RSV	AOPSRC2	AOPSRC1	AOPSRC0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

AOSSRC[2:0]: AUX Output Port, SCK Source Control

000: DIR/ADC automatic (DIR lock:DIR, DIR unlock:ADC) (default)
001: DIR
010: ADC
011: AUXIN0
100: AUXIN1
101: Reserved
110: Reserved
111: Reserved

AOPSRC[2:0]: AUX Output Port, BCK/LRCK/DATA Source Control

000: DIR/ADC automatic (DIR lock:DIR, DIR unlock:ADC) (default)
001: DIR
010: ADC
011: AUXIN0
100: AUXIN1
101: Reserved
110: Reserved
111: Reserved

This source control register is divided into two parts (MOSSRC and MOPSRC). This design allows some additional functionality such as jitter cleaning. To clean the clock jitter of the HDMI receiver output, the HDMI receiver S/PDIF output is connected to the PCM9211 S/PDIF input, and the HDMI receiver I^2S outputs (BCK/LRCK/DATA) are connected with the PCM9211 PCM input port.

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7.5.43 MPIO_B and Main Output Port Hi-Z Control Register (address = 6Dh) [reset = 00000000]

図 7-75. MPIO_B and Main Output Port Hi-Z Control Register

7	6	5	4	3	2	1	0
MPB3HZ	MPB2HZ	MPB1HZ	MPB0HZ	SCKOHZ	BCKHZ	LRCKHZ	DOUTHZ
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

MPB3HZ: MPIO_B3, Hi-Z Control

0: Defined by Group Function Assign register, 6Fh/MPBSEL. (default)

1: Hi-Z

MPB2HZ: MPIO_B2, Hi-Z Control

0: Defined by Group Function Assign register, 6Fh/MPBSEL. (default)

1: Hi-Z

MPB1HZ: MPIO_B1, Hi-Z Control

0: Defined by Group Function Assign register, 6Fh/MPBSEL. (default)

1: Hi-Z

MPB0HZ: MPIO_B0, Hi-Z Control

0: Defined by Group Function Assign register, 6Fh/MPBSEL. (default)

1: Hi-Z

SCKOHZ: Main Output Port, SCKO Hi-Z Control

0: Output (default)

1: Hi-Z

BCKHZ: Main Output Port, BCKO Hi-Z Control

0: Output (default)

1: Hi-Z

LRCKHZ: Main Output Port, LRCKO Hi-Z Control

0: Output (default)

1: Hi-Z

DOUTHZ: Main Output Port, DOUT Hi-Z Control

0: Output (default)

1: Hi-Z

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7.5.44 MPIO_C and MPIO_A Hi-Z Control Register (address = 6Eh) [reset = 00001111]

図 7-76. MPIO_C and MPIO_A Hi-Z Control Register

7	6	5	4	3	2	1	0
MPC3HZ	MPC2HZ	MPC1HZ	MPC0HZ	MPA3HZ	MPA2HZ	MPA1HZ	MPA0HZ
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

MPC3HZ: MPIO_C3, Hi-Z Control

0: Defined by Group Function Assign register, 6Fh/MPCSEL. (default)

1: Hi-Z

MPC2HZ: MPIO_C2, Hi-Z Control

0: Defined by Group Function Assign register, 6Fh/MPCSEL. (default)

1: Hi-Z

MPC1HZ: MPIO_C1, Hi-Z Control

0: Defined by Group Function Assign register, 6Fh/MPCSEL. (default)

1: Hi-Z

MPC0HZ: MPIO_C0, Hi-Z Control

0: Defined by Group Function Assign register, 6Fh/MPCSEL. (default)

1: Hi-Z

MPA3HZ:M PIO_A3, Hi-Z Control

0: Defined by Group Function Assign register, 6Fh/MPASEL.

1: Hi-Z (default)

MPA2HZ:M PIO_A2, Hi-Z Control

0: Defined by Group Function Assign register, 6Fh/MPASEL.

1: Hi-Z (default)

MPA1HZ:M PIO_A1, Hi-Z Control

0: Defined by Group Function Assign register, 6Fh/MPASEL.

1: Hi-Z (default)

MPA0HZ:M PIO_A0, Hi-Z Control

0: Defined by Group Function Assign register, 6Fh/MPASEL.

1: Hi-Z (default)

Note

In multichannel PCM mode, the MCHR and MPAxHz registers (20h) must be set to 0 to get the outputs from the main port.

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7.5.45 MPIO_A, MPIO_B, MPIO_C Group Function Assign Register (address = 6Fh) [reset = 01000000]

図 7-77. MPIO_A, MPIO_B, MPIO_C Group Function Assign Register

7	6	5	4	3	2	1	0
MPASEL1	MPASEL0	MPBSEL2	MPBSEL1	MPBSEL0	MPCSEL2	MPCSEL1	MPCSEL0
R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

MPASEL[1:0]: MPIO_A Group Function Assign Setting

00: Biphase Input Extension (RXIN8 to RXIN11)

01: CLKST Output, VOUT Output, XMCKO Output, INT0 Output (default)

10: Secondary BCK/LRCK Output, XMCKO Output, INT0 Output

11: DIR Flags Output or GPIO (Selected by MPA3SEL, MPA2SEL, MPA1SEL, MPA0SEL)

MPBSEL[2:0]: MPIO_B Group Function Assign Setting

000: AUXIN2 (default)

001: AUXOUT

010: Sampling Frequency Calculated Result: FSOUT[3:0]

011: DIR Flags Output or GPIO (Selected by MPB3SEL, MPB2SEL, MPB1SEL, MPB0SEL)

100: DIR BCUV OUT, BFRAME/VOUT/UOUT/COUT

101: External Slave ADC Input (Clocks: Out, Data: In, EASCKO/EABCKO/EALRCKO/EADIN)

110: Reserved

111: Test Mode

MPCSEL[2:0]: MPIO_C Group Function Assign Setting

000: AUXIN1 (default)

001: ADC Standalone Operation, Clock, and Data I/O, ADSCK/ADBCK/ADLRCK/ADDOUT

010: Sampling Frequency Calculated Result: FSOUT[3:0]

011: DIR Flags Output or GPIO (Selected by MPC3SEL, MPC2SEL, MPC1SEL, MPC0SEL)

100: DIR BCUV OUT, BFRAME/VOUT/UOUT/COUT

101: DIT Standalone Operation, Clock, and Data I/O, TXSCK/TXBCK/TXLRCK/TXDIN

110: Reserved

111: Reserved

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7.5.46 MPIO_A Flags or GPIO Assign Setting Register (address = 70h) [reset = 00000000]

図 7-78. MPIO_A Flags or GPIO Assign Setting Register

7	6	5	4	3	2	1	0
RSV	RSV	MCHRSRC1	MCHRSRC0	MPA3SEL	MPA2SEL	MPA1SEL	MPA0SEL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

MCHRSRC: AUX Output Port, SCK Source Control

00: See 表 7-29, Multi-Channel PCM Routing (default)

01: See 表 7-29, Multi-Channel PCM Routing

10: See 表 7-29, Multi-Channel PCM Routing

11: See 表 7-29, Multi-Channel PCM Routing

MPA3SEL: MPIO_A3 Pin Function, DIR Flags or GPIO Select

0: DIR Flags, set by MPA3FLG[3:0] (default)

1: GPIO, set by GIOA3DIR/GPOA3/GPIA3

MPA2SEL: MPIO_A2 Pin Function, DIR Flags or GPIO Select

0: DIR Flags, set by MPA2FLG[3:0] (default)

1: GPIO, set by GIOA2DIR/GPOA2/GPIA2

MPA1SEL: MPIO_A1 Pin Function, DIR Flags or GPIO Select

0: DIR Flags, set by MPA1FLG[3:0] (default)

1: GPIO, set by GIOA1DIR/GPOA1/GPIA1

MPA0SEL: MPIO_A0 Pin Function, DIR Flags or GPIO Select

0: DIR Flags, set by MPA0FLG[3:0] (default)

1: GPIO, set by GIOA0DIR/GPOA0/GPIA0

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7.5.47 MPIO_B, MPIO_C Flags or GPIO Assign Setting Register (address = 71h) [reset = 00000000]

図 7-79. MPIO_B, MPIO_C Flags or GPIO Assign Setting Register

7	6	5	4	3	2	1	0
MPB3SEL	MPB2SEL	MPB1SEL	MPB0SEL	MPC3SEL	MPC2SEL	MPC1SEL	MPC0SEL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

MPB3SEL: MPIO_B3 Pin Function, DIR Flags or GPIO Select

0: DIR Flags, set by MPB3FLG[3:0] (default)

1: GPIO, set by GIOB3DIR/GPOB3/GPIB3

MPB2SEL: MPIO_B2 Pin Function, DIR Flags or GPIO Select

0: DIR Flags, set by MPB2FLG[3:0] (default)

1: GPIO, set by GIOB2DIR/GPOB2/GPIB2

MPB1SEL: MPIO_B1 Pin Function, DIR Flags or GPIO Select

0: DIR Flags, set by MPB1FLG[3:0] (default)

1: GPIO, set by GIOB1DIR/GPOB1/GPIB1

MPB0SEL: MPIO_B0 Pin Function, DIR Flags or GPIO Select

0: DIR Flags, set by MPB0FLG[3:0] (default)

1: GPIO, set by GIOB0DIR/GPOB0/GPIB0

MPC3SEL: MPIO_C3 Pin Function, DIR Flags or GPIO Select

0: DIR Flags, set by MPC3FLG[3:0] (default)

1: GPIO, set by GIOC3DIR/GPOC3/GPIC3

MPC2SEL: MPIO_C2 Pin Function, DIR Flags or GPIO Select

0: DIR Flags, set by MPC2FLG[3:0] (default)

1: GPIO, set by GIOC2DIR/GPOC2/GPIC2

MPC1SEL: MPIO_C1 Pin Function, DIR Flags or GPIO Select

0: DIR Flags, set by MPC1FLG[3:0] (default)

1: GPIO, set by GIOC1DIR/GPOC1/GPIC1

MPC0SEL: MPIO_C0 Pin Function, DIR Flags or GPIO Select

0: DIR Flags, set by MPC0FLG[3:0] (default)

1: GPIO, set by GIOC0DIR/GPOC0/GPIC0

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7.5.48 MPIO_A1, MPIO_A0 Output Flag Select Register (address = 72h) [reset = 00000000]

図 7-80. MPIO_B, MPIO_C Flags or GPIO Assign Setting Register

7	6	5	4	3	2	1	0
MPA1FLG3	MPA1FLG2	MPA1FLG1	MPA1FLG0	MPA0FLG3	MPA0FLG2	MPA0FLG1	MPA0FLG0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

MPA1FLG[3:0]: MPIO_A1 Pin, Flag Select

0000: CLKST (default)
0001: EMPH
0010: BPSYNC
0011: DTSCD
0100: PARITY
0101: LOCK
0110: VOUT
0111: UOUT
1000: COUT
1001: BFRAME
1010: FSOUT0
1011: FSOUT1
1100: FSOUT2
1101: FSOUT3
1110: INT0
1111: INT1

MPA0FLG[3:0]: MPIO_A0 Pin, Flag Select

0000: CLKST (default)
0001: EMPH
0010: BPSYNC
0011: DTSCD
0100: PARITY
0101: LOCK
0110: VOUT
0111: UOUT
1000: COUT
1001: BFRAME
1010: FSOUT0
1011: FSOUT1
1100: FSOUT2
1101: FSOUT3
1110: INT0
1111: INT1

These register settings are effective only at MPASEL[1:0] = 11, MPA3SEL = 0, and MPA2SEL = 0.

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7.5.49 MPIO_A3, MPIO_A0 Output Flag Select Register (address = 73h) [reset = 00000000]

図 7-81. MPIO_A3, MPIO_A0 Output Flag Select Register

7	6	5	4	3	2	1	0
MPA3FLG3	MPA3FLG2	MPA3FLG1	MPA3FLG0	MPA2FLG3	MPA2FLG2	MPA2FLG1	MPA2FLG0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

MPA3FLG[3:0]: MPIO_A3 Pin, Flag Select

0000: CLKST (default)
0001: EMPH
0010: BPSYNC
0011: DTSCD
0100: PARITY
0101: LOCK
0110: VOUT
0111: UOUT
1000: COUT
1001: BFRAME
1010: FSOUT0
1011: FSOUT1
1100: FSOUT2
1101: FSOUT3
1110: INT0
1111: INT1

MPA2FLG[3:0]: MPIO_A2 Pin, Flag Select

0000: CLKST (default)
0001: EMPH
0010: BPSYNC
0011: DTSCD
0100: PARITY
0101: LOCK
0110: VOUT
0111: UOUT
1000: COUT
1001: BFRAME
1010: FSOUT0
1011: FSOUT1
1100: FSOUT2
1101: FSOUT3
1110: INT0
1111: INT1

These register settings are effective only at MPASEL[1:0] = 11, MPA3SEL = 0, and MPA2SEL = 0.

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7.5.50 MPIO_B1, MPIO_B0 Output Flag Select Register (address = 74h) [reset = 00000000]

図 7-82. MPIO_B1, MPIO_B0 Output Flag Select Register

7	6	5	4	3	2	1	0
MPB1FLG3	MPB1FLG2	MPB1FLG1	MPB1FLG0	MPB0FLG3	MPB0FLG2	MPB0FLG1	MPB0FLG0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

MPB1FLG[3:0]: MPIO_B1 Pin, Flag Select

0000: CLKST (default)
0001: EMPH
0010: BPSYNC
0011: DTSCD
0100: PARITY
0101: LOCK
0110: VOUT
0111: UOUT
1000: COUT
1001: BFRAME
1010: FSOUT0
1011: FSOUT1
1100: FSOUT2
1101: FSOUT3
1110: INT0
1111: INT1

MPB0FLG[3:0]: MPIO_B0 Pin, Flag Select

0000: CLKST (default)
0001: EMPH
0010: BPSYNC
0011: DTSCD
0100: PARITY
0101: LOCK
0110: VOUT
0111: UOUT
1000: COUT
1001: BFRAME
1010: FSOUT0
1011: FSOUT1
1100: FSOUT2
1101: FSOUT3
1110: INT0
1111: INT1

These register settings are effective only at MPBSEL[2:0] = 011, MPB1SEL = 0, and MPB0SEL = 0.

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7.5.51 MPIO_B3, MPIO_B2 Output Flag Select Register (address = 75h) [reset = 00000000]

図 7-83. MPIO_B3, MPIO_B2 Output Flag Select Register

7	6	5	4	3	2	1	0
MPB3FLG3	MPB3FLG2	MPB3FLG1	MPB3FLG0	MPB2FLG3	MPB2FLG2	MPB2FLG1	MPB2FLG0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

MPB3FLG[3:0]: MPIO_B3 Pin, Flag Select

0000: CLKST (default)
0001: EMPH
0010: BPSYNC
0011: DTSCD
0100: PARITY
0101: LOCK
0110: VOUT
0111: UOUT
1000: COUT
1001: BFRAME
1010: FSOUT0
1011: FSOUT1
1100: FSOUT2
1101: FSOUT3
1110: INT0
1111: INT1

MPB2FLG[3:0]: MPIO_B2 Pin, Flag Select

0000: CLKST (default)
0001: EMPH
0010: BPSYNC
0011: DTSCD
0100: PARITY
0101: LOCK
0110: VOUT
0111: UOUT
1000: COUT
1001: BFRAME
1010: FSOUT0
1011: FSOUT1
1100: FSOUT2
1101: FSOUT3
1110: INT0
1111: INT1

These register settings are effective only at MPBSEL[2:0] = 011, MPB3SEL = 0, and MPB2SEL = 0.

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7.5.52 MPIO_C1, MPIO_C0 Output Flag Select Register (address = 76h) [reset = 00000000]

図 7-84. MPIO_C1, MPIO_C0 Output Flag Select Register

7	6	5	4	3	2	1	0
MPC1FLG3	MPC1FLG2	MPC1FLG1	MPC1FLG0	MPC0FLG3	MPC0FLG2	MPC0FLG1	MPC0FLG0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

MPC1FLG[3:0]: MPIO_C1 Pin, Flag Select

0000: CLKST (default)
0001: EMPH
0010: BPSYNC
0011: DTSCD
0100: PARITY
0101: LOCK
0110: VOUT
0111: UOUT
1000: COUT
1001: BFRAME
1010: FSOUT0
1011: FSOUT1
1100: FSOUT2
1101: FSOUT3
1110: INT0
1111: INT1

MPC0FLG[3:0]: MPIO_C0 Pin, Flag Select

0000: CLKST (default)
0001: EMPH
0010: BPSYNC
0011: DTSCD
0100: PARITY
0101: LOCK
0110: VOUT
0111: UOUT
1000: COUT
1001: BFRAME
1010: FSOUT0
1011: FSOUT1
1100: FSOUT2
1101: FSOUT3
1110: INT0
1111: INT1

These register settings are effective only at MPCSEL[2:0] = 011, MPC1SEL = 0, and MPC0SEL = 0.

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7.5.53 MPIO_C3, MPIO_C2 Output Flag Select Register (address = 77h) [reset = 00000000]

図 7-85. MPIO_C3, MPIO_C2 Output Flag Select Register

7	6	5	4	3	2	1	0
MPC3FLG3	MPC3FLG2	MPC3FLG1	MPC3FLG0	MPC2FLG3	MPC2FLG2	MPC2FLG1	MPC2FLG0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

MPC3FLG[3:0]: MPIO_C3 Pin, Flag Select

0000: CLKST (default)
0001: EMPH
0010: BPSYNC
0011: DTSCD
0100: PARITY
0101: LOCK
0110: VOUT
0111: UOUT
1000: COUT
1001: BFRAME
1010: FSOUT0
1011: FSOUT1
1100: FSOUT2
1101: FSOUT3
1110: INT0
1111: INT1

MPC2FLG[3:0]: MPIO_C2 Pin, Flag Select

0000: CLKST (default)
0001: EMPH
0010: BPSYNC
0011: DTSCD
0100: PARITY
0101: LOCK
0110: VOUT
0111: UOUT
1000: COUT
1001: BFRAME
1010: FSOUT0
1011: FSOUT1
1100: FSOUT2
1101: FSOUT3
1110: INT0
1111: INT1

These register settings are effective only at MPCSEL[2:0] = 011, MPC3SEL = 0, and MPC2SEL = 0.

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7.5.54 MPO1, MPO0 Function Assign Setting Register (address = 78h) [reset = 00111101]

図 7-86. MPO1, MPO0 Output Flag Select Register

7	6	5	4	3	2	1	0
MPO1SEL3	MPO1SEL2	MPO1SEL1	MPO1SEL0	MPO0SEL3	MPO0SEL2	MPO0SEL1	MPO0SEL0
R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

MPO1SEL[3:0]: MPO1 Pin, Output Control

0000: Hi-Z
0001: GPO, Output data = High level
0010: GPO, Output data = Low level
0011: VOUT (default)
0100: INT0
0101: INT1
0110: CLKST
0111: EMPH
1000: BPSYNC
1001: DTSCD
1010: PARITY
1011: LOCK
1100: XMCKO
1101: TXOUT
1110: RECOUT0
1111: RECOUT1

MPO0SEL[3:0]: MPO0 Pin, Output Control

0000: Hi-Z
0001: GPO, Output data = High level
0010: GPO, Output data = Low level
0011: VOUT
0100: INT0
0101: INT1
0110: CLKST
0111: EMPH
1000: BPSYNC
1001: DTSCD
1010: PARITY
1011: LOCK
1100: XMCKO
1101: TXOUT (default)
1110: RECOUT0
1111: RECOUT1

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7.5.55 GPIO I/O Direction Control for MPIO_A, MPIO_B Register (address = 79h) [reset = 00000000]

図 7-87. GPIO I/O Direction Control for MPIO_A, MPIO_B Register

7	6	5	4	3	2	1	0
GIOB3DIR	GIOB2DIR	GIOB1DIR	GIOB0DIR	GIOA3DIR	GIOA2DIR	GIOA1DIR	GIOA0DIR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

GIOB3DIR: MPIO_B3 Pin, GPIO I/O Direction Control

0: Input (default)

1: Output

GIOB2DIR: MPIO_B2 Pin, GPIO I/O Direction Control

0: Input (default)

1: Output

GIOB1DIR: MPIO_B1 Pin, GPIO I/O Direction Control

0: Input (default)

1: Output

GIOB0DIR: MPIO_B0 Pin, GPIO I/O Direction Control

0: Input (default)

1: Output

GIOA3DIR: MPIO_A3 Pin Function, GPIO I/O Direction Control

0: Input (default)

1: Output

GIOA2DIR: MPIO_A2 Pin Function, GPIO I/O Direction Control

0: Input (default)

1: Output

GIOA`DIR: MPIO_A1 Pin Function, GPIO I/O Direction Control

0: Input (default)

1: Output

GIOA0DIR: MPIO_A0 Pin Function, GPIO I/O Direction Control

0: Input (default)

1: Output

These registers are effective only at MPIO_A and MPIO_B assigned as GPIO. I/O direction setting is available by pin.

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7.5.56 GPIO I/O Direction Control for MPIO_C Register (address = 7Ah) [reset = 00000000]

図 7-88. GPIO I/O Direction Control for MPIO_C Register

7	6	5	4	3	2	1	0
RSV	RSV	RSV	RSV	GIOC3DIR	GIOC2DIR	GIOC1DIR	GIOC0DIR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

GIOC3DIR: MPIO_C3 Pin, GPIO I/O Direction Control

0: Input (default)

1: Output

GIOC2DIR: MPIO_C2 Pin, GPIO I/O Direction Control

0: Input (default)

1: Output

GIOC1DIR: MPIO_C1 Pin, GPIO I/O Direction Control

0: Input (default)

1: Output

GIOC0DIR: MPIO_C0 Pin, GPIO I/O Direction Control

0: Input (default)

1: Output

These registers are effective only at MPIO_C assigned as GPIO. I/O direction setting is available by pin.

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7.5.57 GPIO Output Data Setting for MPIO_A, MPIO_B Register (address = 7Bh) [reset = 00000000]

図 7-89. GPIO Output Data Setting for MPIO_A, MPIO_B Register

7	6	5	4	3	2	1	0
GPOB3	GPOB2	GPOB1	GPOB1	GPOA3	GPOA2	GPOA1	GPOA0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

GPOB3: MPIO_B3 Pin, GPIO Output Data Setting

0: Output low level (default)

1: Output high level

GPOB2: MPIO_B2 Pin, GPIO Output Data Setting

0: Output low level (default)

1: Output high level

GPOB1: MPIO_B1 Pin, GPIO Output Data Setting

0: Output low level (default)

1: Output high level

GPOB0: MPIO_B0 Pin, GPIO Output Data Setting

0: Output low level (default)

1: Output high level

GPOA3: MPIO_A3 Pin, GPIO Output Data Setting

0: Output low level (default)

1: Output high level

GPOA2: MPIO_A2 Pin, GPIO Output Data Setting

0: Output low level (default)

1: Output high level

GPOA1: MPIO_A1 Pin, GPIO Output Data Setting

0: Output low level (default)

1: Output high level

GPOA0: MPIO_A0 Pin, GPIO Output Data Setting

0: Output low level (default)

1: Output high level

These registers are effective only as GPIOs are assigned to output.

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7.5.58 GPIO Output Data Setting for MPIO_C Register (address = 7Ch) [reset = 00000000]

図 7-90. GPIO I/O Direction Control for MPIO_C Register

7	6	5	4	3	2	1	0
RSV	RSV	RSV	RSV	GPOC3	GPOC2	GPOC1	GPOC0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

GPOC3: MPIO_C3 Pin, GPIO Output Data Setting

0: Output low level (default)

1: Output high level

GPOC2: MPIO_C2 Pin, GPIO Output Data Setting

0: Output low level (default)

1: Output high level

GPOC1: MPIO_C1 Pin, GPIO Output Data Setting

0: Output low level (default)

1: Output high level

GPOC0: MPIO_C0 Pin, GPIO Output Data Setting

0: Output low level (default)

1: Output high level

These registers are effective only as GPIOs are assigned to output.

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7.5.59 GPIO Input Data Register for MPIO_A, MPIO_B Register (address = 7Dh) [reset = N/A]

図 7-91. GPIO Input Data Register for MPIO_A, MPIO_B Register

7	6	5	4	3	2	1	0
GPIB3	GPIB2	GPIB1	GPIB1	GPIA3	GPIA2	GPIA1	GPIA0
N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

GPIB3: MPIO_B3 Pin, GPIO Input Data

0: Detect low level

1: Detect high level

GPIB2: MPIO_B2 Pin, GPIO Input Data

0: Detect low level

1: Detect high level

GPIB1: MPIO_B1 Pin, GPIO Input Data

0: Detect low level

1: Detect high level

GPIB0: MPIO_B0 Pin, GPIO Input Data

0: Detect low level

1: Detect high level

GPIA3: MPIO_A3 Pin, GPIO Input Data

0: Detect low level

1: Detect high level

GPIA2: MPIO_A2 Pin, GPIO Input Data

0: Detect low level

1: Detect high level

GPIA1: MPIO_A1 Pin, GPIO Input Data

0: Detect low level

1: Detect high level

GPIA0: MPIO_A0 Pin, GPIO Input Data

0: Detect low level

1: Detect high level

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7.5.60 GPIO Input Data Register for MPIO_C Register (address = 7Eh) [reset = N/A]

図 7-92. GPIO Input Data Register for MPIO_C Register

7	6	5	4	3	2	1	0
RSV	RSV	RSV	RSV	GPIC3	GPIC2	GPIC1	GPIC0
N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

GPIC3: MPIO_C3 Pin, GPIO Input Data

0: Detect low level

1: Detect high level

GPIC2: MPIO_C2 Pin, GPIO Input Data

0: Detect low level

1: Detect high level

GPIC1: MPIO_C1 Pin, GPIO Input Data

0: Detect low level

1: Detect high level

GPIC0: MPIO_C0 Pin, GPIO Input Data

0: Detect low level

1: Detect high level

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Typical Circuit Connection

図 8-1 shows a typical circuit connection.

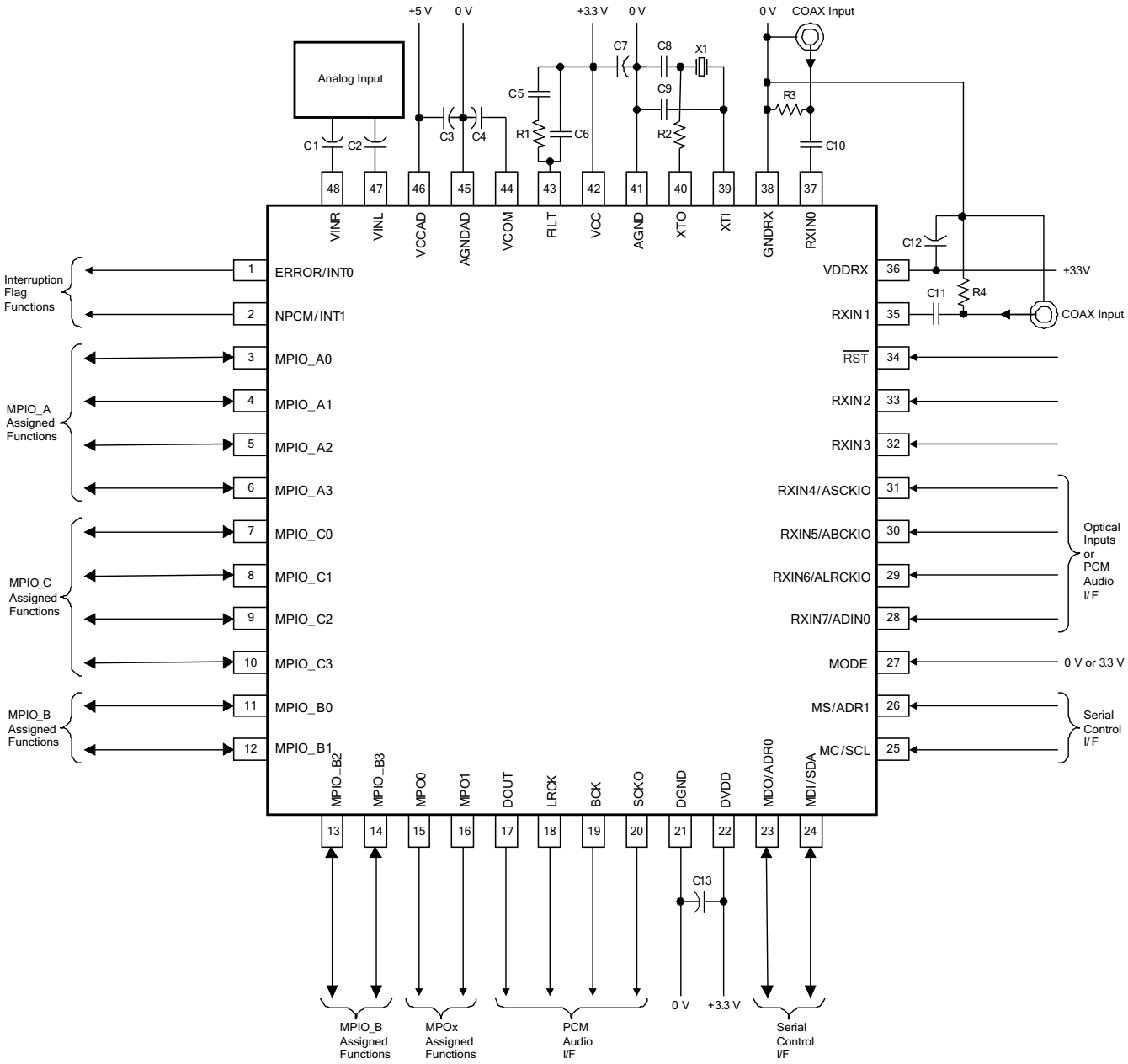

図 8-1. Typical Circuit Connection

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表 8-1 identifies the components labeled in 図 8-1.

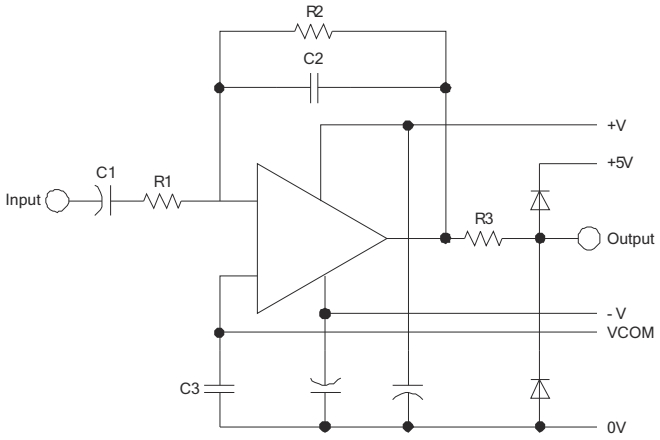
表 8-1. Typical Circuit Components

LABEL	DESCRIPTION	VALUE
R1	Loop filter resistor	680 Ω
R2	Current-limiting resistor	100 to 500 Ω(1)
R3, R4	Coax input termination resistor	75 Ω
C1, C2	Electrolytic capacitor	4.7 µF(2)
C3, C7, C12, C13	Ceramic capacitor	0.1 µF(3)
	Electrolytic capacitor	10 µF(3)
C4	Ceramic capacitor	0.1 µF
	Electrolytic capacitor	10 µF
C5	Loop filter capacitor	0.068 mF
C6	Loop filter capacitor	0.0047 mF
C8, C9	OSC load capacitor	10 to 30 pF(4)
C10, C11	DC blocking capacitor for coax input	0.1 µF
X1	Crystal resonator	24.576 MHz(5)

(1) This is the typical range, but it depends on the crystal resonator.
(2) This value is recommended for 3-Hz cutoff frequency.
(3) This value depends on the power supply.
(4) This is the typical range, but it depends on the crystal resonator and the PCB layout.
(5) Use a fundamental resonator of this size when the XTI clock source is needed.

8.1.2 Application Example for Analog Input

図 8-2 shows an example of V_{COM} biased buffering for 2-V_{RMS} input with overvoltage protection.



Example of C and R values with gain (G) and corner frequency (f_C): R1 = 20 kΩ R2 = 10 kΩ R3 = 1 kΩ C1 = 10 µF C2 = 330 pF C3 = 0.1 µF G = 0.5 f_C = 48 kHz

図 8-2. V_{COM} Biased Buffering Example

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8.2 Typical Application

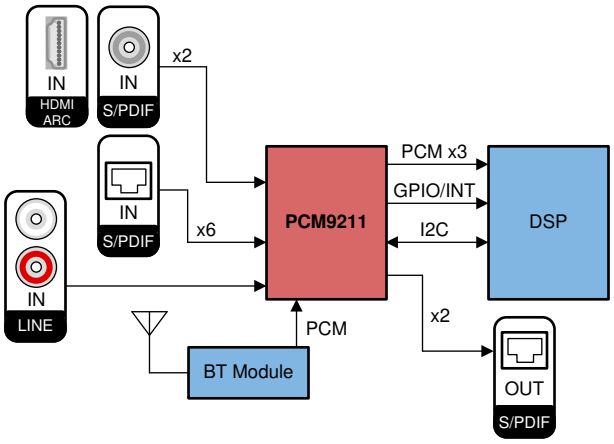

図 8-3. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-2 as the input parameters.

表 8-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Audio Input	PCM, COAX S/PDIF, Optical S/PDIF, 2 ch Single Ended Analog
Audio Output	PCM, S/PDIF
Control	Host I^2C

8.2.2 Detailed Design Procedure

8.2.2.1 S/PDIF Ports

The PCM9211 has total of 12 single ended S/PDIF inputs and 2 of these S/PDIF inputs have built in COAX amplifiers. These S/PDIF inputs are MUXed to one DIR. MPIO_A provides 4 of the 12 S/PDIF inputs, but can also be configured to be an additional I2S input for other applications.

There are two S/PDIF outputs available in the MPO port; MPO0 and MPO1 output can be selected independently. The MPO pins are also able to output DIR flag information, interrupt flags, or to repeat S/PDIF signals selected for the RECOUT0 or RECOUT1 paths.

In this application there are 8 total S/PDIF inputs available (2 with integrated COAX amplifiers) due to RXIN4-RXIN7 being used for a PCM input on AUXIN0.

8.2.2.2 PCM Ports

The PCM9211 can have up to 3 PCM inputs at one time or up to 3 PCM outputs at one time. Each PCM port can be configured top select the data output on the pins, and some such as MPIO_B can be either an input or an output. MPIO_C can be the PCM output for the ADC or a PCM input. In this application the Main Output Port, MPIO_B and MPIO_C are PCM outputs, while AUXIN0 (RXIN4 –RXIN7) is utilized as a PCM input.

8.2.2.3 ADC Operation

In this application, the ADC is operating in standalone mode. This means that the ADC is acting as a master and outputting PCM data on the MPIO_C port.

8.2.2.4 GPIO/Interrupts

The Error/Int0 and NPCM/Int1 pins can be programmed to output flags for various internal flags masked or unmasked in the registers. This can include DIR flags, ADC flags, or port flags.

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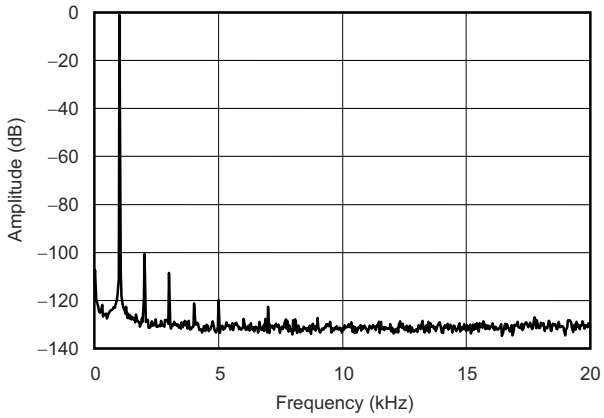
8.2.3 Application Curve



–1 dB, N = 32,768

図 8-4. Output Spectrum

9 Power Supply Recommendations

The PCM9211 requires 3.3-V nominal rails and a 5-V nominal rail. At least one 3.3-V supply is needed for VCC, VDD, and VDDRX. For best performance, separate 3.3-V rails are recommended for each power pin. A 5-V supply is needed for the VCCAD rail that supplies the ADC circuitry. Place the decoupling capacitors for the power supplies close to the device terminals.

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10 Layout

10.1 Layout Guidelines

It is strongly recommend to use one ground plane for the PCM9211 as the internal ground partitions are not connected. While using one ground plane, it is best to make sure that analog and digital circuitry be sufficiently partitioned on the PCB so that analog and digital return currents do not cross.

- Decoupling caps should be placed as close to power pins as possible (VCC, VDD, VDDRX, VCCAD).
- 24.576-MHz crystal should be placed as close to XTI and XTO pins as possible, the resistor value is generally between 100 Ω to 500 Ω depending on crystal; and load capacitors are generally between 10 pF to 30 pF, depending on crystal.
- Further guidelines can be found in 図 10-1.

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10.2 Layout Example

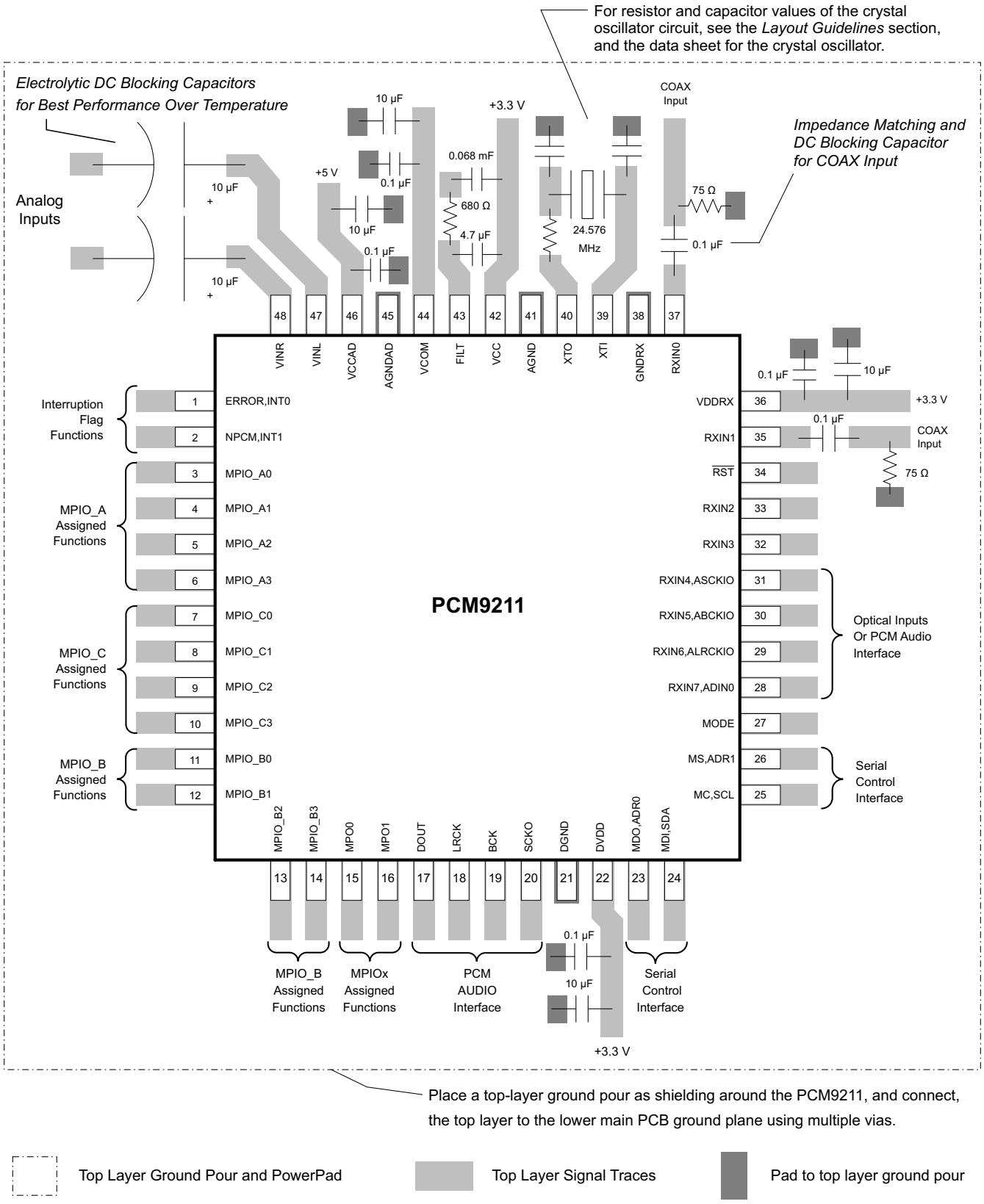

図 10-1. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *PCM9211EVM: PCM9211 Evaluation Module with CodecControl Software* user's guide
- Texas Instruments, *PCM9211EVM Record and Playback via USB Interface* application report
- Texas Instruments, *PurePath™ Console Motherboard* user's guide

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCM9211PT	Active	Production	LQFP (PT) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM9211
PCM9211PT.B	Active	Production	LQFP (PT) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM9211
PCM9211PTR	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM9211
PCM9211PTR.B	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM9211

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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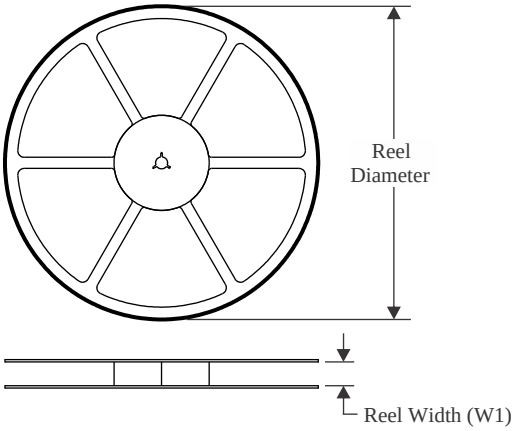
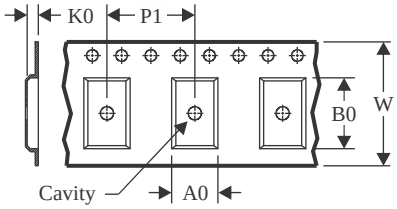
TAPE AND REEL INFORMATION

REEL DIMENSIONS

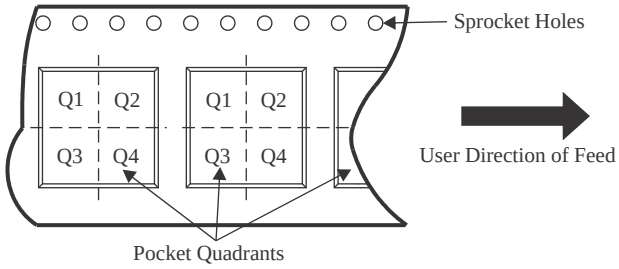


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

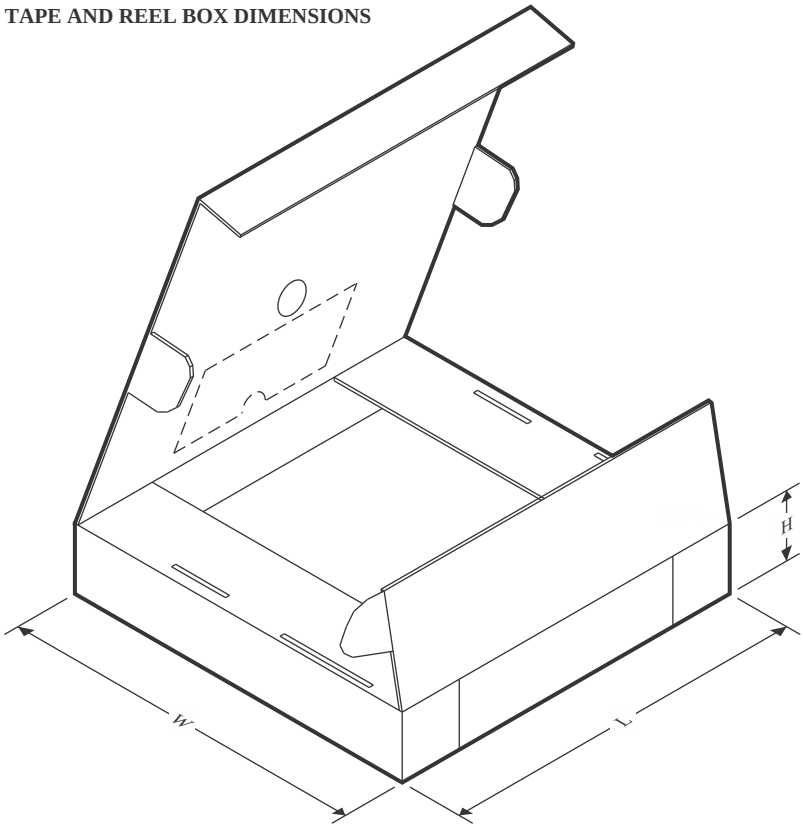
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM9211PTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

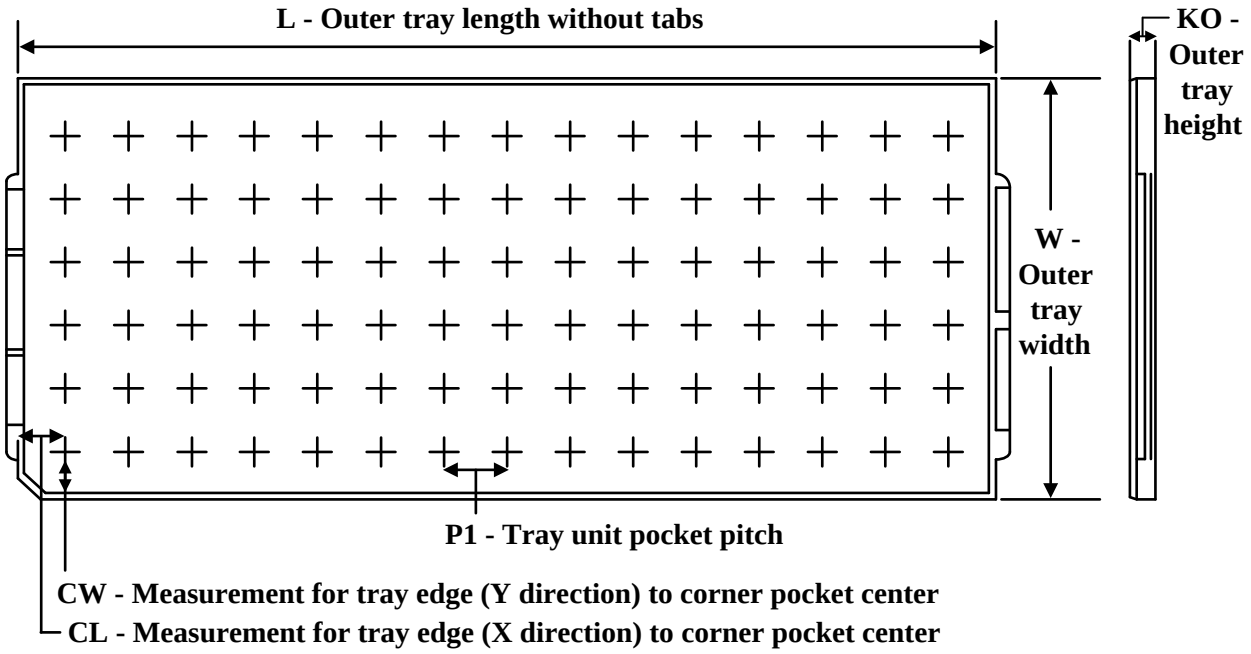
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM9211PTR	LQFP	PT	48	1000	350.0	350.0	43.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

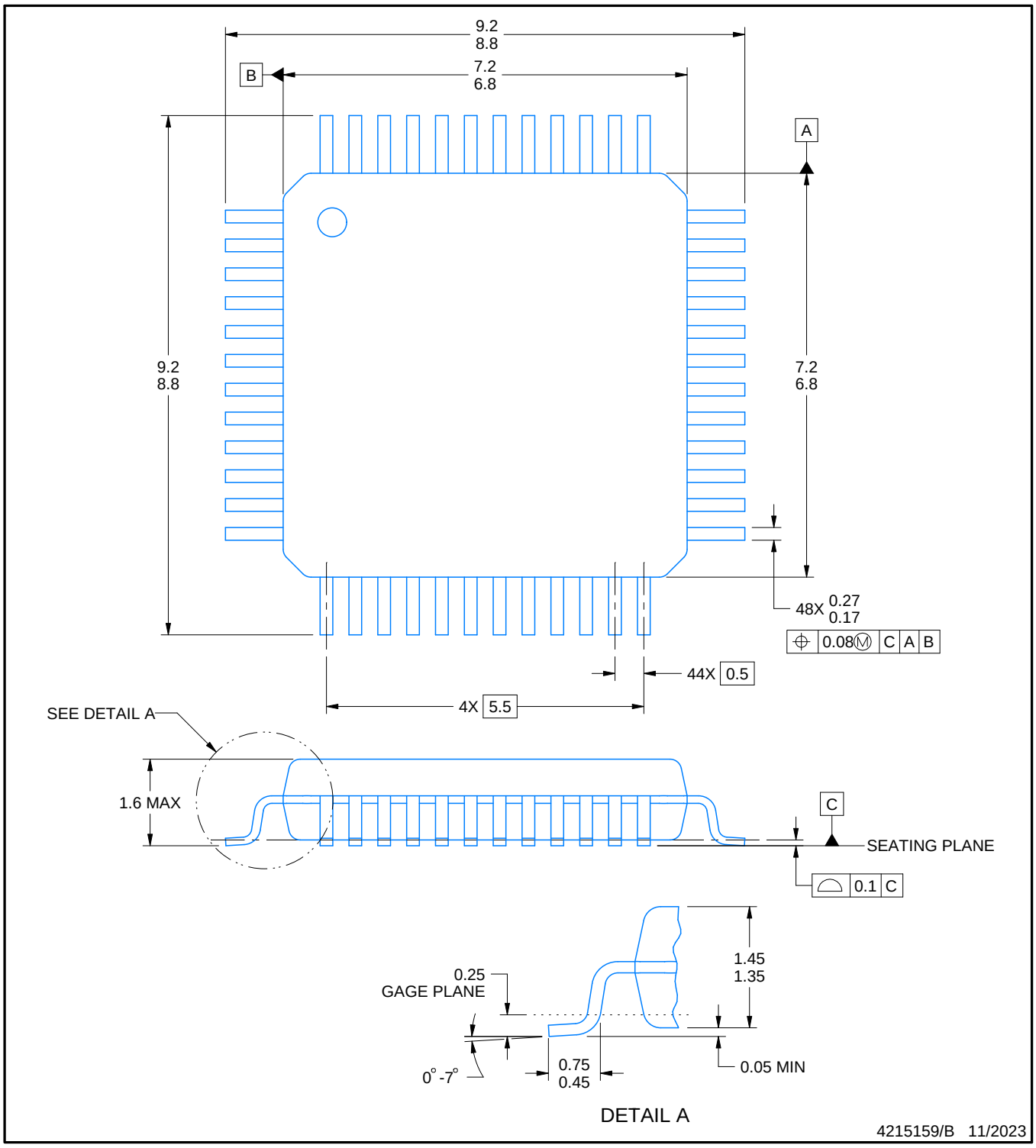
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
PCM9211PT	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
PCM9211PT.B	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

PACKAGE OUTLINE

PT0048A

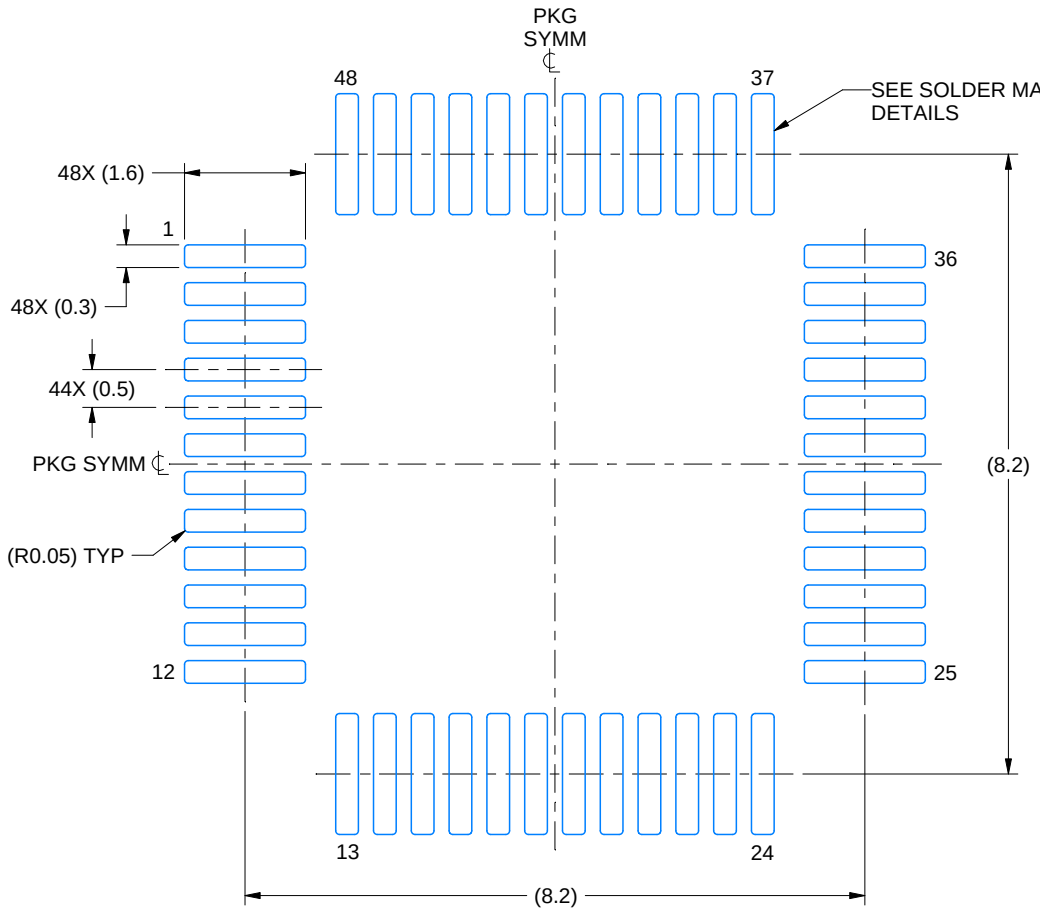
LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK

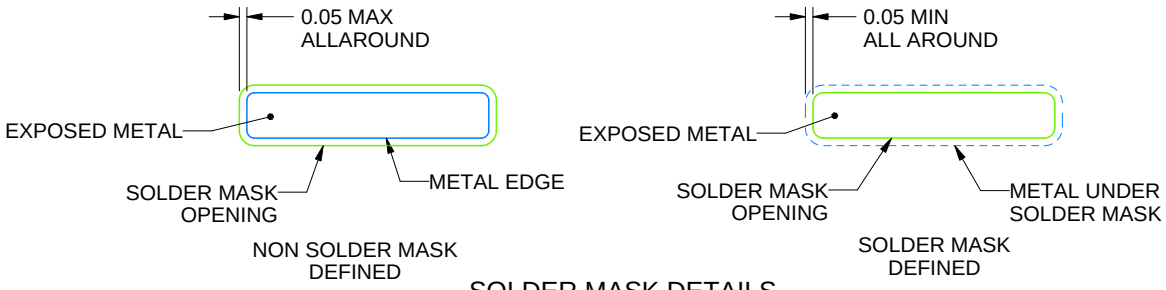


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads conected to the die pads.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000

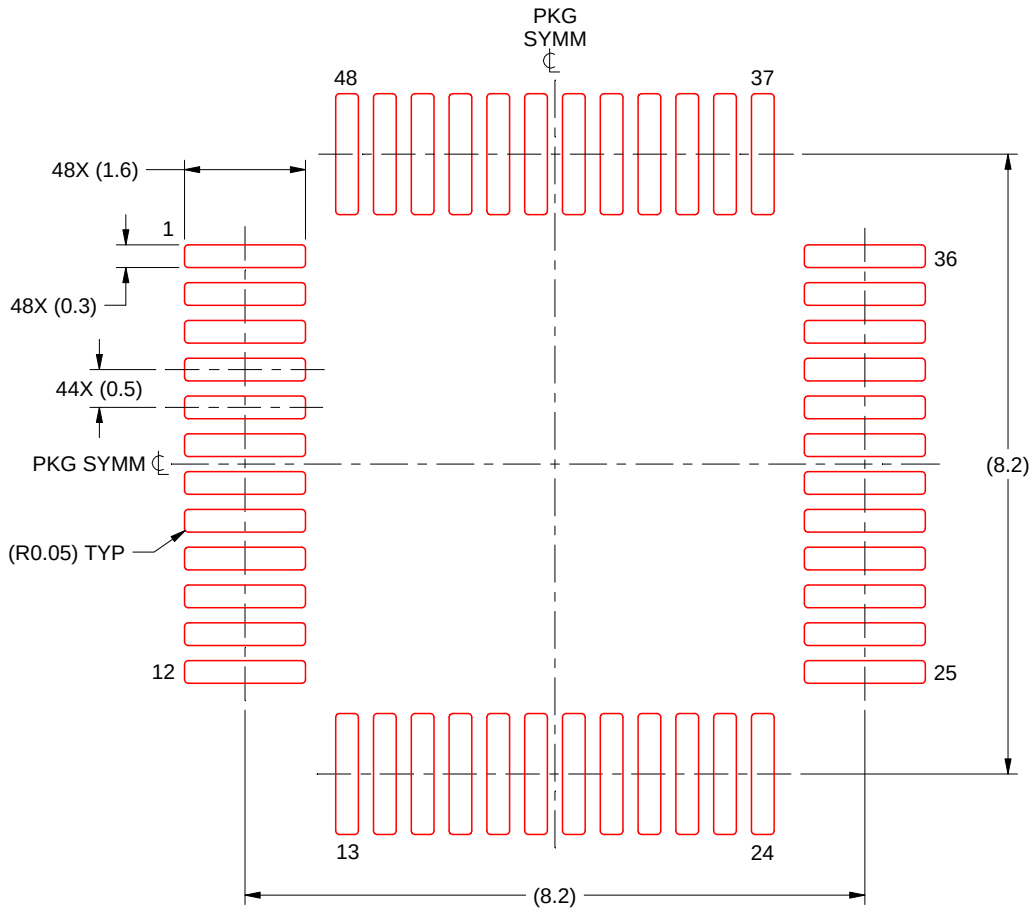


SOLDER MASK DETAILS

4215159/B 11/2023

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

4215159/B 11/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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