

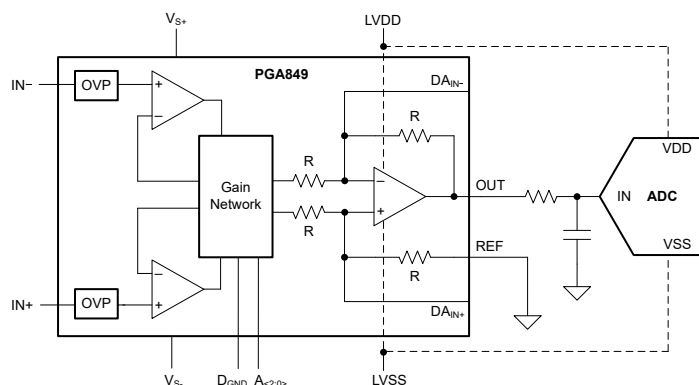
# PGA849 低ノイズ、広帯域、高精度プログラマブルゲイン計測アンプ

## 1 特長

- 差動→シングルエンド変換
- 8つのピンプログラマブルバイナリゲイン
  - $G(V/V) = 1/8, 1/4, 1/2, 1, 2, 4, 8, \text{および } 16$
- "Low" ゲイン誤差ドリフト:  $\pm 2\text{ppm}/^\circ\text{C}$  (最大値)
- 高速信号処理:
  - 広い帯域幅: 10MHz (すべてのゲイン)
  - 高いスループート:  $35\text{V}/\mu\text{s}$  ( $G \geq 1/2 V/V$  時)
  - セトリングタイム:
    - 0.01% まで 700ns, 0.0015% まで 950ns
  - 入力段ノイズ:  $G = 16\text{V}/V$  時に  $8.6\text{nV}/\sqrt{\text{Hz}}$
  - SNRを向上させるフィルタオプション
- 高低の電源電圧に対して  $\pm 40\text{V}$  までの入力過電圧保護機能
- 入力段電源電圧範囲:
  - シングル電源:  $8\text{V} \sim 36\text{V}$
  - デュアル電源:  $\pm 4\text{V} \sim \pm 18\text{V}$
- 独立した出力電源ピン
- 出力段電源電圧範囲:
  - シングル電源:  $4.5\text{V} \sim 36\text{V}$
  - デュアル電源:  $\pm 2.25\text{V} \sim \pm 18\text{V}$
- 仕様温度範囲:  $-40^\circ\text{C} \sim +125^\circ\text{C}$
- 小型パッケージ:  $3\text{mm} \times 3\text{mm}$  QFN

## 2 アプリケーション

- ファクトリオートメーション / 制御
- アナログ入力モジュール
- データアキュイジション (DAQ)
- 試験および測定機器
- パラメトリック測定ユニット (PMU)



PGA849 のアプリケーション概略図

## 3 概要

PGA849 は、差動からシングルエンドへの変換を行う、広帯域幅で低ノイズのプログラマブルゲイン計測アンプです。PGA849 は、3本のデジタルゲイン選択ピンを使用して、 $0.125\text{V}/V$  の減衰ゲインから最大  $16\text{V}/V$  まで、8つのバイナリゲイン設定を備えています。

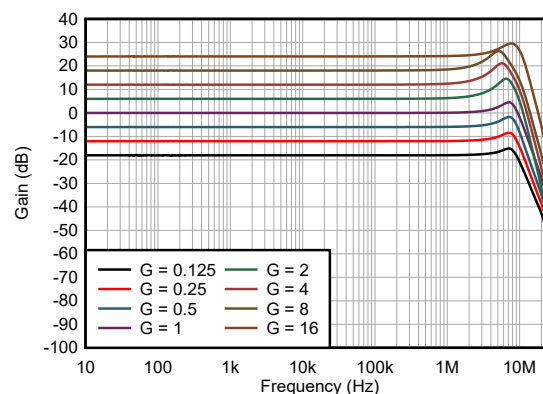
PGA849 アーキテクチャは、追加の ADC ドライバを必要とせずに、最大  $1\text{MSPS}$  のサンプリングレートで高分解能、高精度の A/D コンバータ (ADC) の入力を駆動するように最適化されています。出力段の電源は入力段から分離され、ADC または下流側のデバイスをオーバードライブの損傷から保護します。

スーパーベータ入力トランジスタが提供する入力バイアス電流は非常に低く、それにより入力電流ノイズ密度が  $0.3\text{pA}/\sqrt{\text{Hz}}$  と非常に低くなるため、PGA849 は、事実上あらゆる種類のセンサに対応する汎用性の高い選択肢になっています。低ノイズの電流フィードバックフロントエンドアーキテクチャにより、高周波数でも優れたゲイン平坦性を実現しているため、PGA849 は、優れた高インピーダンスのセンサ読み出しデバイスとなります。入力ピンに保護回路が内蔵されており、電源電圧を最大  $\pm 40\text{V}$  上回る過電圧に対処できます。

### パッケージ情報

| 部品番号   | パッケージ (1)      | パッケージサイズ (2)                   |
|--------|----------------|--------------------------------|
| PGA849 | RGT (VQFN, 16) | $3\text{mm} \times 3\text{mm}$ |

- 詳細については、[セクション 11](#) を参照してください。
- パッケージサイズ (長さ  $\times$  幅) は公称値であり、該当する場合はピンも含まれます。



ゲインと周波数との関係



## Table of Contents

|                                                |           |                                                                  |           |
|------------------------------------------------|-----------|------------------------------------------------------------------|-----------|
| <b>1 特長</b> .....                              | <b>1</b>  | <b>8 Application and Implementation</b> .....                    | <b>23</b> |
| <b>2 アプリケーション</b> .....                        | <b>1</b>  | 8.1 Application Information.....                                 | 23        |
| <b>3 概要</b> .....                              | <b>1</b>  | 8.2 Typical Applications.....                                    | 25        |
| <b>4 Device Comparison Table</b> .....         | <b>2</b>  | 8.3 Power Supply Recommendations.....                            | 28        |
| <b>5 Pin Configuration and Functions</b> ..... | <b>3</b>  | 8.4 Layout.....                                                  | 28        |
| <b>6 Specifications</b> .....                  | <b>4</b>  | <b>9 Device and Documentation Support</b> .....                  | <b>30</b> |
| 6.1 Absolute Maximum Ratings.....              | 4         | 9.1 Device Support.....                                          | 30        |
| 6.2 ESD Ratings .....                          | 4         | 9.2 Documentation Support.....                                   | 30        |
| 6.3 Recommended Operating Conditions.....      | 4         | 9.3 ドキュメントの更新通知を受け取る方法.....                                      | 30        |
| 6.4 Thermal Information.....                   | 4         | 9.4 サポート・リソース.....                                               | 30        |
| 6.5 Electrical Characteristics.....            | 5         | 9.5 Trademarks.....                                              | 30        |
| 6.6 Typical Characteristics.....               | 8         | 9.6 静電気放電に関する注意事項.....                                           | 31        |
| <b>7 Detailed Description</b> .....            | <b>19</b> | 9.7 用語集.....                                                     | 31        |
| 7.1 Overview.....                              | 19        | <b>10 Revision History</b> .....                                 | <b>31</b> |
| 7.2 Functional Block Diagram.....              | 19        | <b>11 Mechanical, Packaging, and Orderable Information</b> ..... | <b>31</b> |
| 7.3 Feature Description.....                   | 20        |                                                                  |           |
| 7.4 Device Functional Modes.....               | 22        |                                                                  |           |

## 4 Device Comparison Table

| DEVICE                 | OUTPUT TYPE  | GAIN (V/V)                    | BANDWIDTH (MHz) | SLEW RATE (V/<br>μS) | NOISE (nV/rtHz) |
|------------------------|--------------|-------------------------------|-----------------|----------------------|-----------------|
| <a href="#">PGA849</a> | Single-ended | 1/8, 1/4, 1/2, 1, 2, 4, 8, 16 | 10              | 35                   | 8.6             |
| <a href="#">INA849</a> | Single-ended | G = 1 + 6kΩ / RG              | 28              | 35                   | 1               |
| <a href="#">PGA855</a> | Differential | 1/8, 1/4, 1/2, 1, 2, 4, 8, 16 | 10              | 35                   | 7.8             |
| <a href="#">INA851</a> | Differential | G = 1 + 6kΩ / RG              | 22              | 37                   | 3.2             |
| <a href="#">INA821</a> | Single-ended | G = 1 + 49.4kΩ / RG           | 4.7             | 2                    | 7               |
| <a href="#">INA819</a> | Single-ended | G = 1 + 50kΩ / RG             | 2               | 0.9                  | 8               |

## 5 Pin Configuration and Functions

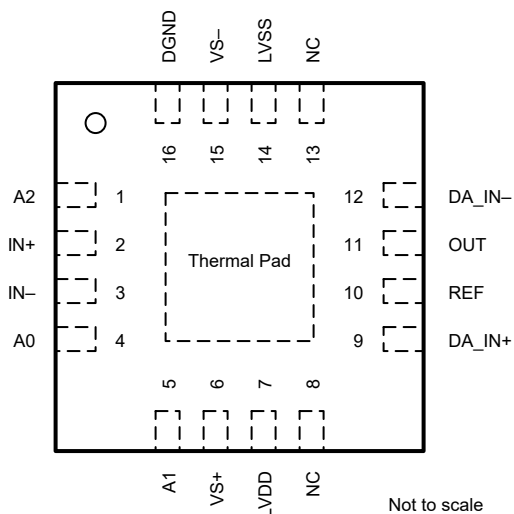


図 5-1. RGT Package, 16-Pin VQFN (Top View)

表 5-1. Pin Functions

| PIN         |             | TYPE   | DESCRIPTION                                                                                                                                                                                                                               |
|-------------|-------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME        | NO.         |        |                                                                                                                                                                                                                                           |
| A0          | 4           | Input  | Gain option pin 0                                                                                                                                                                                                                         |
| A1          | 5           | Input  | Gain option pin 1                                                                                                                                                                                                                         |
| A2          | 1           | Input  | Gain option pin 2                                                                                                                                                                                                                         |
| DA_IN+      | 9           | Input  | Connection to output difference amplifier summing node                                                                                                                                                                                    |
| DA_IN–      | 12          | Input  | Connection to output difference amplifier summing node                                                                                                                                                                                    |
| DGND        | 16          | Power  | Ground reference for digital-logic and gain-setting pins                                                                                                                                                                                  |
| IN–         | 3           | Input  | Negative (inverting) input                                                                                                                                                                                                                |
| IN+         | 2           | Input  | Positive (noninverting) input                                                                                                                                                                                                             |
| LVDD        | 7           | Power  | Output-driver positive supply                                                                                                                                                                                                             |
| LVSS        | 14          | Power  | Output-driver negative supply                                                                                                                                                                                                             |
| NC          | 8           | —      | Do not connect                                                                                                                                                                                                                            |
| NC          | 13          | —      | Do not connect                                                                                                                                                                                                                            |
| OUT         | 11          | Output | Output                                                                                                                                                                                                                                    |
| REF         | 10          | Input  | Reference input. This pin must be driven by a low-impedance source                                                                                                                                                                        |
| VS+         | 6           | Power  | Input-stage positive supply                                                                                                                                                                                                               |
| VS–         | 15          | Power  | Input-stage negative supply                                                                                                                                                                                                               |
| Thermal Pad | Thermal pad | —      | The thermal pad must be soldered to the printed-circuit board (PCB). Connect thermal pad to a plane or large copper pour that is either floating or electrically connected to VS–, even for applications that have low power dissipation. |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|            |                                                                         | MIN              | MAX              | UNIT |
|------------|-------------------------------------------------------------------------|------------------|------------------|------|
| $V_S$      | Supply voltage on $V_{S+}$ , $V_{S-}$ pins; $V_S = (V_{S+}) - (V_{S-})$ | 0                | 40               | V    |
| $V_{SOUT}$ | Supply voltage on LVDD, LVSS pins; $V_{SOUT} = V_{LVDD} - V_{LVSS}$     | 0                | 40               | V    |
|            | Voltage on power pins LVDD, LVSS                                        | $(V_{S-}) - 0.5$ | $(V_{S+}) + 0.5$ | V    |
| $V_{IN}$   | Voltage on signal-input pins $IN+$ , $IN-$                              | $(V_{S-}) - 40$  | $(V_{S+}) + 40$  | V    |
|            | DGND, DA_IN+, DA_IN– pin voltage                                        | $(V_{S-}) - 0.5$ | $(V_{S+}) + 0.5$ | V    |
|            | Voltage on gain-select pins A2, A1, A0                                  | $V_{DGND} - 0.5$ | $(V_{S+}) + 0.5$ | V    |
| $V_O$      | Signal output pin maximum voltage                                       | $V_{LVSS} - 0.5$ | $V_{LVDD} + 0.5$ | V    |
| $V_{REF}$  | Reference input voltage                                                 | $V_{LVSS} - 0.5$ | $V_{LVDD} + 0.5$ | V    |
| $I_O$      | Signal-output pins current                                              | –100             | 100              | mA   |
| $I_{SC}$   | Output short-circuit current <sup>(2)</sup>                             | Continuous       |                  |      |
| $T_A$      | Operating temperature                                                   | –50              | 150              | °C   |
| $T_J$      | Junction Temperature                                                    |                  | 175              | °C   |
| $T_{stg}$  | Storage Temperature                                                     | –65              | 150              | °C   |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Short-circuit to  $V_{SOUT} / 2$ .

### 6.2 ESD Ratings

|             |                         |                                                                       | VALUE | UNIT |
|-------------|-------------------------|-----------------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>     | ±2000 | V    |
|             |                         | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup> | ±1000 |      |

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|            |                             |               | MIN   | MAX | UNIT |
|------------|-----------------------------|---------------|-------|-----|------|
| $V_S$      | Input stage supply voltage  | Single supply | 8     | 36  | V    |
|            |                             | Dual supply   | ±4    | ±18 |      |
| $V_{SOUT}$ | Output stage supply voltage | Single supply | 4.5   | 36  | V    |
|            |                             | Dual supply   | ±2.25 | ±18 |      |
| $T_A$      | Specified temperature       |               | –40   | 125 | °C   |

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | PGA849     | UNIT |
|-------------------------------|----------------------------------------------|------------|------|
|                               |                                              | RGT (VQFN) |      |
|                               |                                              | 16 PINS    |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 47.3       | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 53.6       | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 22.0       | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 1.4        | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 22.0       | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | 7.8        | °C/W |

- (1) For information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 6.5 Electrical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{\text{SOUT}} = \pm 15\text{V}$ ,  $V_{\text{ICM}} = 0\text{V}$ ,  $V_{\text{REF}} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to ground, and  $G = 1\text{V/V}$  (unless otherwise noted)

| PARAMETER        |                              | TEST CONDITIONS                                                                        |           | MIN                      | TYP                      | MAX      | UNIT  |
|------------------|------------------------------|----------------------------------------------------------------------------------------|-----------|--------------------------|--------------------------|----------|-------|
| INPUT            |                              |                                                                                        |           |                          |                          |          |       |
| V <sub>OS</sub>  | Offset voltage (RTI)         | G = 1 to 16                                                                            |           | ±50                      | ±350                     | μV       |       |
|                  |                              | G < 1                                                                                  |           | ±50/G                    | ±350/G                   |          |       |
|                  | Offset voltage drift (RTI)   | G = 1 to 16, T <sub>A</sub> = −40°C to +125°C                                          |           | ±0.2                     | ±1.0                     | μV/°C    |       |
|                  |                              | G < 1, T <sub>A</sub> = −40°C to +125°C                                                |           | ±0.2/G                   | ±1.0/G                   |          |       |
| PSRR             | Power-supply rejection ratio | ±4V ≤ V <sub>S</sub> ≤ ±18V, RTI                                                       | G = 0.125 | 95                       | 110                      | dB       |       |
|                  |                              |                                                                                        | G = 0.25  | 98                       | 114                      |          |       |
|                  |                              |                                                                                        | G = 0.5   | 100                      | 118                      |          |       |
|                  |                              |                                                                                        | G = 1     | 120                      | 134                      |          |       |
|                  |                              |                                                                                        | G = 2     | 120                      | 126                      |          |       |
|                  |                              |                                                                                        | G = 4     | 120                      | 132                      |          |       |
|                  |                              |                                                                                        | G = 8     | 120                      | 136                      |          |       |
|                  |                              |                                                                                        | G = 16    | 120                      | 140                      |          |       |
| Z <sub>id</sub>  | Differential input impedance |                                                                                        |           | 1    1                   |                          | GΩ    pF |       |
| Z <sub>ic</sub>  | Common-mode input impedance  |                                                                                        |           | 1    7                   |                          | GΩ    pF |       |
| V <sub>ICM</sub> | Common-mode input voltage    | V <sub>S</sub> = ±4V to ±18V                                                           |           | (V <sub>S−</sub> ) + 2.5 | (V <sub>S+</sub> ) − 2   | V        |       |
|                  |                              | V <sub>S</sub> = ±4V to ±18V, T <sub>A</sub> = −40°C to +125°C                         |           | (V <sub>S−</sub> ) + 3   | (V <sub>S+</sub> ) − 2.5 |          |       |
| CMRR             | Common-mode rejection ratio  | At DC to 60Hz,<br>V <sub>ICM</sub> = ±10V,<br>T <sub>A</sub> = −40°C to +125°C,<br>RTI | G = 0.125 | 64                       | 82                       | dB       |       |
|                  |                              |                                                                                        | G = 0.25  | 70                       | 88                       |          |       |
|                  |                              |                                                                                        | G = 0.5   | 76                       | 94                       |          |       |
|                  |                              |                                                                                        | G = 1     | 82                       | 100                      |          |       |
|                  |                              |                                                                                        | G = 2     | 88                       | 106                      |          |       |
|                  |                              |                                                                                        | G = 4     | 94                       | 112                      |          |       |
|                  |                              |                                                                                        | G = 8     | 100                      | 118                      |          |       |
|                  |                              |                                                                                        | G = 16    | 106                      | 124                      |          |       |
| BIAS CURRENT     |                              |                                                                                        |           |                          |                          |          |       |
| I <sub>B</sub>   | Input bias current           |                                                                                        |           | ±0.5                     | ±1.8                     | nA       |       |
|                  |                              | T <sub>A</sub> = −40°C to +125°C                                                       |           | ±1                       |                          |          |       |
|                  | Input bias current drift     | T <sub>A</sub> = −40°C to +125°C                                                       |           |                          |                          | ±10      | pA/°C |
| I <sub>OS</sub>  | Input offset current         |                                                                                        |           | ±0.5                     | ±1                       | nA       |       |
|                  |                              | T <sub>A</sub> = −40°C to +125°C                                                       |           | ±1                       |                          |          |       |
|                  | Input offset current drift   | T <sub>A</sub> = −40°C to +125°C                                                       |           |                          |                          | ±10      | pA/°C |

## 6.5 Electrical Characteristics (続き)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{\text{SOUT}} = \pm 15\text{V}$ ,  $V_{\text{ICM}} = 0\text{V}$ ,  $V_{\text{REF}} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to ground, and  $G = 1\text{V/V}$  (unless otherwise noted)

| PARAMETER          |                             | TEST CONDITIONS                                                                  |                                  | MIN                     | TYP                     | MAX              | UNIT |
|--------------------|-----------------------------|----------------------------------------------------------------------------------|----------------------------------|-------------------------|-------------------------|------------------|------|
| NOISE VOLTAGE      |                             |                                                                                  |                                  |                         |                         |                  |      |
| e <sub>NI</sub>    | Voltage noise density (RTI) | f = 1kHz                                                                         | G = 16                           | 8.6                     |                         | nV/√Hz           |      |
|                    |                             |                                                                                  | G = 8                            | 8.8                     |                         |                  |      |
|                    |                             |                                                                                  | G = 4                            | 9.6                     |                         |                  |      |
|                    |                             |                                                                                  | G = 2                            | 13.5                    |                         |                  |      |
|                    |                             |                                                                                  | G = 1                            | 23.8                    |                         |                  |      |
|                    |                             |                                                                                  | G = 0.5                          | 47.4                    |                         |                  |      |
|                    |                             |                                                                                  | G = 0.25                         | 94.9                    |                         |                  |      |
|                    |                             |                                                                                  | G = 0.125                        | 186.3                   |                         |                  |      |
| E <sub>NI</sub>    | Voltage noise (RTI)         | f <sub>B</sub> = 0.1Hz to 10Hz                                                   | G = 16                           | 0.28                    |                         | μV <sub>PP</sub> |      |
|                    |                             |                                                                                  | G = 8                            | 0.29                    |                         |                  |      |
|                    |                             |                                                                                  | G = 4                            | 0.33                    |                         |                  |      |
|                    |                             |                                                                                  | G = 2                            | 0.49                    |                         |                  |      |
|                    |                             |                                                                                  | G = 1                            | 0.91                    |                         |                  |      |
|                    |                             |                                                                                  | G = 0.5                          | 1.82                    |                         |                  |      |
|                    |                             |                                                                                  | G = 0.25                         | 3.59                    |                         |                  |      |
|                    |                             |                                                                                  | G = 0.125                        | 7.28                    |                         |                  |      |
| i <sub>N</sub>     | Input current noise density | f = 1kHz                                                                         | 0.3                              |                         | pA/√Hz                  |                  |      |
| I <sub>N</sub>     | Input current noise         | f <sub>B</sub> = 0.1Hz to 10Hz                                                   | 13                               |                         | pA <sub>PP</sub>        |                  |      |
| GAIN               |                             |                                                                                  |                                  |                         |                         |                  |      |
|                    | Gain range                  |                                                                                  |                                  | 0.125                   | 16                      | V/V              |      |
| GE                 | Gain error                  | G = 0.125                                                                        | ±0.010                           |                         | ±0.045                  | %                |      |
|                    |                             | G = 0.25                                                                         | ±0.005                           |                         | ±0.030                  | %                |      |
|                    |                             | G = 0.5                                                                          | ±0.005                           |                         | ±0.030                  | %                |      |
|                    |                             | G = 1                                                                            | ±0.005                           |                         | ±0.015                  | %                |      |
|                    |                             | G = 2                                                                            | ±0.010                           |                         | ±0.030                  | %                |      |
|                    |                             | G = 4                                                                            | ±0.015                           |                         | ±0.040                  | %                |      |
|                    |                             | G = 8                                                                            | ±0.015                           |                         | ±0.040                  | %                |      |
|                    |                             | G = 16                                                                           | ±0.030                           |                         | ±0.070                  | %                |      |
|                    | Gain nonlinearity           | G = 0.125 to 16, V <sub>OUT</sub> > ±5V                                          |                                  | 2                       | 5                       | ppm              |      |
|                    | Gain drift                  | G = 0.125 to 16, T <sub>A</sub> = −40°C to +125°C                                |                                  | ±1                      | ±2                      | ppm/°C           |      |
| OUTPUT             |                             |                                                                                  |                                  |                         |                         |                  |      |
| V <sub>OUT</sub>   | Output voltage              | No load                                                                          | V <sub>SOUT</sub> = ±2.25V       | V <sub>LVSS</sub> + 0.1 | V <sub>LVDD</sub> − 0.1 | V                |      |
|                    |                             | R <sub>L</sub> = 10kΩ                                                            | V <sub>SOUT</sub> = ±2.25V       | V <sub>LVSS</sub> + 0.2 | V <sub>LVDD</sub> − 0.2 |                  |      |
|                    |                             |                                                                                  | V <sub>SOUT</sub> = ±18V         | V <sub>LVSS</sub> + 0.4 | V <sub>LVDD</sub> − 0.4 |                  |      |
| C <sub>L</sub>     | Load capacitance            | Stable operation for capacitive load                                             |                                  | 100                     |                         | pF               |      |
| I <sub>SC</sub>    | Short-circuit current       | Continuous to V <sub>SOUT</sub> / 2                                              |                                  | ±45                     |                         | mA               |      |
|                    |                             |                                                                                  | T <sub>A</sub> = −40°C to +125°C | ±20                     | ±60                     |                  |      |
| FREQUENCY RESPONSE |                             |                                                                                  |                                  |                         |                         |                  |      |
| BW                 | Bandwidth, −3dB             | G = 0.125 to 16                                                                  |                                  | 10                      |                         | MHz              |      |
| SR                 | Slew rate                   | G ≥ 0.5, V <sub>OUT</sub> = 10                                                   |                                  | 35                      |                         | V/μs             |      |
|                    |                             | G = 0.25, V <sub>OUT</sub> = 5                                                   |                                  | 23                      |                         | V/μs             |      |
|                    |                             | G = 0.125, V <sub>OUT</sub> = 2.5                                                |                                  | 10                      |                         | V/μs             |      |
| t <sub>S</sub>     | Settling time               | G = 0.125 to 16<br>V <sub>INDIFF</sub> = 10V step or V <sub>OUT</sub> = 10V step | To 0.01%                         | 0.7                     |                         | μs               |      |
|                    |                             |                                                                                  | To 0.0015%                       | 0.95                    |                         |                  |      |
|                    | Gain switching time         |                                                                                  |                                  | 2                       |                         | μs               |      |

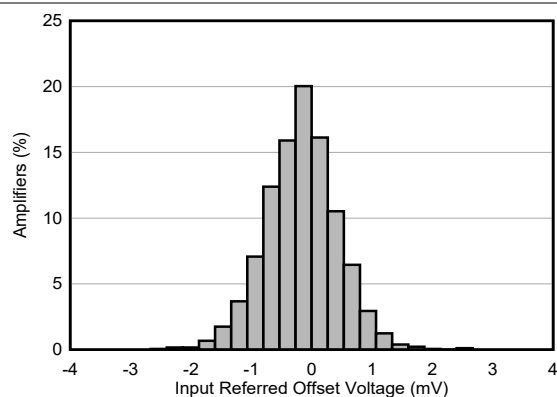
## 6.5 Electrical Characteristics (続き)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{SOUT} = \pm 15\text{V}$ ,  $V_{ICM} = 0\text{V}$ ,  $V_{REF} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to ground, and  $G = 1\text{V/V}$  (unless otherwise noted)

| PARAMETER                 |                                                                    | TEST CONDITIONS                                                     | MIN                     | TYP  | MAX                     | UNIT |
|---------------------------|--------------------------------------------------------------------|---------------------------------------------------------------------|-------------------------|------|-------------------------|------|
| THD+N                     | Total harmonic distortion and Noise                                | Differential input, f = 10kHz, V <sub>OUT</sub> = 10V <sub>PP</sub> |                         | –110 |                         | dB   |
|                           |                                                                    | Single-ended input, f = 10kHz, V <sub>OUT</sub> = 10V <sub>PP</sub> |                         | –105 |                         |      |
| HD2                       | Second-order harmonic distortion                                   | Differential input, f = 10kHz, V <sub>OUT</sub> = 10V <sub>PP</sub> |                         | –120 |                         |      |
|                           |                                                                    | Single-ended input, f = 10kHz, V <sub>OUT</sub> = 10V <sub>PP</sub> |                         | –110 |                         |      |
| HD3                       | Third-order harmonic distortion                                    | Differential input, f = 10kHz, V <sub>OUT</sub> = 10V <sub>PP</sub> |                         | –120 |                         |      |
|                           |                                                                    | Single-ended input, f = 10kHz, V <sub>OUT</sub> = 10V <sub>PP</sub> |                         | –110 |                         |      |
| REFERENCE INPUT           |                                                                    |                                                                     |                         |      |                         |      |
| R <sub>IN</sub>           | Reference input impedance                                          |                                                                     |                         | 10   |                         | kΩ   |
|                           | Reference input current                                            | V <sub>IN</sub> = 0V                                                |                         | 140  |                         | μA   |
|                           | Reference input voltage                                            |                                                                     | V <sub>LVSS</sub>       |      | V <sub>LVDD</sub>       | V    |
|                           | Reference gain to output                                           |                                                                     |                         | 1    |                         | V/V  |
|                           | Reference gain error                                               | V <sub>OUT</sub> = ±10V, inside the voltage swing range             |                         | 0.01 | 0.05                    | %    |
| INPUT STAGE POWER SUPPLY  |                                                                    |                                                                     |                         |      |                         |      |
| I <sub>Q_input</sub>      | Input stage quiescent current<br>V <sub>S+</sub> , V <sub>S–</sub> | V <sub>IN</sub> = 0V                                                |                         | 3    | 3.7                     | mA   |
|                           |                                                                    | T <sub>A</sub> = –40°C to +125°C                                    |                         |      | 4.6                     |      |
| OUTPUT STAGE POWER SUPPLY |                                                                    |                                                                     |                         |      |                         |      |
| I <sub>Q_output</sub>     | Output stage quiescent current<br>LVDD, LVSS                       | V <sub>IN</sub> = 0V, V <sub>REF</sub> = 0V                         |                         | 2.3  | 2.8                     | mA   |
|                           |                                                                    | T <sub>A</sub> = –40°C to 125°C                                     |                         |      | 3.5                     |      |
| DIGITAL LOGIC             |                                                                    |                                                                     |                         |      |                         |      |
| V <sub>IL</sub>           | Digital input logic low                                            | A0, A1, A2 pins, referred to DGND                                   | V <sub>DGND</sub>       |      | V <sub>DGND</sub> + 0.8 | V    |
| V <sub>IH</sub>           | Digital input logic high                                           | A0, A1, A2 pins, referred to DGND                                   | V <sub>DGND</sub> + 1.8 |      | V <sub>S+</sub>         | V    |
|                           | Digital input pin current                                          | A0, A1, A2 pins                                                     |                         | 1.5  | 3                       | μA   |
| V <sub>DGND</sub>         | DGND voltage                                                       |                                                                     | V <sub>S–</sub>         |      | (V <sub>S+</sub> ) – 4  | V    |
|                           | DGND reference current                                             |                                                                     |                         | 4    | 10                      | μA   |

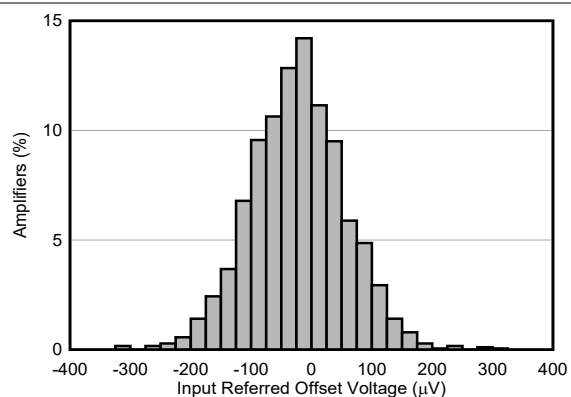
## 6.6 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{\text{SOUT}} = \pm 15\text{V}$ ,  $V_{\text{ICM}} = V_{\text{REF}} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to ground, and  $G = 1\text{V/V}$  (unless otherwise noted)



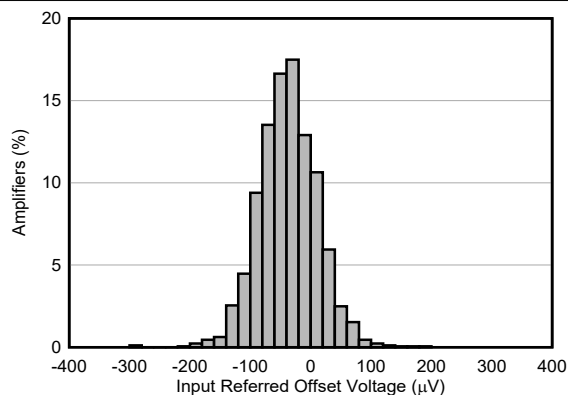
N = 1767      Mean =  $-165.34\mu\text{V}$       Std. dev. =  $600.90\mu\text{V}$   
G = 0.125V/V

図 6-1. Distribution of Offset Voltage (RTI)



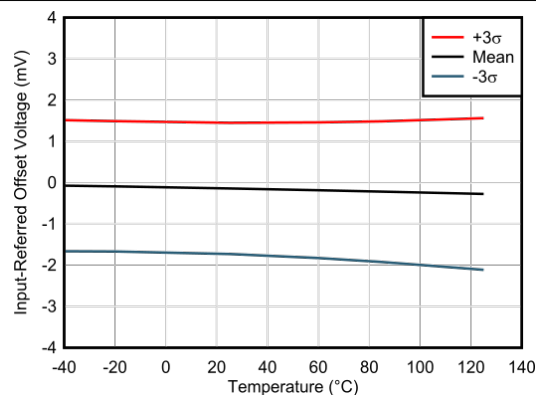
N = 1767      Mean =  $-22.56\mu\text{V}$       Std. dev. =  $78.45\mu\text{V}$   
G = 1V/V

図 6-2. Distribution of Offset Voltage (RTI)



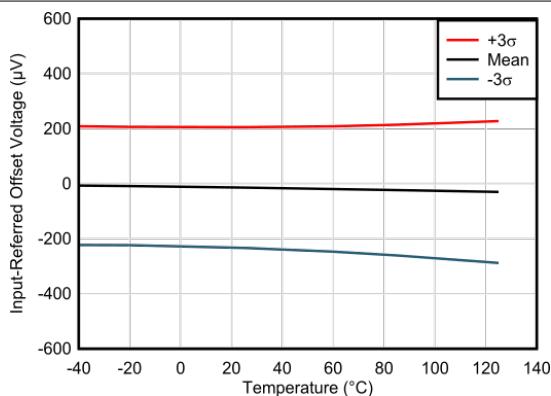
N = 1767      Mean =  $-37.55\mu\text{V}$       Std. dev. =  $48.69\mu\text{V}$   
G = 16V/V

図 6-3. Distribution of Offset Voltage (RTI)



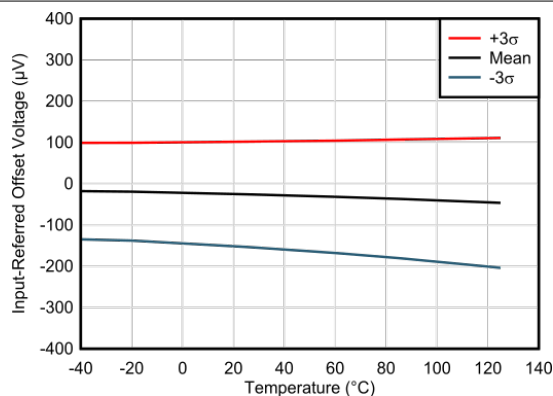
N = 58      1 wafer lot  
G = 0.125V/V

図 6-4. Offset Voltage (RTI) vs Temperature



N = 58      1 wafer lot  
G = 1V/V

図 6-5. Offset Voltage (RTI) vs Temperature



N = 58      1 wafer lot  
G = 16V/V

図 6-6. Offset Voltage (RTI) vs Temperature



## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{SOUT} = \pm 15\text{V}$ ,  $V_{ICM} = V_{REF} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to ground, and  $G = 1\text{V/V}$  (unless otherwise noted)

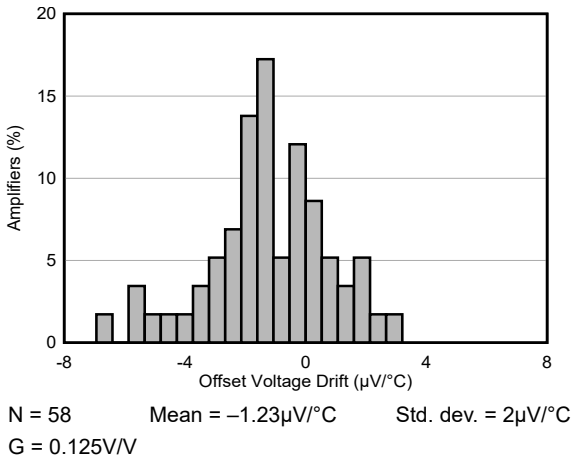


FIG 6-7. Distribution of Offset Voltage Drift (RTI)

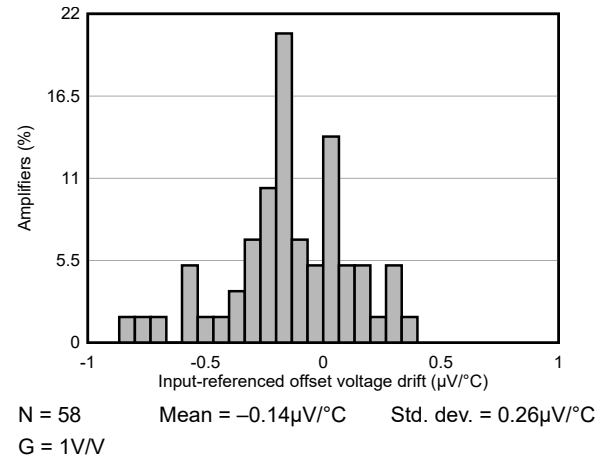


FIG 6-8. Distribution of Offset Voltage Drift (RTI)

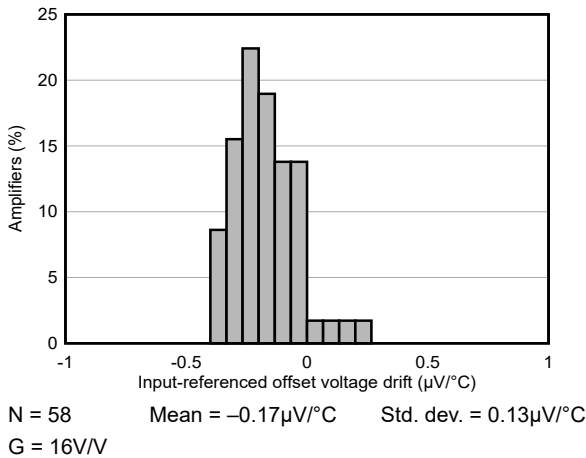


FIG 6-9. Distribution of Offset Voltage Drift (RTI)

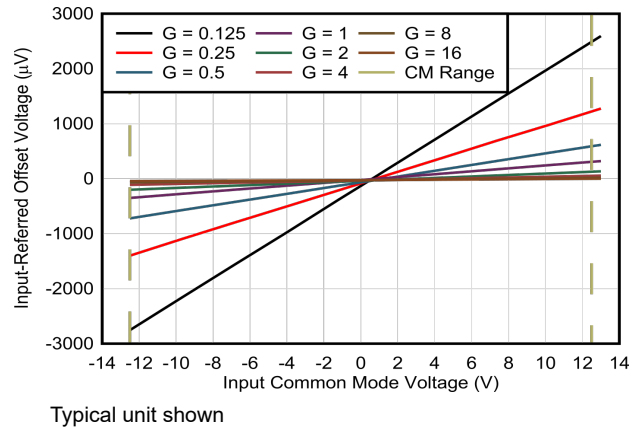


FIG 6-10. Offset Voltage (RTI) vs  $V_{ICM}$

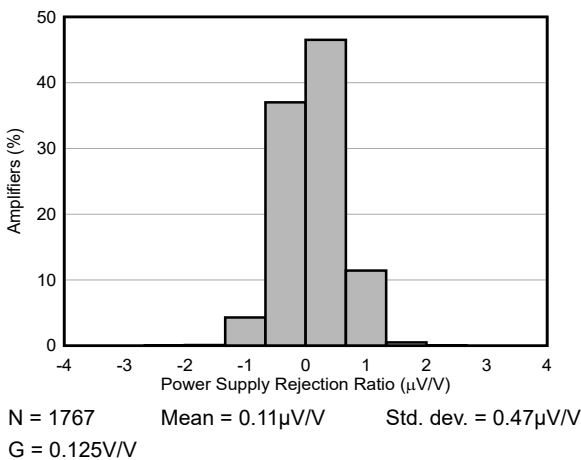


FIG 6-11. PSRR Distribution

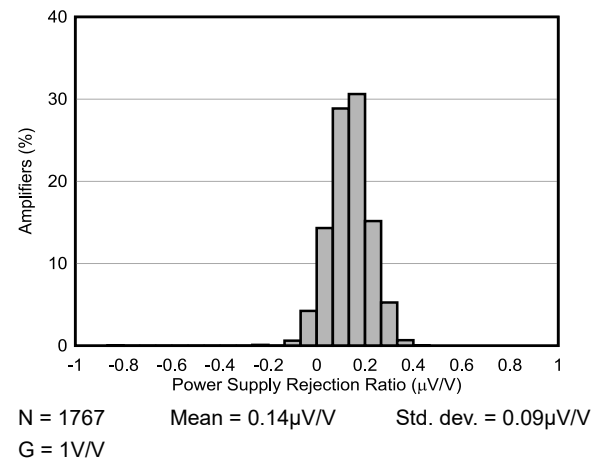
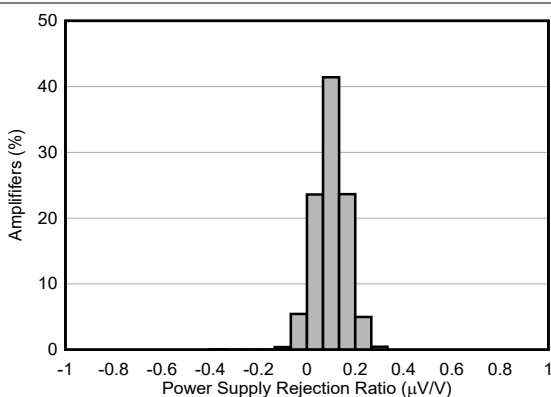


FIG 6-12. PSRR Distribution

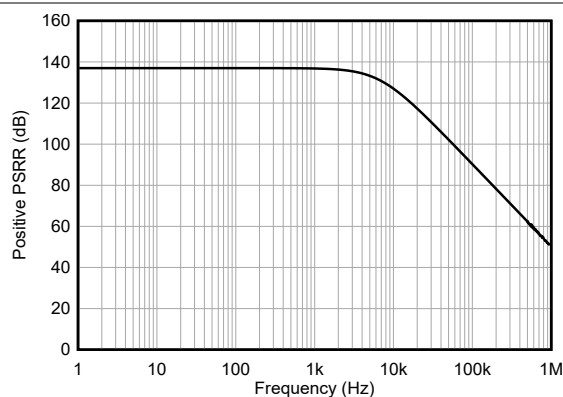
## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{\text{SOUT}} = \pm 15\text{V}$ ,  $V_{\text{ICM}} = V_{\text{REF}} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to ground, and  $G = 1\text{V/V}$  (unless otherwise noted)



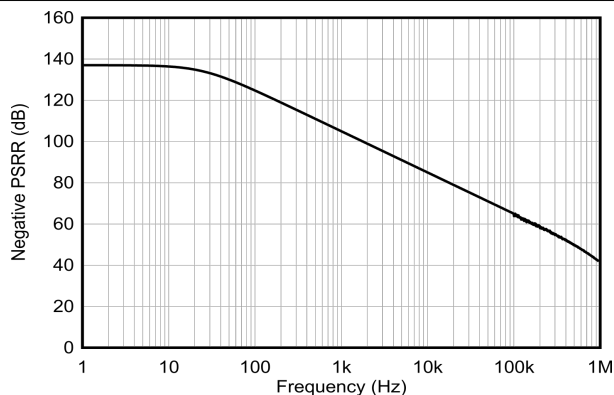
N = 1767      Mean =  $0.10\mu\text{V/V}$       Std. dev. =  $0.06\mu\text{V/V}$   
G =  $16\text{V/V}$

図 6-13. PSRR Distribution



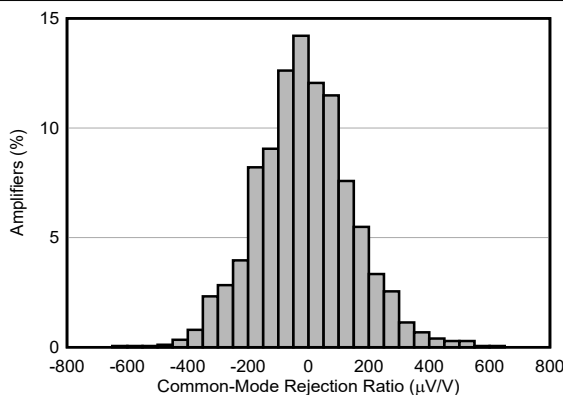
Typical unit shown  
G =  $1\text{V/V}$

図 6-14. Positive PSRR vs Frequency



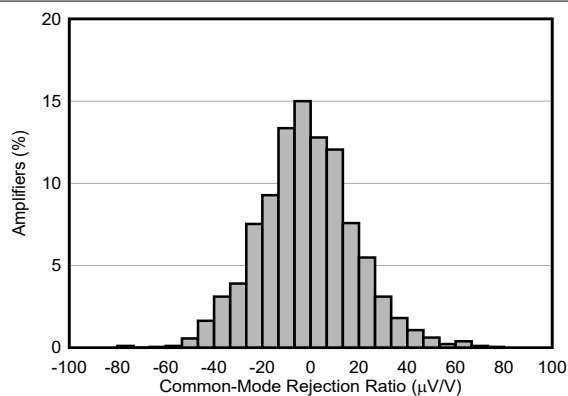
Typical unit shown  
G =  $1\text{V/V}$

図 6-15. Negative PSRR vs Frequency



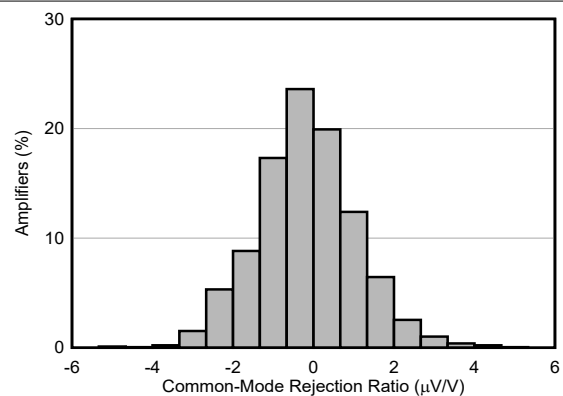
N = 1767      Mean =  $-12.21\mu\text{V/V}$       Std. dev. =  $159.35\mu\text{V/V}$   
G =  $0.125\text{V/V}$

図 6-16. CMRR Distribution



N = 1767      Mean =  $-1.55\mu\text{V/V}$       Std. dev. =  $19.92\mu\text{V/V}$   
G =  $1\text{V/V}$

図 6-17. CMRR Distribution

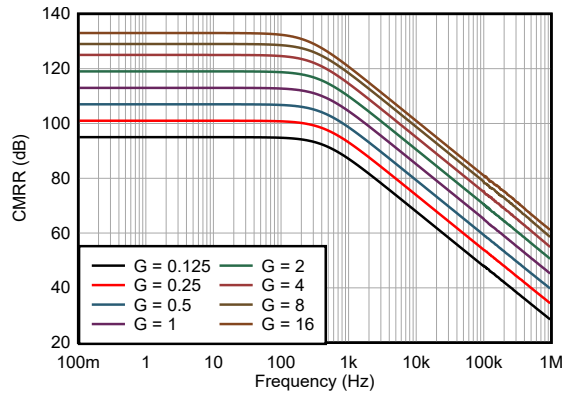


N = 1767      Mean =  $-0.17\mu\text{V/V}$       Std. dev. =  $1.25\mu\text{V/V}$   
G =  $16\text{V/V}$

図 6-18. CMRR Distribution

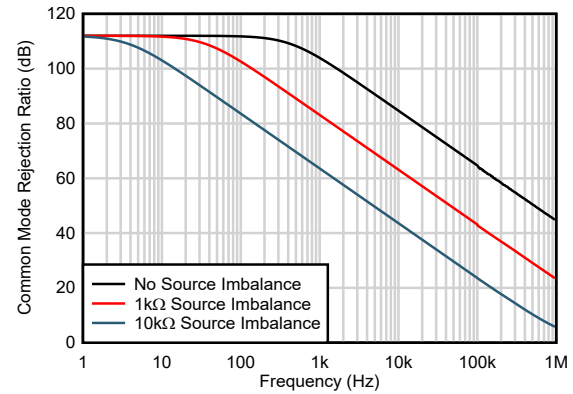
## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{\text{SOUT}} = \pm 15\text{V}$ ,  $V_{\text{ICM}} = V_{\text{REF}} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to ground, and  $G = 1\text{V/V}$  (unless otherwise noted)



Typical unit shown

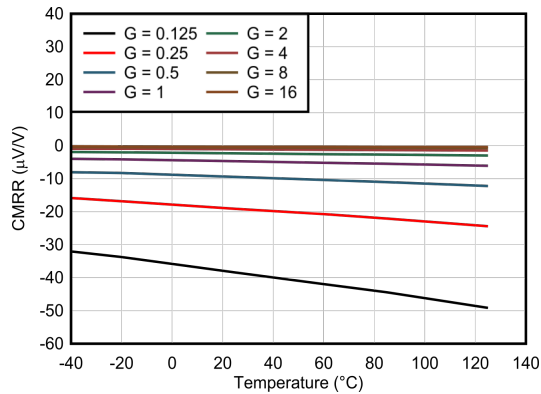
Figure 6-19. CMRR vs Frequency (RTI)



Typical unit shown

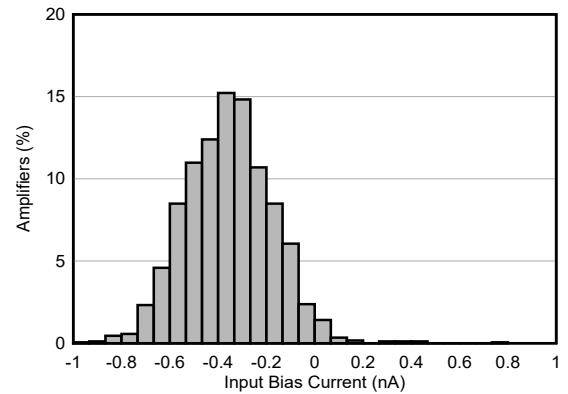
$G = 1\text{V/V}$

Figure 6-20. CMRR vs Frequency (Unbalanced)



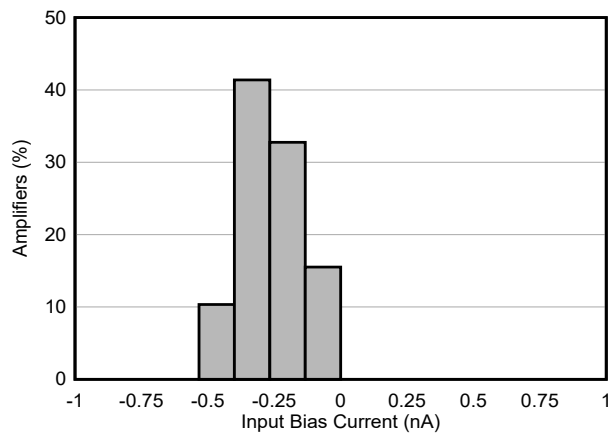
Typical unit shown

Figure 6-21. CMRR vs Temperature



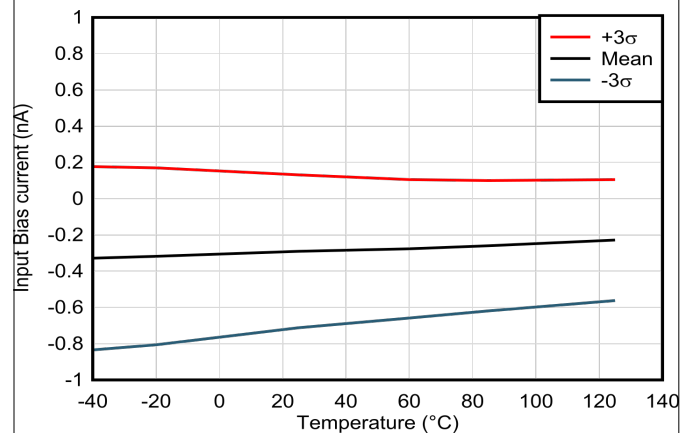
N = 1767      Mean =  $-0.35\text{nA}$       Std. dev. =  $0.181\text{nA}$   
 $G = 1\text{V/V}$

Figure 6-22. Distribution of Input Bias Current



N = 58      Mean =  $-0.265\text{nA}$       Std. dev. =  $0.11\text{nA}$   
 $T_A = 85^\circ\text{C}$        $G = 1\text{V/V}$

Figure 6-23. Distribution of Input Bias Current

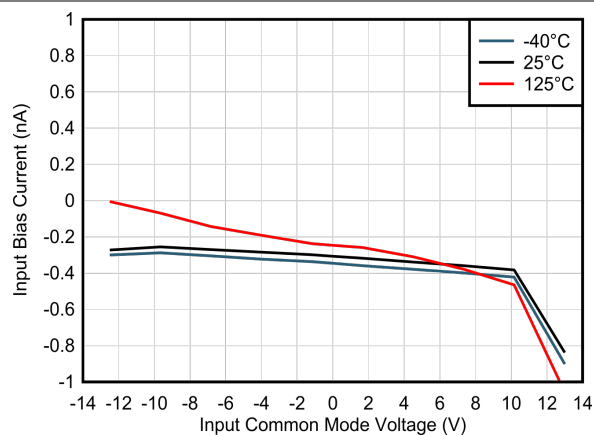


N = 58      1 wafer lot  
 $G = 1\text{V/V}$

Figure 6-24. Input Bias Current vs Temperature

## 6.6 Typical Characteristics (continued)

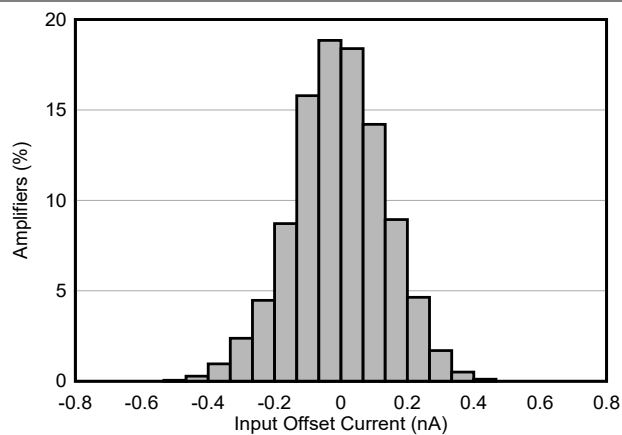
at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{\text{SOUT}} = \pm 15\text{V}$ ,  $V_{\text{ICM}} = V_{\text{REF}} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to ground, and  $G = 1\text{V/V}$  (unless otherwise noted)



Typical unit shown

$G = 1\text{V/V}$

Figure 6-25. Input Bias Current vs  $V_{\text{ICM}}$



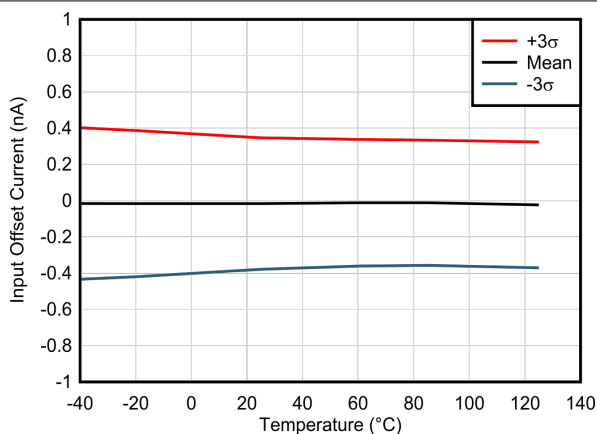
$N = 1767$

Mean =  $-0.006\text{nA}$

Std. dev =  $0.139\text{nA}$

$G = 1\text{V/V}$

Figure 6-26. Distribution of Input Offset Current

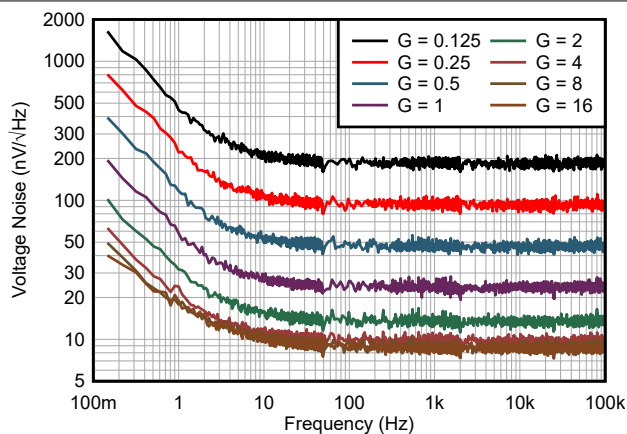


$N = 58$

1 wafer lot

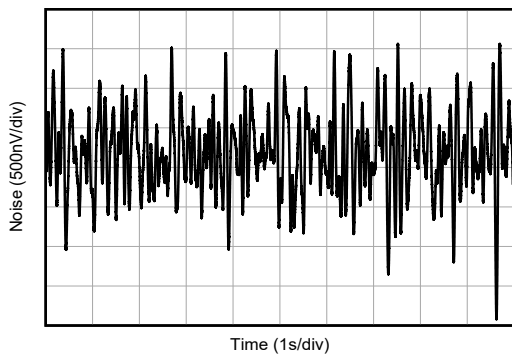
$G = 1\text{V/V}$

Figure 6-27. Input Offset Current vs Temperature



Typical unit shown

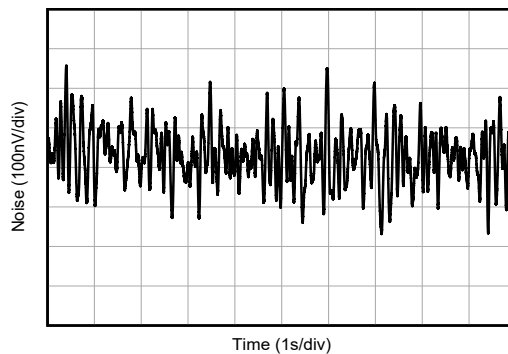
Figure 6-28. Voltage Noise Spectral Density (RTI) vs Frequency



Typical unit shown

$G = 0.125\text{V/V}$

Figure 6-29. 0.1Hz to 10Hz Voltage Noise (RTI)



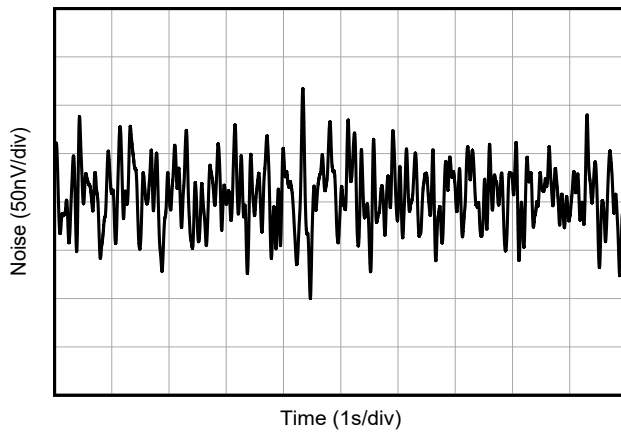
Typical unit shown

$G = 1\text{V/V}$

Figure 6-30. 0.1Hz to 10Hz Voltage Noise (RTI)

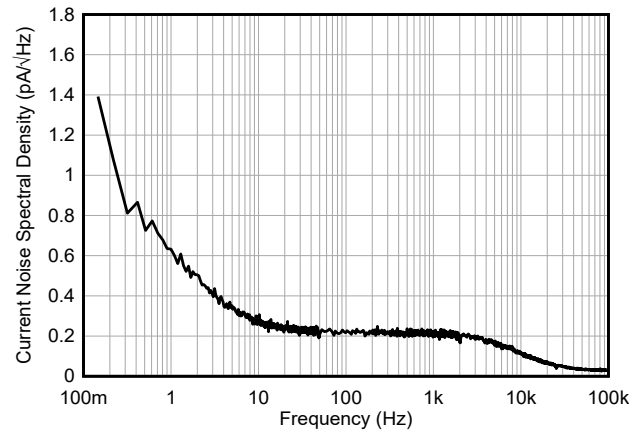
## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{SOUT} = \pm 15\text{V}$ ,  $V_{ICM} = V_{REF} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to ground, and  $G = 1\text{V/V}$  (unless otherwise noted)



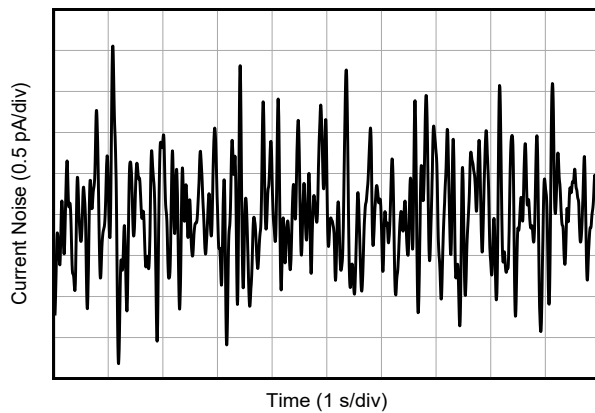
Typical unit shown  
 $G = 16\text{V/V}$

Figure 6-31. 0.1Hz to 10Hz Voltage Noise (RTI)



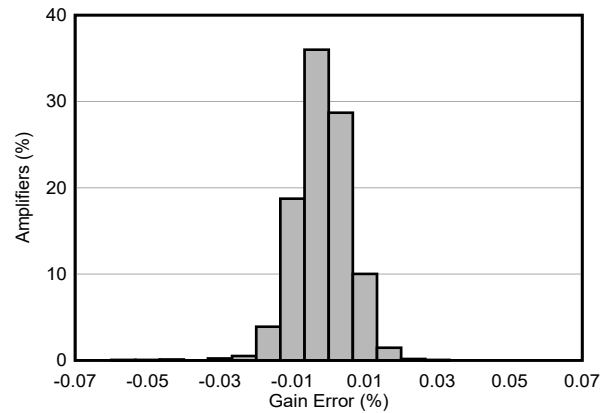
$G = 1\text{V/V}$

Figure 6-32. Current Noise Spectral Density vs Frequency



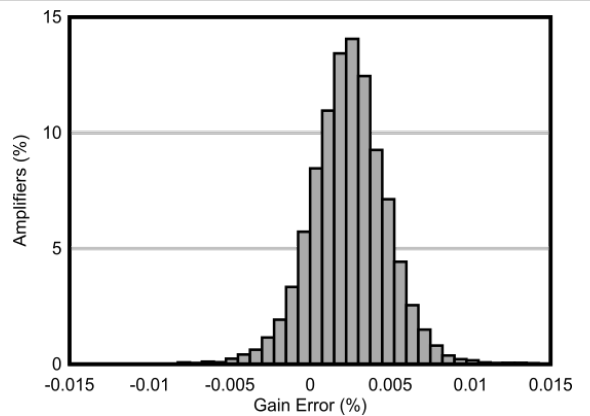
Typical unit shown  
 $G = 1\text{V/V}$

Figure 6-33. 0.1Hz to 10Hz Current Noise



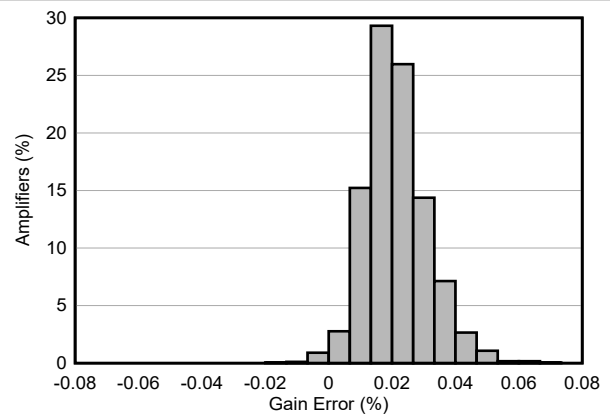
$N = 1767$  Mean =  $-0.0017\%$  Std. dev. =  $0.0074\%$   
 $G = 0.125\text{V/V}$

Figure 6-34. Distribution of Gain Error



$N = 10032$  Mean =  $-0.0016\%$  Std. dev. =  $0.0025\%$   
 $G = 1\text{V/V}$

Figure 6-35. Distribution of Gain Error

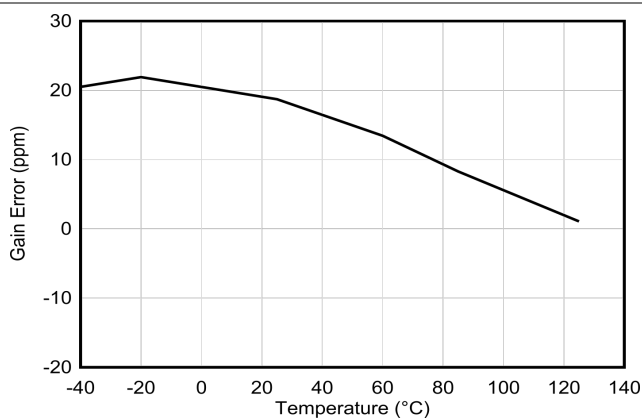


$N = 1767$  Mean =  $0.0124\%$  Std. dev. =  $0.0098\%$   
 $G = 16\text{V/V}$

Figure 6-36. Distribution of Gain Error

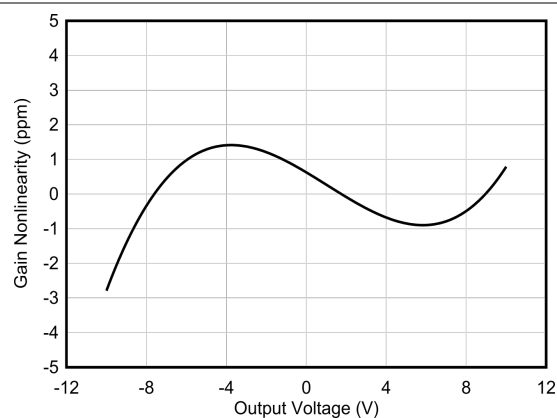
## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{\text{SOUT}} = \pm 15\text{V}$ ,  $V_{\text{ICM}} = V_{\text{REF}} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to ground, and  $G = 1\text{V/V}$  (unless otherwise noted)



Typical unit shown  
 $G = 1\text{V/V}$

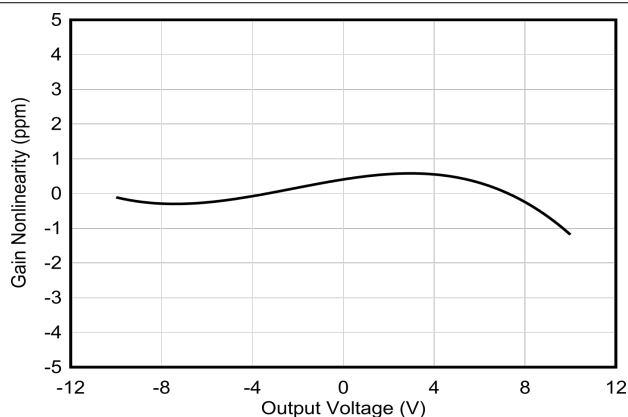
Figure 6-37. Gain Error vs Temperature



$V_{\text{OUT}} = \pm 10\text{V}$   
Typical unit shown

$G = 1\text{V/V}$

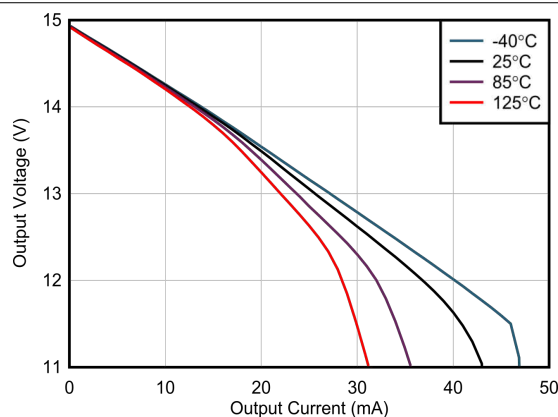
Figure 6-38. Gain Nonlinearity



$V_{\text{OUT}} = \pm 10\text{V}$   
Typical unit shown

$G = 16\text{V/V}$

Figure 6-39. Gain Nonlinearity

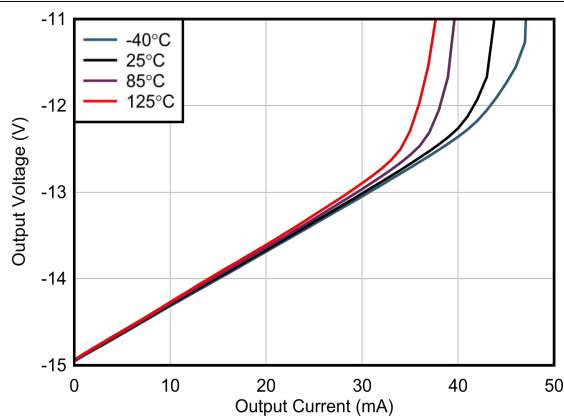


$V_S = \pm 18\text{V}$

$V_{\text{OUT}} = \pm 15\text{V}$

$G = 16\text{V/V}$

Figure 6-40. Positive Output Voltage vs Output Current

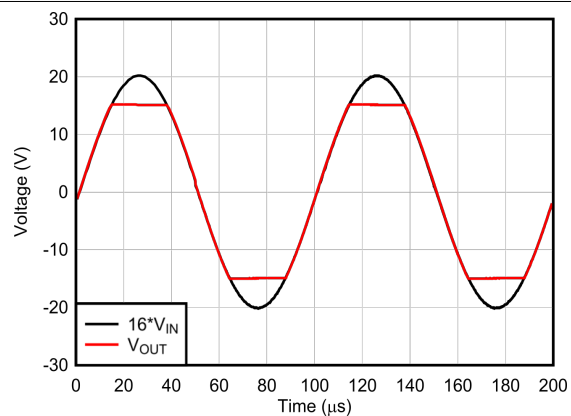


$V_S = \pm 18\text{V}$

$V_{\text{OUT}} = \pm 15\text{V}$

$G = 16\text{V/V}$

Figure 6-41. Negative Output Voltage vs Output Current

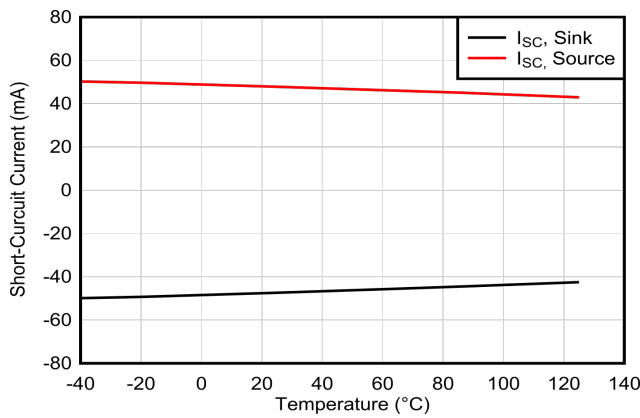


$G = 16\text{V/V}$

Figure 6-42. Overload Recovery

## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{SOUT} = \pm 15\text{V}$ ,  $V_{ICM} = V_{REF} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to ground, and  $G = 1\text{V/V}$  (unless otherwise noted)



Short to  $V_{SOUT}/2$   
 $G = 1\text{V/V}$

Figure 6-43. Output Short-Circuit Current vs Temperature

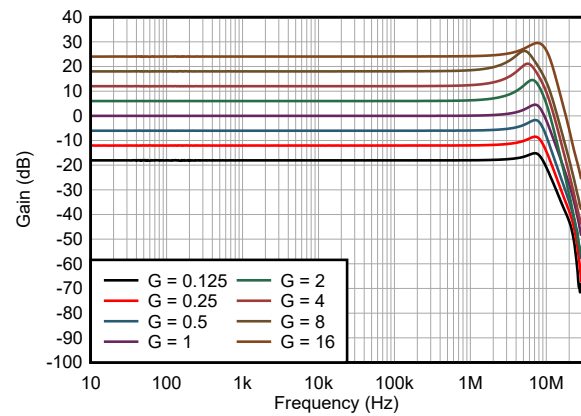
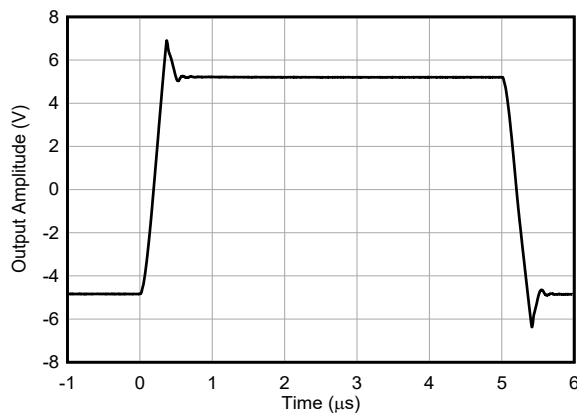
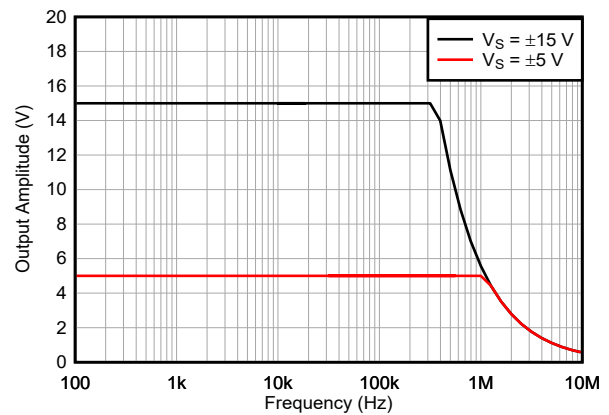


Figure 6-44. Gain vs Frequency



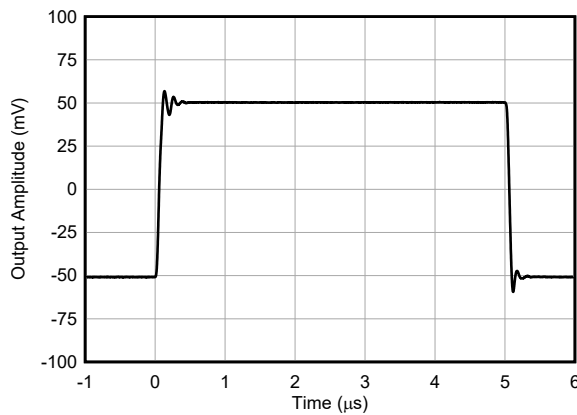
$G = 1\text{V/V}$

Figure 6-45. Large-Signal Step Response



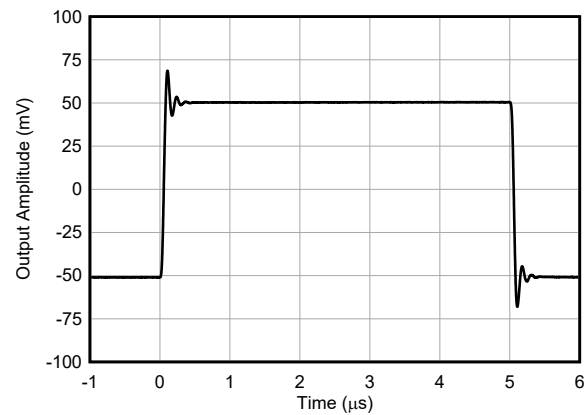
$G = 1\text{V/V}$

Figure 6-46. Large-Signal Step Response vs Frequency



$G = 0.125\text{V/V}$

Figure 6-47. Small-Signal Step Response

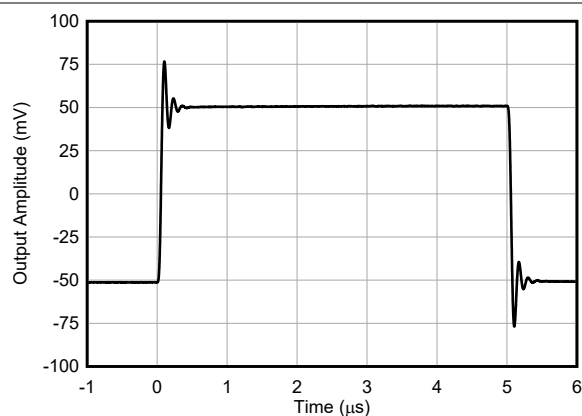


$G = 0.25\text{V/V}$

Figure 6-48. Small-Signal Step Response

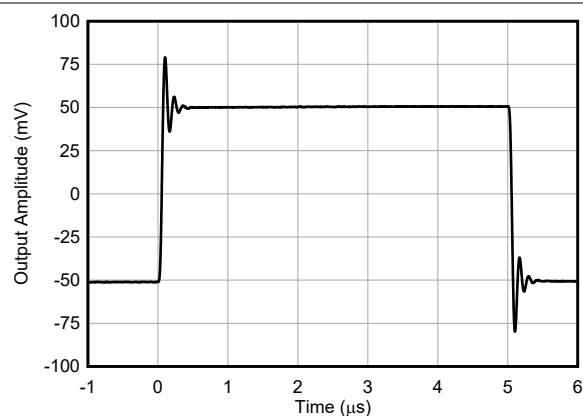
## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{\text{SOUT}} = \pm 15\text{V}$ ,  $V_{\text{ICM}} = V_{\text{REF}} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to ground, and  $G = 1\text{V/V}$  (unless otherwise noted)



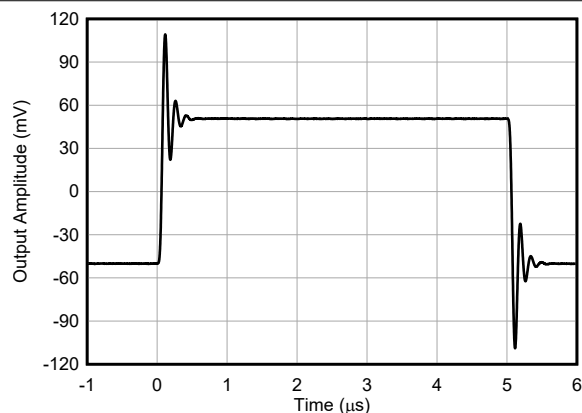
$G = 0.5\text{V/V}$

図 6-49. Small-Signal Step Response



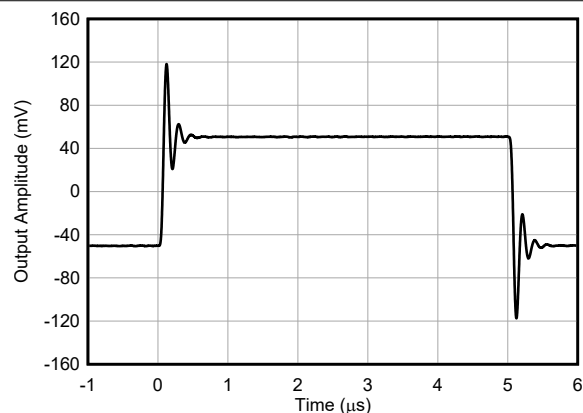
$G = 1\text{V/V}$

図 6-50. Small-Signal Step Response



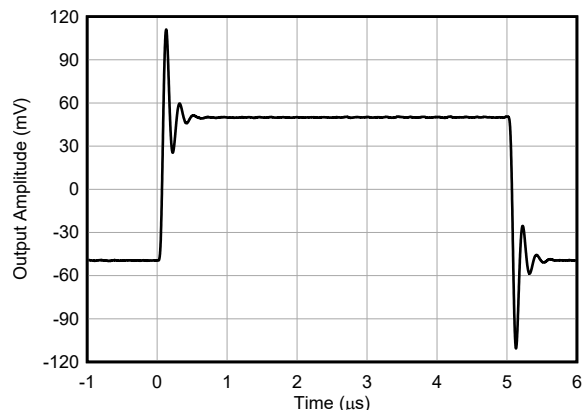
$G = 2\text{V/V}$

図 6-51. Small-Signal Step Response



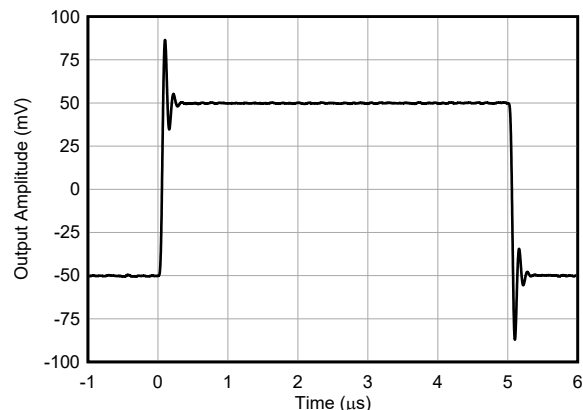
$G = 4\text{V/V}$

図 6-52. Small-Signal Step Response



$G = 8\text{V/V}$

図 6-53. Small-Signal Step Response



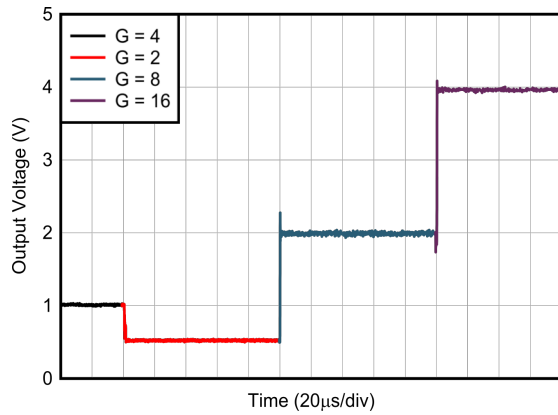
$G = 16\text{V/V}$

図 6-54. Small-Signal Step Response



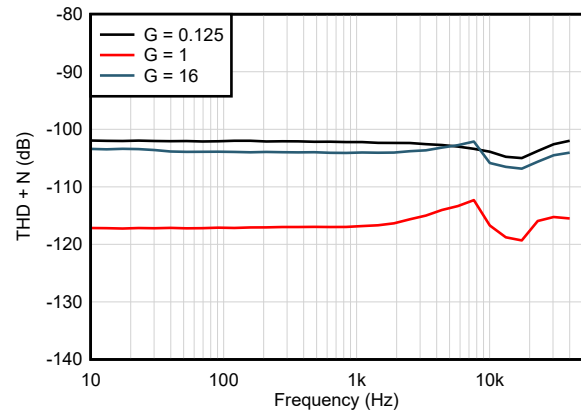
## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{SOUT} = \pm 15\text{V}$ ,  $V_{ICM} = V_{REF} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to ground, and  $G = 1\text{V/V}$  (unless otherwise noted)



$V_{IN} = 250\text{mV}_{PP}$

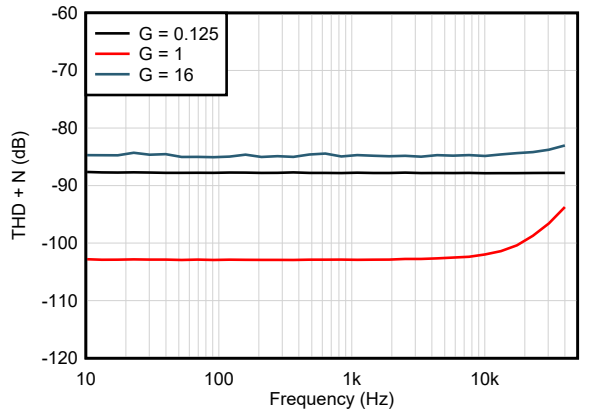
**FIG 6-55. Gain Switching Transient Response**



10Hz to 22kHz band-pass filter

$V_{OUTDIFF} > 2.5\text{V}_{PP}$

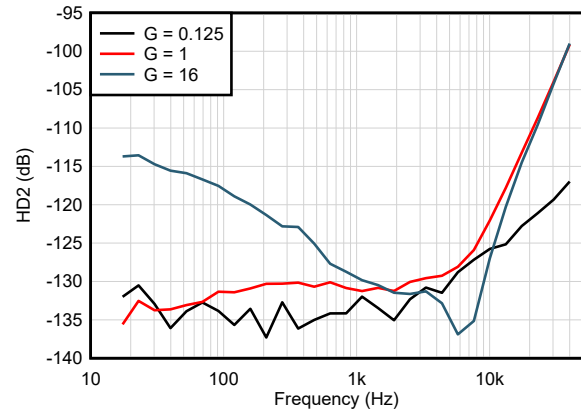
**FIG 6-56. Total Harmonic Distortion + Noise vs Frequency**



10Hz to 500kHz band-pass filter

$V_{OUTDIFF} > 2.5\text{V}_{PP}$

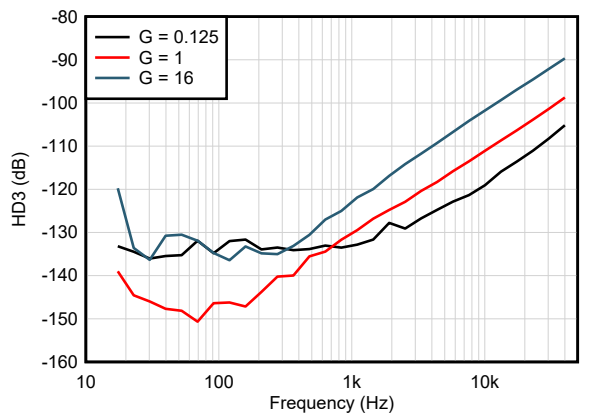
**FIG 6-57. Total Harmonic Distortion + Noise vs Frequency**



10Hz to 500kHz band-pass filter

$V_{OUTDIFF} > 2.5\text{V}_{PP}$

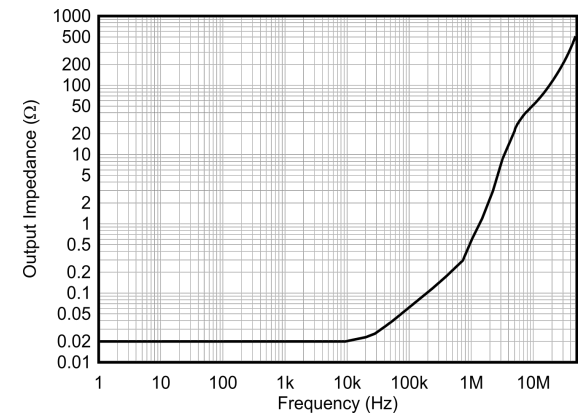
**FIG 6-58. 2nd Harmonic Distortion vs Frequency**



10Hz to 500kHz band-pass filter

$V_{OUTDIFF} > 2.5\text{V}_{PP}$

**FIG 6-59. 3rd Harmonic Distortion vs Frequency**

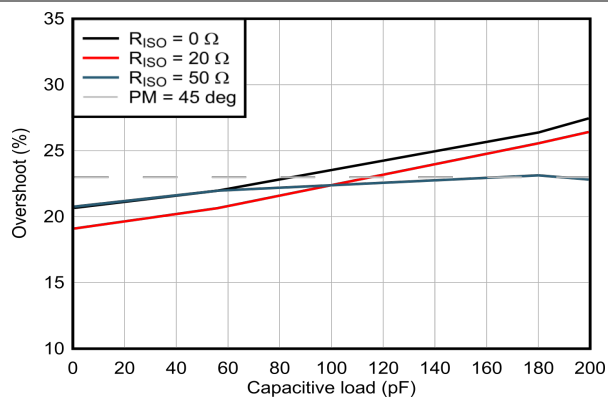


$G = 1\text{V/V}$

**FIG 6-60. Closed-Loop Output Impedance vs Frequency**

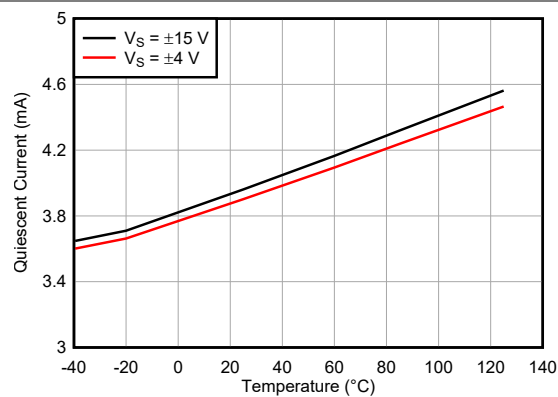
## 6.6 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = V_{\text{SOUT}} = \pm 15\text{V}$ ,  $V_{\text{ICM}} = V_{\text{REF}} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to ground, and  $G = 1\text{V/V}$  (unless otherwise noted)



$G = 1\text{V/V}$

図 6-61. Overshoot vs Capacitive Load



Input stage

$G = 1\text{V/V}$

図 6-62. Quiescent Current vs Temperature

## 7 Detailed Description

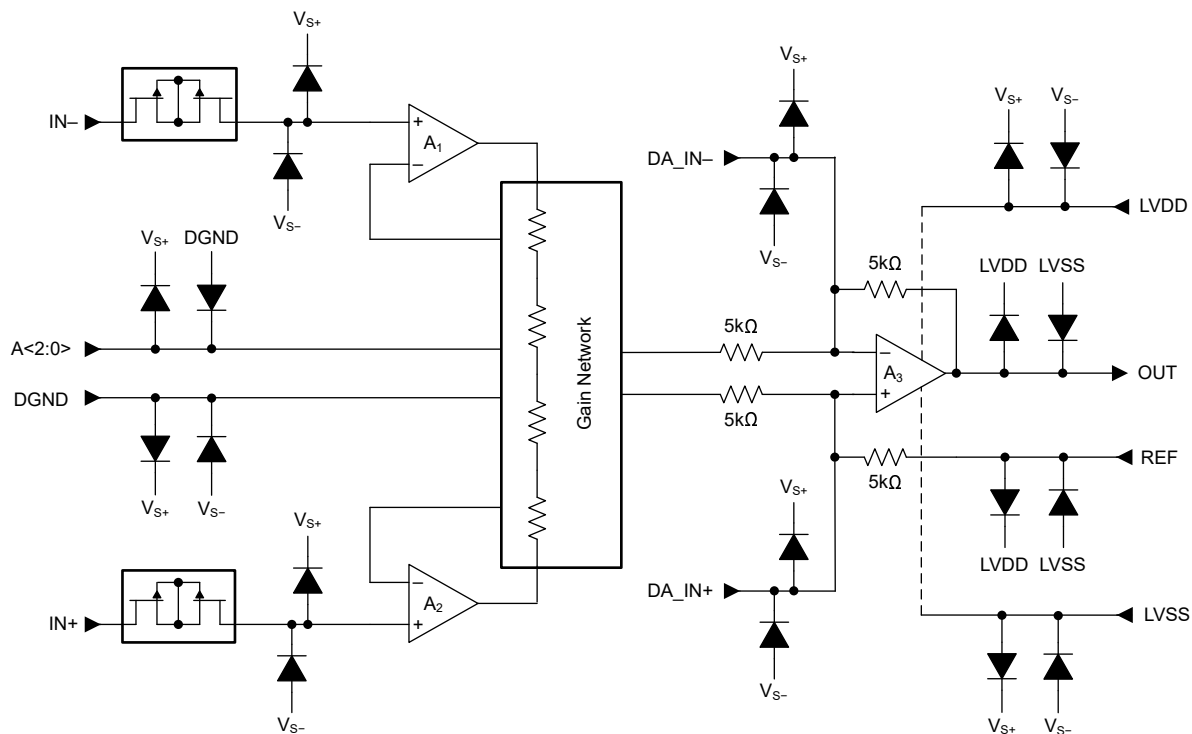
### 7.1 Overview

The PGA849 is a monolithic, high-voltage, precision programmable-gain instrumentation amplifier. The PGA849 combines a high-speed current-feedback input stage with an internally matched gain resistor network, followed by a four-resistor, difference amplifier output stage. Eight pre-programmed binary gains are selectable using gain-select pins A0, A1, A2. Gains range from 0.125V/V to 16V/V, discussed in greater detail in [セクション 7.3.1](#).

A functional block diagram for the PGA849 is shown in the next section. The differential input voltage is fed into a pair of matched, high-impedance input, current-feedback amplifiers. An integrated precision-matched gain resistor network is used to amplify the differential input voltage. An output difference amplifier, A<sub>3</sub>, rejects the input common-mode component and refers the output signal to the voltage level set by the REF pin.

The PGA849 output amplifier bandwidth is optimized to drive high-performance analog-to-digital converters (ADCs) with sampling rates up to 1MSPS, without the need for an additional ADC driver. The output amplifier uses a separate power supply that is independent of the input-stage power supply. When driving an ADC, use a low-impedance connection from LVDD and LVSS to the ADC power supplies. This configuration protects the ADC inputs from damage due to inadvertent overvoltage conditions.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Gain Control

The PGA849 uses three pins to set the amplifier gain. These gain select pins are set with respect to DGND. This configuration simplifies the design when compared to programmable-gain amplifiers requiring a SPI or other digital interface options for gain changes. 図 7-1 shows the gain-setting block diagram. 表 7-1 lists the gain options. Any gain select pin that is not driven by an external source is automatically biased at DGND using internal pulldown options.

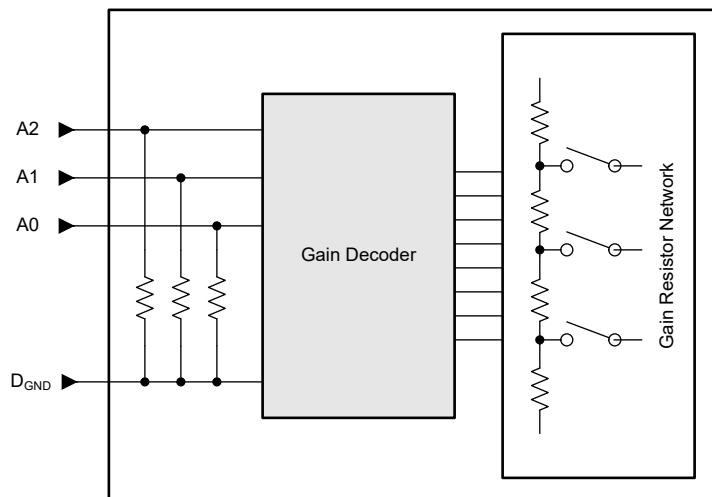


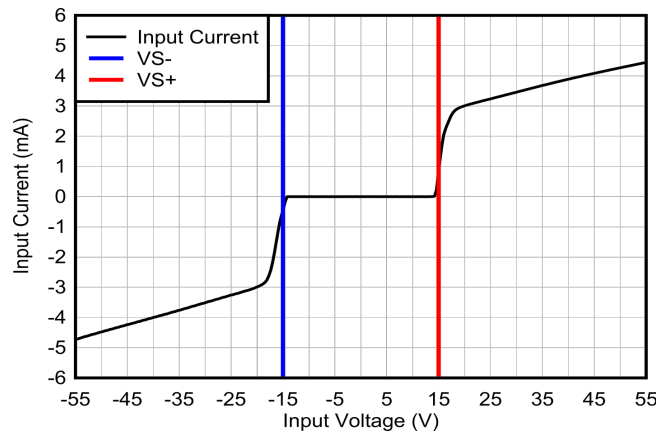
図 7-1. PGA849 Gain Setting Block Diagram

表 7-1. Gain Options

| A2:A0 | GAIN  |
|-------|-------|
| 000   | 0.125 |
| 001   | 0.25  |
| 010   | 0.5   |
| 011   | 1     |
| 100   | 2     |
| 101   | 4     |
| 110   | 8     |
| 111   | 16    |

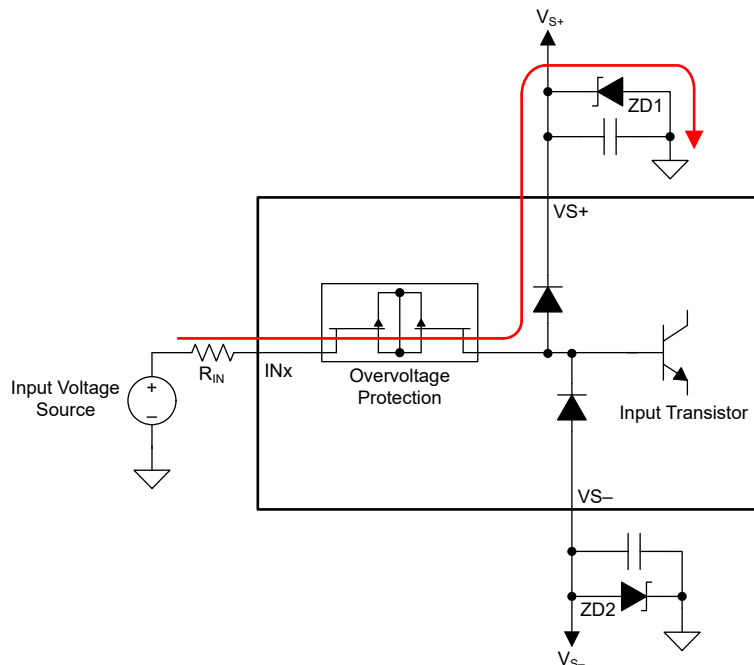
### 7.3.2 Input Protection

The inputs of the PGA849 are individually protected for voltages up to  $\pm 40\text{V}$  beyond either supply. For example, an input common-mode voltage anywhere between  $-55\text{V}$  and  $+55\text{V}$  does not cause damage when powered from  $\pm 15\text{V}$  supplies. Internal circuitry on each input provides low series impedance under normal signal conditions, thus maintaining high performance under normal operating conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately  $4.8\text{mA}$ . [Figure 7-2](#) shows the input protection functionality during an overvoltage condition.



**Figure 7-2. Input Current vs Input Overvoltage**

[Figure 7-3](#) shows that during an input overvoltage condition, current flows through the input protection diodes into the power supplies. In applications where the power supplies are unable to sink current, place Zener diode clamps (ZD1 and ZD2) on the power supplies to provide a current pathway to ground.



**Figure 7-3. Input Current Path During an Overvoltage Condition**

### 7.3.3 Using the Output Difference Amplifier to Shape Noise

The functional block diagram in [セクション 7.2](#) shows that the PGA849 output-stage difference amplifier uses a 5k $\Omega$  feedback resistor between the output and the inverting input. External direct access to the inverting and noninverting inputs of the difference amplifier is provided through the DA\_IN– and DA\_IN+ pins, respectively. This option allows circuit designers to add external capacitors in parallel with the internal resistors to implement noise-filtering or noise-shaping techniques. These pins are also used to implement customized attenuating gains for the output stage. Consider the following important factors when designing parallel circuits with the internal resistors:

- The accuracy of the internal resistor network is 0.01% or better. This accuracy results in a common-mode rejection (CMRR) of 80dB or better. Mismatched leakage currents on these pins can cause CMRR degradation.
- The internal resistors have  $\pm 15\%$  absolute resistance variation and must be considered when implementing custom attenuating gains or noise filters.

#### 注意

Do not treat these pins as outputs, nor use the pins to source or sink current. Excessive currents through the feedback resistors can cause permanent damage to internal circuitry.

## 7.4 Device Functional Modes

The PGA849 has a single functional mode and operates when the input-stage power supply is greater than  $\pm 4\text{V}$  (8V) and the output-stage power supply is greater than  $\pm 2.25\text{V}$  (4.5V); see also [セクション 6.3](#).

## 8 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

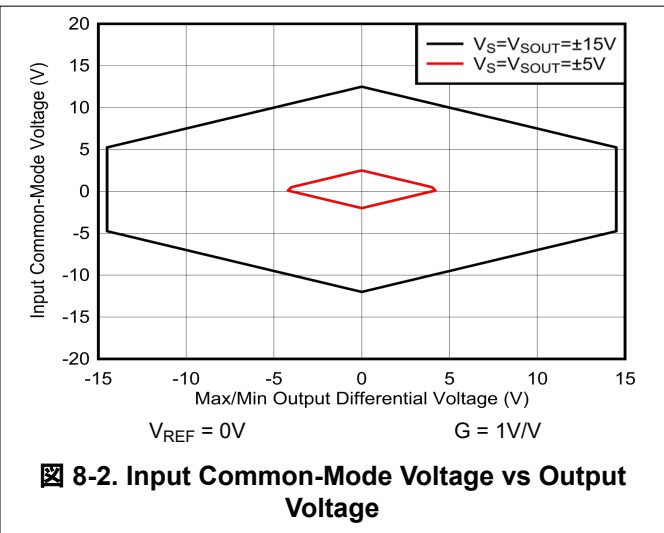
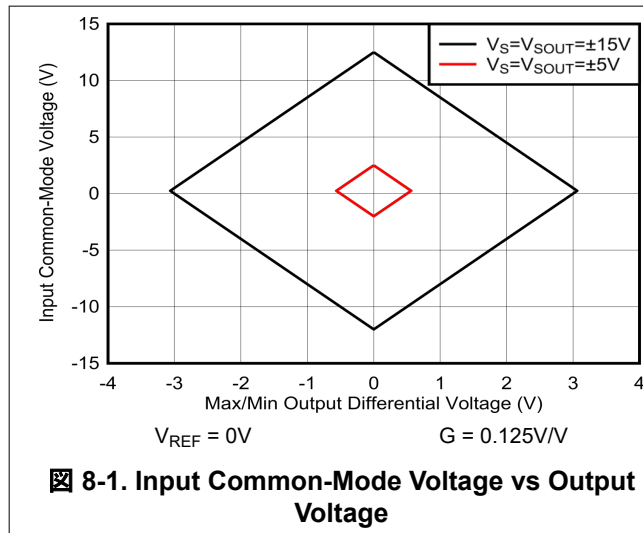
The PGA849 is a monolithic, high-voltage, high-bandwidth, precision programmable gain instrumentation amplifier with a single-ended output. The PGA849 combines a high-speed current-feedback input stage with an internally matched gain resistor network, followed by a four-resistor, differential amplifier output stage. The PGA849 is equipped with eight binary-gain settings, from 0.125V/V to 16V/V, using three digital gain-selection pins: A0, A1, and A2.

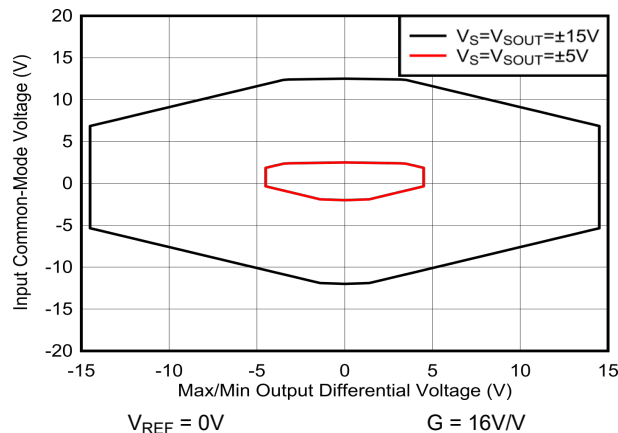
The PGA849 is designed to work with applications such as factory automation and control, analog input modules, data acquisition, test and measurement, and semiconductor test.

#### 8.1.1 Linear Operating Input Range

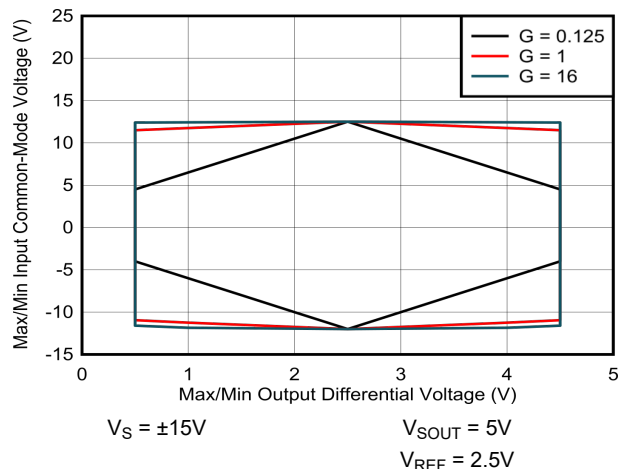
The linear operating input voltage range of the PGA849 input circuitry extends within 3V (maximum) of the negative power supply to 2.5V (maximum) of the positive power supply, and maintains excellent common-mode rejection throughout this range at all temperatures. The linear operating input common-mode range is a function of the input common-mode voltage, input differential voltage, gain, and output common-mode voltage.

The valid common-mode range to enable valid output voltage at no load condition are shown in 8-1 to 8-4.





**图 8-3. Input Common-Mode Voltage vs Output Voltage**

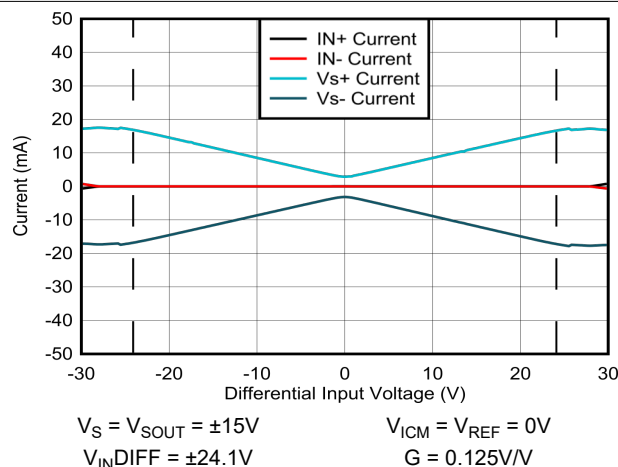


**图 8-4. Input Common-Mode Voltage vs Output Voltage**

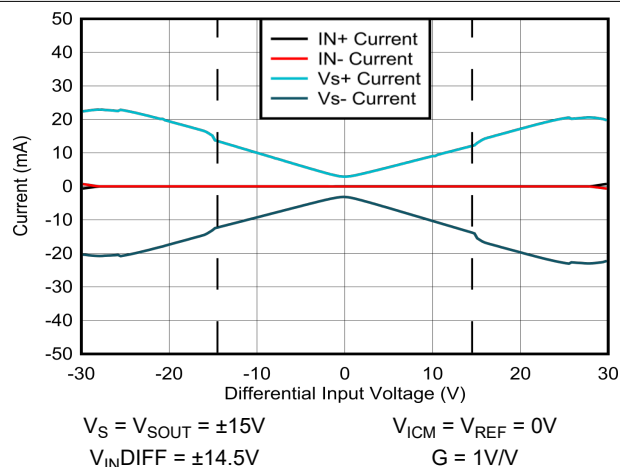
### 8.1.2 Current Consumption with Differential Inputs

Programmable gain amplifiers such as the PGA849 use internal resistors to set the gain. Consequently, the current consumption is increased by the current that passes through these resistors. The largest supply current consumption occurs at  $G = 1\text{V/V}$  when applying large amplitude differential signals.

图 8-5 to 图 8-8 show typical current consumption versus input differential voltage for the input stage supply, and the current drawn by the PGA849 inputs when the device is overdriven. The dashed vertical reference lines outline the linear operating region of the device at that given gain ( $V_{\text{INDIFF}}$ ), outside of this region is when the inputs of the device are overdriven.

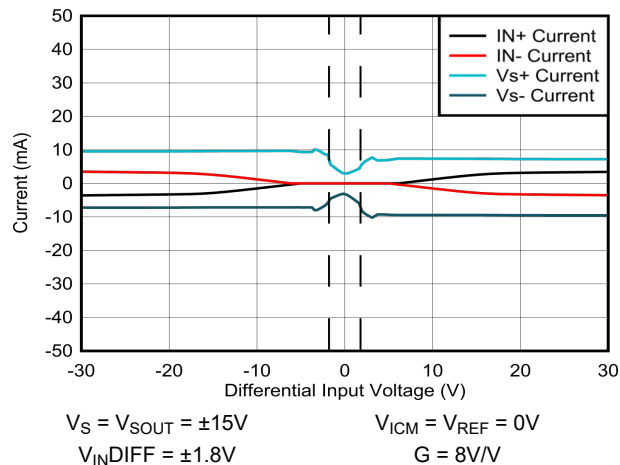


**图 8-5. Current Consumption versus Differential Input Voltage**

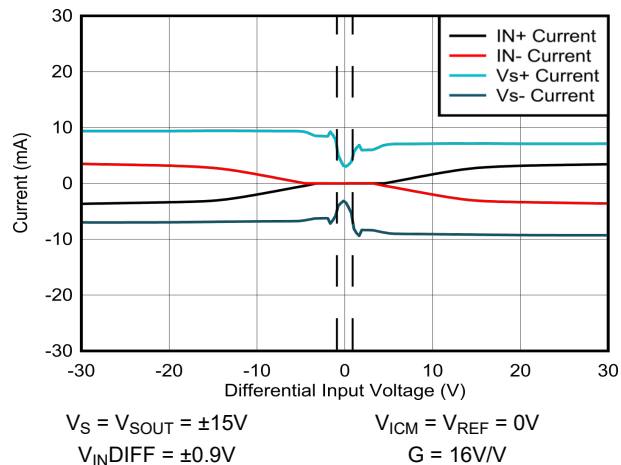


**图 8-6. Current Consumption versus Differential Input Voltage**





### 8-7. Current Consumption versus Differential Input Voltage

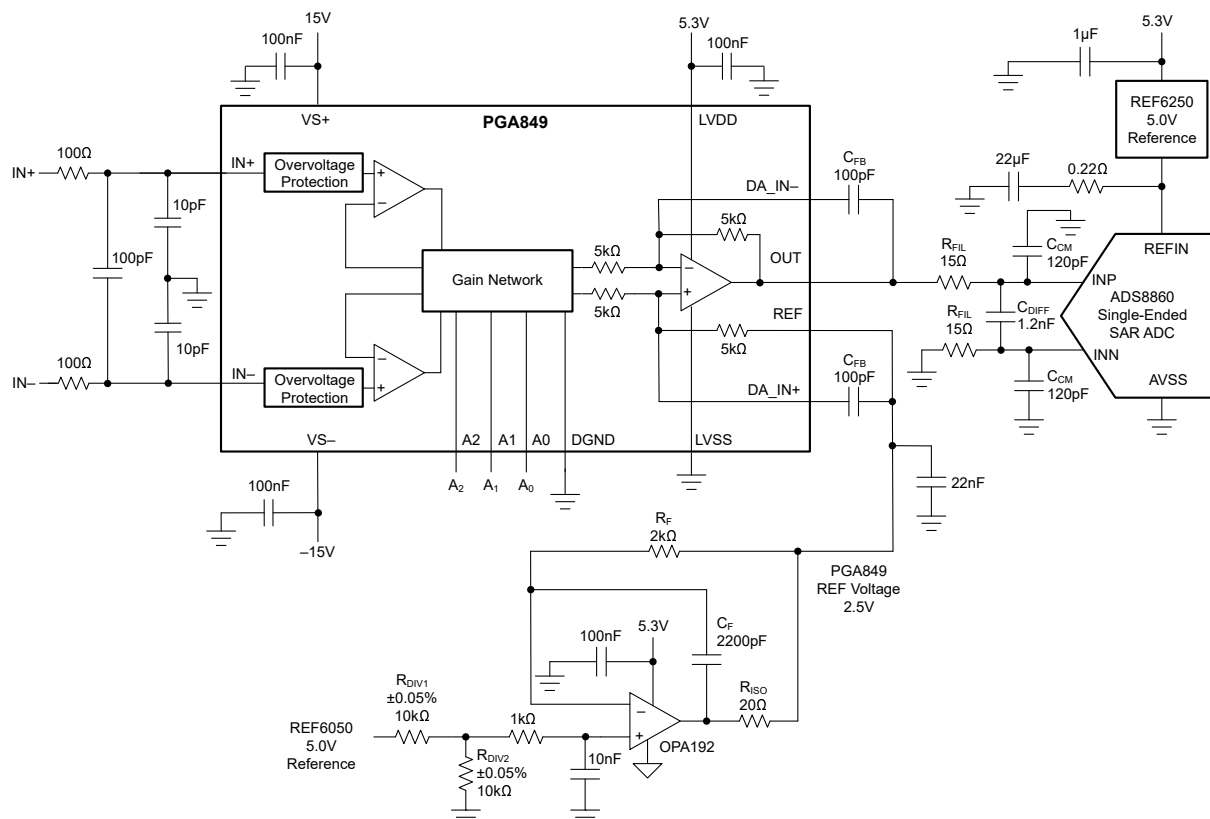


### 8-8. Current Consumption versus Differential Input Voltage

## 8.2 Typical Applications

### 8.2.1 Driving a Single-Ended Input SAR ADC

Figure 8-9 shows the schematic for a 16-bit, precision, 1MSPS, successive approximation register (SAR), analog-to-digital converter (ADC). This circuit is used to measure the driving capability of the PGA849 with the ADS8860 single-ended input ADC.



## 8-9. Driving the ADS8860 SAR ADC

The circuit accepts single-ended or differential input signals. The PGA849 operates with independent input and output power supplies. In this example,  $\pm 15\text{V}$  power supplies are used to power the input-stage, and a unipolar 5.3V supply powers the output-stage. The PGA849 output stage supply is powered by the same 5.3V ADC supply. The 5.3V output supply operation prevents overloading the ADC inputs during PGA overdrive conditions. The REF6250 is selected as the ADC voltage reference. The REF6250 is a low-noise, low-drift, precision, 5V reference connected to the ADS8860 reference input ADC REFIN pin.

The PGA849 output voltage is developed with respect to the REF pin. The REF pin is set to the SAR ADC midscale voltage by dividing the REF6250 ADC reference with a precision resistive voltage divider. The OPA192 buffer drives the PGA849 REF pin. The OPA192 is a precision amplifier with low offset, low drift and 10MHz bandwidth.

### 8.2.1.1 Design Requirements

The design requirements for the application driving the ADS8860 ADC are listed in the following table.

**表 8-1. Design Parameters**

| PARAMETER                                        | VALUE                                                                                                     |
|--------------------------------------------------|-----------------------------------------------------------------------------------------------------------|
| Supply voltages                                  | $V_{S\pm} = \pm 15\text{V}$ , $LVDD = 5.3\text{V}$ , $LVSS = \text{GND}$ , $\text{ADC REFIN} = 5\text{V}$ |
| PGA849 reference pin                             | $V_{\text{REF}} = 2.5\text{V}$                                                                            |
| Full-scale range of ADC                          | $\text{FSR} = 5\text{V}$                                                                                  |
| Sampling rate of ADC                             | $f_{\text{SAMPLE}} = 1\text{MSPS}$                                                                        |
| PGA gain                                         | 0.125, 0.25, 0.5, 1, 2, 4, 8, 16                                                                          |
| Input voltages ( $V_{\text{PP}}$ , differential) | 25V, 16V, 8V, 4V, 2V, 1V, 0.5V, 0.25V                                                                     |
| Signal frequency                                 | 1kHz                                                                                                      |
| RC kickback filter                               | $R_{\text{FIL}} = 15\Omega$ , $C_{\text{DIFF}} = 1.2\text{nF}$ , $C_{\text{CM}} = 120\text{pF}$           |

### 8.2.1.2 Detailed Design Procedure

The first filter located at the input of the PGA (see [Figure 8-9](#)) helps reduce electromagnetic interference (EMI) and radio frequency interference (RFI), high-frequency, extrinsic noise. This filter can be customized per the application bandwidth and antialiasing requirements.

The second filter is provided by  $C_{\text{FB}}$  in parallel with the PGA 5k $\Omega$  feedback resistors. The PGA resistors are  $\pm 15\%$  absolute tolerance, as such, consider the effect of the tolerance on the filter cutoff frequency.  $C_{\text{FB}} = 100\text{pF}$  results in a filter cutoff frequency of 318kHz. On the high side of the resistor tolerance, the filter frequency changes to 277kHz. The device allows for the flexibility to modify the  $C_{\text{FB}}$  capacitor value to adjust bandwidth, with a trade-off on the broadband noise of the circuit.

The third filter placed at the ADS8860 inputs works as a charge reservoir filter to drive the SAR ADC. The charge kickback filter reduces the instantaneous charge demand of the amplifier, maintaining low distortion that otherwise can degrade because of incomplete ADC sample-and-hold settling. The RC filter combination ( $R_{\text{FIL}}$ ,  $C_{\text{DIFF}}$ ) is tuned for ADC sample-and-hold settling and total harmonic distortion (THD) performance, while maintaining stability of the PGA. High-grade C0G capacitors are used everywhere in the signal path for the low distortion properties.

The PGA849 front-end, accounting for all three filters, provides a nominal  $f_{-3\text{dB}}$  bandwidth of 310kHz. On the high side of the internal 5k $\Omega$  feedback resistor tolerance, the PGA849  $f_{-3\text{dB}}$  bandwidth changes to 271kHz and the circuit maintains  $-0.1\text{dB}$  flatness to 41kHz.

The ADS8860 requires a full-scale input in the range of 0V to the 5V ADC reference. The PGA849 REF pin is set to a nominal voltage of 2.5V to shift the signal to the ADC midscale voltage.

The PGA849 REF voltage is generated by feeding the REF6250 5V reference through a 10k $\Omega$ -to-10k $\Omega$  precision voltage divider implemented with  $\pm 0.05\%$  tolerance, low-drift  $\pm 5\text{ppm}/^\circ\text{C}$  resistors. Drive the PGA849 REF pin with a low-impedance source, and use an op amp like the OPA192 as a buffer to drive the REF pin.

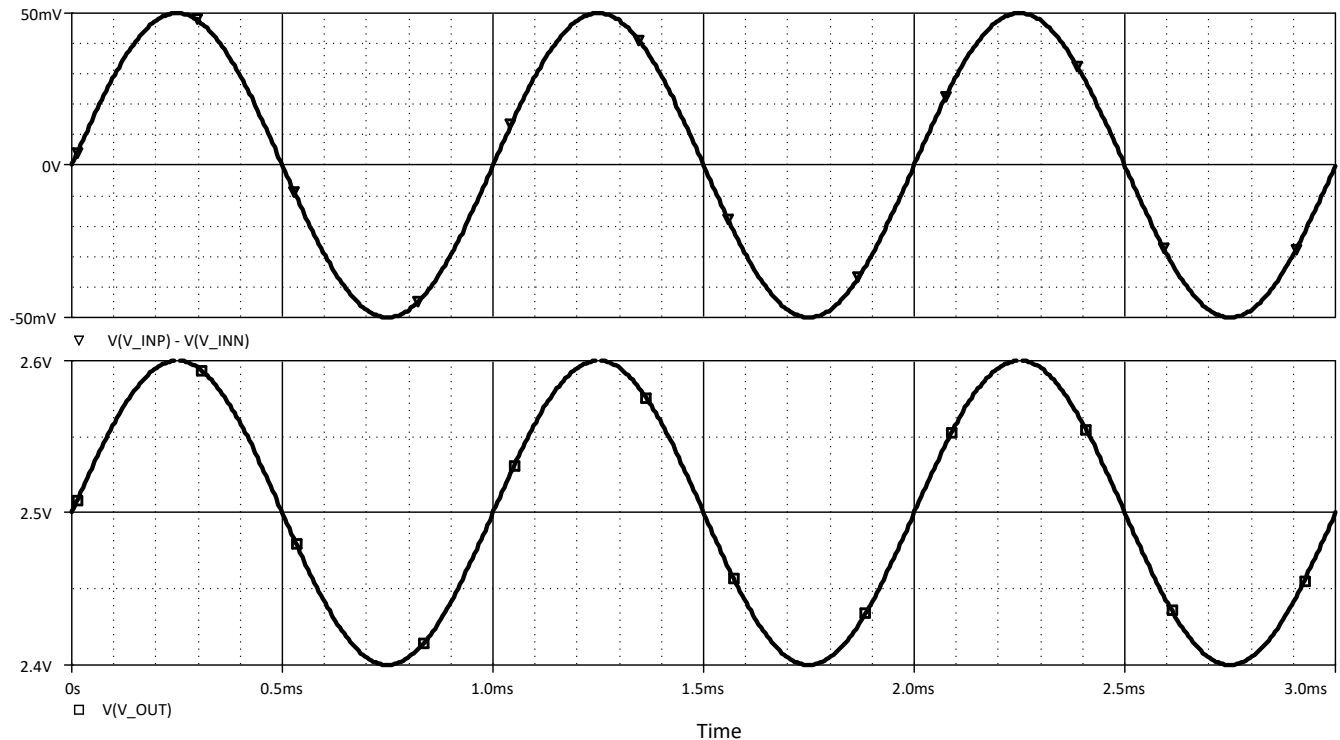
The OPA192 buffer is configured in a dual-feedback configuration to provide stability while driving the REF pin and 22nF bypass capacitor.  $R_{ISO}$  is a 20 $\Omega$  isolation resistor that provides separation of two feedback paths for optimized stability. Feedback path number one is through feedback resistor,  $R_F = 2k\Omega$ , connected directly to the REF pin. Feedback path number two is through feedback capacitor  $C_F = 2nF$  connected to the output of the op amp. The circuit provides a loop gain phase margin of 86°. The noninverting input of the OPA192 buffer has a low-pass filter with  $R = 1k\Omega$ ,  $C = 10nF$  to reduce the resistive divider thermal noise. Using any other load capacitance requires recalculation of the stability components:  $R_F$ ,  $C_F$ , and  $R_{ISO}$ . If modifying the REF bypass capacitance, verify the circuit is stable with simulation using the OPA192 TINA-TI model (or PSpice®-for-TI model), and confirm the circuit provides more than 60° of phase margin.

### 8.2.1.3 Application Curves

表 8-2 lists the PGA849 output voltage with different gain configurations, and 図 8-10 shows the PGA849 output voltage with a gain of 2.

**表 8-2. PGA849 Output Voltage with Different Gain Configurations**

| Input (mV) | Reference (V) | A2:A0 | PGA Gain (V/V) | Minimum Output (V) | Maximum Output (V) |
|------------|---------------|-------|----------------|--------------------|--------------------|
| $\pm 50$   | 2.5           | 000   | 0.125          | 2.494              | 2.506              |
|            |               | 001   | 0.25           | 2.488              | 2.512              |
|            |               | 010   | 0.5            | 2.475              | 2.525              |
|            |               | 011   | 1              | 2.450              | 2.550              |
|            |               | 100   | 2              | 2.400              | 2.600              |
|            |               | 101   | 4              | 2.300              | 2.700              |
|            |               | 110   | 8              | 2.100              | 2.900              |
|            |               | 111   | 16             | 1.700              | 3.300              |



**図 8-10. PGA849 Output Voltage with a Gain of 2, Reference = 2.5V**

## 8.3 Power Supply Recommendations

The nominal performance of the PGA849 is specified with input-stage supply and output-stage supply voltages of  $\pm 15\text{V}$ , and  $V_{\text{ICM}}$  and  $V_{\text{REF}}$  at mid-supply. Within the specified limits, custom input common-mode and output reference voltages can be used without compromising performance; see also [セクション 6.3](#). To prevent damage to internal circuitry, the output-stage power supplies are clamped to stay within the input-stage supply voltage levels; see also [セクション 7.2](#).

### 注意

Supply voltages higher than 40V ( $\pm 20\text{V}$ ) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in [セクション 6.6](#) of this data sheet.

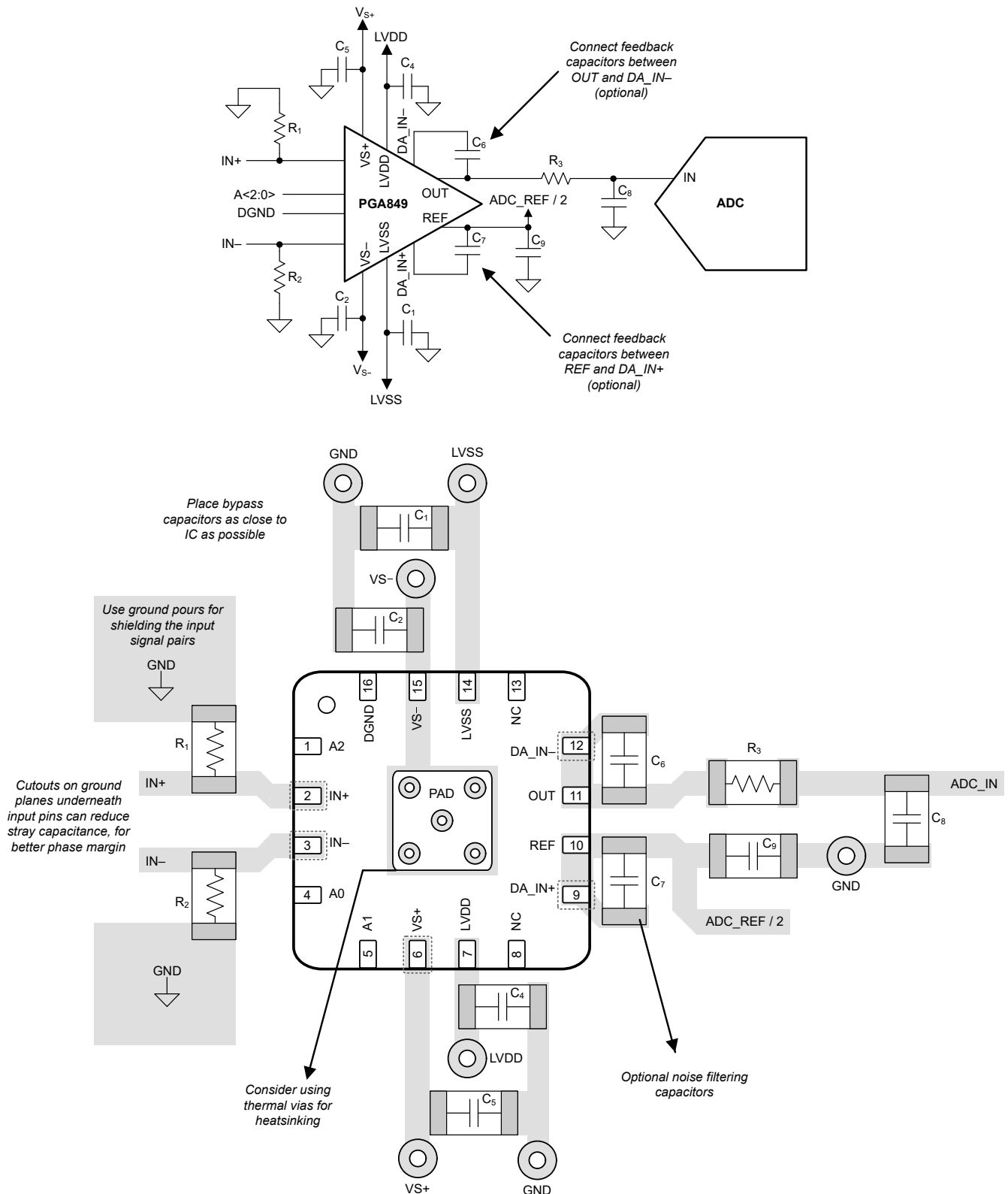
## 8.4 Layout

### 8.4.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- To avoid converting common-mode signals into differential signals and thermal electromotive forces (EMFs), make sure that both input paths are symmetrical and well-matched for source impedance and capacitance.
- Noise can propagate into analog circuitry through the power pins of the device and of the circuit as a whole. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1 $\mu\text{F}$  ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from  $V+$  to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Leakage on the DA\_IN+ and DA\_IN– pins can cause in a dc offset error in the output voltages. Additionally, excessive parasitic capacitance at these pins can result in decreased phase margin and affect the stability of the output stage. If these pins are not used to implement deliberate capacitive feedback, follow best practices to minimize leakage and parasitic capacitance.
- Follow best practices to minimize leakage and parasitic capacitance, which includes implementing *keep-out* areas in any ground planes that lie immediately below the input pins.
- Minimize the number of thermal junctions. If possible, route the signal path using a single layer without vias.
- Keep sufficient distance from major thermal energy sources (circuits with high power dissipation). If not possible, place the device so that the effects of the thermal energy source on the high and low sides of the differential signal path are evenly matched.
- Keep the traces as short as possible.

## 8.4.2 Layout Example



**Figure 8-11. Example Schematic and Associated PCB Layout**

## 9 Device and Documentation Support

### 9.1 Device Support

#### 9.1.1 Development Support

##### 9.1.1.1 PSpice® for TI

**PSpice® for TI** is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

##### 9.1.1.2 TINA-TI™ シミュレーション ソフトウェア (無償ダウンロード)

TINA-TI™ シミュレーション ソフトウェアは、SPICE エンジンに基づいた単純かつ強力な、使いやすい回路シミュレーション プログラムです。TINA-TI シミュレーション ソフトウェアは、TINA™ ソフトウェアのすべての機能を持つ無償バージョンで、パッシブ モデルとアクティブ モデルに加えて、マクロモデルのライブラリがプリロードされています。TINA-TI シミュレーション ソフトウェアには、SPICE の標準的な DC 解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

TINA-TI シミュレーション ソフトウェアは[設計およびシミュレーション ツール Web ページ](#)から無料でダウンロードでき、ユーザーが結果をさまざまな形式で処理できる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック スタート ツールを作成できます。

#### 注

これらのファイルを使用するには、TINA ソフトウェアまたは TINA-TI ソフトウェアがインストールされている必要があります。[TINA-TI™ ソフトウェア フォルダ](#)から、無償の TINA-TI シミュレーション ソフトウェアをダウンロードしてください。

### 9.2 Documentation Support

#### 9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Comprehensive Error Calculation for Instrumentation Amplifiers application note](#)
- Texas Instruments, [Importance of Input Bias Current Return Paths in Instrumentation Amplifier Applications application note](#)

### 9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

### 9.4 サポート・リソース

[テキサス・インスツルメンツ E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

### 9.5 Trademarks

TINA-TI™ and テキサス・インスツルメンツ E2E™ are trademarks of Texas Instruments.

TINA™ is a trademark of DesignSoft, Inc.

PSpice® is a registered trademark of Cadence Design Systems, Inc.

すべての商標は、それぞれの所有者に帰属します。

## 9.6 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 9.7 用語集

**テキサス・インスツルメンツ用語集**      この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision * (March 2024) to Revision A (December 2024) | Page |
|--------------------------------------------------------------------|------|
| • ドキュメントのステータスを「事前情報」から「量産データ」に変更.....                             | 1    |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number      | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">PGA849RGTR</a> | Active        | Production           | VQFN (RGT)   16 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | PGA849              |
| PGA849RGTR.B               | Active        | Production           | VQFN (RGT)   16 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | PGA849              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

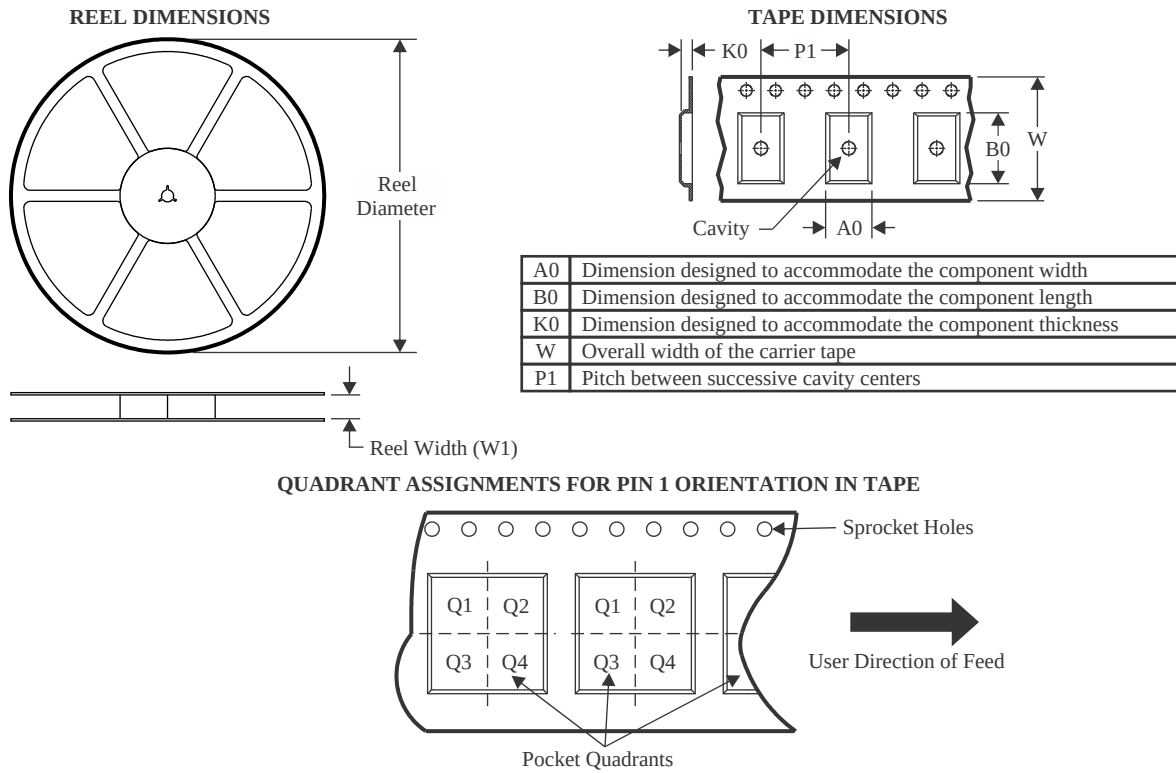
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



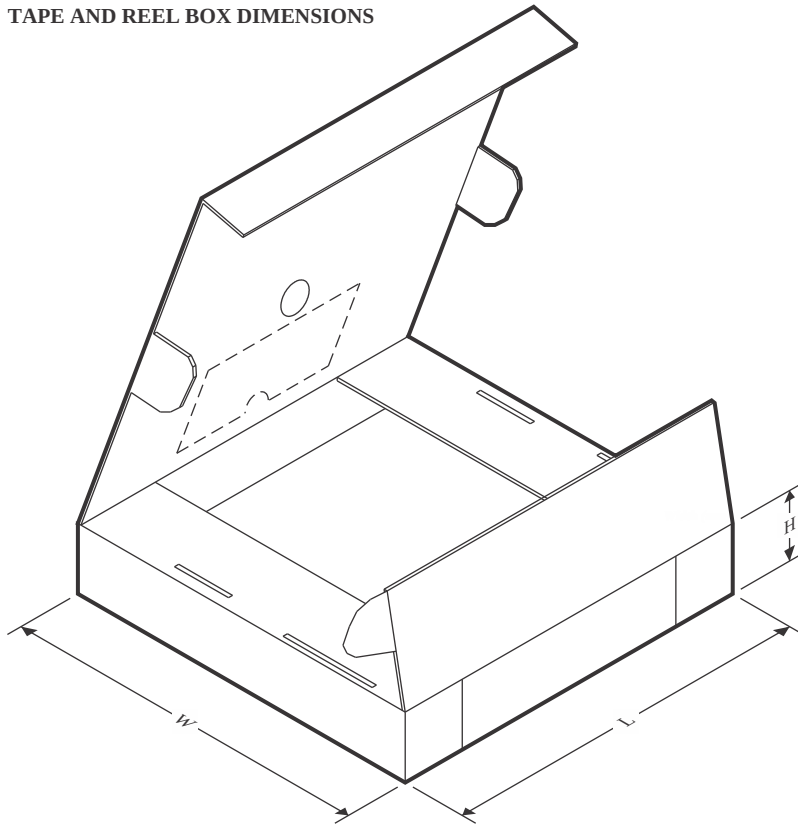
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| PGA849RGTR | VQFN         | RGT             | 16   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

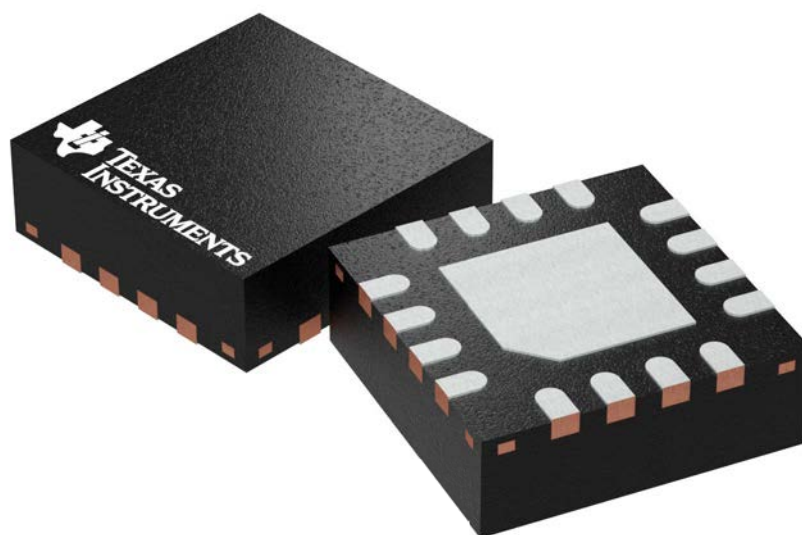
| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| PGA849RGTR | VQFN         | RGT             | 16   | 3000 | 367.0       | 367.0      | 35.0        |

**RGT 16**

**GENERIC PACKAGE VIEW**

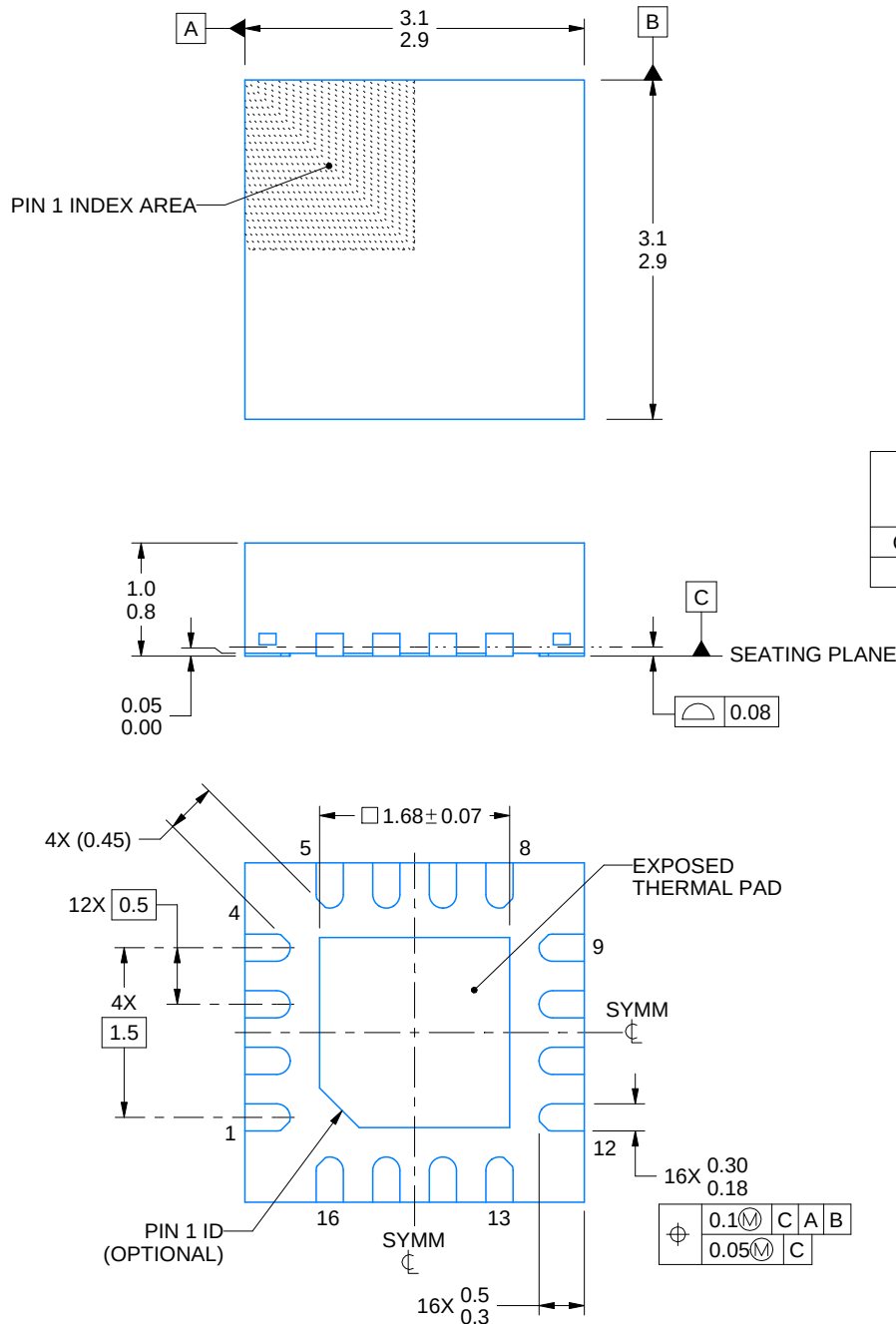
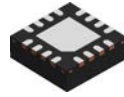
**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4203495/1



4222419/E 07/2025

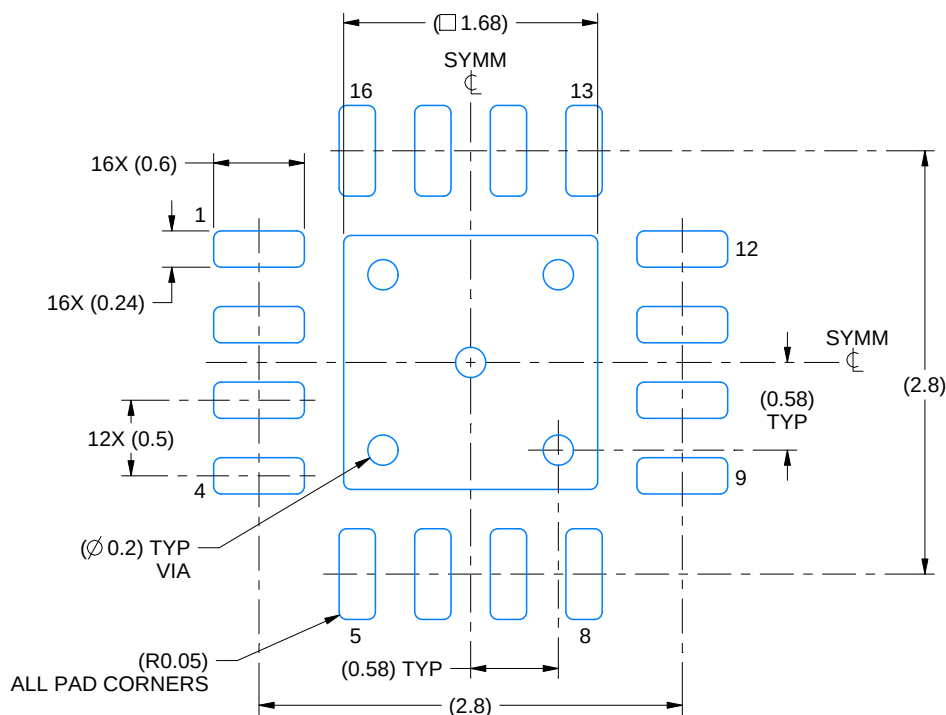
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

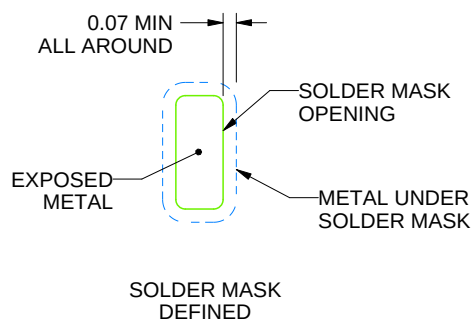
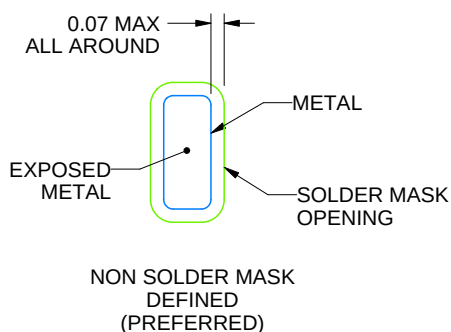
**RGT0016C**

### VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



## SOLDER MASK DETAILS

4222419/E 07/2025

NOTES: (continued)

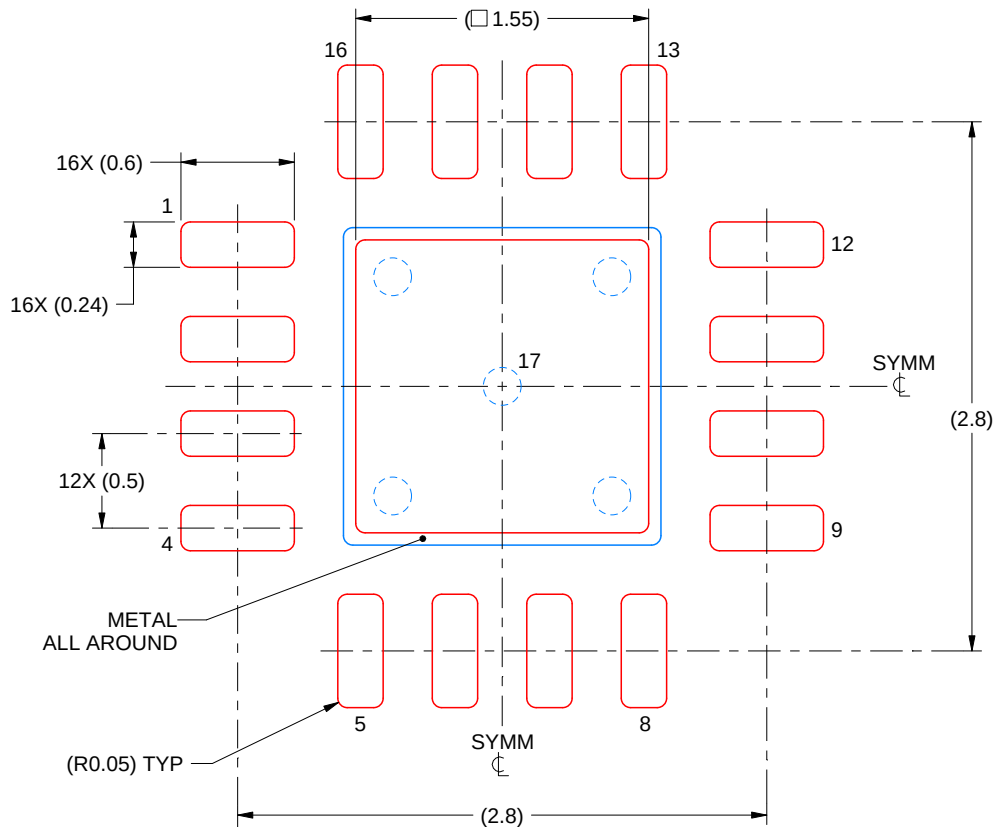
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:  
 85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE:25X

4222419/E 07/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含みいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](https://www.ti.com) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月