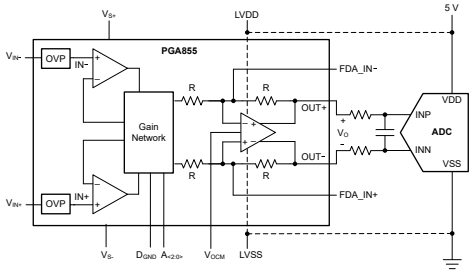
PGA855 低ノイズ、広帯域、完全差動出力、プログラマブル・ゲイン計測アンプ

1 特長

- 8 つのピン・プログラマブル・バイナリ・ゲイン
  - G (V/V) = ⅛、¼、½、1、2、4、8、および 16
- "Low" ゲイン誤差ドリフト：G = 1V/V で 1ppm/°C (最大値)
- 完全差動出力
  - ADC 入力のオーバードライブ保護を可能にする独立した出力電源ピン
  - 出力同相モード制御
- 高速信号処理：
  - 広い帯域幅：10MHz (すべてのゲイン)
  - 高いスルーレート：35V/µs
  - セトリング・タイム：
    誤差 0.01% まで 500ns、0.0015% まで 950ns
  - 入力段ノイズ：G = 16V/V 時に 7.8nV/√Hz
  - SNR を向上させるフィルタ・オプション
- 高低の電源電圧に対して ±40V までの入力過電圧保護機能
- 入力段電源電圧範囲：
  - 単一電源：8V～36V
  - デュアル電源：±4V～±18V
- 出力段電源電圧範囲：
  - 単一電源：4.5V～36V
  - デュアル電源：±2.25V～±18V
- 仕様温度範囲：-40°C～+125°C
- 小型パッケージ：3mm × 3mm VQFN

2 アプリケーション

- ファクトリ・オートメーションおよび制御
- アナログ入力モジュール
- データ・アクイジション (DAQ)
- 試験および測定機器
- 半導体試験装置



PGA855 のアプリケーション概略図

3 概要

PGA855 は、完全差動出力を備えた高帯域のプログラマブル・ゲイン計測アンプです。PGA855 は、3 本のデジタル・ゲイン選択ピンを使用して、0.125V/V の減衰ゲインから最大 16V/V まで、8 つのバイナリ・ゲイン設定を備えています。出力同相電圧は、VOCM ピンを使用して個別に設定できます。

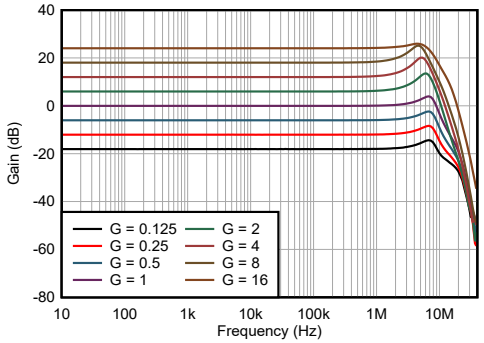
PGA855 アーキテクチャは、追加の ADC ドライバを必要とせずに、最大 1MSPS のサンプリング・レートで高分解能、高精度の A/D コンバータ (ADC) の入力を駆動するように最適化されています。出力段電源 (LVSS/LVDD) は入力段からデカップリングされており、ADC の電源に接続することで、オーバードライブによる損傷から ADC や下流のデバイスを保護できます。

スーパーベータ入力トランジスタが提供する入力バイアス電流は非常に低く、それにより入力電流ノイズ密度が 0.3pA/√Hz と非常に低くなるため、PGA855 は、事実上あらゆる種類のセンサに対応する汎用性の高い選択肢になっています。低ノイズの電流フィードバック・フロントエンド・アーキテクチャにより、高周波数でも優れたゲイン平坦性を実現しているため、PGA855 は、優れた高インピーダンスのセンサ読み出しデバイスとなります。入力ピンに保護回路が内蔵されており、電源電圧を最大±40V 上回る過電圧に対処できます。

パッケージ情報

部品番号	パッケージ(1)	パッケージ・サイズ(2)
PGA855	RGT (VQFN、16)	3mm × 3mm

(1) 利用可能なパッケージについては、パッケージ・オプションについての付録を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



ゲインと周波数との関係

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (September 2023) to Revision B (September 2023)	Page
• 「概要」セクションで 4MSPS を 1MSPS に変更	1
• Changed 4 MSPS to 1 MSPS in *Overview* section	21

Changes from Revision * (April 2023) to Revision A (September 2023)	Page
• PGA855 のステータスを事前情報 (プレビュー) から量産データ (アクティブ) に変更	1

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5 Device Comparison Table

DEVICE	DESCRIPTION	GAIN EQUATION	RG PINS AT PIN
INA849	Ultra-low-noise (1-nV/√Hz), high-bandwidth instrumentation amplifier	G = 1 + 6 kΩ / RG	2, 3
INA851	Low-noise (3.2 nV/√Hz), high-speed (22 MHz), fully-differential instrumentation amp with overvoltage protection (±40 V)	G = 1 + 6 kΩ / RG	2, 3
PGA280	20-mV to ±10-V programmable gain instrumentation amplifier with 3-V or 5-V differential output; analog supply up to ±18 V	Digitally programmable with SPI	N/A
PGA281	Zero-drift, high-voltage programmable gain amplifier	Digitally pin-programmable	N/A

6 Pin Configuration and Functions

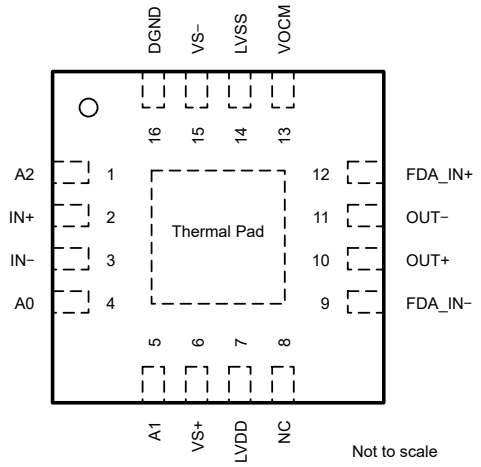


図 6-1. RGT Package, 16-Pin VQFN (Top View)

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A0	4	Input	Gain option pin 0
A1	5	Input	Gain option pin 1
A2	1	Input	Gain option pin 2
DGND	16	Power	Ground reference for digital logic and gain setting pins
FDA_IN–	9	Input	Connection to output driver summing node
FDA_IN+	12	Input	Connection to output driver summing node
IN–	3	Input	Negative (inverting) input
IN+	2	Input	Positive (noninverting) input
LVDD	7	Power	Output driver positive supply. Connect this pin to the positive supply of the ADC to protect from overdriving.
LVSS	14	Power	Output driver negative supply. Connect this pin to the negative supply of the ADC to protect from overdriving.
NC	8	—	Do not connect
OUT–	11	Output	Output (inverting)
OUT+	10	Output	Output (noninverting)
VOCM	13	Input	Level set for output common mode value
VS+	6	Power	Input stage positive supply
VS–	15	Power	Input stage negative supply

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表 6-1. Pin Functions (続き)

PIN		TYPE	DESCRIPTION
NAME	NO.		
Thermal Pad	Thermal pad	—	The thermal pad must be soldered to the printed-circuit board (PCB). Connect thermal pad to a plane or large copper pour that is either floating or electrically connected to VS–, even for applications that have low power dissipation.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage on V_{S+}, $V_{S–}$ pins; $V_S = (V_{S+}) – (V_{S–})$	0	40	V
V_{SOUT}	Supply voltage on LVDD, LVSS pins; $V_{SOUT} = V_{LVDD} – V_{LVSS}$	0	40	V
	Voltage on power pins LVDD, LVSS	$(V_{S–}) – 0.5$	$(V_{S+}) + 0.5$	V
V_{IN}	Voltage on signal-input pins IN+, IN–	$(V_{S–}) – 40$	$(V_{S+}) + 40$	V
	DGND, FDA_IN+, FDA_IN– pin voltage	$(V_{S–}) – 0.5$	$(V_{S+}) + 0.5$	V
	Voltage on gain-select pins A2, A1, A0	$V_{DGND} – 0.5$	$(V_{S+}) + 0.5$	V
V_O	Signal output pins maximum voltage on OUT+, OUT–	$V_{LVSS} – 0.5$	$V_{LVDD} + 0.5$	V
V_{OCM}	Output common-mode voltage	$V_{LVSS} – 0.5$	$V_{LVDD} + 0.5$	V
I_O	Signal-output pins current	–100	100	mA
I_{SC}	Output short-circuit current(2)	Continuous		
T_A	Operating temperature	–50	150	°C
T_J	Junction Temperature		175	°C
T_{stg}	Storage Temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to V_{SOUT} / 2.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Input stage supply voltage	Single supply	8	36	V
		Dual supply	±4	±18	
V_{SOUT}	Output stage supply voltage	Single supply	4.5	36	V
		Dual supply	±2.25	±18	
T_A	Specified temperature		–40	125	°C

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7.4 Thermal Information

THERMAL METRIC[1]		PGA855 RGT (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.8	°C/W

(1) For information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

at T_A = 25 °C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} is at mid-supply, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Differential offset voltage (input referred)	G = 1 to 16			±70	±350	µV
		G < 1			±70/G	±350/G	
	Differential offset voltage drift (input referred)	G = 1 to 16, T_A = –40°C to +125°C			±0.3	±1.0	µV/°C
		G < 1, T_A = –40°C to +125°C			±0.3/G	±1.0/G	
PSRR	Power-supply rejection ratio	±4 V ≤ V_S ≤ ±18 V, RTI	G = 0.125	102	108		dB
			G = 0.25	108	114		dB
			G = 0.5	114	120		
			G = 1	120	126		
			G = 2	120	126		
			G = 4	120	132		
			G = 8	120	136		
			G = 16	120	140		
z_{id}	Differential impedance				100 || 1		GΩ || pF
z_{ic}	Common-mode impedance				100 || 7		GΩ || pF
V_I	Input voltage	V_S = ±4 V to ±18 V, T_A = –40°C to +125°C		($V_{S–}$) + 2.5		(V_{S+}) – 2.5	V
CMRR	Common-mode rejection ratio	At dc to 60 Hz, V_{ICM} = ± 10 V, T_A = –40°C to +125°C, RTI	G = 0.125	64	82		dB
			G = 0.25	70	88		
			G = 0.5	76	94		
			G = 1	82	100		
			G = 2	88	106		
			G = 4	94	112		
			G = 8	100	118		
			G = 16	106	124		
BIAS CURRENT							
I_B	Input bias current				0.5	1.8	nA
		T_A = –40°C to +125°C			1		
	Input bias current drift	T_A = –40°C to +125°C				10	pA/°C
I_{OS}	Input offset current				0.5	1	nA
		T_A = –40°C to +125°C			1		
	Input offset current drift	T_A = –40°C to +125°C				10	pA/°C

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7.5 Electrical Characteristics (続き)

at T_A = 25 °C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} is at mid-supply, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE VOLTAGE							
e_{NI}	Input-referred voltage noise density	f = 1 kHz	G = 16		7.8		nV/√Hz
			G = 8		8.0		
			G = 4		8.6		
			G = 2		12.6		
			G = 1		21.6		
			G = 0.5		42		
			G = 0.25		84		
			G = 0.125		168		
E_{NI}	Input-referred voltage noise	f_B = 0.1 Hz to 10 Hz	G = 16		0.26		μV_{PP}
			G = 8		0.27		
			G = 4		0.29		
			G = 2		0.44		
			G = 1		0.8		
			G = 0.5		1.6		
			G = 0.25		3.2		
			G = 0.125		6.4		
i_N	Input current noise density	f = 1 kHz			0.3		pA/√Hz
I_N	Input current noise	f_B = 0.1 Hz to 10 Hz			13		pA_{PP}
GAIN							
	Differential gain range			0.125		16	V/V
GE	Differential gain error	G = 0.25, 0.5, 2, 4			±0.02	±0.05	%
		G = 1			±0.02	±0.03	
		G = 0.125, 8, 16			±0.03	±0.07	
	Differential gain drift	G = 1, T_A = –40°C to +125°C				±1	ppm/°C
		G = 0.125, 0.25, 0.5, 2, 4, 8, 16, T_A = –40°C to +125°C				±2	
	Differential gain nonlinearity	G = 0.125 to 16, $V_{OUTDIFF}$ = 10 V			2	5	ppm
			T_A = –40°C to +125°C			10	
OUTPUT							
V_{OUT}	Output voltage	No load	V_{SOUT} = ±2.25 V	V_{LVSS} + 0.1		V_{LVDD} – 0.1	V
		R_L = 10 kΩ	V_{SOUT} = ±2.25 V	V_{LVSS} + 0.2		V_{LVDD} – 0.2	
			V_{SOUT} = ±18V	V_{LVSS} + 0.4		V_{LVDD} – 0.4	
C_L	Load capacitance	Stable operation for differential load			50		pF
I_{SC}	Short-circuit current	Continuous to V_{SOUT} / 2			±45		mA
			T_A = –40°C to +125°C	±20		±60	
FREQUENCY RESPONSE							
BW	Bandwidth, –3 dB	G = 0.125 to 16			10		MHz
SR	Slew rate	G = 0.125 to 16, $V_{OUTDIFF}$ > 5 V			35		V/µs
t_S	Settling time	G = 0.125 to 16 V_{INDIFF} = 10-V step or $V_{OUTDIFF}$ = 10-V step	To 0.01%		0.7		µs
			To 0.0015%		0.95		
	Gain switching time				2		µs
THD+N	Total harmonic distortion and Noise	Differential input, f = 10 kHz, V_O = 10 V_{PP}			–110		dB
		Single-ended input, f = 10 kHz, V_O = 10 V_{PP}			–105		
HD2	Second-order harmonic distortion	Differential input, f = 10 kHz, V_O = 10 V_{PP}			–120		dB
		Single-ended input, f = 10 kHz, V_O = 10 V_{PP}			–110		
HD3	Third-order harmonic distortion	Differential input, f = 10 kHz, V_O = 10 V_{PP}			–120		dB
		Single-ended input, f = 10 kHz, V_O = 10 V_{PP}			–110		

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7.5 Electrical Characteristics (続き)

at T_A = 25 °C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} is at mid-supply, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT COMMON-MODE VOLTAGE (V_{OCM}) CONTROL						
V_{OCM}	Common-mode input voltage	V_S = ±4 V	V_{LVSS} + 1.5		V_{LVDD} – 1.5	V
		V_S = ±18 V	V_{LVSS} + 2		V_{LVDD} – 2	
	Small-signal bandwidth V_{OCM} pin	V_{OCM} = 100 mV_{PP}		16		MHz
	Large-signal bandwidth V_{OCM} pin	V_{OCM} = 0.6 V_{PP}		16		MHz
	DC output balance	V_{OCM} fixed at mid-supply (V_O = ±1 V)		70		dB
	Input impedance V_{VOCM} pin			250 || 1		kΩ || pF
	V_{OCM} offset from mid-supply	VOCM pin floating		±1	±3.5	mV
	V_{OCM} offset voltage	V_{OCM} = V_{ICM}, V_O = 0 V		±1	±3.5	mV
	V_{OCM} offset voltage drift	V_{OCM} = V_{ICM}, V_O = 0 V, T_A = –40°C to +125°C		±20	±40	µV/°C
INPUT STAGE POWER SUPPLY						
I_{Q_input}	Input stage quiescent current V_{S+}, $V_{S–}$	V_{IN} = 0 V		3	3.7	mA
		T_A = –40°C to +125°C			4.5	
OUTPUT STAGE POWER SUPPLY						
I_{Q_output}	Output stage quiescent current V_{LVDD}, V_{LVSS}	V_{IN} = 0 V, V_{OCM} fixed at mid-supply		2.3	2.8	mA
		T_A = –40°C to 125°C			3.5	
DIGITAL LOGIC						
V_{IL}	Digital input logic low	A0, A1, A2 pins, referred to DGND	V_{DGND}		V_{DGND} + 0.8	V
V_{IH}	Digital input logic high	A0, A1, A2 pins, referred to DGND	V_{DGND} + 1.8		V_{S+}	V
	Digital input pin current	A0, A1, A2 pins		1.5	3	µA
V_{DGND}	DGND voltage		$V_{S–}$		(V_{S+}) – 4	V
	DGND reference current			4	10	µA

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7.6 Typical Characteristics

at T_A = 25°C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} = 0 V, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)

表 7-1. Table of Graphs

DESCRIPTION	FIGURE
Distribution of Offset Voltage (RTI), G = 16 V/V	図 7-1
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Distribution of Offset Voltage (RTI), G = 1 V/V	図 7-3
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0.1-Hz to 10-Hz Voltage Noise (RTI), G = 0.125 V/V	図 7-38
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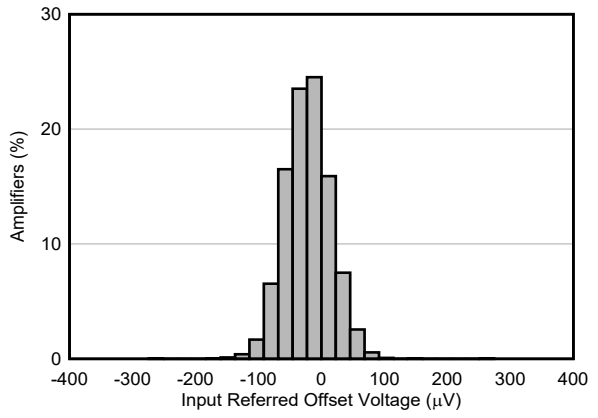
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7.6 Typical Characteristics

at T_A = 25°C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} = 0 V, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)

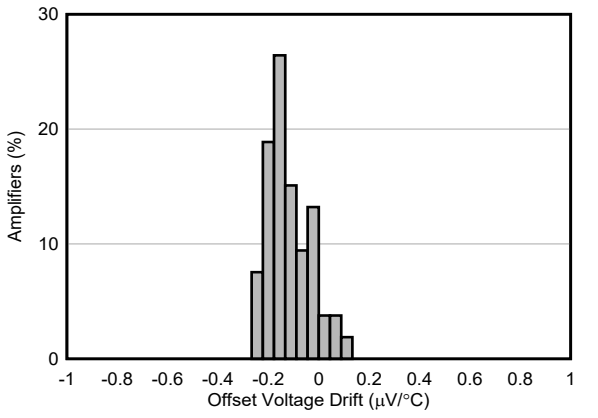
表 7-1. Table of Graphs (続き)

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N = 2500 Mean = –21.25 µV Std. dev. = 36.79 µV
G = 16 V/V

図 7-1. Distribution of Offset Voltage (RTI)



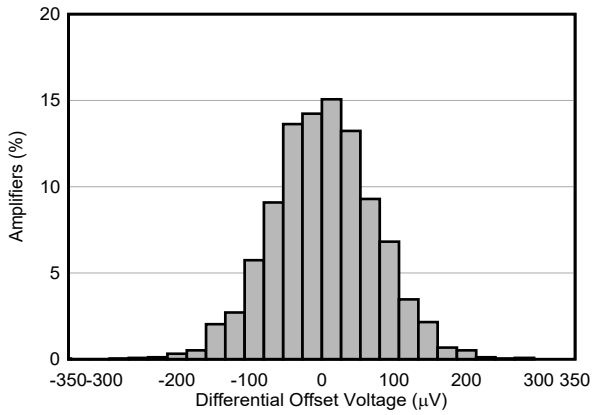
N = 53 Mean = –0.11 µV/°C Std. dev. = 0.08 µV/°C
G = 16 V/V

図 7-2. Distribution of Offset Voltage Drift (RTI)

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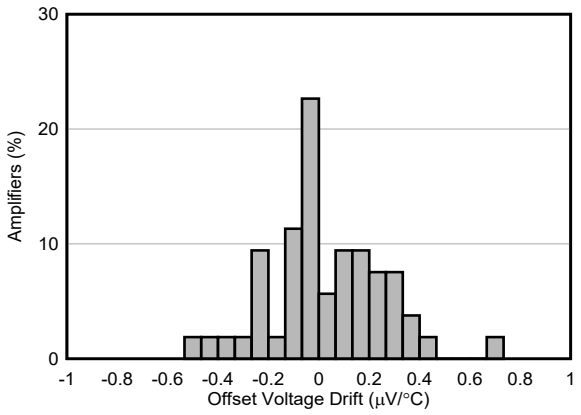
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} = 0 V, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)



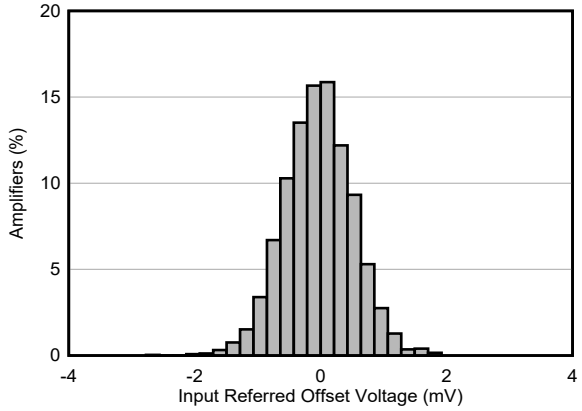
N = 2500 Mean = 2.83 µV Std. dev. = 71.58 µV
G = 1 V/V

図 7-3. Distribution of Offset Voltage (RTI)



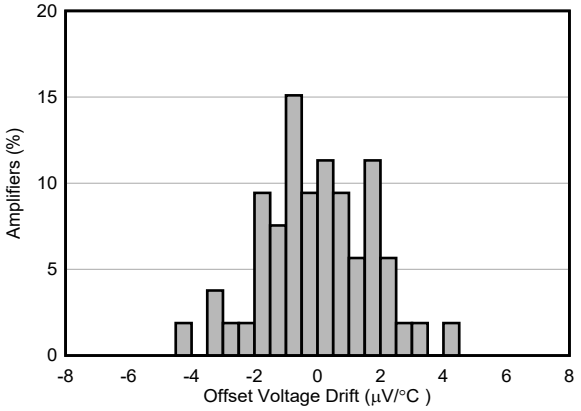
N = 53 Mean = –0.024 µV/°C Std. dev. = 0.22 µV/°C
G = 1 V/V

図 7-4. Distribution of Offset Voltage Drift (RTI)



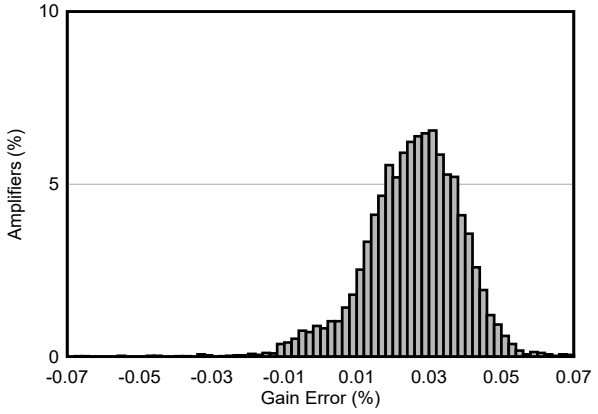
N = 2500 Mean = –36 µV Std. dev. = 540 µV
G = 0.125 V/V

図 7-5. Distribution of Offset Voltage (RTI)



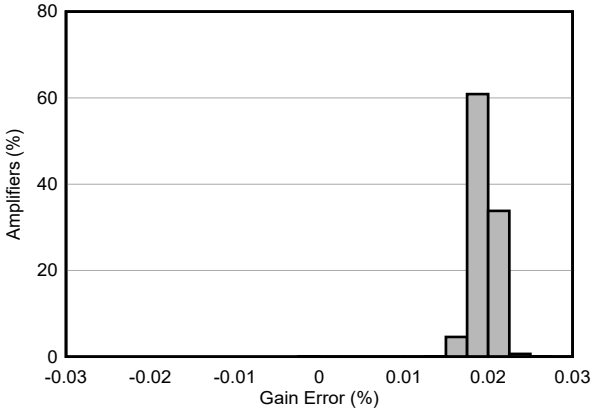
N = 53 Mean = –0.028 µV/°C Std. dev. = 1.69 µV/°C
G = 0.125 V/V

図 7-6. Distribution of Offset Voltage Drift (RTI)



N = 7295 Mean = 0.0257 % Std. dev. = 0.0136 %
G = 16 V/V

図 7-7. Distribution of Differential Gain Error



N = 7295 Mean = 0.0195 % Std. dev. = 0.0012 %
G = 1 V/V

図 7-8. Distribution of Differential Gain Error

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7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} = 0 V, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)

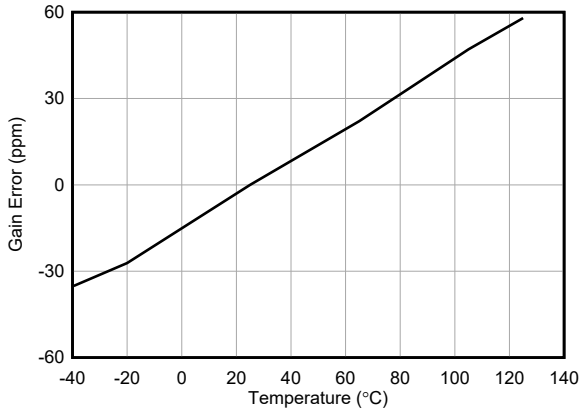
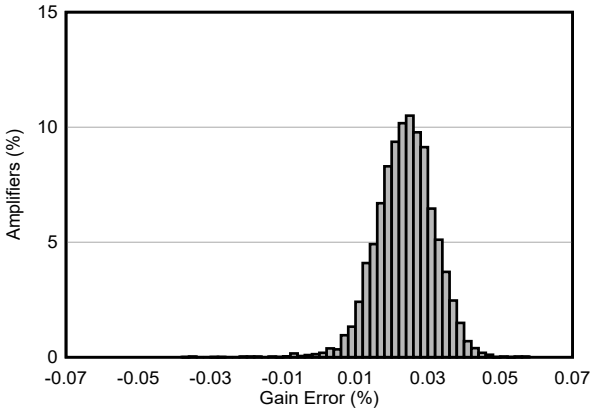
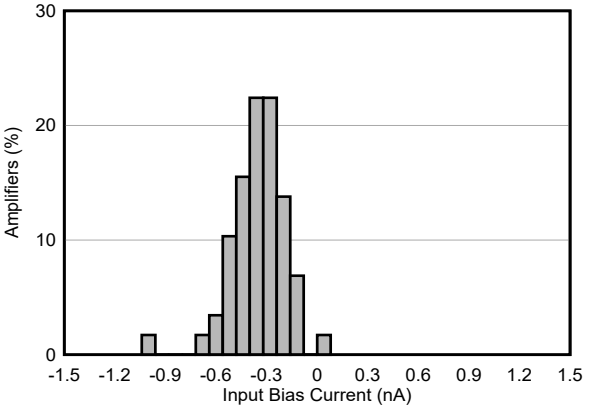


図 7-9. Gain Error vs Temperature



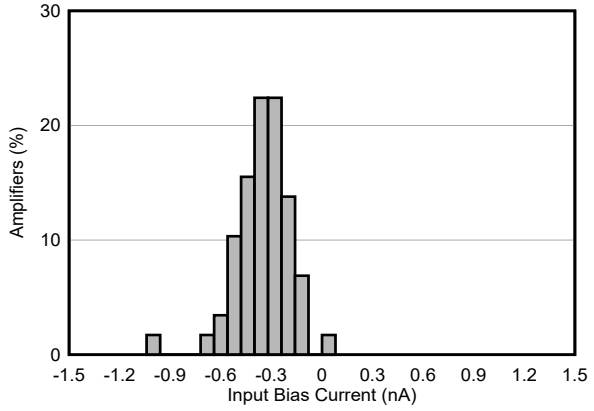
N = 7295 Mean = 0.0238% Std. dev. = 0.008%
G = 0.125 V/V

図 7-10. Distribution of Differential Gain Error



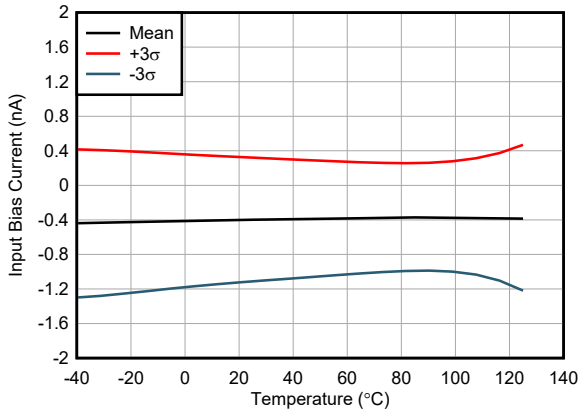
N = 59 Mean = –0.37 nA Std. dev. = 0.183 nA

図 7-11. Distribution of Input Bias Current



N = 59 Mean = –0.34 nA Std. dev. = 0.16 nA
T_A = 85°C

図 7-12. Distribution of Input Bias Current



59 units, 1 wafer lot

図 7-13. Input Bias Current vs Temperature

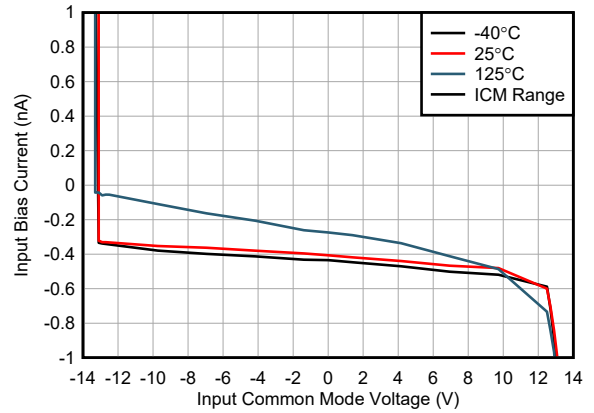
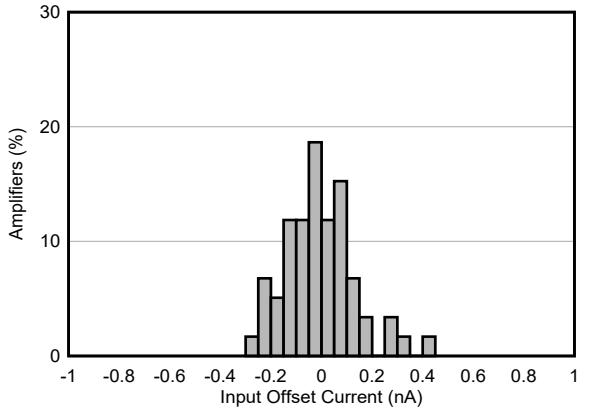


図 7-14. Input Bias Current vs Input Common-Mode Voltage

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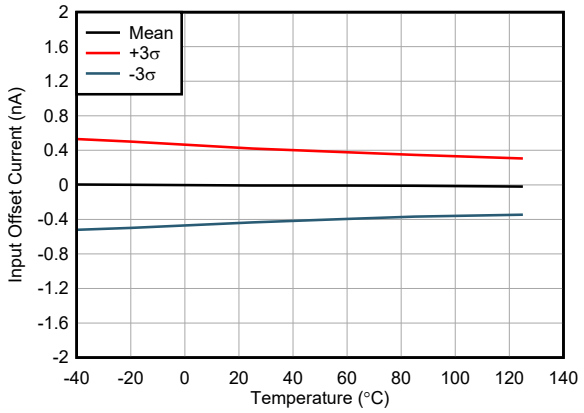
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} = 0 V, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)



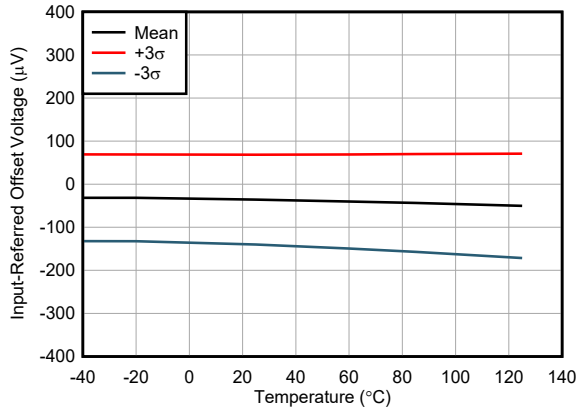
N = 59 Mean = –0.007 nA Std. dev. = 0.142 nA

図 7-15. Distribution of Input Offset Current



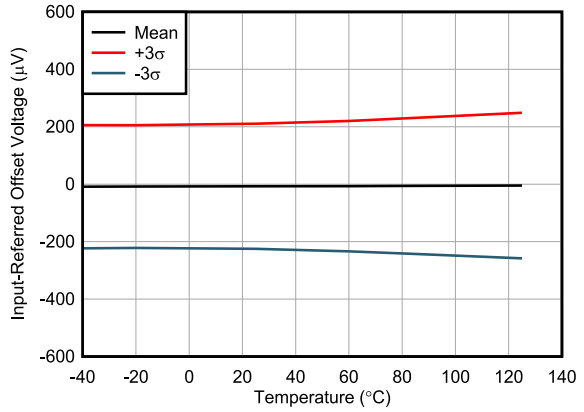
59 units, 1 wafer lot

図 7-16. Input Offset Current vs Temperature



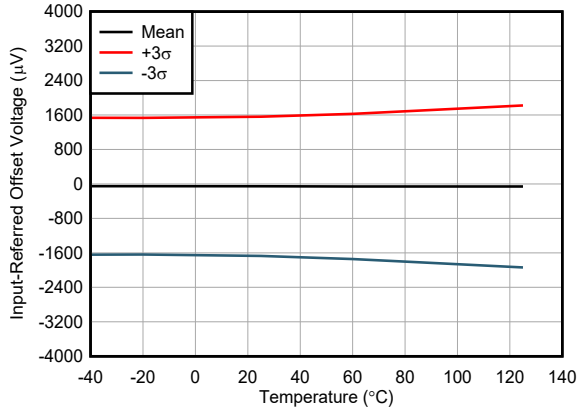
G = 16 V/V 53 units, 1 wafer lot

図 7-17. Offset Voltage (RTI) vs Temperature



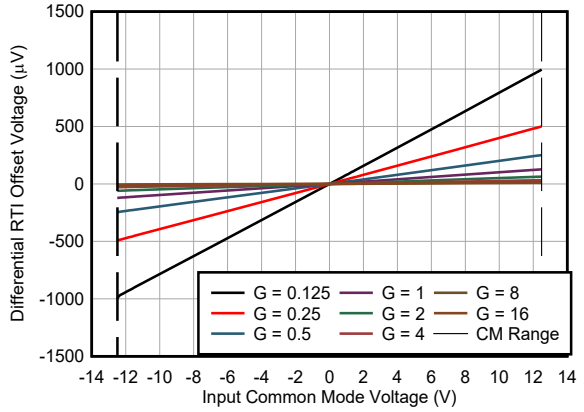
G = 1 V/V 53 units, 1 wafer lot

図 7-18. Offset Voltage (RTI) vs Temperature



G = 0.125 V/V 53 units, 1 wafer lot

図 7-19. Offset Voltage (RTI) vs Temperature



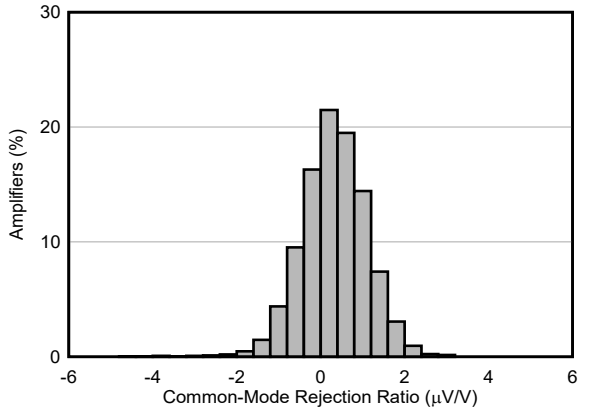
Typical unit shown

図 7-20. Offset Voltage (RTI) vs Input Common-Mode Voltage

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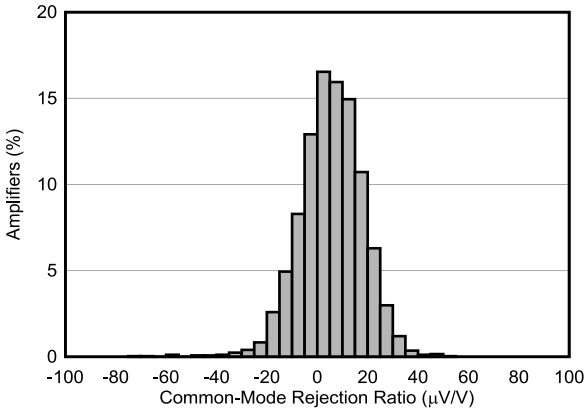
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} = 0 V, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)



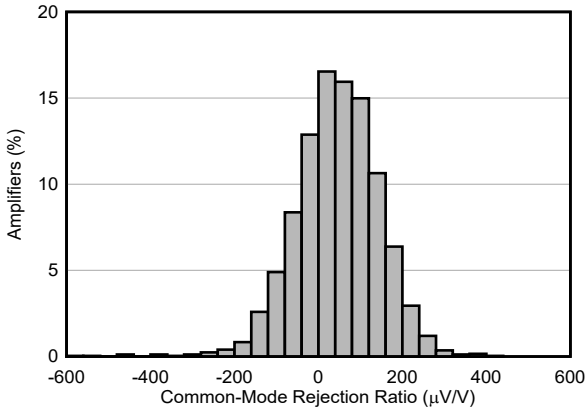
N = 2500 Mean = 0.31 µV/V Std. dev. = 0.78 µV/V
G = 16 V/V

図 7-21. CMRR Distribution



N = 2500 Mean = 5.61 µV/V Std. dev. = 12.50 µV/V
G = 1 V/V

図 7-22. CMRR Distribution



N = 2500 Mean = 44.98 µV/V Std. dev. = 100 µV/V
G = 0.125 V/V

図 7-23. CMRR Distribution

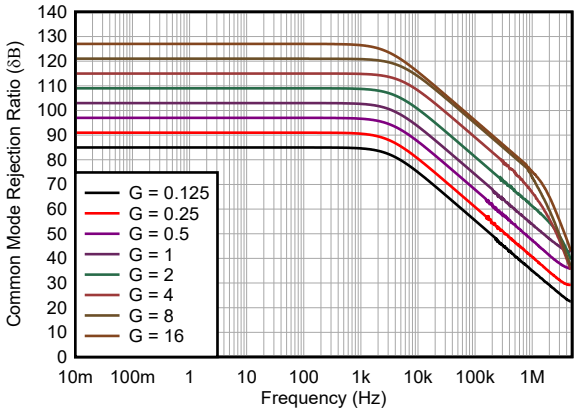


図 7-24. CMRR vs Frequency (RTI)

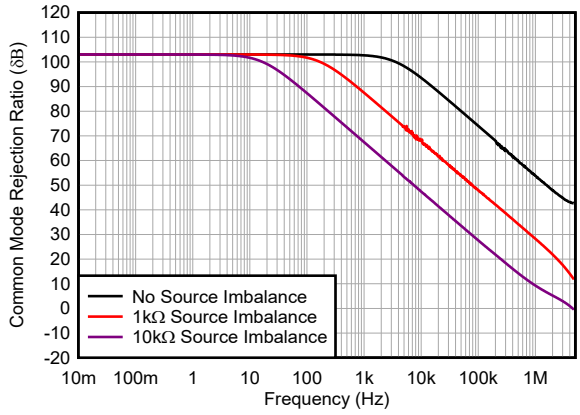
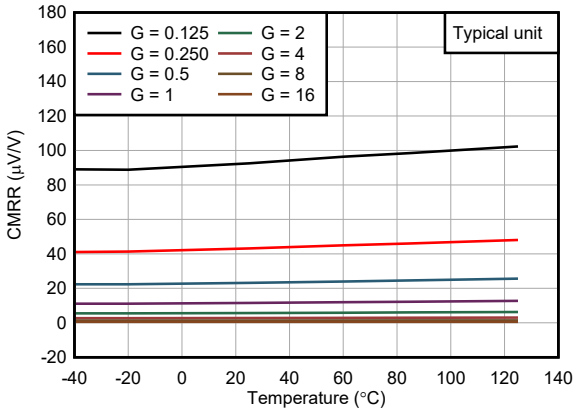


図 7-25. CMRR vs Frequency (Unbalanced)



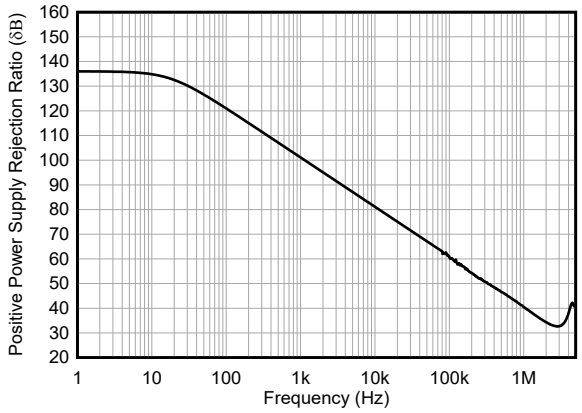
Typical unit shown

図 7-26. Typical CMRR vs Temperature

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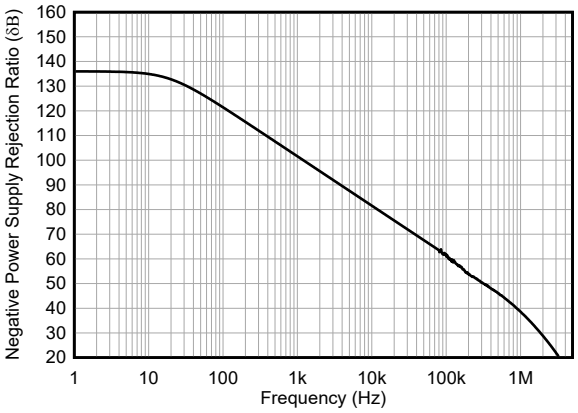
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} = 0 V, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)



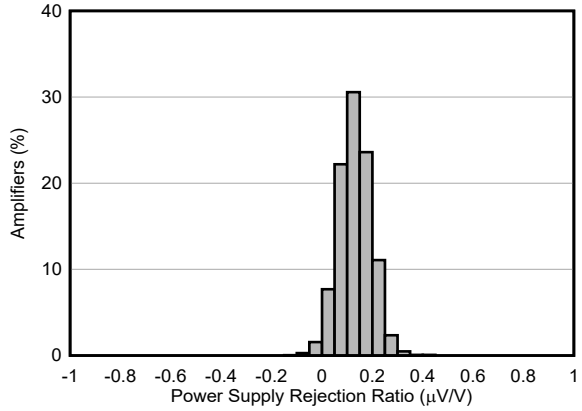
Typical unit shown

図 7-27. Positive PSRR vs Frequency



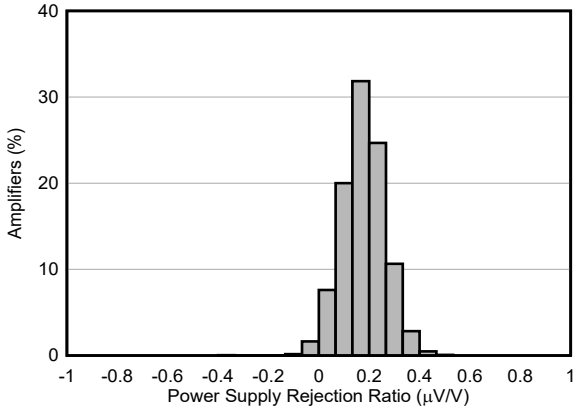
Typical unit shown

図 7-28. Negative PSRR vs Frequency



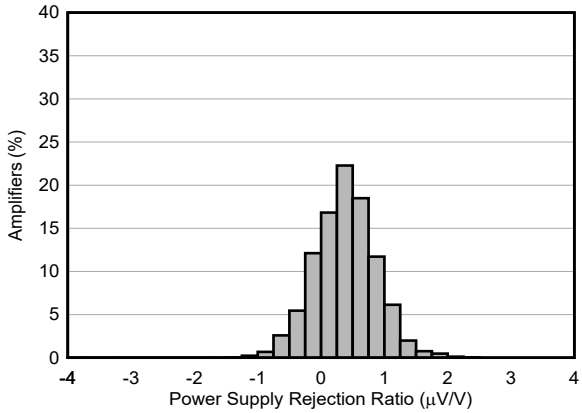
N = 2500 Mean = 0.13 µV/V Std. dev. = 0.06 µV/V
G = 16 V/V

図 7-29. PSRR Distribution



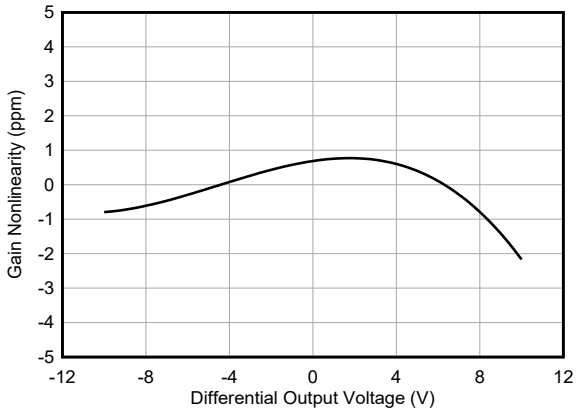
N = 2500 Mean = 0.17 µV/V Std. dev. = 0.08 µV/V
G = 1 V/V

図 7-30. PSRR Distribution



N = 2500 Mean = 0.38 µV/V Std. dev. = 0.48 µV/V
G = 0.125 V/V

図 7-31. PSRR Distribution



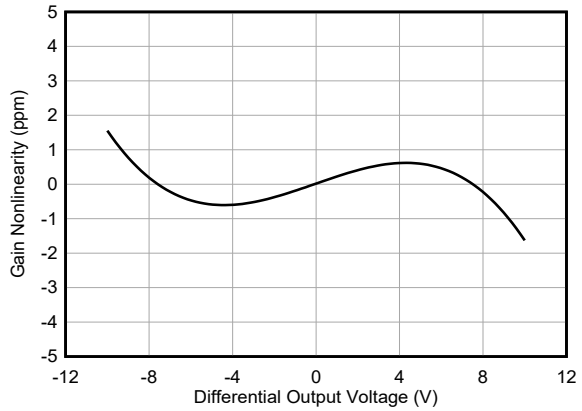
G = 16 V/V $V_{OUTDIFF}$ = 10 V

図 7-32. Gain Nonlinearity

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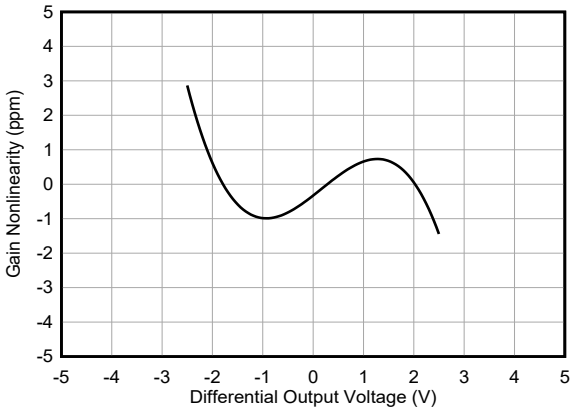
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} = 0 V, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)



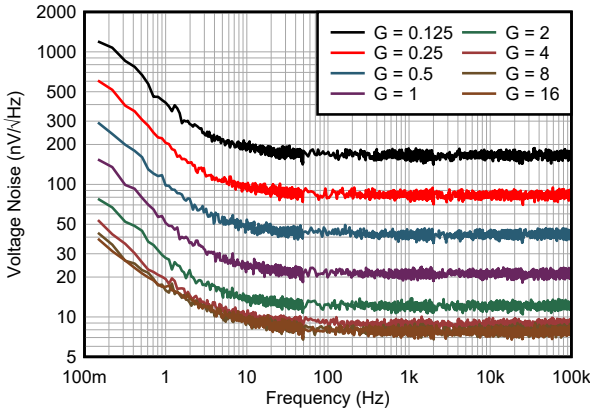
G = 1 V/V $V_{OUTDIFF}$ = 10 V

図 7-33. Gain Nonlinearity



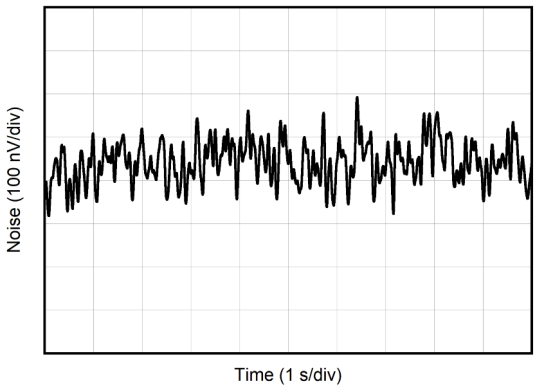
G = 0.125 V/V $V_{OUTDIFF}$ = 2.5 V

図 7-34. Gain Nonlinearity



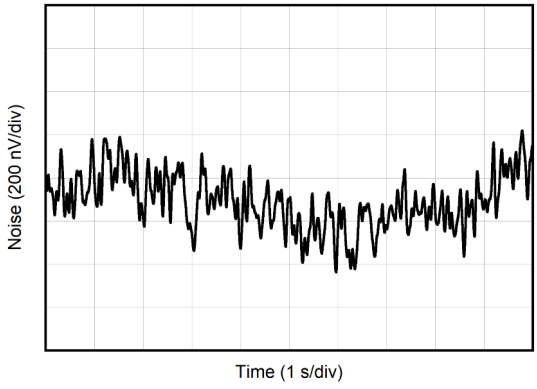
Typical unit shown

図 7-35. Voltage Noise Spectral Density (RTI) vs Frequency



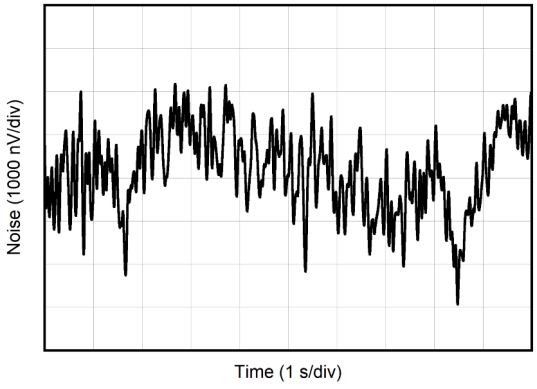
G = 16 V/V

図 7-36. 0.1-Hz to 10-Hz Voltage Noise (RTI)



G = 1 V/V

図 7-37. 0.1-Hz to 10-Hz Voltage Noise (RTI)



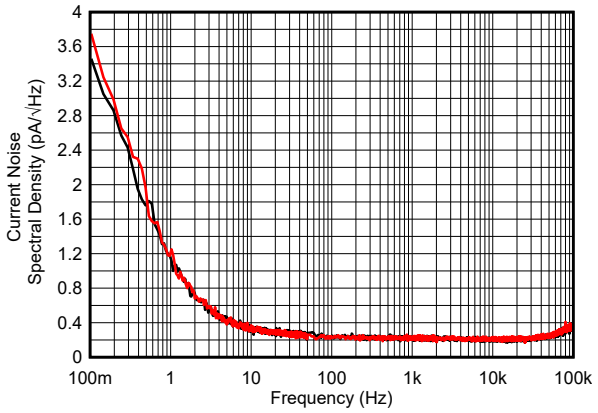
G = 0.125 V/V

図 7-38. 0.1-Hz to 10-Hz Voltage Noise (RTI)

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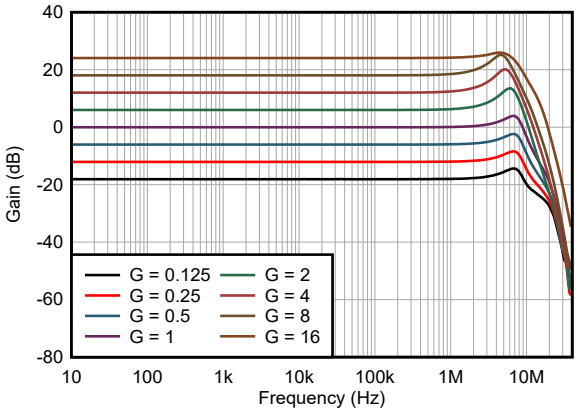
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} = 0 V, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)



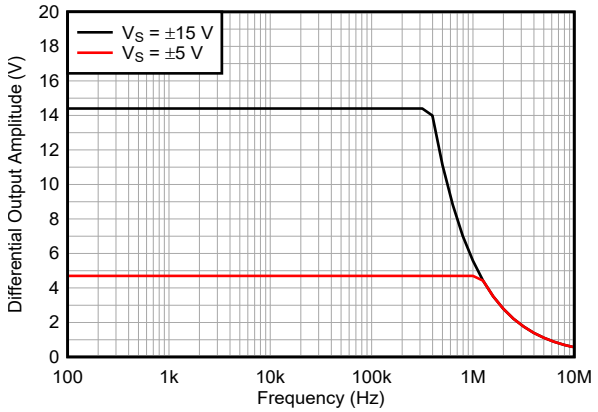
G = 16 V/V

図 7-39. Current Noise Spectral Density vs Frequency



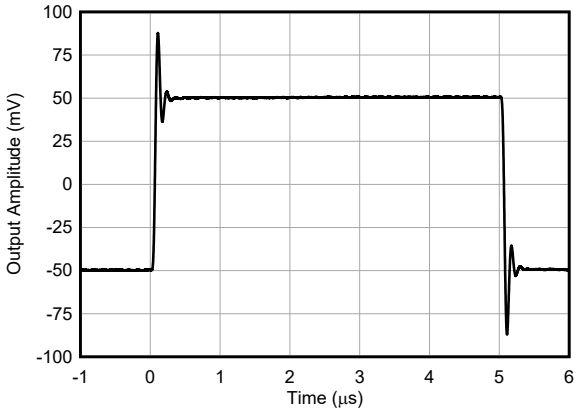
Differential load capacitance = 50 pF

図 7-40. Gain vs Frequency



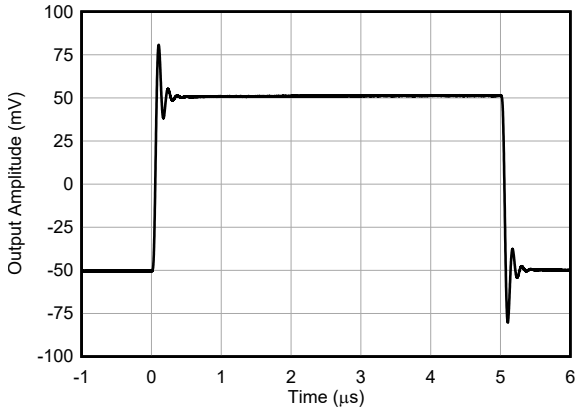
Differential load capacitance = 50 pF

図 7-41. Large-Signal Step Response vs Frequency



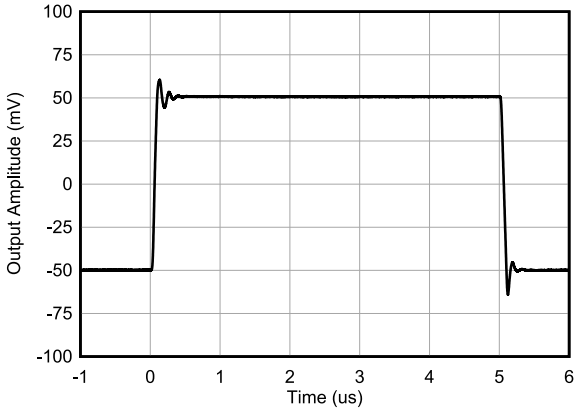
G = 16 V/V Differential load capacitance = 50 pF

図 7-42. Small-Signal Step Response



G = 1 V/V Differential load capacitance = 50 pF

図 7-43. Small-Signal Step Response



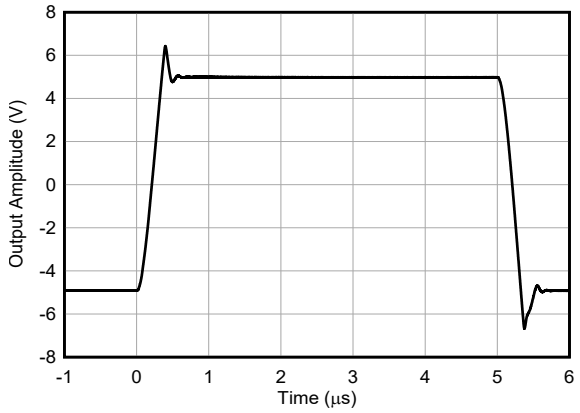
G = 0.125 V/V Differential load capacitance = 50 pF

図 7-44. Small-Signal Step Response

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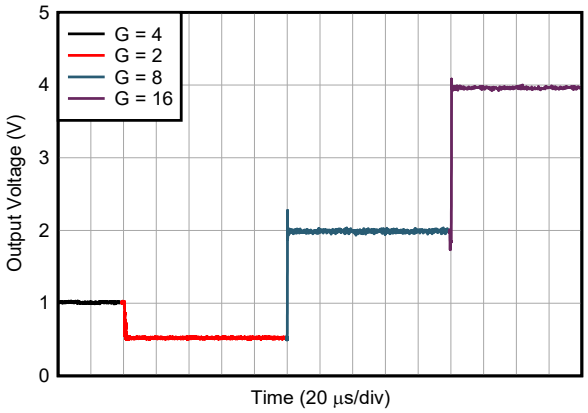
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} = 0 V, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)



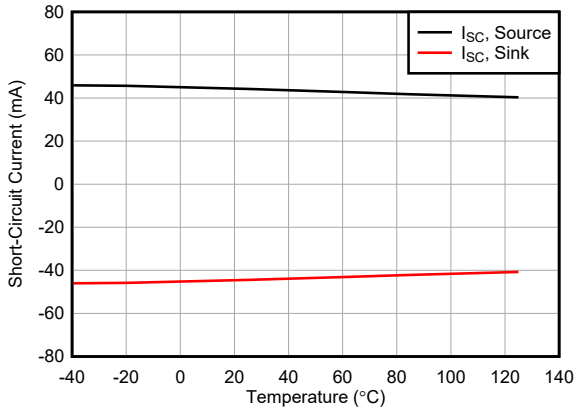
G = 1 V/V

図 7-45. Large-Signal Step Response



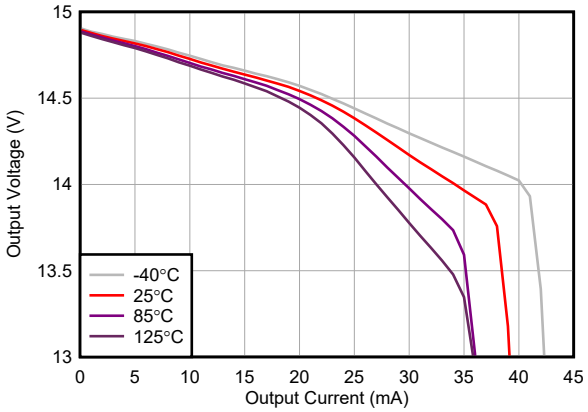
Input voltage = 250 mV_{PP}

図 7-46. Gain Switching Transient Response



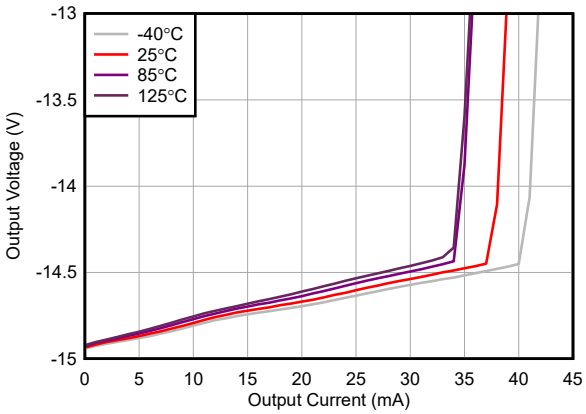
Short to V_{SOUT}/2

図 7-47. Output Short-Circuit Current vs Temperature



V_S = ±18 V V_{SOUT} = ±15 V G = 16 V/V

図 7-48. Positive Output Voltage vs Output Current



V_S = ±18 V V_{SOUT} = ±15 V G = 16 V/V

図 7-49. Negative Output Voltage vs Output Current

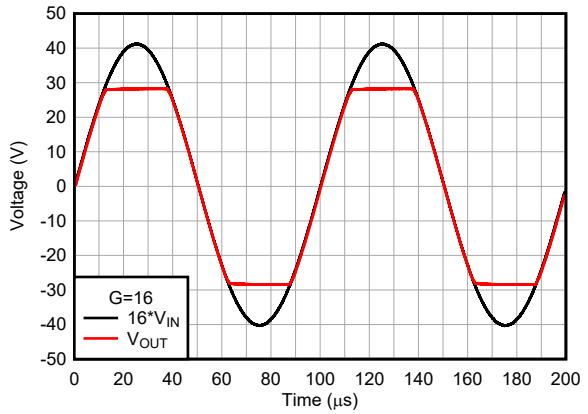


図 7-50. Overload Recovery

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7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} = 0 V, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)

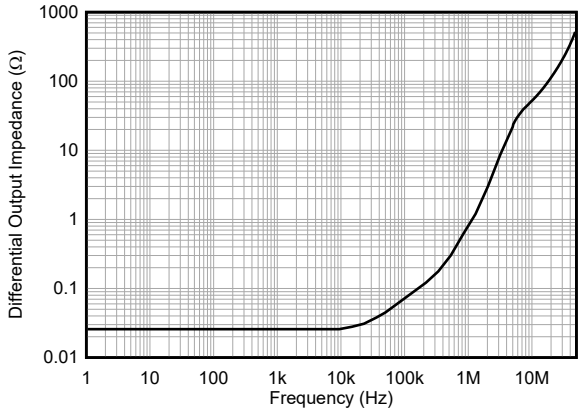


図 7-51. Closed Loop Output Impedance vs Frequency

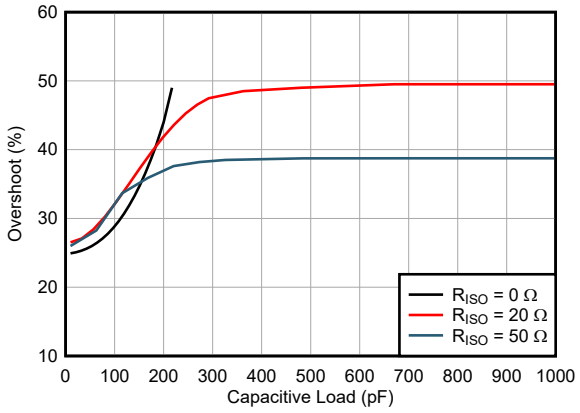


図 7-52. Overshoot vs Capacitive Load

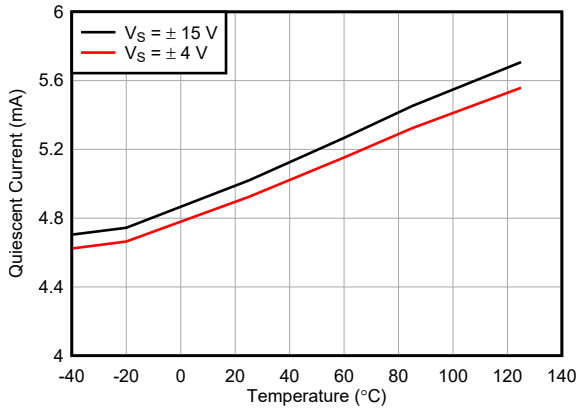
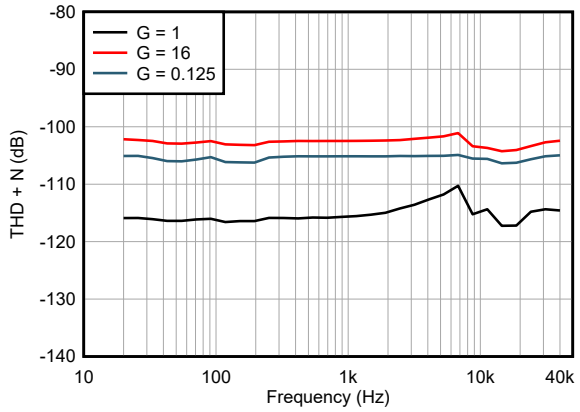
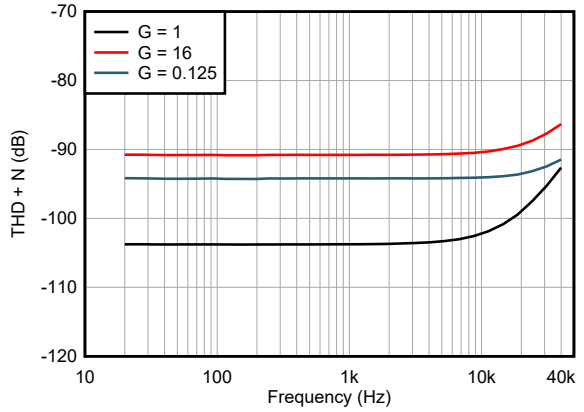


図 7-53. Quiescent Current vs Temperature



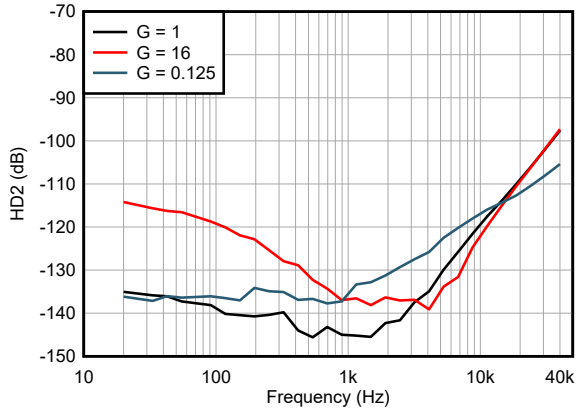
10-Hz to 22-kHz band-pass filter $V_{OUTDIFF}$ > 2.5 V_{PP}

図 7-54. Total Harmonic Distortion + Noise vs Frequency



10-Hz to 500-kHz band-pass filter $V_{OUTDIFF}$ > 2.5 V_{PP}

図 7-55. Total Harmonic Distortion + Noise vs Frequency



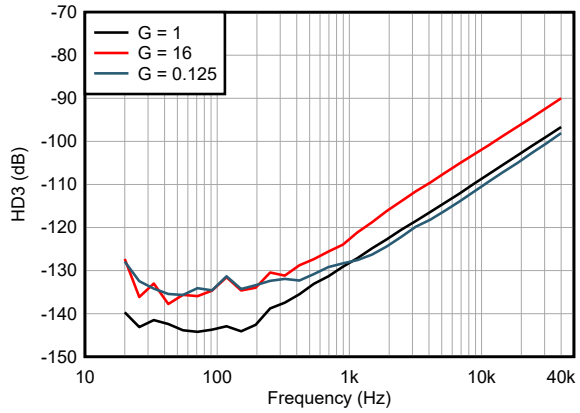
$V_{OUTDIFF}$ > 2.5 V_{PP}

図 7-56. 2nd Harmonic Distortion vs Frequency

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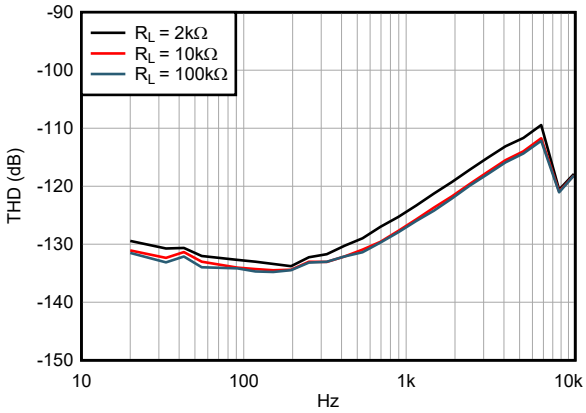
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15 V, V_{ICM} = V_{OCM} = 0 V, R_L = 10 kΩ, and G = 1 V/V (unless otherwise noted)



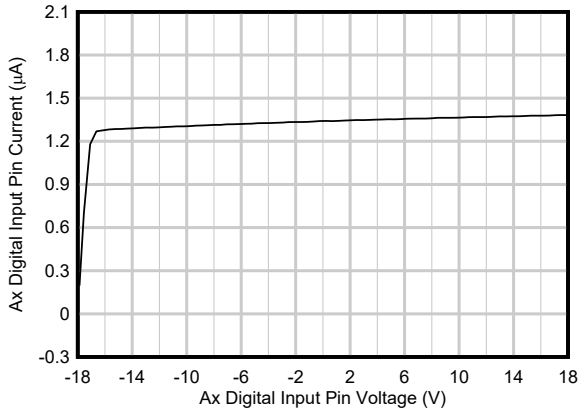
$V_{OUTDIFF}$ > 2.5 V_{PP}

図 7-57. 3rd Harmonic Distortion vs Frequency



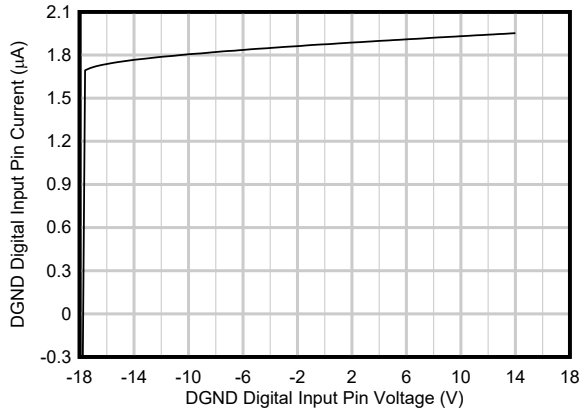
G = 1 V/V $V_{OUTDIFF}$ = 10 V_{PP}

図 7-58. Total Harmonic Distortion vs Frequency



DGND = –18 V

図 7-59. Ax Digital Input Pin Current vs Ax Digital Input Pin Voltage



Ax = DGND

図 7-60. DGND Digital Input Pin Current vs DGND Digital Input Pin Voltage

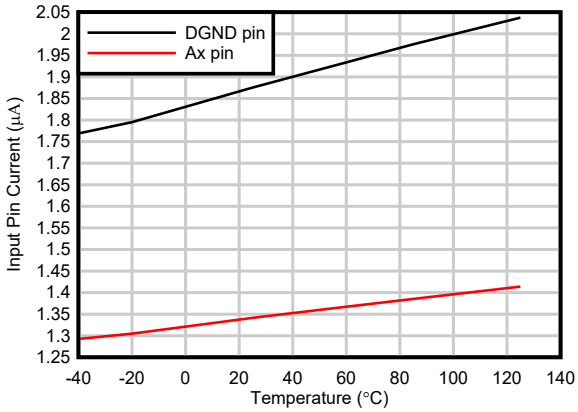


図 7-61. Digital Input Pin Current vs Temperature

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8 Detailed Description

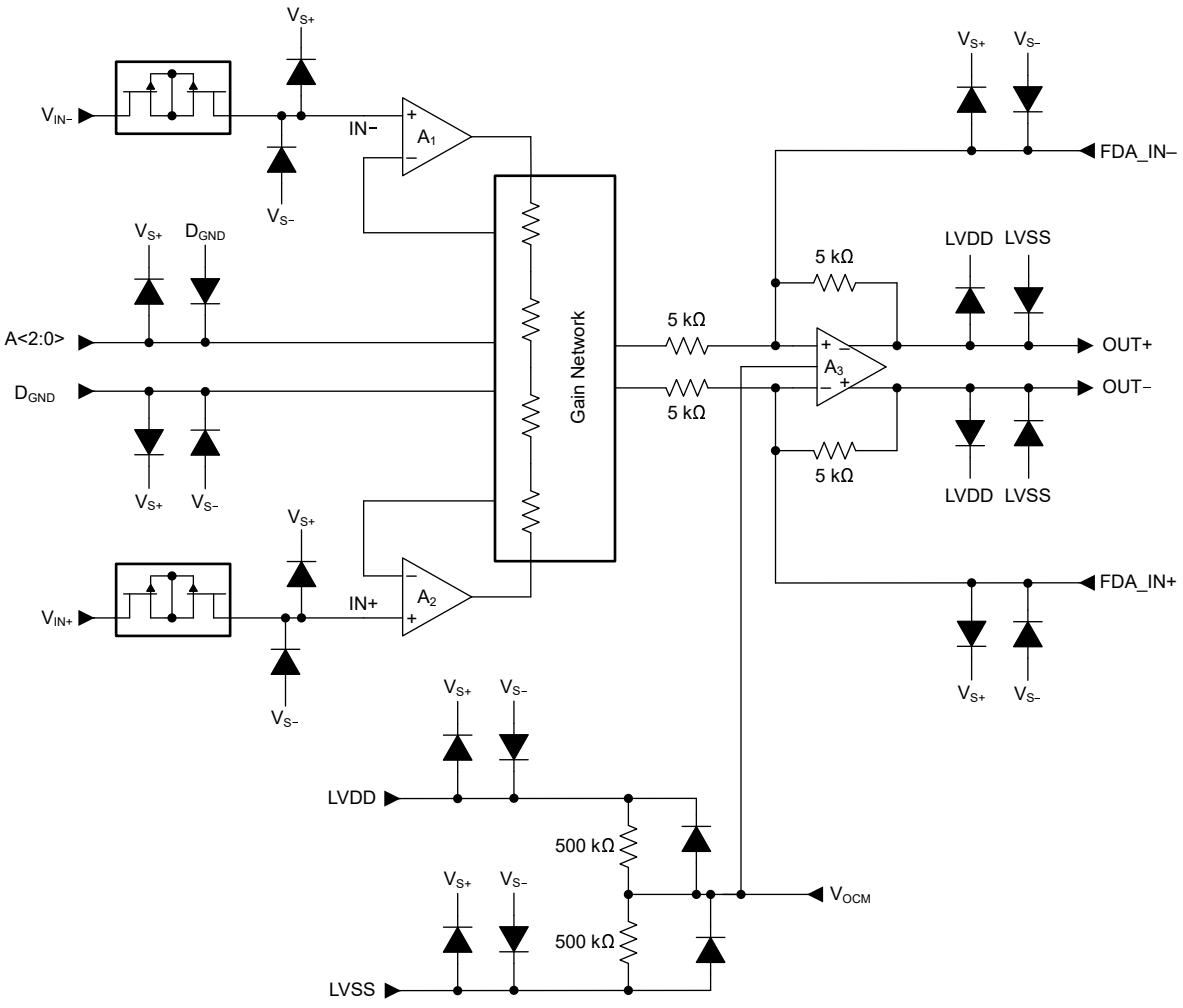
8.1 Overview

The PGA855 is a monolithic, high-voltage, precision programmable-gain instrumentation amplifier. The PGA855 combines a high-speed current-feedback input stage with an internally matched gain resistor network, followed by a four-resistor, fully differential amplifier output stage. Eight preprogrammed binary gains, ranging from 0.125 V/V to 16 V/V are selectable using gain-select pins A0, A1, and A2.

A functional block diagram for PGA855 is shown in the next section. The differential input voltage is fed into a pair of matched, high-impedance input-current-feedback amplifiers. An integrated precision-matched gain resistor network is used to amplify the differential input voltage. A fully differential output difference amplifier, A_3, rejects the input common-mode component and refers the output signal to the voltage level set by the VOCM pin.

The PGA855 output amplifier bandwidth is optimized to drive high-performance analog-to-digital converters (ADCs) with sampling rates up to 1 MSPS without the need for an additional ADC driver. The output amplifier uses a separate power supply that is independent of the input-stage power supply. When driving an ADC, use a low-impedance connection from LVDD and LVSS to the ADC power supplies. This configuration protects the ADC inputs from damage due to inadvertent overvoltage conditions.

8.2 機能ブロック図



8.3 Feature Description

8.3.1 Gain Control

The PGA855 uses three pins to set the amplifier gain. These gain select pins are set with respect to DGND. This configuration simplifies design when compared to programmable-gain amplifiers requiring an SPI or other digital interface options for gain changes. 図 8-1 shows the gain-setting block diagram. 表 8-1 lists the gain options. Any gain select pin that is not driven by an external source is automatically biased at DGND using internal pulldown options.

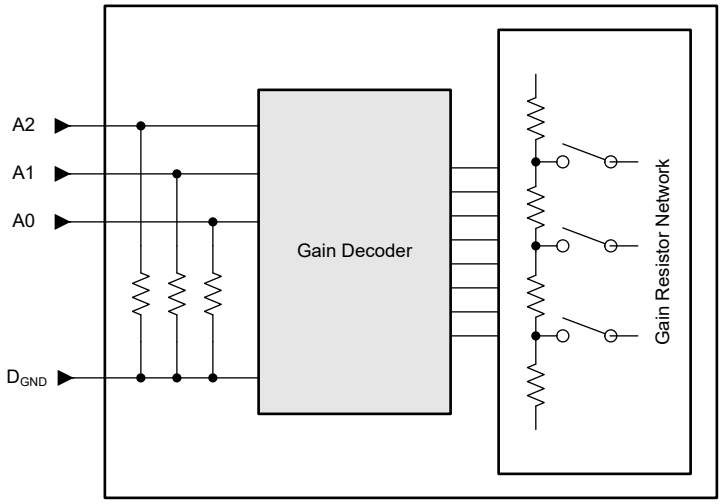


図 8-1. PGA855 Gain Setting Block Diagram

表 8-1. Gain Options

A2:A0	GAIN
000	0.125
001	0.25
010	0.5
011	1
100	2
101	4
110	8
111	16

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8.3.2 Input Protection

The inputs of PGA855 are individually protected for voltages up to ±40 V beyond either supply. For example, an input common-mode voltage anywhere between –55 V and +55 V does not cause damage when powered from ±15-V supplies. Internal circuitry on each input provides low series impedance under normal signal conditions, thus maintaining high performance under normal operating conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately 4.8 mA. 図 8-2 shows the input protection functionality during an overvoltage condition.

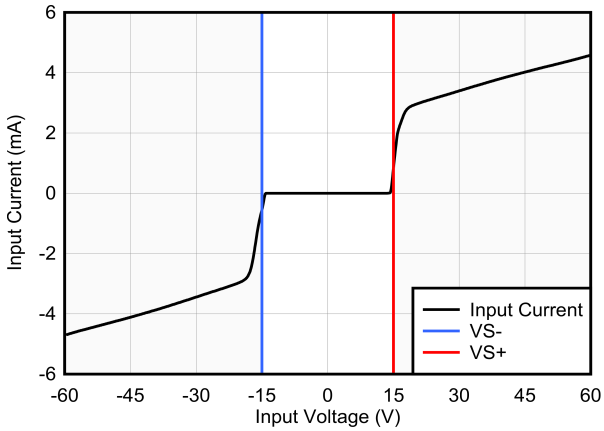


図 8-2. Input Current vs Input Overvoltage

図 8-3 shows that during an input overvoltage condition, current flows through the input protection diodes into the power supplies. In applications where the power supplies are unable to sink current, place Zener diode clamps (ZD1 and ZD2) on the power supplies to provide a current pathway to ground.

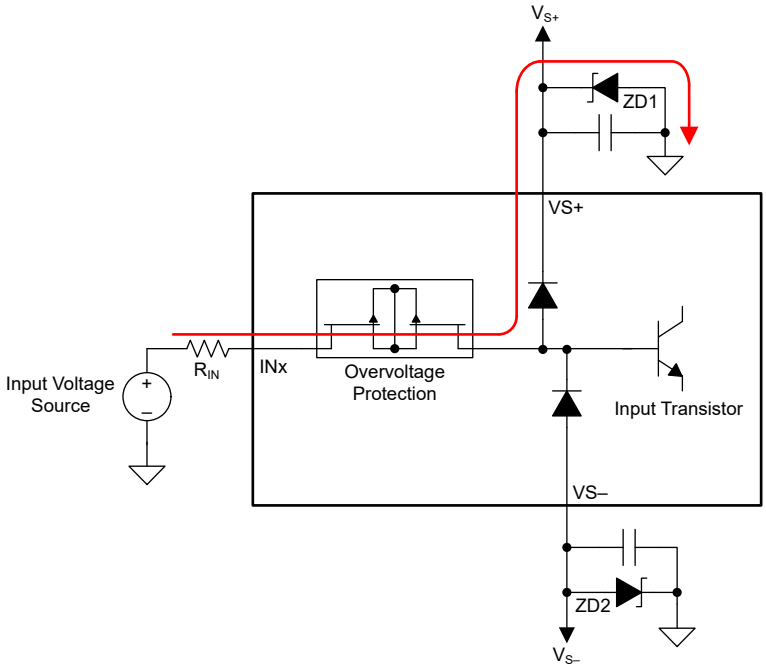


図 8-3. Input Current Path During an Overvoltage Condition

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8.3.3 Output Common-Mode Pin

The output voltages of the PGA855 are balanced with respect to the voltage on the output common-mode pin, VOCM. The starting point for most designs is to assign an output common-mode voltage for the PGA855. For ac-coupled signal paths, this voltage is often the default mid-supply voltage, so as to retain the most available output swing around the voltage centered at VOCM. For dc-coupled signal paths, set this voltage between a maximum of V_{LVDD} – 1.5 V and minimum of V_{LVSS} + 1.5 V. For precision ADC applications, this voltage is typically the input common-mode voltage of the ADC.

The voltage at the VOCM pin is internally buffered to bias the fully differential output amplifier, eliminating the need for an external VOCM buffer. In the event that the VOCM pin is left floating, the output common-mode voltage is biased at output mid-supply using an internal 500-kΩ / 500-kΩ resistor divider network connected between the output-stage power-supply pins.

8.3.4 Using the Fully Differential Output Amplifier to Shape Noise

セクション 8.2 shows that the PGA855 output-stage fully-differential amplifier uses 5-kΩ feedback resistors between the OUT+ and OUT– outputs and the inverting and noninverting inputs, respectively. External direct access to the inverting and noninverting inputs of the fully differential amplifier is provided through the FDA_IN– and FDA_IN+ pins, respectively. This option allows circuit designers to add external feedback capacitors in parallel with the internal feedback resistors to implement noise-filtering or noise-shaping techniques. These pins can also be used to implement customized attenuating gains for the output stage. Consider the following important factors when designing parallel circuits with the internal feedback resistors:

- The accuracy of the internal resistor network is 0.01 % or better. This accuracy results in a common-mode rejection (CMRR) of 80 dB or better. Mismatched leakage currents on these pins can cause CMRR degradation.
- The internal resistors have ±15% absolute resistance variation and must be considered when implementing custom attenuating gains or noise filters.

> **注意**
> Do not treat these pins as outputs, nor use the pins to source or sink current. Excessive currents through the feedback resistors can cause permanent damage to internal circuitry.

8.4 Device Functional Modes

The PGA855 has a single functional mode and operates when the input-stage power supply is greater than ±4 V (8 V) and the output-stage power supply is greater than ±2.25 V (4.5 V); see also セクション 7.3.

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

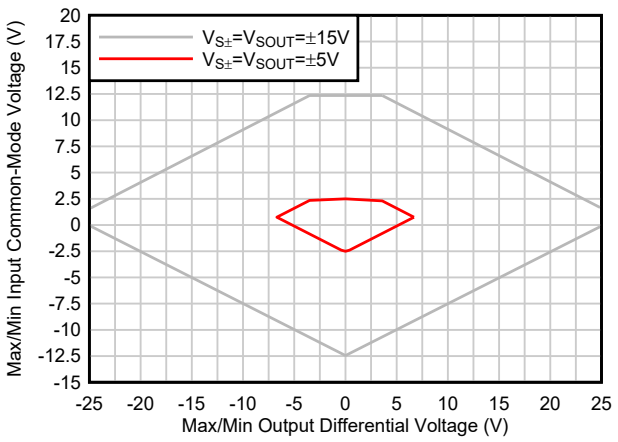
The PGA855 is a monolithic, high-voltage, high bandwidth, precision programmable gain instrumentation amplifier with fully differential outputs. The PGA855 combines a high-speed current-feedback input stage with an internally matched gain resistor network, followed by a four-resistor, fully differential amplifier output stage. The PGA855 is equipped with 8 binary-gain settings, from 0.125 V/V to 16 V/V, using three digital gain-selection pins: A0, A1, and A2.

The PGA855 is designed to work with applications such as factory automation and control, analog input modules, data acquisition, test and measurement, and semiconductor test.

9.1.1 Linear Operating Input Range

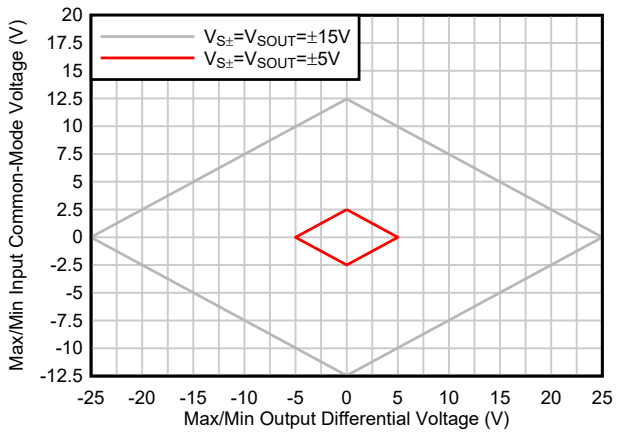
The linear operating input voltage range of the PGA855 input circuitry extends within 2.5 V (maximum) of both power supplies, and maintains excellent common-mode rejection throughout this range. The linear operating input common-mode range is a function of the input common-mode voltage, input differential voltage, gain, and output common-mode voltage.

The valid common-mode range to enable valid output voltage at no load condition are shown in 図 9-1 to 図 9-3.



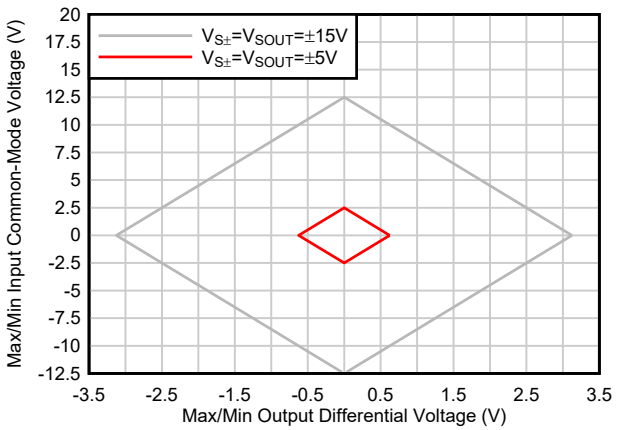
VS = VSOUT = ±5 V, ±15 V　VOCM = 0 V　G = 16 V/V

図 9-1. Input Common-Mode Voltage vs Output Voltage at G = 16 V/V



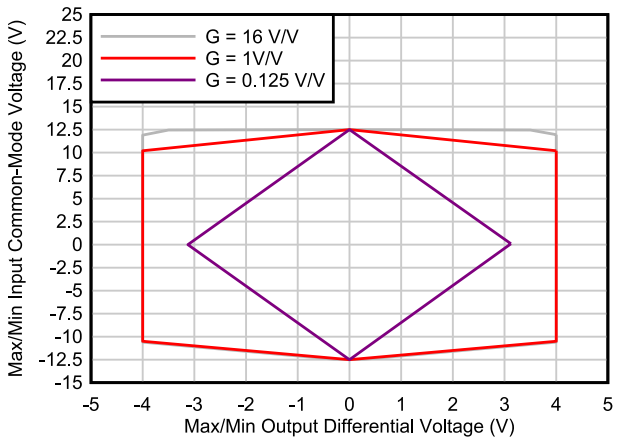
VS = VSOUT = ±5 V, ±15 V　VOCM = 0 V　G = 1 V/V

図 9-2. Input Common-Mode Voltage vs Output Voltage at G = 1 V/V



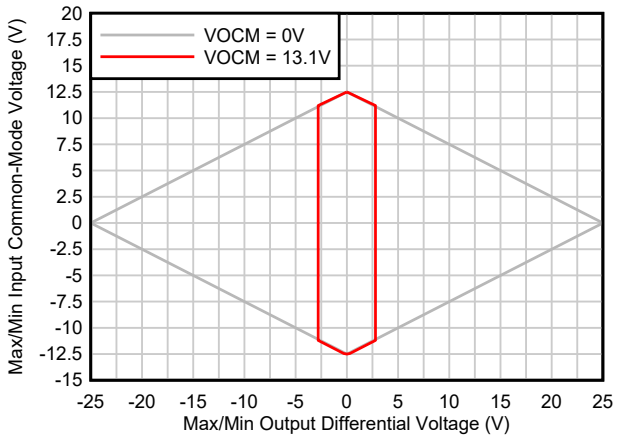
V_S = V_{SOUT} = ±5 V, ±15 V　　VOCM = 0 V　　G = 0.125 V/V

図 9-3. Input Common-Mode Voltage vs Output Voltage at G = 0.125 V/V



V_S = ±15 V　　V_{SOUT} = 5 V

図 9-4. Input Common-Mode Voltage vs Output Voltage at VOCM = 2.5 V



V_S = V_{SOUT} = ±15 V　　G = 1 V/V

図 9-5. Input Common-Mode Voltage vs Output Voltage at VOCM max

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9.2 Typical Applications

9.2.1 ADS127L11 and ADS127L21, 24-Bit, Delta-Sigma ADC Driver Circuit

The application circuit in 図 9-6 shows a schematic for a 24-bit wide-bandwidth, delta-sigma ADC. The ADS127Lx1 ADC offers two digital filters to optimize ac applications (wideband filter) or dc applications (sinc4 filter). 表 9-2 and 表 9-3 show measurement results in both filter settings. For a detailed design procedure to operate the ADS127Lx1 ADC, see the ADS127Lx1EVM-PDK evaluation module user's guide.

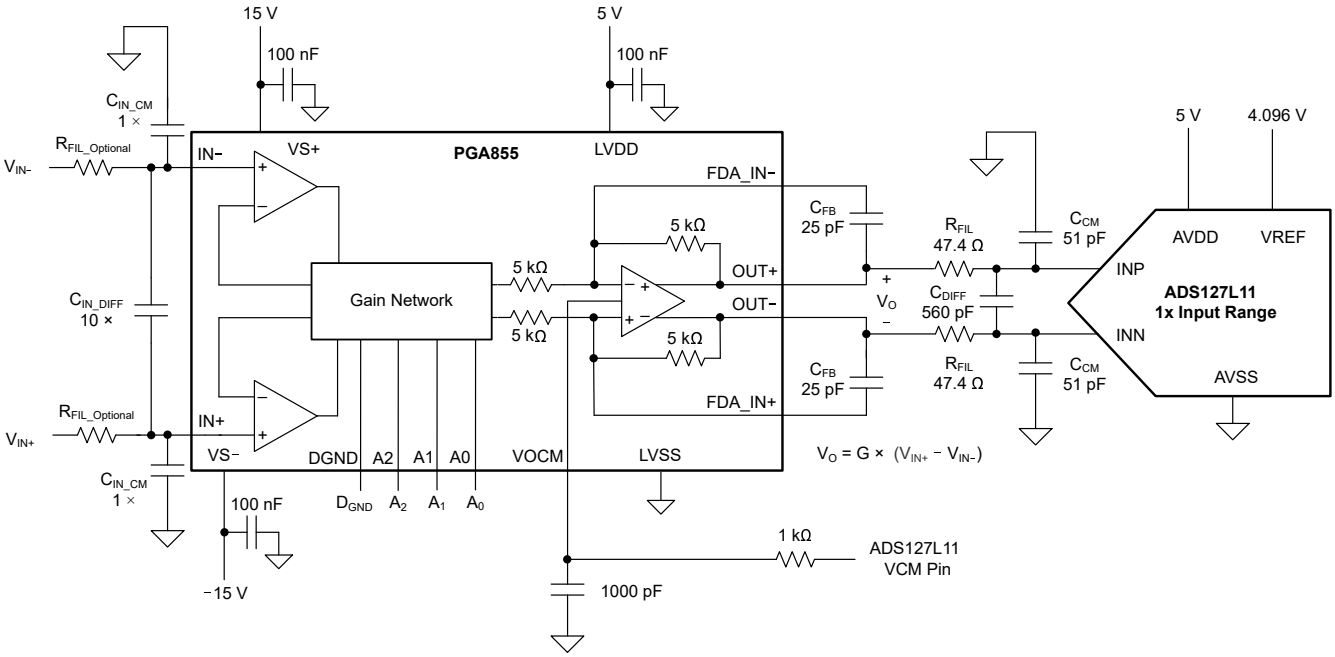


図 9-6. Driving the ADS127Lx1 Delta-Sigma ADC

9.2.1.1 Design Requirements

The design requirements for the application driving the ADS127Lx1 ADC are listed in the following table.

表 9-1. Design Parameters

PARAMETER	VALUE
Differential-to-differential conversion	V_{INDIFF} to $V_{OUTDIFF}$
Supply voltages	$V_{S\pm}$ = ±15 V, V_{LVDD} = 5 V, V_{LVSS} = GND, VREF = 4.096 V
Full-scale range of ADC	FSR = ± 4.096 V
Data rate of ADC	f_{DATA} = 187.5 kSPS
ADC filter configuration	(1) High-speed mode, Sinc4 filter, OSR = 64
	(2) High-speed mode, Wideband filter, OSR = 64
PGA gain	See 表 9-2 and 表 9-3
Signal frequency	Tested at f_{IN} = 1 kHz
RC kickback filter(1)	R_{FIL} = 47.4 Ω, C_{DIFF} = 560 pF, C_{CM} = 51 pF

(1) Consider a trade-off between THD, frequency response, and drift. The differential current drift into the ADC can interact with the filter resistors and result in higher drift errors. However, lower resistance degrades the phase margin of the PGA855. For low drift applications, keep R_{FIL} < 50 Ω.

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9.2.1.2 Detailed Design Procedure

表 9-2 and 表 9-3 show the typical signal-to-noise (SNR) and total harmonic distortion (THD) of the PGA855 driving the ADS127Lx1 delta-sigma ADC using a sinc4 or wideband filter. 図 9-7 and 図 9-8 show the respective FFT plots. For the SNR and THD measurements, a 1-kHz differential signal is applied. The signal amplitude is adjusted to produce a PGA855 output at –0.2 dBFS of the ADC full-scale range. For a list of the equivalent input voltage amplitude signals for the different PGA855 gain configurations, see 表 9-2 and 表 9-3. At gain = 1 V/V, the design achieves –121.4-dB THD and 109.1-dB SNR.

表 9-2. PGA855 and ADS127Lx1 FFT Data Summary, OSR = 64, Sinc4 Filter

PGA GAIN (V/V)	INPUT AMPLITUDE (V_{PP})	SNR (dB)	THD (dB)	ENOB (Bits)
0.125	40.0	106.0	–119.6	17.5
0.25	32.022	109.0	–119.3	17.8
0.5	16.012	109.8	–121.2	17.9
1	8.006	109.6	–121.4	17.9
2	4.002	109.6	–121.4	17.9
4	2.002	107.4	–121.4	17.5
8	1.0	104.0	–121.4	17.0
16	0.5	99.1	–117.0	16.2

表 9-3. PGA855 and ADS127Lx1 FFT Data Summary, OSR = 64, Wideband Filter

PGA GAIN (V/V)	INPUT AMPLITUDE (V_{PP})	SNR (dB)	THD (dB)	ENOB (Bits)
0.125	40.0	106.0	–119.6	17.3
0.25	32.022	107.5	–119.0	17.5
0.5	16.012	107.7	–121.2	17.6
1	8.006	107.6	–121.4	17.6
2	4.002	107.0	–121.4	17.5
4	2.002	105.4	–121.4	17.2
8	1.0	101.7	–121.4	16.6
16	0.5	96.7	–117.0	15.8

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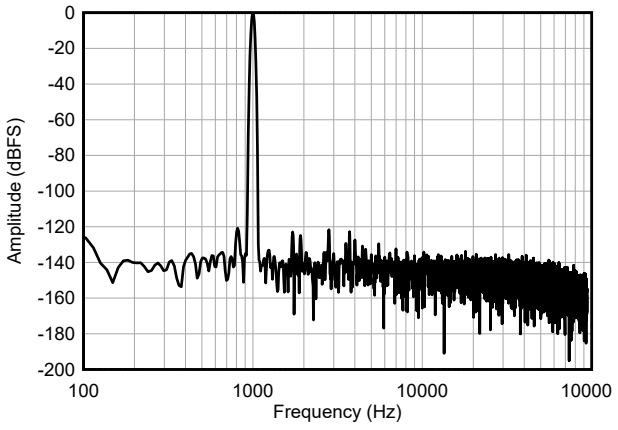
The R-C-R differential low-pass filter at the input of the instrumentation amplifier helps reduce EMI/RFI high-frequency extrinsic noise. This filter can be customized per the bandwidth and application requirements. This design example (see 図 9-6) suggests a filter with the capacitor ratio of C_{IN_DIFF} = 10 × C_{IN_CM}. Using the 10-to-1 ratio for differential capacitor C_{IN_DIFF} versus common-mode capacitors C_{IN_CM} offers good differential and common-mode noise rejection, and this arrangement tends to be less sensitive to the tolerance variation and mismatch of the filter capacitors.

The feedback capacitor, C_{FB}, is in parallel with the PGA855 output-stage 5-kΩ feedback resistors to implement additional noise filtering. The internal resistors have ±15 % absolute resistance variation, and this variation must be taken in to account when implementing noise filtering. In this example, C_{FB} is set to 25 pF, providing a typical $f_{–3dB}$ corner frequency of 1 MHz. The estimated minimum $f_{–3dB}$ corner frequency for this circuit is approximately 938 kHz when accounting for the feedback-resistor variation.

The filter at the ADS127Lx1 inputs works as a charge reservoir to filter the sampled input of the ADC. The charge reservoir reduces the instantaneous charge demand of the amplifier, maintaining low distortion and low gain error that otherwise can degrade because of incomplete amplifier settling. The ADC input filter values are R_{FIL} = 47.4 Ω, C_{DIFF} = 560 pF, and C_{CM} = 51 pF. The ADC input precharge buffers significantly reduce the sample-phase input charge that raises the ADC input impedance to decrease gain error.

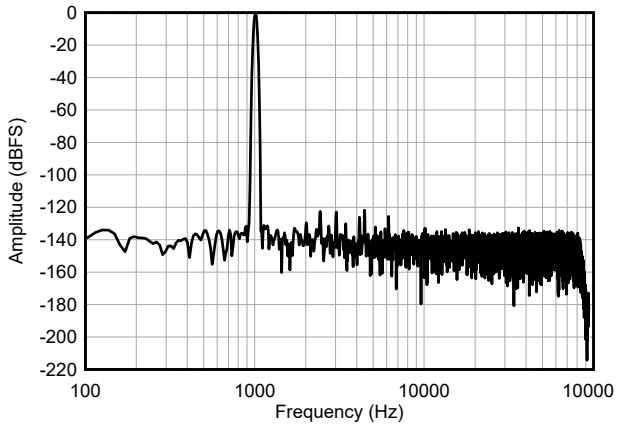
High-grade COG (NPO) are used everywhere in the signal path (C_{IN_DIFF}, C_{IN_CM}, C_{FB}, C_{DIFF}, C_{CM}) for low distortion. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance accuracy. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

9.2.1.3 Application Curves



G = 1 V/V, f_{IN} = 1 kHz, SNR = 109.6 dB, THD = –121.4 dB

図 9-7. Performance FFT Plots With ADS127L11, OSR = 64, Sinc4 Filter



G = 1 V/V, f_{IN} = 1 kHz, SNR = 107.6 dB, THD = –121.4 dB

図 9-8. Performance FFT Plots With ADS127L11, OSR = 64, Wideband Filter

9.2.2 ADS8900B 20-Bit SAR ADC Driver Circuit

The application circuit in 図 9-9 shows the schematic for the 20-bit, precision, 1-MSPS, successive approximation register (SAR), analog-to-digital converter (ADC). This circuit is used to measure the driving capability of the PGA855 with the ADS8900B ADC. The circuit accepts single-ended or differential input signals.

The PGA855 operates with independent input and output power supplies. In this example, ±15-V power supplies are used for the input section, and a 5.3-V power supply for the output section.

To reduce extrinsic voltage supply noise, the ADC portion of the circuit uses the TPS7A4700, a low-noise, 4-μVRMS LDO voltage regulator, to generate a unipolar 5.3-V ADC supply rail and the PGA855 output stage supply is powered by the same 5.3-V ADC supply. The 5.3-V output supply operation prevents overloading the ADC inputs during PGA overdrive conditions. The REF5050 is selected as a voltage reference; this is a low-noise, low-drift, precision 5-V reference connected to the ADS8900B REFIN pin.

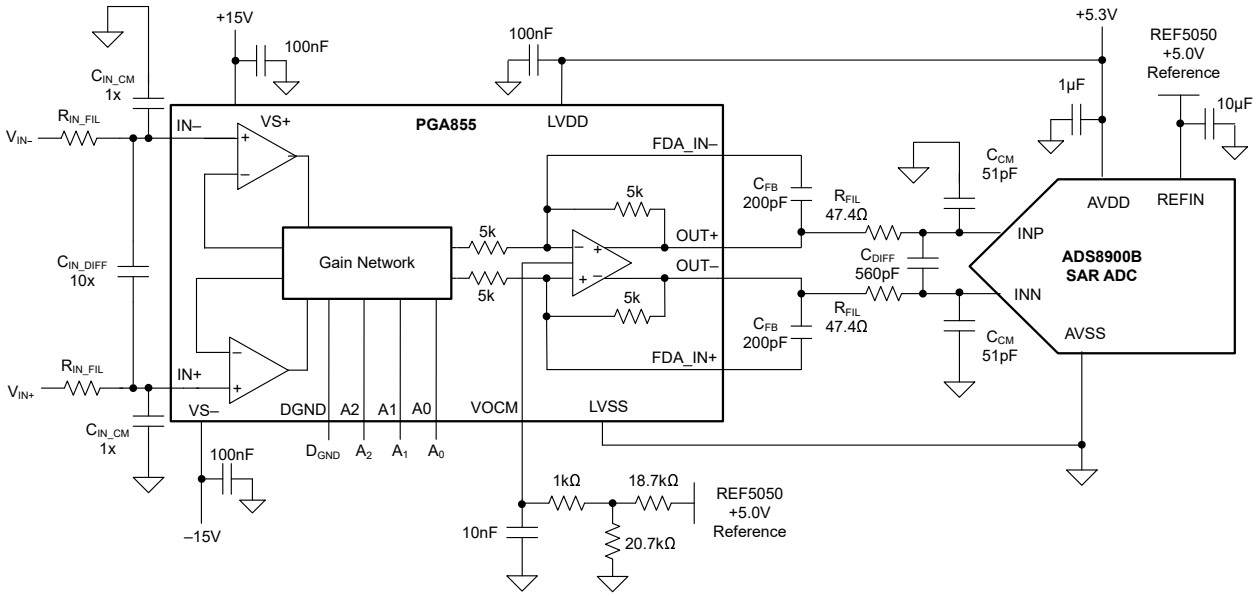


図 9-9. Driving the SAR ADC ADS8900B

9.2.2.1 Design Requirements

The design requirements for the application driving the ADS8900B ADC are listed in the following table.

表 9-4. Design Parameters

PARAMETER	VALUE
Supply voltages	VS± = ±15 V, V_{LVDD} = 5.3 V, V_{LVSS} = GND, VREF = 5 V
Full-scale range of ADC	FSR = ±5 V
Sampling rate of ADC	f_{SAMPLE} = 1 MSPS
PGA gain	See Table 表 9-5
Input signal amplitude	See Table 表 9-5
Signal frequency	Tested at f_{IN} = 1 kHz
RC kickback filter	R_{FIL} = 47.4 Ω, C_{DIFF} = 560 pF, C_{CM} = 51 pF

9.2.2.2 Detailed Design Procedure

The ADS8900B requires an input common-mode voltage within the range of VREF / 2 ±100 mV. The PGA855 VOCM pin is set to a nominal voltage of approximately 2.58 V. The VOCM voltage is purposely set to a voltage slightly greater than VREF / 2 to maximize the output voltage swing range of the PGA855, while allowing margin for the VOCM offset voltage error and drift variation. The VOCM voltage is generated by feeding the REF5050

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reference through an 18.7 kΩ- to 0 kΩ voltage divider implemented with 0.1% tolerance resistors. An additional RC filter with R = 1 kΩ, C = 10 nF is used in close proximity to the VOCM pin as shown on 図 9-9.

The R-C-R differential low-pass filter at the input of the PGA helps reduce EMI/RFI high frequency extrinsic noise. This filter can be customized per the bandwidth and application requirements.

Two first-order filters are implemented with the PGA855 circuit. The first filter is provided by C_{FB} in parallel with the PGA 5-kΩ feedback resistors. The PGA resistors are ±15% absolute tolerance, such as, consider the effect of the tolerance on the filter cutoff frequency, the filter frequency changes to 126 kHz. At this tolerance, the filter maintains –0.1 dB flatness to 24 kHz.

There is flexibility of modifying the C_{FB} capacitor value to adjust bandwidth, with the trade-off on the broadband noise of the circuit.

The second filter placed directly at the ADS8900B inputs works as a charge reservoir to filter the sampled input of the ADC. The charge reservoir reduces the instantaneous charge demand of the amplifier, maintaining low distortion that otherwise can degrade because of incomplete amplifier settling. The RC filter combination (R_{FIL}, C_{DIFF}) is optimized for the SAR ADC sample and hold settling. This combination reduces nonlinear charge kickback of the SAR ADC and is optimized for best THD performance. This combination allows for the best trade-off between harmonic distortion while maintaining stability of the PGA output stage.

High-grade C0G (NPO) are used everywhere in the signal path (C_{IN_DIFF}, C_{IN_CM}, C_{FB}, C_{DIFF}, C_{CM}) for the low distortion properties.

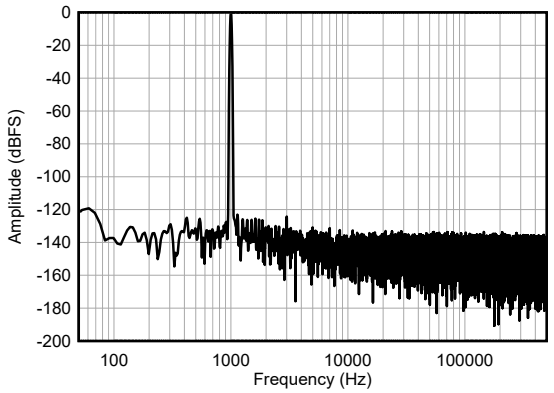
The results are shown in 表 9-5, which includes the typical signal-to-noise ratio (SNR) and total harmonic distortion (THD) of the PGA855 driving the ADS8900B SAR ADC. For the SNR and THD measurements, a 1-kHz differential signal is applied. The signal amplitude is adjusted to produce a PGA855 output at –0.5 dBFS of the ADC full-scale range. 表 9-5 shows the equivalent input voltage amplitude signal for different PGA855 gain configurations. At gain = 1 V/V, the design achieves a –121.4-dB THD and 101.2-dB SNR.

表 9-5. PGA855 and ADS8900B FFT Data Summary: f_{SAMPLE} = 1 MSPS, f_{IN} = 1 kHz

PGA GAIN (V/V)	INPUT AMPLITUDE (V_{PP})	ADC SIGNAL POWER (dBFS)	SNR (dB)	THD (dB)	ENOB (Bits)
0.125	40.10	–6.0	95.9	–118.2	15.6
0.25	36.48	–0.8	101.0	–118.6	16.5
0.5	18.24	–0.8	101.2	–121.0	16.5
1	9.12	–0.8	101.2	–121.7	16.5
2	4.56	–0.8	100.5	–121.6	16.4
4	2.28	–0.8	99.5	–121.3	16.2
8	1.14	–0.8	97.4	–119.4	15.9
16	0.58	–0.8	93.6	–117.3	15.2

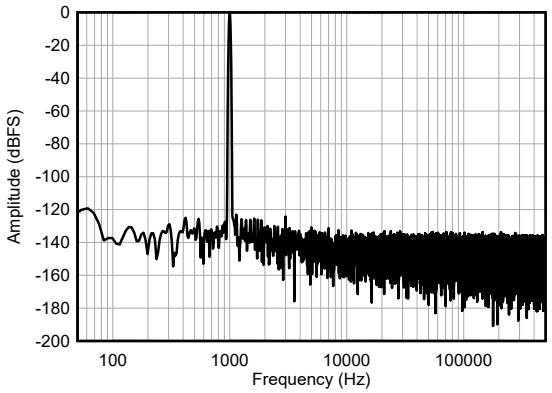
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9.2.2.3 Application Curves



Gain = 1 V/V, f_{SAMPLE} = 1 MSPS, f_{IN} = 1 kHz

図 9-10. Performance FFT Plot With ADS8900B



Gain = 4 V/V, f_{SAMPLE} = 1 MSPS, f_{IN} = 1 kHz

図 9-11. Performance FFT Plot With ADS8900B

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9.3 Power Supply Recommendations

The nominal performance of the PGA855 is specified with input-stage supply and output-stage supply voltages of ±15 V, and V_{ICM} and V_{OCM} at mid-supply. Within the specified limits, custom input and output common-mode voltages can be used without compromising performance; see also セクション 7.3.

> **注意**
> To prevent damage to internal circuitry, the output-stage power supplies are clamped to stay within the input-stage supply voltage levels; see セクション 8.2.

9.4 Layout

9.4.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- To avoid converting common-mode signals into differential signals and thermal electromotive forces (EMFs), make sure that both input paths are symmetrical and well-matched for source impedance and capacitance.
- Noise can propagate into analog circuitry through the power pins of the device and of the circuit as a whole. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V_{S+} and V_{LVDD} to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Leakage on the FDA_IN+ and FDA_IN– pins can cause in a dc offset error in the output voltages. Additionally, excessive parasitic capacitance at these pins can result in decreased phase margin and affect the stability of the output stage. If these pins are not used to implement deliberate capacitive feedback, follow best practices to minimize leakage and parasitic capacitance.
- Follow best practices to minimize leakage and parasitic capacitance, which includes implementing *keep-out* areas in any ground planes that lie immediately below the input pins.
- Minimize the number of thermal junctions. If possible, route the signal path using a single layer without vias.
- Keep sufficient distance from major thermal energy sources (circuits with high power dissipation). If not possible, place the device so that the effects of the thermal energy source on the high and low sides of the differential signal path are evenly matched.
- Keep the traces as short as possible.

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9.4.2 Layout Example

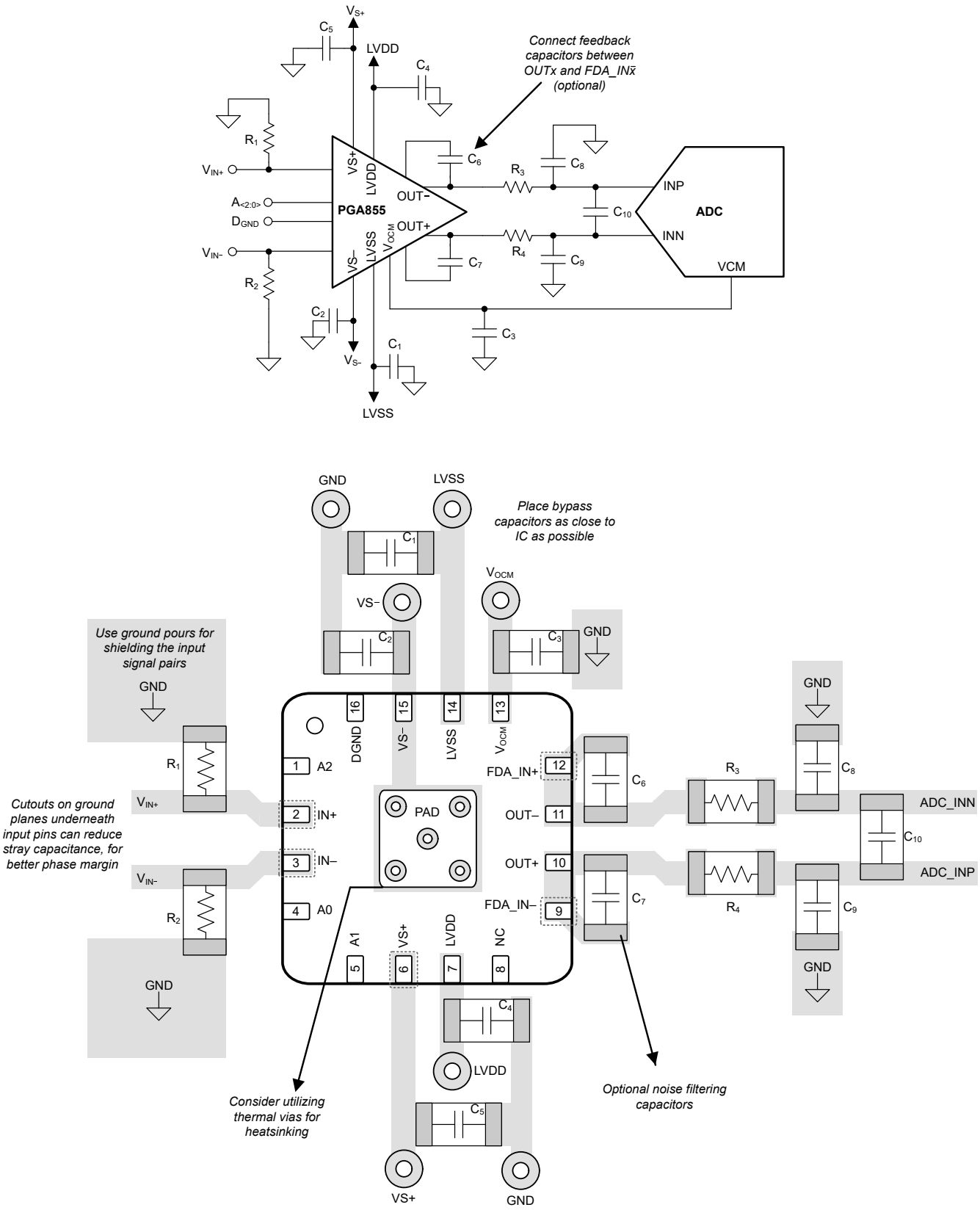


図 9-12. Example Schematic and Associated PCB Layout

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10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

10.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Comprehensive Error Calculation for Instrumentation Amplifiers* application note
- Texas Instruments, *Importance of Input Bias Current Return Paths in Instrumentation Amplifier Applications* application note

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10.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PGA855RGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PGA855
PGA855RGTR.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PGA855

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

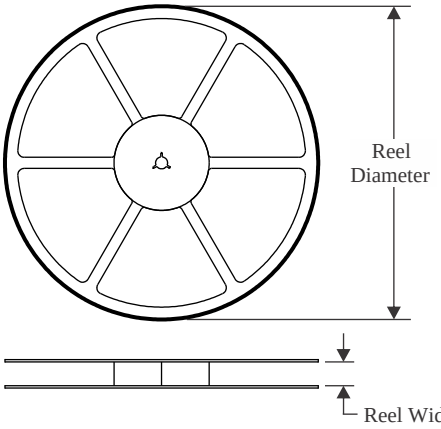
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

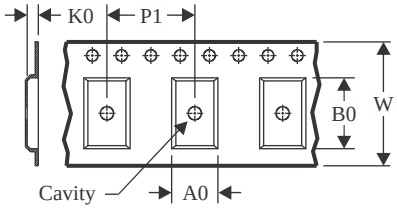
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

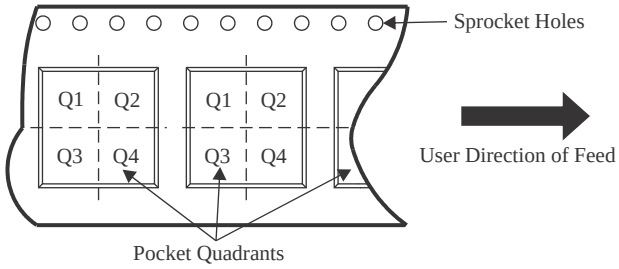


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

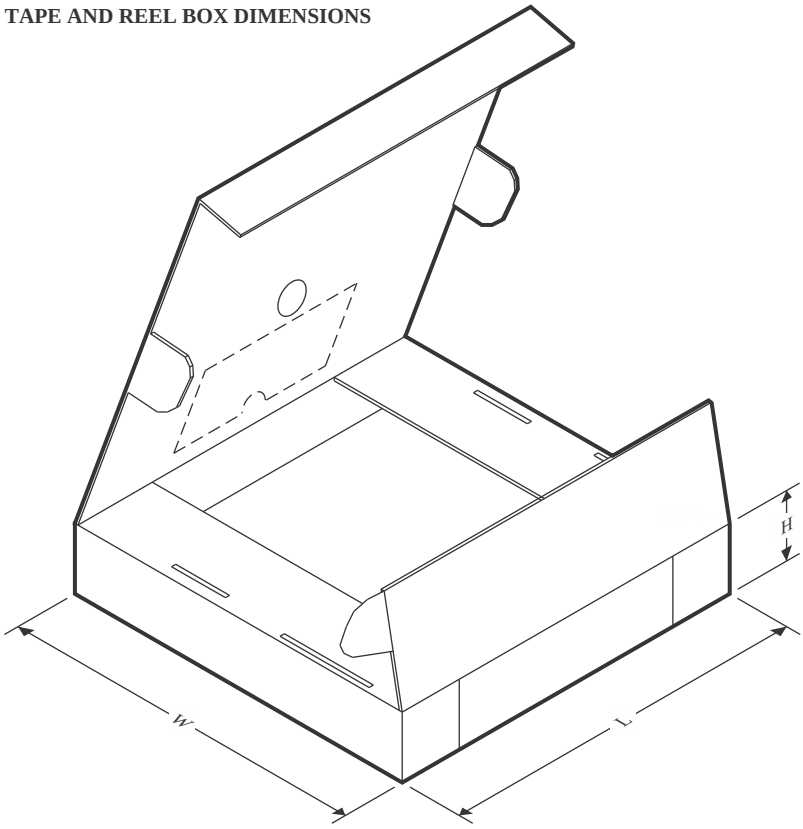
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA855RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

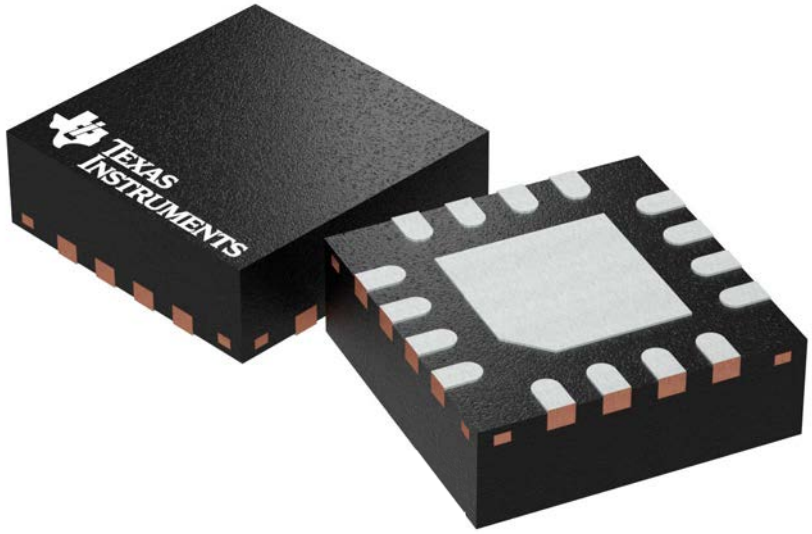


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA855RGTR	VQFN	RGT	16	3000	360.0	360.0	36.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



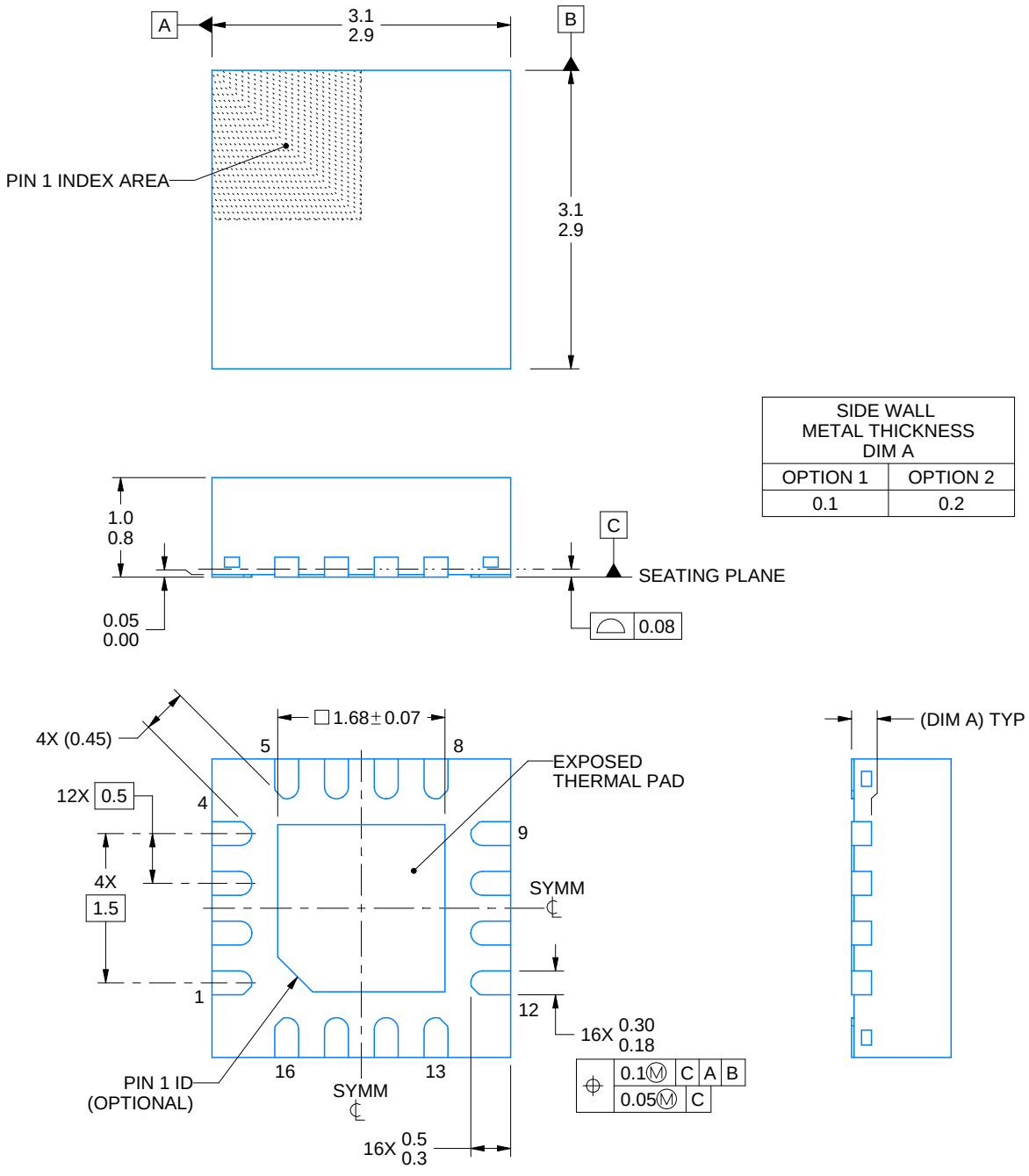
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

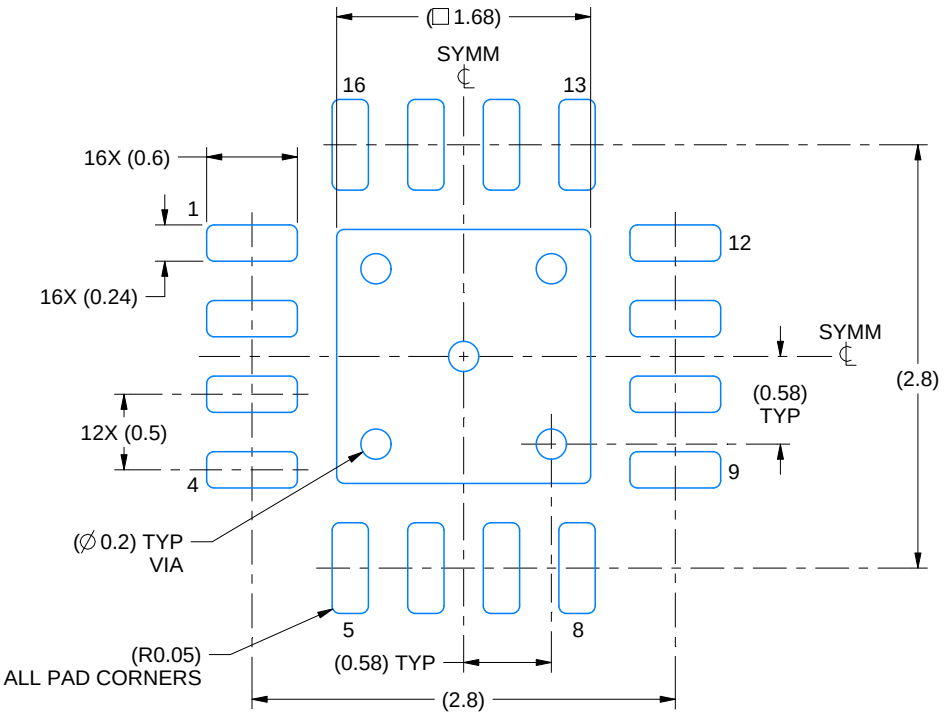
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

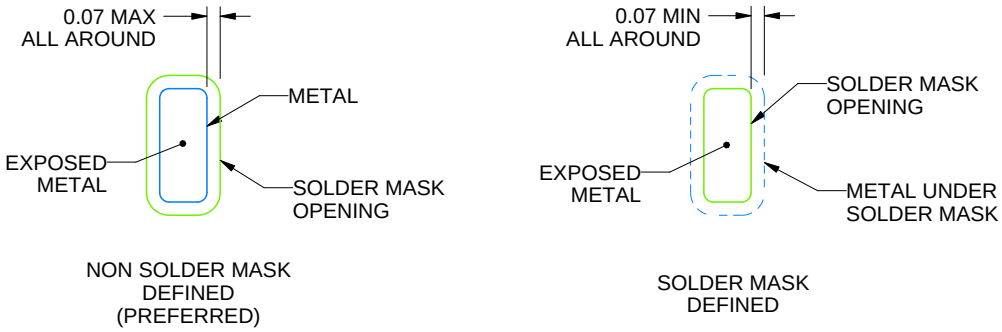


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

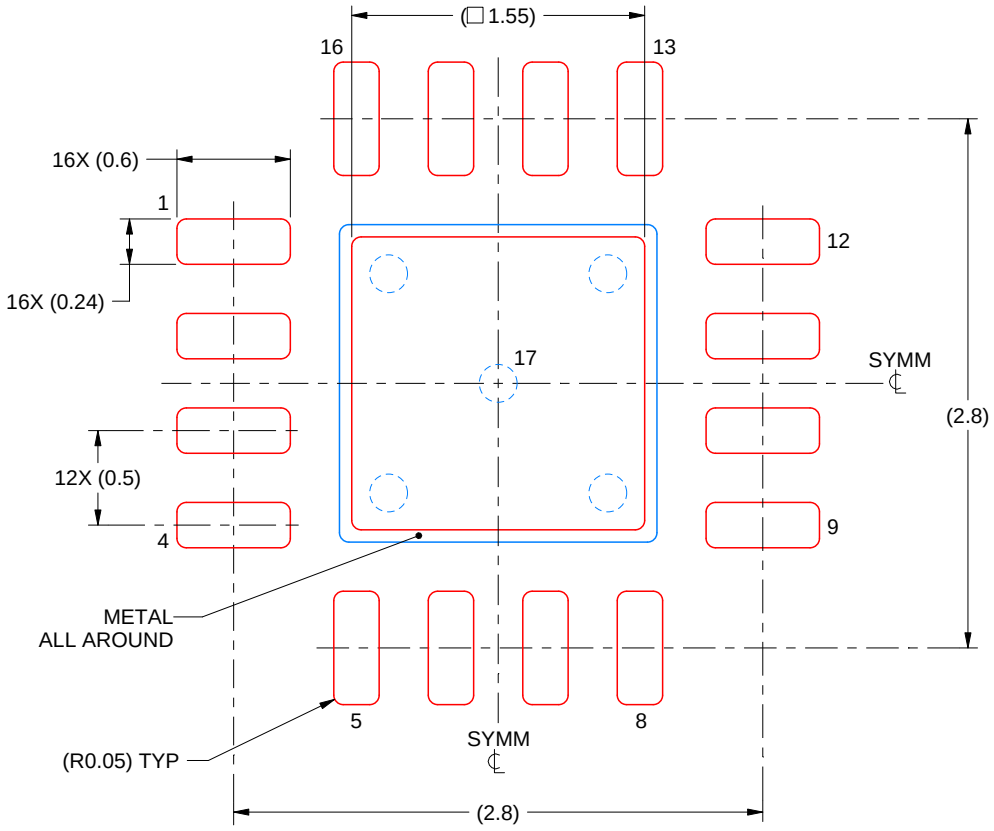


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/E 07/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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