REF35 超低消費電力、高精度電圧リファレンス

1 特長

- 超低静止電流:
  - 650nA (標準値)
- 初期精度:±0.05% (最大値)
- 温度係数 (最大値):
  - 12ppm/℃ (−40℃～105℃、SOT23 パッケージ)
  - 10ppm/℃ (−40℃～85℃、WCSP パッケージ)
- 出力 1/f ノイズ (0.1Hz～10Hz):3.3ppm$_{P-P}$
- ノイズ低減用に NR ピンを搭載
- シャットダウン時の消費電流の低減用に EN ピンを搭載
- 長期安定性:1000 時間で 40ppm
- 熱ヒステリシス:70ppm
- 動作温度範囲:-55℃～+125℃
- 出力電流:+10mA、-5mA
- 入力電圧:V_{REF} + V_{DO} ～ 6V
- 出力電圧オプション:
  - 1.024V、1.2V、1.25V、1.6V、1.8V、2.048V、2.5V、3.0V、3.3V、4.096V、5.0V
- 小型の 6 ピン SOT-23 パッケージ
- 最小フットプリントの 4 ピン WCSP パッケージ

2 アプリケーション

- 流量トランスミッタ
- 血糖値測定器
- サーボ・ドライブ制御モジュール
- 電力品質分析器
- 障害インジケータ
- オシロスコープ
- プロセス分析
- 光学モジュール

3 概要

REF35 は、ナノパワー、低ドリフト、高精度シリーズのリファレンス デバイスのファミリです。REF35 ファミリは、±0.05% の初期精度と 650nA の標準消費電力を特長としています。このデバイスの温度係数 (12ppm/℃) と長期安定性 (1000 時間で 40ppm) は、システムの安定性と信頼性の向上に役立ちます。低消費電力と高精度の仕様を組み合わせて、広範な携帯型 / 低電流アプリケーション向けに設計されています。

REF35 は、3.3ppm$_{p-p}$ ノイズおよび 20ppm/mA のロードレギュレーションで、最大 10mA の電流を供給します。この機能セットにより、REF35 は高精度センサと 12～16 ビット データ コンバータ向けの強力な低ノイズで高精度の電源を実現します。

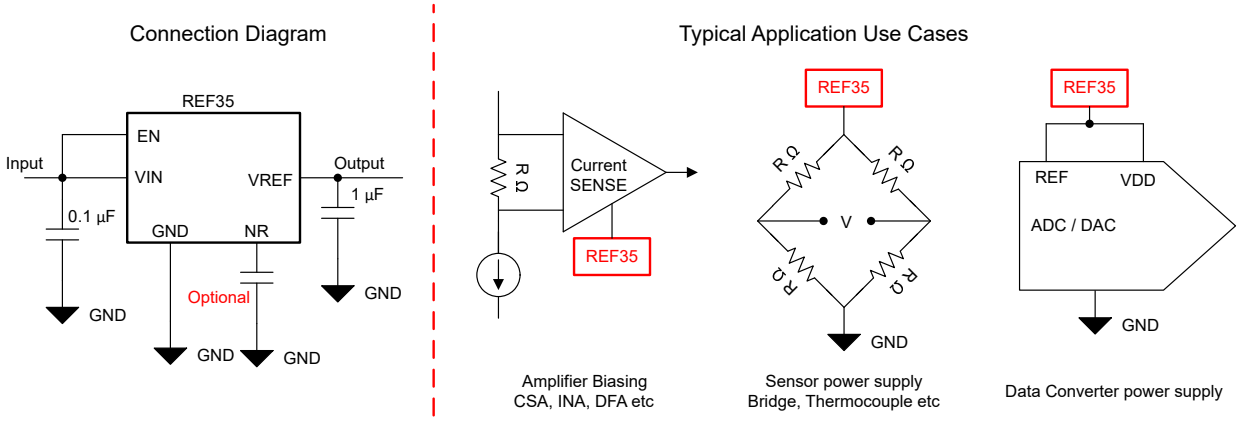
このファミリは -40℃～105℃の範囲で動作仕様を満たし、-55℃～125℃で機能します。この広い温度範囲は産業用アプリケーションに適しています。

REF35 は、1.024V～5.0V の広い出力電圧バリアントで供給されます。このデバイスは、省スペースの 6 ピン SOT-23 パッケージ および 4 ピン WCSP パッケージのオプションで供給されます。利用可能な電圧とパッケージのオプションについては、TI の販売代理店にお問い合わせください。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)(2)
REF35xxx	SOT-23 (6)	2.90mm × 1.60mm
	WCSP (4)	1.05mm × 0.84mm

(1) 利用可能なすべての電圧バリアントおよびパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



REF35 のユースケース

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Device Comparison

PRODUCT		V_{REF}
SOT-23 (6)	WCSP (4)	
REF35102QDBVR	REF35102YBHR	1.024V
REF35120QDBVR	REF35120YBHR	1.2V
REF35125QDBVR	REF35125YBHR	1.25V
REF35160QDBVR	REF35160YBHR	1.6V
REF35170QDBVR	-	1.7V
REF35180QDBVR	REF35180YBHR	1.8V
REF35205QDBVR	-	2.048V
REF35250QDBVR	REF35250YBHR	2.5V
REF35300QDBVR	REF35300YBHR	3.0V
REF35330QDBVR	-	3.3V
REF35360QDBVR	-	3.6V
REF35409QDBVR	REF35409YBHR	4.096V
REF35500QDBVR	-	5.0V

5 Pin Configuration and Functions

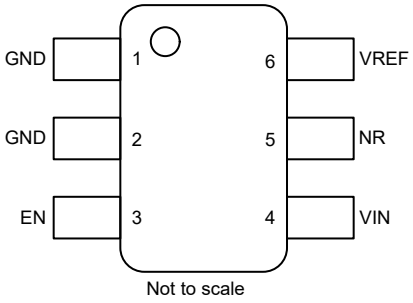


図 5-1. DBV Package 6-Pin SOT-23 Top View

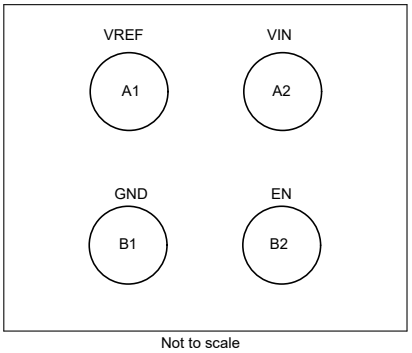


図 5-2. YBH Package 4-Pin WCSP Top View

表 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	SOT-23	WCSP		
GND	1	B1	Ground	Device ground connection. For DBV package pin 1 and pin 2 are internally short.
GND	2	-	Ground	Device ground connection.
EN	3	B2	Input	Enable connection. Enables or disables the device.
VIN	4	A2	Power	Input supply voltage connection.
NR	5	-	Output	Noise reduction pin. Connect a capacitor to reduce noise. This pin can be left floating.
VREF	6	A1	Output	Reference voltage output.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	IN	–0.3	6.5	V
Enable voltage	EN	–0.3	IN + 0.3 (2)	V
Output voltage	V_{REF}	–0.3	IN + 0.3 (2)	V
Output short circuit current	I_{SC}		20	mA
Operating temperature range	T_A	–55	125	°C
Storage temperature range	T_{stg}	–65	170	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) IN + 0.3V or 6.5V, whichever is lower

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins (2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IN	Input voltage (1)	V_{OUT} + V_{DO} (2)		6	V
EN	Enable voltage	0		IN	V
I_L	Output current	–5		10	mA
T_A	Operating temperature	–40	25	125	°C

(1) For V_{REF} = 1.024V to 1.5V, minimum V_{IN} = 1.7V
(2) V_{DO} = Dropout voltage

6.4 Thermal Information

THERMAL METRIC(1)		REF35		UNIT
		YBH (WCSP)	DBV (SOT-23)	
		4 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	178.9	164.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.1	102.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.3	59.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	44.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	60.2	59.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

At V_{IN} = V_{REF} + 0.5V, V_{EN} = V_{IN}, C_L = 10µF, C_{IN} = 0.1µF, I_L = 0mA, minimum and maximum specifications at T_A = –40°C to 125°C, typical specifications T_A = 25°C; unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT							
	Output voltage accuracy	T_A = 25°C		–0.05		0.05	%
	Output voltage temperature coefficient	–40°C ≤ T_A ≤ 105°C				12	ppm/°C
LINE AND LOAD REGULATION							
$\Delta V_{REF}/\Delta V_{IN}$	Line regulation	V_{REF} < 2.5V; V_{IN} = V_{REF} + V_{DO} to V_{INMAX}; –40°C ≤ T_A ≤ 105°C			40	160	ppm/V
		V_{REF} ≥ 2.5V; V_{IN} = V_{REF} + V_{DO} to V_{INMAX}; –40°C ≤ T_A ≤ 105°C			40	120	ppm/V
$\Delta V_{REF}/\Delta I_L$	Load regulation	I_L = 0mA to 10mA, V_{IN} = V_{REF} + V_{DO}	Source		20	60	ppm/mA
		I_L = 0mA to 5mA, V_{IN} = V_{REF} + V_{DO}	Sink		40	350	ppm/mA
POWER SUPPLY							
V_{IN}	Input voltage (1)			V_{REF} + V_{DO}		6	V
I_Q	Quiescent current	Active mode	T_A = 25°C		0.65	0.9	µA
			–40°C ≤ T_A ≤ 85°C			1.3	
			–40°C ≤ T_A ≤ 125°C			2.6	
		Shutdown mode	T_A = 25°C			0.1	
			–40°C ≤ T_A ≤ 125°C			0.5	
V_{EN}	Enable pin voltage	Active mode (EN = 1 or Float)		0.7 x V_{IN}			V
		Shutdown mode (EN = 0)				0.3 x V_{IN}	
I_{EN}	Enable pin current	V_{EN} = V_{IN}			0.05	0.1	uA
V_{DO}	Dropout voltage	I_L = 5mA				120	mV
		I_L = 10mA				250	
I_{SC}	Short circuit current, Sourcing	V_{REF} = 0V, T_A = 25°C			33		mA
I_{SC}	Short circuit current, Sinking	V_{REF} = V_{IN} V, T_A = 25°C			21		mA
TURN-ON TIME							
t_{ON}	Turn-on time (2)	0.1% settling, C_L = 1µF, V_{REF} = 2.5V			2		ms
NOISE							
e_n	Output voltage noise	f = 10Hz to 1kHz, C_L = 1µF			0.7		ppm_{rms}
e_{np-p}	Low-frequency noise	f = 0.1Hz to 10Hz, V_{REF} ≥ 2.5V			3.8		ppm_{p-p}
		f = 0.1Hz to 10Hz, V_{REF} < 2.5V			3.3		ppm_{p-p}
HYSTERESIS AND LONG-TERM STABILITY							
	Long-term stability	0 to 1000h at 35°C			40		ppm
	Output voltage hysteresis	25°C, –40°C, 105°C, 25°C (cycle 1)			70		ppm
	Output voltage hysteresis	25°C, –40°C, 105°C, 25°C (cycle 2)			20		ppm
	Output voltage hysteresis	25°C, –40°C, 85°C, 25°C (cycle 1)			50		ppm
	Output voltage hysteresis	25°C, –40°C, 85°C, 25°C (cycle 2)			13		ppm
STABLE CAPACITANCE RANGE							

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6.5 Electrical Characteristics (続き)

At V_{IN} = V_{REF} + 0.5V, V_{EN} = V_{IN}, C_L = 10µF, C_{IN} = 0.1µF, I_L = 0mA, minimum and maximum specifications at T_A = –40℃ to 125℃, typical specifications T_A = 25℃; unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
	Input capacitor range		0.1			µF
	Output capacitor range (3)		0.1		10	µF

(1) For V_{REF} = 1.024V to 1.5V, minimum V_{IN} = 1.7V
(2) Scales linearly with V_{REF}.
(3) ESR for the capacitor <= 400mΩ

6.6 Electrical Characteristics YBH package

At V_{IN} = V_{REF} + 0.5V, V_{EN} = V_{IN}, C_{REF} = 10µF, C_{IN} = 0.1µF, I_L = 0mA, minimum and maximum specifications at T_A = –40℃ to 125℃, typical specifications T_A = 25℃; unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT							
	Output voltage accuracy	T_A = 25℃		–0.05		0.05	%
	Output voltage temperature coefficient	–40℃ ≤ T_A ≤ 85℃				10	ppm/℃
LINE AND LOAD REGULATION							
$\Delta V_{REF}/\Delta V_{IN}$	Line regulation	V_{REF} < 2.5V; V_{IN} = V_{REF} + V_{DO} to V_{INMAX}			40	160	ppm/V
		V_{REF} ≥ 2.5V; V_{IN} = V_{REF} + V_{DO} to V_{INMAX}			40	80	ppm/V
$\Delta V_{REF}/\Delta I_L$	Load regulation	I_L = 0mA to 10mA, V_{IN} = V_{REF} + V_{DO}	Source		20	60	ppm/mA
		I_L = 0mA to 5mA, V_{IN} = V_{REF} + V_{DO}	Sink		40	350	ppm/mA
POWER SUPPLY							
V_{IN}	Input voltage (1)			V_{REF} + V_{DO}		6	V
I_Q	Quiescent current	Active mode	T_A = 25℃		0.65	0.9	µA
			–40℃ ≤ T_A ≤ 85℃			1.3	
			–40℃ ≤ T_A ≤ 125℃			2.6	
		Shutdown mode	T_A = 25℃			0.1	
			–40℃ ≤ T_A ≤ 125℃			0.5	
V_{EN}	Enable pin voltage	Active mode (EN = 1 or Float)		0.7 x V_{IN}			V
		Shutdown mode (EN = 0)				0.3 x V_{IN}	
I_{EN}	Enable pin current	V_{EN} = V_{IN}			0.05	0.1	uA
V_{DO}	Dropout voltage	I_L = 5mA				120	mV
		I_L = 10mA				250	
I_{SC}	Short circuit current, Sourcing	V_{REF} = 0V, T_A = 25℃			30		mA
I_{SC}	Short circuit current, Sinking	V_{REF} = V_{IN} V, T_A = 25℃			20		mA
TURNON TIME							
t_{ON}	Turn-on time (2)	0.1% settling, C_{REF} = 1µF, V_{REF} = 2.048V			2		ms
NOISE							
e_n	Output voltage noise	f = 10Hz to 1kHz			0.7		ppm_{rms}
e_{np-p}	Low frequency noise	f = 0.1Hz to 10Hz, V_{REF} ≥ 2.5V			3.8		ppm_{p-p}
		f = 0.1Hz to 10Hz, V_{REF} < 2.5V			3.3		ppm_{p-p}
HYSTERESIS AND LONG-TERM STABILITY							
	Long-term stability	0 to 1000h at 35°C			40		ppm

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6.6 Electrical Characteristics YBH package (続き)

At V_{IN} = V_{REF} + 0.5V, V_{EN} = V_{IN}, C_{REF} = 10µF, C_{IN} = 0.1µF, I_L = 0mA, minimum and maximum specifications at T_A = –40°C to 125°C, typical specifications T_A = 25°C; unless otherwise noted

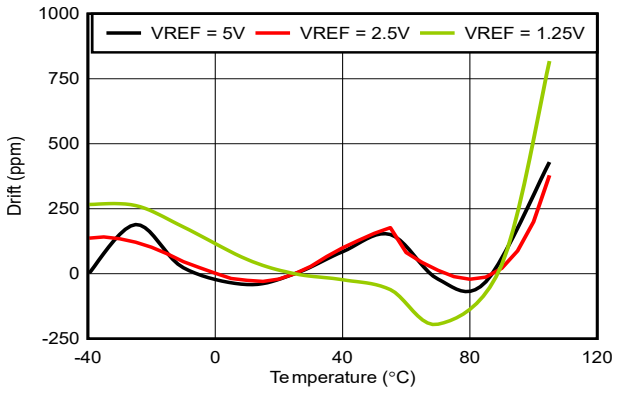
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
	Output voltage hysteresis	25°C, –40°C, 125°C, 25°C (cycle 1)		70		ppm
STABLE CAPACITANCE RANGE						
	Input capacitor range		0.1			µF
	Output capacitor range (3)		0.1		10	µF

(1) For V_{REF} = 1.024V to 1.5V, minimum V_{IN} = 1.7V.
(2) Scales linearly with V_{REF}.
(3) ESR for the capacitor can range from 10mΩ to 400mΩ.

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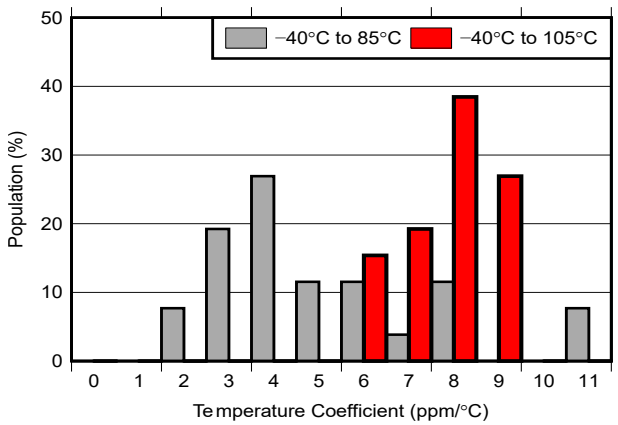
6.7 Typical Characteristics

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.3V, I_L = 0mA, C_L = 10µF, C_{IN} = 0.1µF (unless otherwise noted)



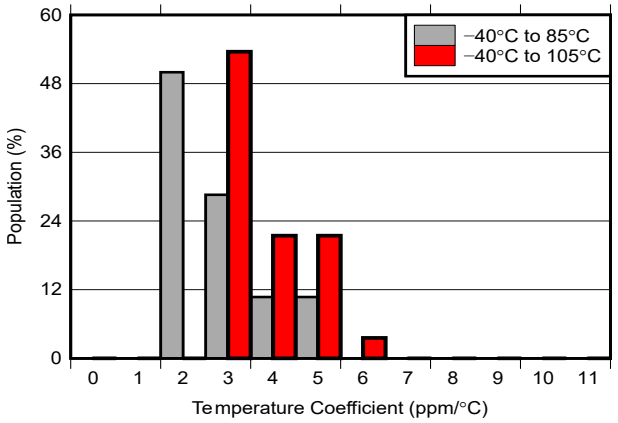
SOT23 Package

図 6-1. Output Voltage Drift vs Free-Air Temperature



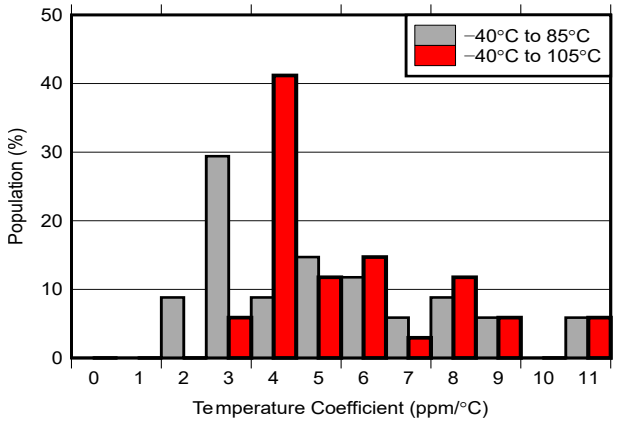
SOT23 Package

図 6-2. Temperature Coefficient Distribution (V_{REF} = 1.25V)



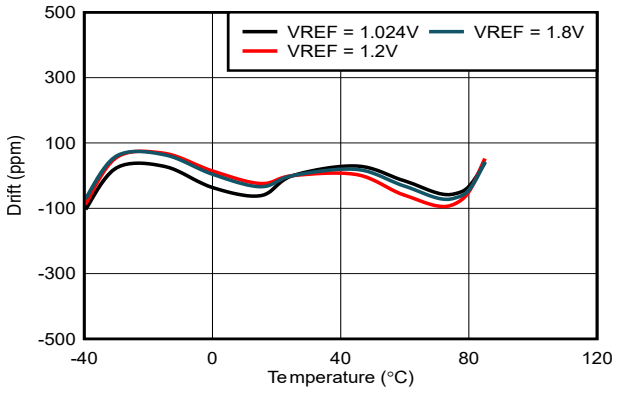
SOT23 Package

図 6-3. Temperature Coefficient Distribution (V_{REF} = 2.5V)



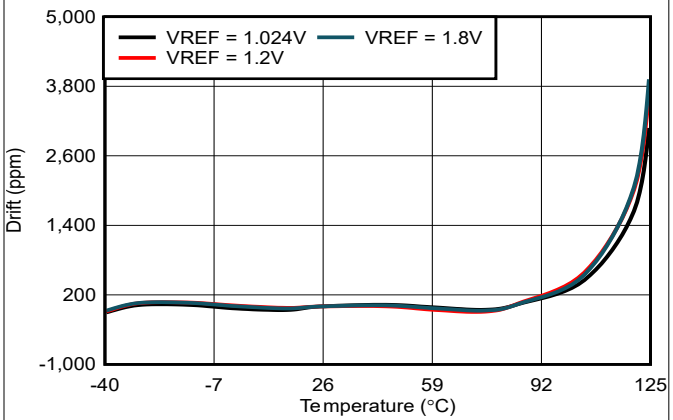
SOT23 Package

図 6-4. Temperature Coefficient Distribution (V_{REF} = 5.0V)



WCSP Package VREF < 2.5V (-40ºC to 85ºC)

図 6-5. Output Voltage Drift vs Free-Air Temperature



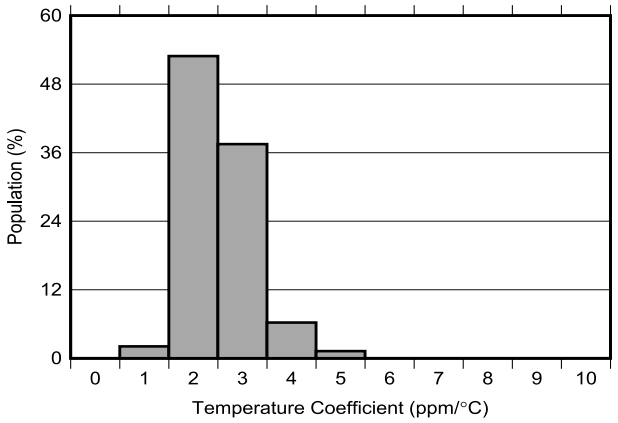
WCSP Package VREF < 2.5V (-40ºC to 125ºC)

図 6-6. Output Voltage Drift vs Free-Air Temperature

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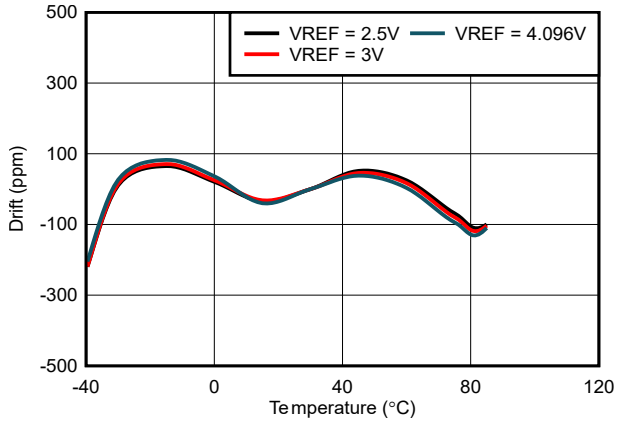
6.7 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.3V, I_L = 0mA, C_L = 10µF, C_{IN} = 0.1µF (unless otherwise noted)



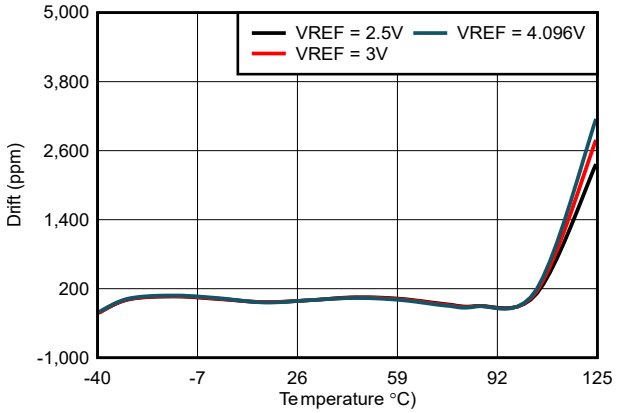
WCSP Package VREF < 2.5V (-40ºC to 85ºC)

図 6-7. Temperature Coefficient Distribution



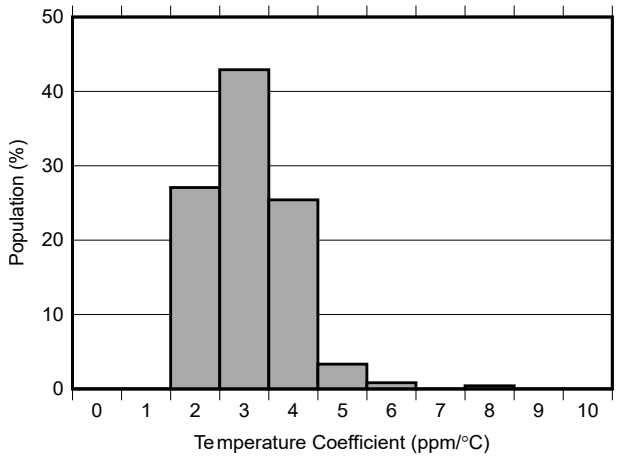
WCSP Package VREF ≥ 2.5V (-40ºC to 85ºC)

図 6-8. Output Voltage Drift vs Free-Air Temperature



WCSP Package VREF ≥ 2.5V (-40ºC to 125ºC)

図 6-9. Output Voltage Drift vs Free-Air Temperature



WCSP Package VREF ≥ 2.5V (-40ºC to 85ºC)

図 6-10. Temperature Coefficient Distribution

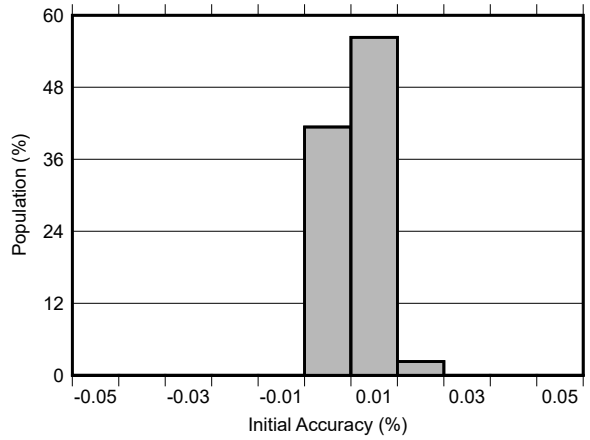


図 6-11. Initial Accuracy Distribution

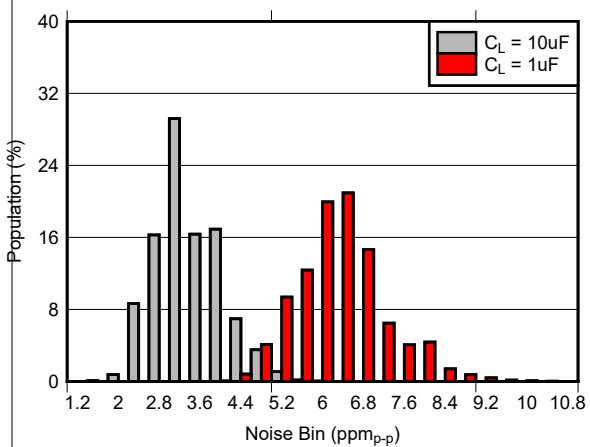


図 6-12. 0.1Hz to 10Hz Noise Distribution (V_{REF} = 1.25V, C_{NR} = Open, I_L = 0mA)

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6.7 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.3V, I_L = 0mA, C_L = 10µF, C_{IN} = 0.1µF (unless otherwise noted)

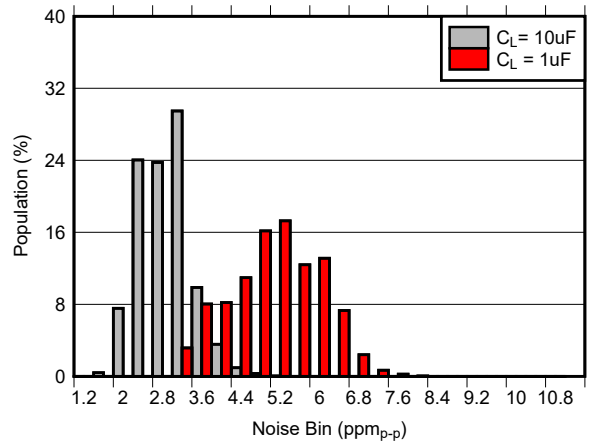


図 6-13. 0.1Hz to 10Hz Noise Distribution (V_{REF} = 2.5V, C_{NR} = Open, I_L = 0mA)

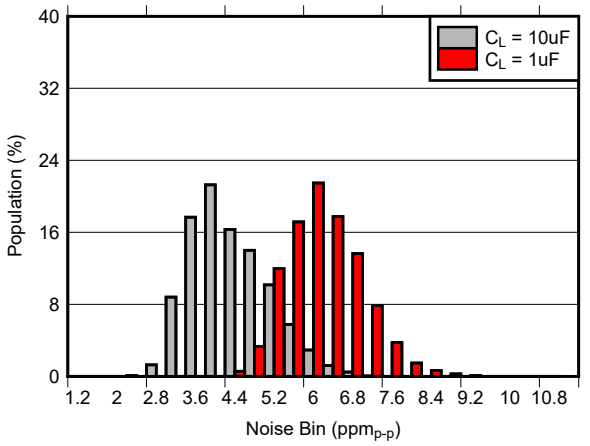


図 6-14. 0.1Hz to 10Hz Noise Distribution (V_{REF} = 5V, C_{NR} = Open, I_L = 0mA)

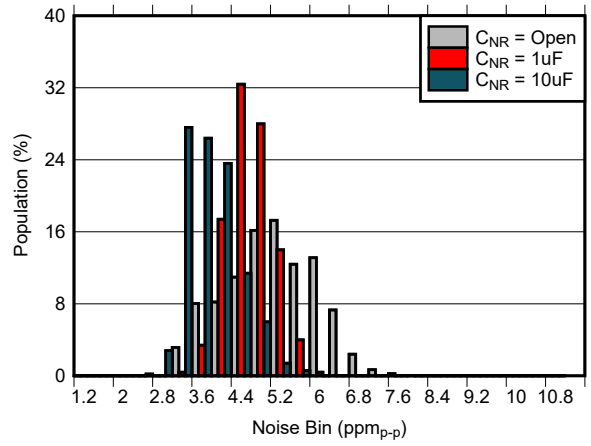


図 6-15. 0.1Hz to 10Hz Noise Distribution (V_{REF} = 2.5V, C_L = 1µF, I_L = 0mA)

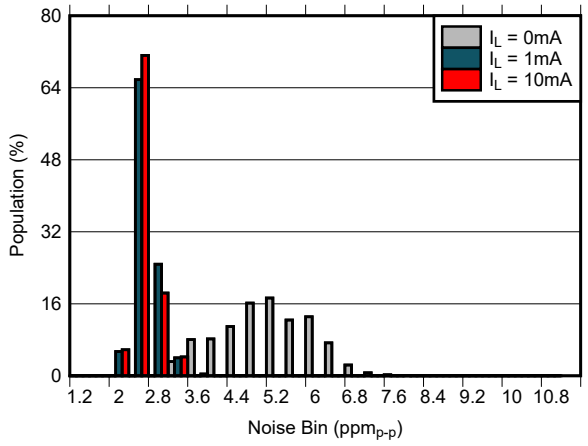


図 6-16. 0.1Hz to 10Hz Noise Distribution (V_{REF} = 2.5V, C_L = 1µF, C_{NR} = Open)

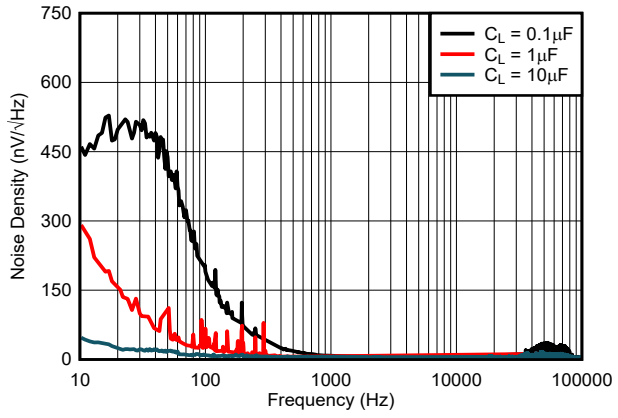


図 6-17. Noise Density vs Frequency (V_{REF} = 1.25V, I_L = 0mA)

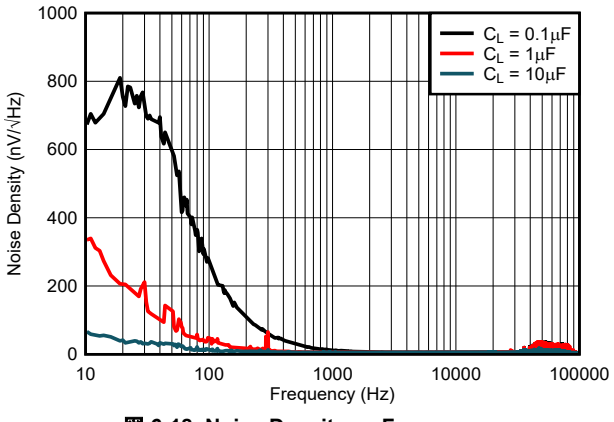


図 6-18. Noise Density vs Frequency (V_{REF} = 2.5V, I_L = 0mA)

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6.7 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.3V, I_L = 0mA, C_L = 10µF, C_{IN} = 0.1µF (unless otherwise noted)

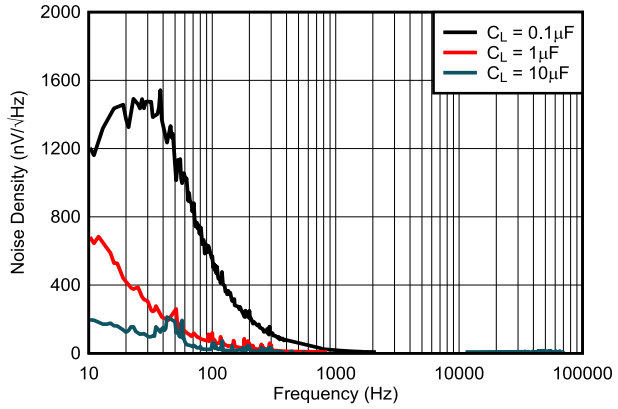


図 6-19. Noise Density vs Frequency (V_{REF} = 5V, I_L = 0mA)

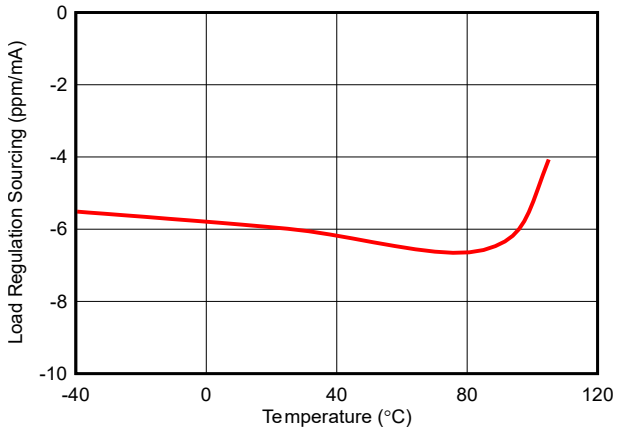


図 6-20. Load Regulation (Sourcing 10mA) vs Free-Air Temperature

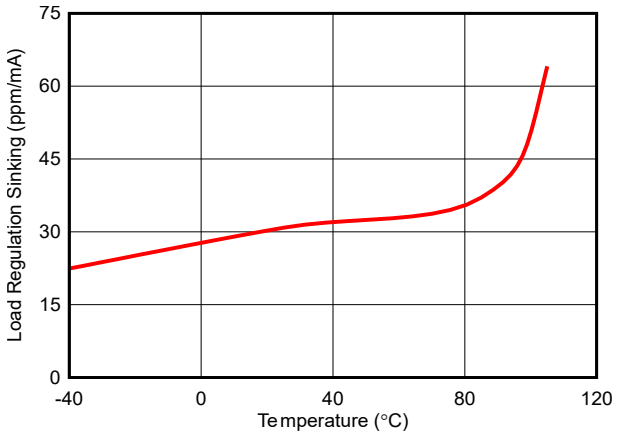


図 6-21. Load Regulation (Sinking 5mA) vs Free-Air Temperature

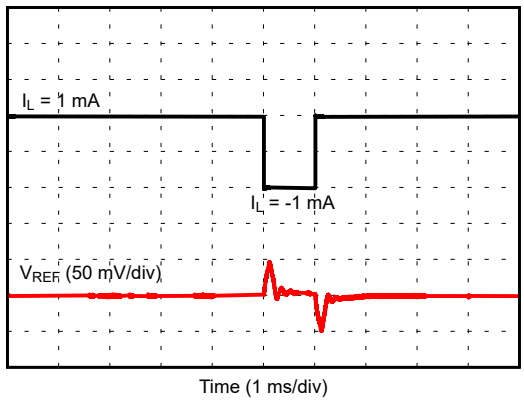


図 6-22. Load Transient Response (V_{REF} = 2.5V, C_L = 10 µF)

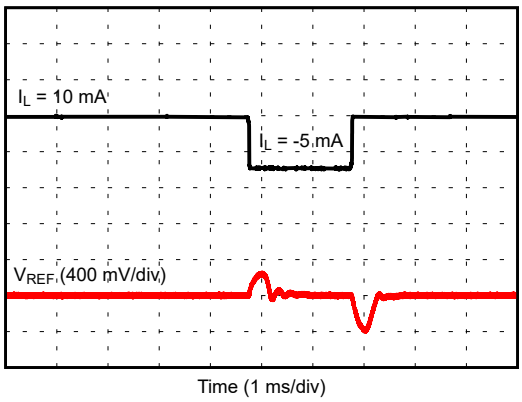


図 6-23. Load Transient Response (V_{REF} = 2.5V, C_L = 10 µF)

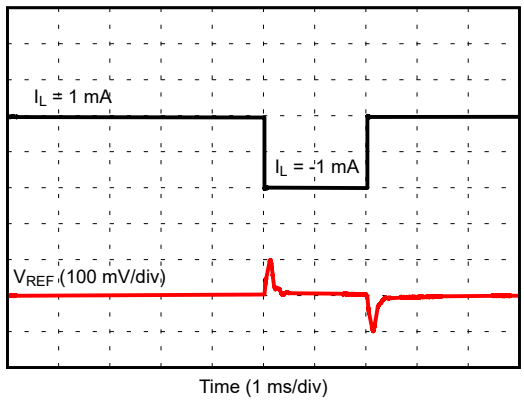


図 6-24. Load Transient Response (V_{REF} = 2.5V, C_L = 1µF)

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6.7 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.3V, I_L = 0mA, C_L = 10µF, C_{IN} = 0.1µF (unless otherwise noted)

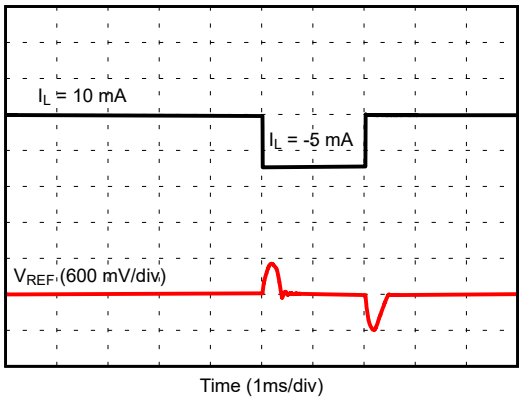


図 6-25. Load Transient Response (V_{REF} = 2.5V, C_L = 1µF)

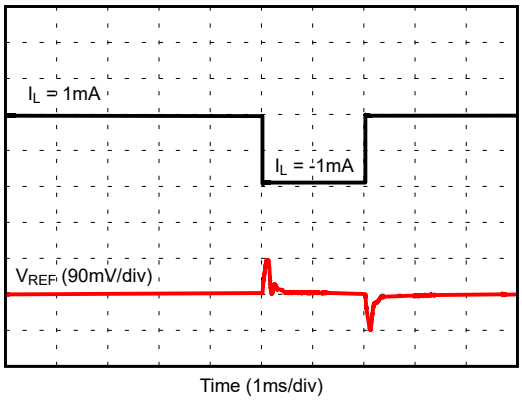


図 6-26. Load Transient Response (V_{REF} = 1.25V, C_L = 1µF)

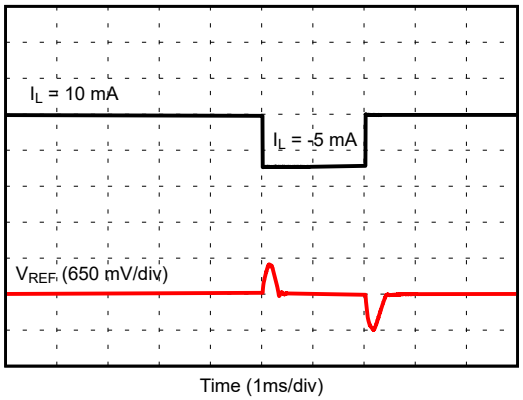


図 6-27. Load Transient Response (V_{REF} = 1.25V, C_L = 1µF)

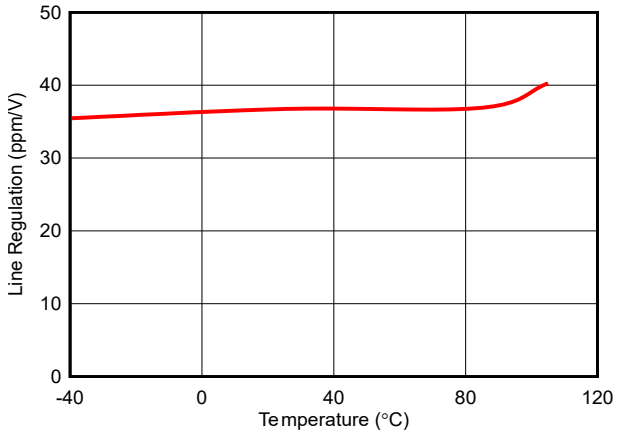


図 6-28. Line Regulation vs Free-Air Temperature

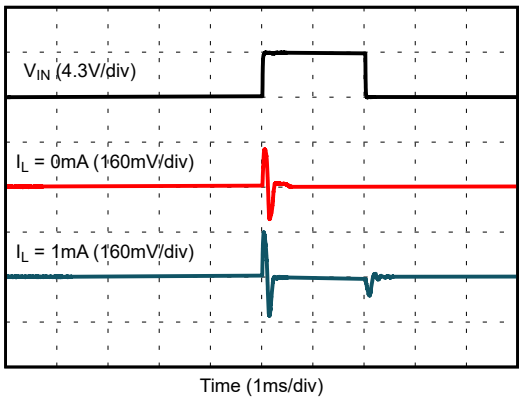


図 6-29. Line Transient Response (V_{REF} = 1.25V, C_L = 1 µF)

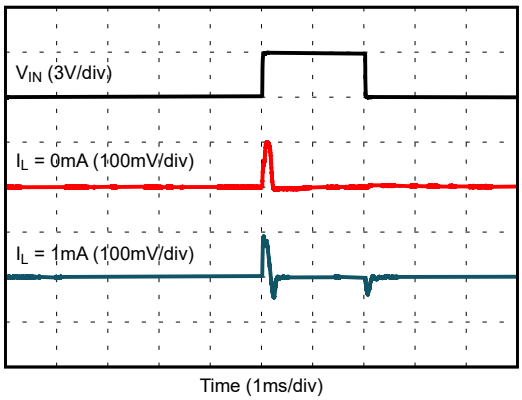


図 6-30. Line Transient Response (V_{REF} = 2.5V, C_L = 1µF)

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6.7 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.3V, I_L = 0mA, C_L = 10µF, C_{IN} = 0.1µF (unless otherwise noted)

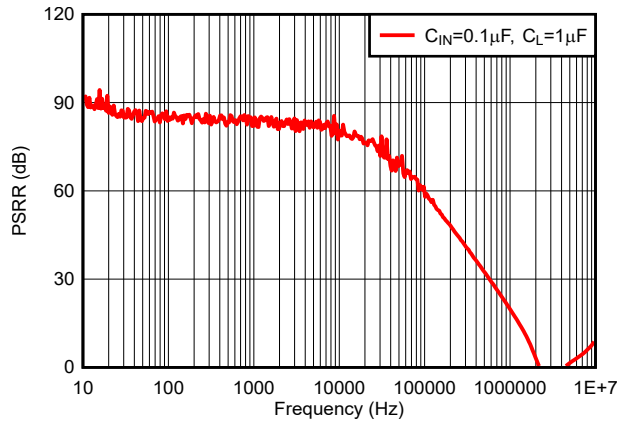


図 6-31. Power Supply Rejection Ratio (V_{REF} = 2.5V, I_L = 0mA)

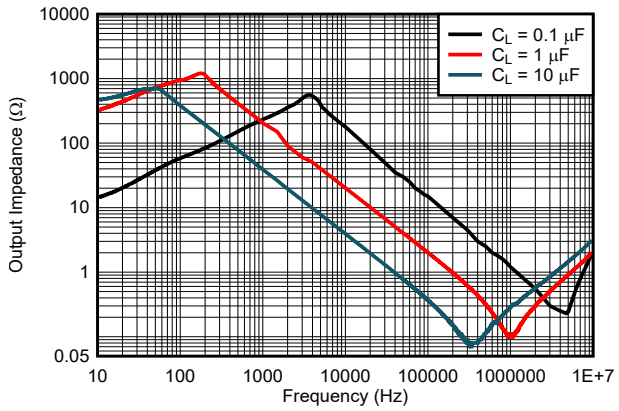


図 6-32. Output Impedance

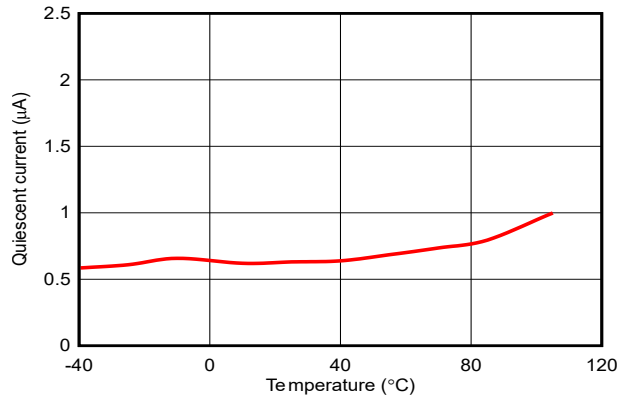


図 6-33. Quiescent Current vs Free-Air Temperature

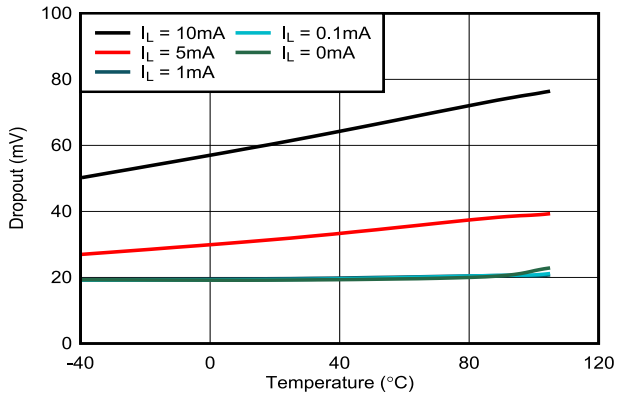


図 6-34. Dropout Voltage vs Free-Air Temperature

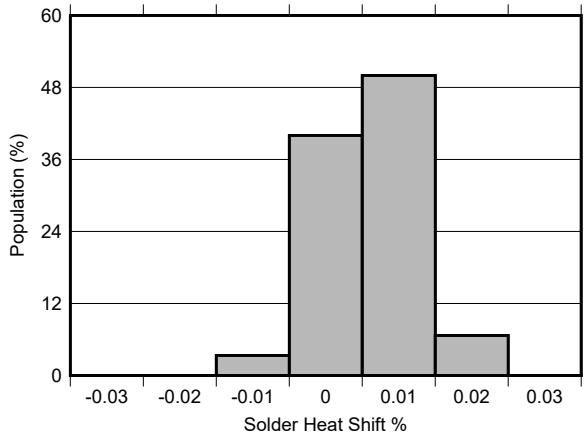


図 6-35. Solder Heat Shift Distribution

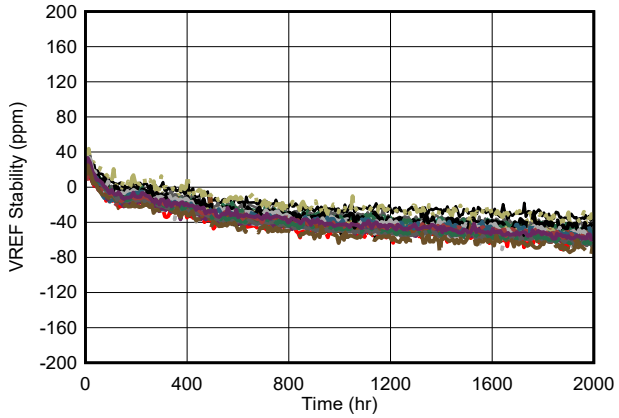


図 6-36. Long Term Stability SOT23 - 2000 hours (V_{REF})

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.3V, I_L = 0mA, C_L = 10µF, C_{IN} = 0.1µF (unless otherwise noted)

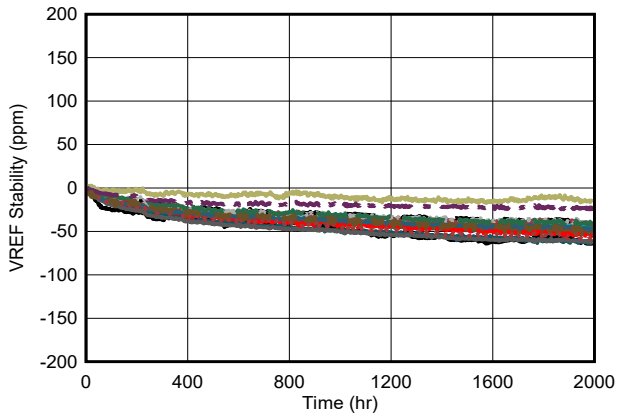


図 6-37. Long Term Stability WCSP - 2000 hours (V_{REF})

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7 Parameter Measurement Information

7.1 Solder Heat Shift

The materials used in the manufacture of the REF35 have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

To illustrate this effect, a total of 32 devices were soldered on one printed circuit board using lead-free solder paste and the paste manufacturer suggested reflow profile. 図 7-1 shows the reflow profile. The printed circuit board is comprised of FR4 material. The board thickness is 1.66mm and the area is 174mm × 135mm.

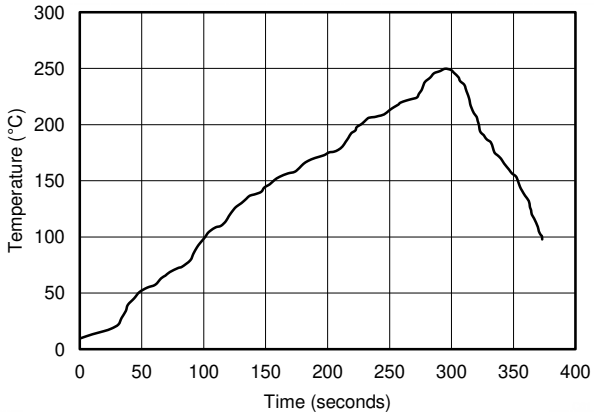


図 7-1. Reflow Profile

The reference output voltage is measured before and after the reflow process; 図 7-2 shows the typical shift. Although all tested units exhibit very low shifts (< 0.03%), higher shifts are also possible depending on the size, thickness, and material of the printed circuit board (PCB). An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, the device must be soldered in the last pass to minimize its exposure to thermal stress.

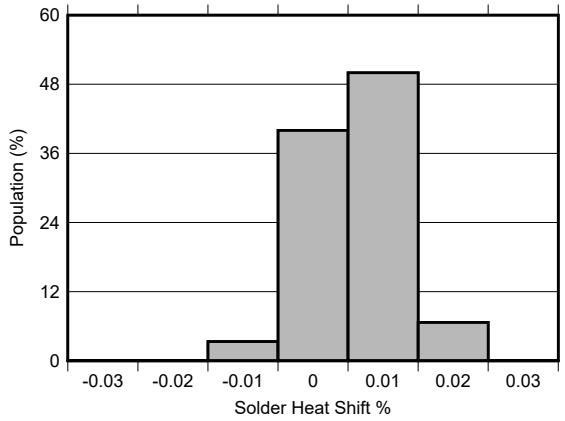


図 7-2. Solder Heat Shift Distribution, V_{REF} (%)

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7.2 Temperature Coefficient

The REF35 is designed and tested for a low output voltage temperature coefficient. The temperature coefficient is defined as the change in output voltage over temperature. The temperature coefficient is calculated using the box method in which a box is formed by the minimum/maximum values for the nominal output voltage over the operating temperature range. REF35 has a low maximum temperature coefficient of 12ppm/°C from –40°C to +105°C. The box method specifies limits for the temperature error but does not specify the exact shape and slope of the device under test. Due to temperature curvature correction to achieve low-temperature drift, the temperature drift is expected to be non-linear. See TI's Analog Design Journal, *Precision voltage references*, for more information on the box method. Use 式 1 for the box method.

$$\text{Drift} = \left(\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF(25°C)} \times \text{Temperature Range}} \right) \times 10^6 \quad (1)$$

図 7-3 shows a typical voltage versus temperature curves for various reference voltages in SOT23 package. 図 7-4 shows the distribution of temperature coefficients for REF35250 devices in SOT23 package.

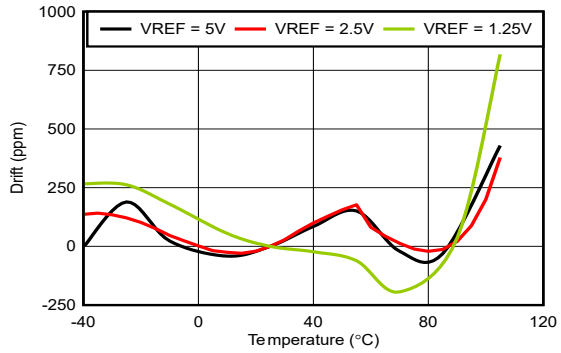


図 7-3. Output Voltage Drift Vs Free-Air Temperature

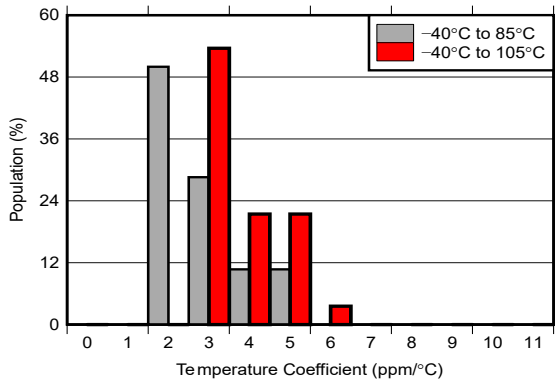


図 7-4. Temperature Coefficient Distribution

7.3 Long-Term Stability

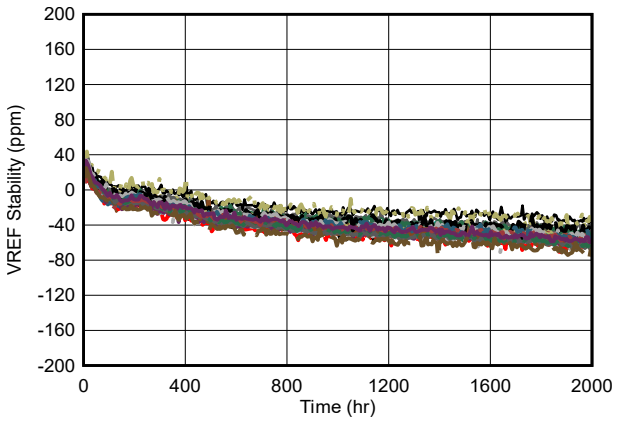
One of the key performance parameters of the REF35 references is long-term stability also known as long-term drift. The long-term stability value is tested in a setup that reflects standard PCB board manufacturing practices. The boards are made of standard FR4 material and the board does not have special cuts or grooves around the devices to relieve the mechanical stress of the PCB. The devices and boards in this test do not undergo high temperature burn in post-soldering prior to testing. These conditions reflect a real world use case scenario and common manufacturing techniques.

During the long-term stability testing, precautions are taken to make sure that only the long-term stability drift is measured. The boards are maintained at 35°C in an oil bath. The oil bath makes sure that the temperature is constant across the device over time compared to an air oven. The measurements are captured every 30 minutes with a calibrated 8.5 digit multimeter.

The typical long-term stability characteristic is expressed as a deviation of the reference voltage output over time.

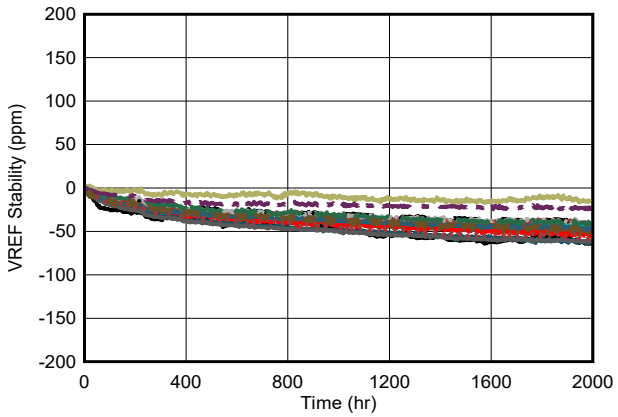
図 7-5 shows that the typical drift value for the REF35 6-pin SOT-23 package is 40ppm from 0 to 1000 hours and 55ppm from 0 to 2000 hours. It is important to understand that long-term stability is not ensured by design and that the value is typical. The REF35 will experience the highest drift in the initial 1000 hr. Subsequent deviation is typically lower than first 1000 hr.

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SOT23 Package

図 7-5. Long Term Stability - 2000 hours (V_{REF})



WCSP Package

図 7-6. Long Term Stability - 2000 hours (V_{REF})

7.4 Thermal Hysteresis

Thermal hysteresis is measured with the REF35 soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. The PCB was baked at 150°C for 30 minutes before thermal hysteresis was measured. Use 式 2 to calculate the thermal hysteresis:

$$V_{HYST} = \left(\frac{| V_{PRE} - V_{POST} |}{V_{NOM}} \right) \times 10^6 \text{ (ppm)} \quad (2)$$

where

- V_{HYST} = thermal hysteresis (in units of ppm)
- V_{NOM} = the specified output voltage
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling
- V_{POST} = output voltage measured after the device has cycled from 25°C through the specified temperature range of –40°C to +85°C or –40°C to +105°C and returns to 25°C.

The graphs below show the typical thermal hysteresis distribution across various temperature ranges in two cycles.

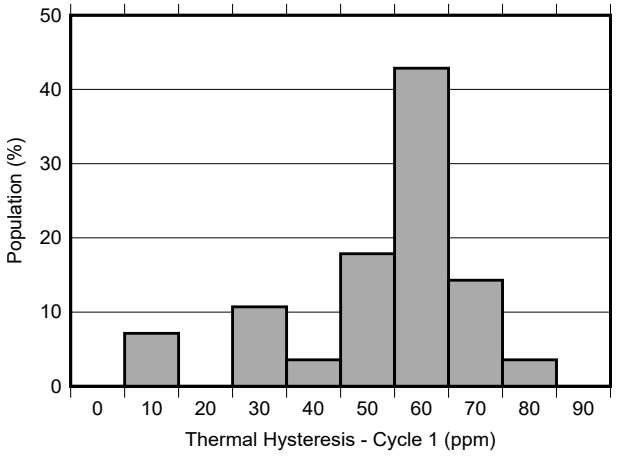


図 7-7. Thermal Hysteresis Distribution –40ºC to 85ºC, Cycle 1

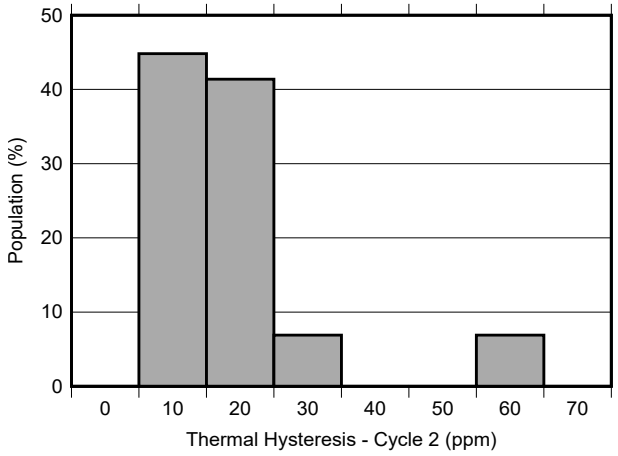


図 7-8. Thermal Hysteresis Distribution –40ºC to 85ºC, Cycle 2

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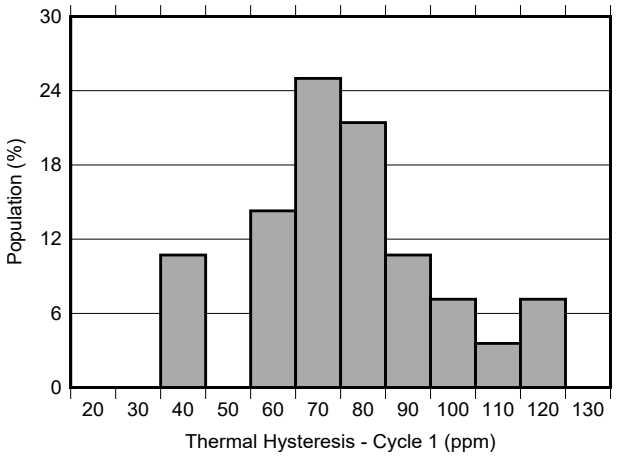


図 7-9. Thermal Hysteresis Distribution –40ºC to 105ºC, Cycle 1

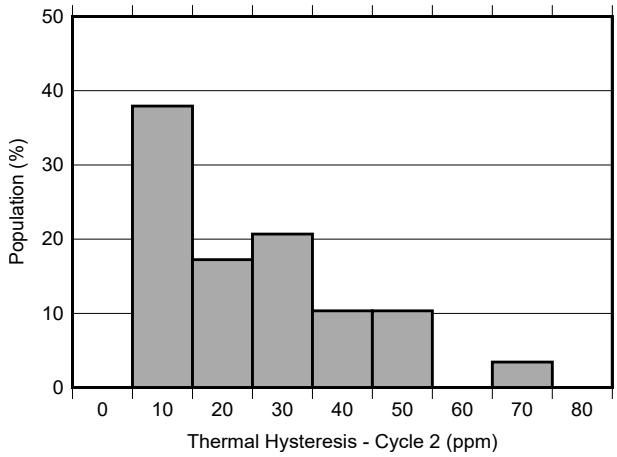


図 7-10. Thermal Hysteresis Distribution –40ºC to 105ºC, Cycle 2

7.5 Noise Performance

The reference pin output noise is categorized as low frequency and broadband noise. The following sections describe these categories in detail.

7.5.1 Low-Frequency (1/f) Noise

Flicker noise, also known as 1/f noise, is a low-frequency noise that affects the device output voltage which can affect precision measurements in ADCs. This noise increases proportionally with output voltage and operating temperature. Noise is measured by filtering the output from 0.1Hz to 10Hz. The 1/f noise is an extremely low value, therefore the frequency of interest must be amplified and band-pass filtered. This is done by using a high-pass filter to block the DC voltage. The resulting noise is then amplified by a gain of 1000. The bandpass filter is created by a series of high-pass and low-pass filter that adds additional gain to make it more visible on a oscilloscope as shown in 図 7-11. 図 7-12 shows the effect of flicker noise over 10 second for REF35250. Flicker noise must be tested in a Faraday cage enclosure to block environmental noise.

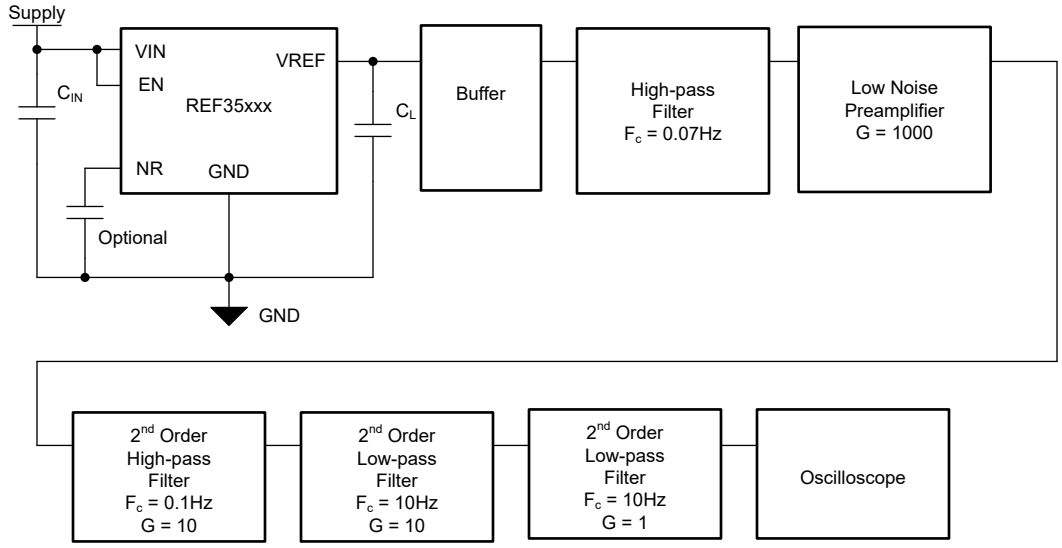


図 7-11. Low-Frequency (1/f) Noise Test Setup

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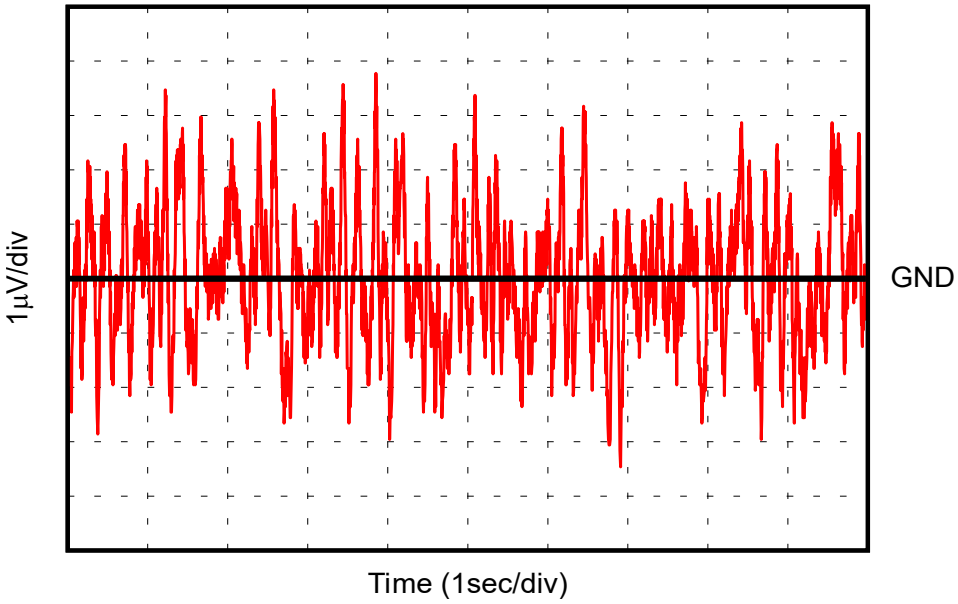


図 7-12. 0.1Hz to 10Hz Voltage Noise

図 7-13 shows the typical 1/f noise (0.1Hz to 10Hz) distribution across various load conditions. REF35 device also offers noise reduction functionality by adding an optional capacitor between NR (pin 5) and ground pins.

図 7-14 shows the typical 1/f noise (0.1Hz to 10Hz) distribution across REF35 devices with various capacitance between NR pin and GND.

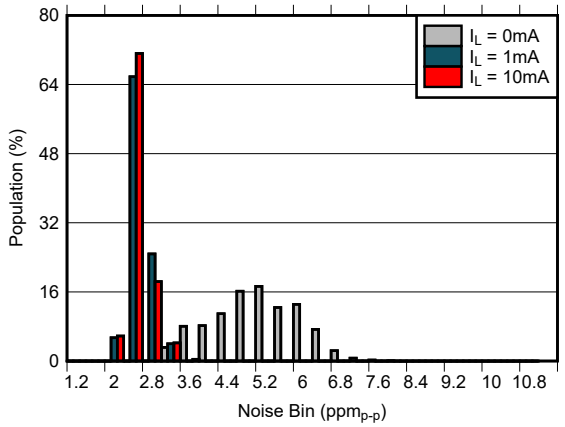


図 7-13. 0.1Hz to 10Hz Noise Distribution vs Load Conditions

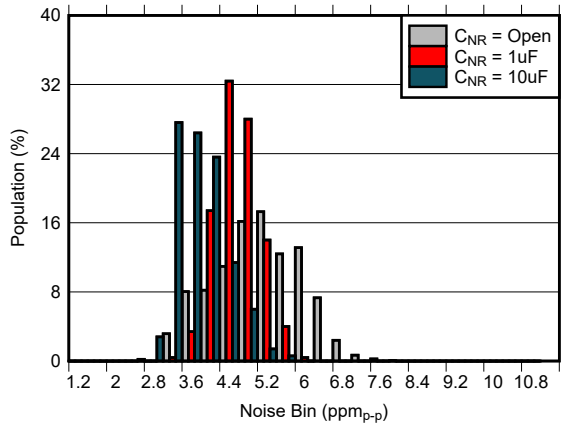


図 7-14. 0.1Hz to 10Hz Noise Distribution vs NR Capacitance

7.5.2 Broadband Noise

Broadband noise is a noise that appears at higher frequency compared to 1/f noise. The broadband noise is measured by high-pass filtering the output of the reference device, followed by a gain stage and measuring the result on a spectrum analyzer as shown in 図 7-15.

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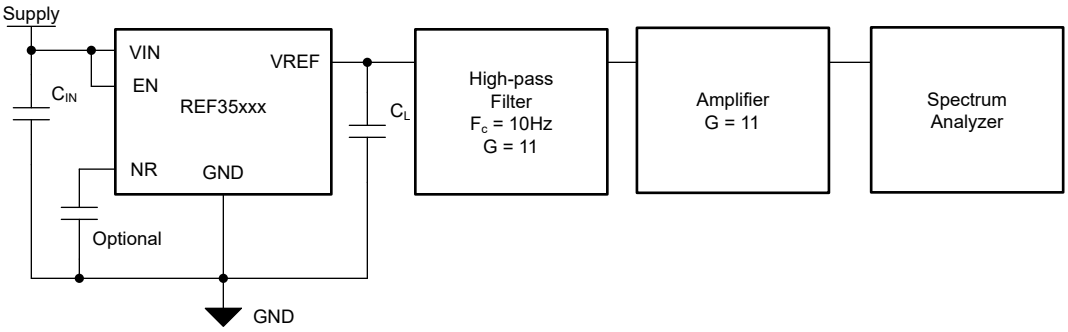


図 7-15. Broadband Noise Test Setup

For noise sensitive designs, a low-pass filter can be used to reduce broadband output noise. When designing a low-pass filter, take special care to make sure the output impedance of the filter does not degrade AC performance. This can occur in RC low-pass filters where a large series resistance can impact the load transients due to output current fluctuations. The REF35 device also offers noise reduction functionality by adding an optional capacitor between NR (pin 5) and ground pins. 図 7-16 and 図 7-17 show the noise spectrum for REF35250 and REF35500 devices respectively across various load capacitance.

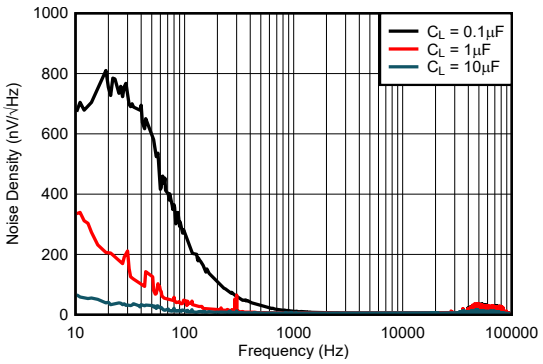


図 7-16. Noise Spectrum 10Hz to 100kHz (V_{REF} = 2.5V)

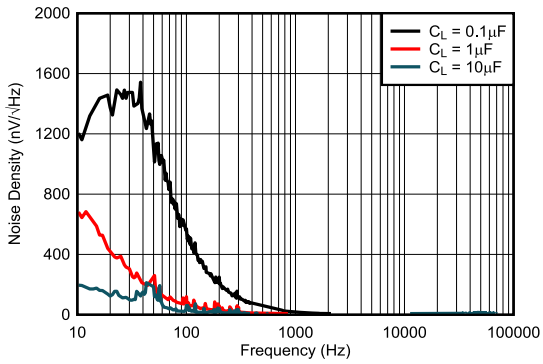


図 7-17. Noise Spectrum 10Hz to 100kHz (V_{REF} = 5V)

7.6 Power Dissipation

The REF35 voltage references are capable of source up to 10mA and sink up to 5mA of load current across the rated input voltage range. However, when used in applications subject to high ambient temperatures, the input voltage and load current must be carefully monitored to make sure that the device does not exceeded its maximum power dissipation rating. The maximum power dissipation of the device can be calculated with 式 3:

$$T_J = T_A + P_D \times R_{\theta JA} \quad (3)$$

where

- P_D is the device power dissipation
- T_J is the device junction temperature
- T_A is the ambient temperature
- $R_{\theta JA}$ is the package (junction-to-air) thermal resistance

Because of this relationship, acceptable load current in high temperature conditions can be less than the maximum current-sourcing capability of the device. In no case must the device be operated outside of its maximum power rating because doing so can result in premature failure or permanent damage to the device.

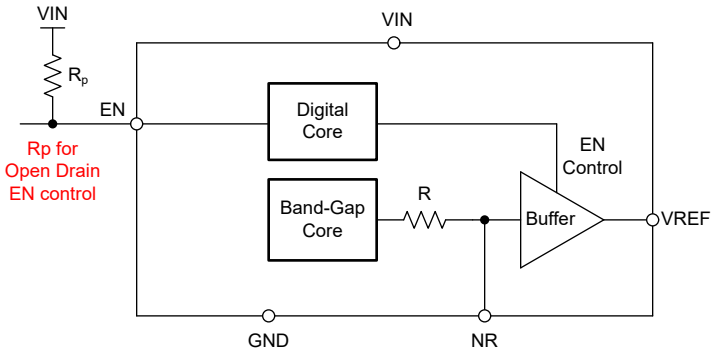
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8 Detailed Description

8.1 Overview

The REF35 is family of ultra-low current, low-noise, precision band-gap voltage references that are specifically designed for excellent initial voltage accuracy and drift. The *Functional Block Diagram* is a simplified block diagram of the REF35 showing basic band-gap topology.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Supply Voltage

The REF35 family of references features an extremely low dropout voltage. For 10mA loaded conditions, a maximum dropout voltage is 250mV. 図 6-34 shows a typical dropout voltage (V_{DO}) versus load current. The device supports operation with input voltage range from V_{REF} + V_{DO} to 6V. The typical quiescent current is 650nA and maximum quiescent current over temperature is only 2.6µA. The low dropout voltage coupled with ultra-low current enable the operation across multiple battery powered applications.

8.3.2 EN Pin

The REF35 family supports device enable and disable functionality through logic level control on EN pin. The EN pin of REF35 does not use an internal pull-up resistor. Instead, the pin uses new 'clean EN' technology. This allows the EN pin to be in a no connect condition at start-up, and no extra current is drawn from the supply when the EN pin is pulled low in shutdown mode. When EN pin is pulled high or left unconnected at start-up, the device is in active mode. When EN pin is driven by an open-drain output, a pull-up resistor to VIN is required. The device must be in active mode for normal operation. The EN pin must not be pulled higher than VIN supply voltage.

The device can be placed in shutdown mode by pulling the EN pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device drops to 100nA at room temperature. When changing the device state from shutdown to active state, make sure the EN pin is not left floating.

Also note that for applications where EN pin is no-connect, total parasitic capacitance on EN pin must be restricted within 30pF.

See the *Electrical Characteristics* table for logic high and logic low voltage levels.

8.3.3 NR Pin

The REF35 pin allows access to the band-gap through the NR pin. Placing a capacitor from the NR pin to GND creates a low-pass filter in combination with the internal resistance of 60 kΩ. Leakage of the capacitance directly impacts the accuracy and temperature drift. If NR functionality is used, choose a low leakage capacitor. A capacitance of 1µF creates a low-pass filter with corner frequency around 2.7Hz. Such a filter decreases the overall noise on the VREF pin. Higher capacitance results in a lower filter cut off frequency, further reducing output noise. Please note, using the capacitor on NR pin also increases start-up time.

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8.4 Device Functional Modes

8.4.1 Basic Connections

図 8-1 shows the typical connections for the REF35. TI recommends a supply bypass capacitor (C_{IN}) ranging from 0.1µF to 10µF. A 0.1µF to 10µF output capacitor (C_L) must be connected from REF to GND. The equivalent series resistance (ESR) value of C_L must be lower than 400mΩ to verify output stability.

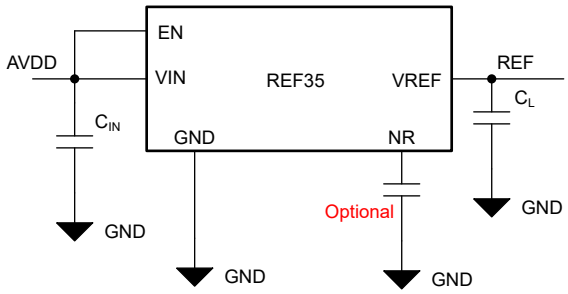


図 8-1. Basic Connections

8.4.2 Start-Up

図 8-2 shows the start-up behavior of REF35250 device with 1µF load capacitance. REF35 device verifies the output voltage settles to the expected output voltage within specified accuracy without oscillations. The start-up time is dependent on the output voltage variant, output capacitance and NR pin capacitance. Higher capacitance leads to longer start-up time.

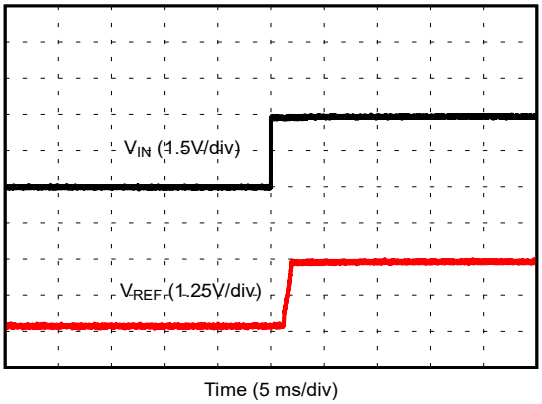


図 8-2. REF35250 Start-Up Behavior, C_L = 1µF

8.4.3 Output Transient Behavior

The REF35 output buffer is capable of sourcing 10mA load current as well as sink 5mA of load current. The output stage is designed using class AB architecture with ultra-low quiescent current. This architecture avoids the dead zone around the no load condition. The output buffer uses a fast start-up implementation to achieve 2ms typical turn-on time at C_L = 1µF and no-load current condition.

図 8-3 and 図 8-4show the output settling behavior for light load transient and high load transient respectively.

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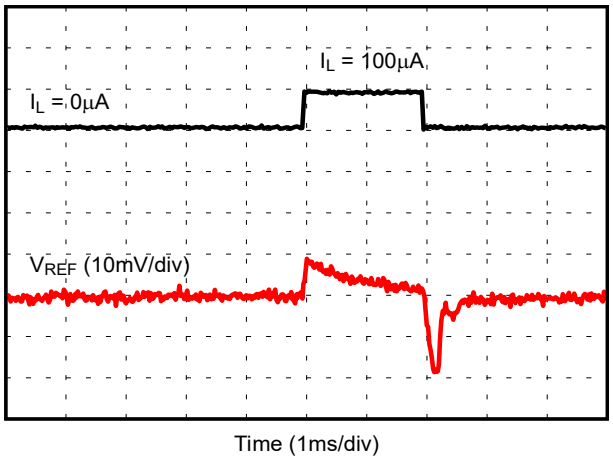


図 8-3. Load Transient Response 0µA to 100µA, C_L = 1µF

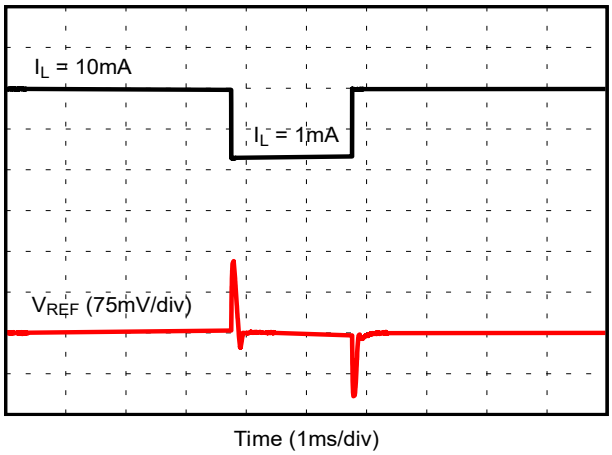


図 8-4. Load Transient Response 1mA to 10mA, C_L = 1µF

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

REF35 with low current consumption and class leading performance specifications is suitable reference for multiple applications. The device can also be used as a precision low noise power supply to sensor or data converter instead of traditional LDO or DC/DC based power supply. Basic applications includes positive/negative voltage reference and data acquisition systems. The table below shows the typical application of REF35 and its companion ADC/DAC.

表 9-1. Typical Applications and Companion ADC/DAC

APPLICATIONS	ADC/DAC
PLC - DCS	ADS7028, DAC8881, ADS1287, ADS7953
Rack Server	ADS7028, ADS7128, ADS7138
Field Transmitters - Pressure, Flow	ADS124S08
Optical Module, Optical Line Card	ADS7066, ADS7138
Power quality analyzer	ADC3662
Thermal imaging	ADC3541

9.2 Typical Applications

9.2.1 Negative Reference Voltage

For applications requiring a negative and positive reference voltage, the REF35 and OPA735 can be used to provide a dual-supply reference from a 5V supply. 図 9-1 shows the REF35250 used to provide a 2.5V supply reference voltage. The low drift performance of the REF35250 complements the low offset voltage and zero drift of the OPA735 to provide an accurate solution for split-supply applications. Take care to match the temperature coefficients of R1 and R2.

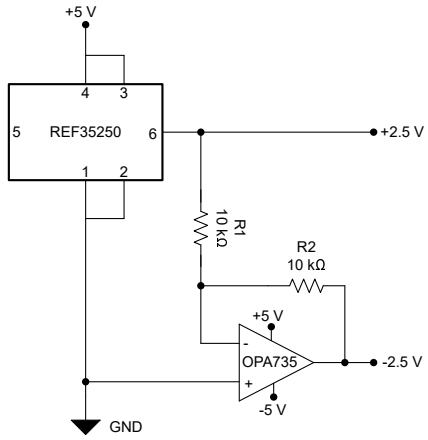


図 9-1. REF35 and OPA735 Create Positive and Negative Reference Voltages

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9.2.2 Precision Power Supply and Reference

図 9-2 shows the basic configuration for the REF35 device as precision power supply to ADS7038 data converter which uses its power supply AVDD as reference. Connect bypass capacitors according to the guidelines in the *Input and Output Capacitors* section.

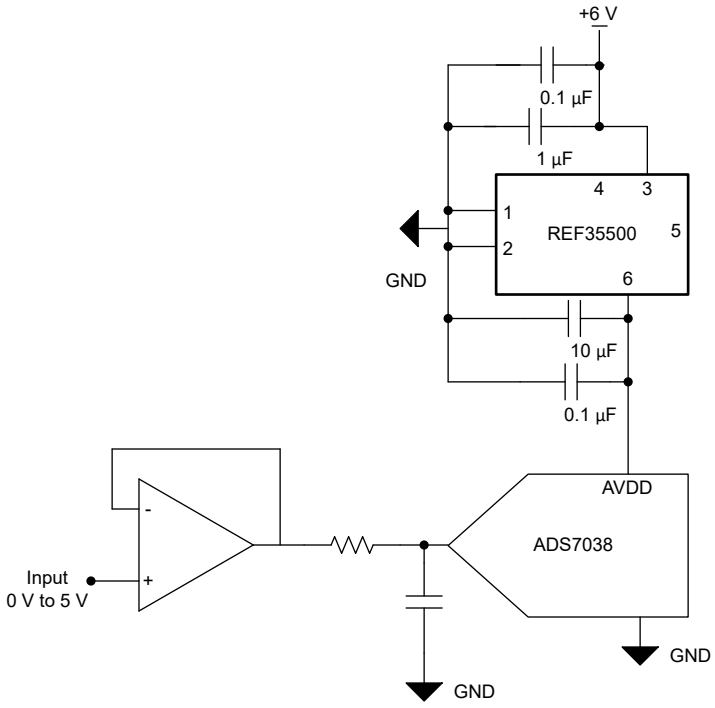


図 9-2. Basic Reference Connection

9.2.2.1 Design Requirements

A detailed design procedure is described based on a design example. For this design example, use the parameters listed in 表 9-2 as the input parameters.

表 9-2. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage range V_{IN}	0V - 5V
Output resolution	12-bit
REF35 input capacitor	1µF
REF35 output capacitor	10µF

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Selection of Reference

The REF35500 reference is selected for this design. The REF35500 device operates of very low quiescent current while offering ±0.05% initial accuracy and very low noise. These parameters help improve system accuracy as compared to external LDO based power supply. The 5V reference voltage supports the 0V to 5V input range specification.

9.2.2.2.2 Input and Output Capacitors

A 1µF to 10µF electrolytic or ceramic capacitor can be connected to the input to improve transient response in applications where the supply voltage may fluctuate.

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A ceramic capacitor of at least a 0.1µF must be connected to the output to improve stability and help filter out high frequency noise. Add an additional 10µF capacitor in parallel to improve transient performance in response to sudden changes in load current; however, keep in mind that doing so increases the start-up time of the device.

Best performance and stability is attained with low-ESR, low-inductance ceramic chip-type output capacitors (X5R, X7R, or similar). If using an electrolytic capacitor on the output, place a 0.1µF ceramic capacitor in parallel to reduce overall ESR on the output. Place the input and output capacitors as close as possible to the device.

9.2.2.2.3 Selection of ADC

ADS7038 12-bit 8 channel multiplexed ADC is chosen for this application. The ADC offers low current operation with averaging mode to increase the resolution to 16-bit with internal averaging modes while operating with slow sampling speed.

9.2.2.3 Application Curves

表 9-3 and 図 9-3 show the captured measurement results for various DC inputs. The ADC output is captured and analyzed for output accuracy error and code spread with REF35500 as power supply versus LDO as power supply.

REF35 offers better accuracy and lower noise than the LDO device at lower quiescent current. This results in lower error in measurement as well as lower ADC output code variation across various OSR settings.

表 9-3. DC Input Performance Test Results

INPUT V	ADC OSR SETTING	REF35500		LDO	
		ERROR	CODE SPREAD	ERROR	CODE SPREAD
1.0V	0	0.01mV	32 LSB	8.9mV	48 LSB
	8	0.3mV	10 LSB	9.21mV	16 LSB
	128	0.38mV	6 LSB	9.26mV	6 LSB
2.5V	0	0.69mV	32 LSB	22.89mV	64 LSB
	8	1.44mV	10 LSB	23.63mV	18 LSB
	128	1.17mV	3 LSB	23.41mV	5 LSB
4V	0	2.27mV	32 LSB	37.84mV	48 LSB
	8	3.01mV	24 LSB	38.62mV	24 LSB
	128	2.46mV	3 LSB	38.09mV	17 LSB

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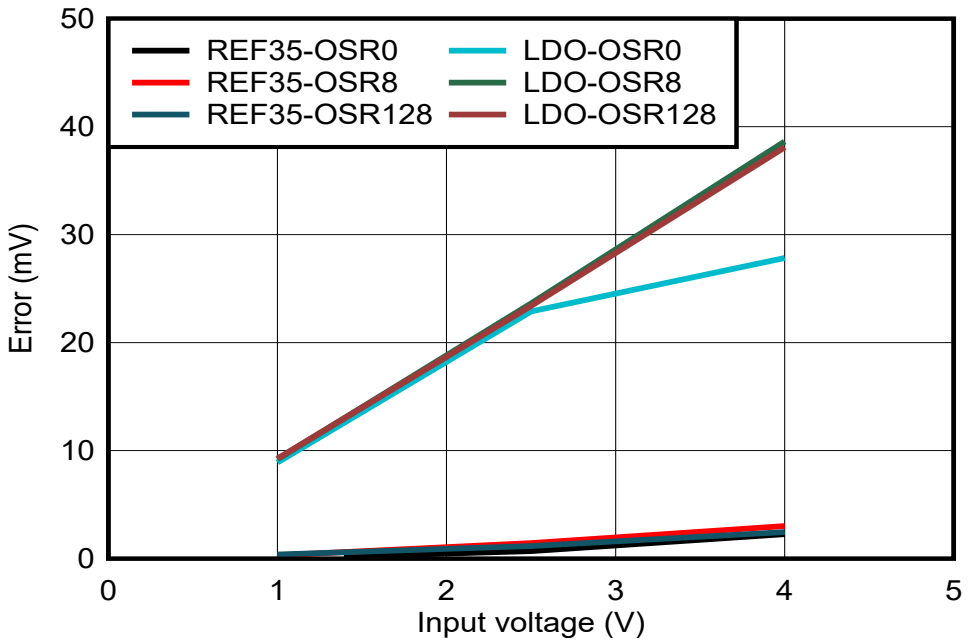


図 9-3. Error vs Input Voltage

9.3 Power Supply Recommendations

The REF35 family of references feature an extremely low-dropout voltage. These references can be operated with a supply of only 50mV above the output voltage at no load. TI recommends a supply bypass capacitor ranging between 0.1µF to 10µF.

9.4 Layout

9.4.1 Layout Guidelines

図 9-4 shows an example of a PCB layout for a data acquisition system using the REF35. Some key considerations are:

- Connect low-ESR, 0.1µF ceramic bypass capacitors at V_{IN}, V_{REF} of the REF35.
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

図 9-5 shows the pin compatibility with TI REF30xx, REF31xx and REF33xx series references in the 3-pin SOT-23 package when using the REF35xxx family footprint. You must rotate the REF30xx, REF31xx and REF33xx reference devices by 180º before assembly.

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9.4.2 Layout Examples

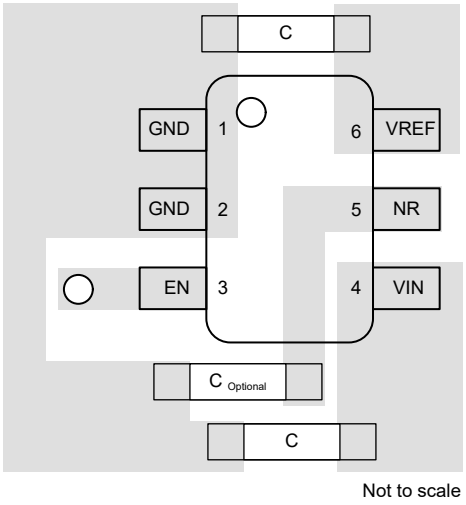


図 9-4. Layout Example - DBV package

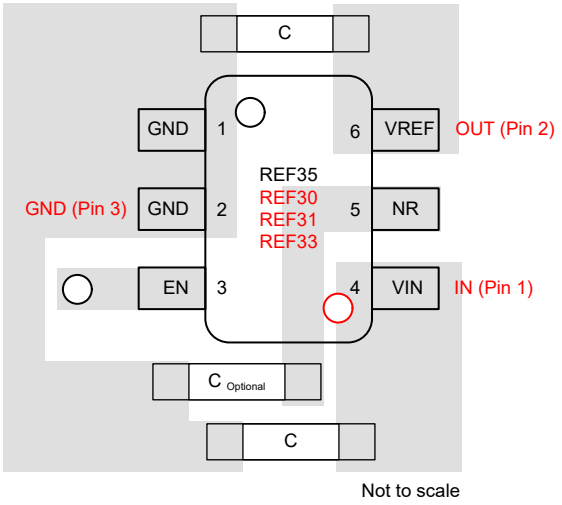


図 9-5. Pin Compatibility With REF30xx, REF31xx and REF33xx

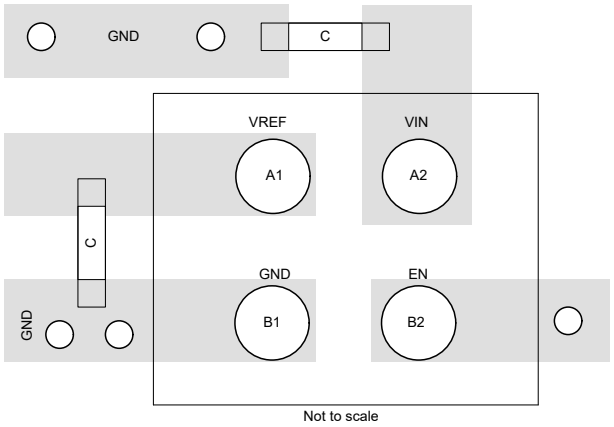


図 9-6. Layout Example - YBH package

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors* data sheet
- Texas Instruments, *Low-Drift Bidirectional Single-Supply Low-Side Current Sensing Reference Design*
- Texas Instruments, *Precision voltage references* Analog Design Journal

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (April 2024) to Revision C (September 2024)	Page
• Updated YBH Package dimensions	30

Changes from Revision A (August 2022) to Revision B (April 2024)	Page
• WCSP パッケージの特長の説明を追加。	1
• WCSP パッケージの製品プレビュー ステータスを削除。	1
• Added REF35170QBVR & REF35360QDBVR devices as released variant. Updated the WCSP device release options.	3
• Added more details to device pin external connections.	3

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- Added YBH package performance details.....6
- Added typical characteristics for WCSP package..... 8

Changes from Revision * (December 2021) to Revision A (August 2022) **Page**

- 量産データのリリース.....1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

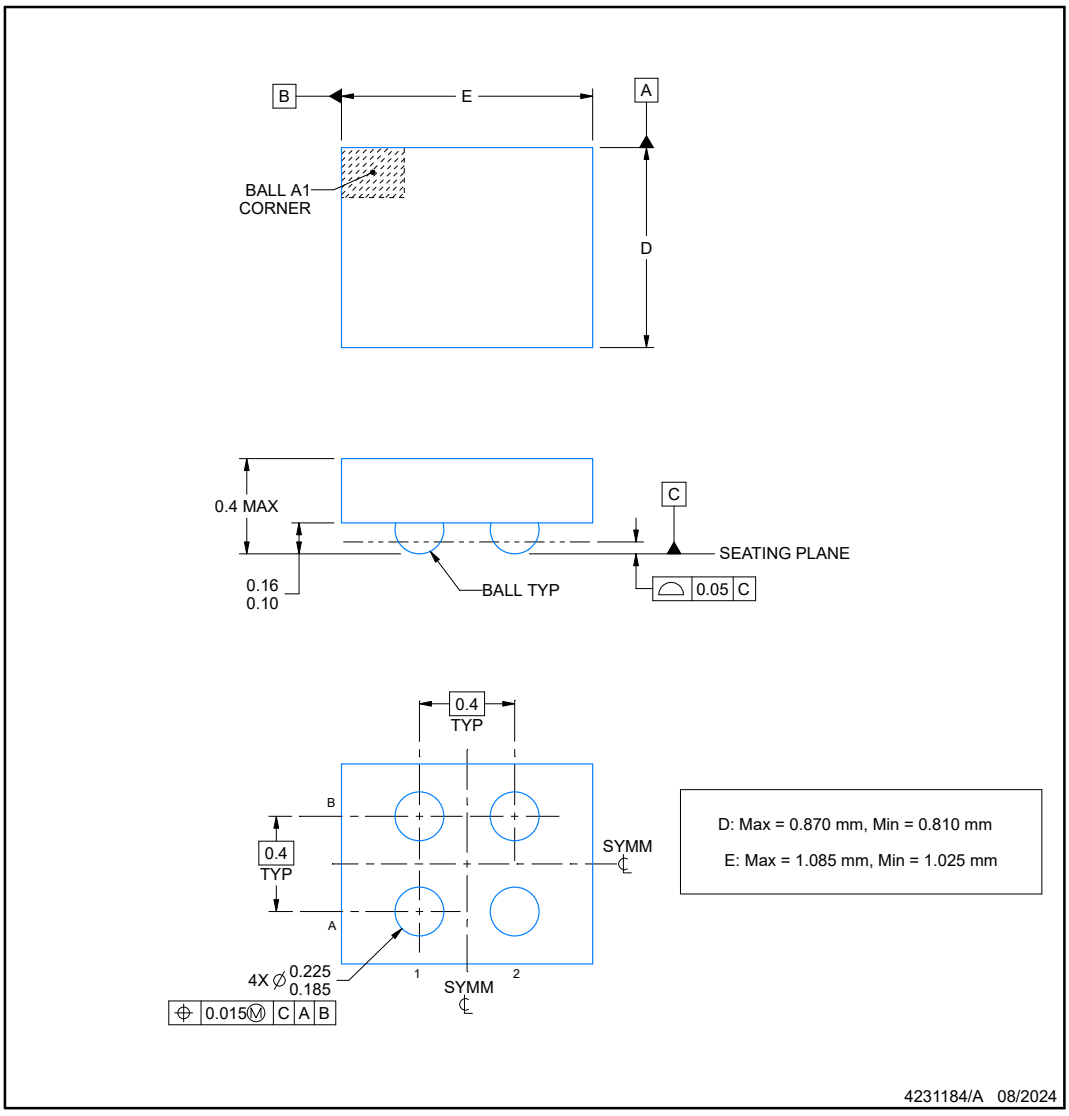
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PACKAGE OUTLINE

YBH0004-C01

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

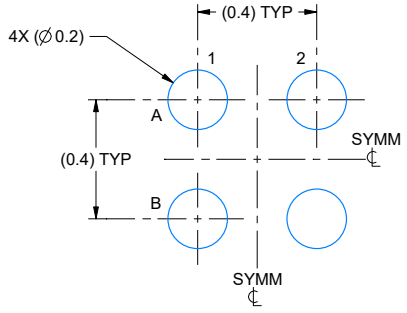
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EXAMPLE BOARD LAYOUT

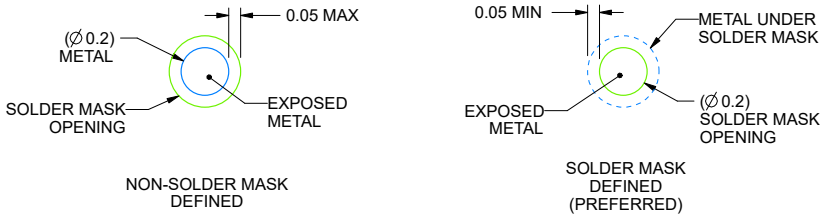
YBH0004-C01

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4231184/A 08/2024

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

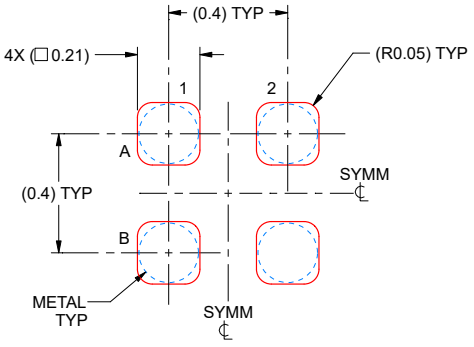
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EXAMPLE STENCIL DESIGN

YBH0004-C01

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4231184/A 08/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF35102QDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2RTI
REF35102QDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2RTI
REF35102YBHR	Active	Production	DSBGA (YBH) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	M
REF35102YBHR.A	Active	Production	DSBGA (YBH) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	M
REF35120QDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2RVI
REF35120QDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2RVI
REF35120YBHR	Active	Production	DSBGA (YBH) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	A
REF35120YBHR.A	Active	Production	DSBGA (YBH) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	A
REF35125QDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2RUI
REF35125QDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2RUI
REF35125YBHR	Active	Production	DSBGA (YBH) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	L
REF35125YBHR.A	Active	Production	DSBGA (YBH) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	L
REF35160QDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2UII
REF35160QDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2UII
REF35160YBHR	Active	Production	DSBGA (YBH) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C
REF35160YBHR.A	Active	Production	DSBGA (YBH) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C
REF35170QDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	31QI
REF35170QDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	31QI
REF35180QDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2J2I
REF35180QDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2J2I
REF35180YBHR	Active	Production	DSBGA (YBH) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
REF35180YBHR.A	Active	Production	DSBGA (YBH) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
REF35205QDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2UKI
REF35205QDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2UKI
REF35250QDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2RSI
REF35250QDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2RSI
REF35250YBHR	Active	Production	DSBGA (YBH) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B
REF35250YBHR.A	Active	Production	DSBGA (YBH) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B
REF35300QDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2SLI

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF35300QDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2SLI
REF35300YBHR	Active	Production	DSBGA (YBH) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S
REF35300YBHR.A	Active	Production	DSBGA (YBH) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S
REF35330QDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2ULI
REF35330QDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2ULI
REF35360QDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	31RI
REF35360QDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	31RI
REF35409QDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2UMI
REF35409QDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2UMI
REF35409YBHR	Active	Production	DSBGA (YBH) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T
REF35409YBHR.A	Active	Production	DSBGA (YBH) | 4	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T
REF35500QDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2RWI
REF35500QDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2RWI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF REF35 :

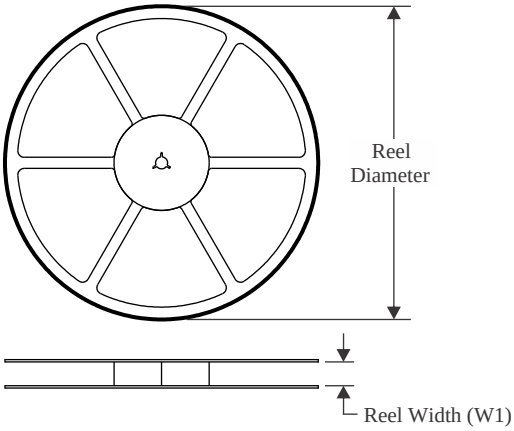
- Automotive : REF35-Q1

NOTE: Qualified Version Definitions:

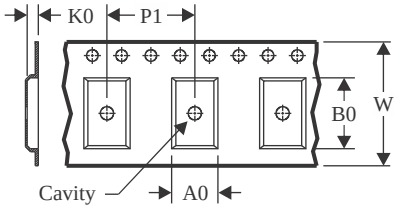
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

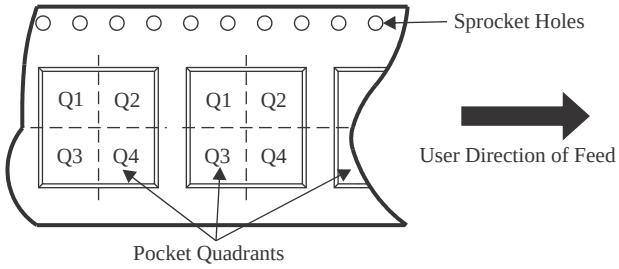


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

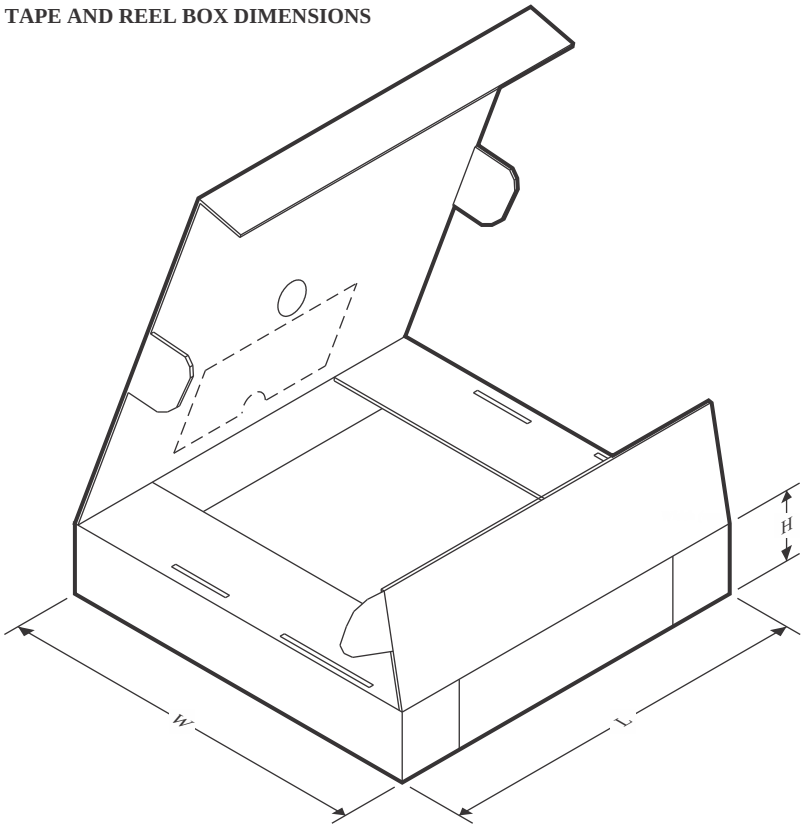


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF35102QDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF35102YBHR	DSBGA	YBH	4	12000	180.0	8.4	0.94	1.17	0.45	2.0	8.0	Q2
REF35120QDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF35120YBHR	DSBGA	YBH	4	12000	180.0	8.4	0.94	1.17	0.45	2.0	8.0	Q2
REF35125QDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF35125YBHR	DSBGA	YBH	4	12000	180.0	8.4	0.94	1.17	0.45	2.0	8.0	Q2
REF35160QDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF35160YBHR	DSBGA	YBH	4	12000	180.0	8.4	0.94	1.17	0.45	2.0	8.0	Q2
REF35170QDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF35180QDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF35180YBHR	DSBGA	YBH	4	12000	180.0	8.4	0.94	1.17	0.45	2.0	8.0	Q2
REF35205QDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF35250QDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF35250YBHR	DSBGA	YBH	4	12000	180.0	8.4	0.94	1.17	0.45	2.0	8.0	Q2
REF35300QDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF35300YBHR	DSBGA	YBH	4	12000	180.0	8.4	0.94	1.17	0.45	2.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF35330QDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF35360QDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF35409QDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF35409YBHR	DSBGA	YBH	4	12000	180.0	8.4	0.94	1.17	0.45	2.0	8.0	Q2
REF35500QDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF35102QDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF35102YBHR	DSBGA	YBH	4	12000	182.0	182.0	20.0
REF35120QDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF35120YBHR	DSBGA	YBH	4	12000	182.0	182.0	20.0
REF35125QDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF35125YBHR	DSBGA	YBH	4	12000	182.0	182.0	20.0
REF35160QDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF35160YBHR	DSBGA	YBH	4	12000	182.0	182.0	20.0
REF35170QDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF35180QDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF35180YBHR	DSBGA	YBH	4	12000	182.0	182.0	20.0
REF35205QDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF35250QDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF35250YBHR	DSBGA	YBH	4	12000	182.0	182.0	20.0
REF35300QDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF35300YBHR	DSBGA	YBH	4	12000	182.0	182.0	20.0
REF35330QDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF35360QDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0

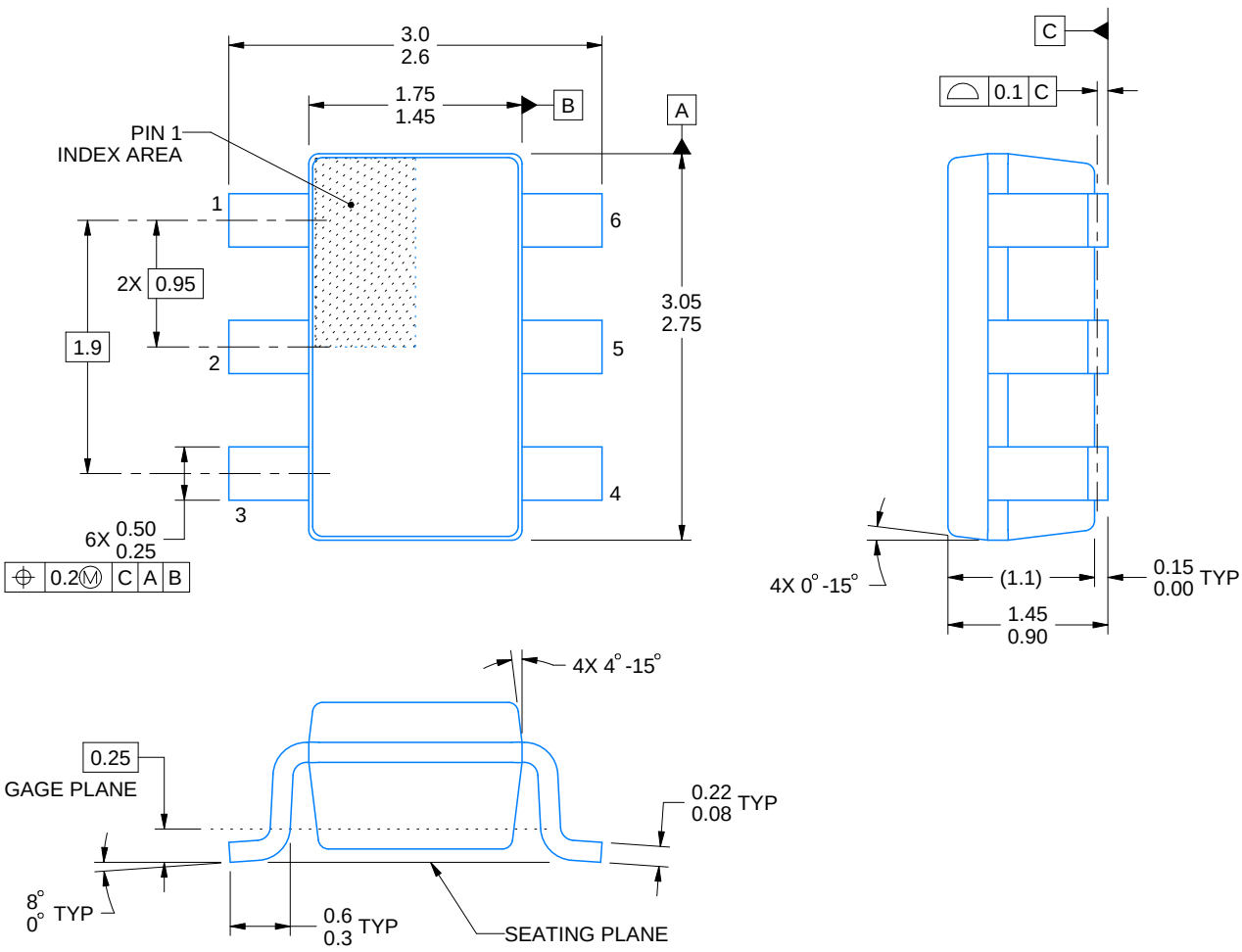
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF35409QDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0
REF35409YBHR	DSBGA	YBH	4	12000	182.0	182.0	20.0
REF35500QDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

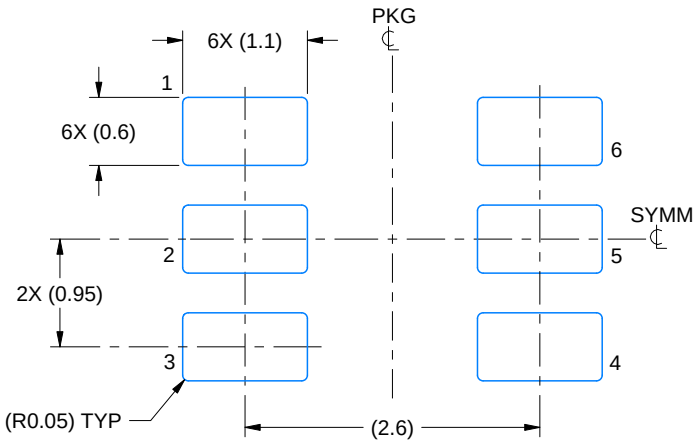
SMALL OUTLINE TRANSISTOR



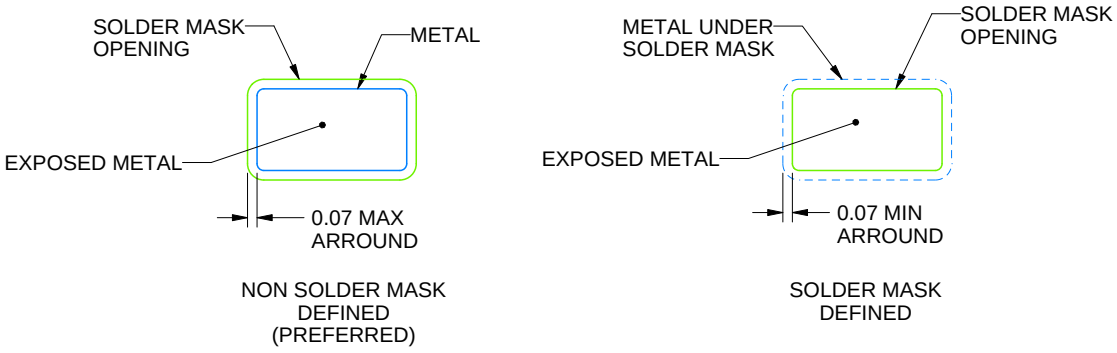
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

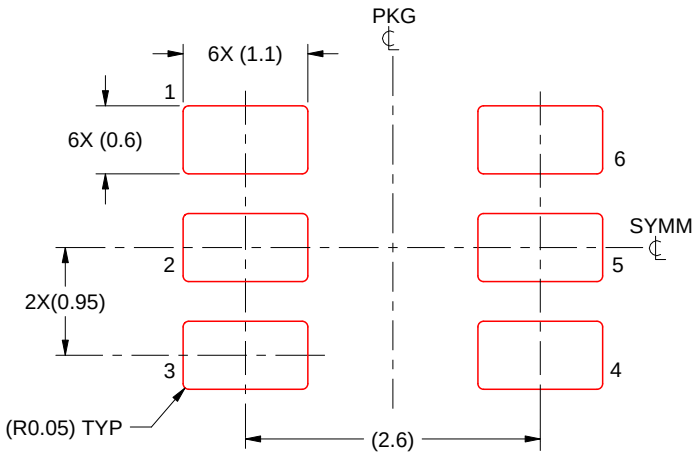


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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