


**SN54ACT374, SN74ACT374**

JAJSR17H – OCTOBER 1995 – REVISED MARCH 2024

# SNx4ACT374 3 ステート出力、オクタール D タイプ・エッジ・トリガ・フリップ・フロップ

## 1 特長

- 4.5V~5.5V の  $V_{CC}$  で動作
- 5.5V までの入力電圧に対応
- 最大  $t_{pd}$  10ns (5V 時)
- 入力は TTL 電圧互換

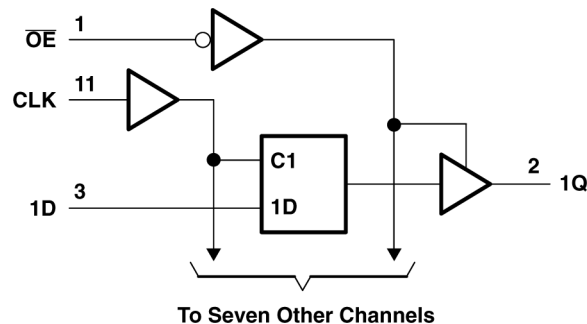
## 2 概要

これらの 8 ビット フリップ フロップ は、大きい容量性負荷または比較的 low インピーダンス負荷の駆動用に特化して設計された 3 ステート出力を備えています。本デバイスは、バッファレジスタ、I/O ポート、双方向バスドライバ、作業レジスタの実装に特に適しています。

### 製品情報

| 部品番号       | パッケージ (1)      | パッケージサイズ (2)     | 本体サイズ (3)        |
|------------|----------------|------------------|------------------|
| SNx4ACT374 | DB (SSOP, 20)  | 7.2mm × 7.8mm    | 7.20mm × 5.30mm  |
|            | DW (SOIC, 20)  | 12.80mm × 10.3mm | 12.80mm × 7.50mm |
|            | N (PDIP, 20)   | 24.33mm × 9.4mm  | 24.33mm × 6.35mm |
|            | NS (SO, 20)    | 12.6mm × 7.8mm   | 12.60mm × 5.30mm |
|            | PW (TSSOP, 20) | 6.50mm × 6.4mm   | 6.50mm × 4.40mm  |

- (1) 詳細については、[セクション 10](#) を参照してください。
- (2) パッケージサイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。
- (3) 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。



## Table of Contents

|                                                  |          |                                                                  |           |
|--------------------------------------------------|----------|------------------------------------------------------------------|-----------|
| <b>1 特長</b> .....                                | <b>1</b> | 6.3 Device Functional Modes.....                                 | <b>8</b>  |
| <b>2 概要</b> .....                                | <b>1</b> | <b>7 Application and Implementation</b> .....                    | <b>9</b>  |
| <b>3 Pin Configuration and Functions</b> .....   | <b>3</b> | 7.1 Power Supply Recommendations.....                            | <b>9</b>  |
| <b>4 Specifications</b> .....                    | <b>4</b> | 7.2 Layout.....                                                  | <b>9</b>  |
| 4.1 Absolute Maximum Ratings.....                | <b>4</b> | <b>8 Device and Documentation Support</b> .....                  | <b>10</b> |
| 4.2 Recommended Operating Conditions.....        | <b>4</b> | 8.1 Documentation Support (Analog).....                          | <b>10</b> |
| 4.3 Thermal Information.....                     | <b>5</b> | 8.2 ドキュメントの更新通知を受け取る方法.....                                      | <b>10</b> |
| 4.4 Electrical Characteristics.....              | <b>5</b> | 8.3 サポート・リソース.....                                               | <b>10</b> |
| 4.5 Timing Requirements.....                     | <b>6</b> | 8.4 Trademarks.....                                              | <b>10</b> |
| 4.6 Switching Characteristics.....               | <b>6</b> | 8.5 静電気放電に関する注意事項.....                                           | <b>10</b> |
| 4.7 Operating Characteristics.....               | <b>6</b> | 8.6 用語集.....                                                     | <b>10</b> |
| <b>5 Parameter Measurement Information</b> ..... | <b>7</b> | <b>9 Revision History</b> .....                                  | <b>10</b> |
| <b>6 Detailed Description</b> .....              | <b>8</b> | <b>10 Mechanical, Packaging, and Orderable Information</b> ..... | <b>11</b> |
| 6.1 Overview.....                                | <b>8</b> |                                                                  |           |
| 6.2 Functional Block Diagram.....                | <b>8</b> |                                                                  |           |

### 3 Pin Configuration and Functions

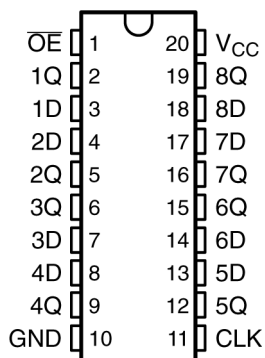


図 3-1. SN54ACT374 J or W Package; SN74ACT374 DB, DW, N, NS, or PW Package; (Top View)

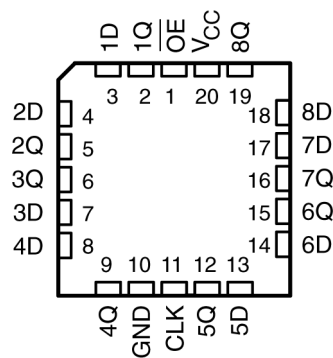


図 3-2. SN54ACT374 FK Package (Top View)

表 3-1. Pin Functions

| PIN             |     | TYPE | DESCRIPTION |
|-----------------|-----|------|-------------|
| NAME            | NO. |      |             |
| OE              | 1   | I    | Enable pin  |
| 1Q              | 2   | O    | Output 1    |
| 1D              | 3   | I    | Input 1     |
| 2D              | 4   | I    | Input 2     |
| 2Q              | 5   | O    | Output 2    |
| 3Q              | 6   | O    | Output 3    |
| 3D              | 7   | I    | Input 3     |
| 4D              | 8   | I    | Input 4     |
| 4Q              | 9   | O    | Output 4    |
| GND             | 10  | –    | Ground pin  |
| CLK             | 11  | I    | Clock pin   |
| 5Q              | 12  | O    | Output 5    |
| 5D              | 13  | I    | Input 5     |
| 6D              | 14  | I    | Input 6     |
| 6Q              | 15  | O    | Output 6    |
| 7Q              | 16  | O    | Output 7    |
| 7D              | 17  | I    | Input 7     |
| 8D              | 18  | I    | Input 8     |
| 8Q              | 19  | O    | Output 8    |
| V <sub>CC</sub> | 20  | –    | Power pin   |

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>1</sup>

|                    |                                            | MIN                                  | MAX            | UNIT    |
|--------------------|--------------------------------------------|--------------------------------------|----------------|---------|
| $V_{CC}$           | Supply voltage range                       | -0.5                                 | 7              | V       |
| $V_I$ <sup>1</sup> | Input voltage range                        | -0.5                                 | $V_{CC} + 0.5$ | V       |
| $V_O$ <sup>1</sup> | Output voltage range                       | -0.5                                 | $V_{CC} + 0.5$ | V       |
| $I_{IK}$           | Input clamp current                        | $(V_I < 0 \text{ or } V_I > V_{CC})$ |                | ±20 mA  |
| $I_{OK}$           | Output clamp current                       | $(V_O < 0 \text{ or } V_O > V_{CC})$ |                | ±20 mA  |
| $I_O$              | Continuous output current                  | $(V_O = 0 \text{ to } V_{CC})$       |                | ±50 mA  |
|                    | Continuous current through $V_{CC}$ or GND |                                      |                | ±200 mA |
| $T_{stg}$          | Storage temperature range                  | -65                                  | 150            | °C      |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 4.2 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)<sup>1</sup>

|                     |                                    | SN54ACT374 |          | SN74ACT374 |          | UNIT |
|---------------------|------------------------------------|------------|----------|------------|----------|------|
|                     |                                    | MIN        | MAX      | MIN        | MAX      |      |
| $V_{CC}$            | Supply voltage                     | 4.5        | 5.5      | 4.5        | 5.5      | V    |
| $V_{IH}$            | High-level input voltage           | 2          |          | 2          |          | V    |
| $V_{IL}$            | Low-level input voltage            |            | 0.8      |            | 0.8      | V    |
| $V_I$               | Input voltage                      | 0          | $V_{CC}$ | 0          | $V_{CC}$ | V    |
| $V_O$               | Output voltage                     | 0          | $V_{CC}$ | 0          | $V_{CC}$ | V    |
| $I_{OH}$            | High-level output current          |            | -24      |            | -24      | mA   |
| $I_{OL}$            | Low-level output current           |            | 24       |            | 24       | mA   |
| $\Delta t/\Delta v$ | Input transition rise or fall rate |            | 8        |            | 8        | ns/V |
| $T_A$               | Operating free-air temperature     | -55        | 125      | -40        | 85       | °C   |

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 4.3 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                        | SNx4ACT374 |           |         |         |            | UNIT |
|-------------------------------|----------------------------------------|------------|-----------|---------|---------|------------|------|
|                               |                                        | DB (SSOP)  | DW (SOIC) | N       | NS (SO) | PW (TSSOP) |      |
|                               |                                        | 20 PINS    | 20 PINS   | 20 PINS | 20 PINS | 20 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance | 70         | 58        | 69      | 106.2   | 126.2      | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                       | TEST CONDITIONS                                             | V <sub>CC</sub> | T <sub>A</sub> = 25°C |      |       | SN54ACT374 |      | SN74ACT374 |      | UNIT |
|---------------------------------|-------------------------------------------------------------|-----------------|-----------------------|------|-------|------------|------|------------|------|------|
|                                 |                                                             |                 | MIN                   | TYP  | MAX   | MIN        | MAX  | MIN        | MAX  |      |
| V <sub>OH</sub>                 | I <sub>OH</sub> = -50 μA                                    | 4.5 V           | 4.4                   | 4.49 |       | 4.4        |      | 4.4        |      | V    |
|                                 |                                                             | 5.5 V           | 5.4                   | 5.49 |       | 5.4        |      | 5.4        |      |      |
|                                 | I <sub>OH</sub> = -24 mA                                    | 4.5 V           | 3.86                  |      |       | 3.7        |      | 3.76       |      |      |
|                                 |                                                             | 5.5 V           | 4.86                  |      |       | 4.7        |      | 4.76       |      |      |
|                                 | I <sub>OH</sub> = -50 mA <sup>(1)</sup>                     | 5.5 V           |                       |      |       | 3.85       |      |            |      |      |
|                                 | I <sub>OH</sub> = -75 mA <sup>(1)</sup>                     | 5.5 V           |                       |      |       |            |      | 3.85       |      |      |
| V <sub>OL</sub>                 | I <sub>OL</sub> = 50 μA                                     | 4.5 V           |                       |      | 0.1   |            | 0.1  |            | 0.1  | V    |
|                                 |                                                             | 5.5 V           |                       |      | 0.1   |            | 0.1  |            | 0.1  |      |
|                                 | I <sub>OL</sub> = 24 mA                                     | 4.5 V           |                       |      | 0.36  |            | 0.44 |            | 0.44 |      |
|                                 |                                                             | 5.5 V           |                       |      | 0.36  |            | 0.5  |            | 0.44 |      |
|                                 | I <sub>OL</sub> = 50 mA <sup>(1)</sup>                      | 5.5 V           |                       |      |       |            | 1.65 |            |      |      |
|                                 | I <sub>OL</sub> = 75 mA <sup>(1)</sup>                      | 5.5 V           |                       |      |       |            |      |            | 1.65 |      |
| I <sub>OZ</sub>                 | V <sub>O</sub> = V <sub>CC</sub> or GND                     | 5.5 V           |                       |      | ±0.25 |            | ±5   |            | ±2.5 | μA   |
| I <sub>I</sub>                  | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 5.5 V           |                       |      | ±0.1  |            | ±1   |            | ±1   | μA   |
| I <sub>CC</sub>                 | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5 V           |                       |      | 4     |            | 80   |            | 40   | μA   |
| ΔI <sub>CC</sub> <sup>(2)</sup> | One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>  | 5.5 V           |                       | 0.6  |       |            | 1.6  |            | 1.5  | mA   |
| C <sub>i</sub>                  | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 5 V             |                       | 4.5  |       |            |      |            |      | pF   |

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## 4.5 Timing Requirements

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

|                    |                                        | $T_A = 25^\circ\text{C}$ |     | SN54ACT374 |     | SN74ACT374 |     | UNIT |
|--------------------|----------------------------------------|--------------------------|-----|------------|-----|------------|-----|------|
|                    |                                        | MIN                      | MAX | MIN        | MAX | MIN        | MAX |      |
| $f_{\text{clock}}$ | Clock frequency                        |                          | 100 |            | 70  |            | 90  | MHz  |
| $t_w$              | Pulse duration, CLK high or low        | 5                        |     | 5          |     | 5          |     | ns   |
| $t_{\text{su}}$    | Setup time, data before CLK $\uparrow$ | 5                        |     | 5.5        |     | 5.5        |     | ns   |
| $t_h$              | Hold time, data after CLK $\uparrow$   | 1.5                      |     | 1.5        |     | 1.5        |     | ns   |

## 4.6 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

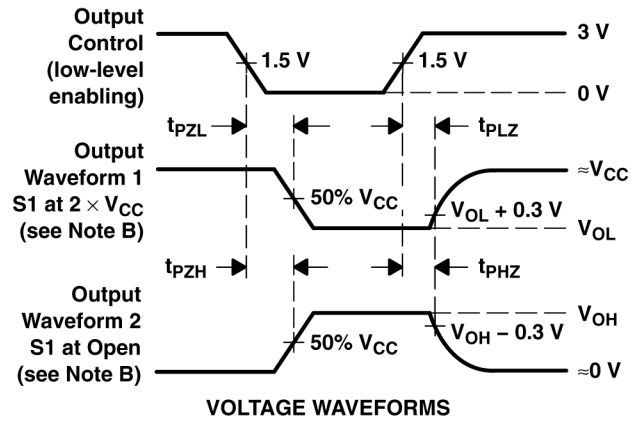
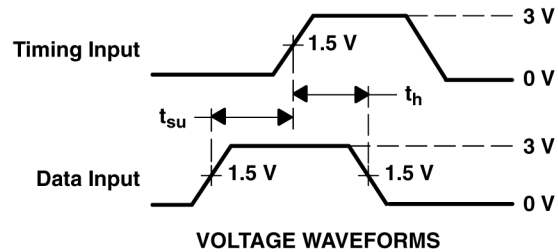
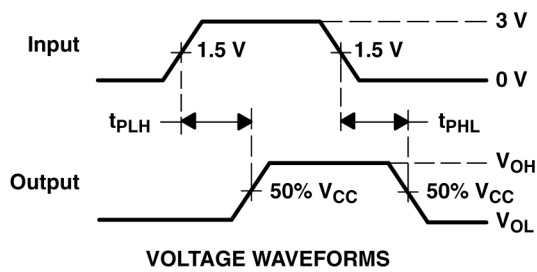
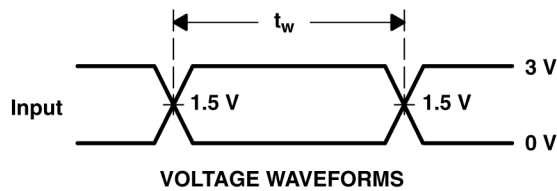
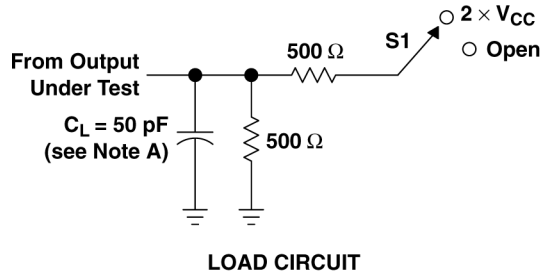
| PARAMETER        | FROM (INPUT)           | TO (OUTPUT) | $T_A = 25^\circ\text{C}$ |     |      | SN54ACT374 |      | SN74ACT374 |      | UNIT |
|------------------|------------------------|-------------|--------------------------|-----|------|------------|------|------------|------|------|
|                  |                        |             | MIN                      | TYP | MAX  | MIN        | MAX  | MIN        | MAX  |      |
| $f_{\text{max}}$ |                        |             | 100                      | 160 |      | 70         |      | 90         |      | MHz  |
| $t_{\text{PLH}}$ | CLK                    | Q           | 2                        | 8.5 | 10   | 1.5        | 12   | 2          | 11.5 | ns   |
| $t_{\text{PHL}}$ |                        |             | 2                        | 8   | 9.5  | 1.5        | 11.5 | 1.5        | 11   |      |
| $t_{\text{PZH}}$ | $\overline{\text{OE}}$ | Q           | 2                        | 8   | 9.5  | 1.5        | 11.5 | 1.5        | 10.5 | ns   |
| $t_{\text{PZL}}$ |                        |             | 1.5                      | 8   | 9    | 1.5        | 11.5 | 1.5        | 10.5 |      |
| $t_{\text{PHZ}}$ | $\overline{\text{OE}}$ | Q           | 1.5                      | 8.5 | 11.5 | 1.5        | 13   | 1          | 12.5 | ns   |
| $t_{\text{PLZ}}$ |                        |             | 1.5                      | 7   | 8.5  | 1.5        | 11   | 1          | 10   |      |

## 4.7 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER       |                               | TEST CONDITIONS        |                    | TYP | UNIT |
|-----------------|-------------------------------|------------------------|--------------------|-----|------|
| $C_{\text{pd}}$ | Power dissipation capacitance | $C_L = 50\text{ pF}$ , | $f = 1\text{ MHz}$ | 40  | pF   |

## 5 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.

### 5-1. Load Circuit and Voltage Waveforms

| TEST              | S1                |
|-------------------|-------------------|
| $t_{PLH}/t_{PHL}$ | Open              |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | Open              |

## 6 Detailed Description

### 6.1 Overview

The eight flip-flops of the 'ACT374 devices are D-type edge-triggered flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines in bus-organized systems without need for interface or pullup components.

$\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

For specified high-impedance state during power up or power down,  $\overline{OE}$  must be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 6.2 Functional Block Diagram

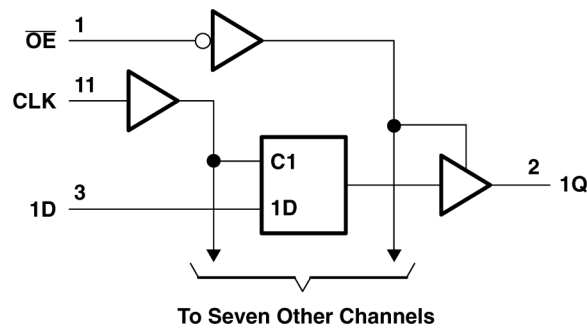


图 6-1. Logic Diagram (Positive Logic)

### 6.3 Device Functional Modes

表 6-1. Function Table (Each Flip-Flop)

| INPUTS |        |   | OUTPUT Q |
|--------|--------|---|----------|
| OE     | CLK    | D |          |
| L      | ↑      | H | H        |
| L      | ↑      | L | L        |
| L      | H or L | X | $Q_0$    |
| H      | X      | X | Z        |

## 7 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 7.1 Power Supply Recommendations

### 7.2 Layout

#### 7.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

#### 7.2.2 Layout Example

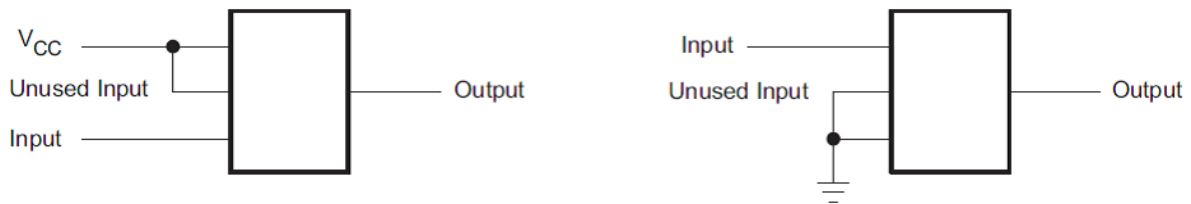


図 7-1. Layout Example

## 8 Device and Documentation Support

### 8.1 Documentation Support (Analog)

#### 8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

| PARTS      | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54ACT374 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| SN74ACT374 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

### 8.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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### 8.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 8.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 8.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision G (August 2023) to Revision H (March 2024)                    | Page              |
|-------------------------------------------------------------------------------------|-------------------|
| • 製品情報の表にパッケージ サイズを追加.....                                                          | <a href="#">1</a> |
| • Updated RθJA values: NS = 60 to 106.2, PW = 83 to 126.2, all values in °C/W ..... | <a href="#">5</a> |
| • Added <i>Application and Implementation</i> section.....                          | <a href="#">9</a> |

**Changes from Revision F (November 2002) to Revision G (August 2023)**
**Page**

- 「製品情報」表、「ピンの機能」表、「熱に関する情報」表、「デバイスの機能モード」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ..... **1**

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                     |
|---------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-----------------------------------------|
| <a href="#">5962-87631012A</a>  | Active        | Production           | LCCC (FK)   20  | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>87631012A<br>SNJ54ACT<br>374FK |
| <a href="#">5962-8763101RA</a>  | Active        | Production           | CDIP (J)   20   | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8763101RA<br>SNJ54ACT374J          |
| <a href="#">5962-8763101SA</a>  | Active        | Production           | CFP (W)   20    | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8763101SA<br>SNJ54ACT374W          |
| <a href="#">5962-8763101VSA</a> | Active        | Production           | CFP (W)   20    | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8763101VS<br>A<br>SNV54ACT374W     |
| 5962-8763101VSA.A               | Active        | Production           | CFP (W)   20    | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8763101VS<br>A<br>SNV54ACT374W     |
| <a href="#">SN74ACT374DBR</a>   | Active        | Production           | SSOP (DB)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AD374                                   |
| SN74ACT374DBR.A                 | Active        | Production           | SSOP (DB)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AD374                                   |
| <a href="#">SN74ACT374DW</a>    | Obsolete      | Production           | SOIC (DW)   20  | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | ACT374                                  |
| <a href="#">SN74ACT374DWR</a>   | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ACT374                                  |
| SN74ACT374DWR.A                 | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ACT374                                  |
| <a href="#">SN74ACT374N</a>     | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74ACT374N                             |
| SN74ACT374N.A                   | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74ACT374N                             |
| <a href="#">SN74ACT374NSR</a>   | Active        | Production           | SOP (NS)   20   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ACT374                                  |
| SN74ACT374NSR.A                 | Active        | Production           | SOP (NS)   20   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ACT374                                  |
| <a href="#">SN74ACT374PW</a>    | Obsolete      | Production           | TSSOP (PW)   20 | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | AD374                                   |
| <a href="#">SN74ACT374PWR</a>   | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AD374                                   |
| SN74ACT374PWR.A                 | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AD374                                   |
| <a href="#">SNJ54ACT374FK</a>   | Active        | Production           | LCCC (FK)   20  | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>87631012A<br>SNJ54ACT<br>374FK |

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                 |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------------|
| SNJ54ACT374FK.A              | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-87631012A<br>SNJ54ACT<br>374FK |
| <a href="#">SNJ54ACT374J</a> | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8763101RA<br>SNJ54ACT374J      |
| SNJ54ACT374J.A               | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8763101RA<br>SNJ54ACT374J      |
| <a href="#">SNJ54ACT374W</a> | Active        | Production           | CFP (W)   20   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8763101SA<br>SNJ54ACT374W      |
| SNJ54ACT374W.A               | Active        | Production           | CFP (W)   20   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8763101SA<br>SNJ54ACT374W      |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54ACT374, SN54ACT374-SP, SN74ACT374 :**

- Catalog : [SN74ACT374](#), [SN54ACT374](#)

- Military : [SN54ACT374](#)

- Space : [SN54ACT374-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ACT374DBR | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74ACT374DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74ACT374NSR | SOP          | NS              | 20   | 2000 | 330.0              | 24.4               | 8.4     | 13.0    | 2.5     | 12.0    | 24.0   | Q1            |
| SN74ACT374PWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ACT374DBR | SSOP         | DB              | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74ACT374DWR | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| SN74ACT374NSR | SOP          | NS              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| SN74ACT374PWR | TSSOP        | PW              | 20   | 2000 | 353.0       | 353.0      | 32.0        |

## TUBE

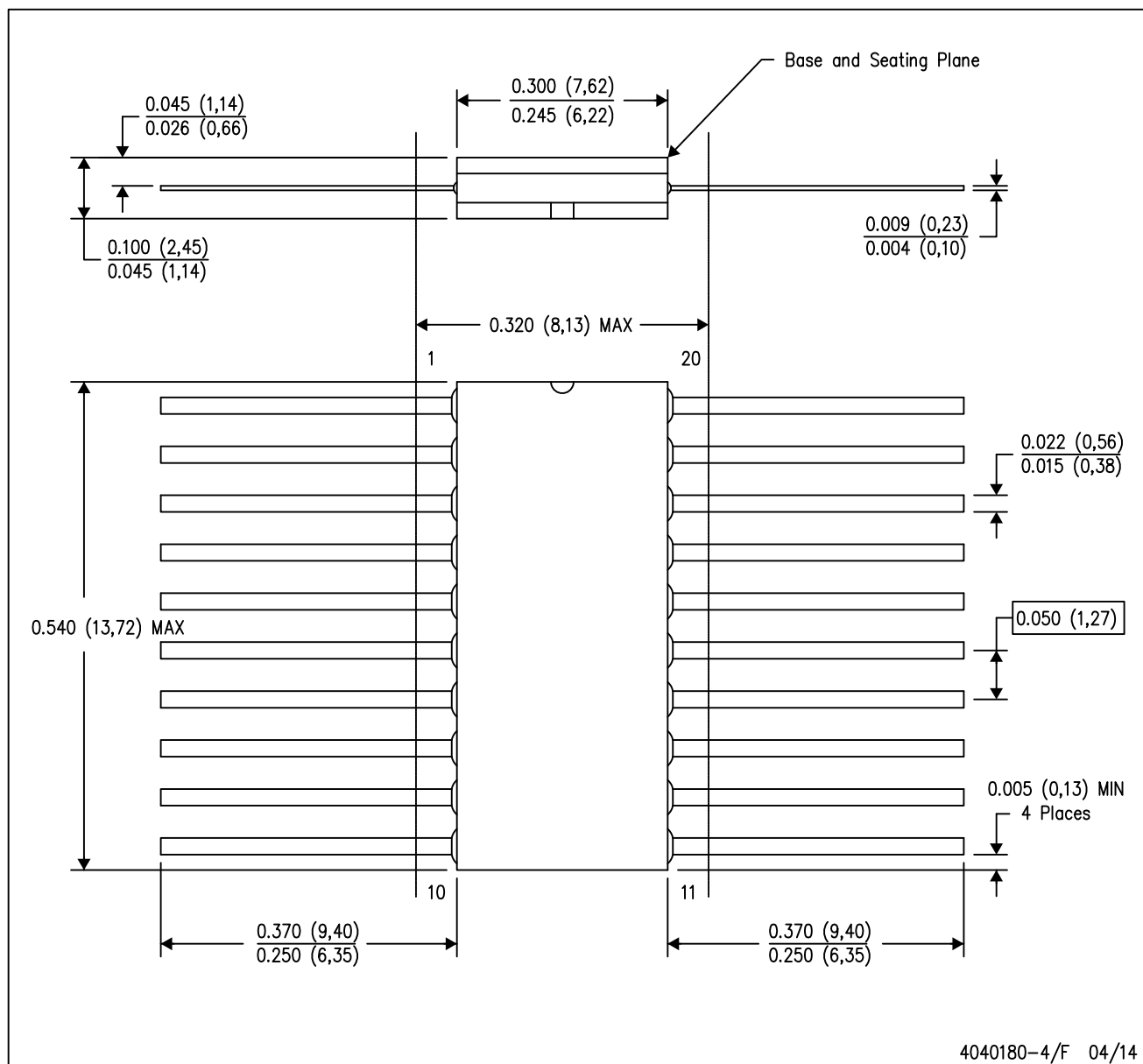


\*All dimensions are nominal

| Device            | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-87631012A    | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| 5962-8763101SA    | W            | CFP          | 20   | 25  | 506.98 | 26.16  | 6220   | NA     |
| 5962-8763101VSA   | W            | CFP          | 20   | 25  | 506.98 | 26.16  | 6220   | NA     |
| 5962-8763101VSA.A | W            | CFP          | 20   | 25  | 506.98 | 26.16  | 6220   | NA     |
| SN74ACT374N       | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| SN74ACT374N.A     | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| SNJ54ACT374FK     | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SNJ54ACT374FK.A   | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SNJ54ACT374W      | W            | CFP          | 20   | 25  | 506.98 | 26.16  | 6220   | NA     |
| SNJ54ACT374W.A    | W            | CFP          | 20   | 25  | 506.98 | 26.16  | 6220   | NA     |

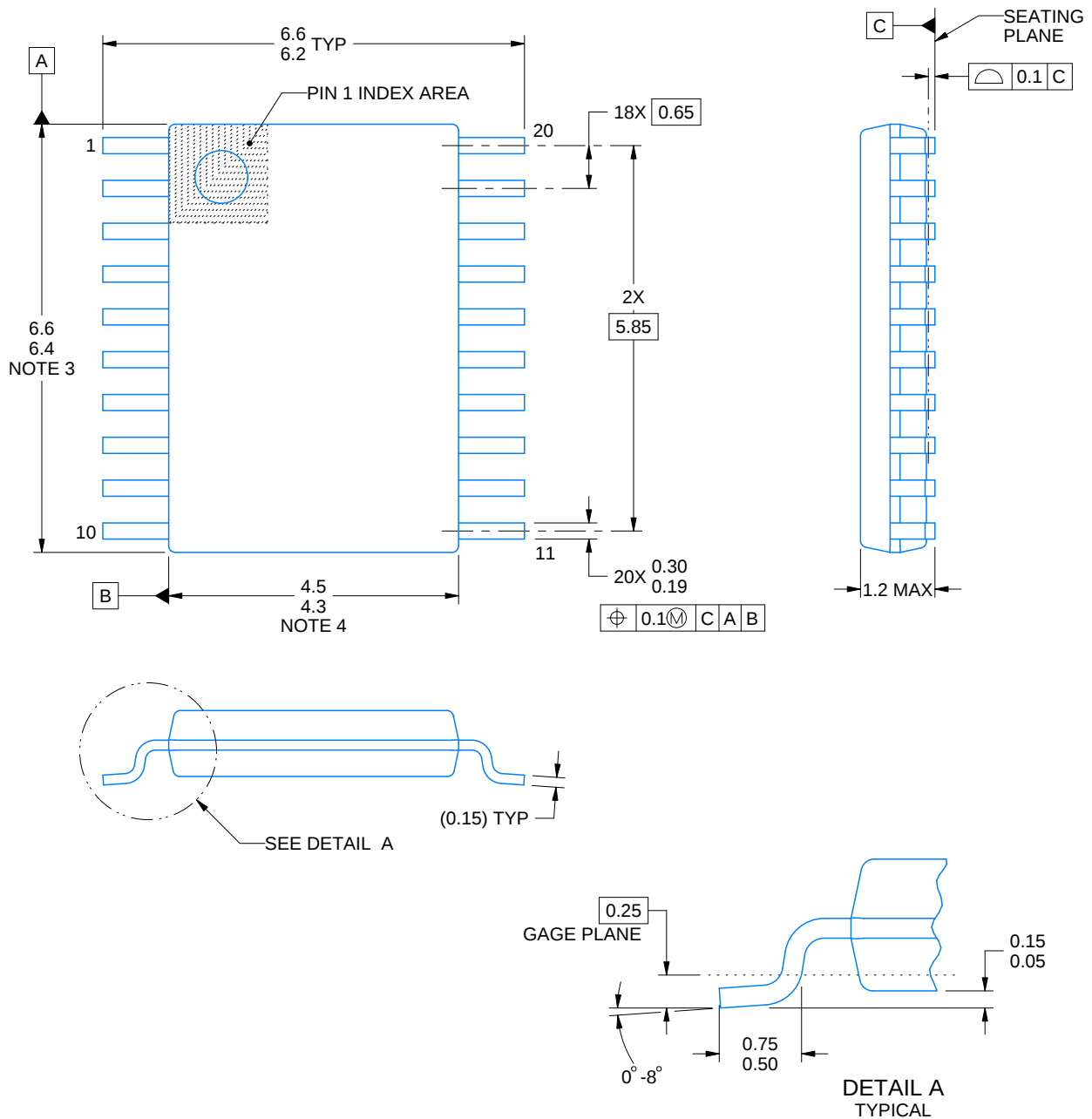
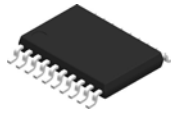
W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



4220206/A 02/2017

## NOTES:

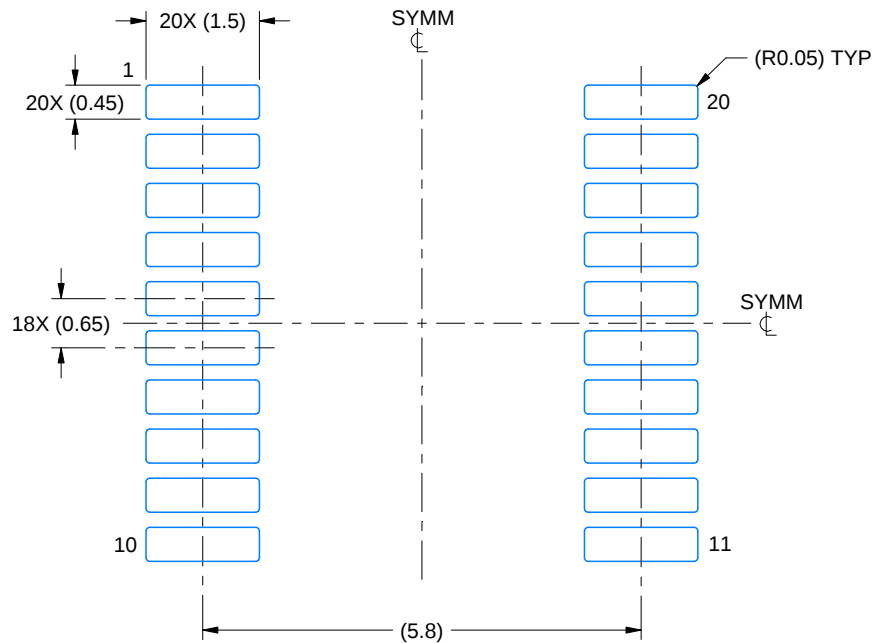
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

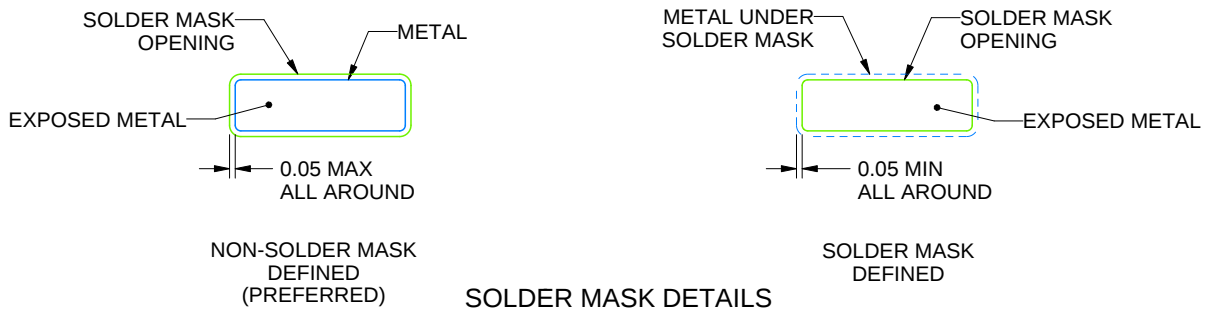
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

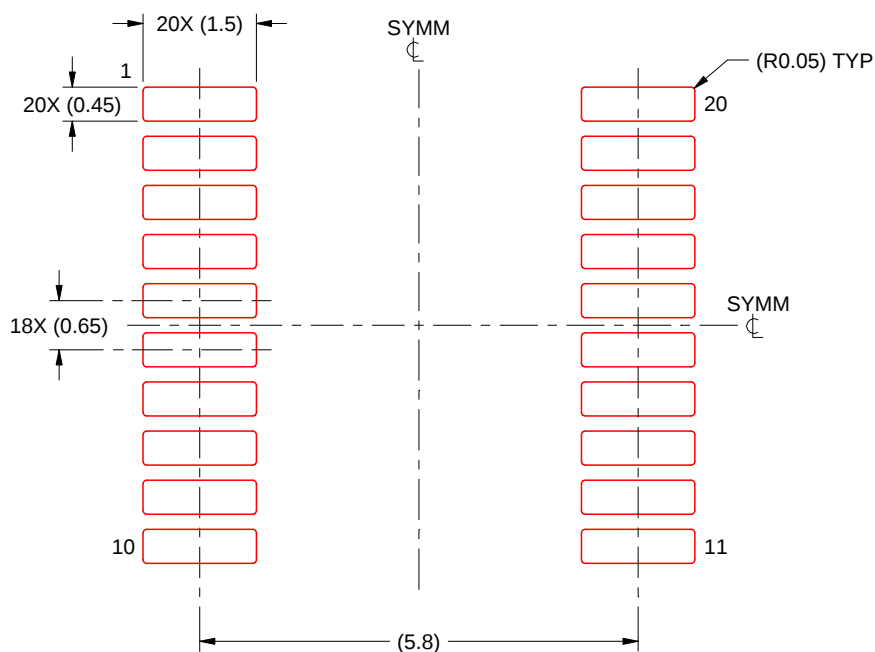
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

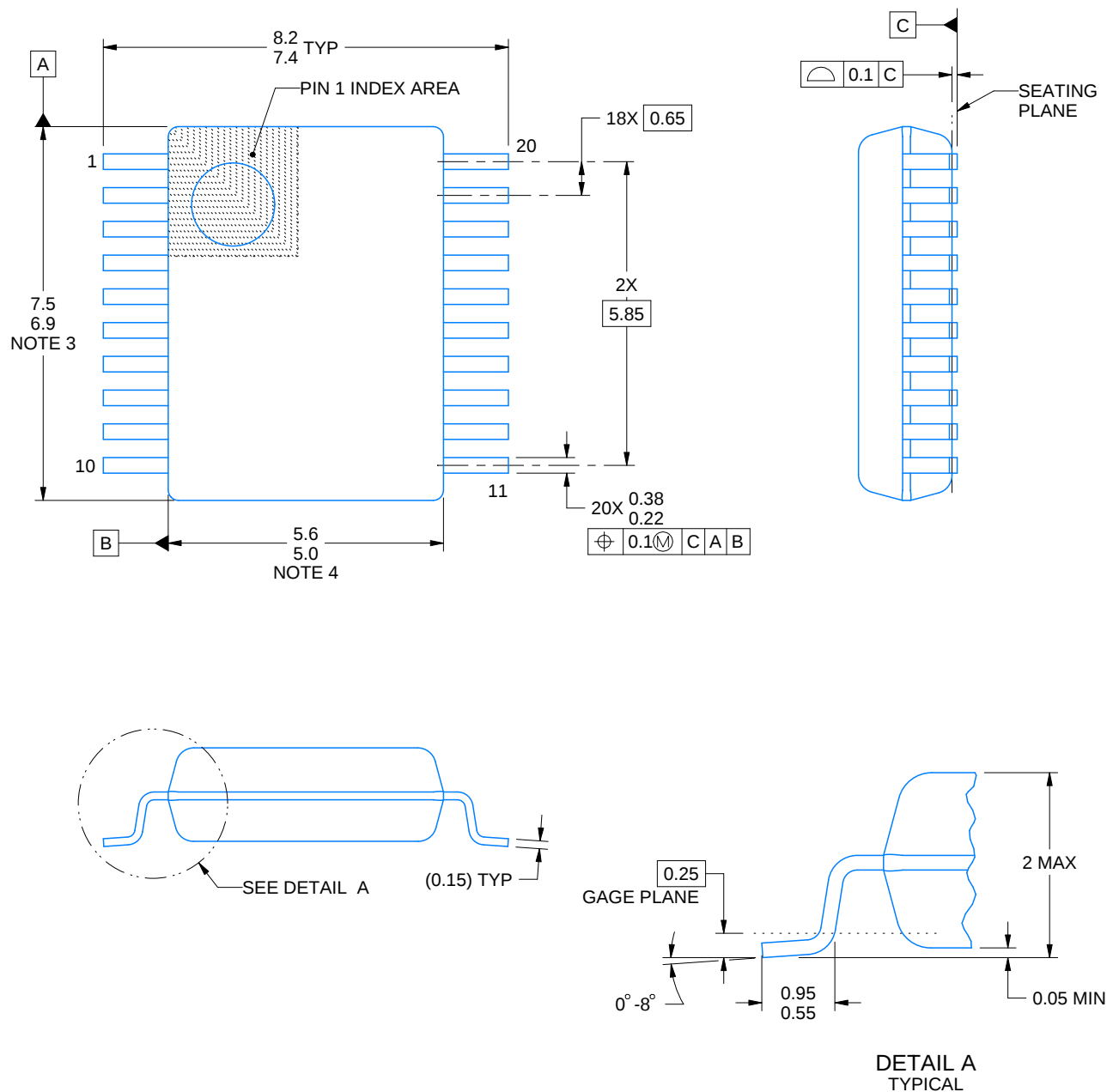
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



## SSOP - 2 mm max height

## SMALL OUTLINE PACKAGE



4214851/B 08/2019

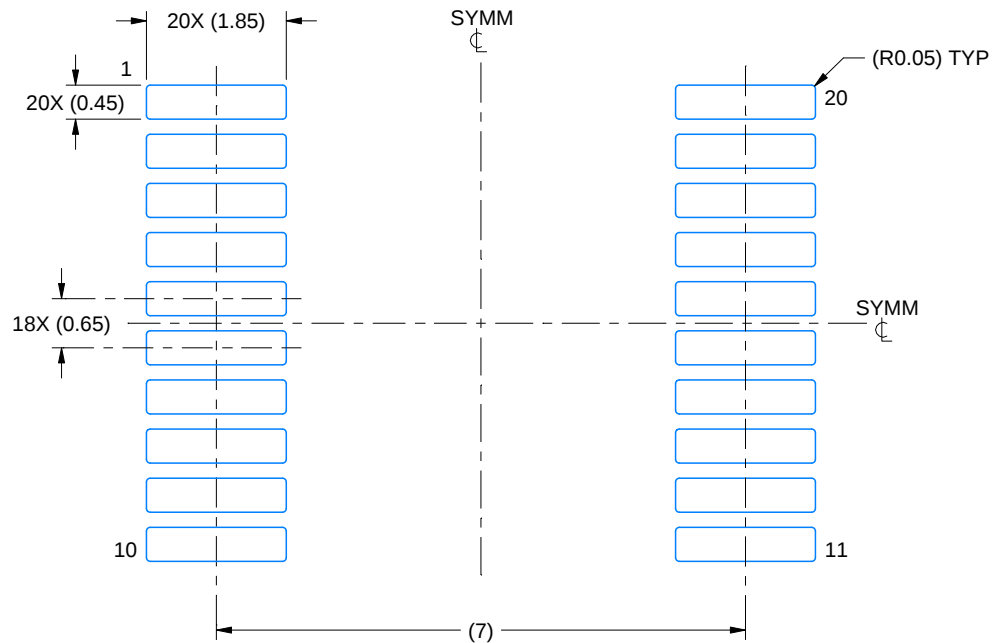
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

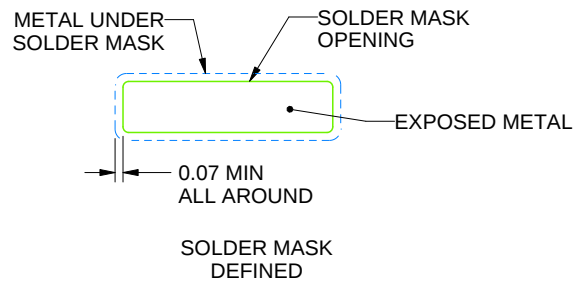
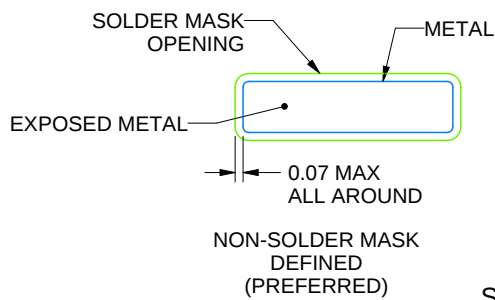
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

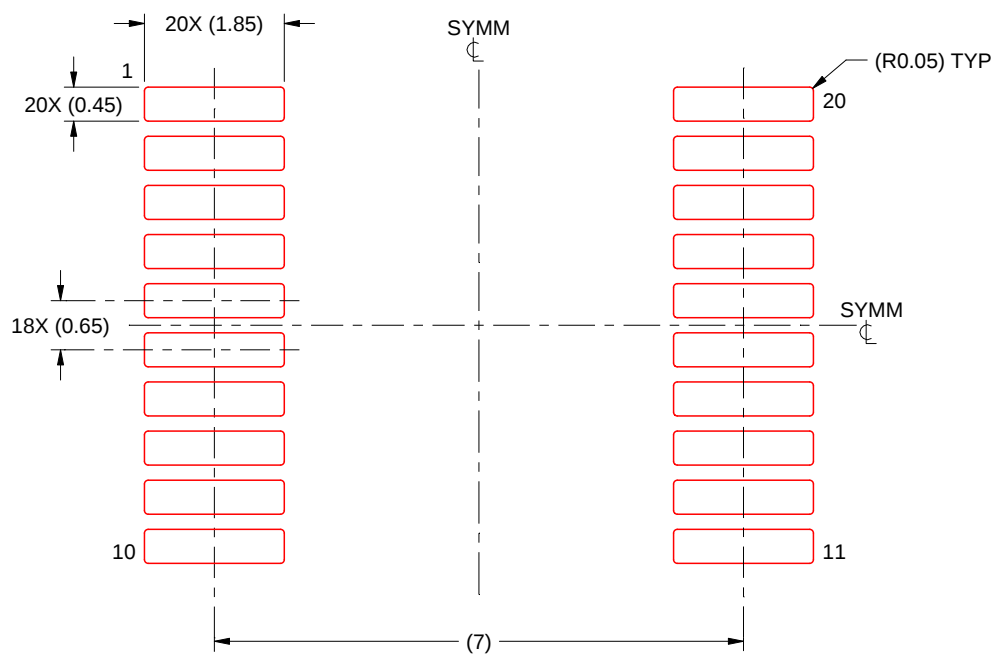
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

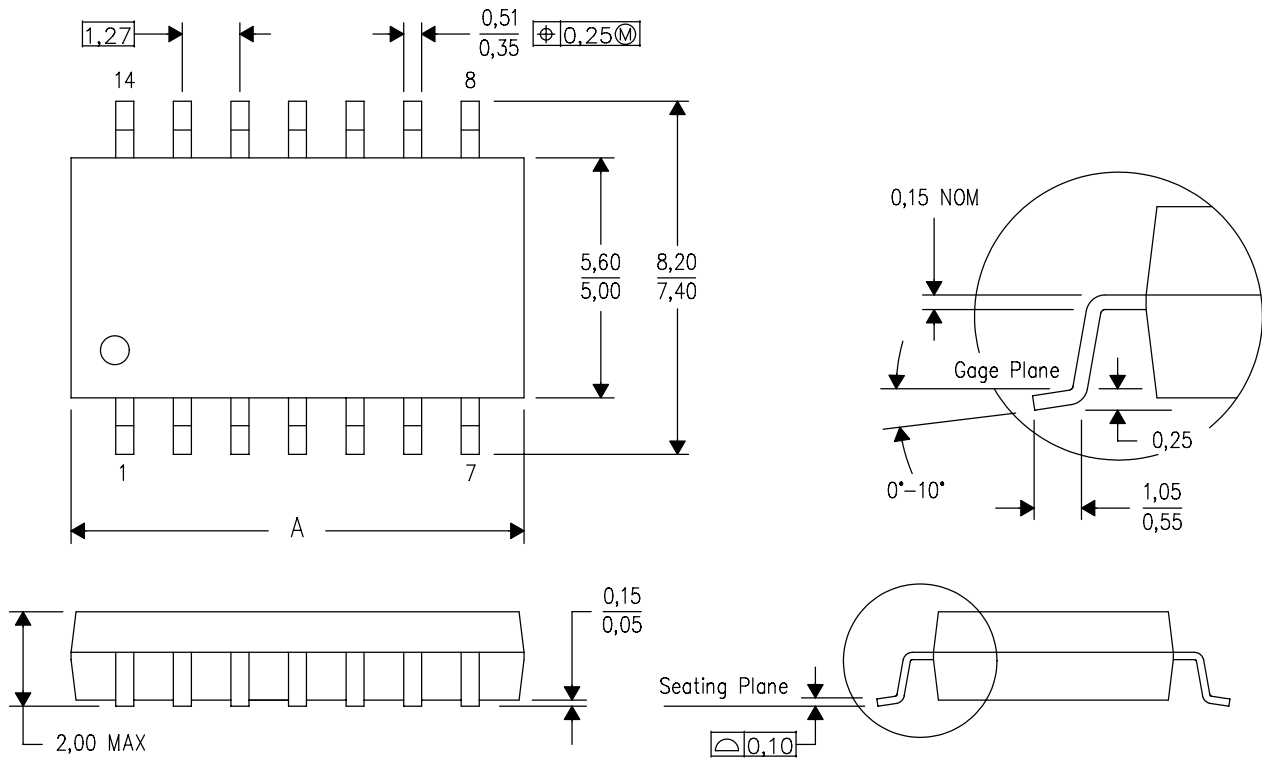
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



| DIM \ PINS ** | 14    | 16    | 20    | 24    |
|---------------|-------|-------|-------|-------|
| A MAX         | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN         | 9,90  | 9,90  | 12,30 | 14,70 |

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

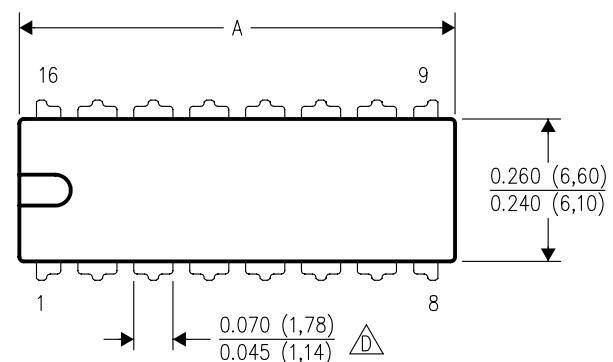


4229370VA\

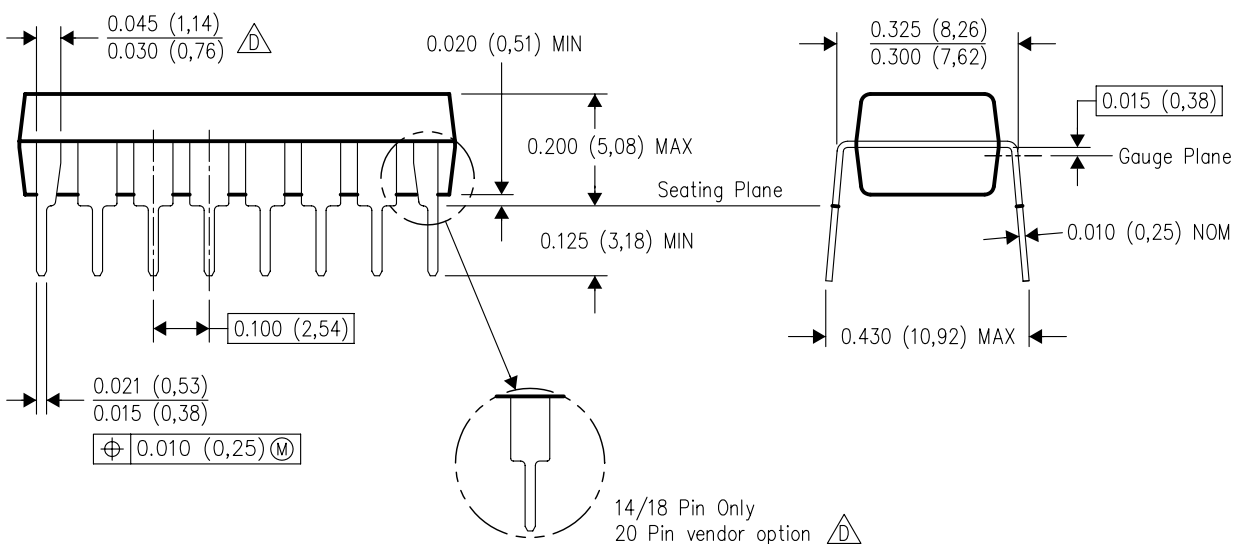
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



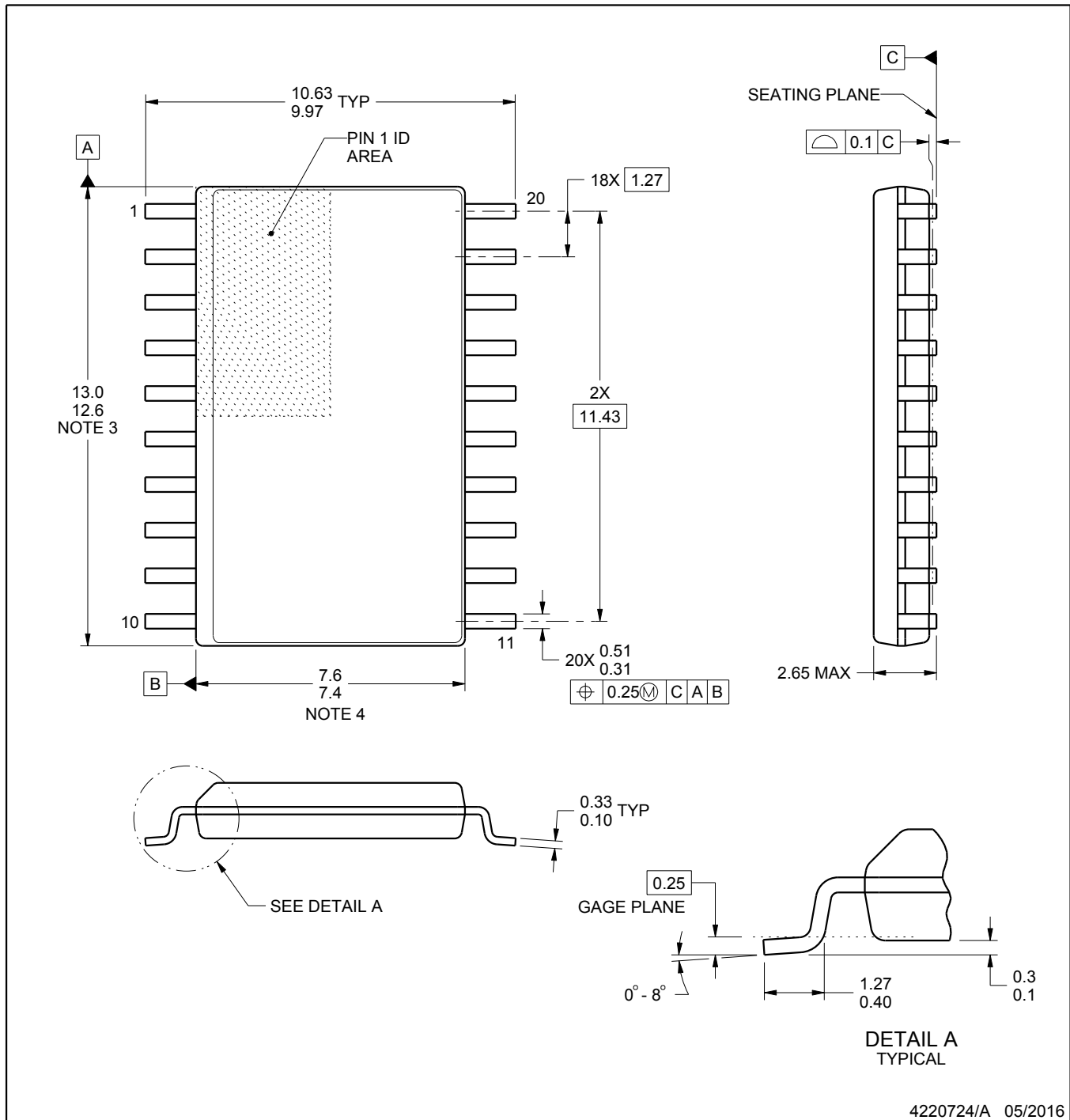
| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



## NOTES:

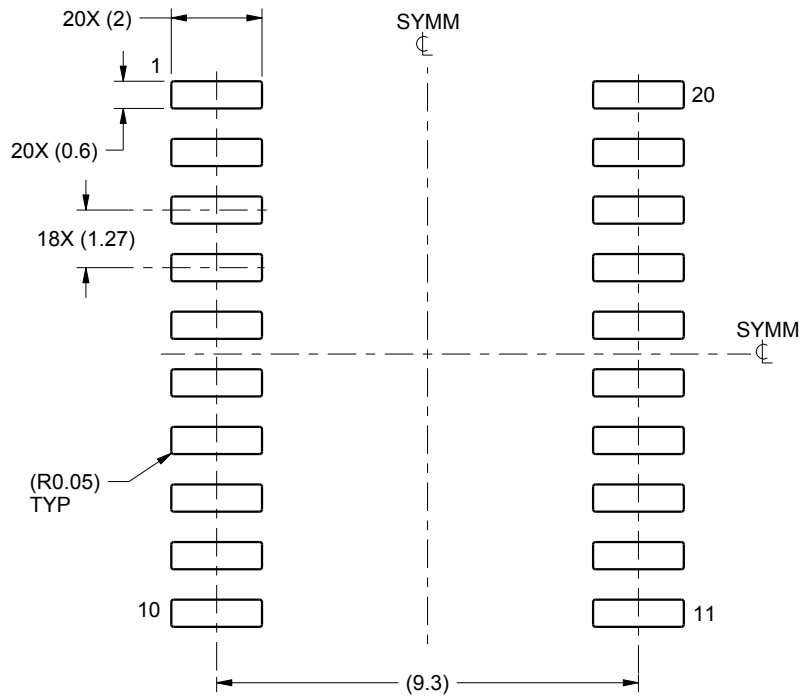
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

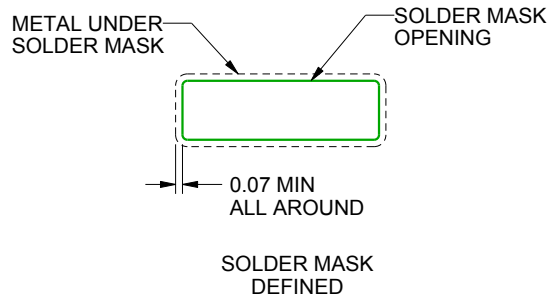
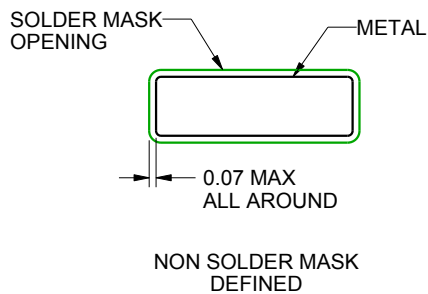
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

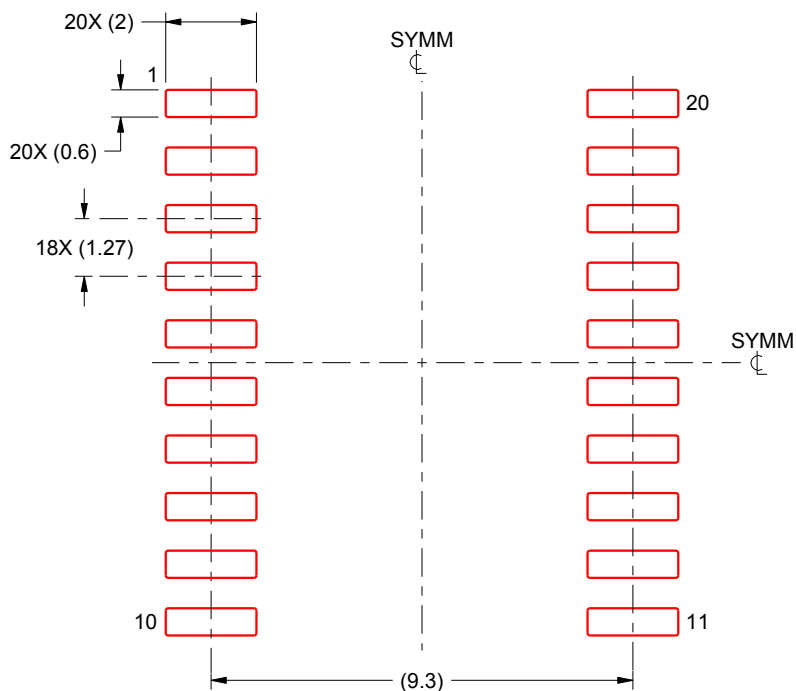
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

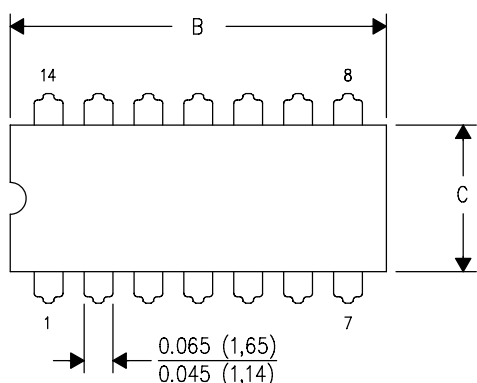
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

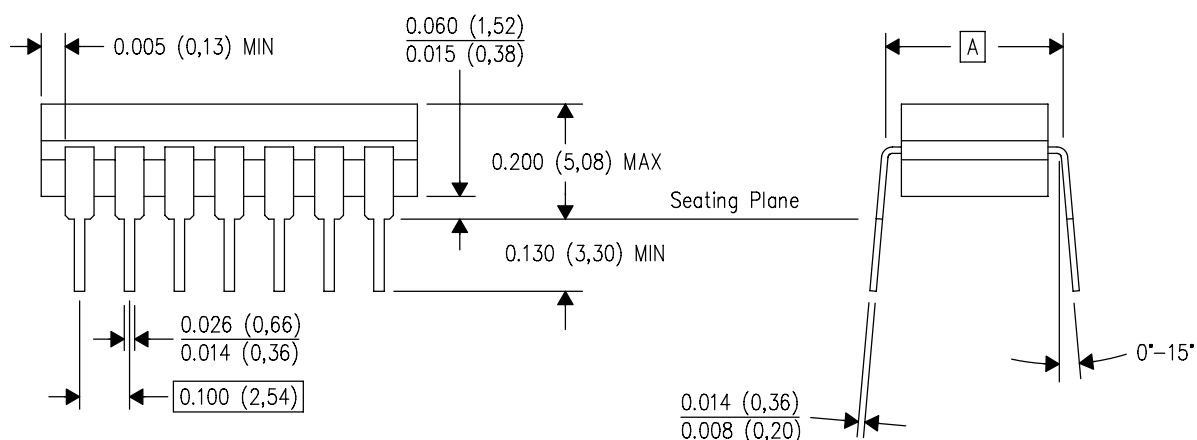
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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