TEXAS INSTRUMENTS
SN54HC253, SN74HC253
JAJSO59F – DECEMBER 1982 – REVISED FEBRUARY 2022

# SNx4HC253 3 ステート出力、デュアル、4 ライン入力 1 ライン出力、データ・セレクタ / マルチプレクサ

## 1 特長

- 'HC153 の 3 ステート・バージョン
- 幅広い動作電圧範囲:2V～6V
- 大電流反転出力は最大 15 個の LSTTL 負荷を駆動可能
- 低消費電力、$I_{CC}$:80μA 以下
- $t_{pd}$ = 9ns (標準値)
- 5V で ±6mA の出力駆動能力
- 低い入力電流:最大 1μA
- n ラインから 1 ラインへの多重化に対応
- パラレル / シリアル変換を実行

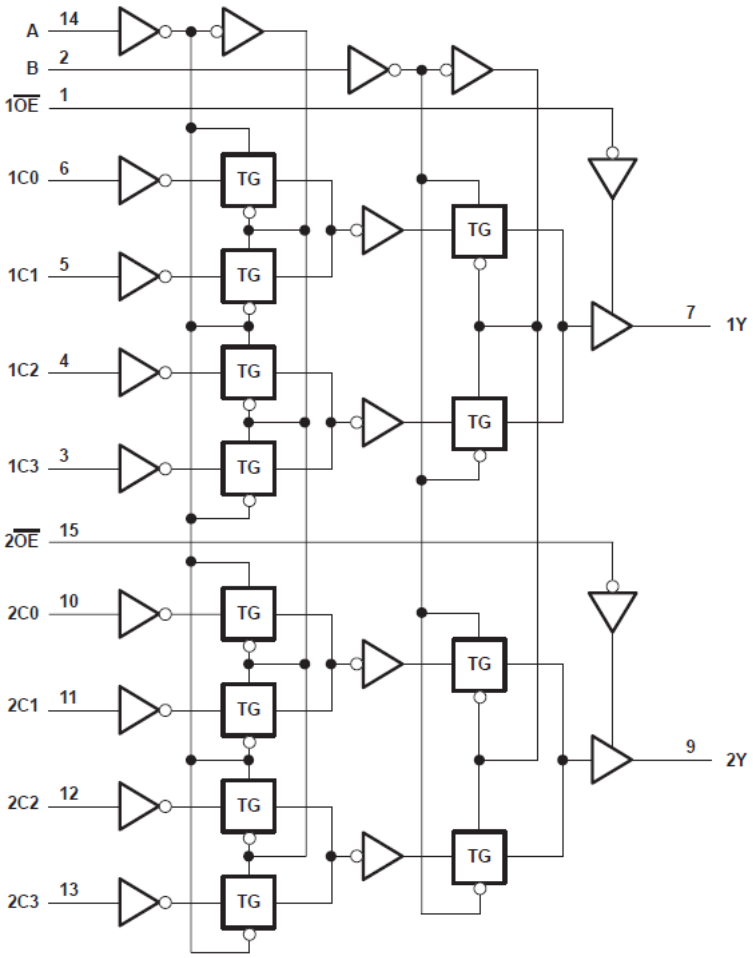
## 2 概要

SNx4HC253 デバイスは、4 つのデータ源の 1 つを選択するためのフル・バイナリ・デコード機能とストローブ制御 ($\overline{OE}$) 3 ステート出力を備えた 2 つのデータ・セレクタ / マルチプレクサを内蔵しています。

**製品情報**

| 部品番号 | パッケージ[1] | 本体サイズ (公称) |
|---|---|---|
| SN74HC253D | SOIC (16) | 9.90mm × 3.90mm |
| SN74HC253DB | SSOP (16) | 6.20mm × 5.30mm |
| SN74HC253N | PDIP (16) | 19.31mm × 6.35mm |
| SN74HC253NS | SO (16) | 6.20mm × 5.30mm |
| SN54HC253J | CDIP (16) | 24.38mm × 6.92mm |
| SNJ54HC253FK | LCCC (20) | 8.89mm × 8.45mm |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。




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ここに示すピン番号は D、DB、J、N、NS、W の各パッケージのものです。

## 機能ブロック図


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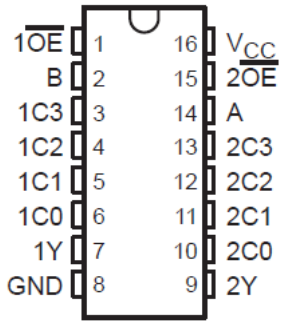
## 3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

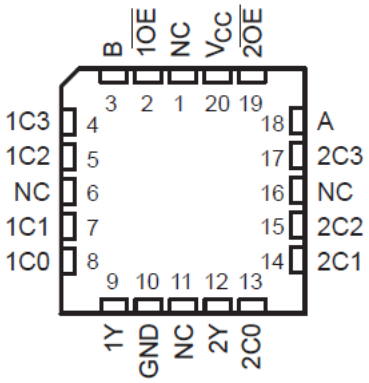
| Changes from Revision E (September 2003) to Revision F (February 2022) | Page |
|---|---|
| • 最新のデータシート規格を反映するように、文書全体にわたって表、図、相互参照の採番方法を更新 | 1 |

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## 4 Pin Configuration and Functions




**J, D, DB, N, or NS Package**
**16-Pin CDIP, SOIC, SSOP, PDIP, SO**
**Top View**




NC – No internal connection

**FK Package**
**20-Pin LCCC**
**Top View**


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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $I_{IK}$ | Input clamp current(2) | $V_I < 0$ or $V_I > V_{CC}$ | | ±20 | mA |
| $I_{OK}$ | Output clamp current(2) | $V_O < 0$ or $V_O > V_{CC}$ | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O = 0$ to $V_{CC}$ | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 Recommended Operating Conditions(1)

| | | | SN54HC253 | | | SN74HC253 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5 | 6 | 2 | 5 | 6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | | 1.5 | | | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | | | 3.15 | | | |
| | | $V_{CC}$ = 6 V | 4.2 | | | 4.2 | | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | | 0.5 | | | 0.5 | V |
| | | $V_{CC}$ = 4.5 V | | | 1.35 | | | 1.35 | |
| | | $V_{CC}$ = 6 V | | | 1.8 | | | 1.8 | |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| Δt/Δv | Input transition rise/fall time | $V_{CC}$ = 2 V | | | 1000 | | | 1000 | ns |
| | | $V_{CC}$ = 4.5 V | | | 500 | | | 500 | |
| | | $V_{CC}$ = 6 V | | | 400 | | | 400 | |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | −40 | | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 5.3 Thermal Information

| THERMAL METRIC(1) | | D (SOIC) 16 PINS | DB (SSOP) 16 PINS | N (PDIP) 16 PINS | NS (SO) 16 PINS | UNIT |
|---|---|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 73 | 82 | 67 | 64 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

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## 5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS[1] | | $V_{CC}$ (V) | $T_A$ = 25°C | | | SN54HC253 | | SN74HC253 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = −20 µA | | 2 | 1.9 | 1.998 | | 1.9 | | 1.9 | | V |
| | | | 4.5 | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | | 6 | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | $I_{OH}$ = −6 mA | | 4.5 | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | $I_{OH}$ = −7.8 mA | | 6 | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| $V_{OL}$ | $I_{OL}$ = 20 µA | | 2 | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | | 4.5 | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | | 6 | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 6 mA | | 4.5 | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | $I_{OL}$ = 7.8 mA | | 6 | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| $I_I$ | $V_I$ = $V_{CC}$ or 0 | | 6 | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or 0 | | 6 | | ±0.01 | ±0.5 | | ±10 | | ±5 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or 0 | $I_O$ = 0 | 6 | | | 8 | | 160 | | 80 | µA |
| $C_i$ | | | 2 to 6 | | 3 | 10 | | 10 | | 10 | pF |

(1) $V_I$ = $V_{IH}$ or $V_{IL}$, unless otherwise noted.

## 5.5 Switching Characteristics

over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 6)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ (V) | $T_A$ = 25°C | | | SN54HC253 | | SN74HC253 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A or B | Any Y | 2 | | 62 | 150 | | 225 | | 190 | ns |
| | | | 4.5 | | 19 | 30 | | 45 | | 38 | |
| | | | 6 | | 16 | 26 | | 38 | | 32 | |
| | Data (Any C) | Y | 2 | | 54 | 126 | | 210 | | 175 | |
| | | | 4.5 | | 16 | 28 | | 42 | | 35 | |
| | | | 6 | | 13 | 23 | | 36 | | 30 | |
| $t_{en}$ | $\overline{OE}$ | Y | 2 | | 28 | 100 | | 150 | | 125 | ns |
| | | | 4.5 | | 11 | 20 | | 30 | | 25 | |
| | | | 6 | | 9 | 17 | | 26 | | 21 | |
| $t_{dis}$ | $\overline{OE}$ | Y | 2 | | 21 | 135 | | 203 | | 170 | ns |
| | | | 4.5 | | 14 | 30 | | 45 | | 38 | |
| | | | 6 | | 12 | 35 | | 38 | | 31 | |
| $t_t$ | | Y | 2 | | 28 | 60 | | 90 | | 75 | ns |
| | | | 4.5 | | 8 | 12 | | 18 | | 15 | |
| | | | 6 | | 6 | 10 | | 15 | | 13 | |


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## 5.6 Switching Characteristics

over recommended operating free-air temperature range, $C_L$ = 150 pF (unless otherwise noted) (see Figure 6)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ (V) | $T_A$ = 25°C | | | SN54HC253 | | SN74HC253 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A or B | Any Y | 2 | | 76 | 235 | | 355 | | 295 | ns |
| | | | 4.5 | | 23 | 47 | | 71 | | 59 | |
| | | | 6 | | 20 | 41 | | 60 | | 51 | |
| | Data (Any C) | Y | 2 | | 68 | 220 | | 335 | | 275 | |
| | | | 4.5 | | 20 | 44 | | 67 | | 55 | |
| | | | 6 | | 17 | 38 | | 57 | | 51 | |
| $t_{en}$ | $\overline{OE}$ | Y | 2 | | 44 | 185 | | 280 | | 230 | ns |
| | | | 4.5 | | 16 | 37 | | 56 | | 46 | |
| | | | 6 | | 14 | 32 | | 48 | | 40 | |
| $t_t$ | | Y | 2 | | 45 | 210 | | 315 | | 265 | ns |
| | | | 4.5 | | 17 | 42 | | 63 | | 53 | |
| | | | 6 | | 13 | 36 | | 53 | | 45 | |

## 5.7 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per multiplexer | No load | 45 | pF |

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## 6 Parameter Measurement Information

$t_{pd}$ is the maximum between $t_{PLH}$ and $t_{PHL}$

$t_t$ is the maximum between $t_{TLH}$ and $t_{THL}$

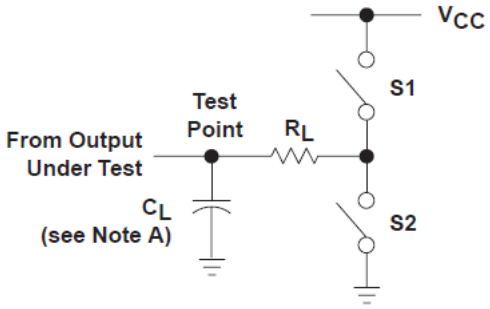



**図 6-1. Load Circuit**

| PARAMETER | | $R_L$ | $C_L$ | S1 | S2 |
|---|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 1 kΩ | 50 pF or 150 pF | Open | Closed |
| | $t_{PZL}$ | | | Closed | Open |
| $t_{dis}$ | $t_{PHZ}$ | 1 kΩ | 50 pF | Open | Closed |
| | $t_{PLZ}$ | | | Closed | Open |
| $t_{pd}$ or $t_t$ | | -- | 50 pF or 150 pF | Open | Open |

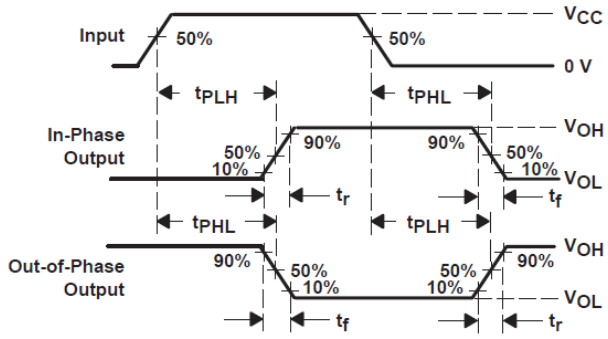



**図 6-2. Voltage Waveforms**
**Propagation Delay and Output Transition Times**

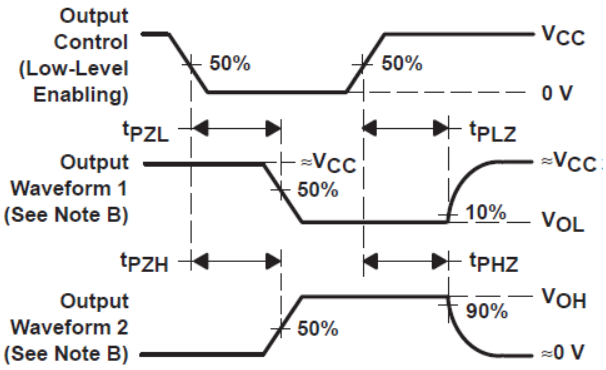



**図 6-3. Voltage Waveforms**
**Enable and Disable Times for 3-State Outputs**

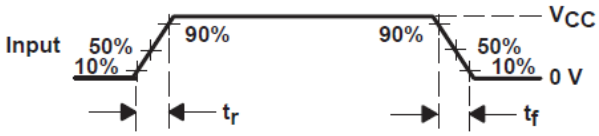



**図 6-4. Voltage Waveform**
**Input Rise and Fall Times**

A. $C_L$ includes probe and test-fixture capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when diabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when diabled by the output control.

C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following charactersitics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 6 ns, $t_f$ = 6 ns.

D. The outputs are measured one at a time with one input transition per measurement.

E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.

F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.


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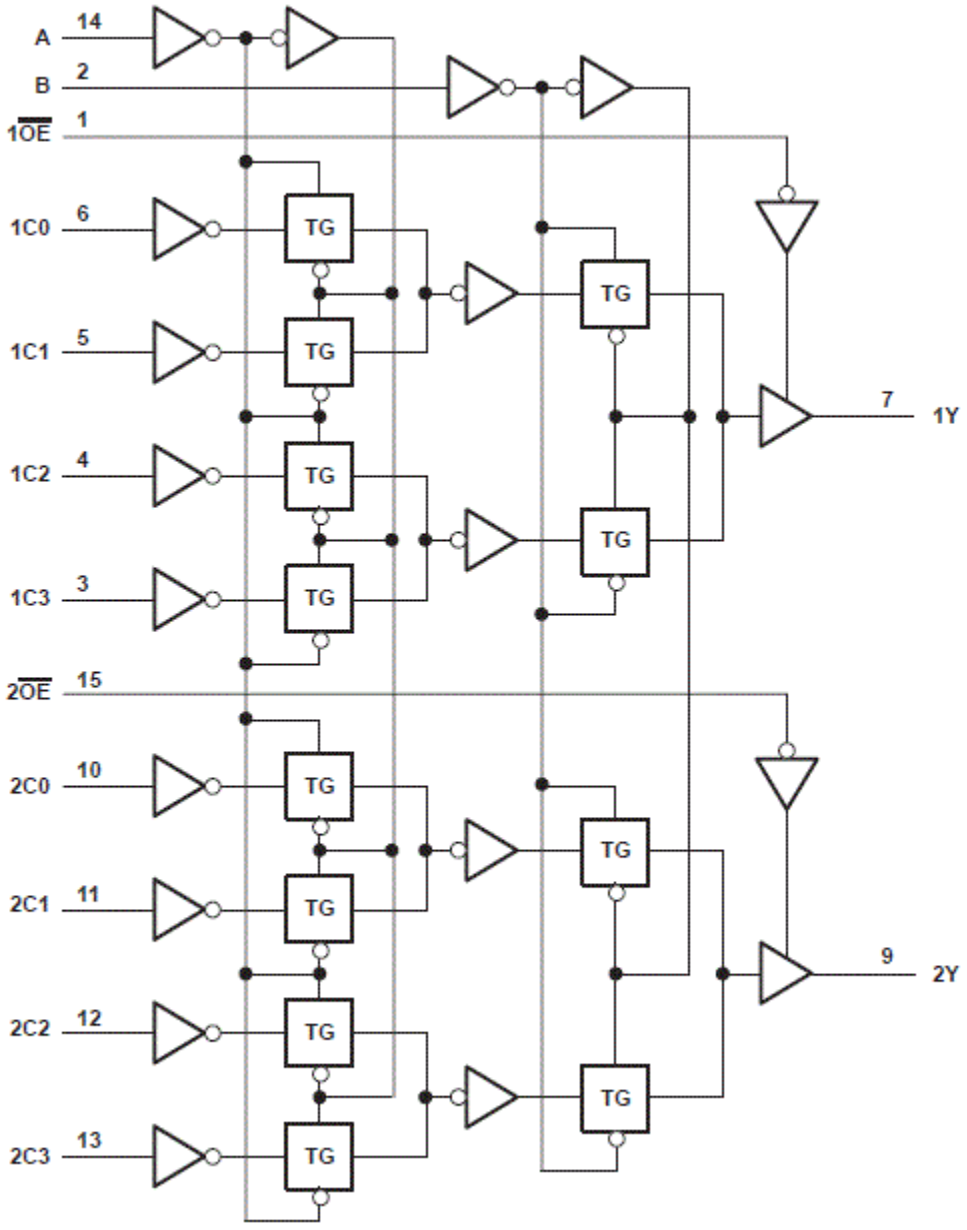
# 7 Detailed Description

## 7.1 Overview

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output-control inputs are provided for each of the two 4-line sections.

The 3-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (in the high-impedance state), the low impedance of the single enabled output drives the bus line to a high or low logic level. Each output has its own output-enable ($\overline{OE}$) input. The outputs are disabled when their respective $\overline{OE}$ is high.

## 7.2 Functional Block Diagram



## 7.3 Device Functional Modes

**表 7-1. Function Table**

| INPUTS | | | | | | | OUTPUT Y |
|---|---|---|---|---|---|---|---|
| SELECT[1] | | DATA | | | | $\overline{OE}$ | |
| B | A | C0 | C1 | C2 | C3 | | |
| X | X | X | X | X | X | H | Z |
| L | L | L | X | X | X | L | L |
| L | L | H | X | X | X | L | H |
| L | H | X | L | X | X | L | L |
| L | H | X | H | X | X | L | H |
| H | L | X | X | L | X | L | L |
| H | L | X | X | H | X | L | H |
| H | H | X | X | X | L | L | L |
| H | H | X | X | X | H | L | H |

(1) Select inputs A and B are common to both sections.


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# 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

# 9 Layout

## 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.

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# 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.2 サポート・リソース

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## 10.3 Trademarks

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## 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.5 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-88682012A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-88682012A SNJ54HC 253FK |
| 5962-8868201EA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8868201EA SNJ54HC253J |
| SN54HC253J | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54HC253J |
| SN54HC253J.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54HC253J |
| SN74HC253D | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -40 to 85 | HC253 |
| SN74HC253DBR | Last Time Buy | Production | SSOP (DB) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC253 |
| SN74HC253DBR.A | Last Time Buy | Production | SSOP (DB) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC253 |
| SN74HC253DR | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | HC253 |
| SN74HC253DR.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC253 |
| SN74HC253DT | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -40 to 85 | HC253 |
| SN74HC253N | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HC253N |
| SN74HC253N.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HC253N |
| SN74HC253NE4 | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HC253N |
| SN74HC253NSR | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC253 |
| SN74HC253NSR.A | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC253 |
| SNJ54HC253FK | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-88682012A SNJ54HC 253FK |
| SNJ54HC253FK.A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-88682012A SNJ54HC 253FK |
| SNJ54HC253J | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8868201EA SNJ54HC253J |
| SNJ54HC253J.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8868201EA SNJ54HC253J |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54HC253, SN74HC253 :**

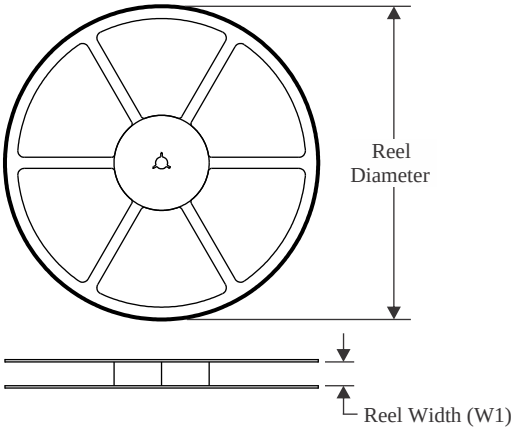
- Catalog : SN74HC253
- Automotive : SN74HC253-Q1, SN74HC253-Q1
- Enhanced Product : SN74HC253-EP, SN74HC253-EP
- Military : SN54HC253

NOTE: Qualified Version Definitions:

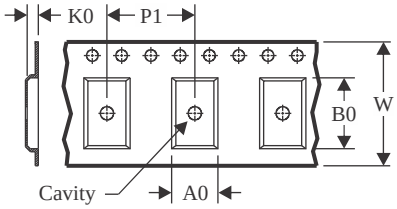
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

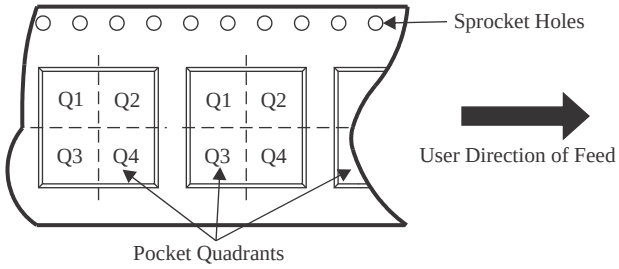



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

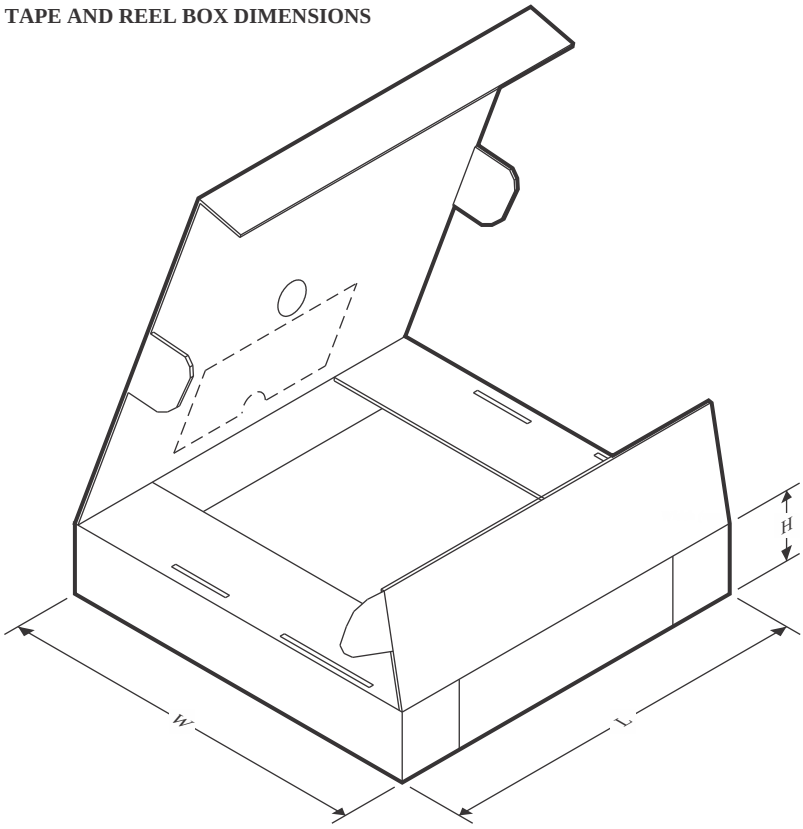
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HC253DBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74HC253DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC253NSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HC253NSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.45 | 10.55 | 2.5 | 12.0 | 16.2 | Q1 |

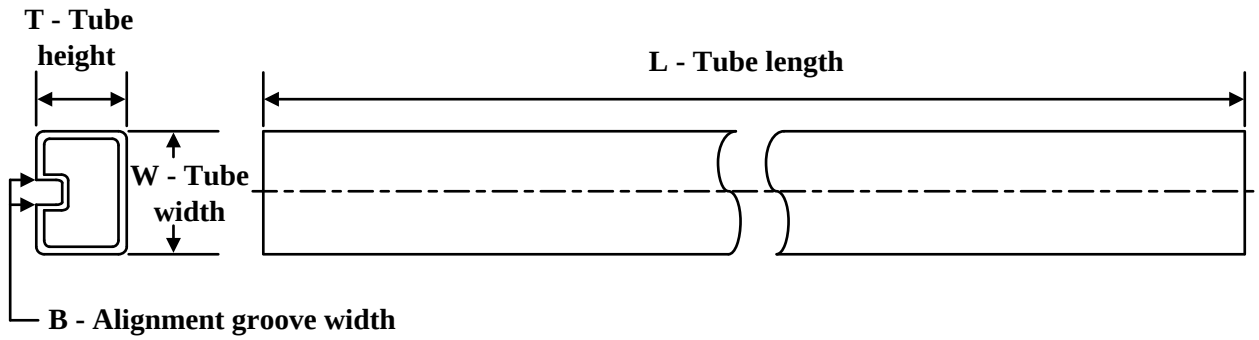
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74HC253DBR | SSOP | DB | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74HC253DR | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74HC253NSR | SOP | NS | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74HC253NSR | SOP | NS | 16 | 2000 | 353.0 | 353.0 | 32.0 |

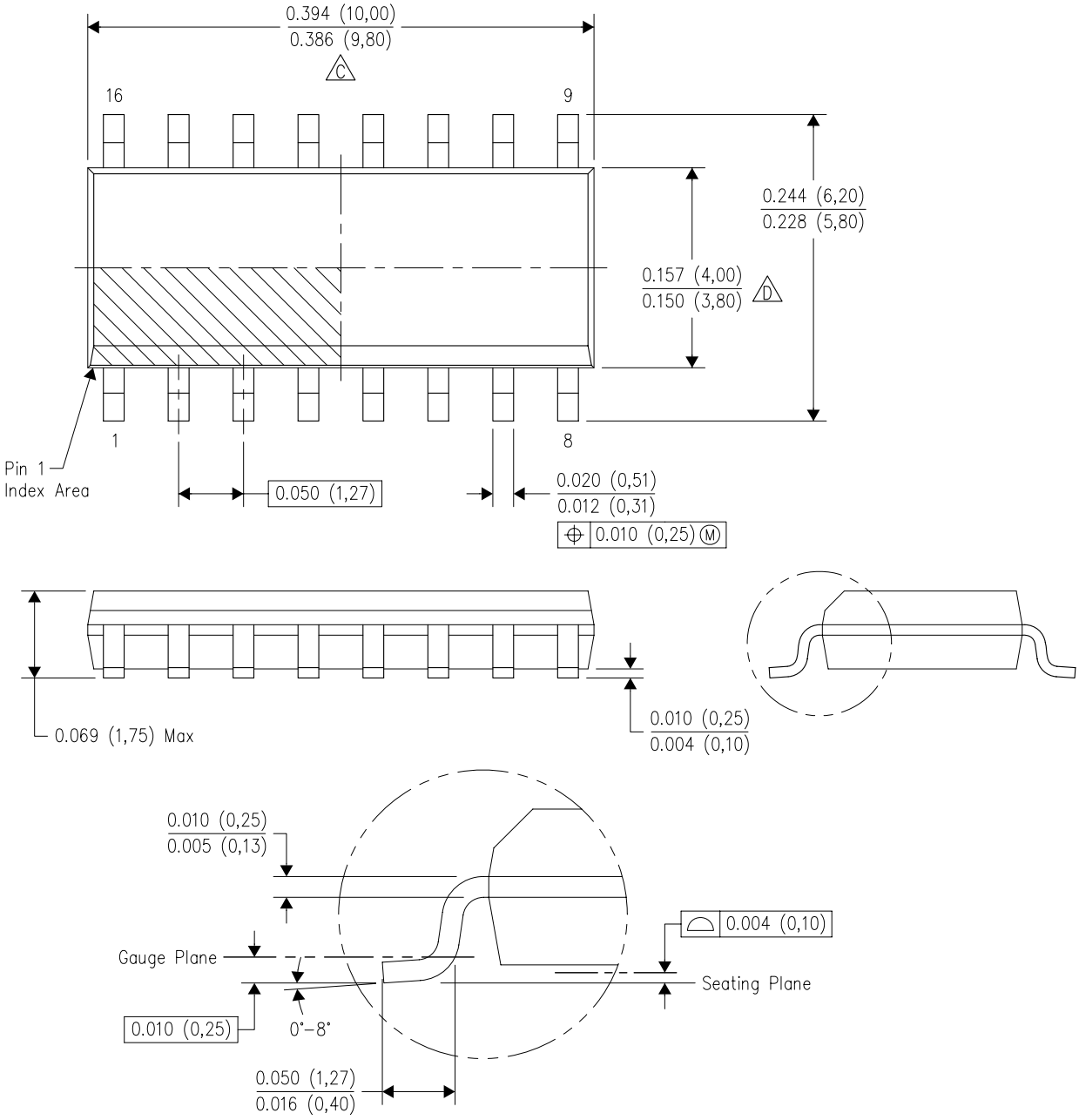
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-88682012A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SN74HC253N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC253N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC253N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC253N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC253NE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC253NE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54HC253FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54HC253FK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



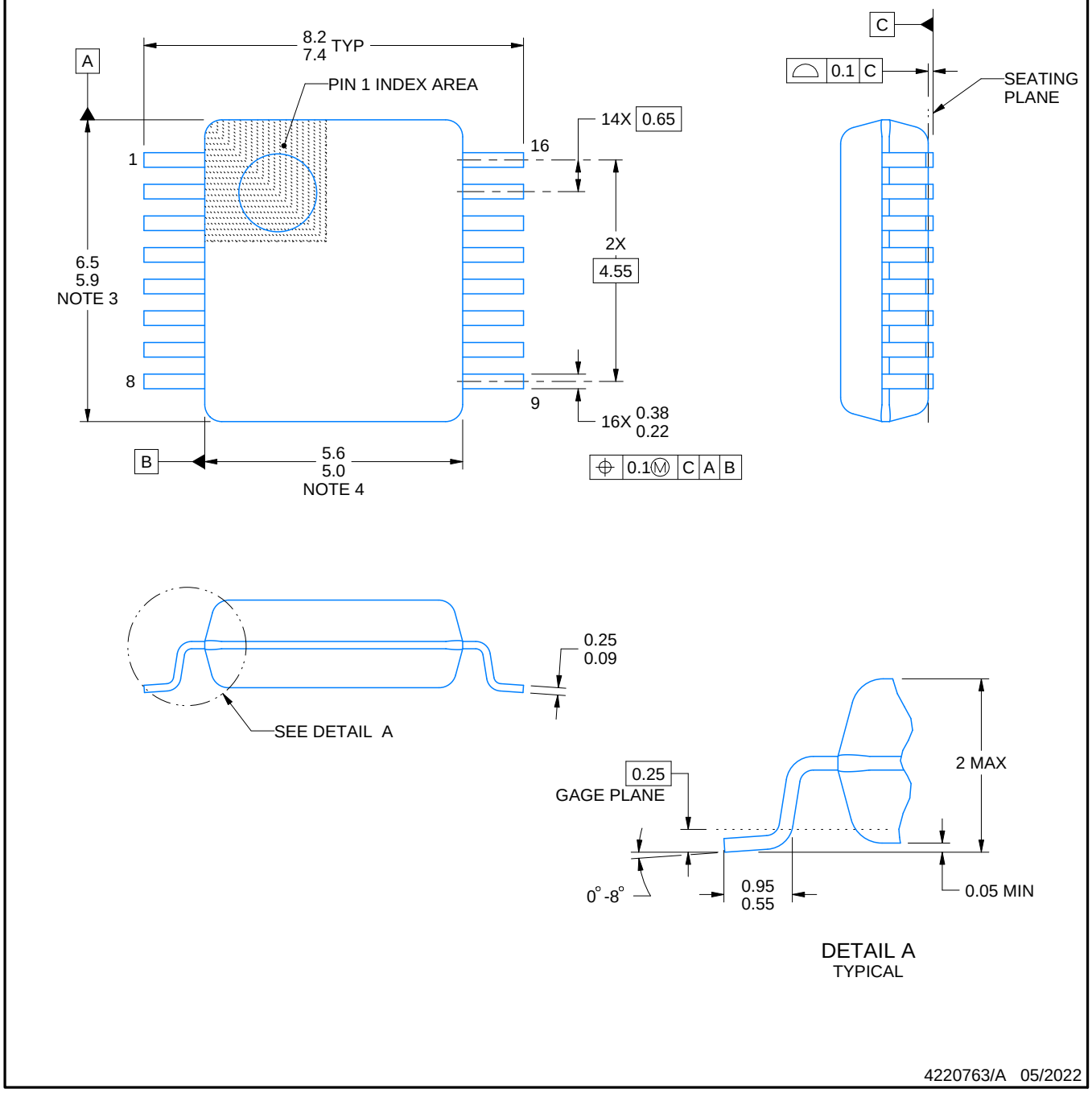

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

# PACKAGE OUTLINE

## DB0016A

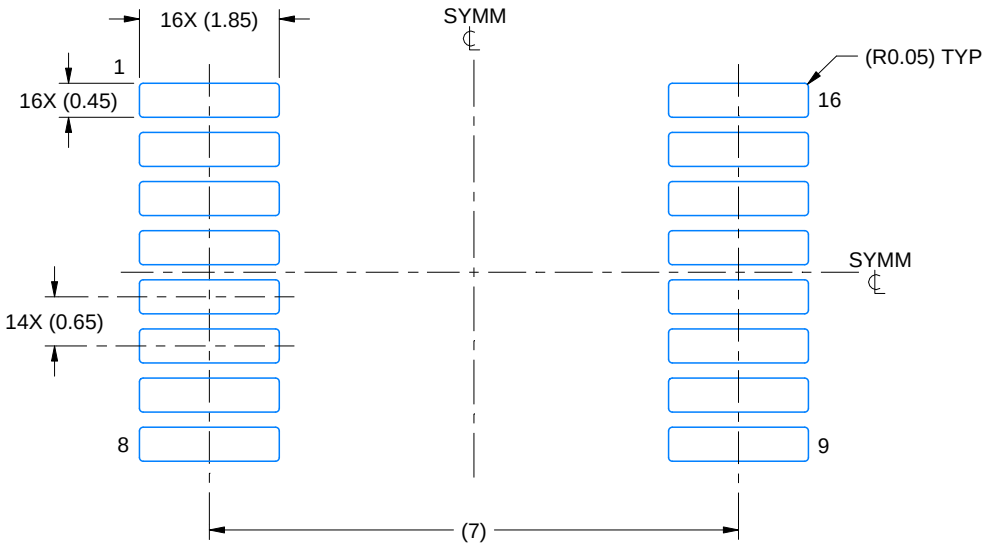
## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

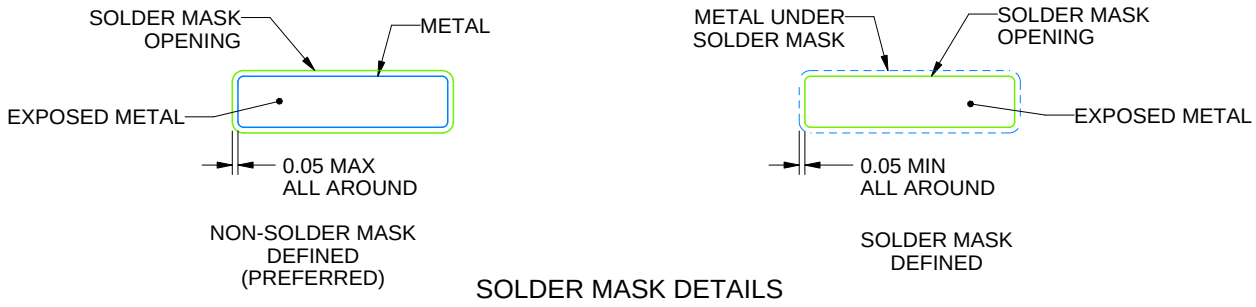



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

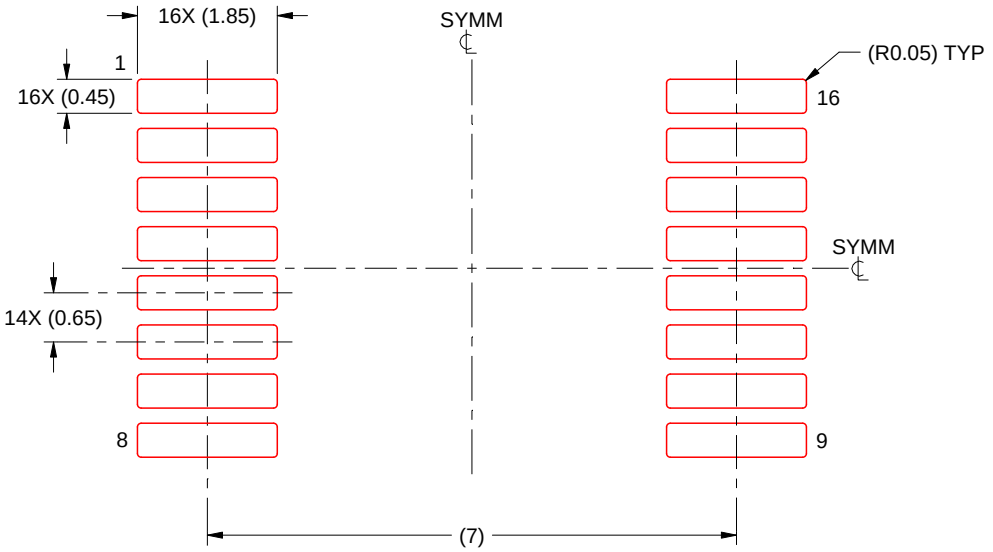



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

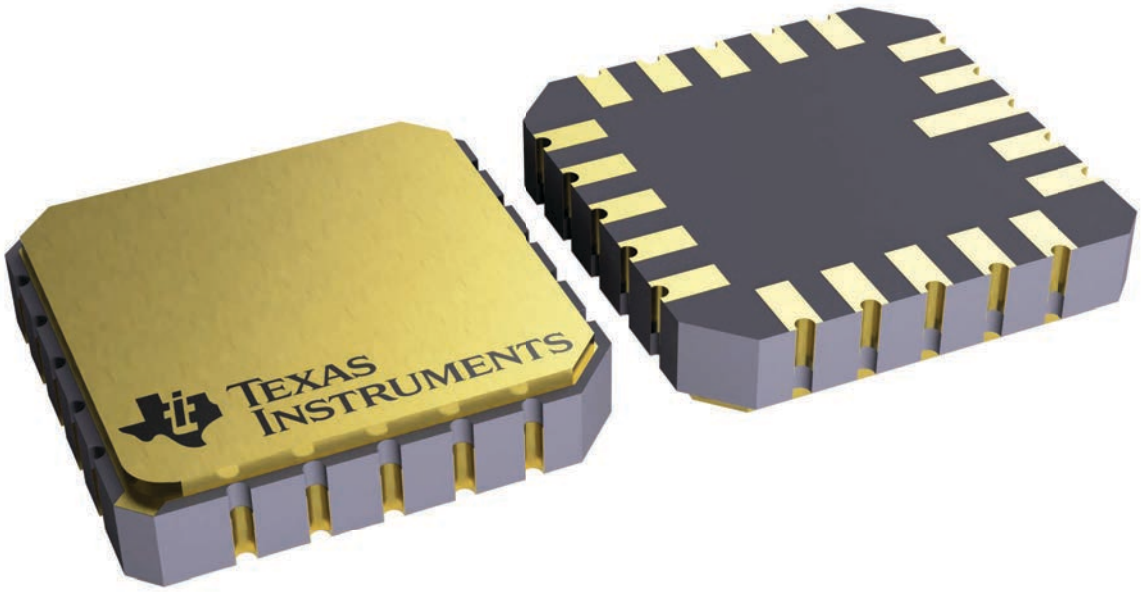
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

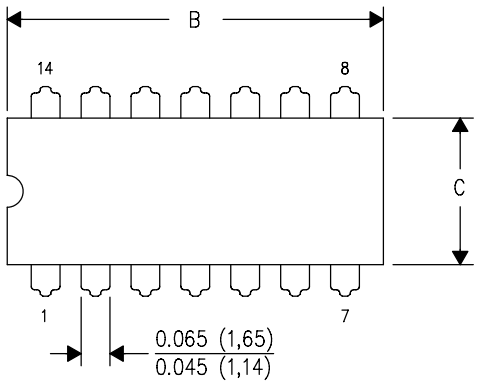



4229370VA\

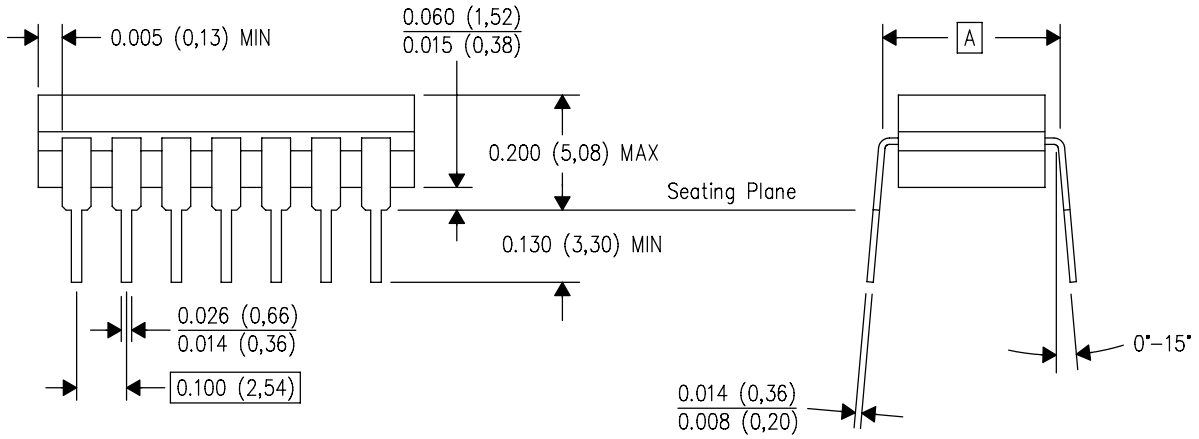
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



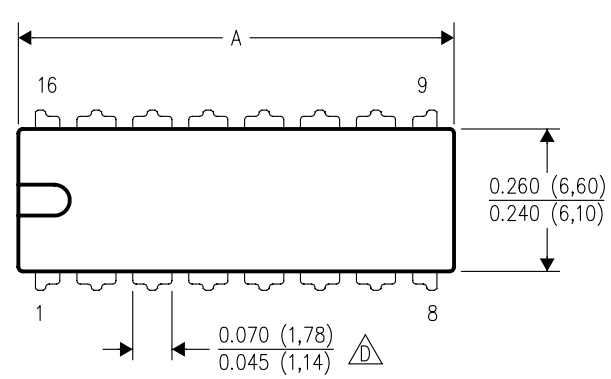

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

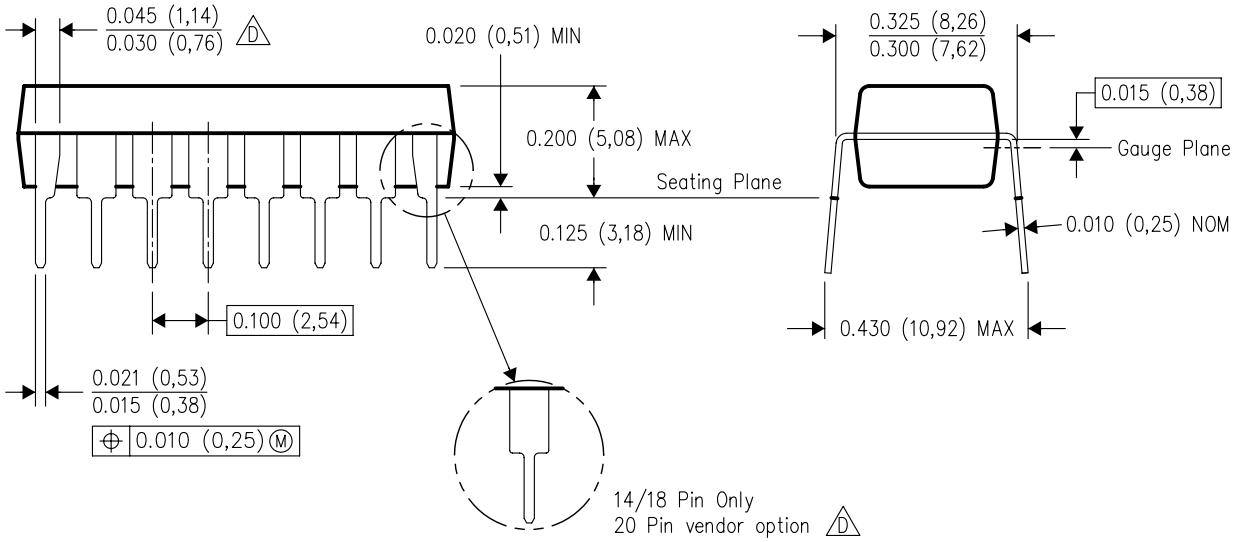
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

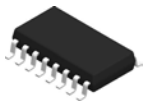



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

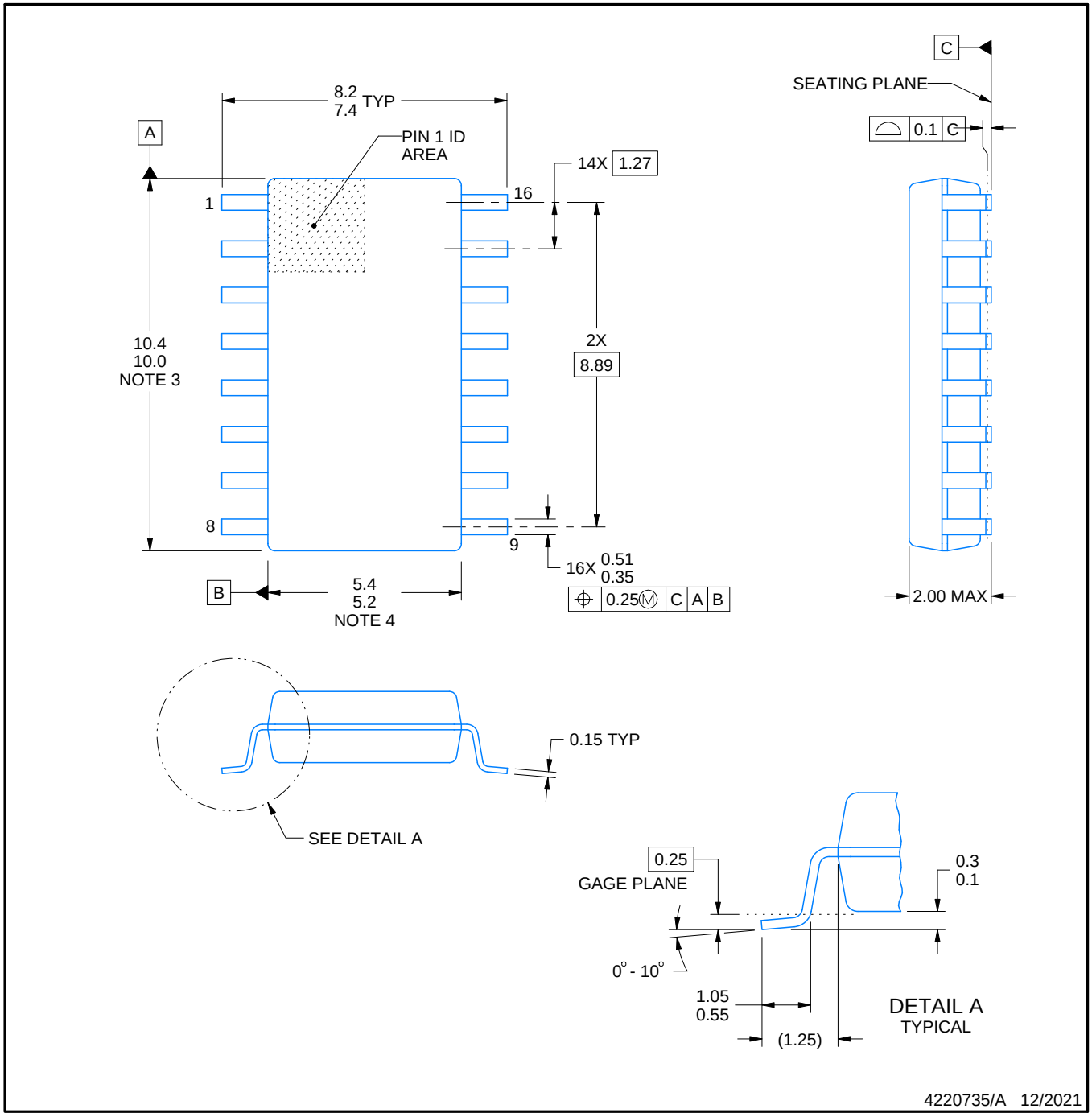


# PACKAGE OUTLINE

## NS0016A

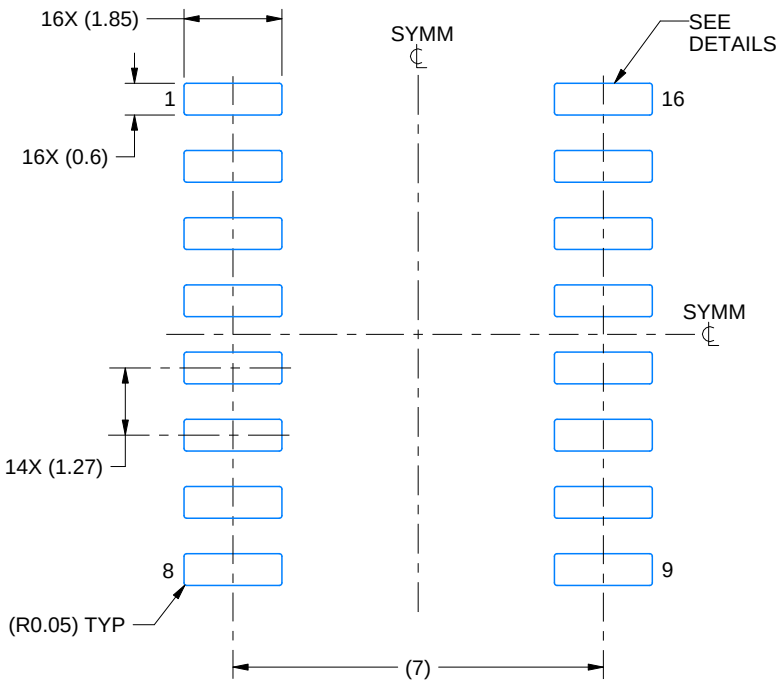
## SOP - 2.00 mm max height

SOP

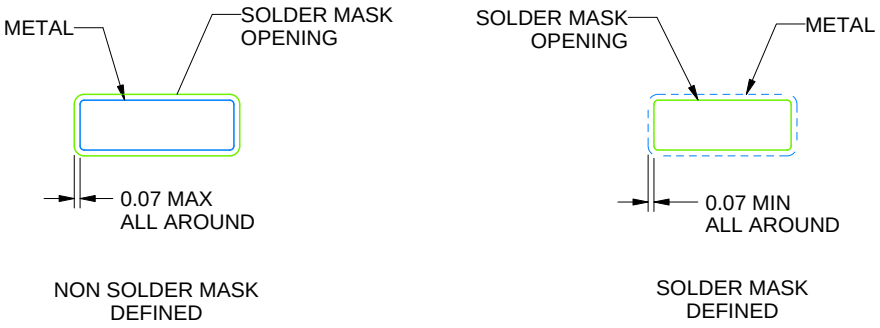



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.




LAND PATTERN EXAMPLE
SCALE:7X




NON SOLDER MASK
DEFINED

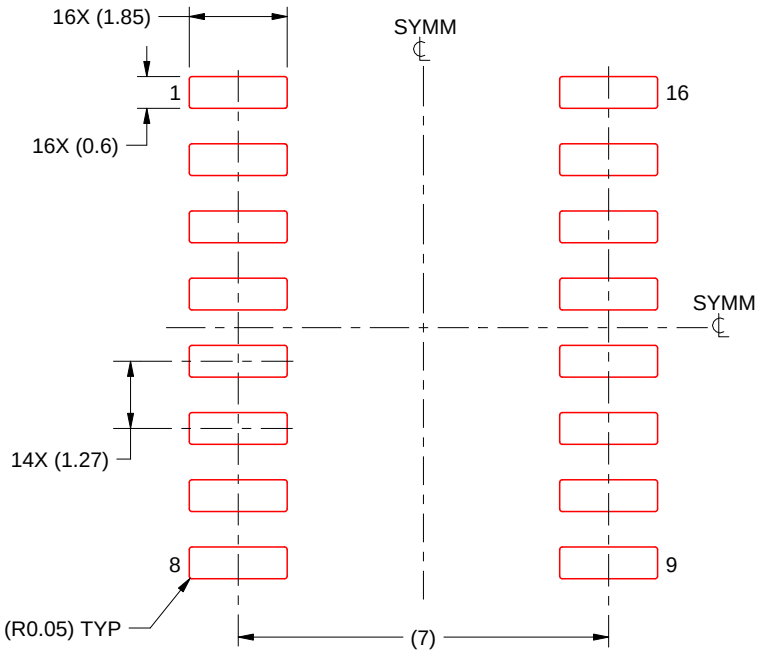
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月