TEXAS INSTRUMENTS
SN54HC541, SN74HC541
JAJSOM7E – JANUARY 1996 – REVISED MAY 2022

SNx4HC541 3 ステート出力、オクタル・バッファ / ライン・ドライバ

1 特長

- 広い動作電圧範囲:2V～6V
- バス・ラインを直接、または最大 15 の LSTTL 負荷を駆動する大電流 3 ステート出力
- 低い消費電力、最大 I_{CC}:80µA
- t_{pd} = 10ns (標準値)
- 5V で ±6mA の出力駆動能力
- 低い入力電流:最大値 1µA
- データ・フロースルーのピン配置 (すべての入力は出力の反対側)

2 アプリケーション

- LED
- サーバー
- PC およびノートパソコン
- ウェアラブルな健康機器
- 電子 POS

3 概要

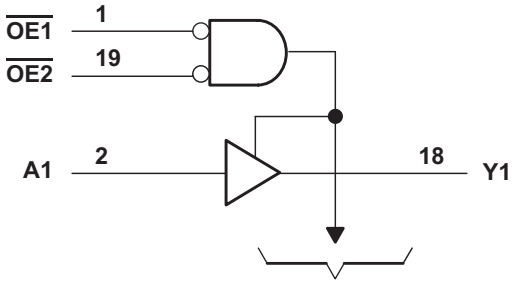
これらのオクタル・バッファおよびライン・ドライバは、SNx4HC541 デバイスの性能を備え、入力と出力がパッケージを挟んで反対側に位置するようにピンを配置しています。この配置のおかげで、プリント基板のレイアウトが非常に簡単です。

3 ステート出力は、2 入力 NOR ゲートによって制御されます。いずれかの出力イネーブル ($\overline{OE1}$ または $\overline{OE2}$) 入力が High の場合、8 つの出力はすべて高インピーダンス状態になります。SNx4HC541 デバイスは、出力側に真のデータを提供します。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
SN74HC541DW	SOIC (20)	12.80mm × 7.50mm
SN74HC541DB	SSOP (20)	7.20mm × 5.30mm
SN74HC541N	PDIP (20)	24.33mm × 6.35mm
SN74HC541NS	SO (20)	12.60mm × 5.30mm
SN74HC541PW	TSSOP (20)	6.50mm × 4.40mm
SN54HC541J	CDIP (20)	24.20mm × 6.92mm
SN54HC541FK	LCCC (20)	8.89mm × 8.89mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

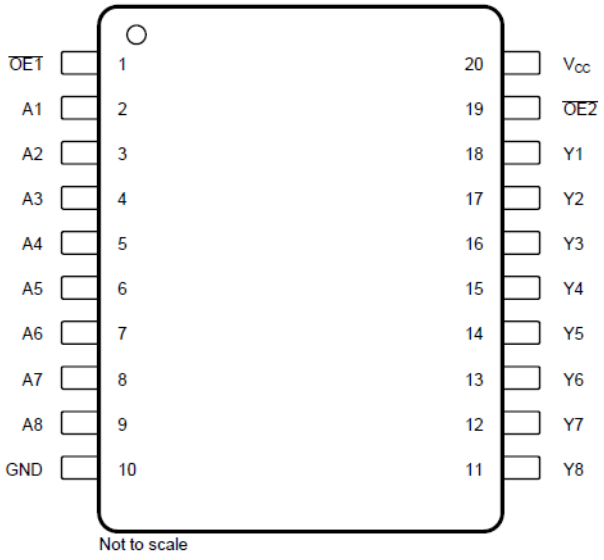
Changes from Revision D (September 2016) to Revision E (May 2022) — **Page**

- Updated ESD ratings table to include modern TI terminology ... 4
- Junction-to-ambient thermal resistance values increased. DB was 90.2 is now 122.7, DW was 77.5 is now 109.1, N was 45.2 is now 84.6, NS was 72.8 is now 113.4, PW was 98.3 is now 131.8 ... 5

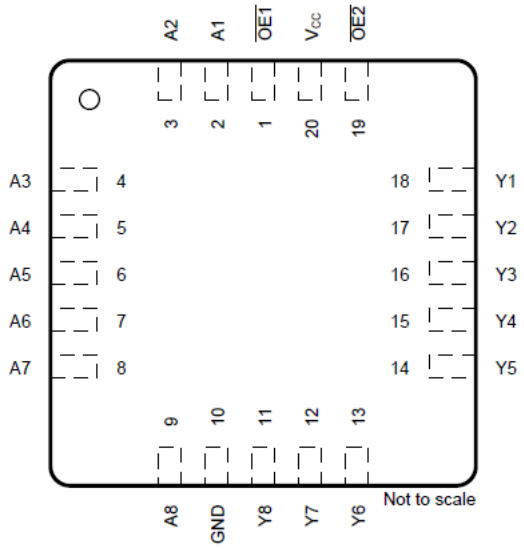
Changes from Revision C (August 2003) to Revision D (September 2016) — **Page**

- 「アプリケーション」セクション、「熱に関する情報」表、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ... 1
- 「注文情報」表を削除 (このデータシートの末尾にある「メカニカル、パッケージ、および注文情報」を参照) ... 1
- Changed $R_{\theta JA}$ for DB package from 70°C/W: to 90.2°C/W ... 5
- Changed $R_{\theta JA}$ for DW package from 58°C/W: to 77.5°C/W ... 5
- Changed $R_{\theta JA}$ for N package from 69°C/W: to 45.2°C/W ... 5
- Changed $R_{\theta JA}$ for NS package from 60°C/W: to 72.8°C/W ... 5
- Changed $R_{\theta JA}$ for PW package from 83°C/W: to 98.3°C/W ... 5

5 Pin Configuration and Functions



DB, DW, N, NS, J, or PW Package
20-Pin SSOP, SOIC, PDIP, SO, CDIP, or TSSOP
Top View



FK Package
20-Pin LCCC
Top View

Pin Functions

PIN		I/O[1]	DESCRIPTION
NO.	NAME		
1	$\overline{OE1}$	I	Output enable (active low) Both $\overline{OE}$ must be low to enable outputs
2	A1	I	Channel 1 input
3	A2	I	Channel 2 input
4	A3	I	Channel 3 input
5	A4	I	Channel 4 input
6	A5	I	Channel 5 input
7	A6	I	Channel 6 input
8	A7	I	Channel 7 input
9	A8	I	Channel 8 input
10	GND	—	Ground
11	Y8	O	Channel 8 output
12	Y7	O	Channel 7 output
13	Y6	O	Channel 6 output
14	Y5	O	Channel 5 output
15	Y4	O	Channel 4 output
16	Y3	O	Channel 3 output
17	Y2	O	Channel 2 output
18	Y1	O	Channel 1 output
19	$\overline{OE2}$	I	Output enable (active low) both $\overline{OE}$ must be low to enable outputs
20	V_{CC}	—	Power pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See note(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise and fall time	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature	SN54HC541	–55		125	°C
		SN74HC541	–40		85	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC		SN74HC541					UNIT
		DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	122.7	109.1	84.6	113.4	131.8	°C/W
$R_{\theta JC\ (top)}$	Junction-to-case (top) thermal resistance	81.6	76	72.5	78.6	72.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.5	77.6	65.3	78.4	82.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	46.1	51.5	55.3	47.1	21.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	77.1	77.1	65.2	78.1	82.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics, T_A = 25°C

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	2 V	1.9	1.998		V
			4.5 V	4.4	4.499		
			6 V	5.9	5.999		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	2 V	0.002		0.1	V
			4.5 V	0.001		0.1	
			6 V	0.001		0.1	
		I_{OL} = 6 mA	4.5 V	0.17		0.26	
		I_{OL} = 7.8 mA	6 V	0.15		0.26	
I_I	$V_I = V_{CC}$ or 0		6 V	±0.1		±100	nA
I_{OZ}	$V_O = V_{CC}$ or 0		6 V	±0.01		±0.5	µA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0		6 V			8	µA
C_i			2 V to 6 V		3	10	pF

6.6 Electrical Characteristics, SN54HC541

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	2 V	1.9			V
			4.5 V	4.4			
			6 V	5.9			
		I_{OH} = –6 mA	4.5 V	3.7			
		I_{OH} = –7.8 mA	6 V	5.2			

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	2 V			0.1	V
			4.5 V			0.1	
			6 V			0.1	
		I_{OL} = 6 mA	4.5 V			0.4	
		I_{OL} = 7.8 mA	6 V			0.4	
I_I	$V_I = V_{CC}$ or 0		6 V			±1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0		6 V			±10	µA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0		6 V			160	µA
C_i			2 V to 6 V			10	pF

6.7 Electrical Characteristics, SN74HC541

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	2 V	1.9			V
			4.5 V	4.4			
			6 V	5.9			
		I_{OH} = –6 mA	4.5 V	3.84			
		I_{OH} = –7.8 mA	6 V	5.34			
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	2 V			0.1	V
			4.5 V			0.1	
			6 V			0.1	
		I_{OL} = 6 mA	4.5 V			0.33	
		I_{OL} = 7.8 mA	6 V			0.33	
I_I	$V_I = V_{CC}$ or 0		6 V			±1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0		6 V			±5	µA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0		6 V			80	µA
C_i			2 V to 6 V			10	pF

6.8 Switching Characteristics, C_L = 50 pF, T_A = 25°C

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see 図 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	2 V		40	115	ns
			4.5 V		12	23	
			6 V		10	20	
t_{en}	$\overline{OE}$	Y	2 V		80	150	ns
			4.5 V		17	30	
			6 V		15	26	
t_{dis}	$\overline{OE}$	Y	2 V		40	150	ns
			4.5 V		18	30	
			6 V		17	26	
t_t		Y	2 V		28	60	ns
			4.5 V		8	12	
			6 V		6	10	

6.9 Switching Characteristics, C_L = 50 pF, SN54HC541

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see 図 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	2 V			171	ns
			4.5 V			34	
			6 V			29	
t_{en}	$\overline{OE}$	Y	2 V			224	ns
			4.5 V			45	
			6 V			38	
t_{dis}	$\overline{OE}$	Y	2 V			224	ns
			4.5 V			45	
			6 V			38	
t_t		Y	2 V			90	ns
			4.5 V			18	
			6 V			15	

6.10 Switching Characteristics, C_L = 50 pF, SN74HC541

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see 図 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	2 V			144	ns
			4.5 V			29	
			6 V			25	
t_{en}	$\overline{OE}$	Y	2 V			188	ns
			4.5 V			38	
			6 V			32	
t_{dis}	$\overline{OE}$	Y	2 V			188	ns
			4.5 V			38	
			6 V			32	
t_t		Y	2 V			75	ns
			4.5 V			15	
			6 V			13	

6.11 Switching Characteristics, C_L = 150 pF, T_A = 25°C

over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see 図 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	2 V		65	165	ns
			4.5 V		16	33	
			6 V		14	28	
t_{en}	$\overline{OE}$	Y	2 V		100	200	ns
			4.5 V		20	40	
			6 V		17	34	
t_t		Y	2 V		45	210	ns
			4.5 V		17	42	
			6 V		13	36	

6.12 Switching Characteristics, C_L = 150 pF, SN54HC541

over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see 図 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	2 V			246	ns
			4.5 V			49	
			6 V			42	
t_{en}	$\overline{OE}$	Y	2 V			298	ns
			4.5 V			60	
			6 V			51	
t_t		Y	2 V			315	ns
			4.5 V			63	
			6 V			53	

6.13 Switching Characteristics, C_L = 150 pF, SN74HC541

over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see 図 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	2 V			206	ns
			4.5 V			41	
			6 V			35	
t_{en}	$\overline{OE}$	Y	2 V			250	ns
			4.5 V			50	
			6 V			43	
t_t		Y	2 V			265	ns
			4.5 V			53	
			6 V			45	

6.14 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	No load	35	pF

6.15 Typical Characteristics

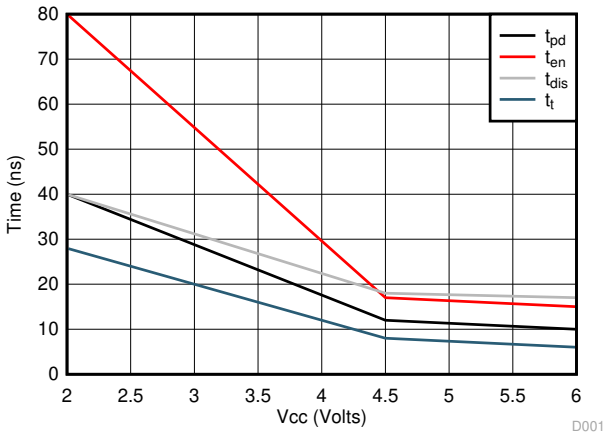


図 6-1. Typical Delay vs. V_{CC} for C_L = 50 pF

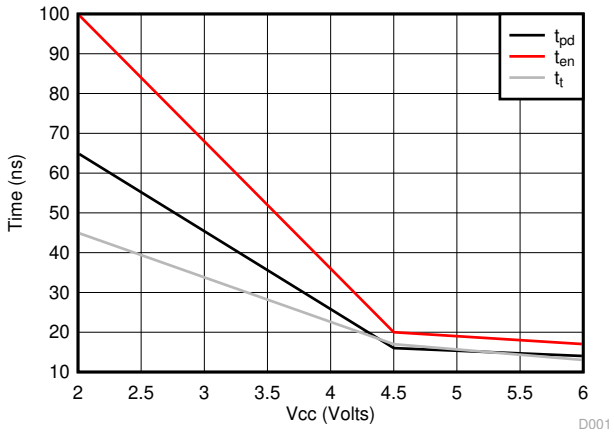
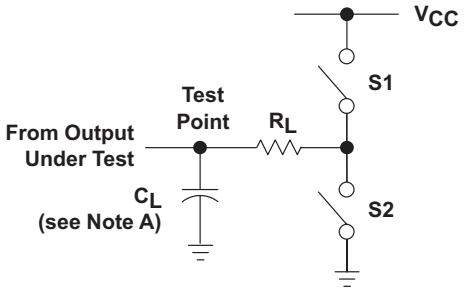


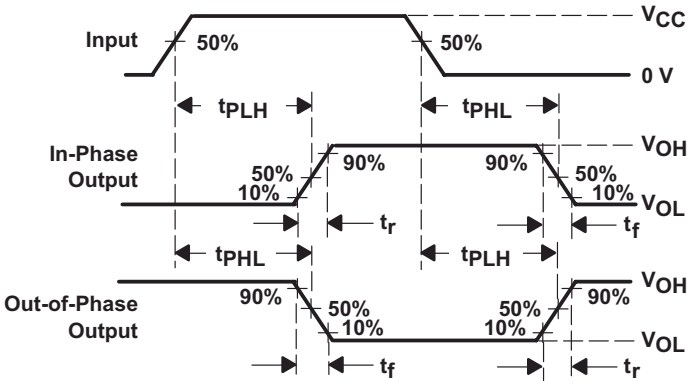
図 6-2. Typical Delay vs. V_{CC} for C_L = 150 pF

7 Parameter Measurement Information

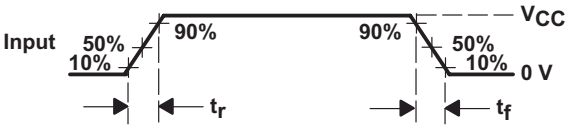


LOAD CIRCUIT

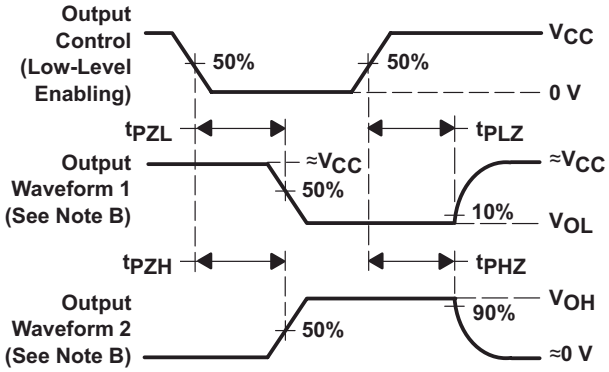
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

図 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74HC541 device has 8 inputs and outputs where data from the A inputs go to the Y outputs. The output enables of the device control whether the information from the A inputs go to the Y outputs. These enable pins cause the device to go into high Z if either $\overline{OE1}$ or $\overline{OE2}$ are high. The $\overline{OE}$s should be tied to V_{CC} through a pull up resistor to ensure the high impedance state during power up or power down; the minimum value of the resistor is determined by the current sinking capability of the driver.

8.2 Functional Block Diagram

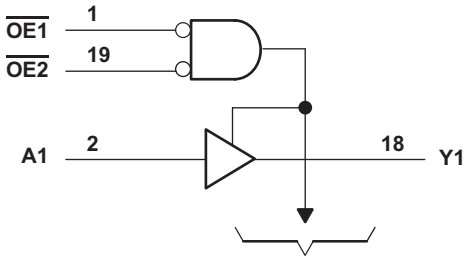


図 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

The SNx4HC541 has a wide operating voltage range of 2 V to 6 V. The device has multiple enable pins, and the device pinout enables simple board layout with outputs across from inputs.

8.4 Device Functional Modes

表 8-1 lists the functional modes of the SNx4HC541.

表 8-1. Function Table (Each Buffer/Driver)

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Hi-Z
X	H	X	Hi-Z

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

SN74HC541 is a wide range CMOS device that can be used over large voltage ranges. The device can be used anywhere from 2 to 6 Volts. The device can drive up to 6 mA of current at 5 Volts. This makes it perfect for driving bus lines directly or up to 15 LSTTL Loads. It can be used to drive anything from micro controllers and system logic devices to LEDs.

9.2 Typical Application

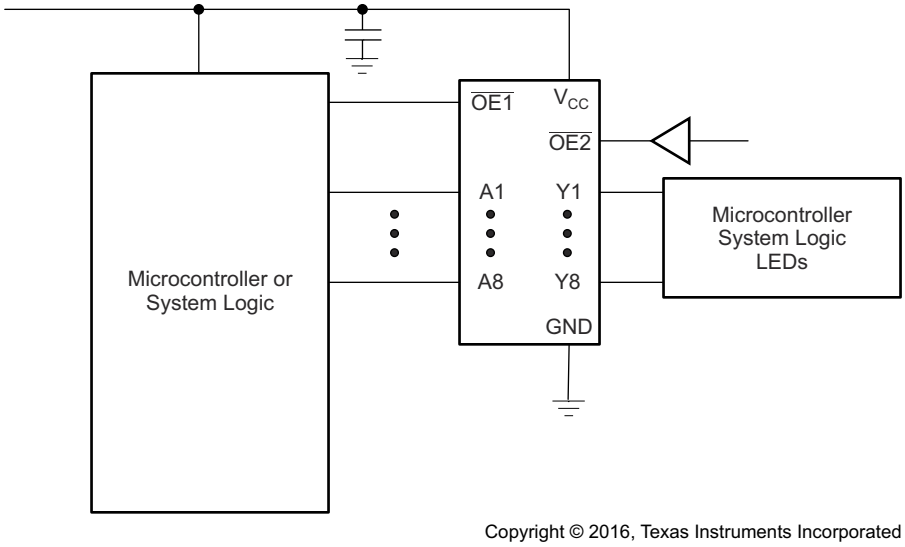


図 9-1. Typical Application Diagram

9.2.1 Design Requirements

This device uses CMOS technology and has a wide voltage range. Take care to avoid pulling too much current from the outputs as to not exceed 6 mA. Also, take care to not go over V_{CC} voltage to avoid damage to the device.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs: See (Δt/ΔV) in the *セクション 6.3* table.
   - Specified high and low levels: See (VIH and VIL) in the *セクション 6.3* table.
   - Inputs should not be pulled above V_{CC}.
2. Recommended Output Conditions
   - Load currents should not exceed 6 mA for the part
   - Outputs should not be pulled above V_{CC}.

9.2.3 Application Curve

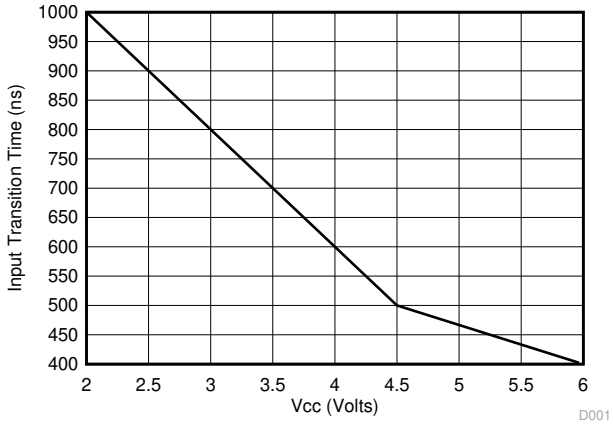


図 9-2. Input Transition Time vs. V_{CC}

10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *セクション 6.3* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1-µF is recommended; if there are multiple V_{CC} pins, then 0.01-µF or 0.022-µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1-µF and a 1-µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. The *セクション 6.3* section specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This does not disable the input section of the I/Os, so they cannot float when disabled.

11.2 Layout Example

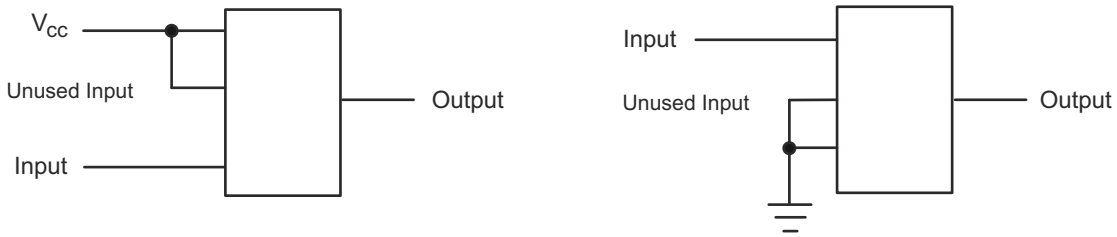


図 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC541	Click here	Click here	Click here	Click here	Click here
SN74HC541	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
JM38510/65711BRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65711BRA
JM38510/65711BRA.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65711BRA
M38510/65711BRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65711BRA
SN54HC541J	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC541J
SN54HC541J.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC541J
SN74HC541DBR	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC541
SN74HC541DBR.A	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC541
SN74HC541DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC541
SN74HC541DWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC541
SN74HC541N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC541N
SN74HC541N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC541N
SN74HC541NE4	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC541N
SN74HC541NSR	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC541
SN74HC541NSR.A	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC541
SN74HC541PW	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 85	HC541
SN74HC541PWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC541
SN74HC541PWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC541
SN74HC541PWT	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 85	HC541
SNJ54HC541FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54HC 541FK
SNJ54HC541FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54HC 541FK
SNJ54HC541J	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54HC541J
SNJ54HC541J.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54HC541J

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC541, SN74HC541 :

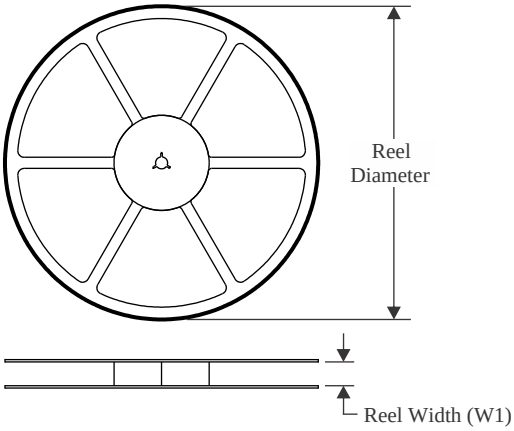
- Catalog : SN74HC541
- Military : SN54HC541

NOTE: Qualified Version Definitions:

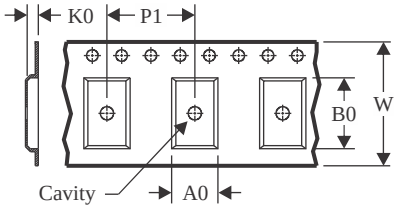
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

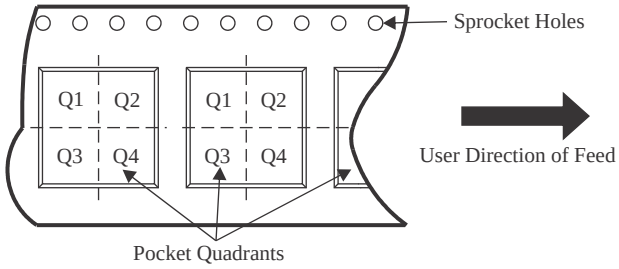


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

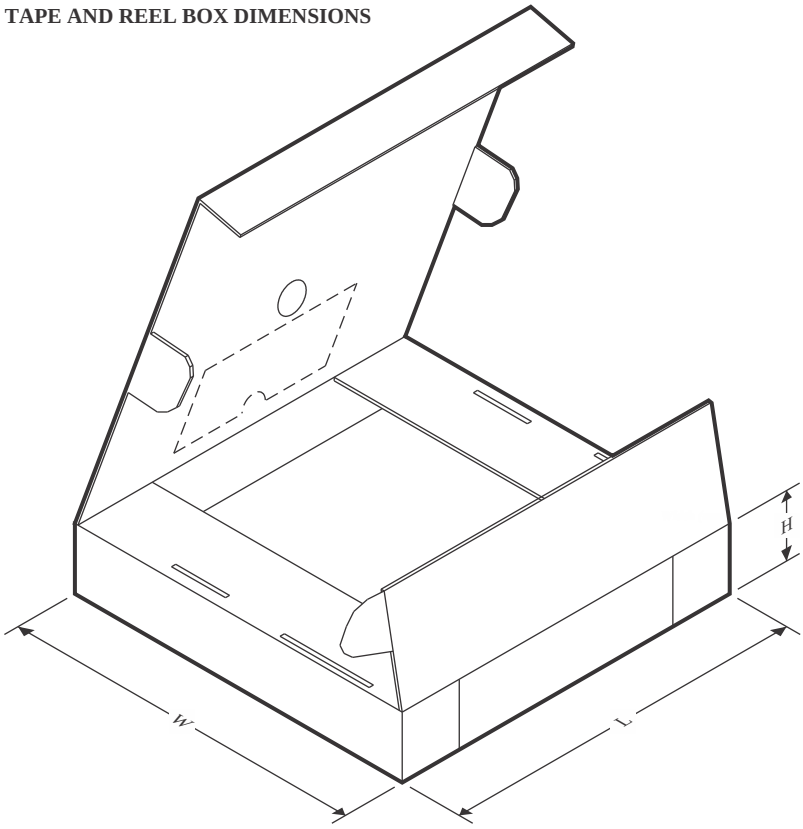
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC541DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HC541DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74HC541NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HC541PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

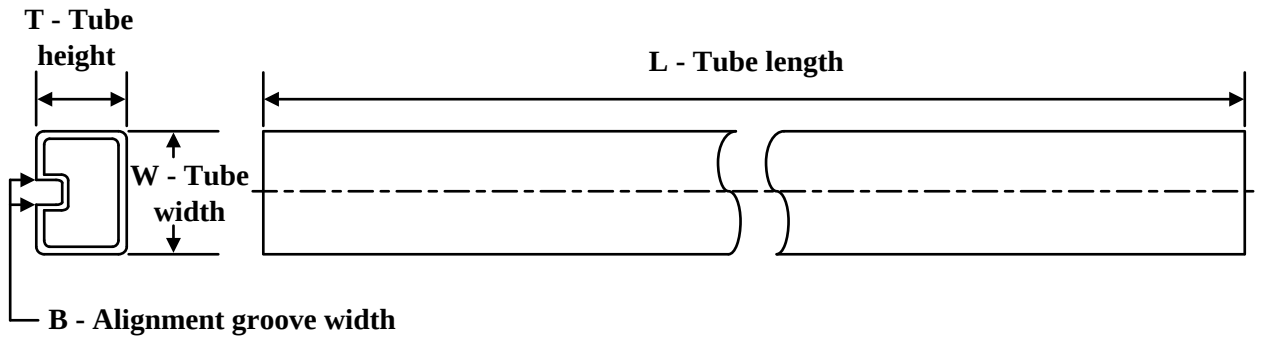
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC541DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74HC541DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74HC541NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74HC541PWR	TSSOP	PW	20	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

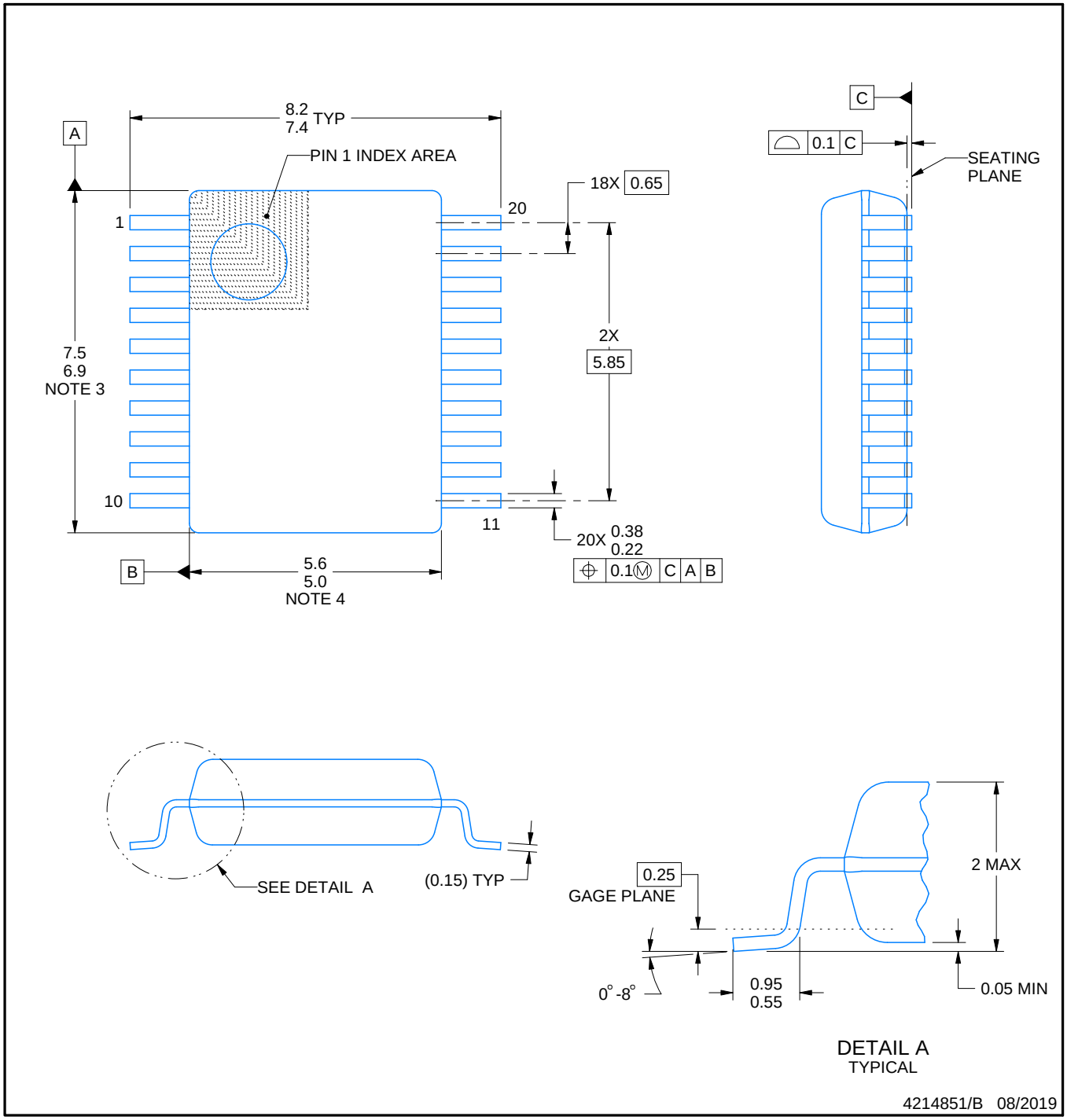
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74HC541N	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC541N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC541NE4	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54HC541FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC541FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

PACKAGE OUTLINE

DB0020A

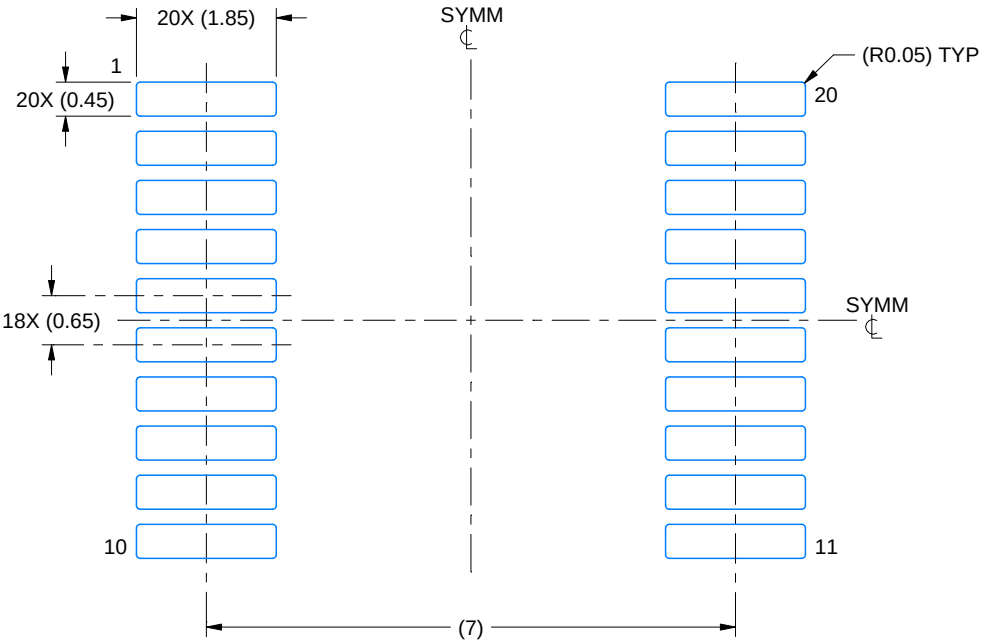
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

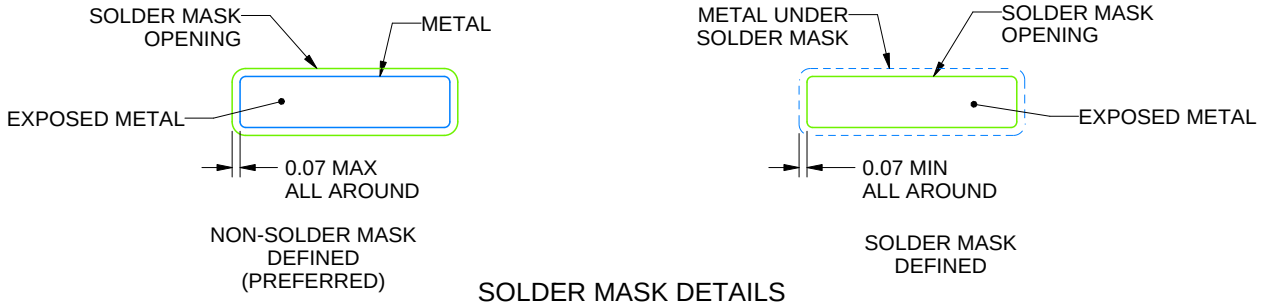


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

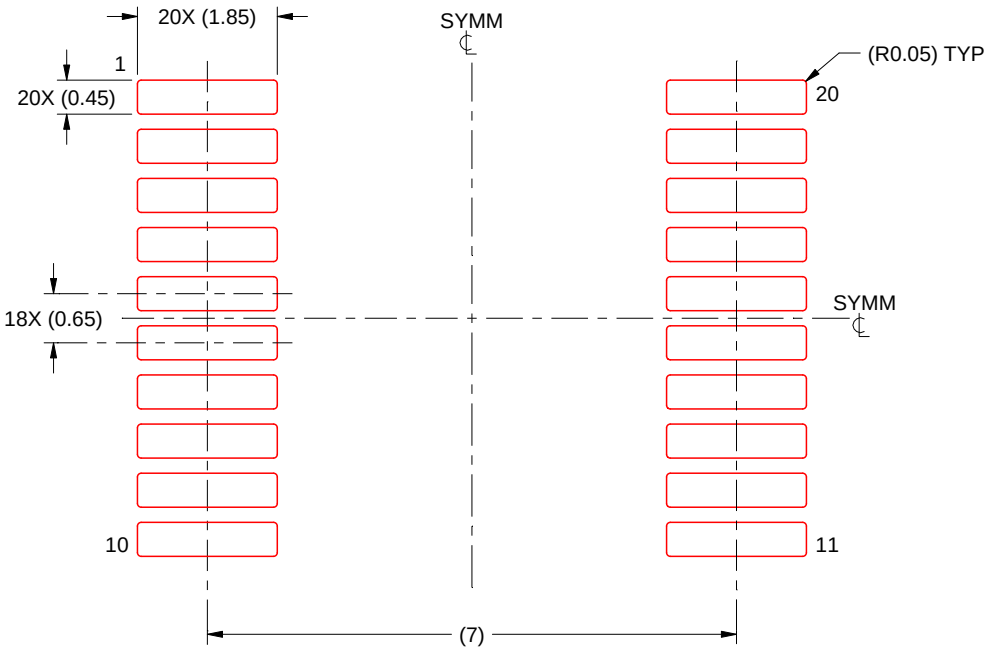
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

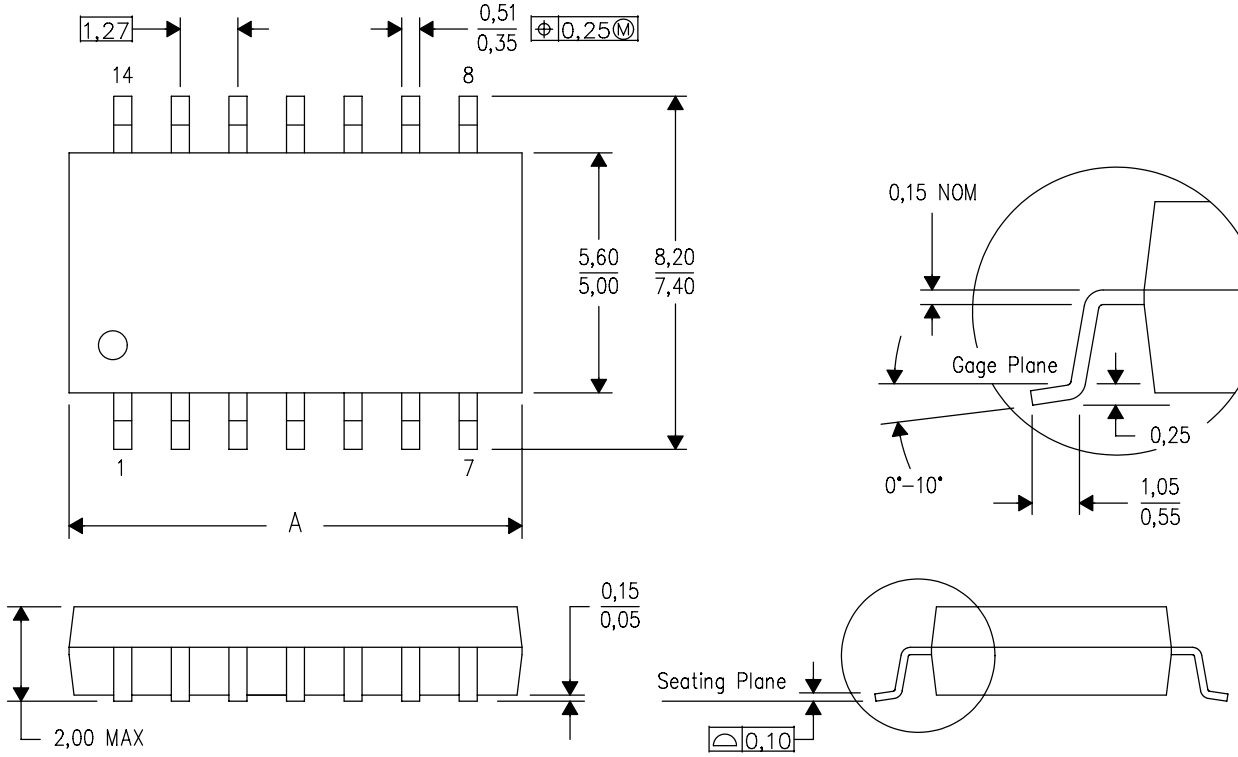
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

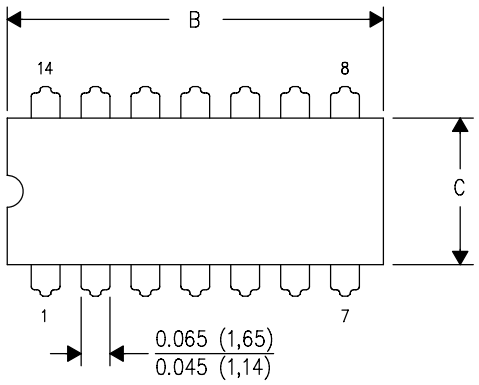
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

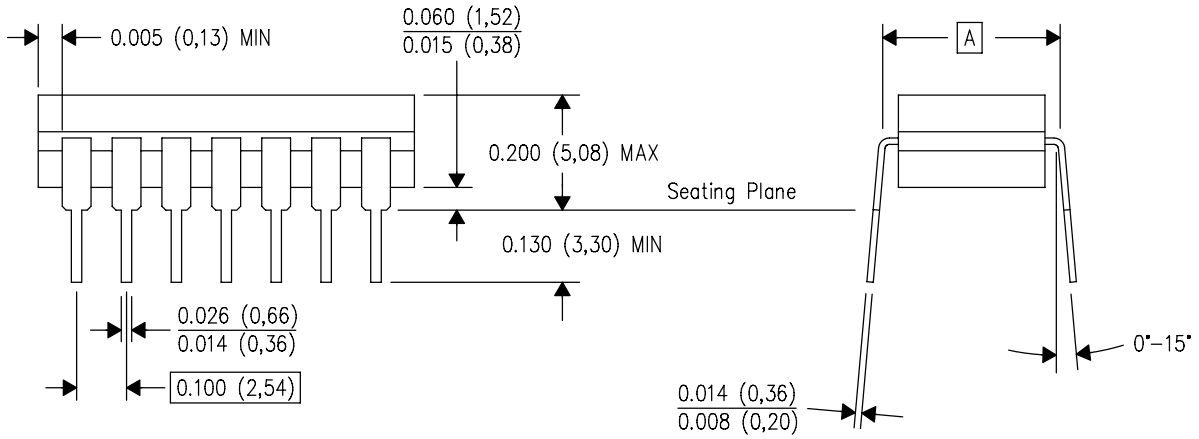
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

GENERIC PACKAGE VIEW

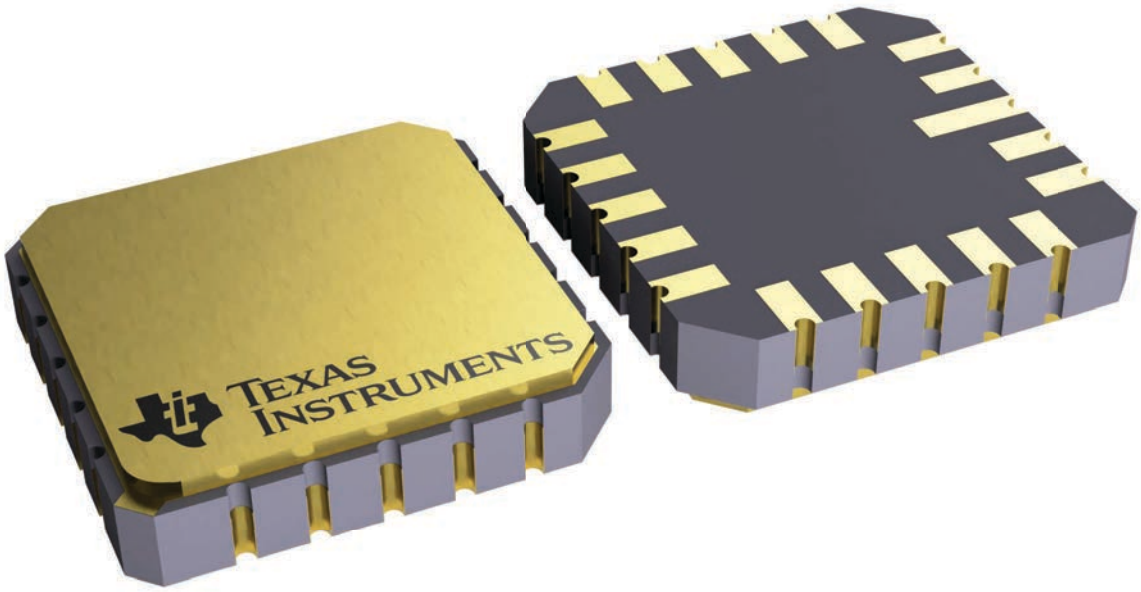
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

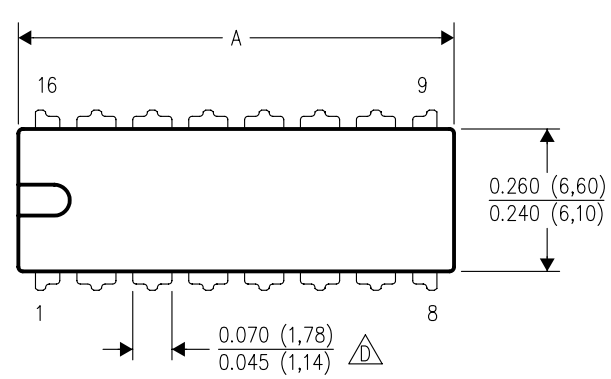


4229370VA\

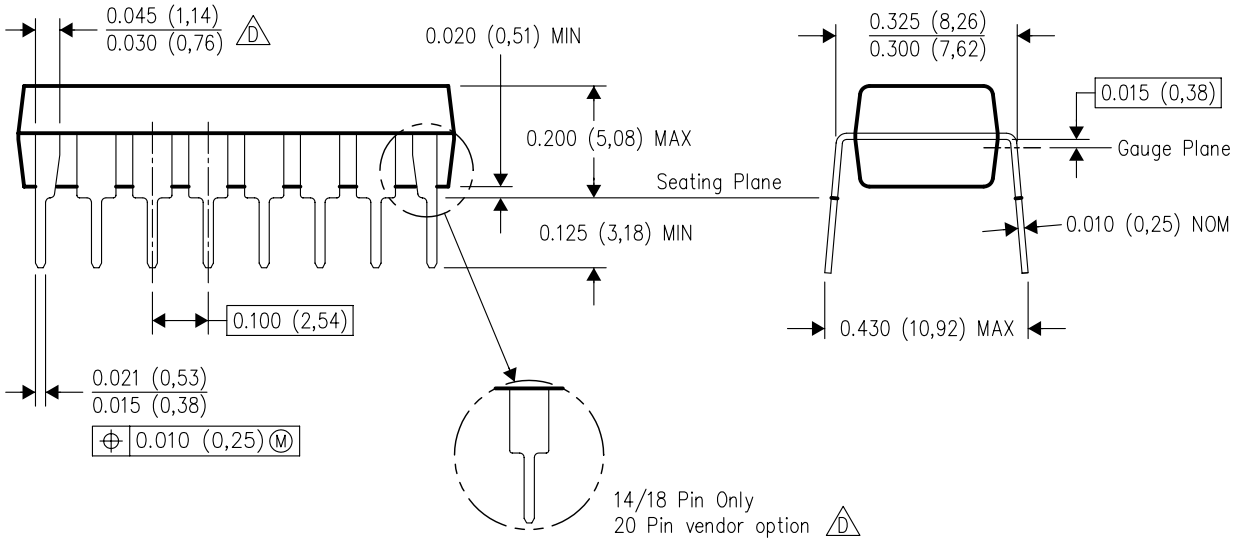
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

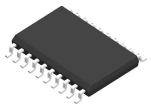


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

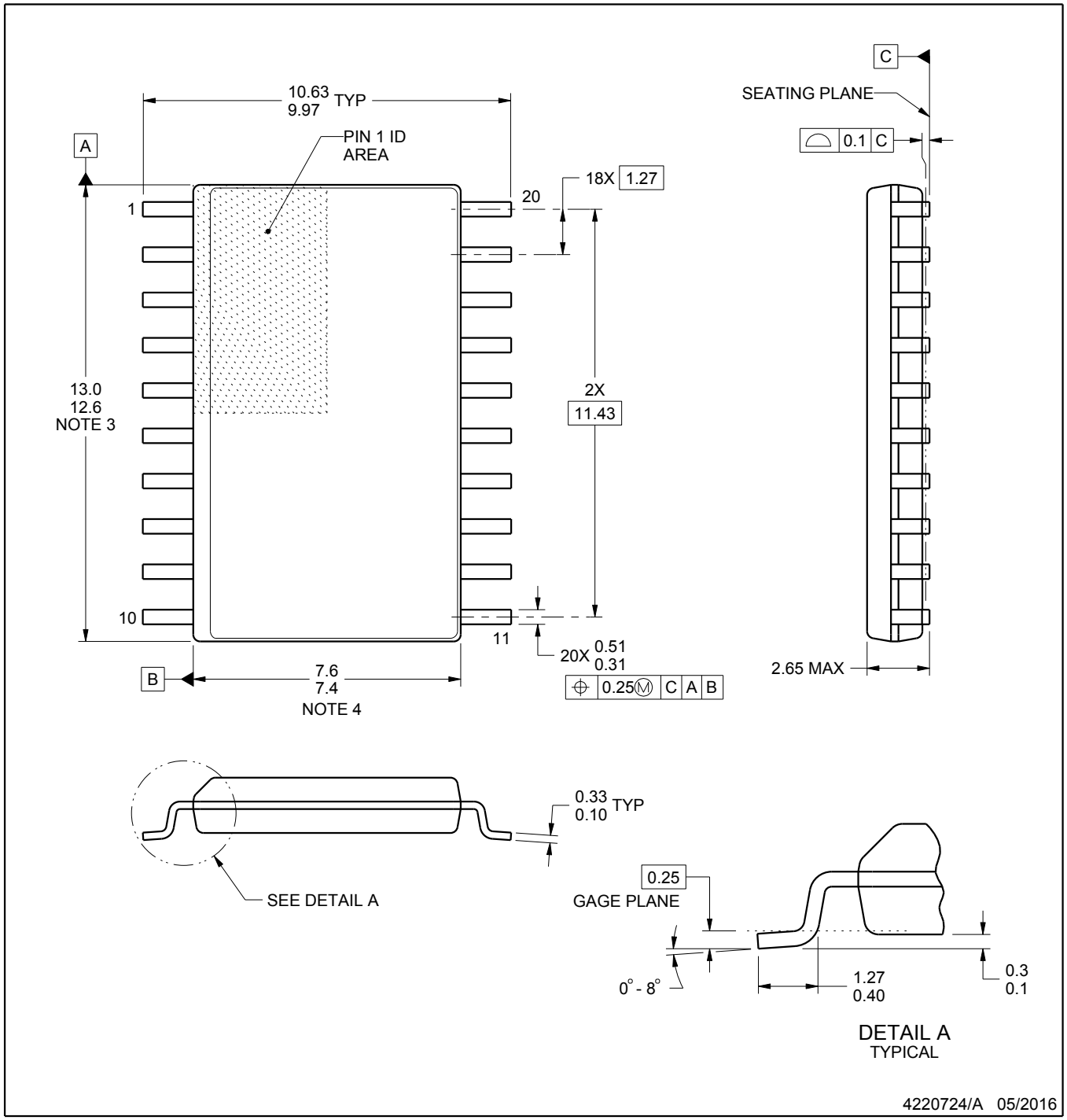


PACKAGE OUTLINE

DW0020A

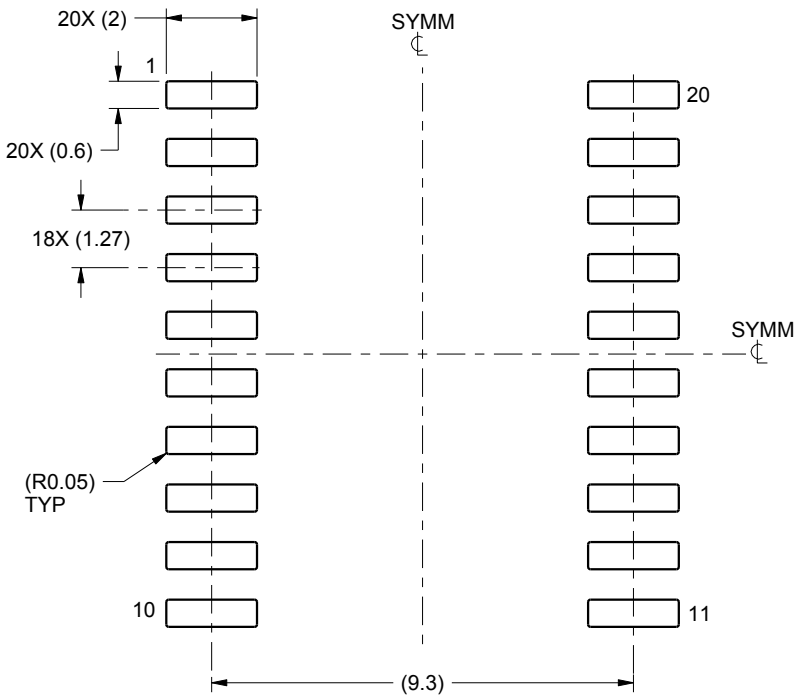
SOIC - 2.65 mm max height

SOIC

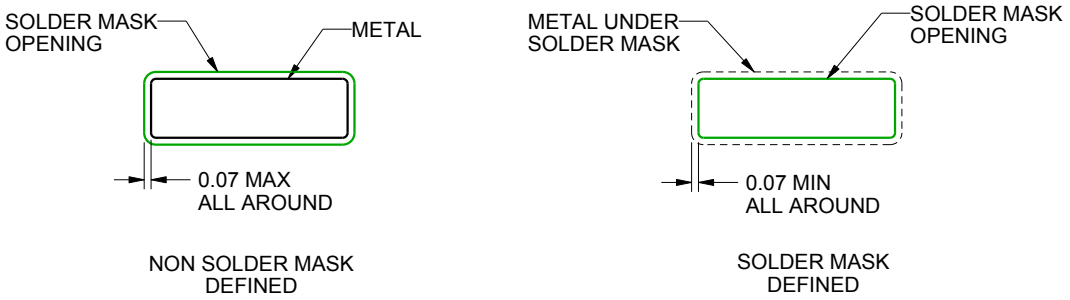


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

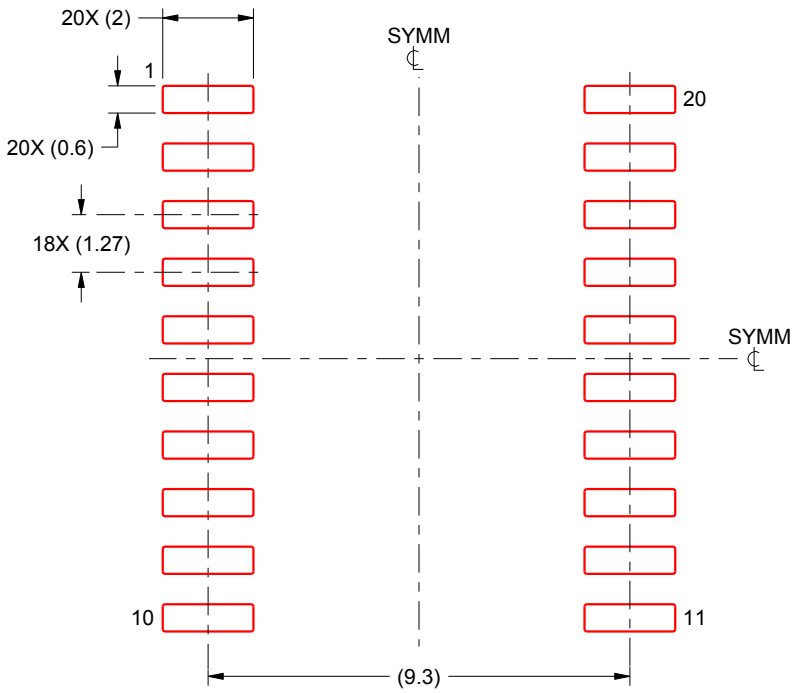


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

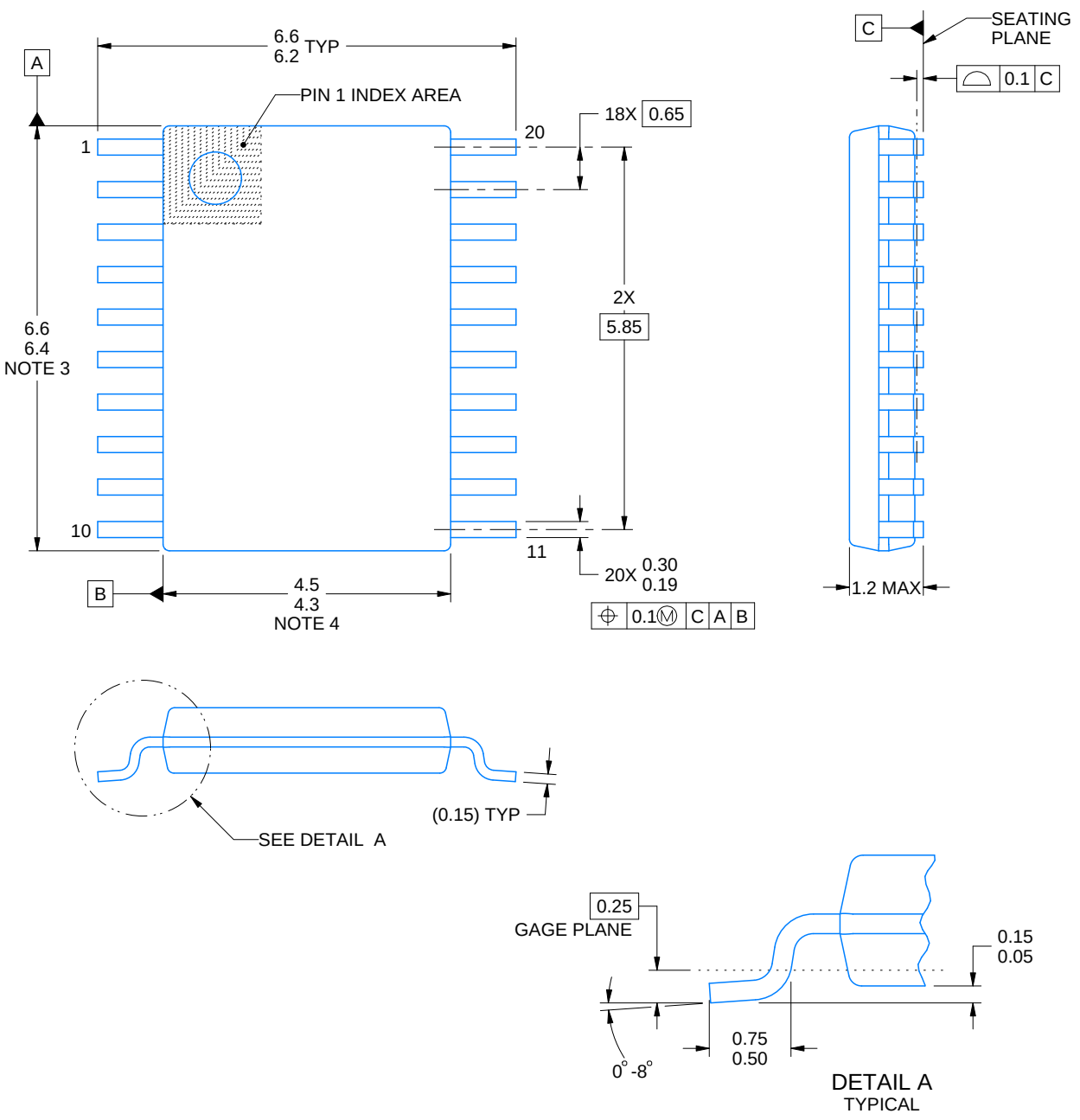
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0020A

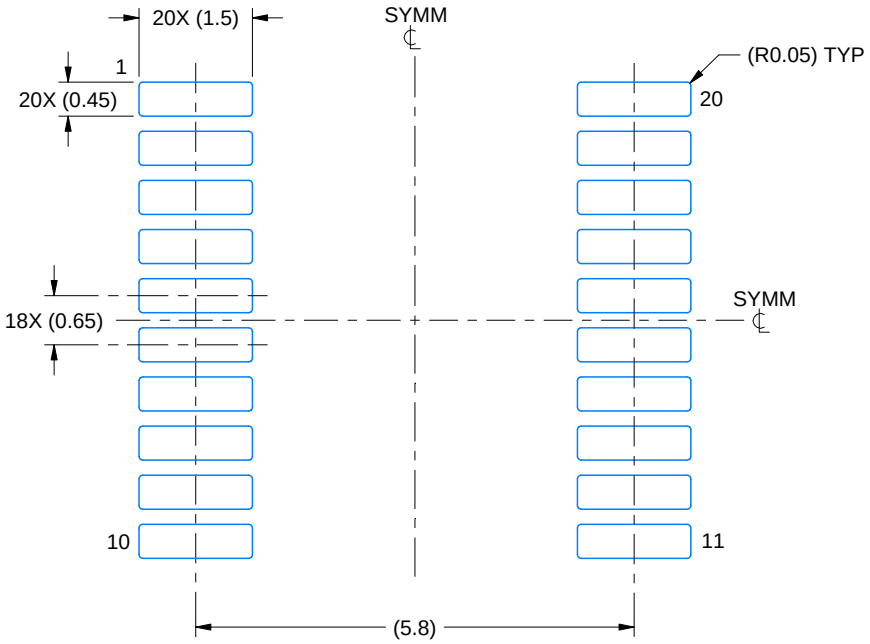
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



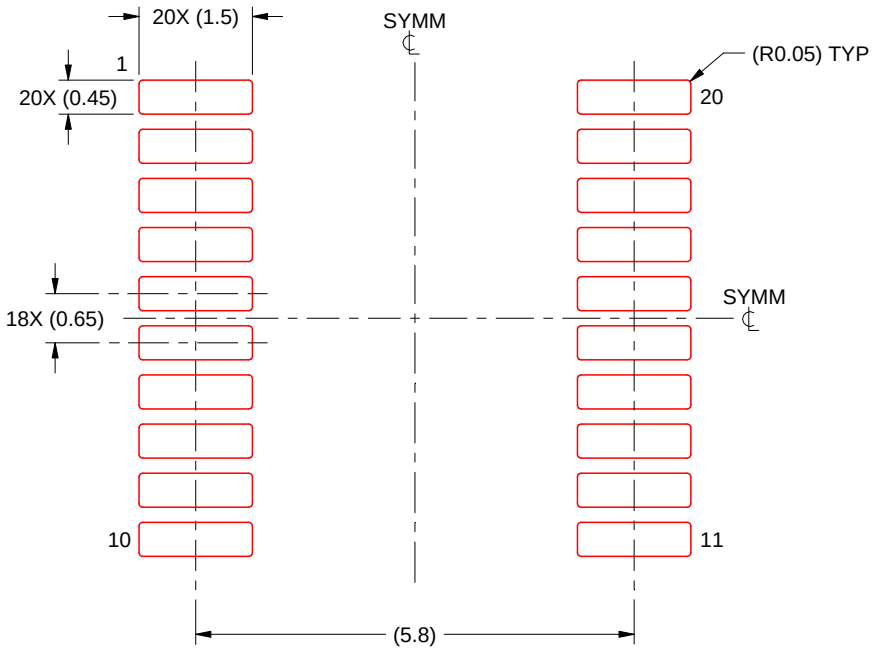
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月