

SNx4LVC257A 3 ステート出力、クワッド、2 ライン入力 1 ライン出力、 データ セレクタ / マルチプレクサ

1 特長

- 1.65V ~ 3.6V で動作
- 5.5V までの入力電圧に対応
- 最大 t_{pd} 4.6ns (3.3V 時)
- V_{OLP} 標準値 (出力グランド バウンス)
<0.8V ($V_{CC} = 3.3V$, $T_A = 25^\circ C$)
- V_{OHV} 標準値 (出力 V_{OH} アンダーシュート)
>2V ($V_{CC} = 3.3V$, $T_A = 25^\circ C$)
- JESD 17 準拠で 250mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護
 - 2000V、人体モデル (A114-A)
 - 200V、マシン モデル (A115-A)
- MIL-PRF-38535 準拠の製品については、特に記述のない限り、すべてのパラメータはテスト済みです。その他のすべての製品については、量産プロセスにすべてのパラメータのテストが含まれているとは限りません。

2 アプリケーション

- ケーブル モデム終端システム
- 試験および測定機器
- I/O エクスパンダ
- モーター ドライバ
- ネットワーク スイッチ
- サーバー
- 通信インフラ

3 概要

この クワッド 2 ライン入力 1 ライン出力、データ セレクタ / マルチプレクサは、1.65V ~ 3.6V の V_{CC} で動作するように設計されています。

SNx4LVC257A デバイスは、バス構成システムで 4 ビットのデータ ソースからの信号を 4 つの出力データ ラインへ多重化するように設計されています。出カインネーブル ($\overline{OE}$) 入力 High ロジック レベルの場合、3 ステート出力はデータ ラインに負荷を印加しません。

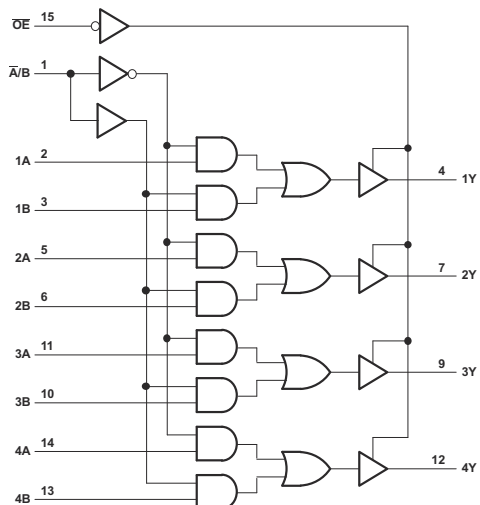
入力は 3.3V または 5V のデバイスから駆動できます。この機能により、3.3V と 5V が混在するシステム環境での変換装置としてこのデバイスを使用できます。

製品情報

部品番号	パッケージ (1)	パッケージ サイズ (2)	本体サイズ (3)
SNx4LVC257A	BQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm
	D (SOIC, 16)	9.90mm × 6mm	9.90mm × 3.90mm
	DB (SSOP, 16)	6.20mm × 7.8mm	6.20mm × 5.30mm
	NS (SOP, 16)	5mm × 6.4mm	5mm × 4.4mm
	PW (TSSOP, 16)	5.00mm × 6.4mm	5.00mm × 4.40mm
	RGY (VQFN, 16)	4mm × 3.5mm	4mm × 3.5mm

- (1) 詳細については、「[メカニカル、パッケージ、および注文情報](#)」を参照してください。
- (2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
- (3) 本体サイズ (長さ × 幅) は公称値であり、ピンは含まれません。





ここに示すピン番号は D、DB、J、NS、PW、RGY、W の各パッケージのものです。

論理図 (正論理)

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4 Pin Configuration and Functions

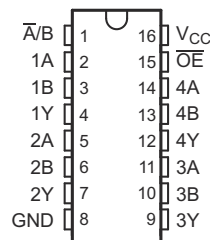


図 4-1. D, DB, NS, J, W, or PW Package; 16-Pin SOIC, SSOP, SO, CDIP, CFP, or TSSOP (Top View)

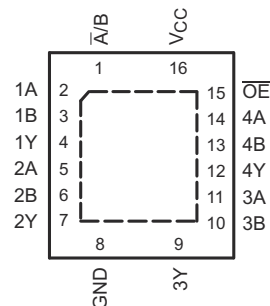


図 4-2. BQB or RGY Package; 16-Pin WQFN or VQFN with Exposed Thermal Pad (Top View)

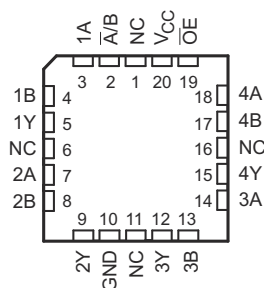


図 4-3. FK Package, 20-Pin LCCC Top View

NAME	PIN		I/O	DESCRIPTION
	SOIC, SSOP, SO, CDIP, CFP, TSSOP, WQFN, or VQFN	LCCC		
A/B	1	2	I	Select Pin, Low selects A, High selects B
1A	2	3	I/O	Multiplexer Signal Input
1B	3	4	I/O	Multiplexer Signal Input
1Y	4	5	I/O	Multiplexer Output
2A	5	7	I/O	Multiplexer Signal Input
2B	6	8	I/O	Multiplexer Signal Input
2Y	7	9	I/O	Multiplexer Output
3A	11	14	I/O	Multiplexer Signal Input
3B	10	13	I/O	Multiplexer Signal Input
3Y	9	12	I/O	Multiplexer Output
4A	14	18	I/O	Multiplexer Signal Input
4B	13	17	I/O	Multiplexer Signal Input
4Y	12	15	I/O	Multiplexer Output
GND	8	10	—	Ground
NC ⁽¹⁾	—	1, 6, 11, 16	—	No connect
OE	15	19	I/O	Active low Output enable
V _{CC}	16	20	—	Power pin

(1) NC – no internal connection

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		−0.5	6.5	V
V _I	Input voltage ⁽²⁾		−0.5	6.5	V
V _O	Output voltage ^{(2) (3)}		−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	−50		mA
I _{OK}	Output clamp current	V _O < 0	−50		mA
I _O	Continuous output current		±50		mA
	Continuous current through V _{CC} or GND		±100		mA
T _{stg}	Storage temperature		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			SN54LVC257A		SN74LVC257A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V			1.7		
		V _{CC} = 2.7 V to 3.6 V	2		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V			0.7		
		V _{CC} = 2.7 V to 3.6 V		0.8		0.8	
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V				−4	mA
		V _{CC} = 2.3 V				−8	
		V _{CC} = 2.7 V		−12		−12	
		V _{CC} = 3 V		−24		−24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V				4	mA
		V _{CC} = 2.3 V				8	
		V _{CC} = 2.7 V		12		12	
		V _{CC} = 3 V		24		24	

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN54LVC257A		SN74LVC257A		UNIT
		MIN	MAX	MIN	MAX	
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVC257A						UNIT
		BQB (WQFN)	D (SOIC)	DB (SSOP)	NS (SO)	PW (TSSOP)	RGY (VQFN)	
		16 PINS						
R _{θJA}	Junction-to-ambient thermal resistance	98.8	118.1	82	64	141.8	87.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC257A			SN74LVC257A			UNIT
			MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
V _{OH}	I _{OH} = −100 μA	1.65 V to 3.6 V				V _{CC} − 0.2			V
	I _{OH} = −100 μA	2.7 V to 3.6 V	V _{CC} − 0.2						
	I _{OH} = −4 mA	1.65 V				1.2			
	I _{OH} = −8 mA	2.3 V				1.7			
	I _{OH} = −12 mA	2.7 V	2.2			2.2			
		3 V	2.4			2.4			
I _{OH} = −24 mA	3 V	2.2			2.2				
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V				0.2			V
		2.7 V to 3.6 V	0.2						
	I _{OL} = 4 mA	1.65 V				0.45			
	I _{OL} = 8 mA	2.3 V				0.7			
	I _{OL} = 12 mA	2.7 V	0.4			0.4			
	I _{OL} = 24 mA	3 V	0.55			0.55			
I _I	V _I = 5.5 V or GND	3.6 V	±5			±5			μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V	±15			±10			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10			10			μA
ΔI _{CC}	One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			500			μA
C _i	V _I = V _{CC} or GND	3.3 V	5			5			pF
C _o	V _O = V _{CC} or GND	3.3 V	5			5			pF

(1) All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

5.6 Switching Characteristics, SN54LVC257A

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC257A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	5.4		1	4.6	ns
	$\overline{A}/B$		7.5		1	6.4	
t _{en}	$\overline{OE}$	Y	6.7		1	5.6	ns
t _{dis}	$\overline{OE}$	Y	4.7		0.5	4.3	ns
t _{sk(o)}					1		ns

5.7 Switching Characteristics, SN74LVC257A

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC257A								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	1	13.5	1	7.4	1	5.4	1	4.6	ns
	$\overline{A}/B$		1	15.6	1	9.5	1	7.5	1	6.4	
t _{en}	$\overline{OE}$	Y	1	14.6	1	8.7	1	6.7	1	5.6	ns
t _{dis}	$\overline{OE}$	Y	1	15.4	1	6.7	1	4.7	1	4.3	ns
t _{sk(o)}									1		ns

5.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance	f = 10 MHz	13.5	14.5	15.5	pF

5.9 Typical Characteristics

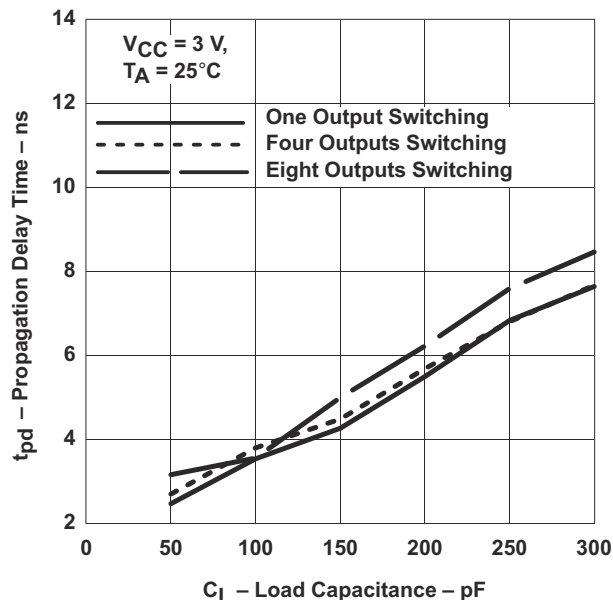


図 5-1. Propagation Delay (Low to High Transition) vs Load Capacitance

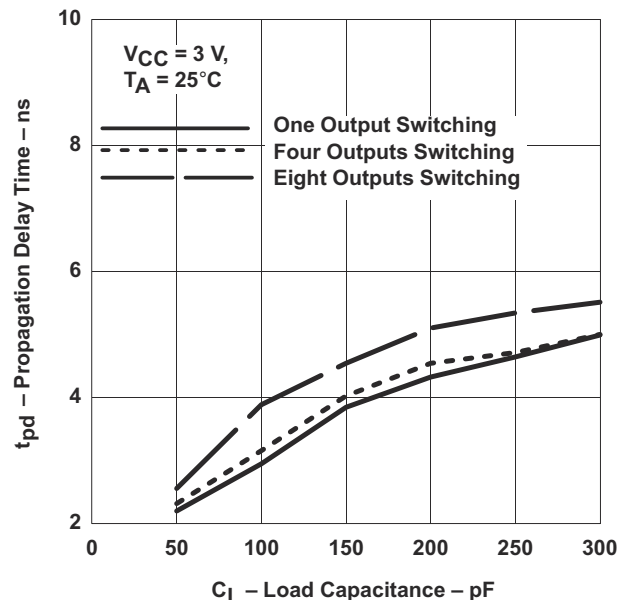
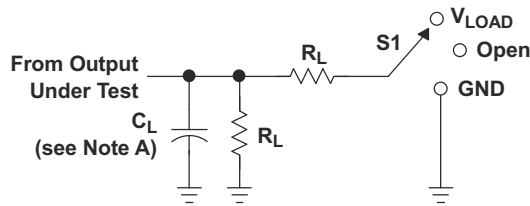


図 5-2. Propagation Delay (High to Low Transition) vs Load Capacitance

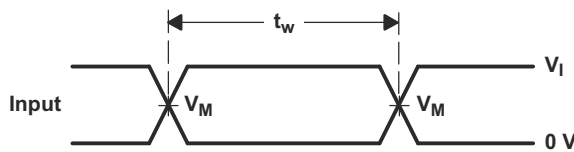
6 Parameter Measurement Information



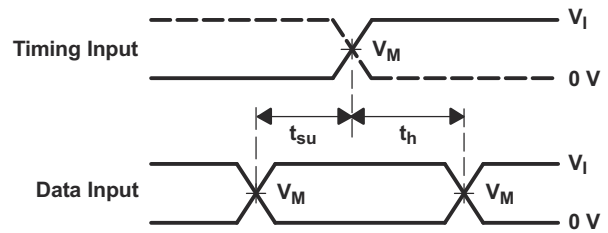
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

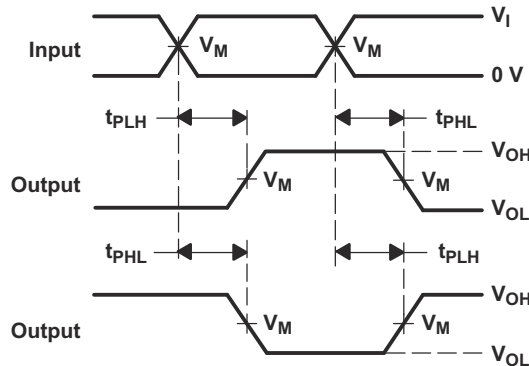
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
1.8 V $\pm$ 0.15 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
2.5 V $\pm$ 0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V $\pm$ 0.3 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



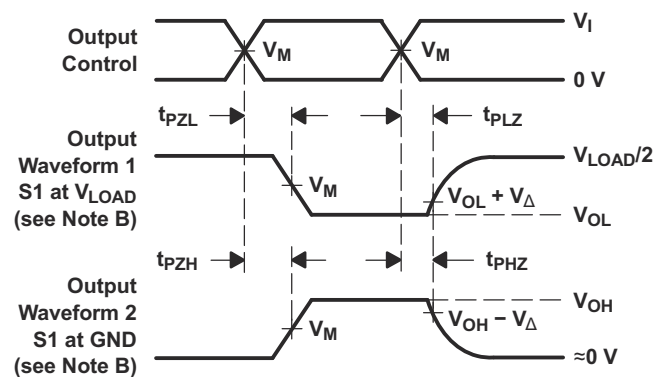
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50 \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

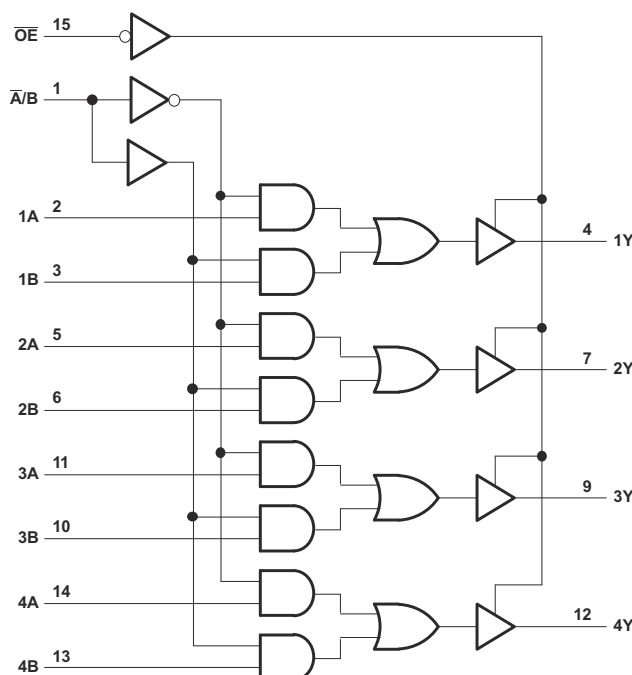
7 Detailed Description

7.1 Overview

These quadruple 2-line to 1-line data selectors and multiplexers are designed for 1.65-V to 3.6-V V_{CC} operation.

The SNx4LVC257A devices are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ($\overline{OE}$) input is at a high logic level.

7.2 Functional Block Diagram



7.3 Feature Description

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V and 5-V system environment. Device features a maximum t_{pd} of 4.6 ns allowing the device to be used in high-speed applications as well.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ must be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.4 Device Functional Modes

表 7-1 lists the functional modes for the SN54LVC257A and SN74LVC257A devices.

表 7-1. Function Table

INPUTS				OUTPUT Y
$\overline{OE}$	$\overline{A/B}$	A	B	
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

1 Application Information

The SNx4LVC257A devices are useful for digital signal data selector or multiplexer applications.

2 Typical Application

The SNx4LVC257A devices use CMOS technology and have balanced output drive. These devices can be used for down level translation and multiplexer function as shown in 図 8-1.

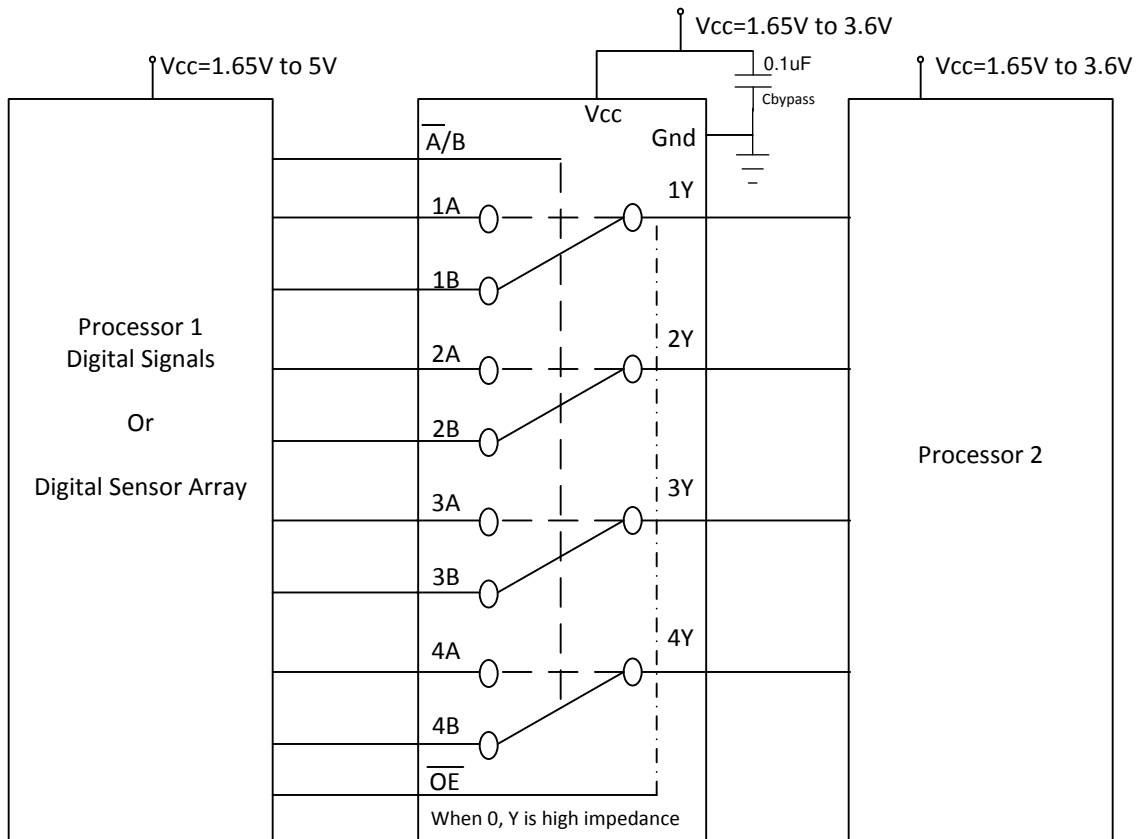


図 8-1. SNx4LVC257A Used as Level Translation and as a Multiplexer

2.1 Design Requirements

Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions must be considered to prevent ringing.

2.2 Detailed Design Procedure

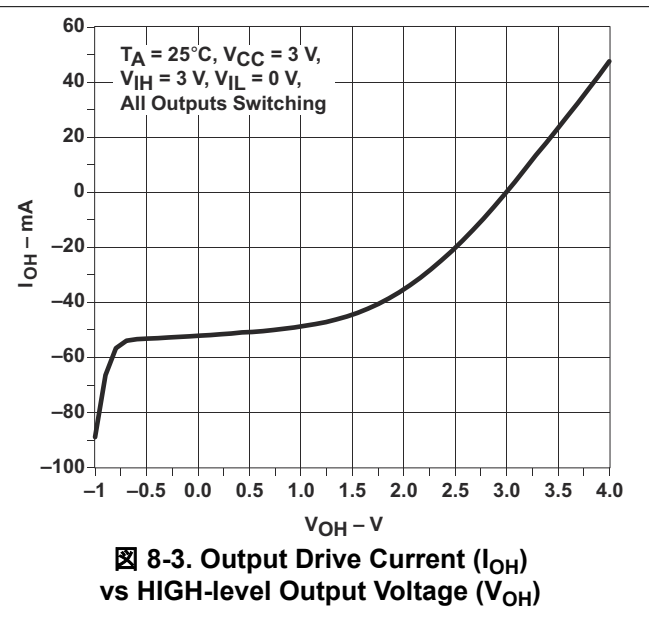
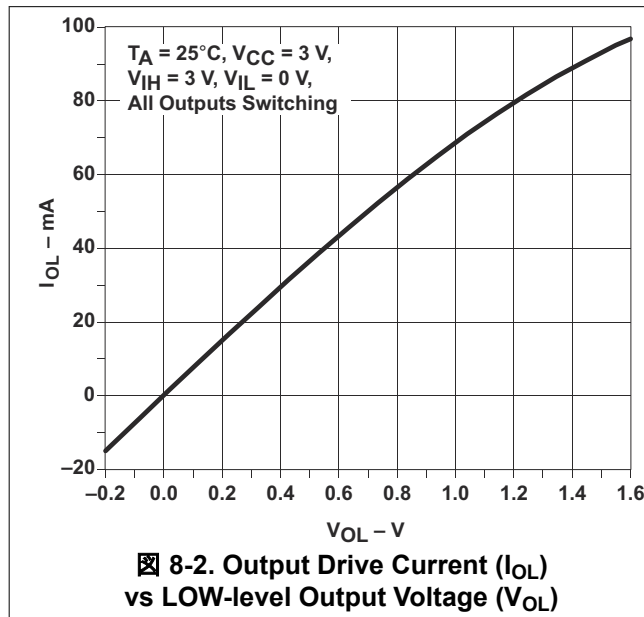
1. Recommended Input Conditions

- For rise time and fall time specification, see $(\Delta t/\Delta V)$ in the [セクション 5.3](#) table.
- For specified high and low levels, see $(V_{IH}$ and $V_{IL})$ in the [セクション 5.3](#) table.
- Inputs are over voltage tolerant allowing them to go as high as $(V_I \text{ max})$ in the [セクション 5.3](#) table at any valid V_{CC} .

2. Recommend Output Conditions

- Load currents must not exceed $(I_O \text{ max})$ per output and must not exceed (continuous current through V_{CC} or GND) total current for the part. These limits are in the [セクション 5.3](#) table.
- Outputs must not be pulled above V_{CC} .

2.3 Application Curves



3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [セクション 5.3](#) table.

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μF capacitor is recommended. If there are multiple V_{CC} terminals then 0.01- μF or 0.022- μF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor must be installed as close to the power terminal as possible for the best results.

4 Layout

4.1 Layout Guidelines

When using multiple bit logic devices, inputs must not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [図 8-4](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be

applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient.

4.2 Layout Example

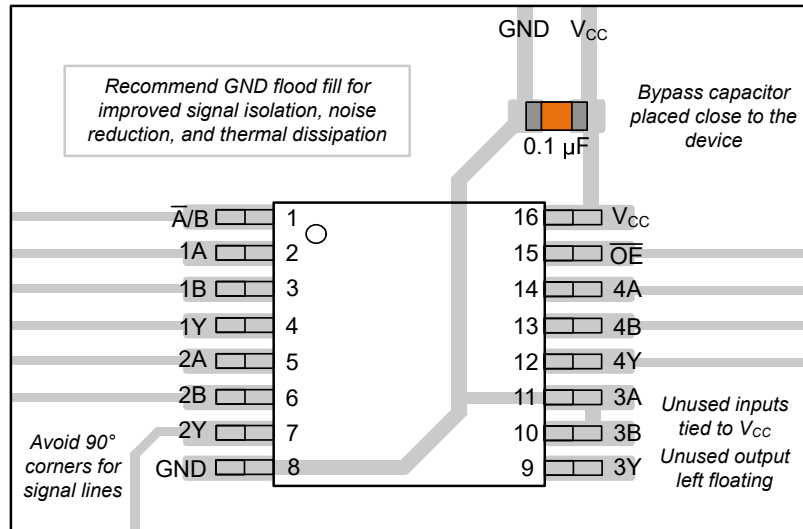


図 8-4. Example Layout for the SN74LVC257A

8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs, [SCBA004](#)

8.1.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LVC257A	Click here	Click here	Click here	Click here	Click here
SN74LVC257A	Click here	Click here	Click here	Click here	Click here

8.2 Community Resources

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

8.5 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

8.6 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.7 用語集

テキサス・インスツルメンツ用語集 この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision P (May 2024) to Revision Q (December 2024)	Page
• Updated R θ JA values: D = 73 to 118.1, PW = 108 to 141.8, RGY = 39 to 87.1; Updated D, PW, and RGY packages for R θ JC(top), R θ JB, Ψ JT, Ψ JB, and R θ JC(bot), all values in °C/W.....	6

Changes from Revision O (June 2015) to Revision P (May 2024)	Page
• 「パッケージ情報」表、「ピン構成および機能」セクション、「熱に関する情報」表に BQA パッケージを追加	1
• 「製品情報」表にパッケージ サイズを追加、「デバイスのオプション」表を削除	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-0050901QFA	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-0050901QF A SNJ54LVC257AW
SN74LVC257ABQBR	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC257A
SN74LVC257ABQBR.A	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC257A
SN74LVC257AD	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A
SN74LVC257AD.B	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A
SN74LVC257ADBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257ADBR.B	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257ADR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A
SN74LVC257ADR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A
SN74LVC257ADR.B	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A
SN74LVC257ADRG4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A
SN74LVC257ANSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A
SN74LVC257ANSR.B	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A
SN74LVC257APW	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257APW.B	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257APWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257APWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257APWR.B	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257APWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257APWRG4.B	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257APWT	Active	Production	TSSOP (PW) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257APWT.B	Active	Production	TSSOP (PW) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A
SN74LVC257ARGYR	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC257A
SN74LVC257ARGYR.A	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC257A
SN74LVC257ARGYR.B	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC257A
SNJ54LVC257AW	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-0050901QF A SNJ54LVC257AW

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

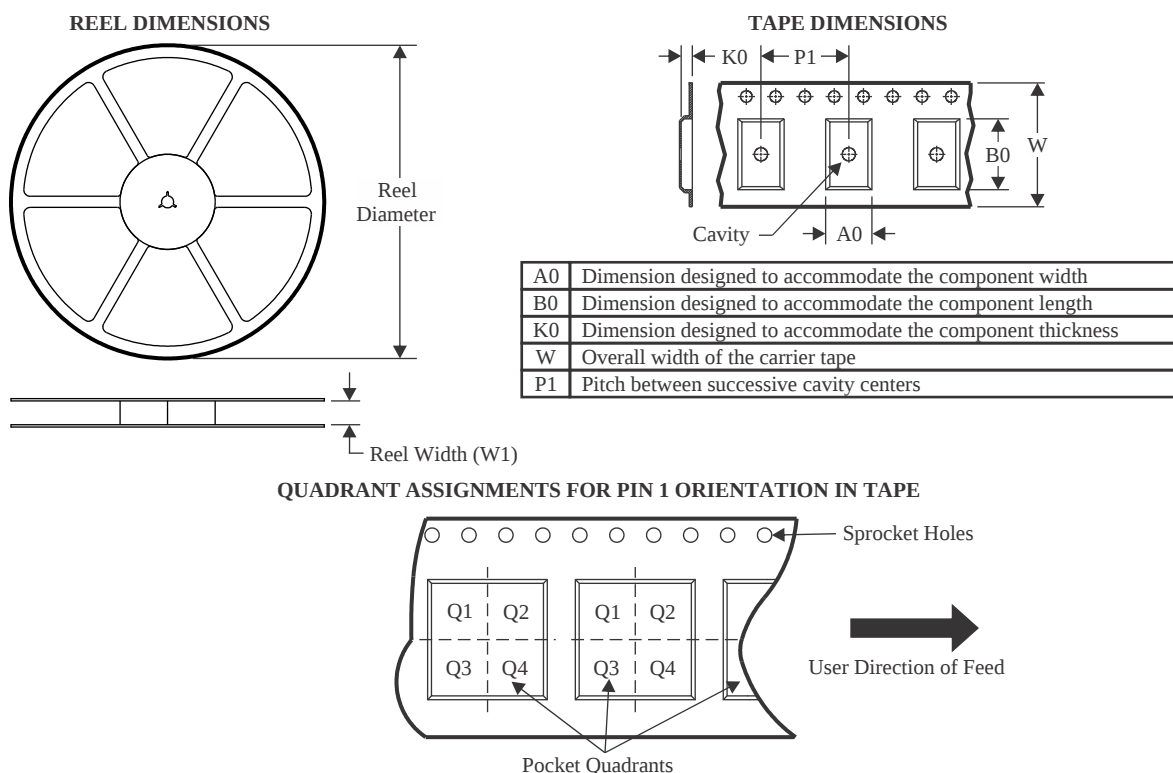
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LVC257A, SN74LVC257A :

- Catalog : [SN74LVC257A](#)
- Automotive : [SN74LVC257A-Q1](#), [SN74LVC257A-Q1](#)
- Enhanced Product : [SN74LVC257A-EP](#), [SN74LVC257A-EP](#)
- Military : [SN54LVC257A](#)

NOTE: Qualified Version Definitions:

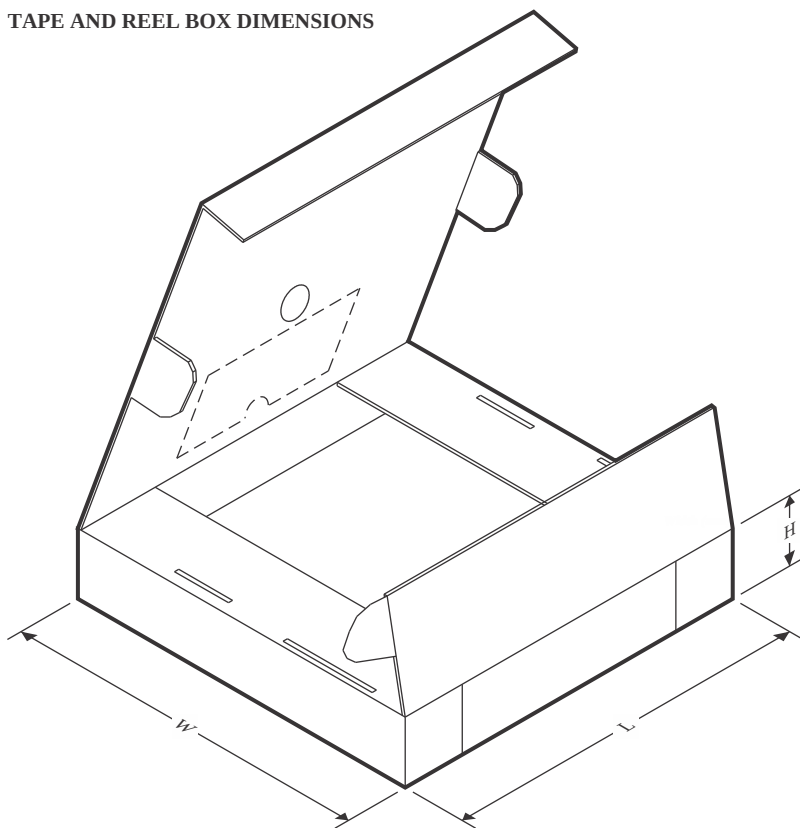
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC257ABQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
SN74LVC257ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC257ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LVC257ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LVC257ANSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LVC257APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC257APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC257APWR	TSSOP	PW	16	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
SN74LVC257APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC257APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC257APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC257ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN74LVC257ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



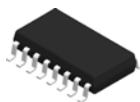
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC257ABQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
SN74LVC257ADBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74LVC257ADR	SOIC	D	16	2500	353.0	353.0	32.0
SN74LVC257ADR	SOIC	D	16	2500	353.0	353.0	32.0
SN74LVC257ANSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74LVC257APWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74LVC257APWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74LVC257APWR	TSSOP	PW	16	2000	366.0	364.0	50.0
SN74LVC257APWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74LVC257APWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74LVC257APWT	TSSOP	PW	16	250	353.0	353.0	32.0
SN74LVC257ARGYR	VQFN	RGY	16	3000	353.0	353.0	32.0
SN74LVC257ARGYR	VQFN	RGY	16	3000	360.0	360.0	36.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-0050901QFA	W	CFP	16	25	506.98	26.16	6220	NA
SN74LVC257AD	D	SOIC	16	40	507	8	3940	4.32
SN74LVC257AD.B	D	SOIC	16	40	507	8	3940	4.32
SN74LVC257APW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74LVC257APW.B	PW	TSSOP	16	90	530	10.2	3600	3.5
SNJ54LVC257AW	W	CFP	16	25	506.98	26.16	6220	NA

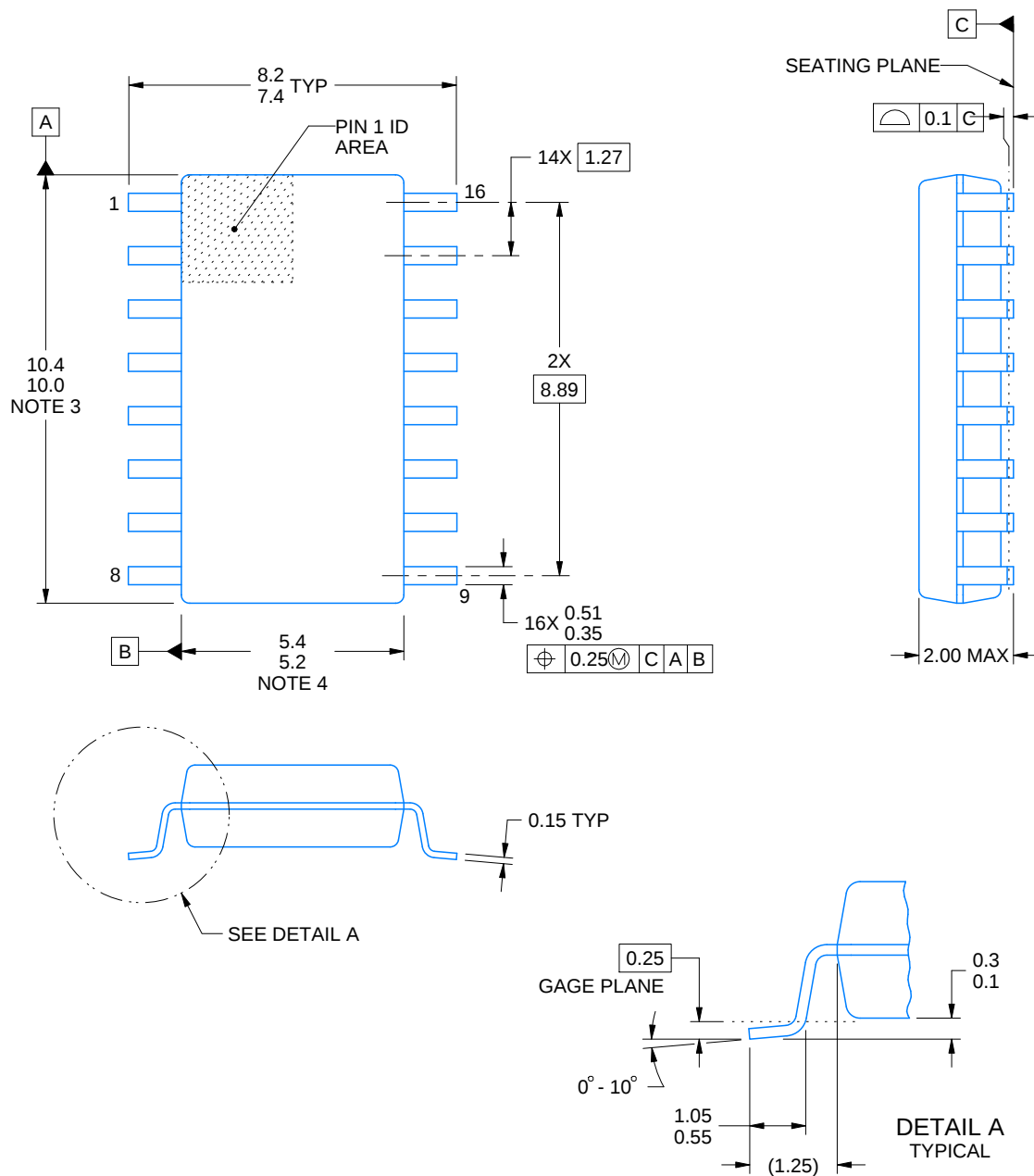


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

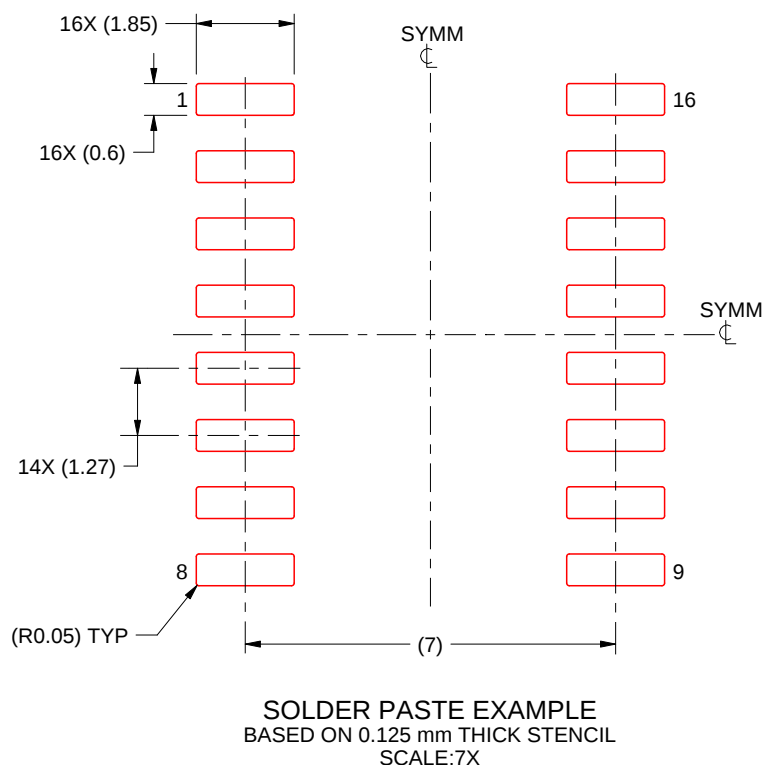
SOP



4220735/A 12/2021

NOTES:

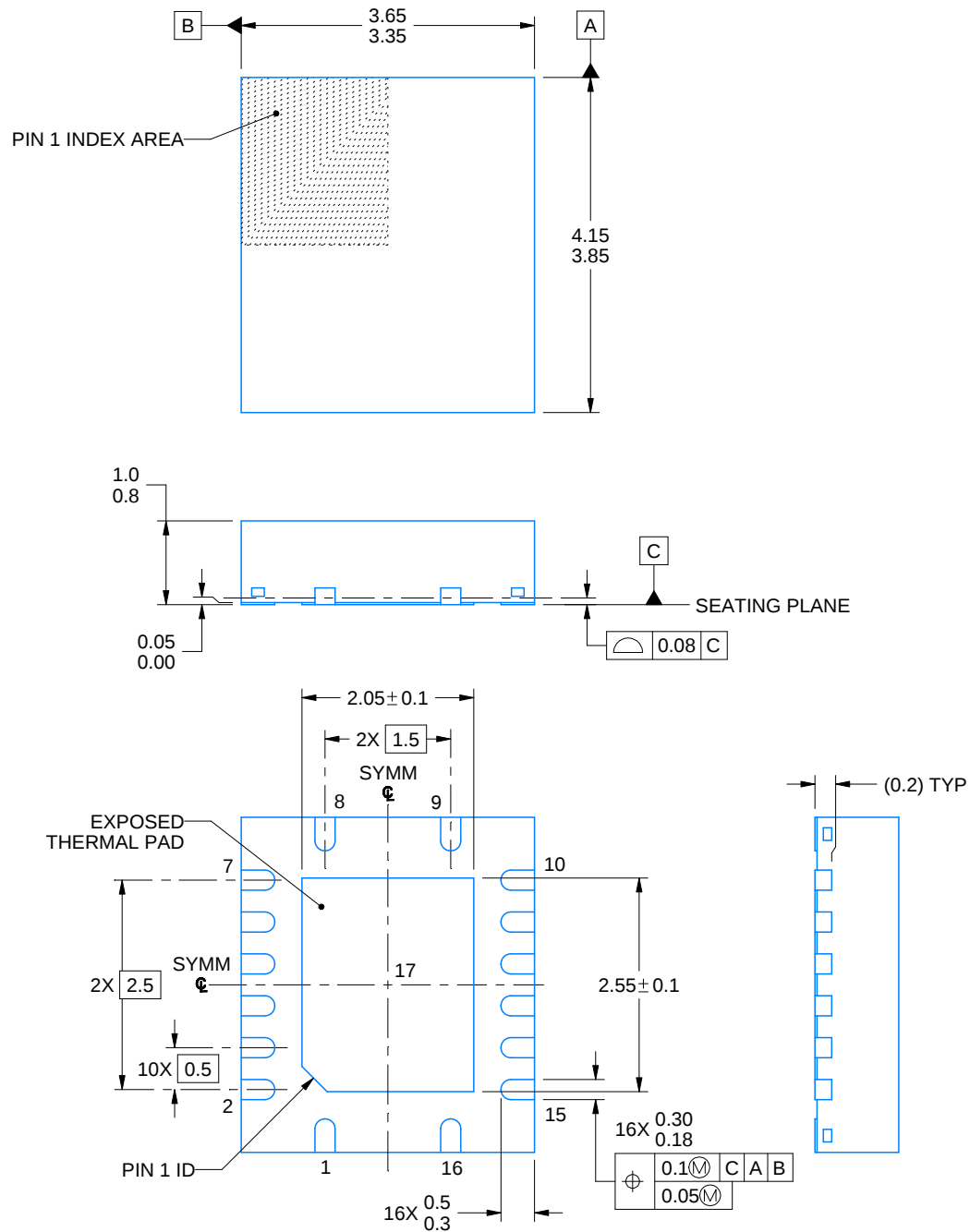
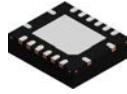
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4225140/A 07/2019

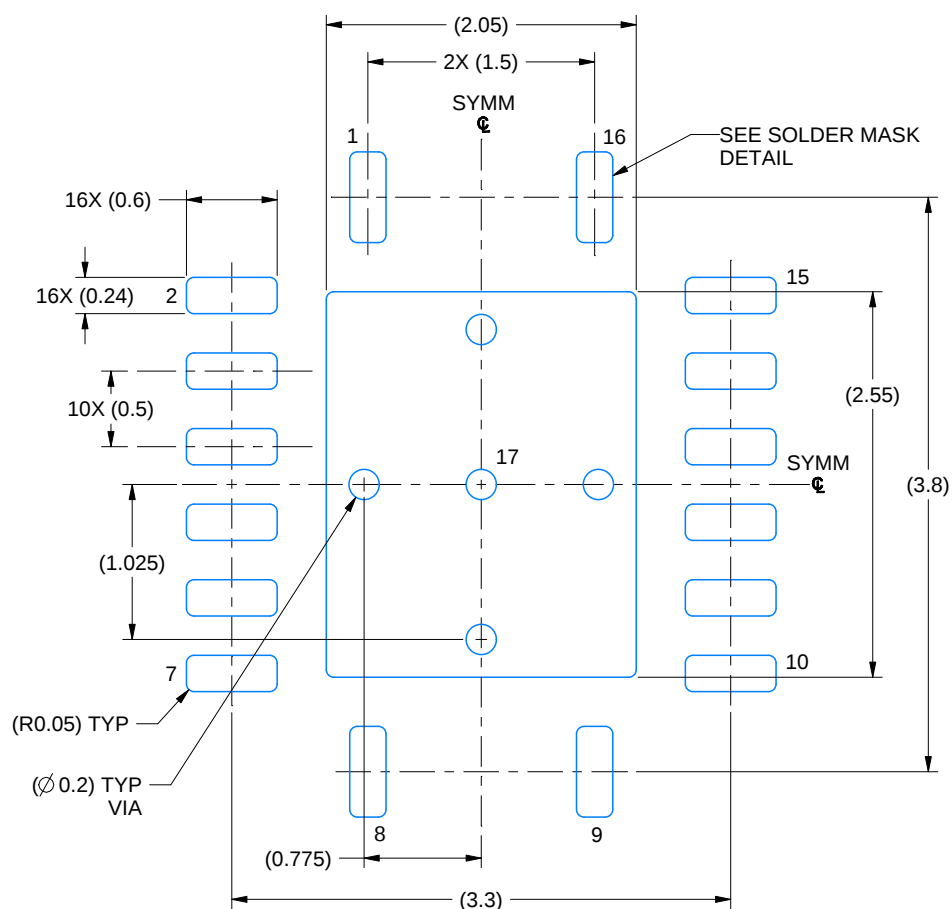
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

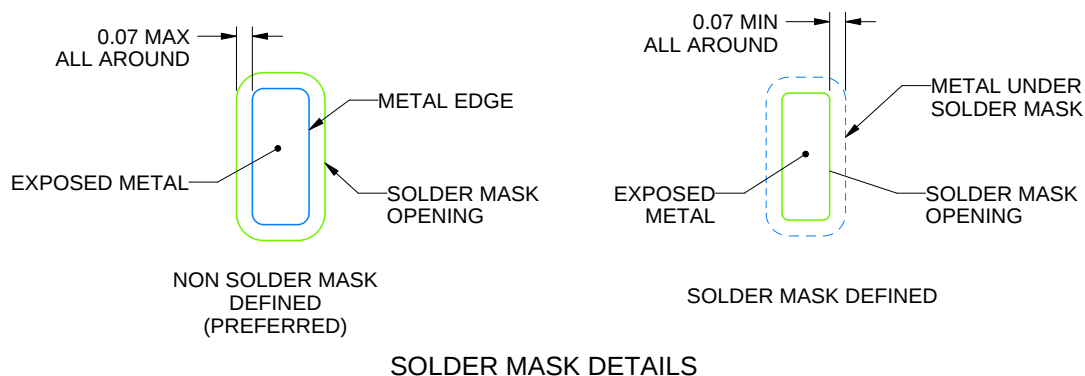
RGY0016A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4225140/A 07/2019

NOTES: (continued)

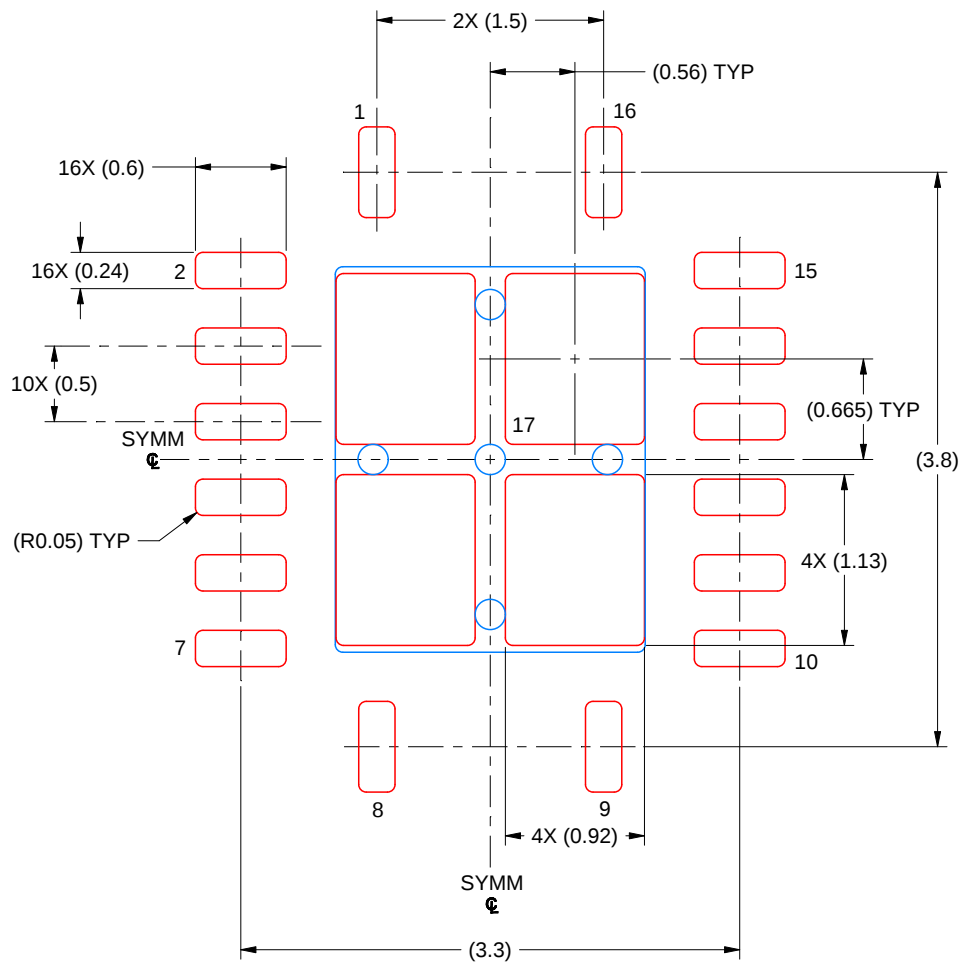
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGY0016A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

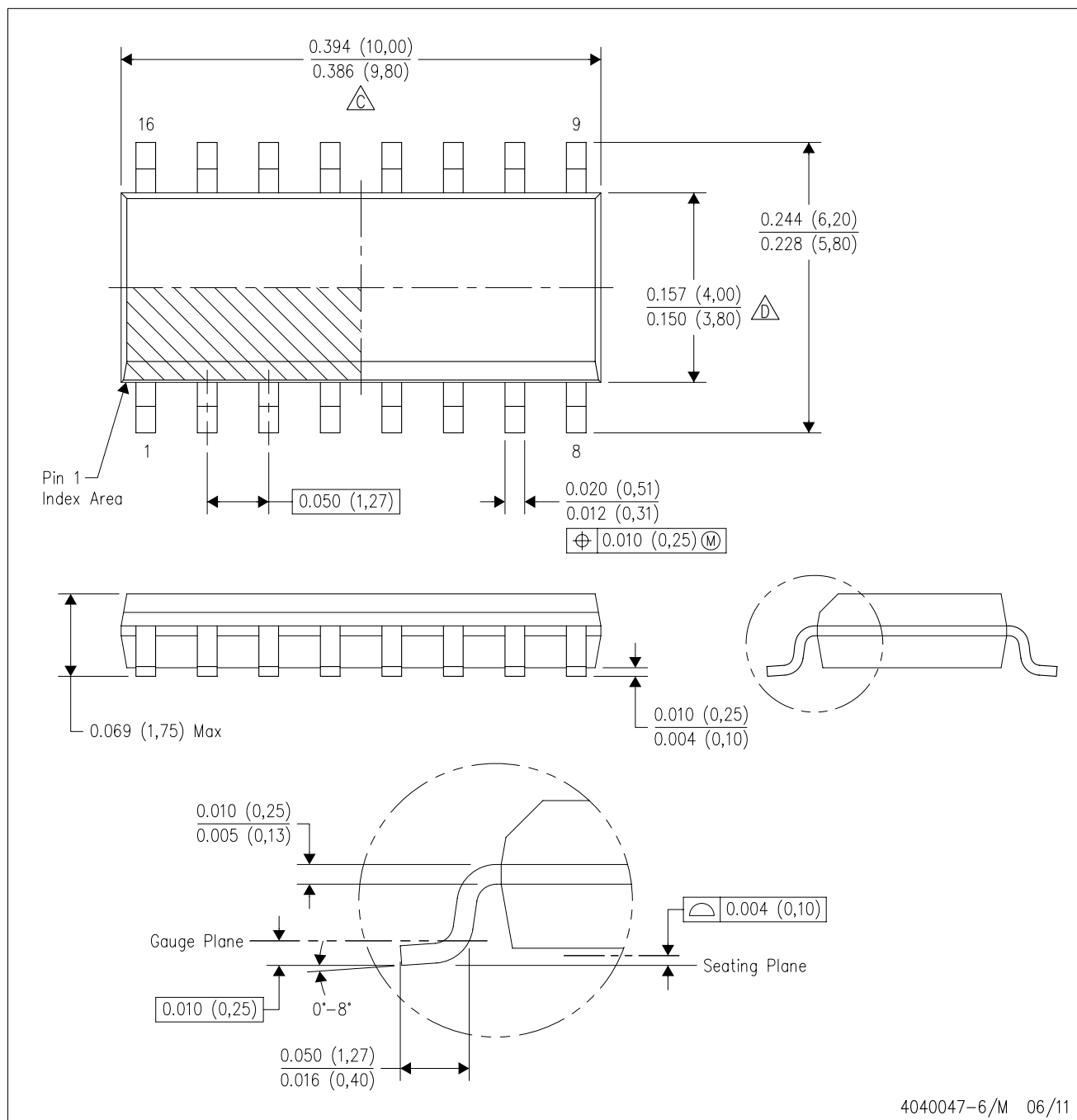
4225140/A 07/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

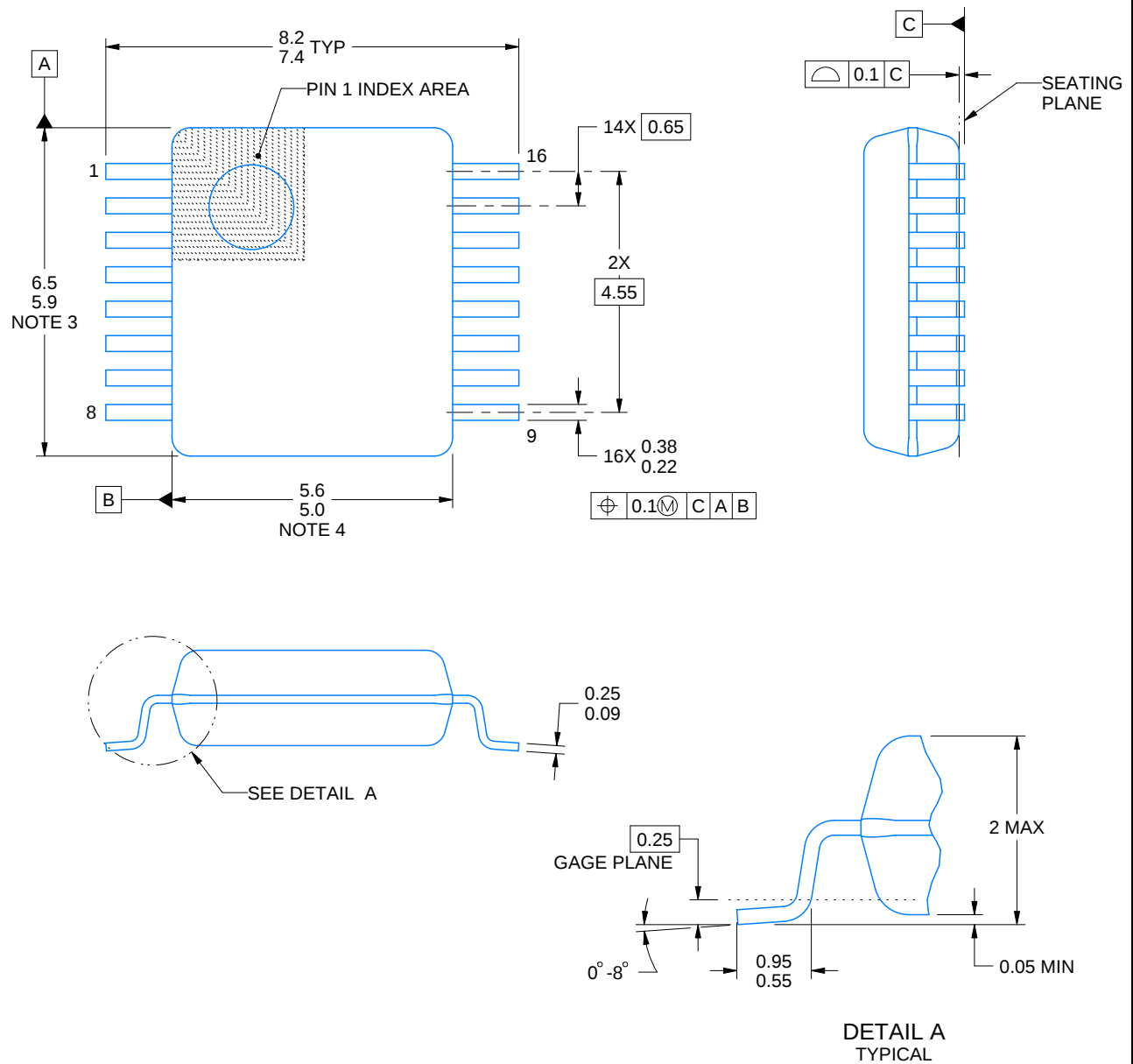
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



4220763/A 05/2022

NOTES:

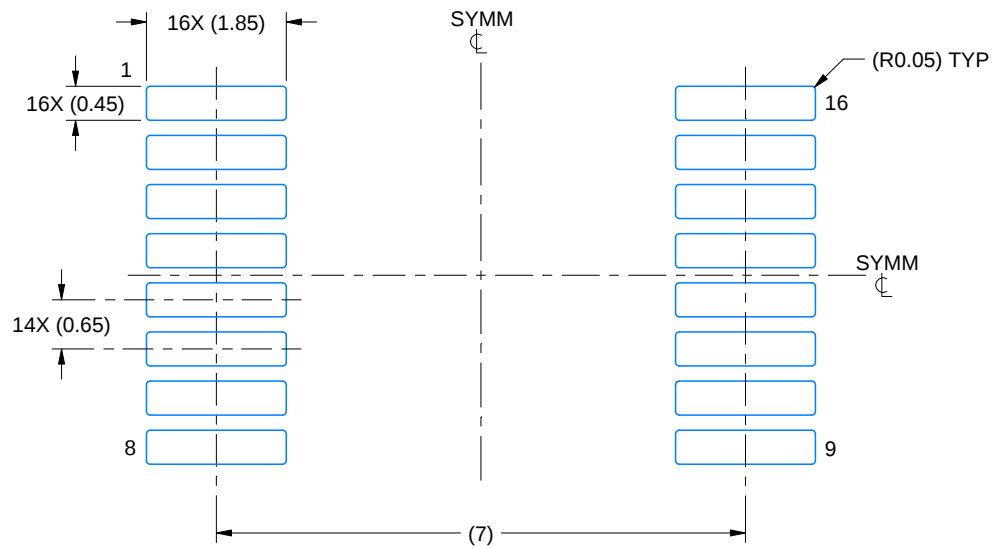
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

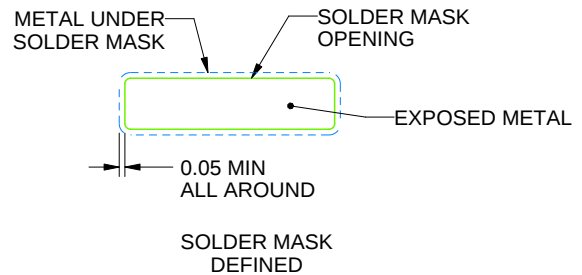
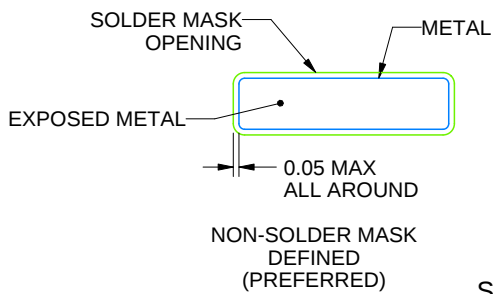
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

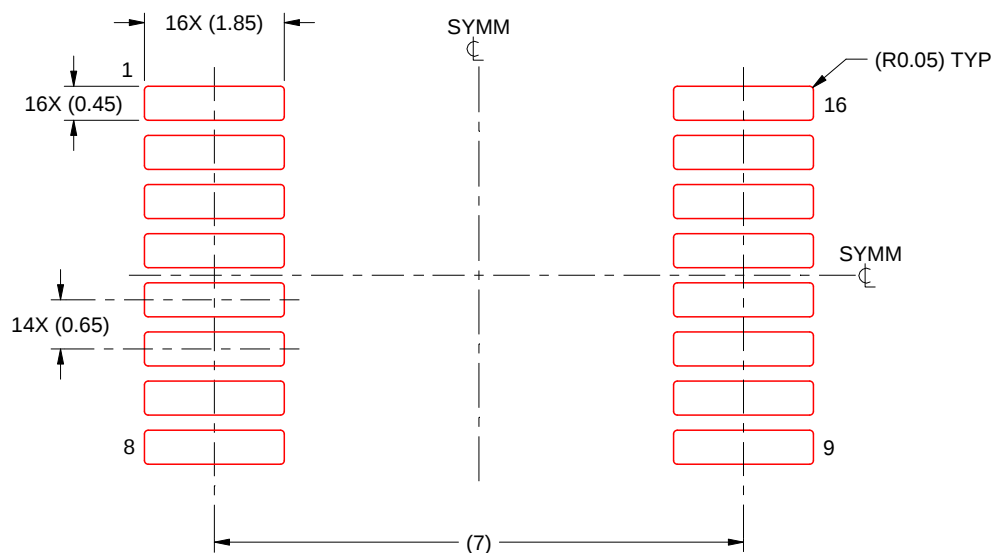
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

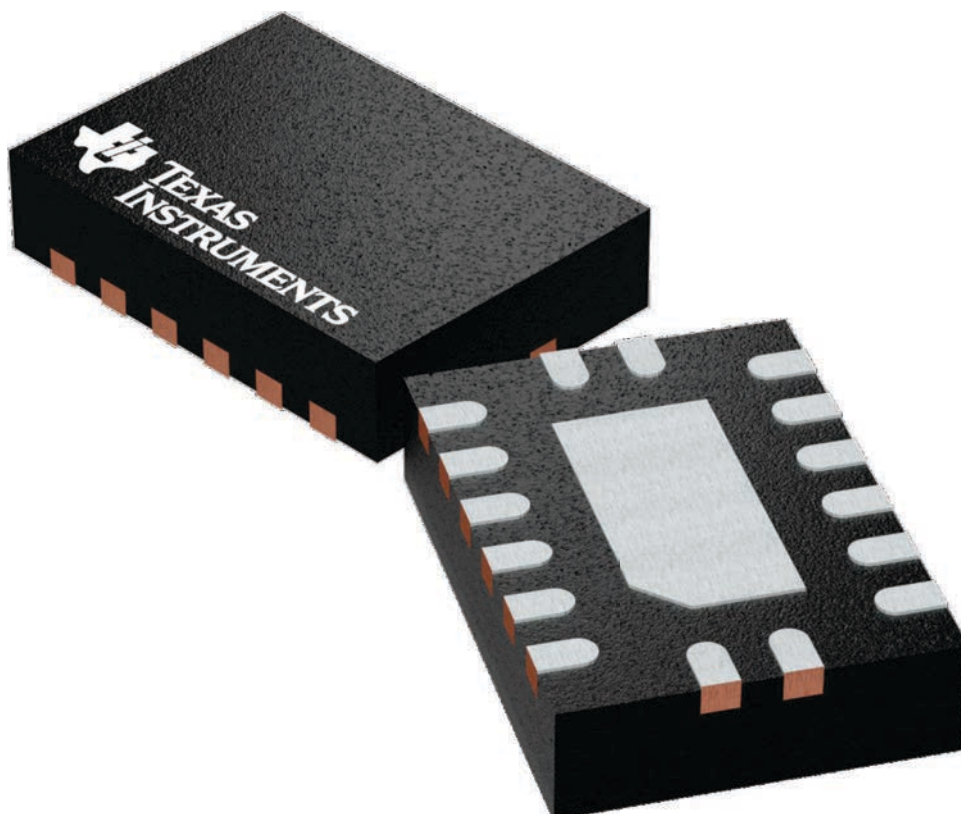
BQB 16

WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

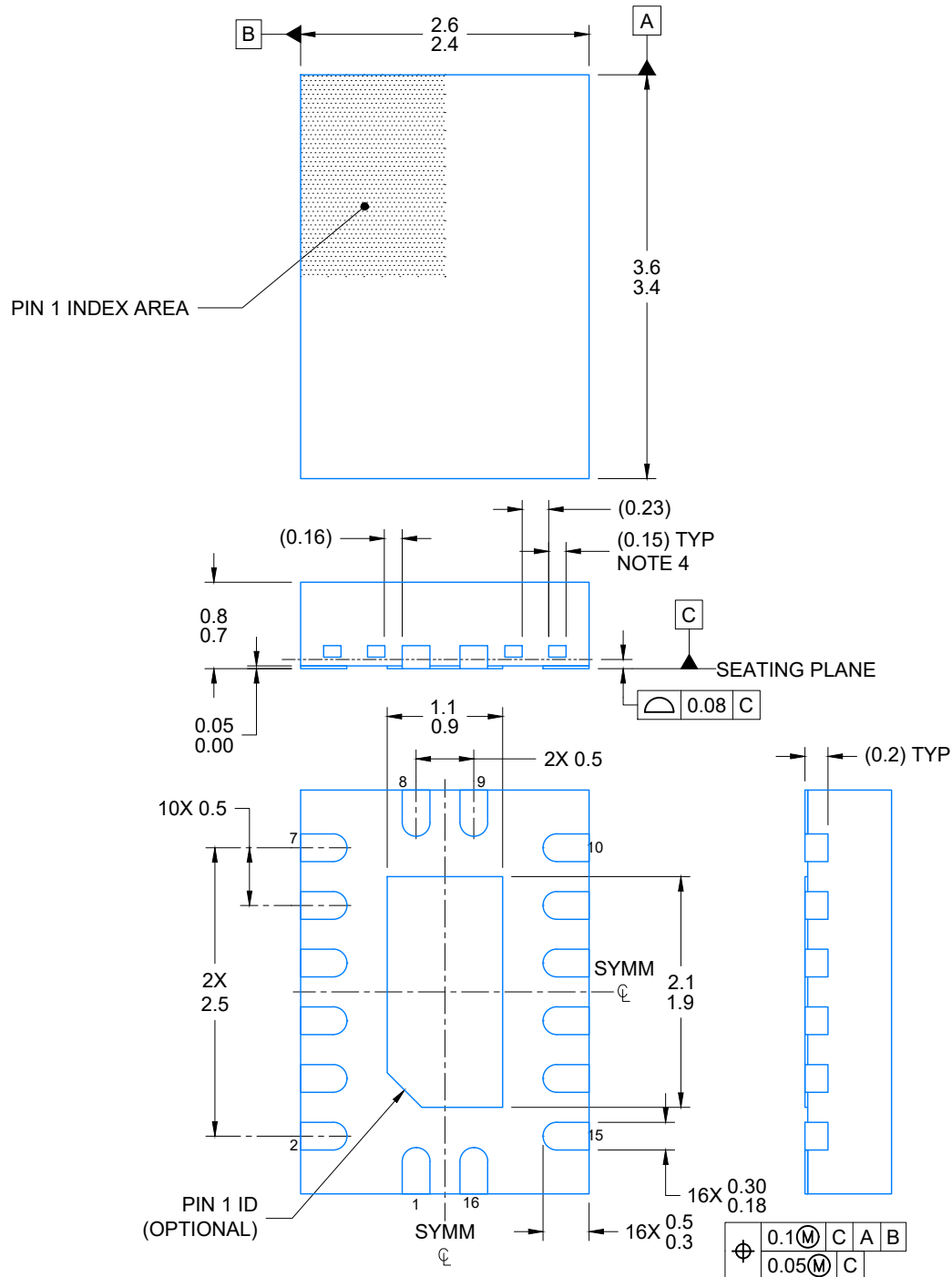


4226161/A

BQB0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



4224640/B 01/2026

NOTES:

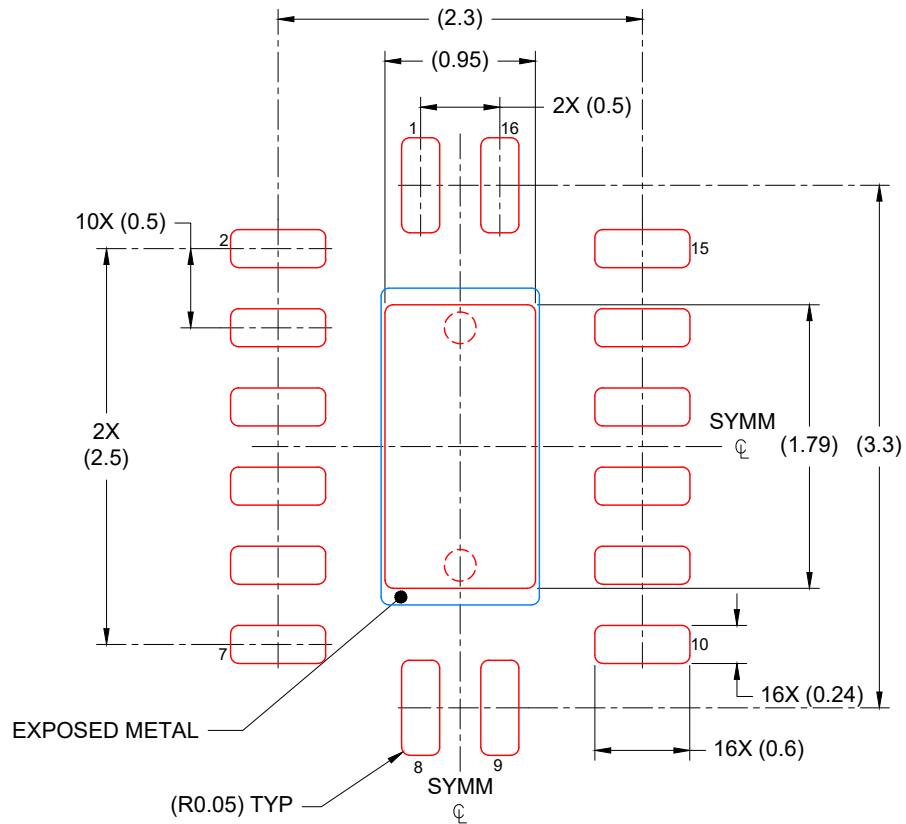
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may differ or may not be present

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

BQB0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

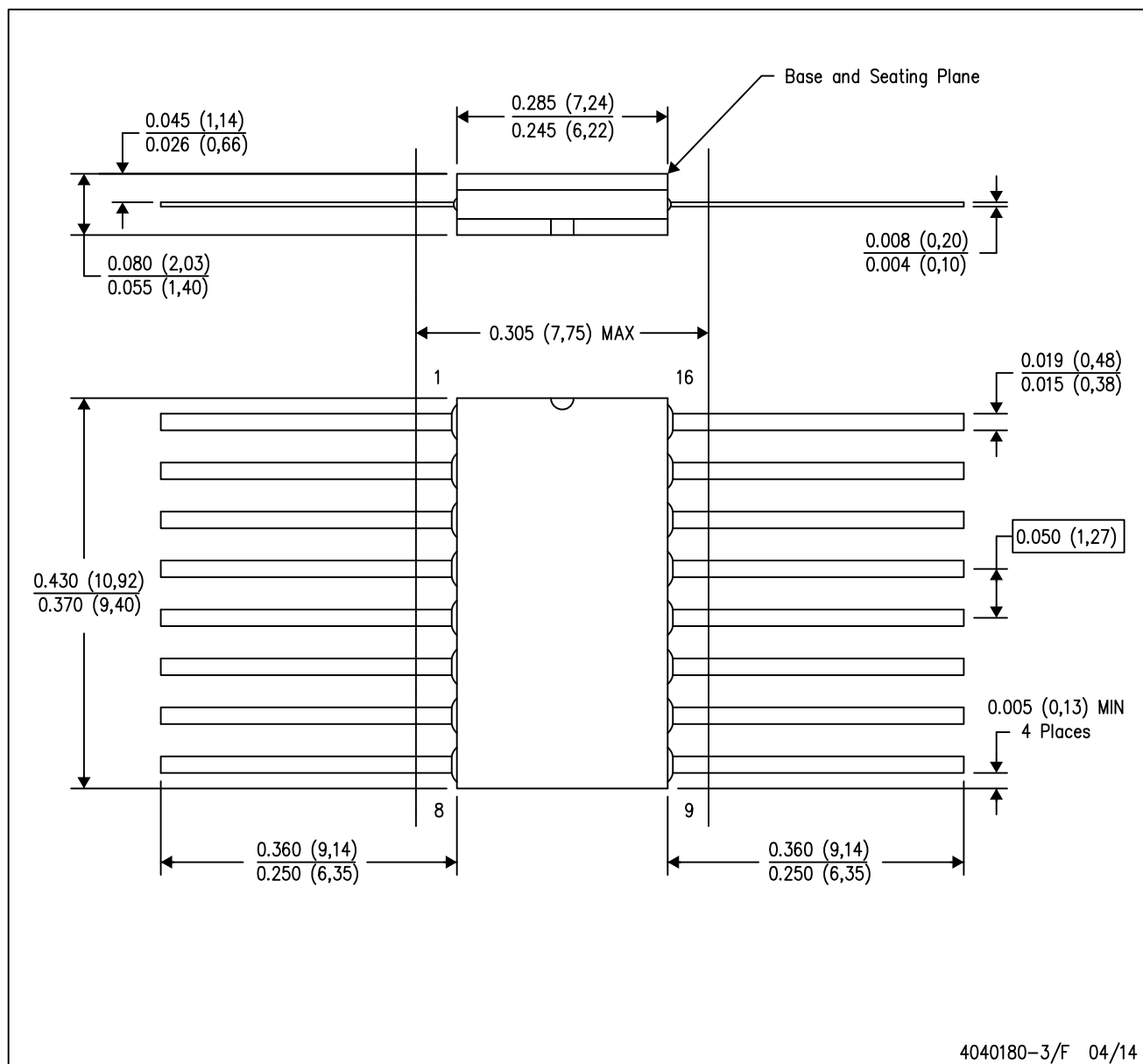
4224640/B 01/2026

NOTES: (continued)

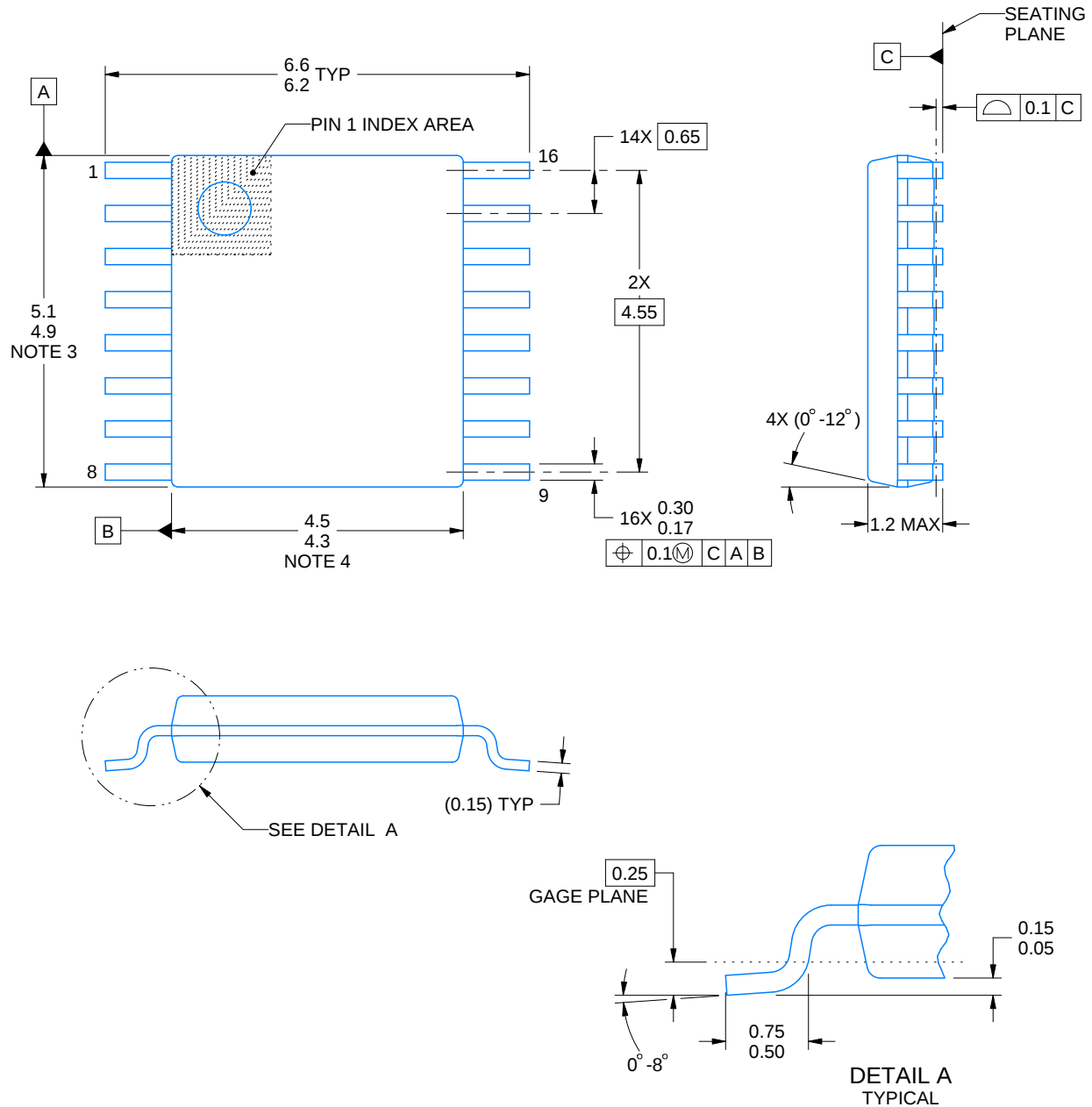
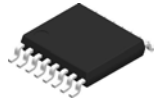
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP2-F16



4220204/B 12/2023

NOTES:

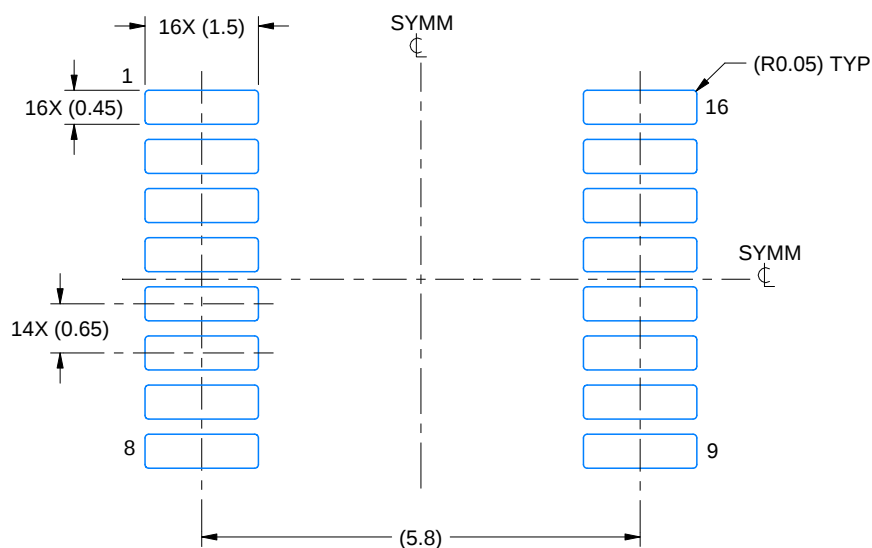
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

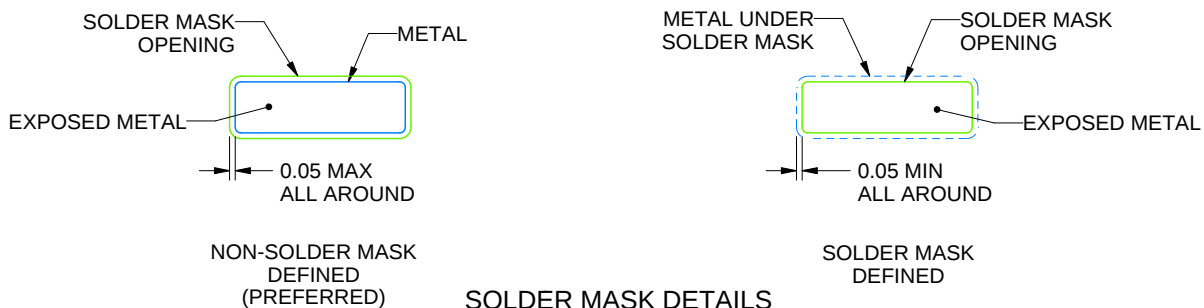
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

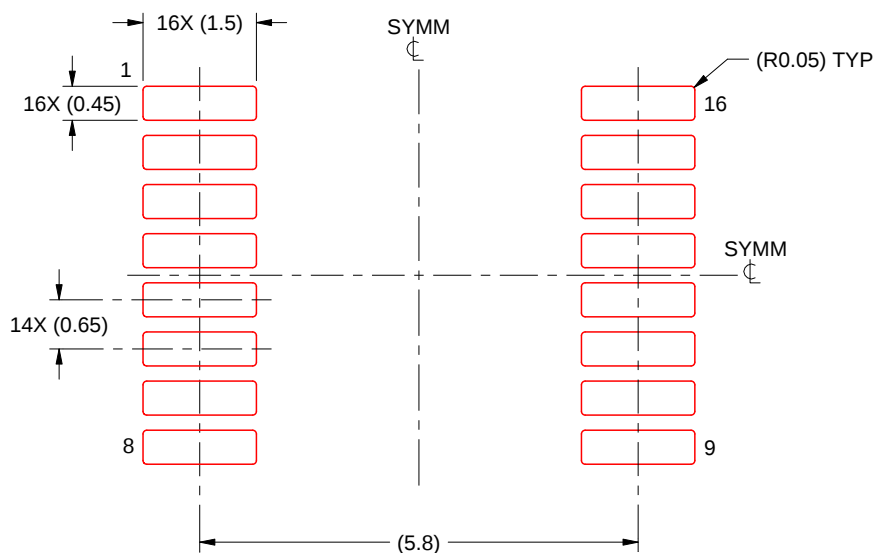
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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