SNx5C116x Dual Differential Drivers and Receivers

1 Features

- Meet or exceed standards TIA/EIA-422-B and ITU recommendation V.11
- BiCMOS process technology
- Low supply-current requirements: 9mA maximum
- Low pulse skew
- Receiver input impedance: 17kΩ typical
- Receiver input sensitivity: ±200mV
- Receiver common-mode input voltage range of −7V to7 V
- Operate from single 5V power supply
- Glitch-free power-up and power-down protection
- Receiver 3-state outputs active-low enable for SN65C1167 and SN75C1167 only
- Improved replacements for the MC34050 and MC34051

2 Applications

- Motor Drives
- Factory Automation
- Building Automation

3 Description

The SN65C1167, SN75C1167, SN65C1168, and SN75C1168 dual drivers and receivers are integrated circuits designed for balanced transmission lines. The devices meet TIA/EIA-422-B and ITU recommendation V.11.

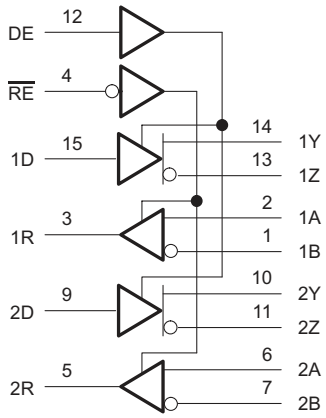
The SN65C1167 and SN75C1167 combine dual 3-state differential line drivers and 3-state differential line receivers, both of which operate from a single 5V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be connected together externally to function as direction control. The SN65C1168 and SN75C1168 drivers have individual active-high enables.

Package Information

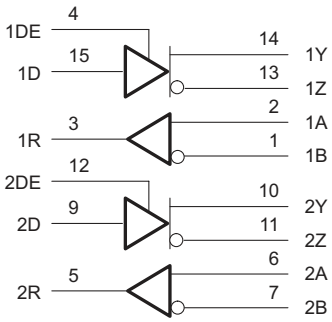
PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN65C1167	DB (SSOP)	6.2mm x 5.30mm
	NS (SOP)	10.3mm x 5.30mm
SN75C1167	DB (SSOP)	6.2mm x 5.30mm
	N (PDIP)	19.3mm x 6.35mm
	NS (SOP)	10.3mm x 5.30mm
SN65C1168	N (PDIP)	19.3mm x 6.35mm
	NS (SOP)	10.3mm x 5.30mm
	PW (TSSOP)	5mm x 4.40mm
SN75C1168	DB (SSOP)	6.2mm x 5.30mm
	N (PDIP)	19.3mm x 6.35mm
	NS (SOP)	10.3mm x 5.30mm
	PW (TSSOP)	5mm x 4.4mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

SN65C1167, SN75C1167



SN65C1168, SN75C1168



Logic Diagram (Positive Logic)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

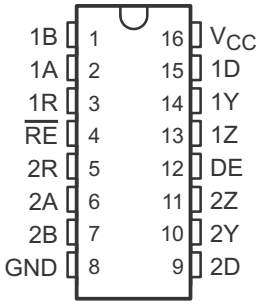


Figure 4-1. SN65C1167: DB or NS Package
SN75C1167: DB, N, or NS Package
(Top View)

Table 4-1. Pin Functions, SNx5C1167

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1B	1	I	Inverting Input of Channel 1 Differential Receiver
1A	2	I	Non-Inverting Input of Channel 1 Differential Receiver
1R	3	O	Single Ended Receiver Output for Channel 1
$\overline{RE}$	4	I	Receiver Active Low Enable Input for Channel 1 and 2
2R	5	O	Single Ended Receiver Output for Channel 2
2A	6	I	Non-Inverting Input of Channel 1 Differential Receiver
2B	7	I	Inverting Input of Channel 2 Differential Receiver
GND	8	G	Device Ground
2D	9	I	Single Ended Driver Input for Channel 2
2Y	10	O	Non-Inverting Output of Channel 2 Differential Driver
2Z	11	O	Inverting Output of Channel 2 Differential Driver
DE	12	I	Driver Active High Enable Input for Channel 1 and 2
1Z	13	O	Inverting Output of Channel 1 Differential Driver
1Y	14	O	Non-Inverting Output of Channel 1 Differential Driver
1D	15	I	Single Ended Driver Input for Channel 1
V_{CC}	16	P	Device VCC, connect 4.5V to 5.5V Source between this Pin and Device Ground

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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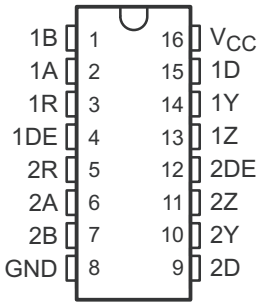


Figure 4-2. SN65C1168: N, NS, or PW Package
SN75C1168: DB, N, NS, or PW Package
(Top View)

Table 4-2. Pin Functions, SNx5C1168

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1B	1	I	Inverting Input of Channel 1 Differential Receiver
1A	2	I	Non-Inverting Input of Channel 1 Differential Receiver
1R	3	O	Single Ended Receiver Output for Channel 1
1DE	4	I	Driver Active High Enable Input for Channel 1
2R	5	O	Single Ended Receiver Output for Channel 2
2A	6	I	Non-Inverting Input of Channel 1 Differential Receiver
2B	7	I	Inverting Input of Channel 2 Differential Receiver
GND	8	G	Device Ground
2D	9	I	Single Ended Driver Input for Channel 2
2Y	10	O	Non-Inverting Output of Channel 2 Differential Driver
2Z	11	O	Inverting Output of Channel 2 Differential Driver
2DE	12	I	Driver Active High Enable Input for Channel 2
1Z	13	O	Inverting Output of Channel 1 Differential Driver
1Y	14	O	Non-Inverting Output of Channel 1 Differential Driver
1D	15	I	Single Ended Driver Input for Channel 1
V_{CC}	16	P	Device VCC, connect 4.5V to 5.5V Source between this Pin and Device Ground

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.5	7	V
V_I	Input voltage range	Driver	–0.5	V_{CC} + 0.5	V
		A or B, Receiver	–11	14	
V_{ID}	Differential input voltage range(3)	Receiver	–14	14	V
V_O	Output voltage range	Driver	–0.5	7	V
I_{IK} or I_{OK}	Clamp current range	Driver		±20	mA
I_O	Output current range	Driver		±150	mA
		Receiver		±25	
I_{CC}	Supply current			200	mA
	GND current			−200	mA
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages values except differential input voltage are with respect to the network GND.
(3) Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	± 8kV	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	± 1kV	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. .

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IC}	Common-mode input voltage(1)	Receiver			±7	V
V_{ID}	Differential input voltage	Receiver			±7	V
V_{IH}	High-level input voltage	Except A, B	2			V
V_{IL}	Low-level input voltage	Except A, B			0.8	V
I_{OH}	High-level output current	Receiver			−6	mA
		Driver			−20	
I_{OL}	Low-level output current	Receiver			6	mA
		Driver			20	

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5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
T_A	Operating free-air temperature	SN75C1167, SN75C1168	0		70	°C
		SN65C1167, SN65C1168	–40		85	

(1) Refer to TIA/EIA-422-B for exact conditions.

5.4 Thermal Information

THERMAL METRIC(1)		DB (SSOP) 16 PINS	N (PDIP) 16 PINS	NS (SOP) 16 PINS	PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.6	60.6	88.5	107.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.7	48.1	46.2	38.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.3	40.6	50.7	53.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.8	27.5	13.5	3.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.5	40.3	50.3	53.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics, Driver Section(2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −20mA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 20mA			0.2	0.4	V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0mA		2		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage (2)	R_L = 100Ω, See Figure 6-1		2	3.1		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage					±0.4	V
V_{OC}	Common-mode output voltage					±3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage					±0.4	V
$I_{O(OFF)}$	Output current with power off	V_{CC} = 0V	V_O = 6V			100	µA
			V_O = −0.25V			−100	
I_{OZ}	High-impedance-state output current	V_O = 2.5				20	µA
		V_O = 5				−20	
I_{IH}	High-level input current	V_I = V_{CC} or V_{IH}				1	µA
I_{IL}	Low-level input current	V_I = GND or V_{IL}				−1	µA
I_{OS}	Short-circuit output current(3)	V_O = V_{CC} or GND,		−30		−150	mA
I_{CC}	Supply current (total package)(4)	No load, Enabled	V_I = V_{CC} or GND		4	6	mA
			V_I = 2.4 or 0.5V		5	9	
C_i	Input capacitance				6		pF

(1) All typical values are at V_{CC} = 5V, and T_A = 25°C.
(2) Refer to TIA/EIA-422-B for exact conditions.
(3) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
(4) This parameter is measured per input, while the other inputs are at V_{CC} or GND.

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5.6 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	R1 = R2 = 50Ω, C1 = C2 = C3 = 40pF, See Figure 6-2	R3 = 500Ω, S1 is open,		7	12	ns
t_{PLH}	Propagation delay time, low- to high-level output				7	12	ns
$t_{sk(p)}$	Pulse skew				0.5	4	ns
t_r	Rise time	R1 = R2 = 50Ω, C1 = C2 = C3 = 40pF, SeeFigure 6-3	R3 = 500Ω, S1 is open,		5	10	ns
t_f	Fall time				5	10	ns
t_{PZH}	Output enable time to high level	R1 = R2 = 50Ω, C1 = C2 = C3 = 40pF, See Figure 6-4	R3 = 500Ω, S1 is closed,		10	19	ns
t_{PZL}	Output enable time to low level				10	19	ns
t_{PHZ}	Output disable time from low level	R1 = R2 = 50Ω, C1 = C2 = C3 = 40pF, See Figure 6-4	R3 = 500Ω, S1 is closed,		7	16	ns
t_{PLZ}	Output disable time from high level				7	16	ns

(1) All typical values are at V_{CC} = 5V, and T_A = 25°C.

5.7 Electrical Characteristics, Receiver Section

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage, differential input						0.2	V
V_{IT-}	Negative-going input threshold voltage, differential input				−0.2(2)			V
V_{hys}	Input hysteresis (V_{IT+} – V_{IT-})					60		mV
V_{IK}	Input clamp voltage, $\overline{RE}$	SN75C1167	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = −6 mA	3.8	4.2		V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV,	I_{OL} = 6 mA		0.1	0.3	V
I_{OZ}	High-impedance-state output current	SN75C1167	V_O = VCC or GND			±0.5	±5	µA
I_I	Line input current		Other input at 0 V	V_I = 10 V			1.5	mA
				V_I = −10 V			−2.5	
I_I	Enable input current, $\overline{RE}$	SN75C1167	V_I = V_{CC} or GND				±1	µA
r_i	Input resistance		V_{IC} = −7 V to 7 V,	Other input at 0 V	4	17		kΩ
I_{CC}	Supply current (total package)		No load, Enabled	V_I = V_{CC} or GND		4	6	mA
				V_{IH} = 2.4 V or 0.5 V(3)		5	9	

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) Refer to TIA/EIA-422-B for exact conditions.

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5.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (2)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 6-5	9	17	27	ns
t_{PHL}	Propagation delay time, high- to low-level output		9	17	27	ns
t_{TLH}	Transition time, low- to high-level output	V_{IC} = 0V, See Figure 6-5		4	9	ns
t_{THL}	Transition time, high- to low-level output			4	9	ns
t_{PZH}	Output enable time to high level	R_L = 1kW, See Figure 6-6		13	22	ns
t_{PZL}	Output enable time to low level			13	22	ns
t_{PHZ}	Output disable time from high level			13	22	ns
t_{PLZ}	Output disable time from low level			13	22	ns

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) Measured per input while the other inputs are at V_{CC} or GND

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6 Parameter Measurement Information

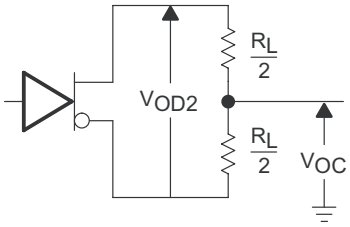
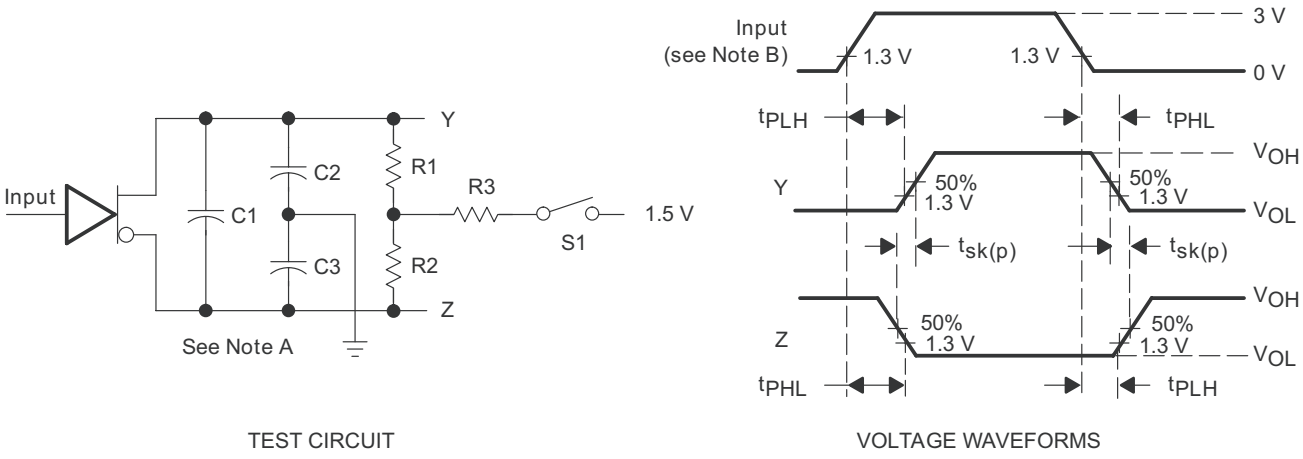


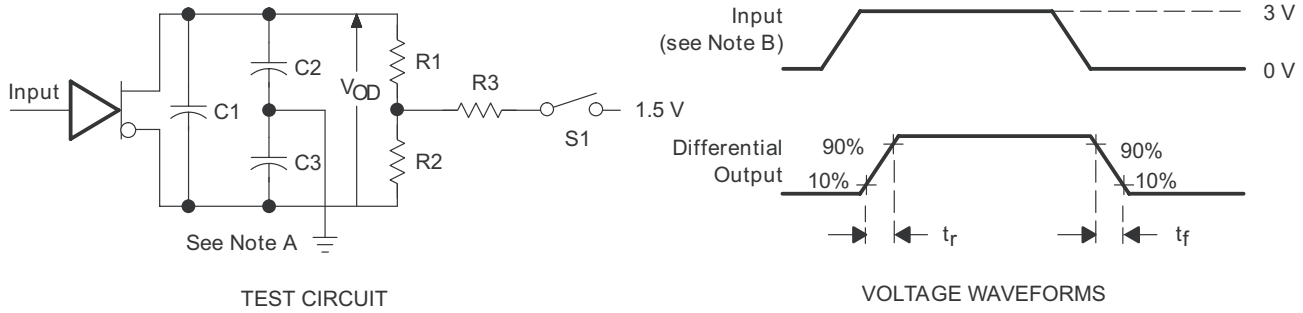
Figure 6-1. Driver Test Circuit, V_{OD} and V_{OC}



A. C1, C2, and C3 include probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, 50% duty cycle, t_r = t_f ≤ 6ns.

Figure 6-2. Driver Test Circuit and Voltage Waveforms

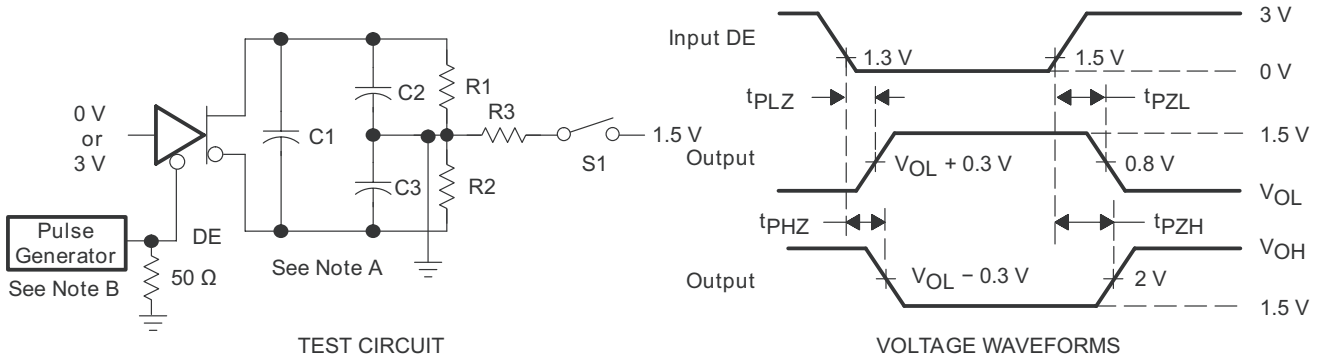


A. C1, C2, and C3 include probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, 50% duty cycle, t_r = t_f ≤ 6ns.

Figure 6-3. Driver Test Circuit and Voltage Waveforms

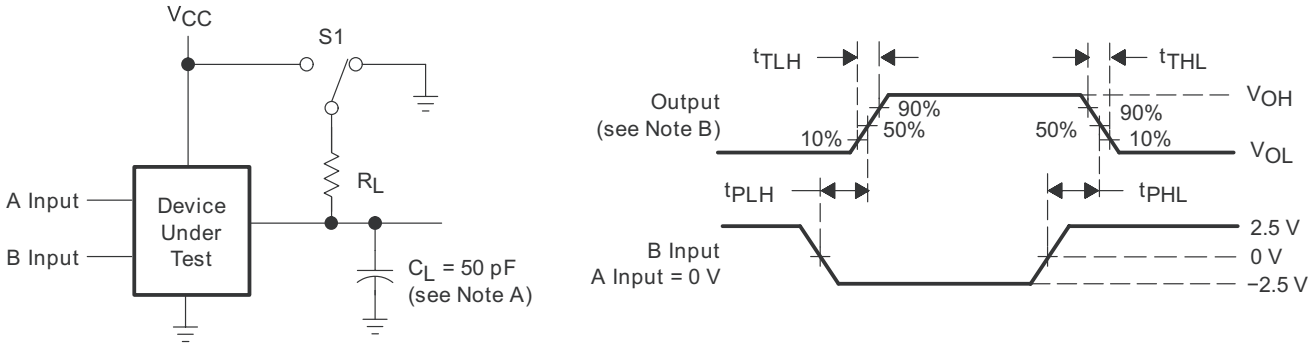
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TEST CIRCUIT VOLTAGE WAVEFORMS

A. C1, C2, and C3 include probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, 50% duty cycle, t_r = t_f ≤ 6ns.

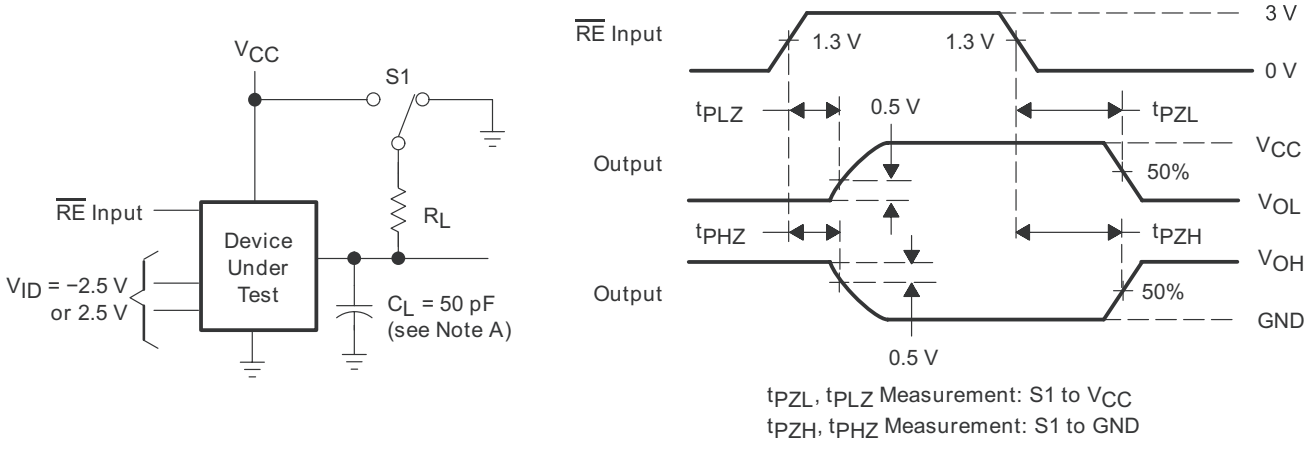
Figure 6-4. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, 50% duty cycle, t_r = t_f ≤6ns.

Figure 6-5. Receiver Test Circuit and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, 50% duty cycle, t_r = t_f ≤ 6ns.

Figure 6-6. Receiver Test Circuit and Voltage Waveforms

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7 Detailed Description

7.1 Functional Block Diagram

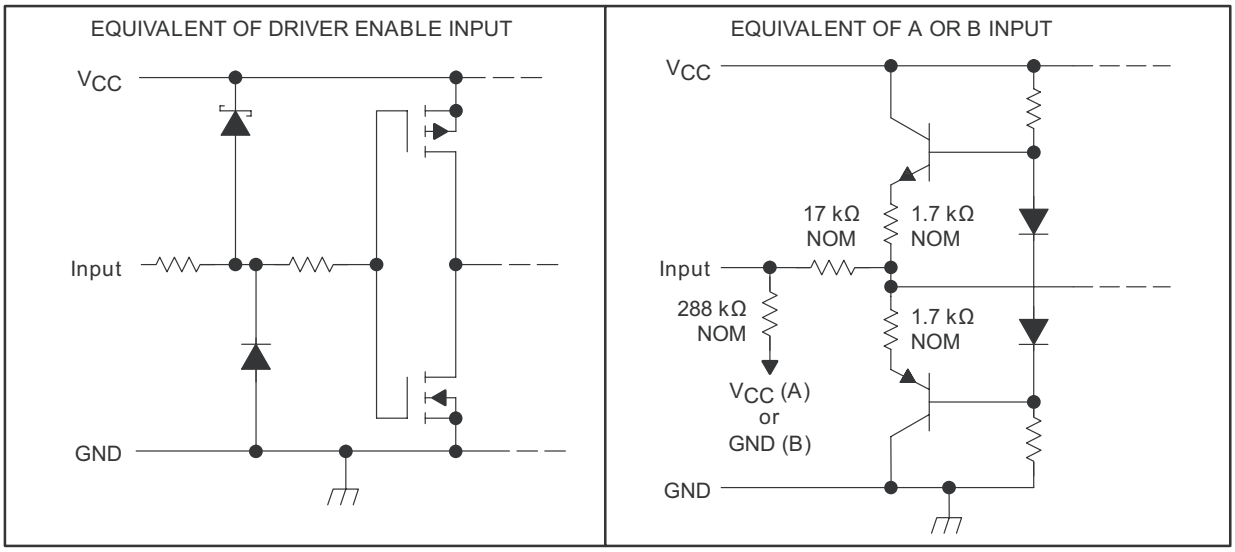


Figure 7-1. Schematic of Inputs

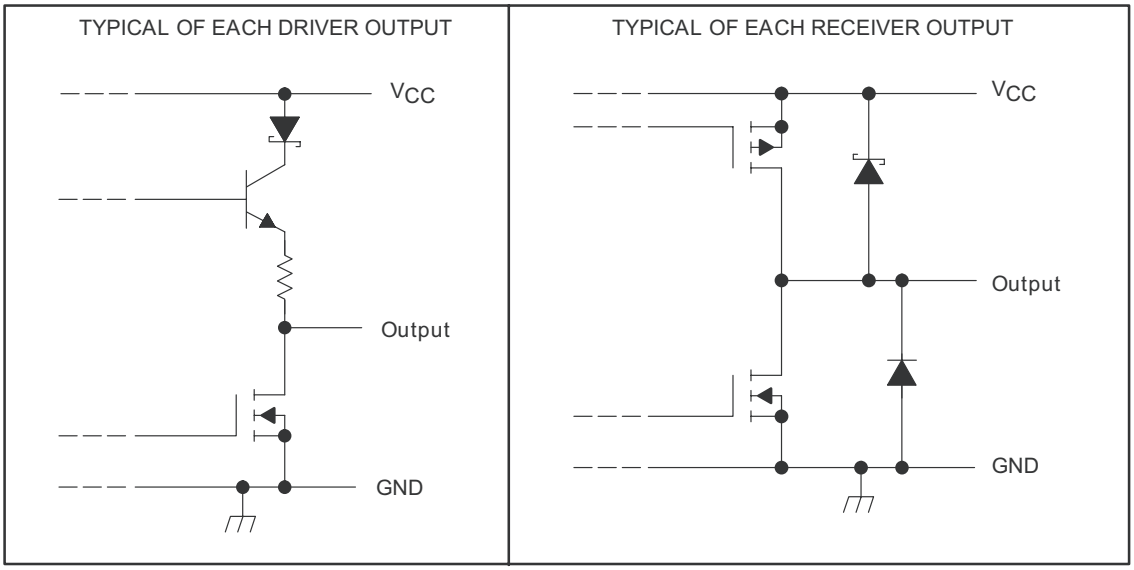


Figure 7-2. Schematic of Outputs

7.2 Device Functional Modes

7.2.1 Functions Table

Table 7-1. Each Driver(1)

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Table 7-2. Each Receiver(1)

DIFFERENTIAL INPUTS A − B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
$-0.2V < V_{ID} < 0.2V$	L	?
$V_{ID} \leq -0.2V$	L	L
X	H	Z
Open	L	H

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant,
Z = high impedance (off), Open = input disconnected or connected driver off

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8 Device and Documentation Support

8.1 Documentation Support

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (November 2009) to Revision G (February 2024)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document	1
• Changed the I_{CC} for V_I = 2.4 or 0.5V MAX value From: 3mA To: 9mA in the *Electrical Characteristics, Driver Section*	6

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65C1167NSR	Obsolete	Production	SOP (NS) | 16	-	-	Call TI	Call TI	-40 to 85	65C1167
SN65C1168N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN65C1168N
SN65C1168N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN65C1168N
SN65C1168NSR	Obsolete	Production	SOP (NS) | 16	-	-	Call TI	Call TI	-40 to 85	65C1168
SN65C1168PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	CB1168
SN75C1167DB	Obsolete	Production	SSOP (DB) | 16	-	-	Call TI	Call TI	0 to 70	CA1167
SN75C1167DBR	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1167
SN75C1167DBR.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1167
SN75C1167N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75C1167N
SN75C1167N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75C1167N
SN75C1168DBR	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168
SN75C1168DBR.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168
SN75C1168N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75C1168N
SN75C1168N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75C1168N
SN75C1168NE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75C1168N
SN75C1168NS	Active	Production	SOP (NS) | 16	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C1168
SN75C1168NS.A	Active	Production	SOP (NS) | 16	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C1168
SN75C1168NSR	Obsolete	Production	SOP (NS) | 16	-	-	Call TI	Call TI	0 to 70	75C1168
SN75C1168PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	0 to 70	CA1168

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

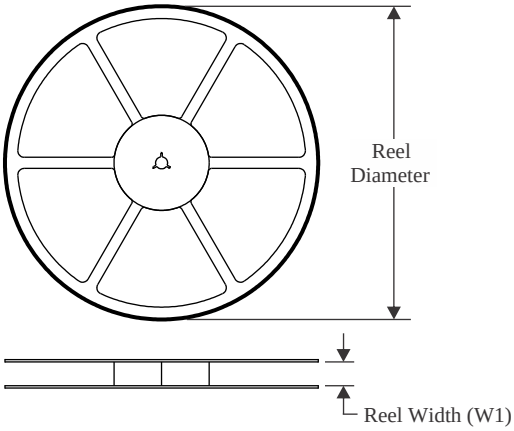
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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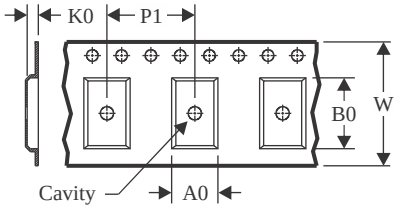
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

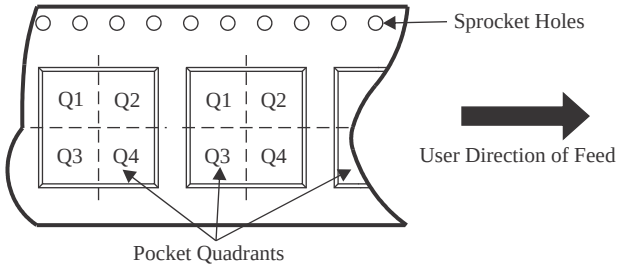


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

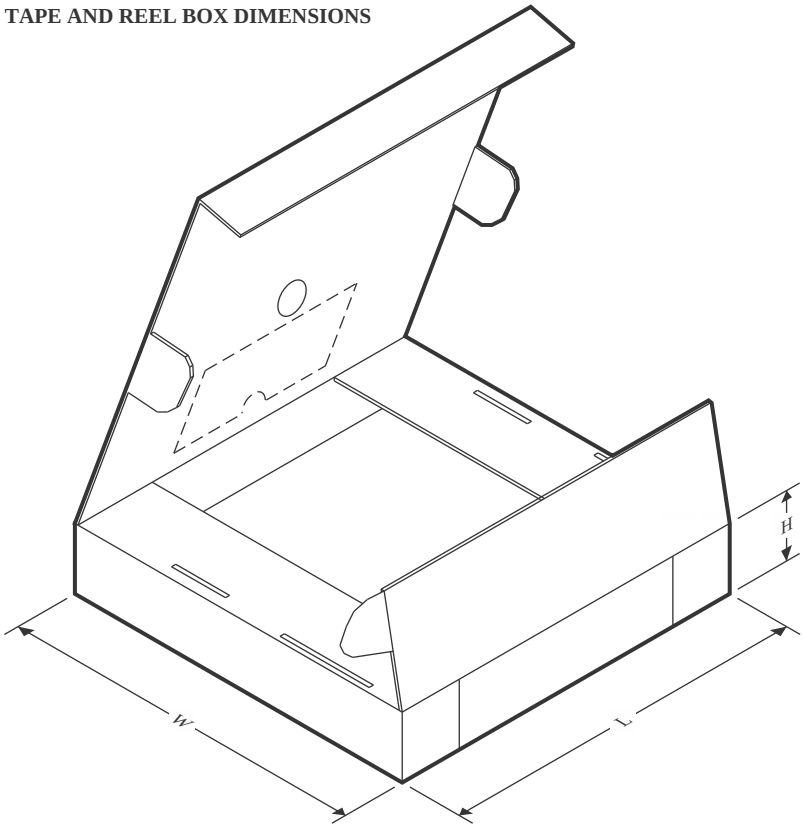
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75C1167DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN75C1168DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

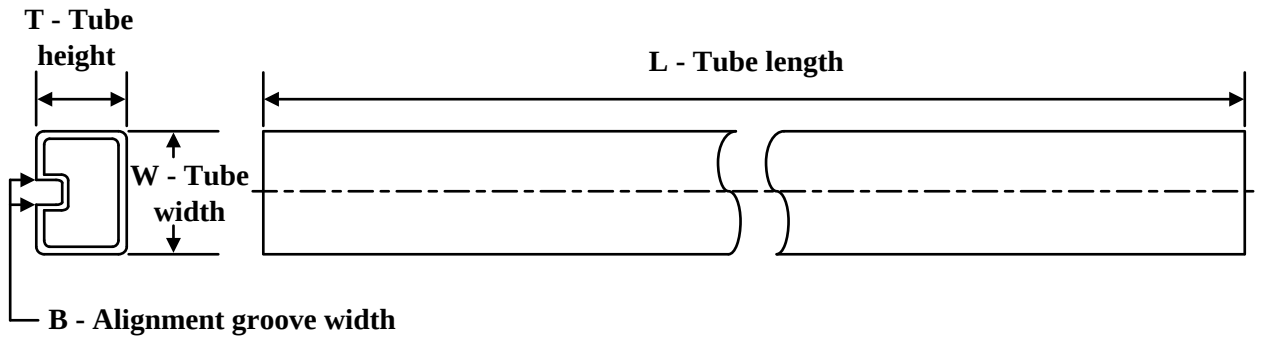
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75C1167DBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN75C1168DBR	SSOP	DB	16	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

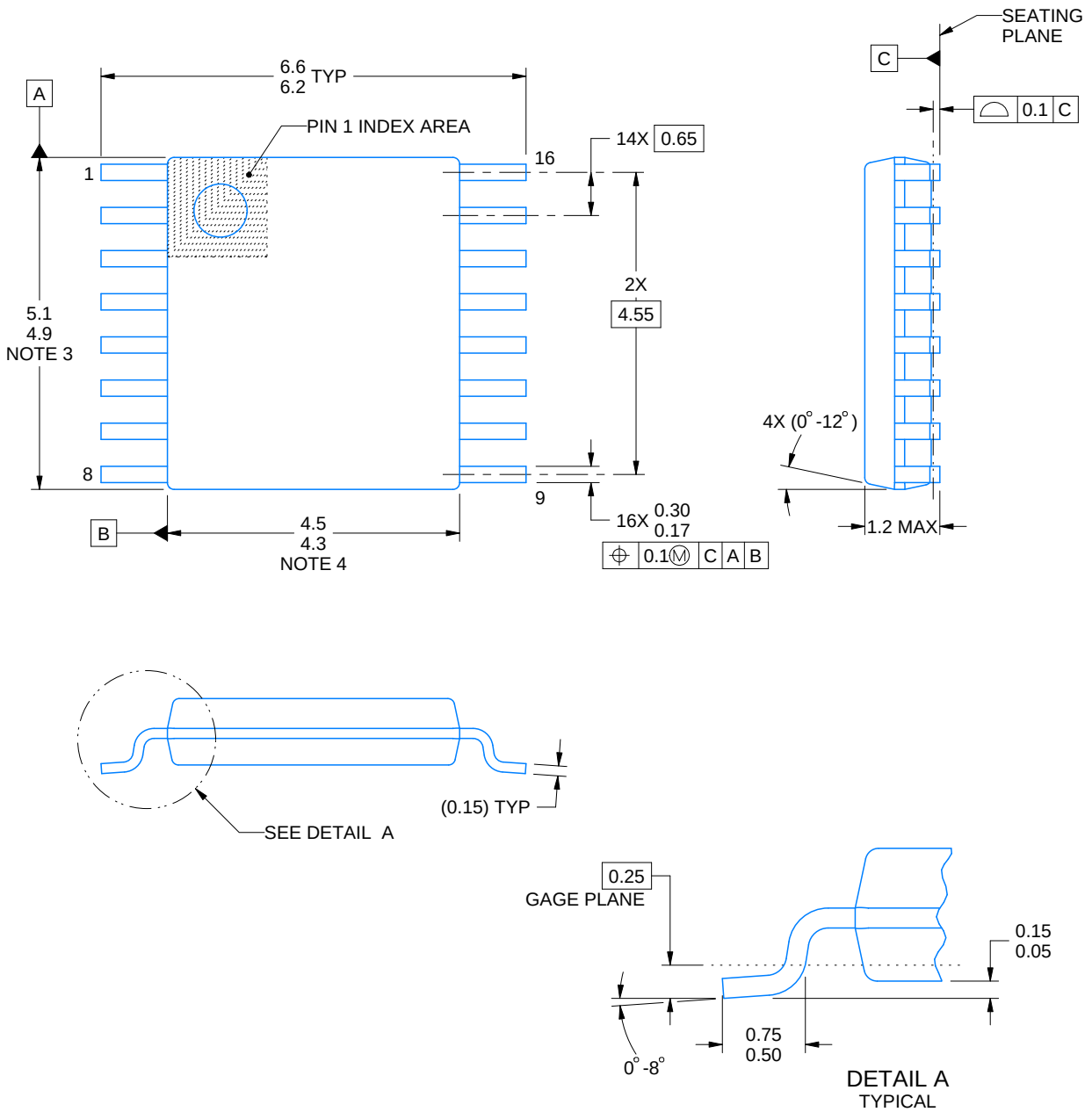
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65C1168N	N	PDIP	16	25	506	13.97	11230	4.32
SN65C1168N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN75C1167N	N	PDIP	16	25	506	13.97	11230	4.32
SN75C1167N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN75C1168N	N	PDIP	16	25	506	13.97	11230	4.32
SN75C1168N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN75C1168NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN75C1168NS	NS	SOP	16	50	530	10.5	4000	4.1
SN75C1168NS.A	NS	SOP	16	50	530	10.5	4000	4.1

PACKAGE OUTLINE

PW0016A

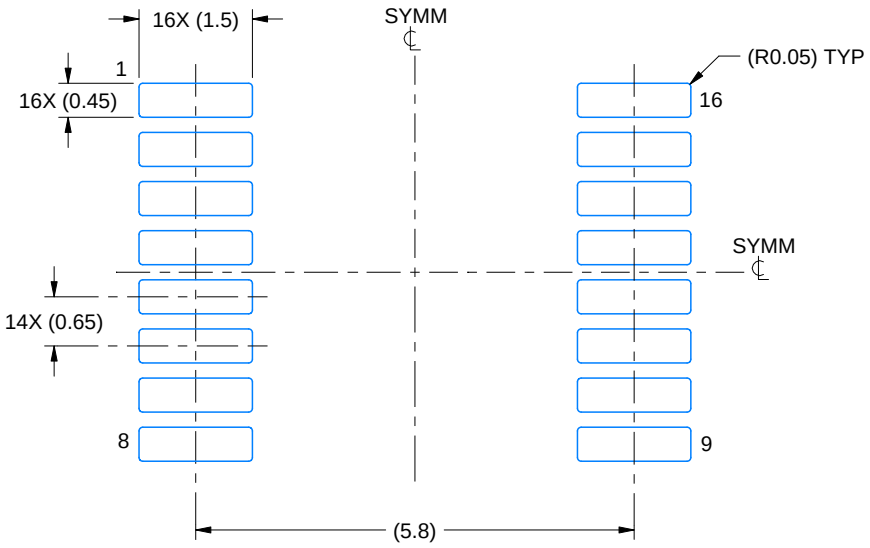
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

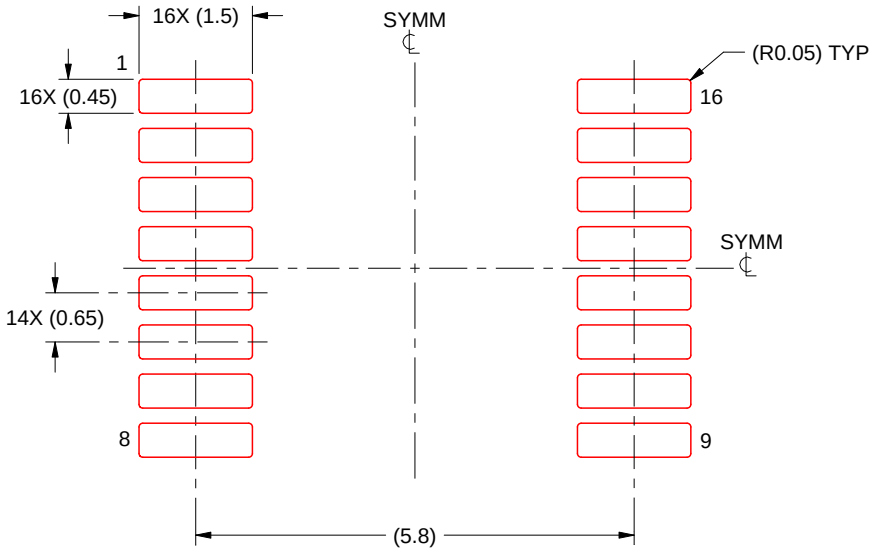


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

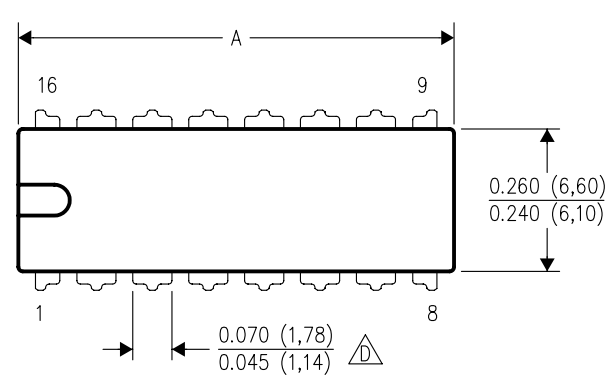
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

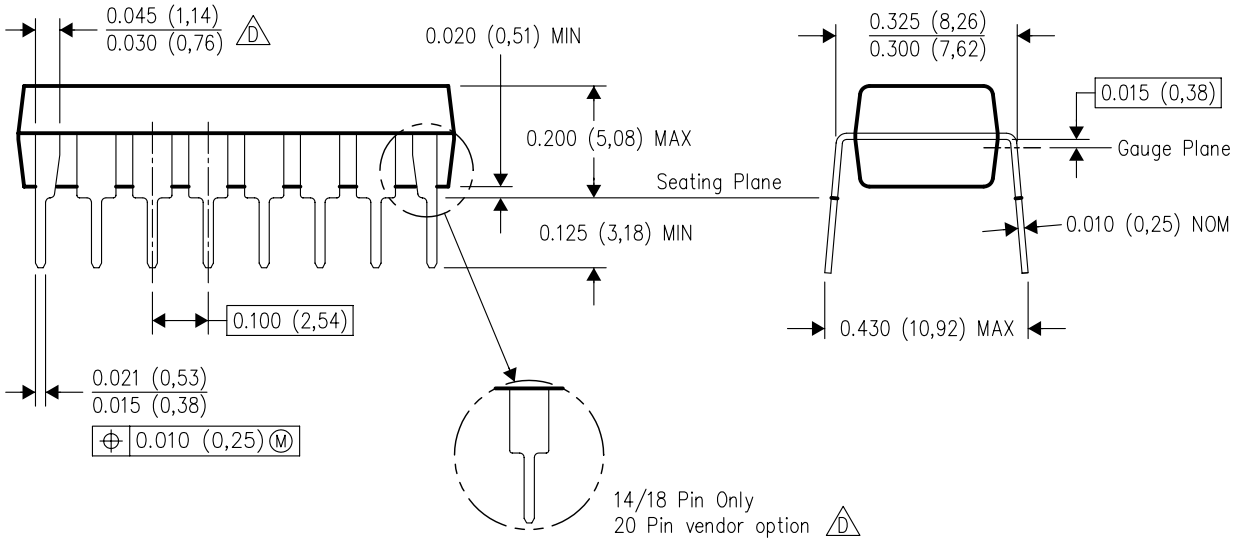
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

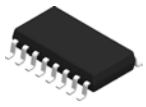


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

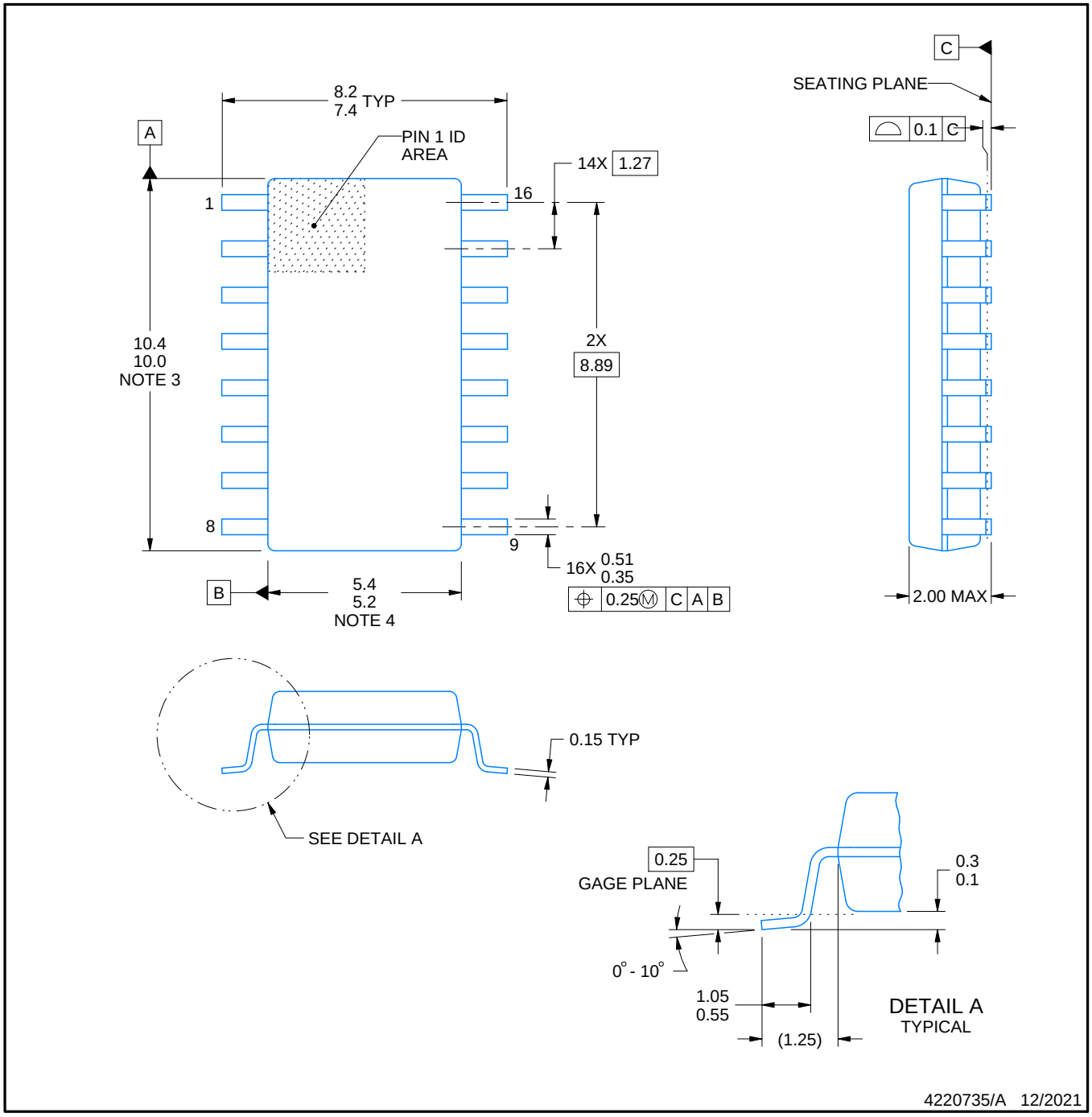


PACKAGE OUTLINE

NS0016A

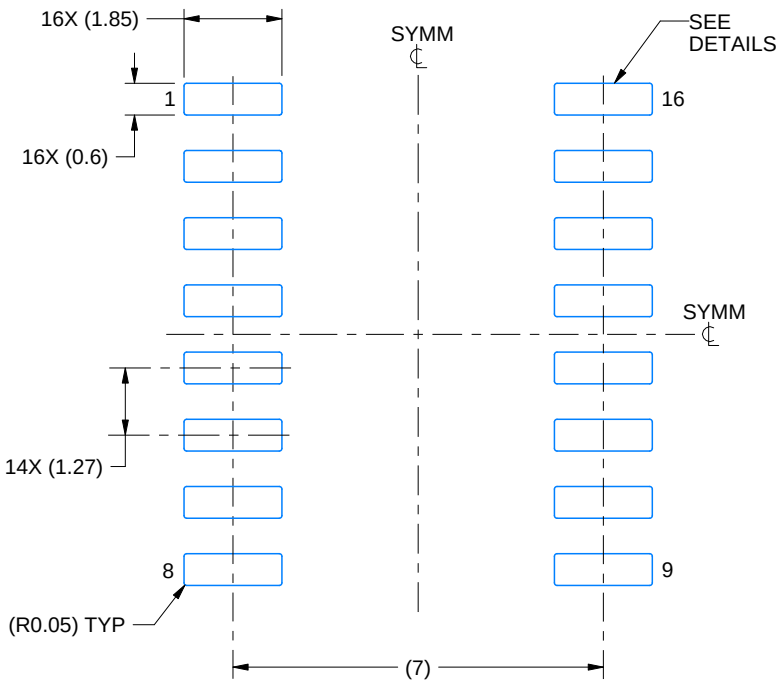
SOP - 2.00 mm max height

SOP

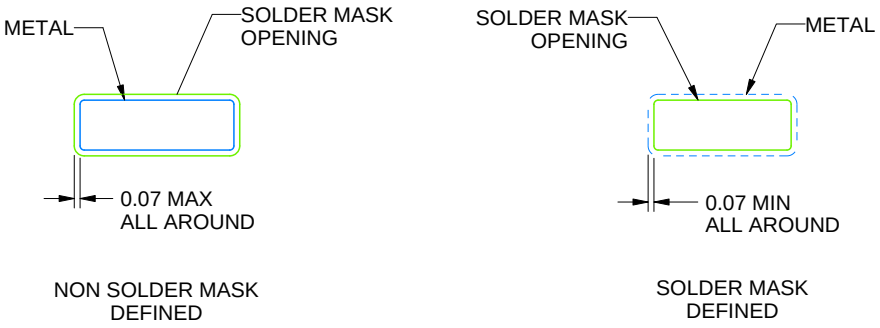


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

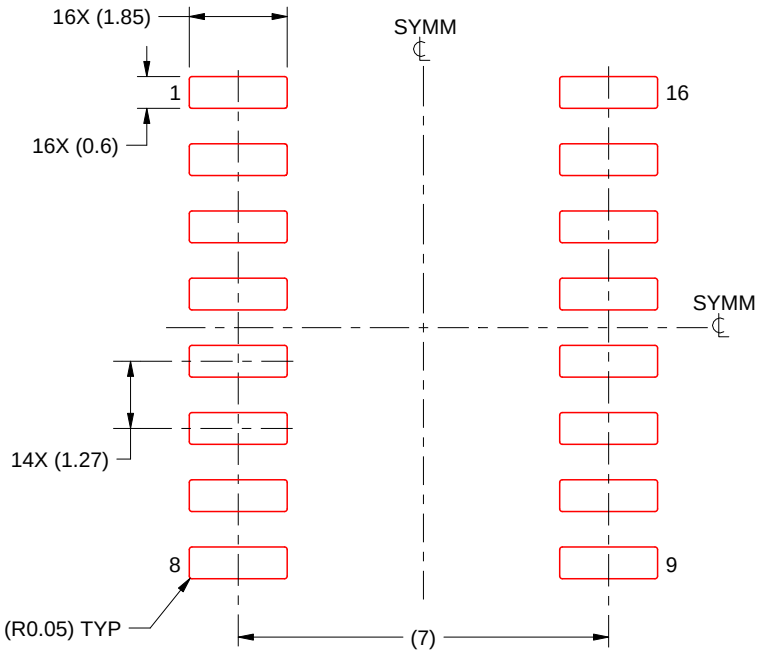
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

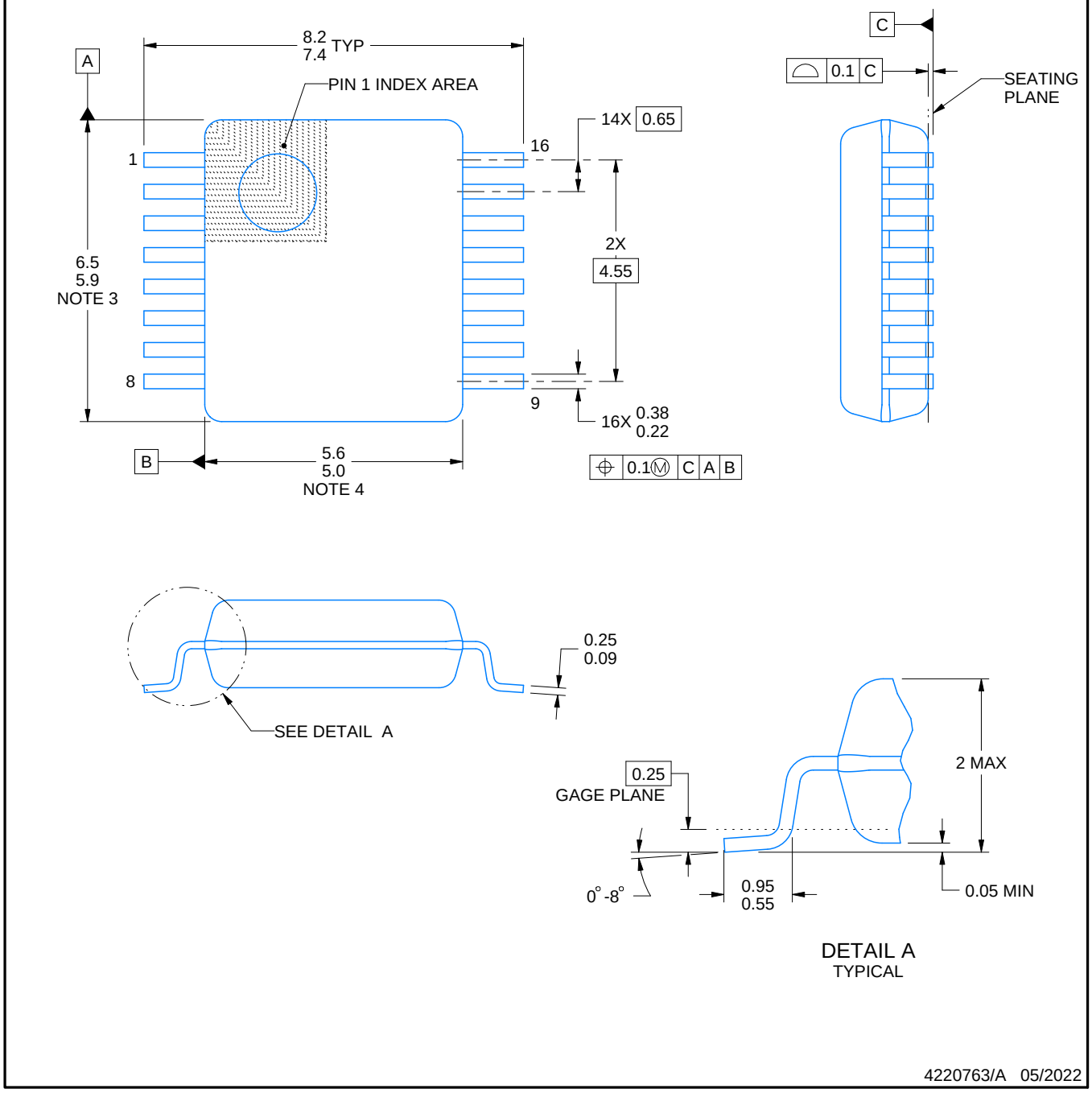
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DB0016A

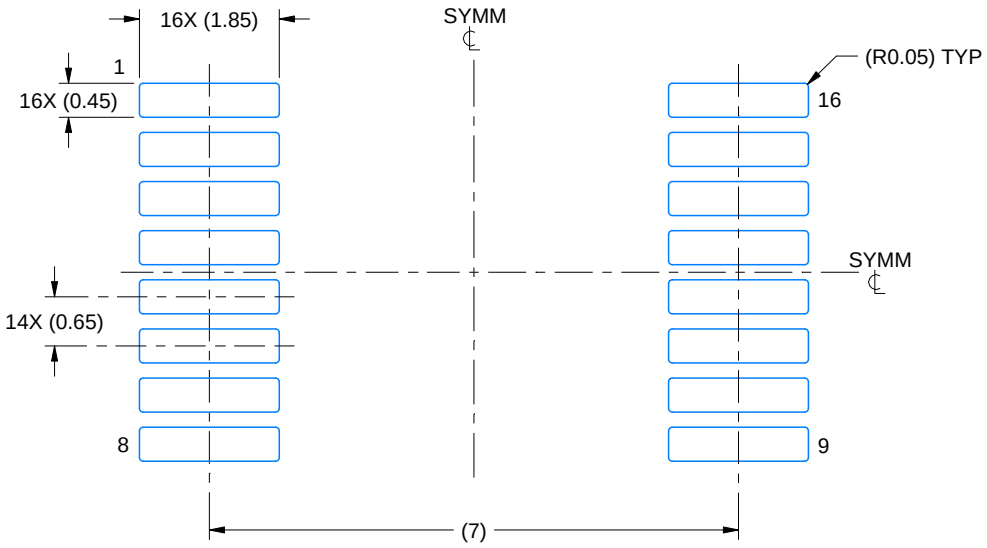
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

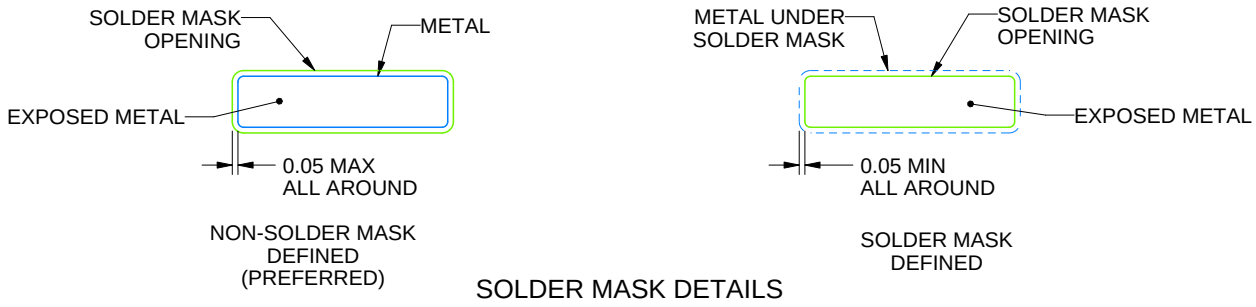


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

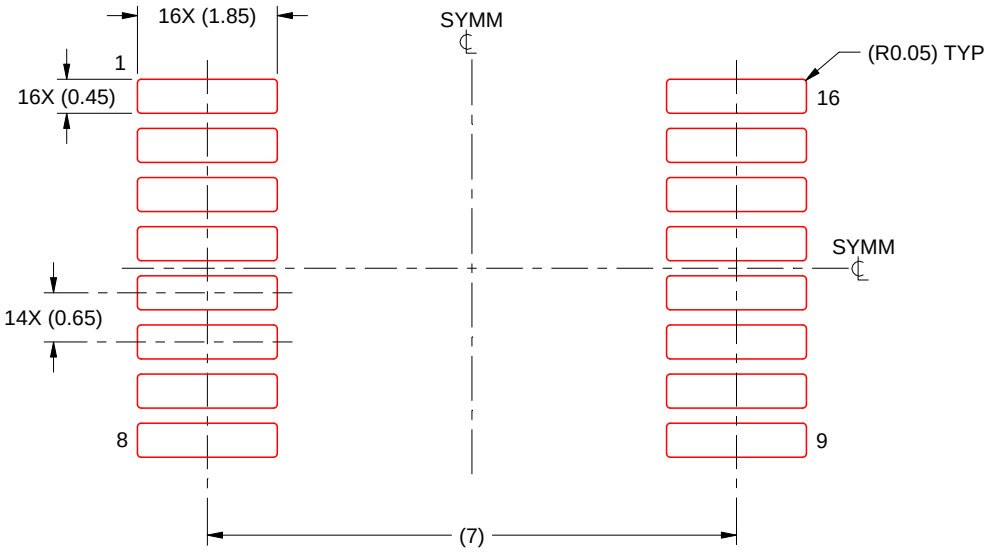


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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