SN65C116xE ±15kV ESD 保護機能搭載、デュアル差動ドライバ / レシーバ

1 特長

- TIA/EIA-422-B および ITU Recommendation V.11 適合以上の性能
- 5V 単一電源で動作
- RS-422 バス ピン用 ESD 保護機能
  - ±15kV 人体モデル (HBM)
  - ±8kV IEC 61000-4-2 接触放電
  - ±8kV IEC 61000-4-2 エアギャップ放電
- 小さい消費電流要件:9mA 以下
- 低パルス スキュー
- レシーバ入力インピーダンス:17kΩ (標準値)
- レシーバ入力感度:±200mV
- レシーバ同相入力電圧範囲:-7V～+7V
- グリッチ フリーのパワーアップ / パワーダウン保護機能
- レシーバ 3 ステート出力アクティブ Low イネーブル (SN65C1167E のみ)

2 アプリケーション

- AC / サーボ モーター ドライブ
- ファクトリ オートメーション / 制御
- ワイヤレス インフラ

3 概要

SN65C1167E および SN65C1168E はデュアル ドライバとデュアル レシーバで構成されており、RS-422 バス ピンを ±15kV の ESD (人体モデル [HBM]) と ±8kV の ESD (IEC61000-4-2 エアギャップ放電および接触放電) から保護できます。これらのデバイスは、TIA/EIA-422-B および ITU Recommendation V.11 の要件を満たしています。

SN65C1167E は、デュアル 3 ステート差動ライン ドライバとデュアル 3 ステート差動ライン レシーバを統合しており、どちらも 5V 単一電源で動作します。ドライバとレシーバはそれぞれアクティブ High、アクティブ Low のイネーブルを備えており、それらのイネーブルを外部で互いに接続することで、方向制御として機能させることができます。

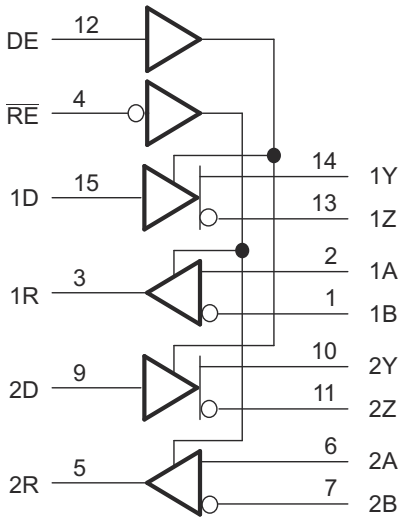
SN65C1168E ドライバは、個別のアクティブ High イネーブルを搭載しています。

パッケージ情報

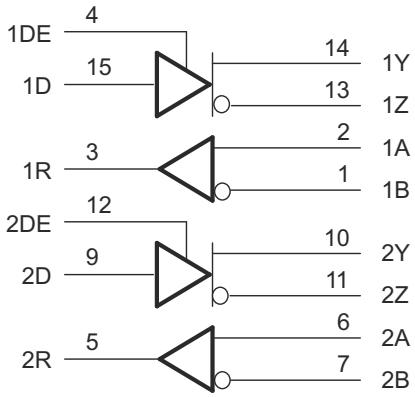
部品番号	パッケージ (1)	パッケージ サイズ(2)
SN65C116xE	SO (16)	10.3mm × 5.3mm
	TSSOP (16)	5mm × 4.4mm
	VQFN (16)	4mm × 3.5mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

SN65C1167E



SN65C1168E



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ブロック図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

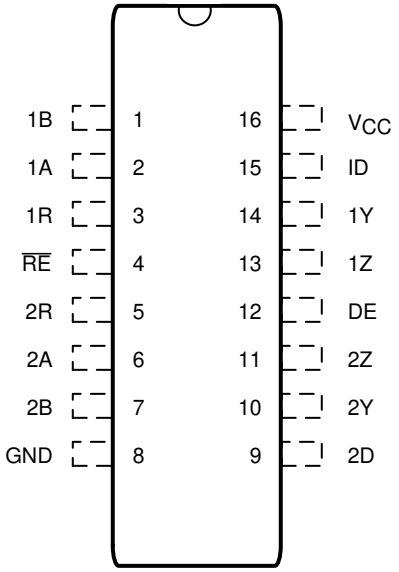


図 4-1. NS or PW Package 16 Pin (NS or TSSOP) Top View

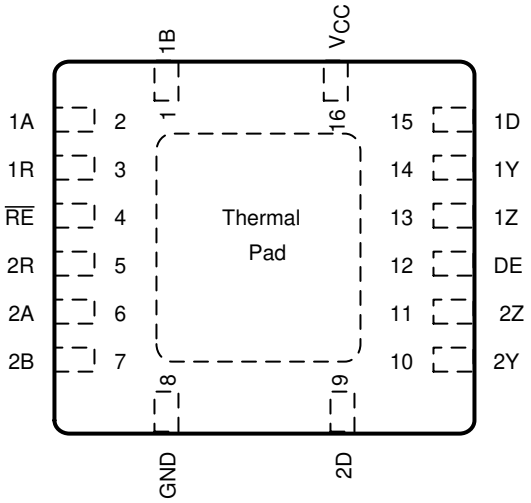


図 4-2. RGY Package 16 Pin (VQFN) Top View

表 4-1. Pin Functions, SN65C1167E

PIN				I/O	DESCRIPTION
NAME	SO	TSSOP	VQFN		
1A	2	2	2	I	RS422 differential input (noninverting) to receiver 1
2A	6	6	6	I	RS422 differential input (noninverting) to receiver 2
1B	1	1	1	I	RS422 differential input (inverting) to receiver 1
2B	7	7	7	I	RS422 differential input (inverting) to receiver 2
1D	15	15	15	I	Logic data input to RS422 driver 1
2D	9	9	9	I	Logic data input to RS422 driver 2
DE	12	12	12	I	Driver enable (active high)
GND	8	8	8	—	Device ground pin
1R	3	3	3	O	Logic data output of RS422 receiver 1
2R	5	5	5	O	Logic data output of RS422 receiver 2
$\overline{RE}$	4	4	4	I	Receiver enable pin (active low)
V_{CC}	16	16	16	—	Power supply
1Y	14	14	14	O	RS-422 differential (noninverting) driver output 1
2Y	10	10	10	O	RS-422 differential (noninverting) driver output 2
1Z	13	13	13	O	RS-422 differential (inverting) driver output 1
2Z	11	11	11	O	RS-422 differential (inverting) driver output 2

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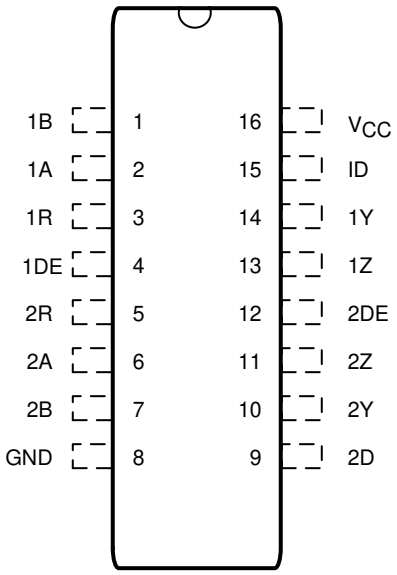


図 4-3. NS or PW Package 16 Pin (NS or TSSOP) Top View

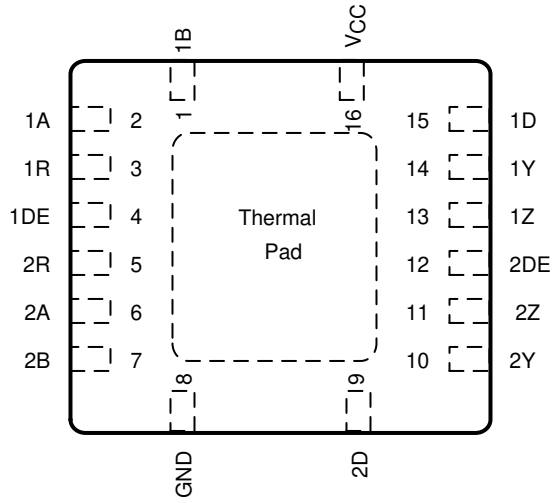


図 4-4. RGY Package 16 Pin (VQFN) Top View

表 4-2. Pin Functions, SN65C1168E

PIN				I/O	DESCRIPTION
NAME	SO	TSSOP	VQFN		
1A	2	2	2	I	RS422 differential input (noninverting) to receiver 1
2A	6	6	6	I	RS422 differential input (noninverting) to receiver 2
1B	1	1	1	I	RS422 differential input (inverting) to receiver 1
2B	7	7	7	I	RS422 differential input (inverting) to receiver 2
1D	15	15	15	I	Logic data input to RS422 driver 1
2D	9	9	9	I	Logic data input to RS422 driver 2
1DE	4	4	4	I	Driver 1 enable (active high)
2DE	12	12	12	I	Driver 2 enable (active high)
GND	8	8	8	—	Device ground
1R	3	3	3	O	Logic data output of RS422 receiver 1
2R	5	5	5	O	Logic data output of RS422 receiver 2
V_{CC}	16	16	16	—	Power supply
1Y	14	14	14	O	RS-422 differential (noninverting) driver output 1
2Y	10	10	10	O	RS-422 differential (noninverting) driver output 2
1Z	13	13	13	O	RS-422 differential (noninverting) driver output 1
2Z	11	11	11	O	RS-422 differential (noninverting) driver output 2

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5 Specifications

5.1 Absolute Maximum Ratings

over recommended operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.5	7	V
V_I	Input voltage	Driver, DE, RE	–0.5	7	V
		A or B, Receiver	–14	14	
V_{ID}	Differential input voltage(3)	Receiver	–14	14	V
V_O	Output voltage	Driver	–0.5	7	V
		Receiver	–0.5	V_{CC} + 0.5	
I_{IK}	Input clamp current	Driver, V_I < 0		–20	mA
I_{OK}	Output clamp current	Driver, V_O < 0		–20	mA
		Receiver		±20	
I_O	Output current	Driver		±150	mA
		Receiver		±25	
I_{CC}	Supply current			200	mA
	GND current			–200	mA
T_J	Operating virtual junction temperature			150	°C
T_A	Operating free-air temperature		–40	85	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential input voltage are with respect to the network GND.
(3) Differential input voltage is measured at the noninverting terminal, with respect to the inverting terminal.

5.2 Driver Output and Receiver Input ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±15000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		IEC 61000-4-2, air-gap discharge	±8000	
		IEC 61000-4-2, contact discharge	±8000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IC}	Common-mode input voltage(1)	Receiver			±7	V
V_{ID}	Differential input voltage	Receiver			±7	V
V_I	Input voltage	Except A, B	0		5.5	V
V_O	Output voltage	Receiver	0		V_{CC}	V
V_{IH}	High-level input voltage	Except A, B	2			V
V_{IL}	Low-level input voltage	Except A, B			0.8	V
I_{OH}	High-level output current	Receiver			–6	mA
		Driver			–20	
I_{OL}	Low-level output current	Receiver			6	mA
		Driver			20	
T_A	Operating free-air temperature		–40		85	°C

(1) Refer to TIA/EIA-422-B for exact conditions.

5.4 Thermal Information

THERMAL METRIC(1)		SN65C116xE			UNIT
		SO (NS)	PW (TSSOP)	RGY (VQFN)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	88.5	107.5	48.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.2	38.4	46.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	50.7	53.7	24.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.5	3.2	2.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.3	53.1	24.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	8.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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5.5 Driver Section Electrical Characteristics

over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18mA					–1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2V,	V_{IL} = 0.8V,	I_{OH} = –20mA	2.4	3.5		V
V_{OL}	Low-level output voltage	V_{IH} = 2V,	V_{IL} = 0.8V,	I_{OL} = 20mA		0.2	0.4	V
$\|V_{OD1}\|$	Differential output voltage 1	I_O = 0mA			2		6	V
$\|V_{OD2}\|$	Differential output voltage 2	R_L = 100Ω,	See 図 6-1 (2)		2	3.7		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage	R_L = 100Ω,	See 図 6-1 (2)				±0.4	V
V_{OC}	Common-mode output voltage	R_L = 100Ω,	See 図 6-1 (2)				±3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage	R_L = 100Ω,	See 図 6-1 (2)				±0.4	V
$I_{O(OFF)}$	Output current with power off	V_{CC} = 0V	V_O = 6V				100	µA
			V_O = –0.25V				100	
I_{OZ}	High-impedance-state output current	V_O = 2.5V					20	µA
		V_O = 5V					–20	
I_{IH}	High-level input current	V_I = V_{CC} or V_{IH}					1	µA
I_{IL}	Low-level input current	V_I = GND or V_{IL}					–1	µA
I_{OS}	Short-circuit output current	V_O = V_{CC} or GND(3)			–30		–150	mA
I_{CC}	Supply current (total package)	No load, Enabled	V_I = V_{CC} or GND			4	6	mA
			V_I = 2.4 or 0.5V(4)			5	9	
C_i	Input capacitance					6		pF

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) Refer to TIA/EIA-422-B for exact conditions.
(3) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
(4) This parameter is measured per input, while the other inputs are at V_{CC} or GND.

5.6 Receiver Section Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage, differential input						0.2	V
$V_{IT–}$	Negative-going input threshold voltage, differential input				–0.2(2)			V
V_{hys}	Input hysteresis (V_{IT+} – $V_{IT–}$)					60		mV
V_{IK}	Input clamp voltage, $\overline{RE}$	SN65C1167E	I_I = –18mA				–1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200mV,	I_{OH} = –6mA	3.8	4.2		V
V_{OL}	Low-level output voltage		V_{ID} = –200mV,	I_{OL} = 6mA		0.1	0.3	V
I_{OZ}	High-impedance state output current	SN65C1167E	V_O = V_{CC} or GND			±0.5	±5	µA
I_I	Line input current		Other input at 0V	V_I = 10V			1.5	mA
				V_I = –10V			–2.5	
I_I	Enable input current, $\overline{RE}$	SN65C1167E	V_I = V_{CC} or GND				±1	µA
r_I	Input resistance		V_{IC} = –7V to 7V,	Other input at 0V	4	17		kΩ
I_{CC}	Supply current (total package)		No load, Enabled	V_I = V_{CC} or GND		4	6	mA
				V_{IH} = 2.4V or 0.5V(3)		5	9	

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) Refer to TIA/EIA-422-B for exact conditions.

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5.7 Driver Section Switching Characteristics

over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	R1 = R2 = 50Ω, C1 = C2 = C3 = 40pF, See 図 6-2	R3 = 500Ω, S1 is open,		8	16	ns
t_{PLH}	Propagation delay time, low- to high-level output				8	16	ns
$t_{sk(p)}$	Pulse skew				1.5	4	ns
t_r	Rise time	R1 = R2 = 50Ω, C1 = C2 = C3 = 40pF, See 図 6-3	R3 = 500Ω, S1 is open,		5	8	ns
t_f	Fall time				5	8	ns
t_{PZH}	Output-enable time to high level	R1 = R2 = 50Ω, C1 = C2 = C3 = 40pF, See 図 6-4	R3 = 500Ω, S1 is closed,		10	19	ns
t_{PZL}	Output-enable time to low level				10	19	ns
t_{PHZ}	Output-disable time from high level	R1 = R2 = 50Ω, C1 = C2 = C3 = 40pF, See 図 6-4	R3 = 500Ω, S1 is closed,		7	16	ns
t_{PLZ}	Output-disable time from low level				7	16	ns
f_{SW}	Maximum switching frequency	R1 = R2 = 50Ω, C1 = C2 = C3 = 40pF, See 図 6-3	R3 = 500Ω, S1 is open,	20			MHz

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.

5.8 Receiver Section Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)(2)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output		See 図 6-5		9	15	27	ns
t_{PHL}	Propagation delay time, high- to low-level output		See 図 6-5		9	15	27	ns
t_{TLH}	Transition time, low- to high-level output		V_{IC} = V,	See 図 6-5		4	9	ns
t_{THL}	Transition time, high- to low-level output					4	9	ns
t_{PZH}	Output-enable time to high level	SN65C1167E	R_L = 1kΩ, C_L= 50pF	See 図 6-6		7	22	ns
t_{PZL}	Output-enable time to low level					7	22	ns
t_{PHZ}	Output-disable time from high level					12	22	ns
t_{PLZ}	Output-disable time from low level					12	22	ns

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) Measured per input while the other inputs are at V_{CC} or GND

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6 Parameter Measurement Information

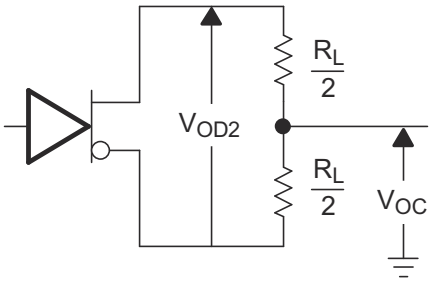
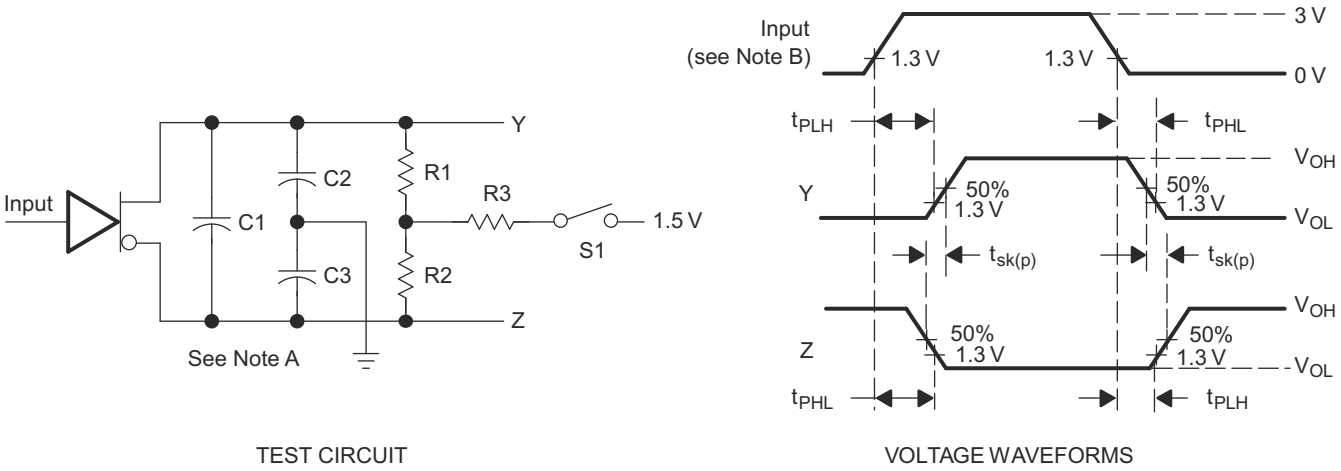


図 6-1. Driver Test Circuit, V_{OD} and V_{OC}

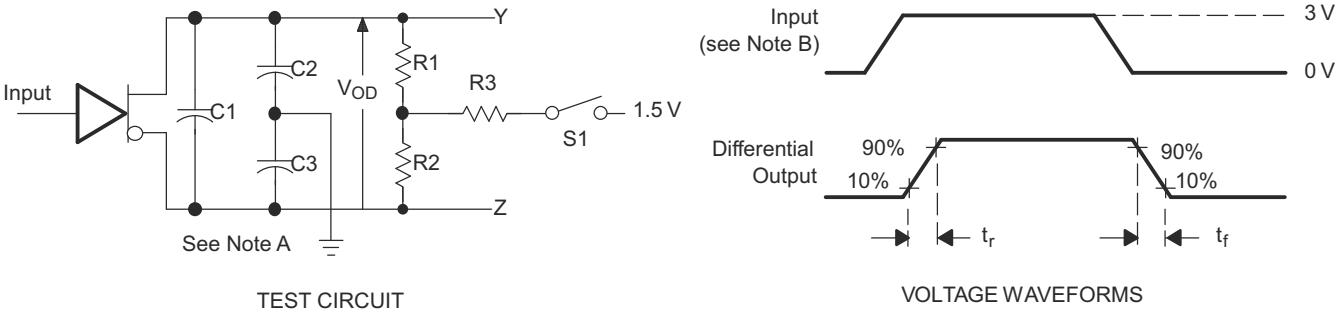


TEST CIRCUIT VOLTAGE WAVEFORMS

A. C1, C2, and C3 include probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ns.

図 6-2. Driver Test Circuit and Voltage Waveforms



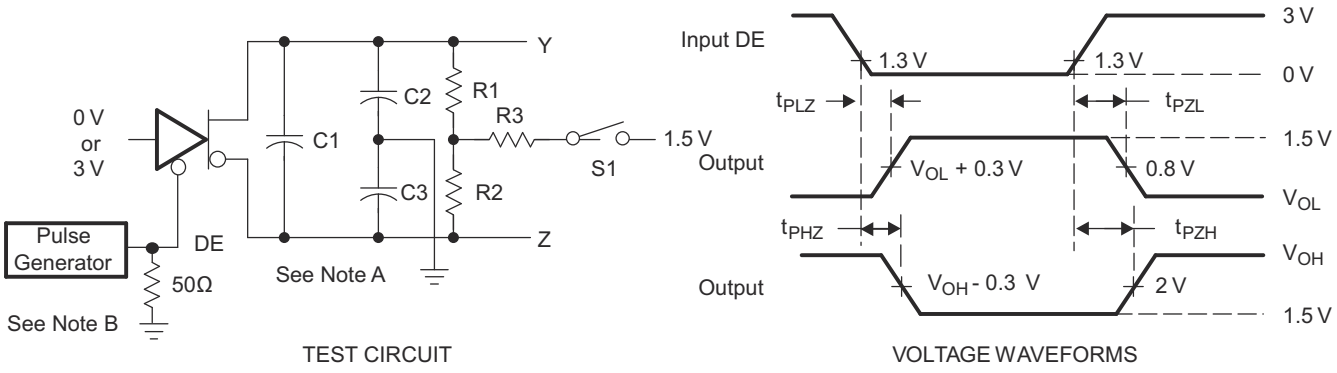
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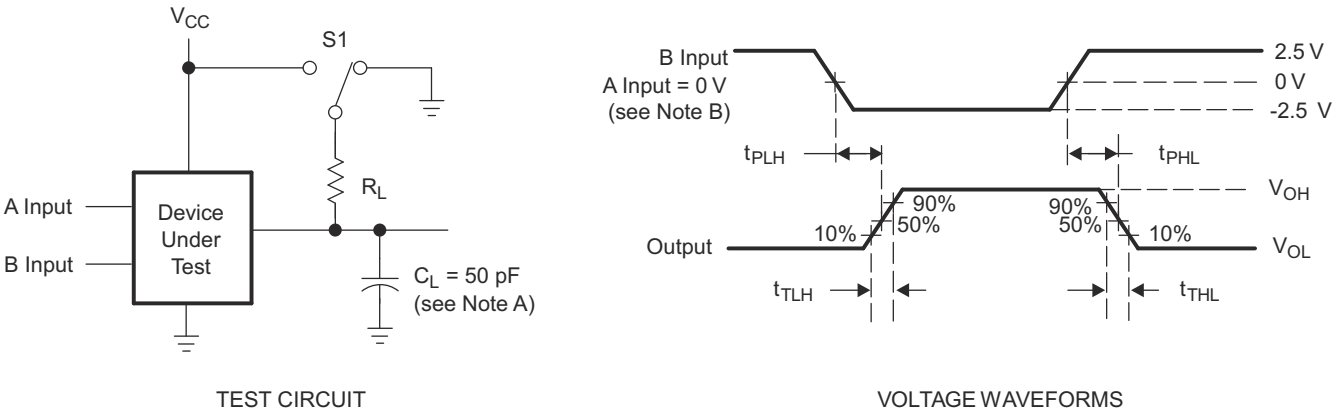
図 6-3. Driver Test Circuit and Voltage Waveforms

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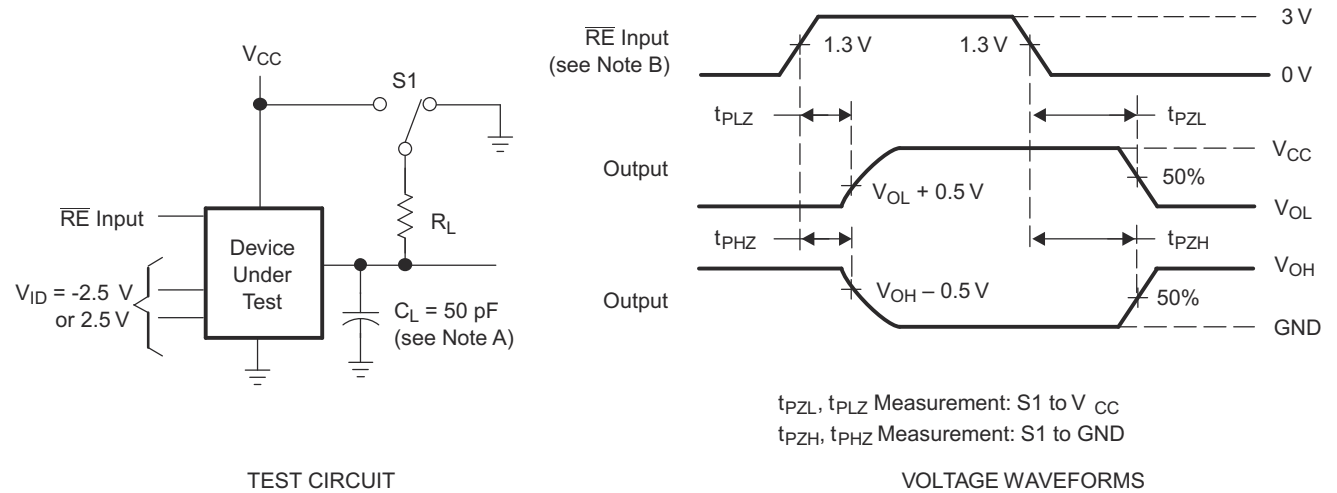
A. C1, C2, and C3 include probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ns.

図 6-4. Driver Test Circuit and Voltage Waveforms



A. C1, C2, and C3 include probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ns.

図 6-5. Receiver Test Circuit and Voltage Waveforms



A. C1, C2, and C3 include probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ns.

図 6-6. Receiver Test Circuit and Voltage Waveforms

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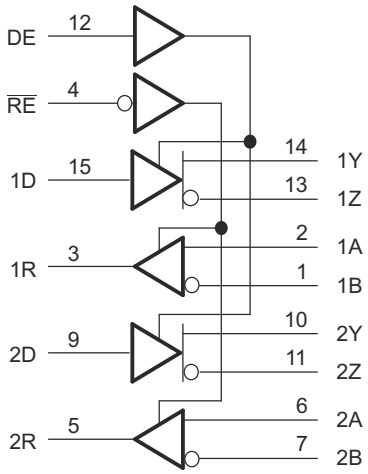
7 Detailed Description

7.1 Overview

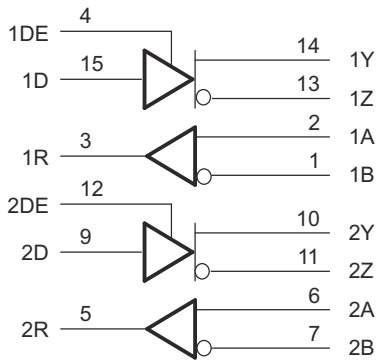
The SN65C1167E and SN65C1168E consist of dual drivers and dual receivers powered from a single 5V supply. These devices meet the requirements of TIA/EIA-422-B and ITU recommendation V.11.

7.2 Functional Block Diagram

SN65C1167E



SN65C1168E



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7.3 Feature Description

7.3.1 Active High Driver Output Enables

Both drivers of SN65C1167E can be configured with the single DE logic input. Both drivers are set at high-impedance when disabled.

SN65C1168E drivers can be configured individually by 1DE and 2DE logic inputs. Both drivers are set at high-impedance when disabled.

7.3.2 Active Low Receiver Enables

Both SN65C1167E receivers can be configured with the single $\overline{RE}$ logic input. Receiver logic outputs are set at high-impedance when disabled.

7.4 Device Functional Modes

表 7-1 and 表 7-2 list the functional modes of SN65C1167E and SN65C1168E.

表 7-1. Each Driver

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

表 7-2. SN65C1167E, Each Receiver(1)

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
V_{ID} ≥ 0.2 V	L	H
–0.2 V < V_{ID} < 0.2 V	L	?
V_{ID} ≤ –0.2 V	L	L
X	H	Z
Open	L	H

(1) H = High level, L = Low level, ? = Indeterminate, X = Irrelevant, Z = High impedance (off)

表 7-3. SN65C1168E, Each Receiver(1)

DIFFERENTIAL INPUTS A–B	OUTPUT R
V_{ID} ≥ 0.2V	H
–0.2V < V_{ID} < 0.2V	?
V_{ID} ≤ –0.2V	L
Open	H

(1) H = High level, L = Low level, ? = Indeterminate

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8 Application and Implementation

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8.1 Application Information

図 8-1 shows a typical RS-422 application. One transmitter is able to broadcast to multiple receiving nodes connected together over a shared differential bus. Twisted-pair cabling with a controlled differential impedance is used, and a termination resistance is placed at the farthest receive end of the cable in order to match the transmission line impedance and minimize signal reflections.

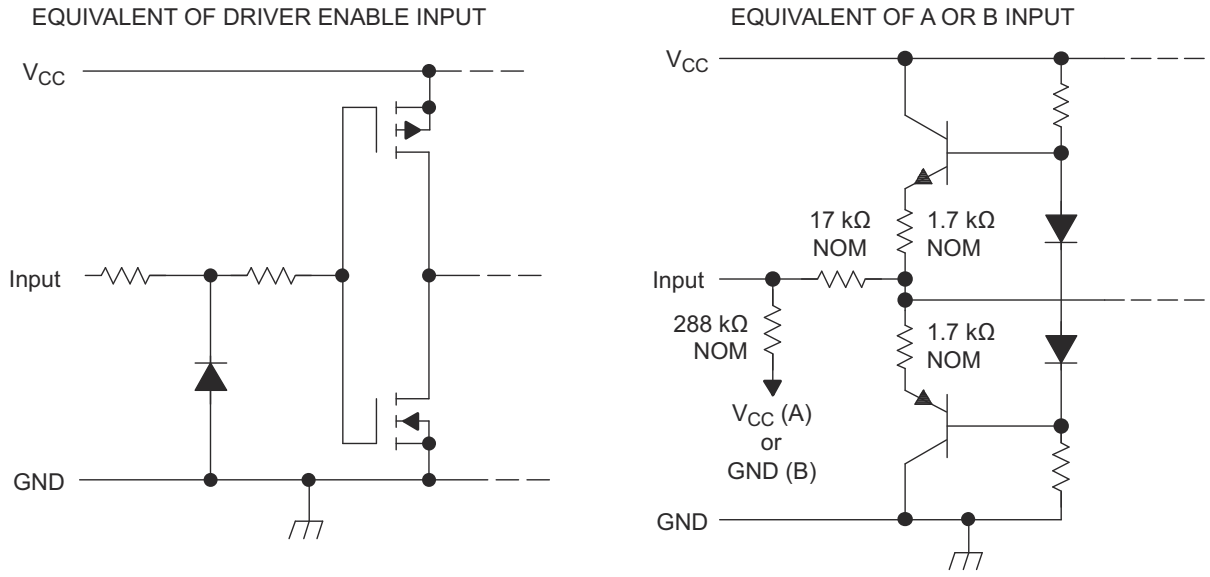


図 8-1. Schematic of Inputs

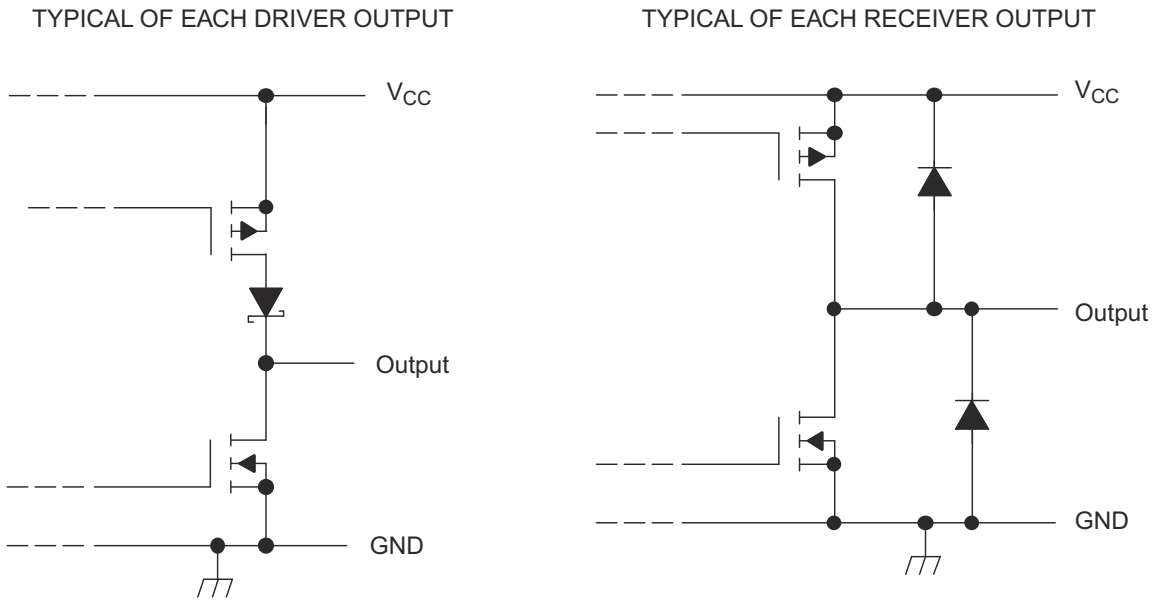


図 8-2. Schematic of Outputs

8.2 Typical Application

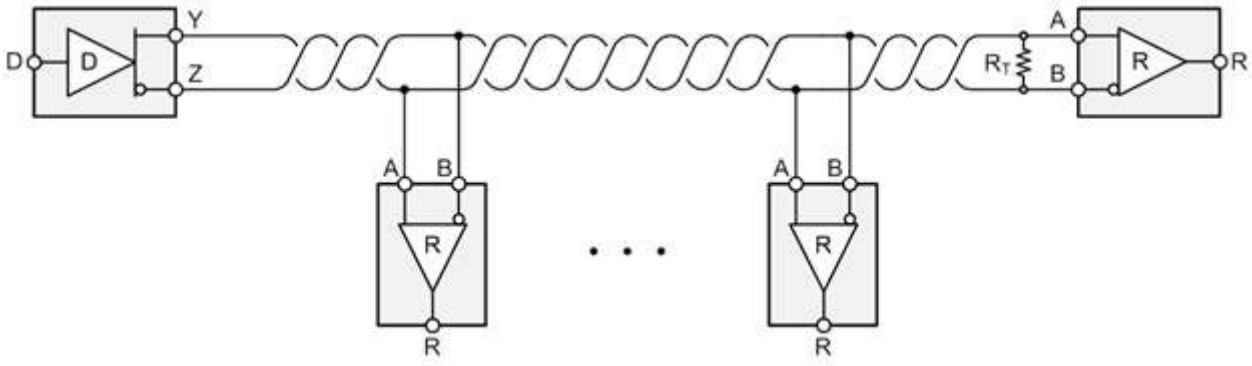


図 8-3. Typical RS-422 Application

8.2.1 Design Requirements

A typical RS-422 implementation using SN65C116xE requires the following:

- 5V power source.
- Connector that ensures the correct polarity for port pins.
- Cabling that supports the desired operating rate and transmission distance.

8.2.2 Detailed Design Procedure

Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line. If desired, add external fail-safe biasing to ensure ±200 mV on the A-B port when the driver circuit is disabled.

8.3 Power Supply Recommendations

Use a 5V power supply for V_{CC} place 0.1µF bypass capacitors close to the power supply pins to reduce errors coupling in from noisy or high impedance power supplies.

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9 Device and Documentation Support

9.1 Device Support

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (May 2017) to Revision C (February 2024)	Page
• 「製品情報」表を「パッケージ情報」表に変更	1
• Deleted the thermal packaging information from the *Absolute Maximum Ratings*	5
• Changed the *Thermal Information* table	6

Changes from Revision A (April 2007) to Revision B (May 2017)	Page
• 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1
• Changed the Rise Time Max value From: 10 ns To: 8 ns in the *Driver Section Switching Characteristics* table	8
• Changed the Fall Time Max value From: 10 ns To: 8 ns in the *Driver Section Switching Characteristics* table.	8
• Added Maximum switching frequency to the *Driver Section Switching Characteristics* table	8

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11 Mechanical, Packaging, and Orderable Information

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65C1167ENS	Obsolete	Production	SOP (NS) | 16	-	-	Call TI	Call TI	-40 to 85	65C1167E
SN65C1167ENSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1167E
SN65C1167ENSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1167E
SN65C1167ENSRG4	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1167E
SN65C1167ENSRG4.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1167E
SN65C1167EPW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	CB1167E
SN65C1167EPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1167E
SN65C1167EPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1167E
SN65C1167EPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1167E
SN65C1167EPWRG4.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1167E
SN65C1167ERGYR	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1167
SN65C1167ERGYR.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1167
SN65C1167ERGYRG4	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1167
SN65C1167ERGYRG4.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1167
SN65C1168ENSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1168E
SN65C1168ENSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1168E
SN65C1168EPW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	CB1168E
SN65C1168EPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168E
SN65C1168EPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168E
SN65C1168EPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168E
SN65C1168ERGYR	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB1168
SN65C1168ERGYR.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB1168
SN65C1168ERGYRG4	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168
SN65C1168ERGYRG4.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168

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(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

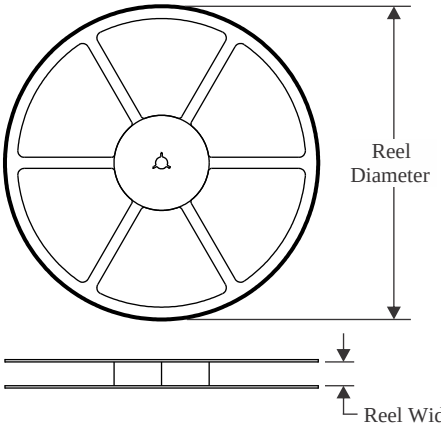
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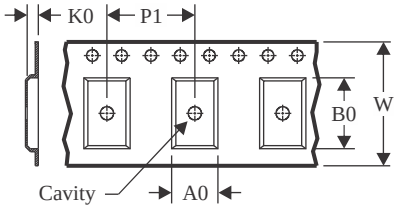
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

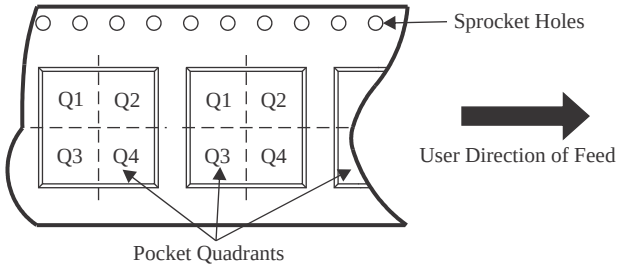


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

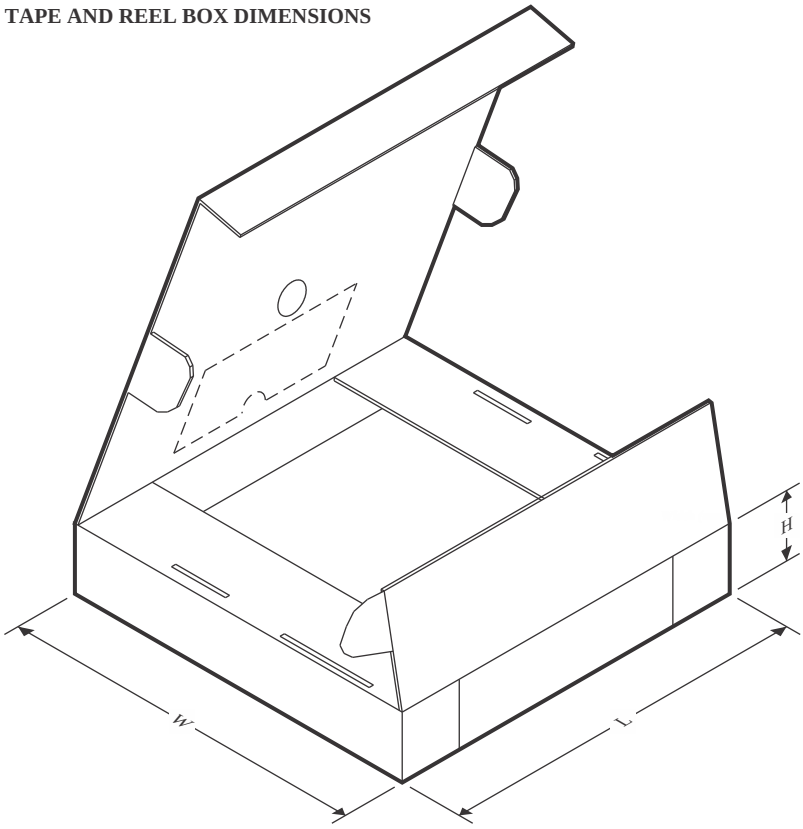
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

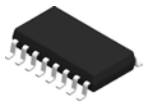
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C1167ENSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN65C1167ENSRG4	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN65C1167EPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65C1167EPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65C1167ERGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN65C1167ERGYRG4	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN65C1168ENSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN65C1168EPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65C1168ERGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN65C1168ERGYRG4	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C1167ENSR	SOP	NS	16	2000	353.0	353.0	32.0
SN65C1167ENSRG4	SOP	NS	16	2000	353.0	353.0	32.0
SN65C1167EPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN65C1167EPWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
SN65C1167ERGYR	VQFN	RGY	16	3000	360.0	360.0	36.0
SN65C1167ERGYRG4	VQFN	RGY	16	3000	360.0	360.0	36.0
SN65C1168ENSR	SOP	NS	16	2000	353.0	353.0	32.0
SN65C1168EPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN65C1168ERGYR	VQFN	RGY	16	3000	360.0	360.0	36.0
SN65C1168ERGYRG4	VQFN	RGY	16	3000	360.0	360.0	36.0

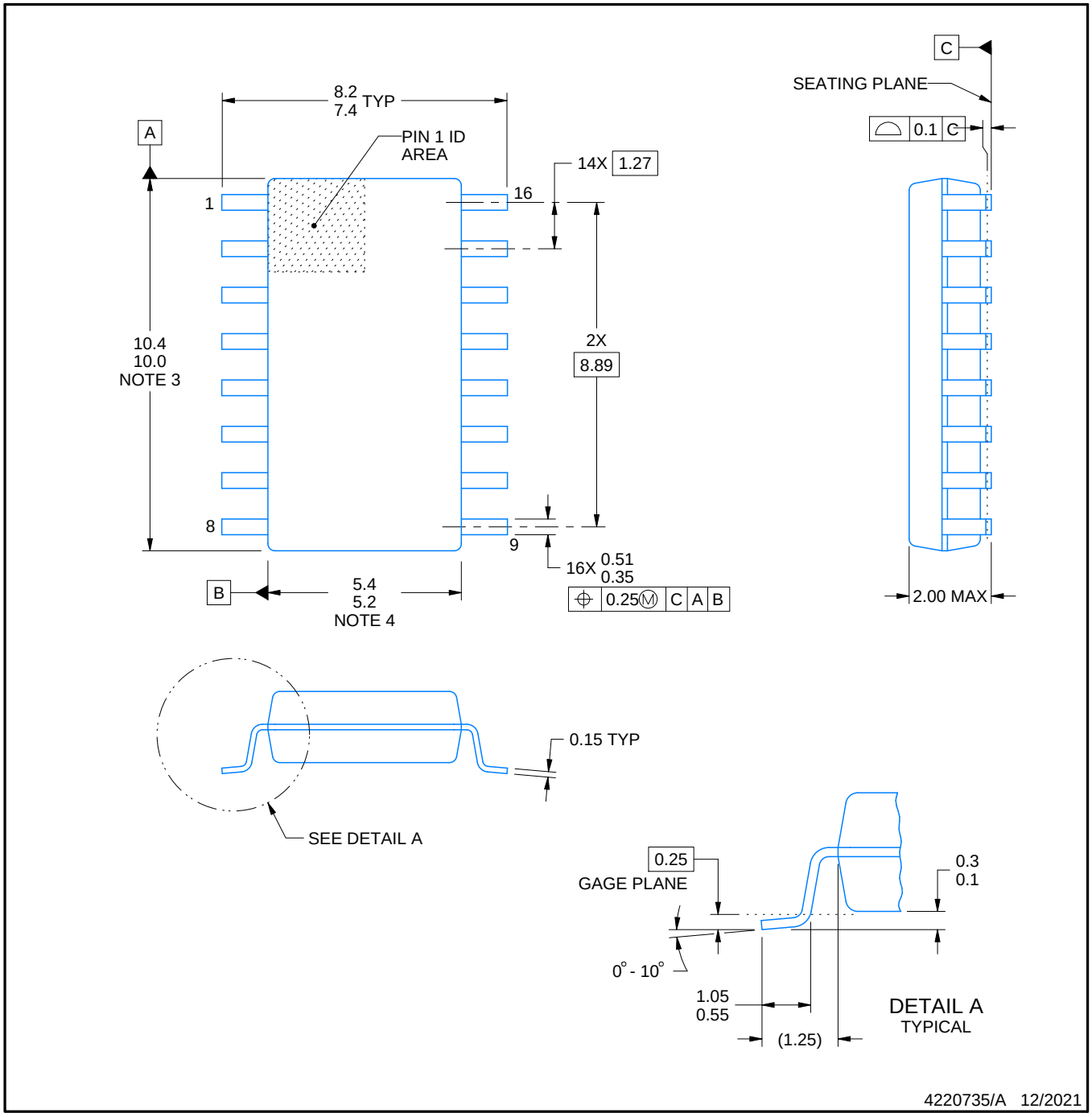


PACKAGE OUTLINE

NS0016A

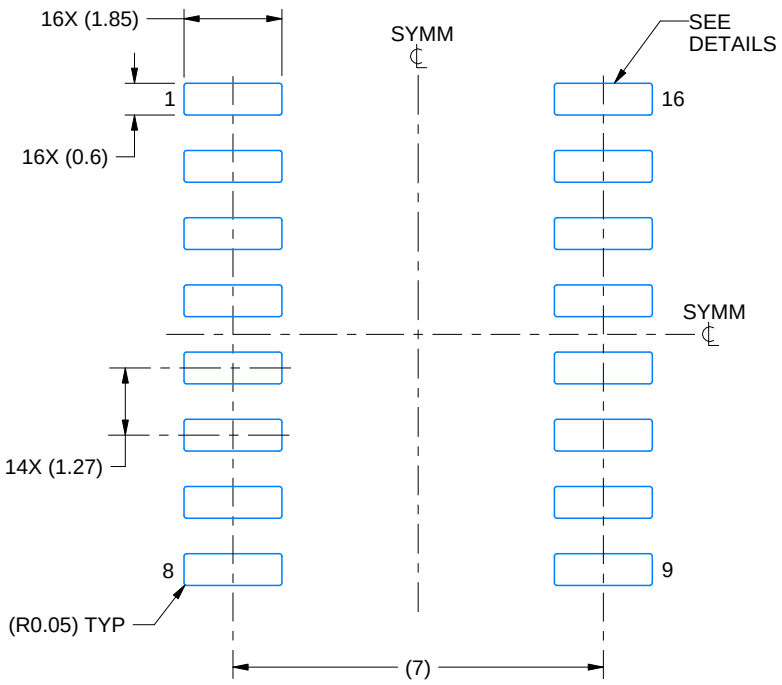
SOP - 2.00 mm max height

SOP

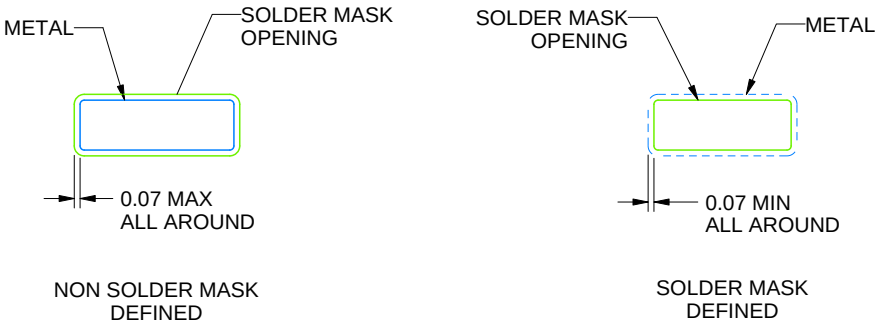


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

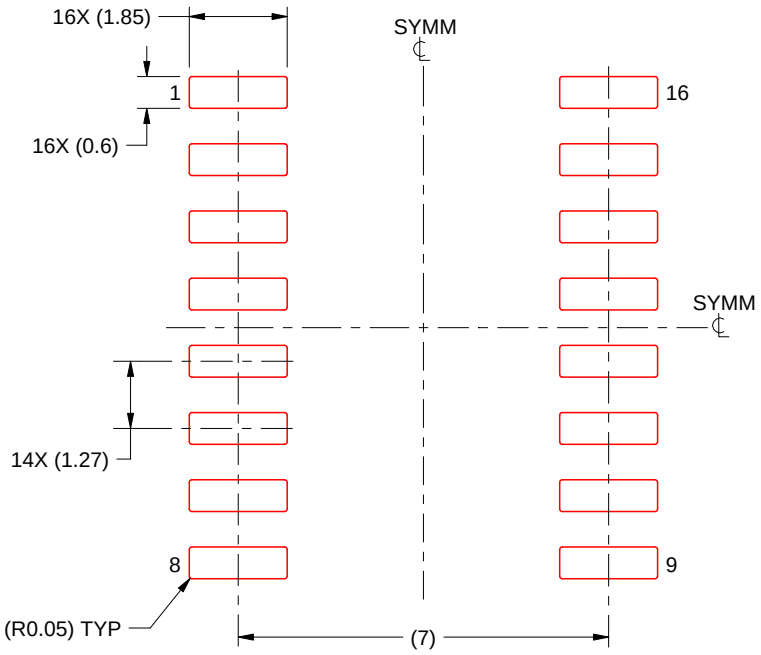
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

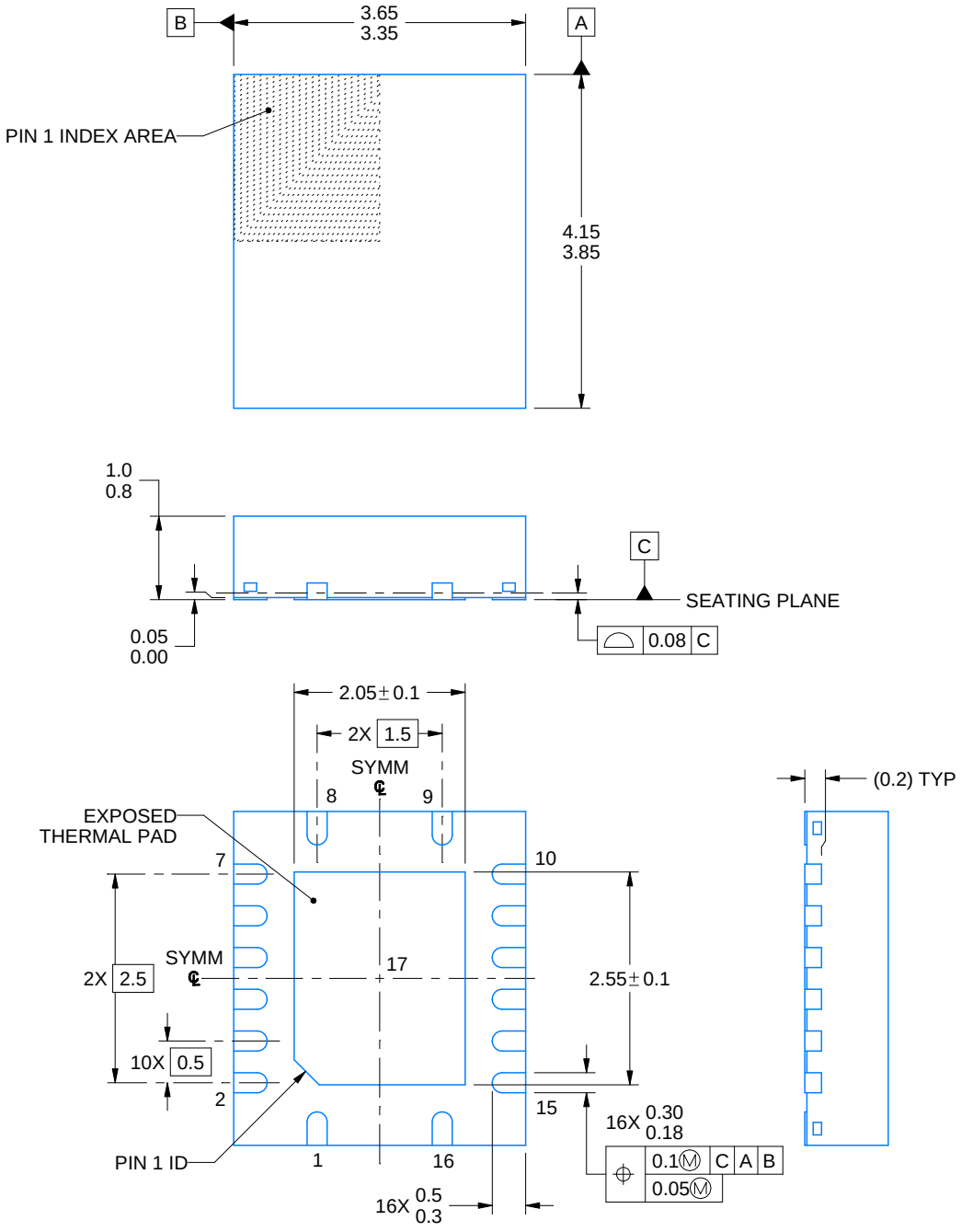
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

RGY0016A

PACKAGE OUTLINE

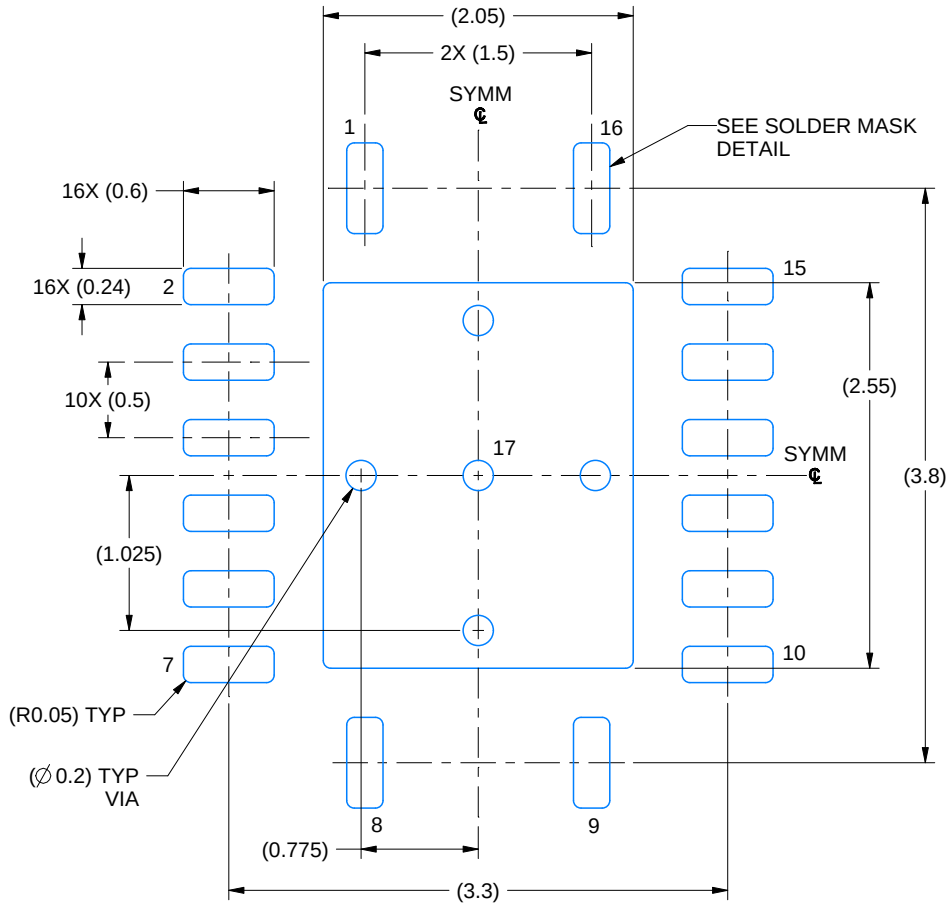
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

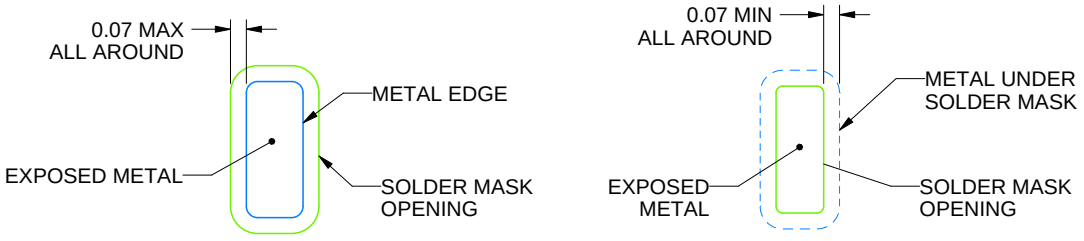


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

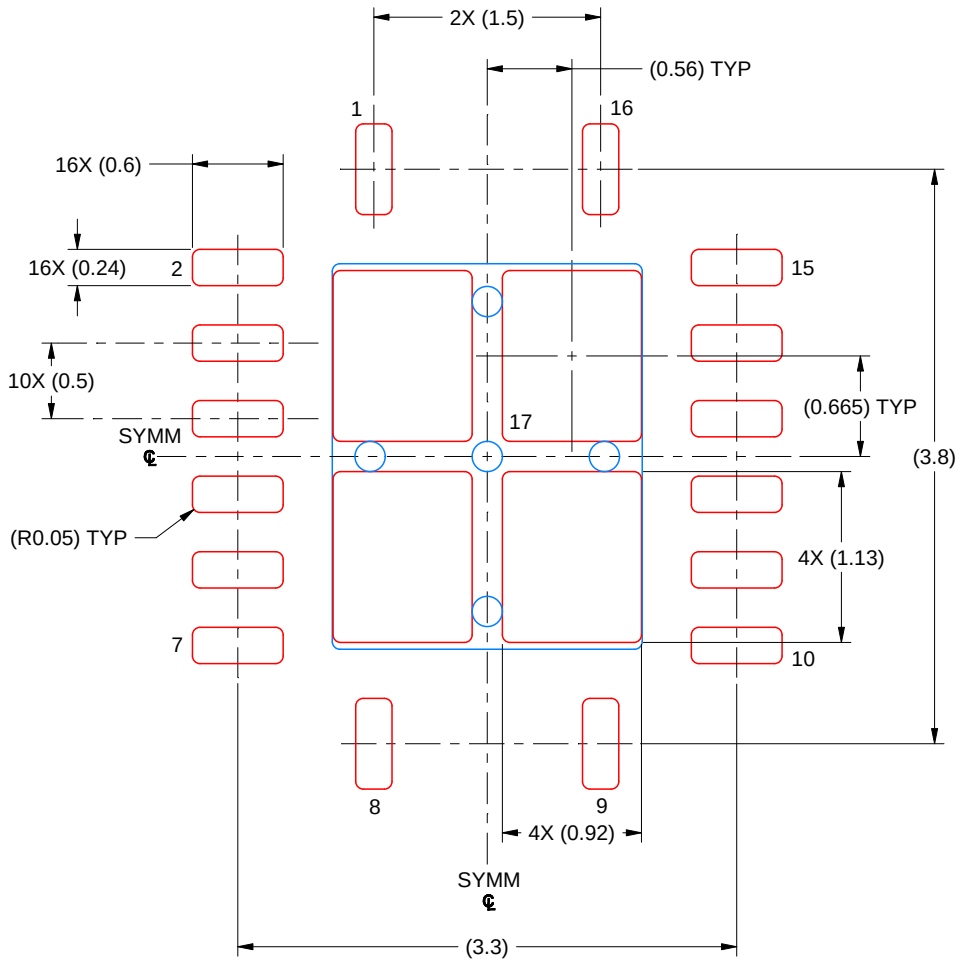


SOLDER MASK DETAILS

4225140/A 07/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225140/A 07/2019

NOTES: (continued)

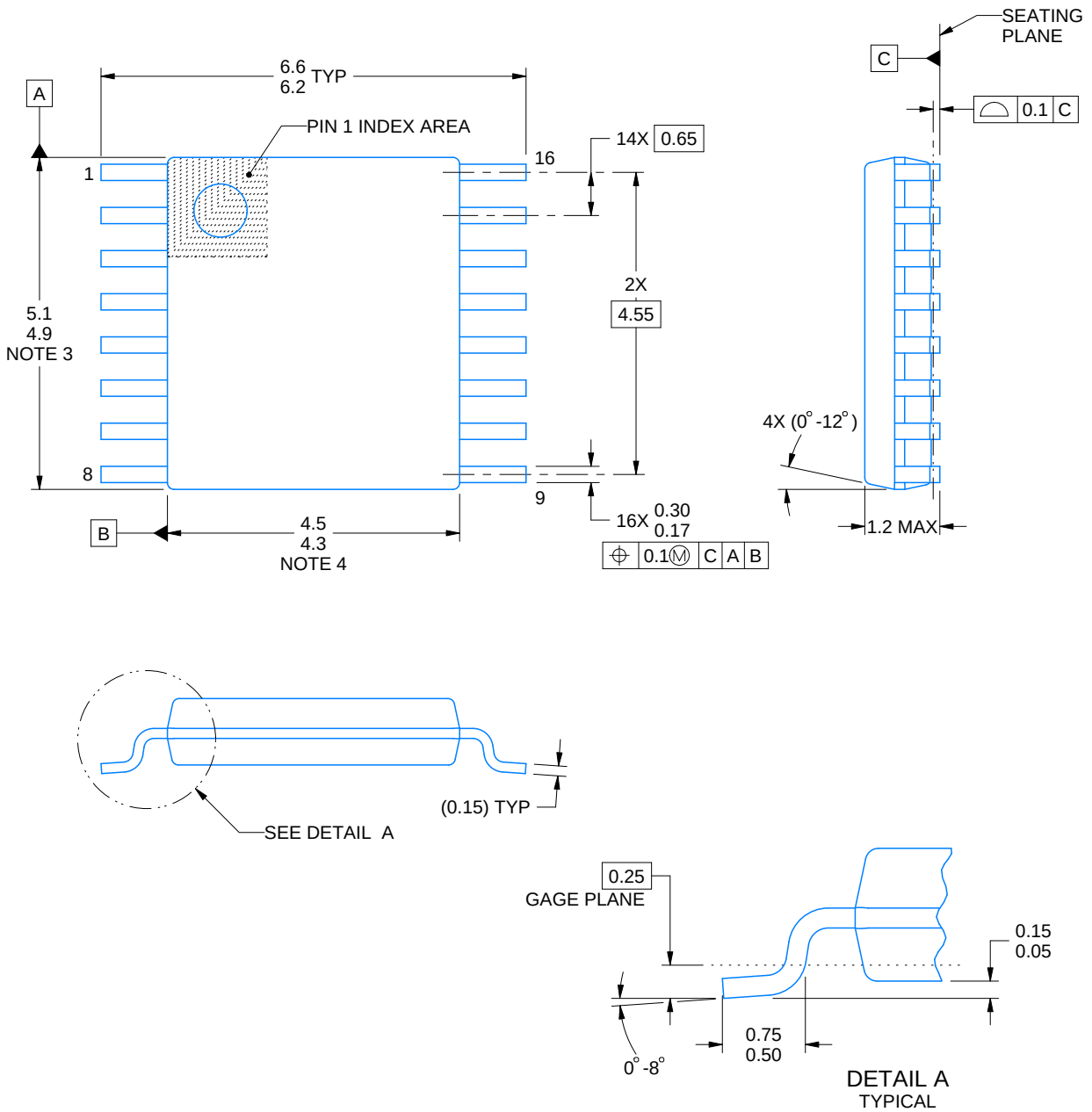
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0016A

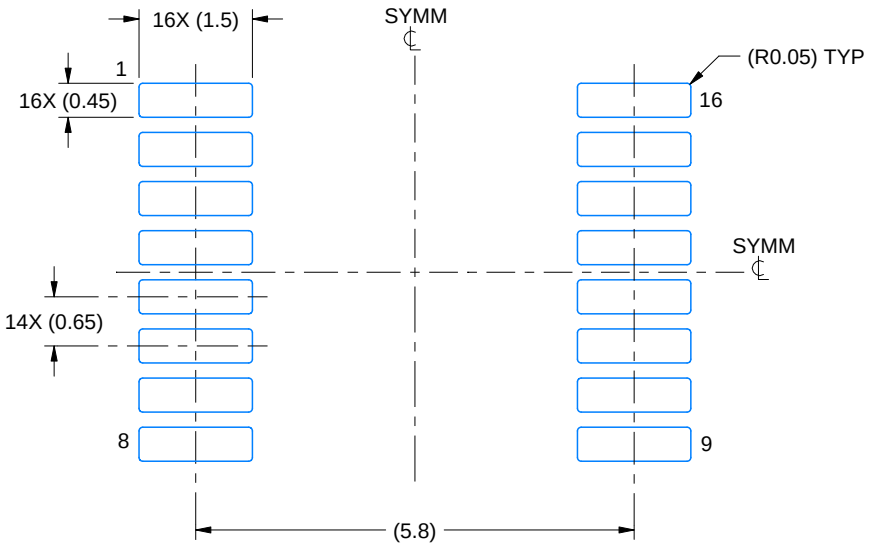
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

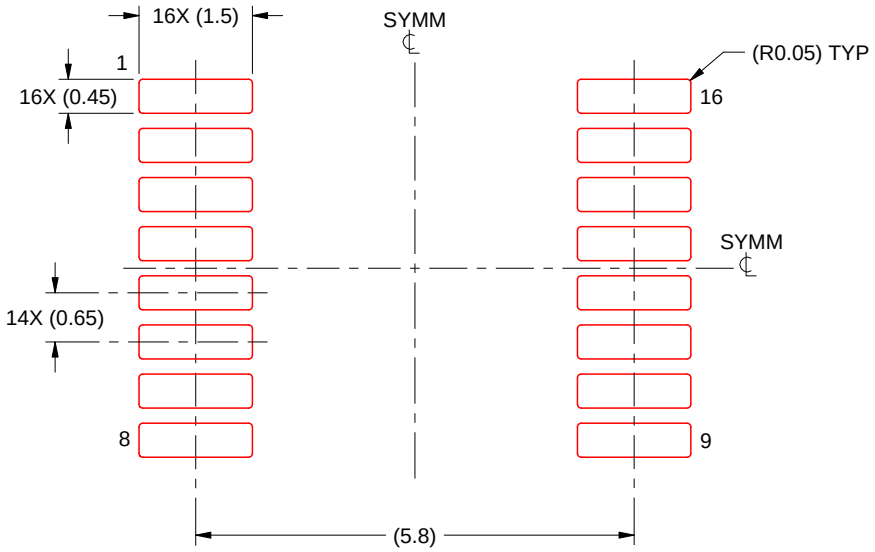


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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