

3V~5.5V シングル・チャネル RS-232 対応ライン・ドライバ/レシーバ

1 特長

- 3V~5.5V の V_{CC} 電源で動作
- 最大 1Mbit/s で動作
- 小さいスタンバイ電流: 1 μ A (標準値)
- 外付けコンデンサ: $4 \times 0.1\mu$ F
- 3.3V 電源で 5V ロジック入力を受容
- 人体モデル (HBM) で ± 15 kV を超える RS-232 バス・ピン ESD 保護
- 自動パワー・ダウン機能により、ドライバを自動的にディスエーブルすることで電力を節約

2 アプリケーション

- 産業用 PC
- 有線ネットワーク
- データ・センターおよびエンタープライズ・コンピューティング
- バッテリ駆動システム
- PDA
- ノートブック PC
- ノート PC
- パームトップ PC
- ハンドヘルド機器

3 概要

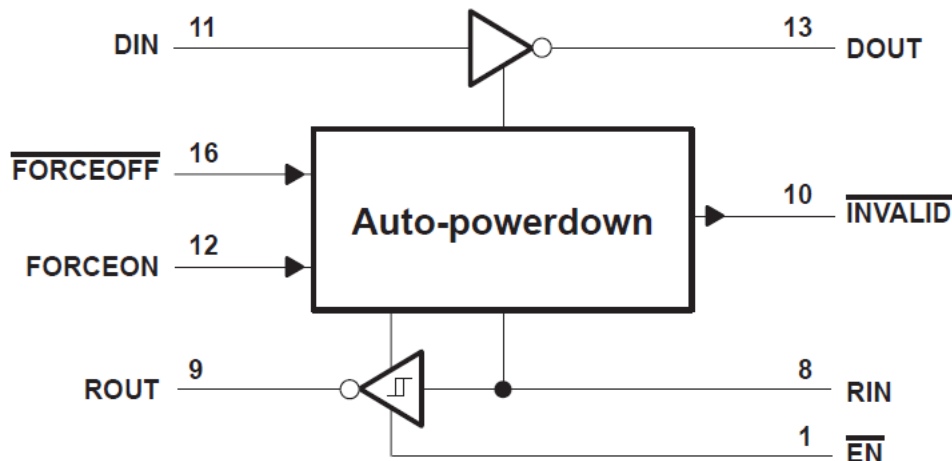
SN65C3221 と SN75C3221 は 1 つのライン・ドライバ、1 つのライン・レシーバ、1 つのデュアル・チャージ・ポンプ回路で構成されており、 ± 15 kV のピン間 (シリアル・ポート接続ピン、GND を含む) ESD 保護機能を備えています。これらのデバイスは、非同期通信コントローラとシリアルポート・コネクタの間の電氣的インターフェイスとして機能します。チャージ・ポンプと 4 つの小さな外付けコンデンサにより、3V~5.5V の単一電源で動作できます。これらのデバイスは最大 1Mbit/s のデータ信号速度、24V/ μ s ~ 150V/ μ s のドライバ出力スルーレートで動作します。

シリアル・ポートが使われていない際のパワー・マネージメントを柔軟に制御できます。FORCEON が LOW かつ FORCEOFF が HIGH の場合、自動パワー・ダウン機能が動作します。この動作モード中、デバイスがレシーバ入力で有効な RS-232 信号を検出しない場合、ドライバ出力はディスエーブルになります。FORCEOFF を LOW に設定しかつ EN を HIGH に設定すると、ドライバとレシーバはどちらもシャットダウンされ、消費電流は 1 μ A に減少します。シリアル・ポートを切り離した場合、またはペリフェラル・ドライバをオフにした場合、自動パワー・ダウン状態になります。FORCEON と FORCEOFF を HIGH にすると、自動パワー・ダウンを無効にできます。自動パワー・ダウンが有効な場合、レシーバの入力に有効な信号が印加されると、デバイスは自動的にアクティブになります。INVALID 出力は、レシーバの入力に RS-232 信号が存在するかどうかをユーザーに通知します。INVALID は、レシーバの入力電圧が 2.7V を上回っている場合、-2.7V を下回っている場合、-0.3V と 0.3V の間にあった期間が 30 μ s 未満である場合のいずれかの場合、HIGH (有効データ) になります。INVALID は、レシーバの入力電圧が 30 μ s を超える期間 -0.3V と 0.3V の間にある場合、LOW (無効データ) になります。レシーバの入力レベルについては、図 7-5 を参照してください。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
SNx5C3221	SSOP (DB) 16	6.20mm × 5.30mm
	TSSOP (PW) 16	10.3mm × 7.50mm

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



論理図 (正論理)



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (October 2004) to Revision F (July 2021)	Page
• 「アプリケーション」の一覧を変更.....	1
• 注文情報の表を削除.....	1
• 製品情報の表を追加.....	1
• Removed the thermal parameters from <i>Absolute Maximum Ratings</i> table and moved them to <i>Thermal Information</i> table.....	4
• Added <i>ESD Ratings</i> table. Moved the driver and receiver ESD specifications to this table.....	4
• Changed the thermal parameters for PW package of SN65C3221 and DB package of SN75C3221. Added additional thermal parameters for both the packages in the <i>Thermal Information</i> table.....	5
• Added the <i>Detailed Description</i> section.....	11

5 Pin Configuration and Functions

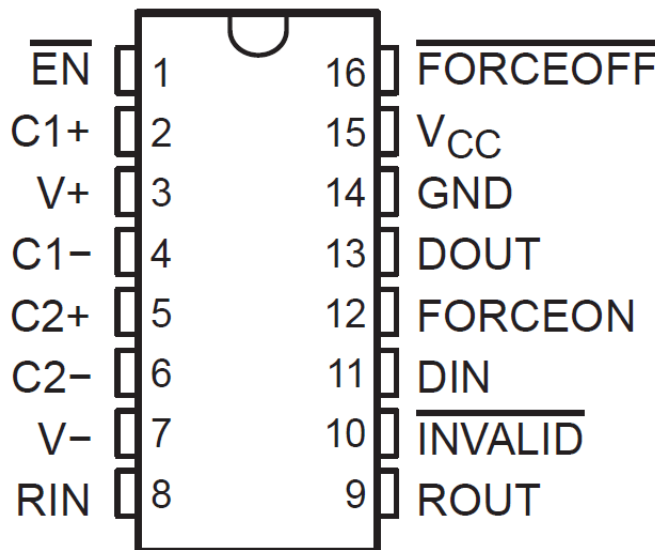


图 5-1. DB or PW Package
Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
C1+	2	—	Positive terminals of the voltage-doubler charge-pump capacitors
C2+	5		
C1–	4	—	Negative terminals of the voltage-doubler charge-pump capacitors
C2–	6		
DIN	11	I	Driver input
DOUT	13	O	RS-232 driver output
EN	1	I	Low input enables receiver ROUT output. High input sets ROUT to high impedance.
FORCEOFF	16	I	Automatic power-down control input
FORCEON	12	I	Automatic power-down control input
GND	14	—	Ground
INVALID	10	O	Invalid output pin. Output low when all RIN inputs are unpowered.
RIN	8	I	RS-232 receiver input
ROUT	9	O	Receiver output
V _{CC}	15	—	3-V to 5.5-V supply voltage
V+	3	O	5.5-V supply generated by the charge pump
V–	7	O	–5.5-V supply generated by the charge pump

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		−0.3	6	V
V ₊	Positive output supply voltage range ⁽²⁾		−0.3	7	V
V _−	Negative output supply voltage range ⁽²⁾		−7	0.3	V
V ₊ − V _−	Supply voltage difference ⁽²⁾			13	V
V _I	Input voltage range	Driver (FORCEOFF, FORCEON, $\overline{\text{EN}}$)	−0.3	6	V
		Receiver	−25	25	
V _O	Output voltage range	Driver	−13.2	13.2	V
		Receiver (INVALID)	−0.3	V _{CC} + 0.3	
T _J	Operating virtual junction temperature			150	°C
T _{stg}	Storage temperature		−65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under [セクション 6.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal GND.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ¹	RIN and DOUT Pins	±15000	V
		All other pins	±3000	
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ²	All pins	±1500	

6.3 Recommended Operating Conditions⁽¹⁾

(see [図 9-1](#))

			MIN	NOM	MAX	UNIT
	Supply voltage	V _{CC} = 3.3 V	3	3.3	3.6	V
		V _{CC} = 5 V	4.5	5	5.5	
V _{IH}	Driver and control high-level input voltage	DIN, FORCEOFF, FORCEON, $\overline{\text{EN}}$	V _{CC} = 3.3 V	2		V
			V _{CC} = 5 V	2.4		
V _{IL}	Driver and control low-level input voltage	DIN, FORCEOFF, FORCEON, $\overline{\text{EN}}$			0.8	V
V _I	Driver and control input voltage	DIN, FORCEOFF, FORCEON	0		5.5	V
V _I	Receiver input voltage		−25		25	V
T _A	Operating free-air temperature	SN65C3221	−40		85	°C
		SN75C3221	0		70	

- (1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.3.1 Thermal Information

THERMAL METRIC ¹		SN65C3221		SN75C3221		UNIT
		DB (SSOP)	PW (TSSOP)	DB (SSOP)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	82.0	110.9	105.8	108.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.7	41.7	51.9	41.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.4	57.2	57.6	51.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.0	4.2	14.1	3.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	43.8	56.6	56.8	50.9	°C/W

6.4 Electrical Characteristics

over recommended operating free-air temperature ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽²⁾ (see [Figure 9-1](#))

PARAMETER			TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
I_I	Input leakage current	FORCEOFF, FORCEON, EN			±0.01	±1	μA
I_{CC}	Supply current ($T_A = 25^\circ\text{C}$)	Auto-powerdown disabled	No load, FORCEOFF and FORCEON at V_{CC}		0.3	1	mA
		Powered off	No load, FORCEOFF at GND		1	10	μA
		Auto-powerdown enabled	No load, FORCEOFF at V_{CC} , FORCEON at GND, All RIN are open or grounded		1	10	

(1) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

(2) Test conditions are $C1-C4 = 0.1\text{ }\mu\text{F}$ at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; $C1 = 0.047\text{ }\mu\text{F}$, $C2-C4 = 0.33\text{ }\mu\text{F}$ at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

6.5 Electrical Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)⁽³⁾ (see [9-1](#))

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	DOUT at R _L = 3 kΩ to GND,	DIN = GND	5	5.4		V
V _{OL}	Low-level output voltage	DOUT at R _L = 3 kΩ to GND,	DIN = V _{CC}	–5	–5.4		V
I _{IH}	High-level input current	V _I = V _{CC}			±0.01	±1	μA
I _{IL}	Low-level input current	V _I at GND			±0.01	±1	μA
I _{OS}	Short-circuit output current ⁽²⁾	V _{CC} = 3.6 V,	V _O = 0 V		±35	±60	mA
		V _{CC} = 5.5 V,	V _O = 0 V		±35	±90	
r _o	Output resistance	V _{CC} , V ₊ , and V _– = 0 V,	V _O = ±2 V	300	10M		Ω
I _{off}	Output leakage current	FORCEOFF = GND	V _O = ±12 V, V _{CC} = 3 V to 3.6 V			±25	μA
			V _O = ±10 V, V _{CC} = 4.5 V to 5.5 V			±25	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

(3) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.6 Switching Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽³⁾ (see [9-1](#))

PARAMETER		TEST CONDITIONS			MIN	TYP ⁽¹⁾	MAX	UNIT	
Maximum data rate (see 7-1)		R _L = 3 kΩ	C _L = 1000 pF		250			kbit/s	
			C _L = 250 pF,	V _{CC} = 3 V to 4.5 V	1000				
			C _L = 1000 pF,	V _{CC} = 4.5 V to 5.5 V	1000				
t _{sk(p)}	Pulse skew ⁽²⁾	C _L = 150 pF to 2500 pF	R _L = 3 kΩ to 7 kΩ,	See 7-2	100			ns	
SR(tr)	Slew rate, transition region (see 7-1)	V _{CC} = 3.3 V, R _L = 3 kΩ to 7 kΩ	C _L = 150 pF to 1000 pF			18		150	V/μs

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

(3) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.7 Electrical Characteristics - Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽²⁾ (see [9-1](#))

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = –1 mA	V _{CC} – 0.6 V	V _{CC} – 0.1 V		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.6	2.4	V
		V _{CC} = 5 V		1.9	2.4	
V _{IT–}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.1		V
		V _{CC} = 5 V	0.8	1.4		
V _{hys}	Input hysteresis (V _{IT+} – V _{IT–})			0.5		V
I _{off}	Output leakage current	FORCEOFF = 0 V		±0.05	±10	μA
r _i	Input resistance	V _I = ±3 V to ±25 V	3	5	7	kΩ

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.8 Switching Characteristics - Receiver

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)⁽³⁾

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	$C_L = 150$ pF,	See 7-3		150		ns
t_{PHL}	Propagation delay time, high- to low-level output	$C_L = 150$ pF,	See 7-3		150		ns
t_{en}	Output enable time	$C_L = 150$ pF, $R_L = 3$ k Ω ,	See 7-4		200		ns
t_{dis}	Output disable time	$C_L = 150$ pF, $R_L = 3$ k Ω ,	See 7-4		200		ns
$t_{sk(p)}$	Pulse skew ⁽²⁾	See 7-3			50		ns

(1) All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25^\circ\text{C}$.

(2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

(3) Test conditions are C1–C4 = 0.1 μF at $V_{CC} = 3.3$ V $\pm$ 0.3 V; C1 = 0.047 μF , C2–C4 = 0.33 μF at $V_{CC} = 5$ V $\pm$ 0.5 V.

6.9 Electrical Characteristics - Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted) (see [7-5](#))

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$V_{T+}(\text{valid})$	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	FORCEON = GND, FORCEOFF = V_{CC}			2.7	V
$V_{T-}(\text{valid})$	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	FORCEON = GND, FORCEOFF = V_{CC}		–2.7		V
$V_{T}(\text{invalid})$	Receiver input threshold for $\overline{\text{INVALID}}$ low-level output voltage	FORCEON = GND, FORCEOFF = V_{CC}		–0.3	0.3	V
V_{OH}	$\overline{\text{INVALID}}$ high-level output voltage	$I_{OH} = -1$ mA, FORCEON = GND, FORCEOFF = V_{CC}		$V_{CC}-0.6$		V
V_{OL}	$\overline{\text{INVALID}}$ low-level output voltage	$I_{OL} = 1.6$ mA, FORCEON = GND, FORCEOFF = V_{CC}			0.4	V

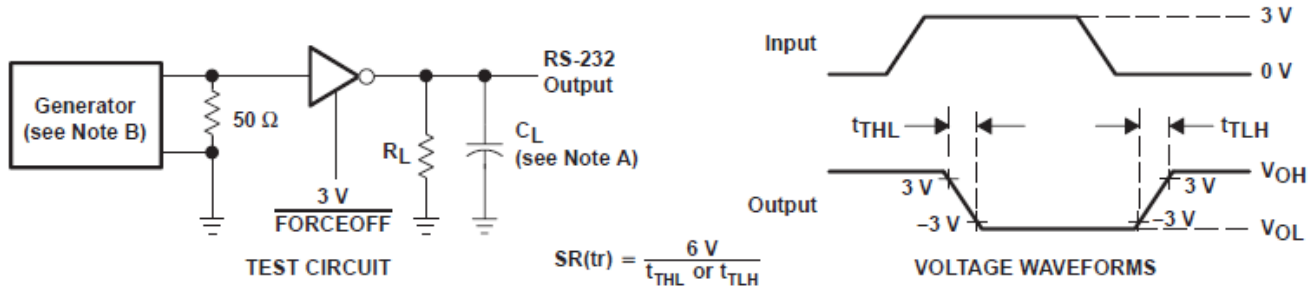
6.10 Switching Characteristics - Auto-Powerdown

over operating free-air temperature range (unless otherwise noted) (see [7-5](#))

PARAMETER		MIN	TYP ⁽¹⁾	MAX	UNIT
t_{valid}	Propagation delay time, low- to high-level output		1		μs
t_{invalid}	Propagation delay time, high- to low-level output		30		μs
t_{en}	Supply enable time		100		μs

(1) All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25^\circ\text{C}$.

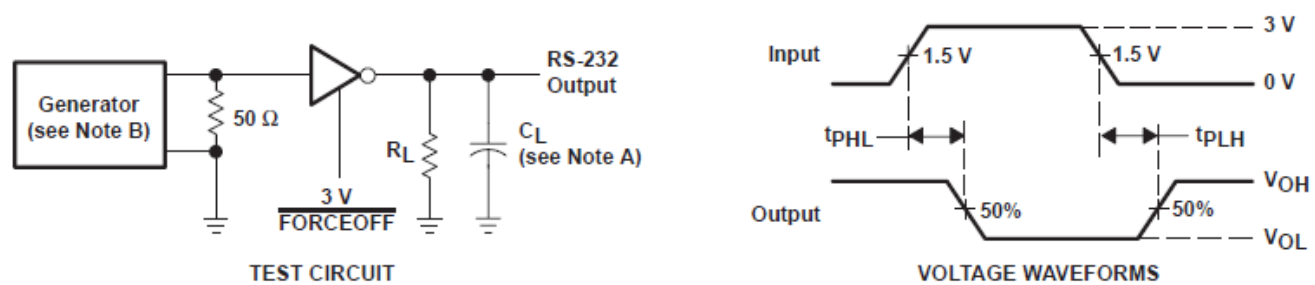
7 Parameter Measurement Information



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

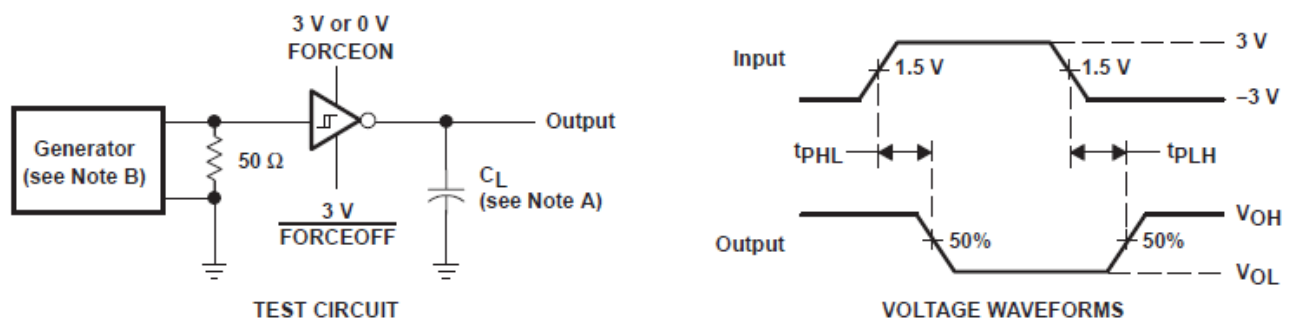
图 7-1. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

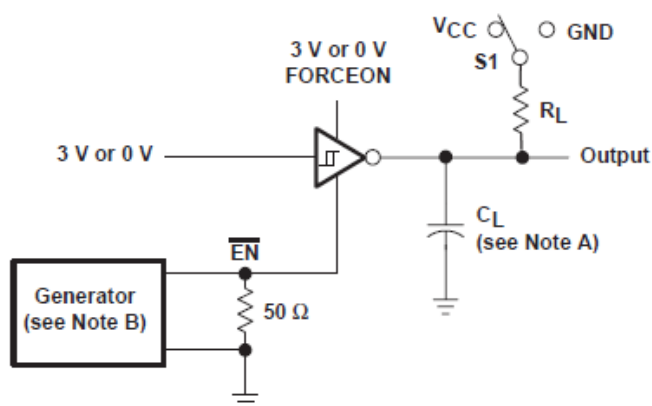
图 7-2. Driver Pulse Skew



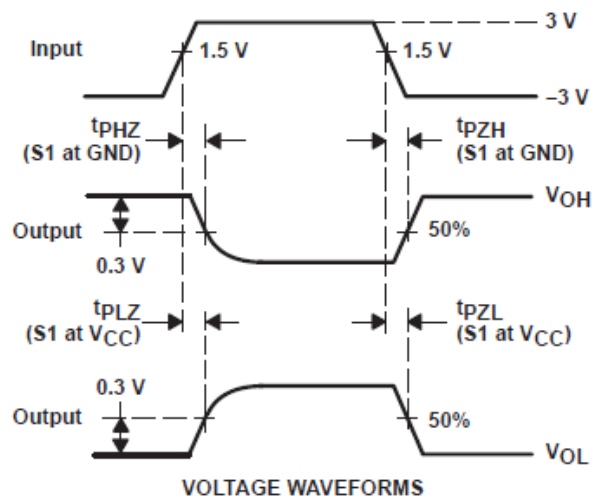
NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

图 7-3. Receiver Propagation Delay Times

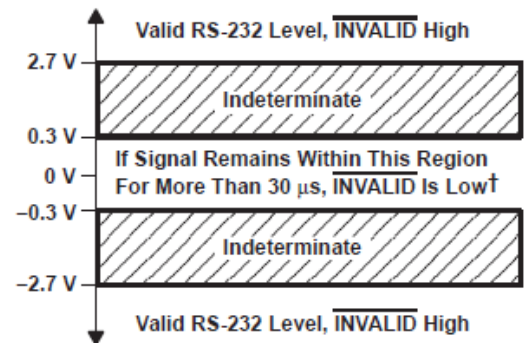
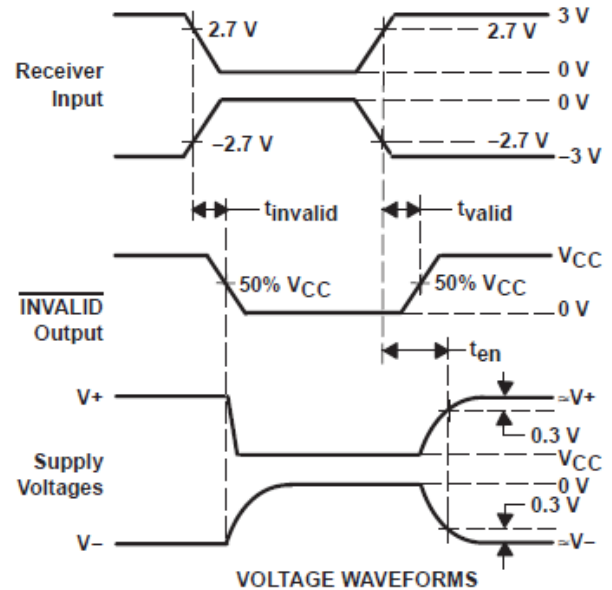
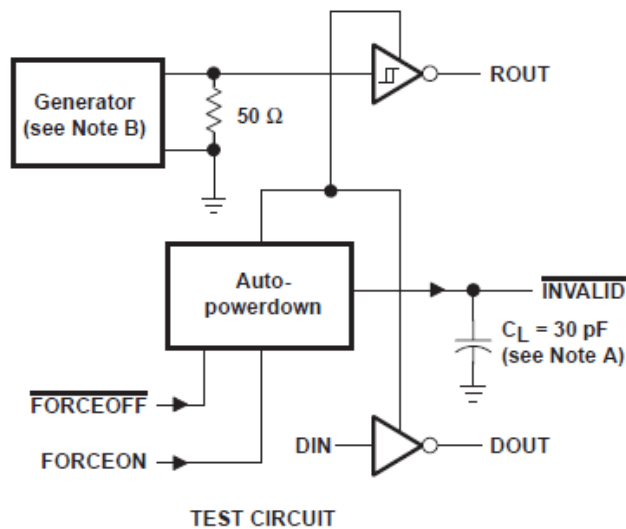


TEST CIRCUIT



- NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
D. t_{PZL} and t_{PZH} are the same as t_{en} .

图 7-4. Receiver Enable and Disable Times



† Auto-powerdown disables drivers and reduces supply current to 1 μA .

NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 5 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

图 7-5. $\overline{\text{INVALID}}$ Propagation Delay Times and Driver Enabling Time

8 Detailed Description

8.1 Device Functional Modes

表 8-1. Each Driver⁽¹⁾

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto- powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	
H	L	H	Yes	L	Normal operation with auto- powerdown enabled
L	L	H	No	Z	
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

表 8-2. Each Receiver⁽¹⁾

INPUTS			OUTPUT ROUT
RIN	EN	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

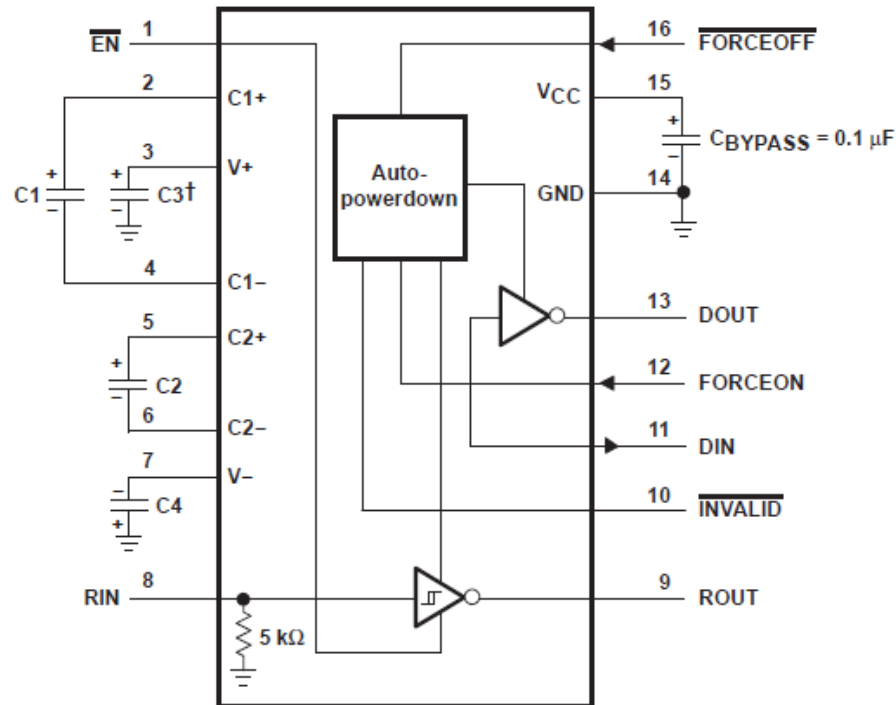
(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = disconnected input or connected driver off.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information



† C3 can be connected to V_{CC} or GND

Resistor values shown are nominal.

图 9-1. Typical Operating Circuit and Capacitor Values

表 9-1. V_{CC} vs Capacitor Values

V_{CC}	C1	C2, C3, and C4
3.3 V $\pm$ 0.3 V	0.1 μ F	0.1 μ F
5 V $\pm$ 0.5 V	0.047 μ F	0.33 μ F
3 V to 5.5 V	0.1 μ F	0.47 μ F

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65C3221DB	Obsolete	Production	SSOP (DB) 16	-	-	Call TI	Call TI	-40 to 85	CB3221
SN65C3221DBR	Obsolete	Production	SSOP (DB) 16	-	-	Call TI	Call TI	-40 to 85	CB3221
SN65C3221PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	CB3221
SN65C3221PWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3221
SN65C3221PWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3221
SN75C3221DBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA3221
SN75C3221DBR.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA3221
SN75C3221DW	Preview	Production	SOIC (DW) 16	40 TUBE	-	Call TI	Call TI	0 to 70	
SN75C3221PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA3221
SN75C3221PWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA3221

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

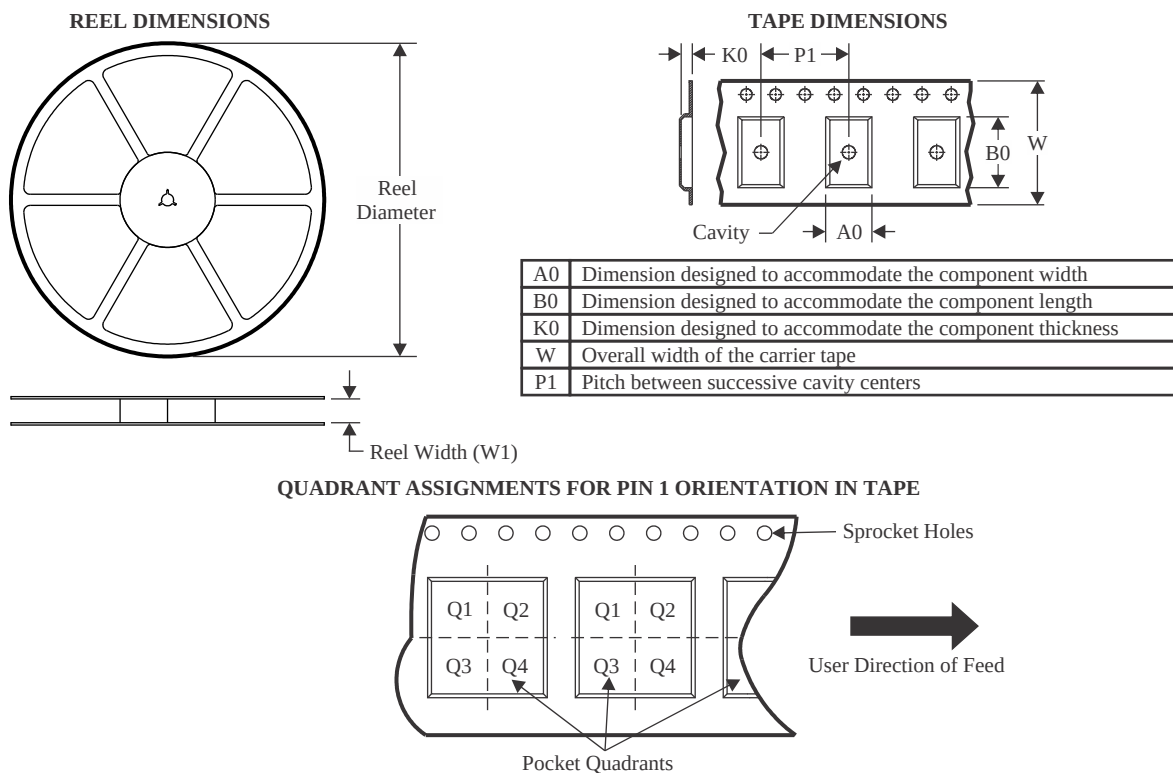
OTHER QUALIFIED VERSIONS OF SN65C3221 :

- Automotive : [SN65C3221-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

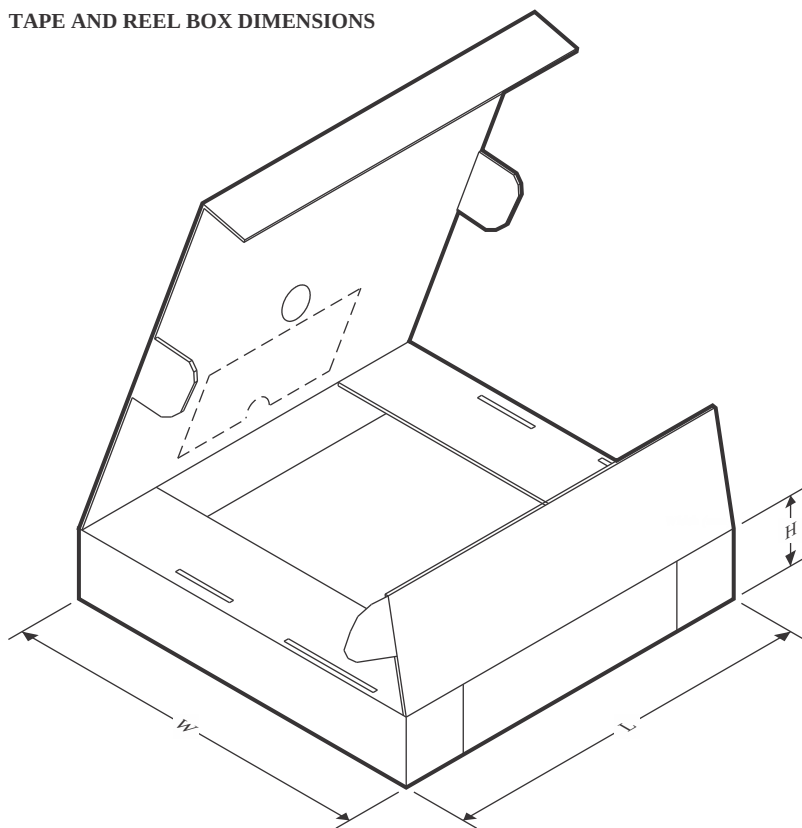
TAPE AND REEL INFORMATION



*All dimensions are nominal

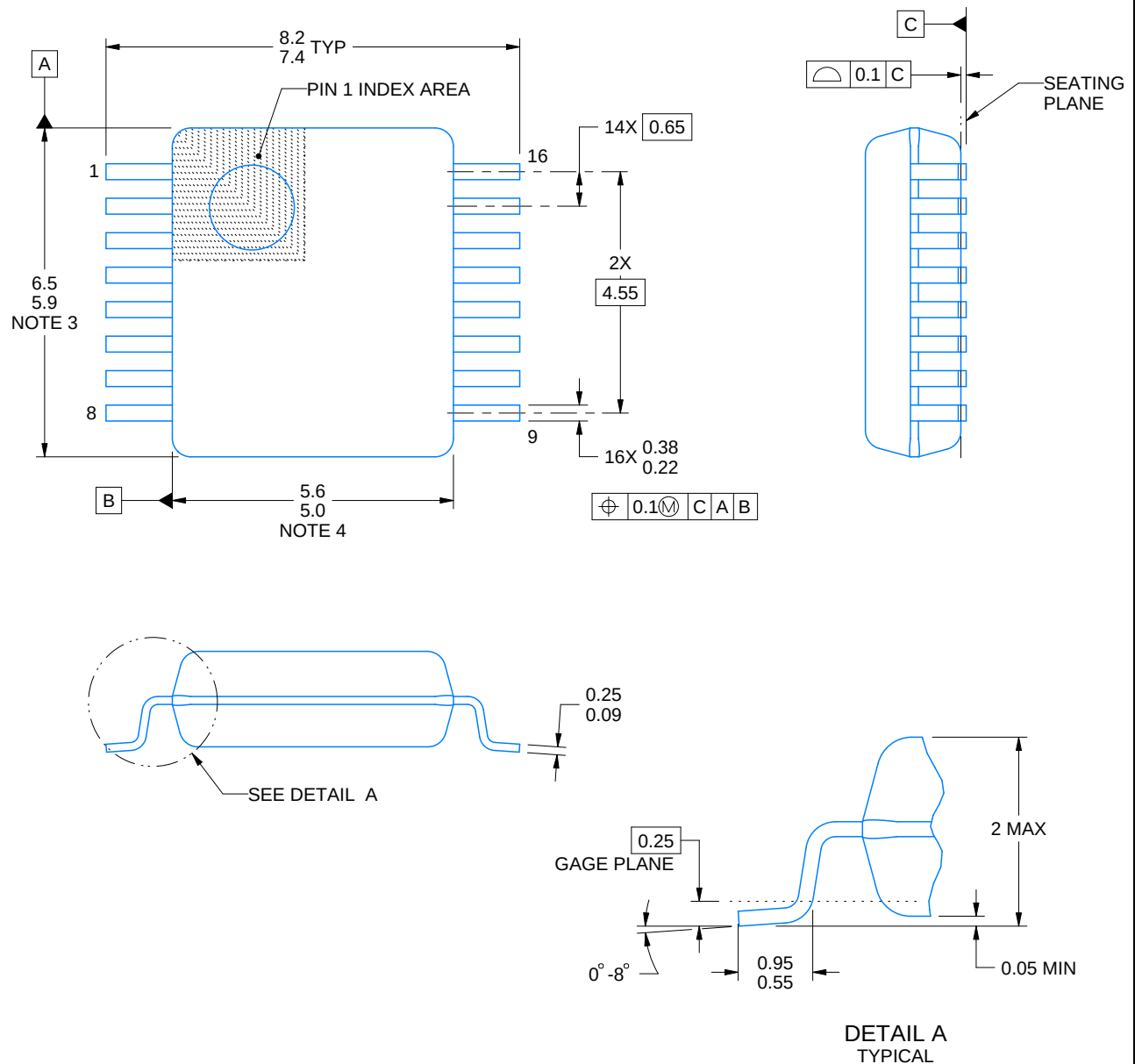
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C3221PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65C3221PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65C3221PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65C3221PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN75C3221DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN75C3221PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C3221PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN65C3221PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN65C3221PWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0
SN65C3221PWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0
SN75C3221DBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN75C3221PWR	TSSOP	PW	16	2000	353.0	353.0	32.0



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NOTES:

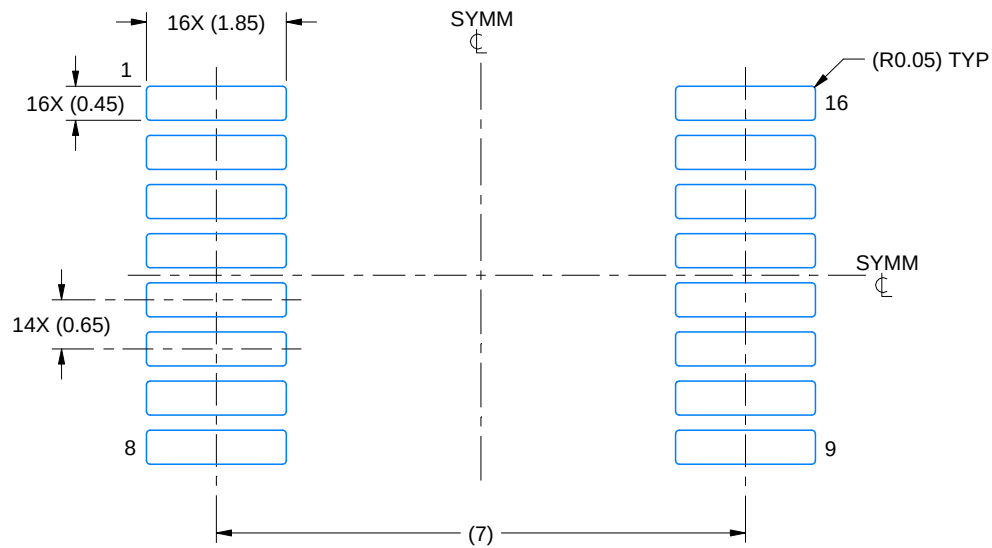
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

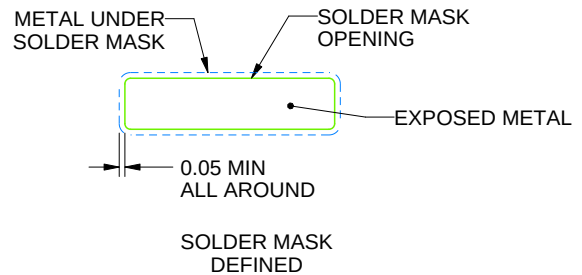
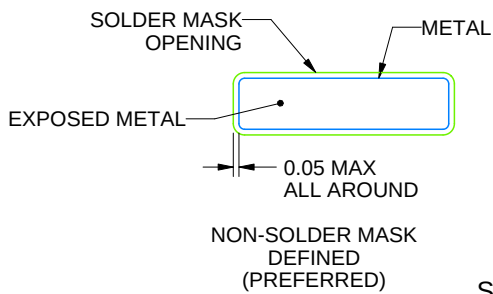
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

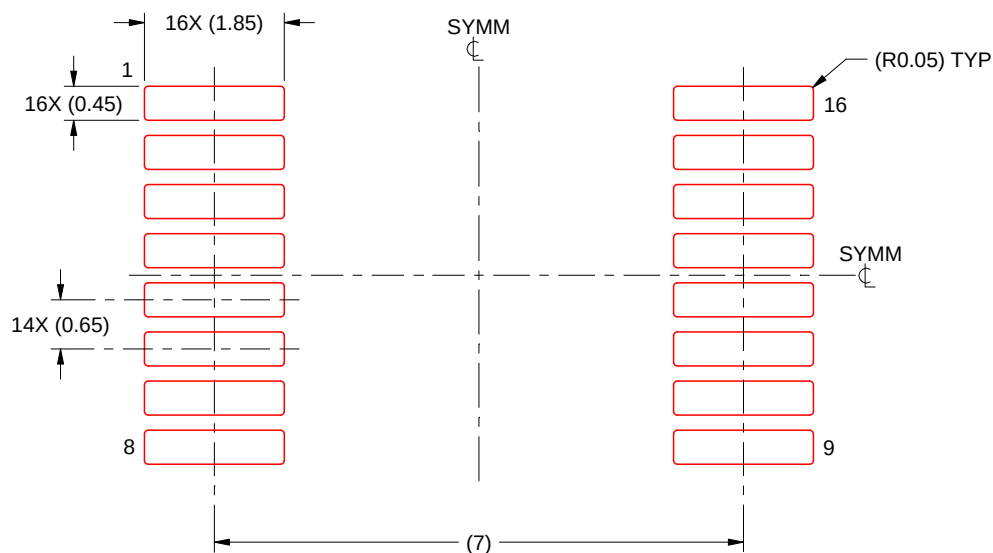
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

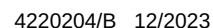
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



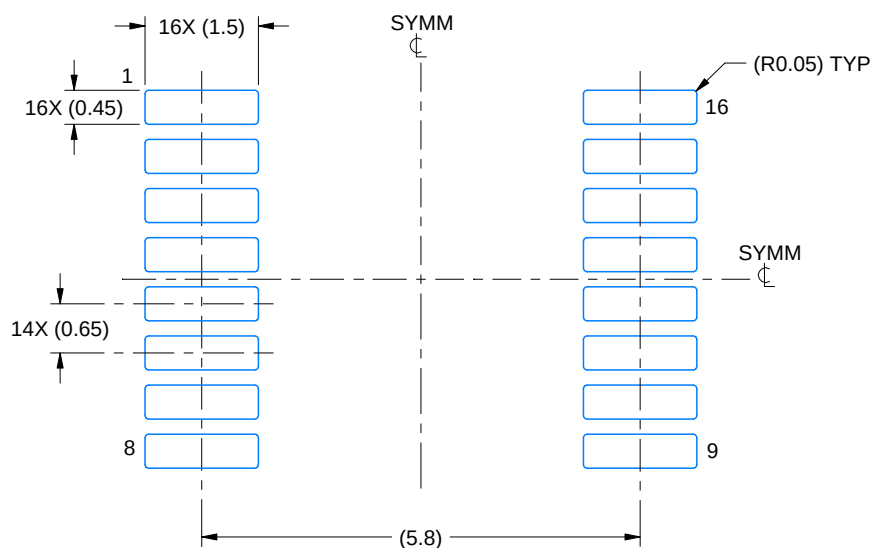
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

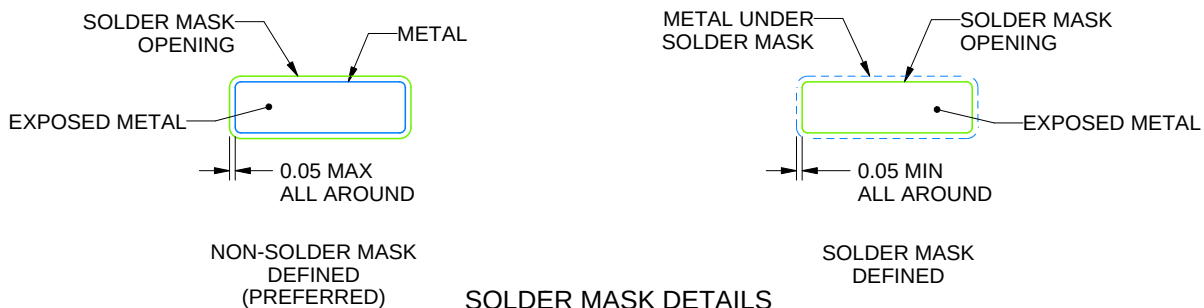
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

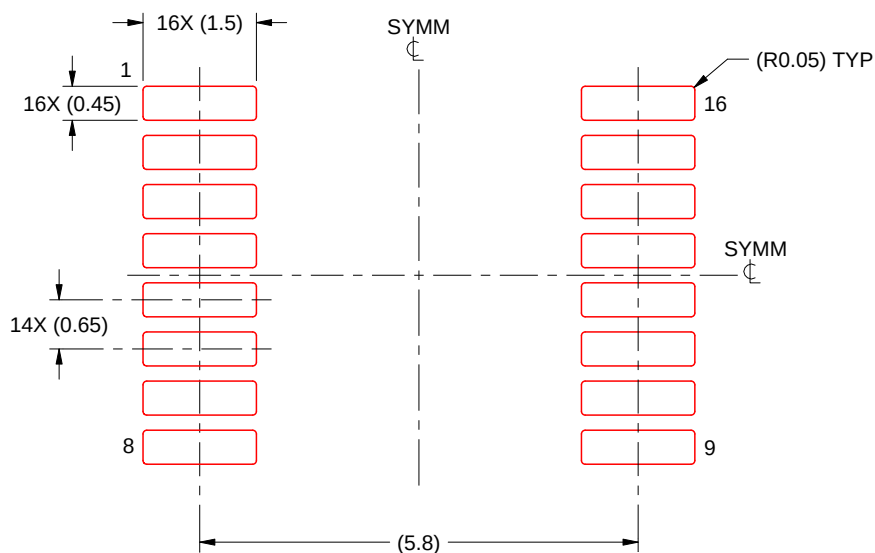
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月