# SN65HVS883 24V、8チャネル・デジタル入力シリアライザ

## 1 特長

- 8つのセンサ入力
  - 最大34Vの高い入力電圧
  - 0ms～3msのデバウンス・フィルタを選択可能
  - 0.2mA～5.2mAまで可変の電流制限
  - フィールド入力および電源ラインに対する15kV HBMまでの保護
- 外部のステータスLED用の出力ドライバ
- カスケード接続により、入力を8個単位で増やすことが可能
- SPI互換のインターフェイス
- 外部デジタル・アイソレータへの、レギュレートされた5V出力
- 低電源電圧インジケータ

## 2 アプリケーション

- 産業自動化およびプロセス制御用のセンサ入力
  - IEC61131-2タイプ1、2、3スイッチ
  - EN60947-5-2近接スイッチ
- PCおよびPLCシステム用の、チャネル数の多いデジタル入力モジュール
- 非集中化I/Oモジュール

## 3 概要

SN65HVS883は24V、8チャネルのデジタル入力シリアライザで、産業自動化において、PCおよびPLCベースのシステム用の、チャネル密度の高いデジタル入力モジュールとして使用されます。ガルバニー絶縁体と組み合わせることで、デバイスはフィールド側の24Vセンサ出力と、制御側の低電圧コントローラ入力との間で、完全なインターフェイスになります。

EN60947-5-2準拠の2線および3線の近接スイッチから供給される入力信号は、電流制限されてから、内部のデバウンス・フィルタにより検証されます。入力のスイッチング特性は、IEC61131-2のタイプ1、2、3センサ・スイッチに準拠しています。

負荷およびクロック信号を印加すると、入力データが並列にラッチされてシフト・レジスタに送られ、後段のアイソレータによりクロックに合わせて直列に、シリアルPLC入力へ送られます。

前段のデバイスのシリアル出力を後段のデバイスのシリアル入力へ接続することによって、複数のSN65HVS883をカスケード接続すると、チャネル数の多い入力モジュールの設計が可能になります。入力の状態は、3mAの定電流LED出力により示されます。内部の基準電流を設定するため、高精度の外付け抵抗が必要です。内蔵の電圧レギュレータにより、低消費電力アイソレータへ5Vの電源が供給されます。内部の電源電圧モニタにより、チップOK (CHOK)信号が出力されます。

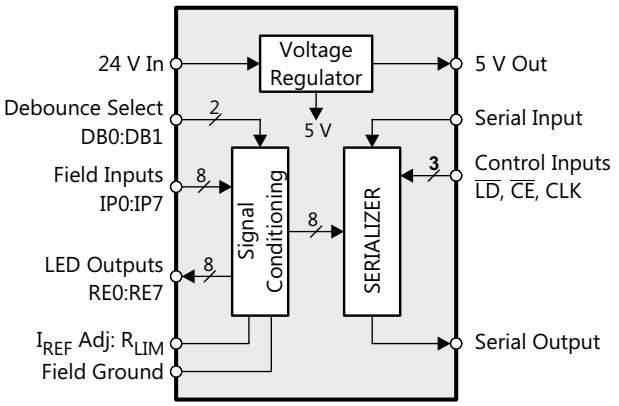
SN65HVS883は28ピンのPWP PowerPAD™パッケージで供給され、効率的な放熱が可能です。このデバイスは、-40℃～85℃の温度範囲で動作が規定されています。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ(公称) |
|---|---|---|
| SN65HVS883 | HTSSOP (28) | 9.70mm×4.40mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

**I/O構造の簡略図**

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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| 日付 | 改訂内容 | 注 |
|---|---|---|
| 2016年9月 | * | 初版 |


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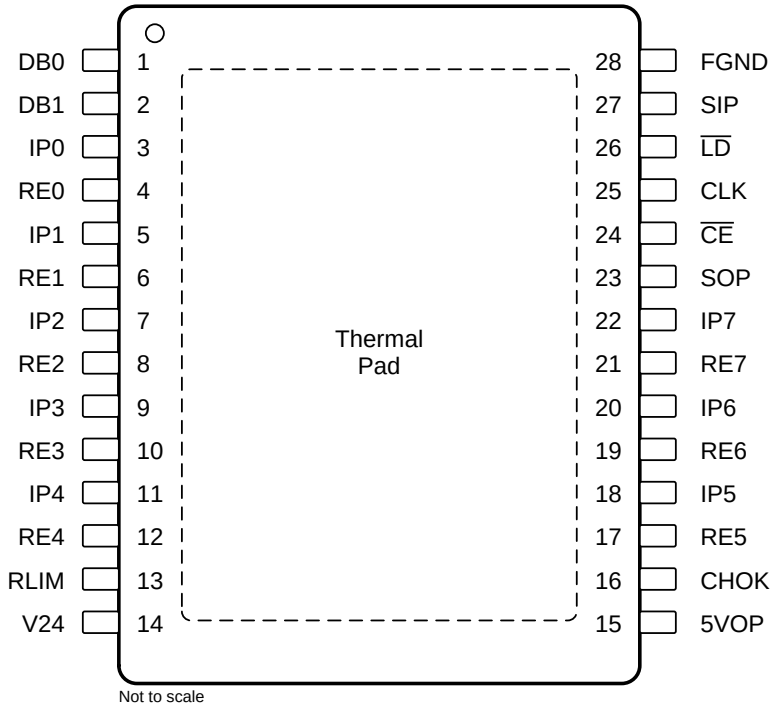
# 5 Pin Configuration and Functions

**PWP Package**
**28 Pin (HTSSOP) With Exposed Thermal Pad**
**Top View**




**Pin Functions**

| PIN | | DESCRIPTION |
|---|---|---|
| PIN NO. | NAME | |
| 1, 2 | DB0, DB1 | Debounce select inputs |
| 3, 5, 7, 9, 11, 18, 20, 22 | IPx | Input channel x |
| 4, 6, 8, 10, 12, 17, 19, 21 | REx | Return path x (LED drive) |
| 13 | RLIM | Current limiting resistor |
| 14 | V24 | 24 VDC field supply |
| 15 | 5VOP | 5 V output to supply low-power isolators |
| 16 | CHOK | Chip okay indicator output |
| 23 | SOP | Serial data output |
| 24 | $\overline{CE}$ | Clock enable input |
| 25 | CLK | Serial clock input |
| 26 | $\overline{LD}$ | Load pulse input |
| 27 | SIP | Serial data input |
| 28 | FGND | Field ground |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| V24 | Field power input | V24 | –0.3 | 36 | V |
| $V_{IPx}$ | Field digital inputs | IPx | –0.3 | 36 | V |
| $V_{ID}$ | Voltage at any logic input | DB0, DB1, CLK, SIP, $\overline{CE}$, $\overline{LD}$ | –0.5 | 6 | V |
| $I_O$ | Output current | CHOK, SOP | | ±8 | mA |
| $P_{TOT}$ | Continuous total power dissipation | | See *Thermal Information* table | | |
| $T_J$ | Junction temperature | | | 170 | °C |

## 6.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | All pins | ±4000 | V |
| | | | IPx,V24 | ±15000 | |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 (2) | All pins | ±1000 | |
| | | Machine Mode (3) | All pins | ±100 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) JEDEC Standard 22, Method A115-A.

## 6.3 Recommended Operating Conditions

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{24}$ | Field supply voltage | 10 | 24 | 34 | V |
| $V_{IPL}$ | Field input low-state input voltage (1) | 0 | | 4 | V |
| $V_{IPH}$ | Field input high-state input voltage (1) | 10 | | 34 | V |
| $V_{IL}$ | Logic low-state input voltage | 0 | | 0.8 | V |
| $V_{IH}$ | Logic high-state input voltage | 2 | | 5.5 | V |
| $R_{LIM}$ | Current limiter resistor | 17 | 25 | 500 | kΩ |
| $f_{IP}$ | Input data rate (2) | 0 | | 1 | Mbps |
| $T_J$ | | | | 150 | °C |
| $T_A$ | | –40 | | 85 | °C |

(1) Field input voltages correspond to an input resistor of $R_{IN}$ = 1.2 kΩ
(2) Maximum data rate corresponds to 0 ms debounce time, (DB0 = open, DB1 = FGND), and $R_{IN}$ = 0 Ω

## 6.4 Thermal Information

| THERMAL METRIC (1) | | | SN65HVS883 PWP (HTSSOP) 28 PINS | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | | 35 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | | 4.27 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | | 15 | °C/W |
| PD | Device power dissipation | $I_{LOAD}$ = 50 mA, $R_{IN}$ = 0, IPO–IP7 = V24 = 30 V, RE7 = FGND, $f_{CLK}$ = 100 MHz, $I_{IP-LIM}$ and $I_{CC}$ = worst case with $R_{LIM}$ = 25 kΩ | 2591 | mW |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.


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## 6.5 Electrical Characteristics

all voltages measured against FGND unless otherwise stated, see Figure 12

| SYMBOL | PARAMETER | PIN | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{TH-(IP)}$ | Low-level device input threshold voltage | IP0–IP7 | 18 V< V24 < 34 V, $R_{IN}$ = 0 Ω , $R_{LIM}$ = 25 kΩ | 4 | 4.3 | | V |
| $V_{TH+(IP)}$ | High-level device input threshold voltage | | | | 5.2 | 5.5 | V |
| $V_{HYS(IP)}$ | Device input hysteresis | | | | 0.9 | | V |
| $V_{TH-(IN)}$ | Low-level field input threshold voltage | measured at field side of $R_{IN}$ | 18 V < V24 < 34 V, $R_{IN}$ = 1.2 kΩ ± 5%, $R_{LIM}$ = 25 kΩ | 6 | 8.4 | | V |
| $V_{TH+(IN)}$ | High-level field input threshold voltage | | | | 9.4 | 10 | V |
| $V_{HYS(IN)}$ | Field input hysteresis | | | | 1 | | V |
| $V_{TH-(V24)}$ | Low-level V24-monitor threshold voltage | V24 | | 15 | 16.05 | | V |
| $V_{TH+(V24)}$ | High-level V24-monitor threshold voltage | | | | 16.8 | 18 | V |
| $V_{HYS(V24)}$ | V24-monitor hysteresis | | | | 0.75 | | V |
| $R_{IP}$ | Input resistance | IP0–IP7 | 3 V < $V_{IPx}$ < 6 V, $R_{IN}$ = 1.2 kΩ ± 5%, $R_{LIM}$ = 25 kΩ | 1.4 | 1.83 | 2.3 | kΩ |
| $I_{IP-LIM}$ | Input current limit | | 10 V < $V_{IPx}$ < 34 V, $R_{LIM}$ = 25 kΩ | 3.15 | 3.6 | 4 | mA |
| $V_{OL}$ | Logic low-level output voltage | SOP, CHOK | $I_{OL}$ = 20 μA | | | 0.4 | V |
| $V_{OH}$ | Logic high-level output voltage | | $I_{OH}$ = –20 μA | 4 | | | V |
| $I_{IL}$ | Logic input leakage current | $\overline{DB0}$, $\overline{DB1}$, SIP, $\overline{LD}$, $\overline{CE}$, CLK | | –50 | | 50 | μA |
| $I_{RE-on}$ | RE on-state current | RE0–RE7 | $R_{LIM}$ = 25 kΩ, $RE_X$ = FGND | 2.8 | 3.15 | 3.5 | mA |
| $I_{CC(V24)}$ | Supply current | V24 | IP0 to IP7 = V24, 5VOP = open, $RE_X$ = FGND, All logic inputs open | | | 8.7 | mA |
| $V_{O(5V)}$ | Linear regulator output voltage | 5VOP | 18 V < V24 < 34 V, no load | 4.5 | 5 | 5.5 | V |
| | | | 18 V < V24 < 34 V, $I_L$ = 50 mA | 4.5 | 5 | 5.5 | |
| $I_{LIM(5V)}$ | Linear regulator output current limit | | | | 115 | | mA |
| $\Delta V_5/\Delta V_{24}$ | Line regulation | 5VOP, V24 | 18 V < V24 < 34 V, $I_L$ = 5 mA | | | 2 | mV/V |
| $t_{DB}$ | Debounce times of input channels | IP0–IP7 | DB0 = open, DB1 = FGND | | 0 | | ms |
| | | | DB0 = FGND, DB1 = open | | 1 | | |
| | | | DB0 = DB1 = open | | 3 | | |
| $t_{DB-HL}$ | Voltage monitor debounce time after V24 < 15 V (CHOK turns low) | V24, CHOK | | | 1 | | ms |
| $t_{DB-LH}$ | Voltage monitor debounce time after V24 > 18 V (CHOK turns high) | | | | 6 | | ms |
| $T_{SHDN}$ | Shutdown temperature | | | | 170 | | °C |

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## 6.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

| SYMBOL | PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{W1}$ | CLK pulse width | See Figure 9 | 4 | | | ns |
| $t_{W2}$ | $\overline{LD}$ pulse width | See Figure 7 | 6 | | | ns |
| $t_{SU1}$ | SIP to CLK setup time | See Figure 10 | 4 | | | ns |
| $t_{H1}$ | SIP to CLK hold time | See Figure 10 | 2 | | | ns |
| $t_{SU2}$ | Falling edge to rising edge ($\overline{CE}$ to CLK) setup time | See Figure 11 | 4 | | | ns |
| $t_{REC}$ | $\overline{LD}$ to CLK recovery time | See Figure 8 | 2 | | | ns |
| $f_{CLK}$ | Clock pulse frequency (50% duty cycle) | See Figure 9 | DC | | 100 | MHz |

## 6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH1}$, $t_{PHL1}$ | CLK to SOP | $C_L$ = 15 pF, see Figure 9 | | | 10 | ns |
| $t_{PLH2}$, $t_{PHL2}$ | $\overline{LD}$ to SOP | $C_L$ = 15 pF, see Figure 7 | | | 14 | ns |
| $t_r$, $t_f$ | Rise and fall times | $C_L$ = 15 pF, see Figure 9 | | | 5 | ns |


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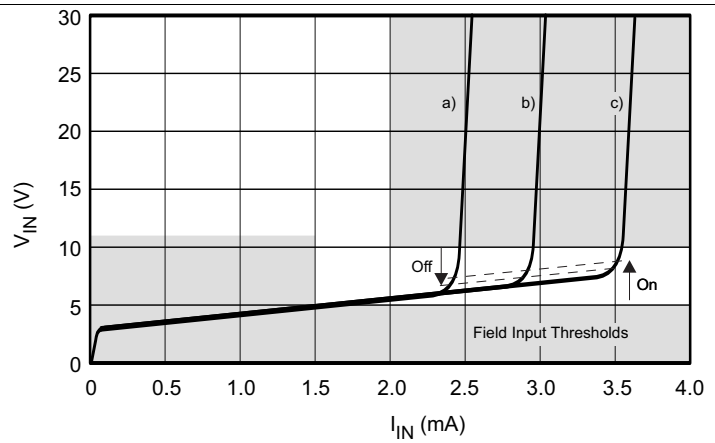
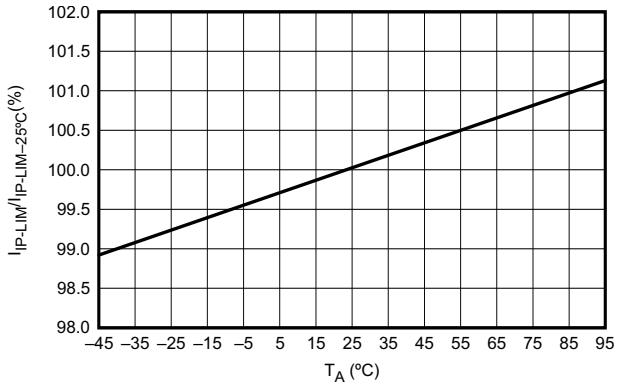
## 6.8 Typical Input Characteristics




$R_{IN}$ = 1.2 kΩ

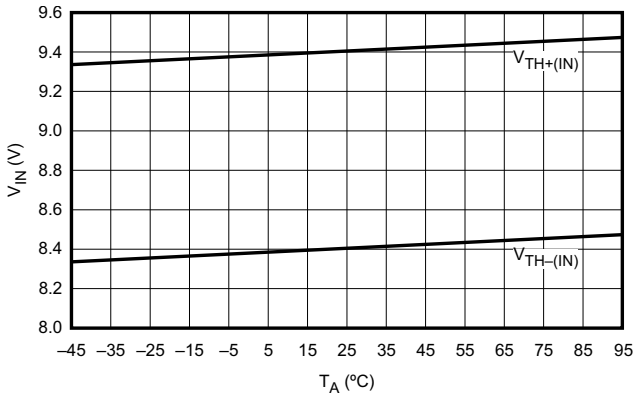
a) $I_{IP\text{-}LIM}$ = 2.5 mA ($R_{LIM}$ = 36.1 kΩ)
b) $I_{IP\text{-}LIM}$ = 3.0 mA ($R_{LIM}$ = 30.1 kΩ)
c) $I_{IP\text{-}LIM}$ = 3.6 mA ($R_{LIM}$ = 24.9 kΩ)

**Figure 1. Typical Input Characteristics**




V24 = 24 V $V_{IN}$ = 24 V $R_{IN}$ = 1.2 kΩ
$R_{LIM}$ = 24.9 kΩ

**Figure 2. Typical Current Limiter Variation vs Ambient Temperature**




V24 = 24 V $R_{IN}$ = 1.2 kΩ $R_{LIM}$ = 24.9 kΩ

**Figure 3. Typical Limiter Threshold Voltage Variation vs Ambient Temperature**

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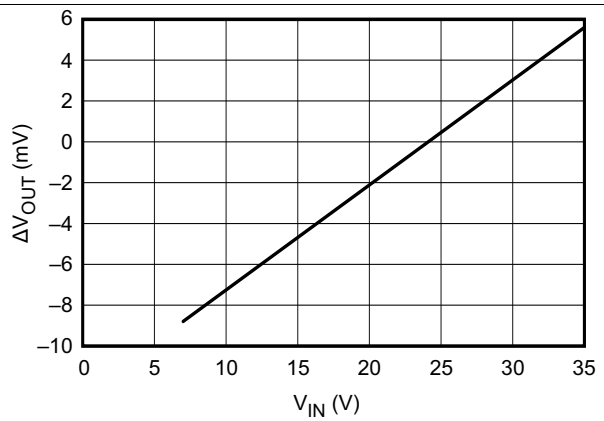
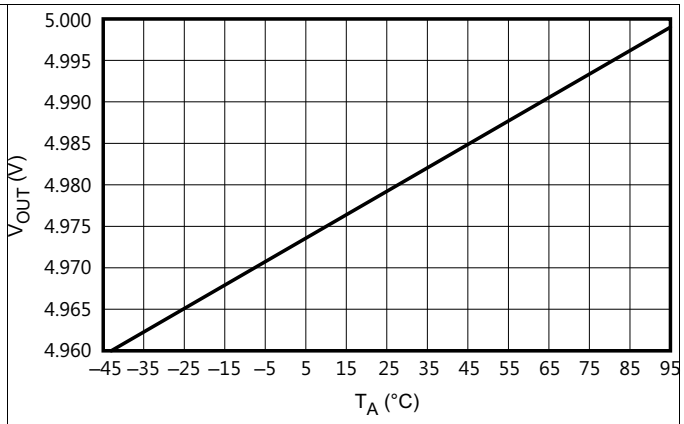
## 6.9 Typical Voltage Regulator Performance Characteristics



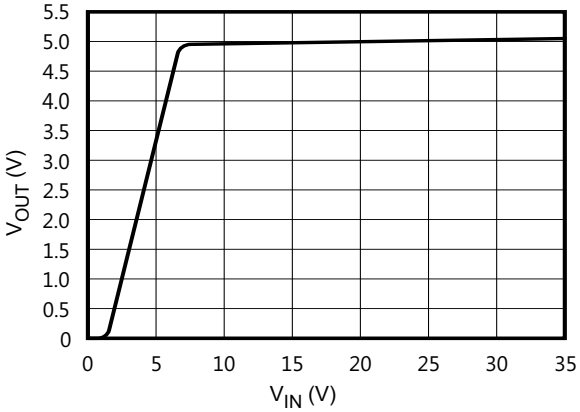

$I_{LOAD}$ = 5 mA $T_A$ = 27°C

**Figure 4. Line Regulation**




$I_{LOAD}$ = 0 mA

**Figure 5. Output Voltage vs Ambient Temperature**




$R_{LOAD}$ = 100 Ω

**Figure 6. Output Voltage vs Input Voltage**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# 7 Parameter Measurement Information

## 7.1 Waveforms

For the complete serial interface timing, refer to Figure 21.

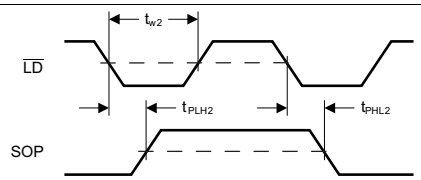


**Figure 7. Parallel – Load Mode**

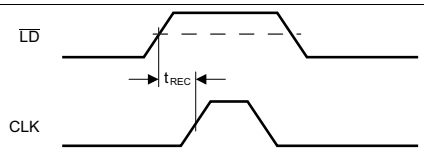


**Figure 8. Serial – Shift Mode**

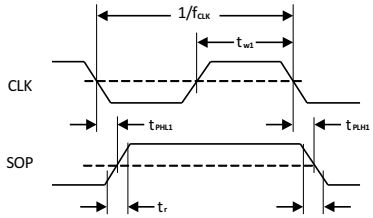


**Figure 9. Serial – Shift Mode**

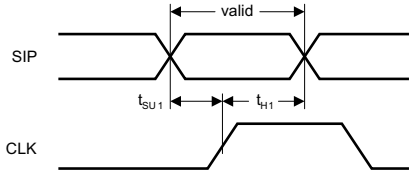


**Figure 10. Serial – Shift Mode**

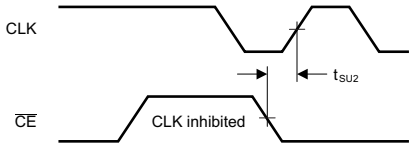


**Figure 11. Serial – Shift Clock Inhibit Mode**

## 7.2 Signal Conventions

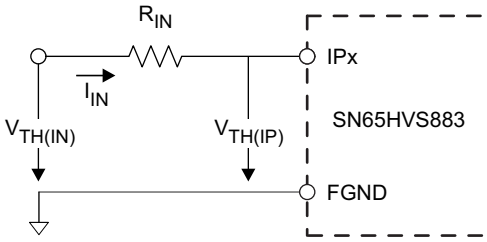


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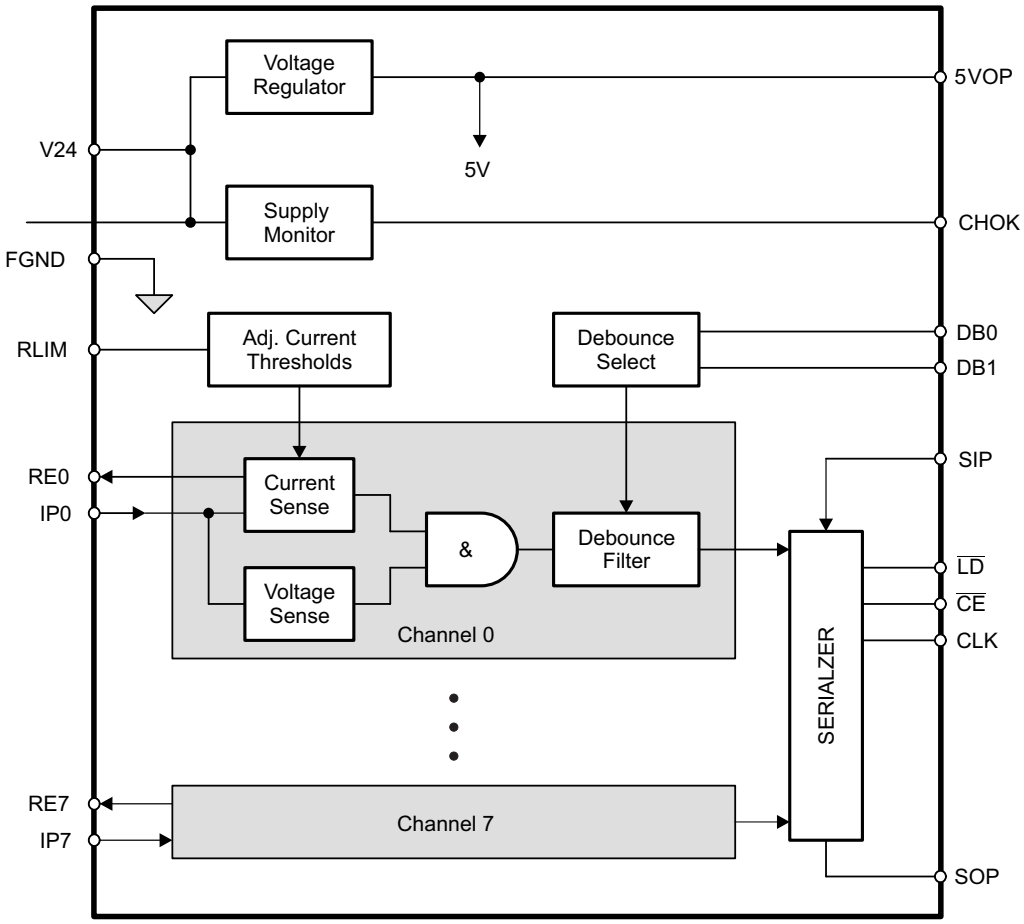
**Figure 12. On/Off Threshold Voltage Measurements**

# 8 Detailed Description

## 8.1 Overview

The SN65HVS883 is an 8 channel, digital input serializer which operates from a 24 V supply and accepts digital inputs of up to 34 V on the 8 channels (IP0-IP7). The device provides a serially shifted digital output with reduced voltage ranges of 0-5 V for applications in industrial and building automation systems. The SN65HVS883 meets JEDEC standards for ESD protection (refer to *ESD Ratings*), and is SPI compatible for interfacing with standard microcontrollers. The serializer operates in 2 fundamental modes: Load Mode and Shift mode. In Load mode, information from the field inputs is allowed to latch into the shift register. In Shift mode, the information stored in the parallel shift register can be serially shifted to the serial output (SOP). A detailed description of the functional modes is available in the *Device Functional Modes* section.

## 8.2 Functional Block Diagram

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## 8.3 Feature Description

### 8.3.1 Digital Inputs

Each digital input operates as a controlled current sink limiting the input current to a maximum value of $I_{LIM}$. The current limit is derived from the reference current via $I_{LIM} = n \times I_{REF}$, and $I_{REF}$ is determined by $I_{REF} = V_{REF}/R_{LIM}$. Thus, changing the current limit requires the change of $R_{LIM}$ to a different value via: $R_{LIM} = n \times V_{REF}/I_{LIM}$.

Inserting the actual values for n and $V_{REF}$ gives: $R_{LIM} = 90\ V / I_{LIM}$.

While the device is specified for a current limit of **3.6 mA**, (via $R_{LIM} = 25\ k\Omega$), it is easy to lower the current limit to further reduce the power consumption. For example, for a current limit of **2.5 mA** simply calculate:

$$R_{LIM} = \frac{90\ V}{I_{LIM}} = \frac{90\ V}{2.5\ mA} = 36\ k\Omega \tag{1}$$

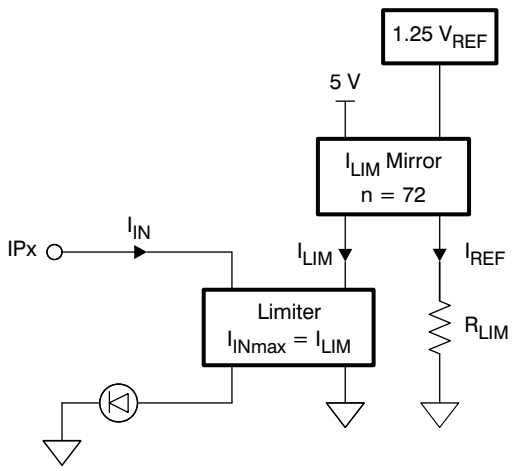


**Figure 13. Digital Input Stage**

### 8.3.2 Debounce Filter

The HVS883 applies a simple analog/digital filtering technique to remove unintended signal transitions due to contact bounce or other mechanical effects. Any new input (either low or high) must be present for the duration of the selected debounce time to be latched into the shift register as a valid state.

The logic signal levels at the control inputs, DB0 and DB1 of the internal Debounce-Select logic determine the different debounce times listed in the following truth table.

**Table 1. Debounce Times**

| DB1 | DB0 | FUNCTION |
|---|---|---|
| Open | Open | 3 ms delay |
| Open | FGND | 1 ms delay |
| FGND | Open | 0 ms delay (Filter bypassed) |
| FGND | FGND | Reserved |

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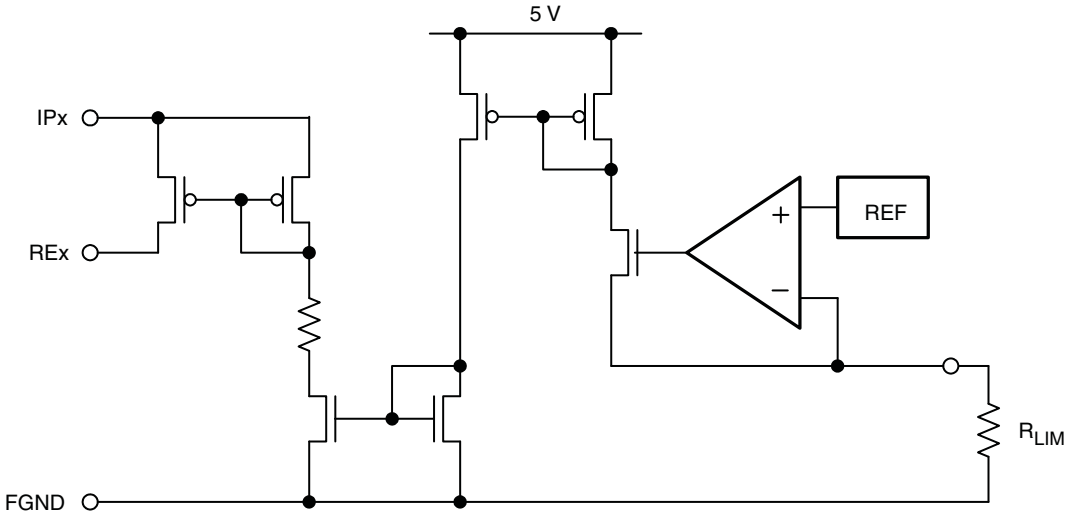


**Figure 14. Equivalent Input Diagram**

### 8.3.3 Shift Register

The conversion from parallel input to serial output data is performed by an eight-channel, parallel-in serial-out shift register. Parallel-in access is provided by the internal inputs, PIP0–PIP7, that are enabled by a low level at the load input ($\overline{LD}$). When clocked, the latched input data shift towards the serial output (SOP). The shift register also provides a clock-enable function.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while $\overline{LD}$ is held high and the clock enable ($\overline{CE}$) input is held low for all registers in the shift register except the last register which is latched by a high-to-low transition. Parallel loading is inhibited when LD is held high. The parallel inputs to the register are enabled while $\overline{LD}$ is low independently of the levels of the CLK, $\overline{CE}$, or serial (SIP) inputs.

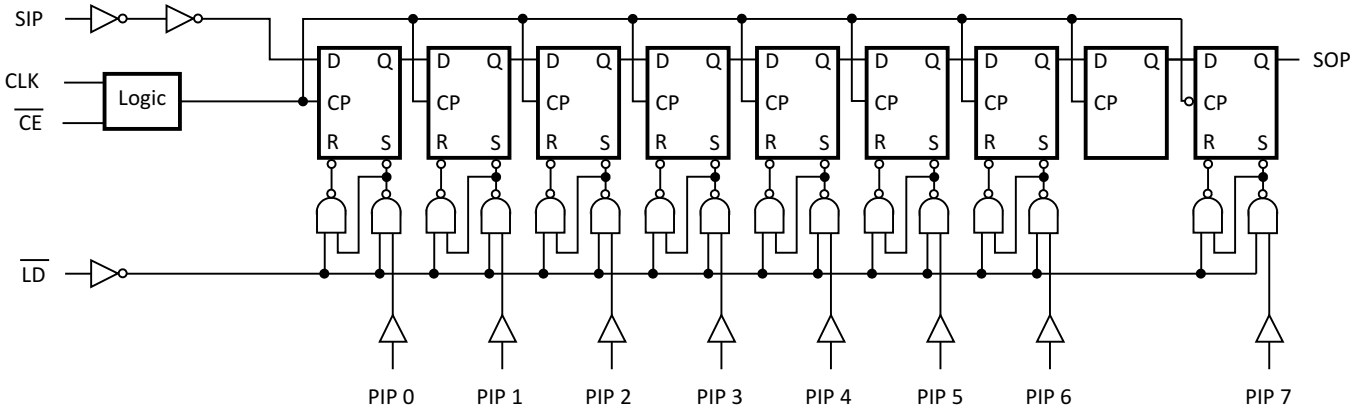


**Figure 15. Shift Register Logic Structure**


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**Table 2. Function Table**

| INPUTS | | | FUNCTION |
|---|---|---|---|
| $\overline{LD}$ | CLK | $\overline{CE}$ | |
| L | X | X | Parallel load |
| H | X | H | No change |
| H | ↑ | L | Shift(1) |
| H | ↓ | L | Shift(2) |

(1) Shift = content of each internal register, except the last register, shifts towards serial output.
(2) Shift = content of the last register shifts towards serial output.

### 8.3.4 Voltage Regulator

The on-chip linear voltage regulator provides a 5 V supply to the internal- and external circuitry, such as digital isolators, with an output drive capability of 50 mA and a typical current limit of 115 mA. The regulator accepts input voltages from 34 V down to 10 V. Because the regulator output is intended to supply external digital isolator circuits proper output voltage decoupling is required. For best results connect a 1 μF and a 0.1 μF ceramic capacitor as close as possible to the 5VOP-output. For longer traces between the SN65HVS883 and isolators of the ISO72xx family use additional 0.1 μF and 10 pF capacitors next to the isolator supply pins. Make sure, however, that the total load capacitance does not exceed 4.7 μF.

For good stability the voltage regulator requires a minimum load current, $I_{L\text{-}MIN}$. Ensure that under any operating condition the ratio of the minimum load current in mA to the total load capacitance in μF is larger than 1:

$$\frac{I_{L\text{-}MIN}}{C_L} > \frac{1\ \text{mA}}{1\ \mu\text{F}} \tag{2}$$

### 8.3.5 Supply Voltage Monitor

The integrated supply voltage monitor senses the supply voltage of the SN65HVS883 at the V24-pin. If this voltage drops below 15 V but stays within the regulator's operating range, i.e., 15 V > V24 > 10 V, the output CHOK goes low 1 ms later. When the supply voltage returns to 24 V, the CHOK output turns logic high after 6 ms. Should the supply voltage drop below 10 V, the device ceases operation. Upon the supply returning to above 18 V, the CHOK output turns high again after 6 ms.

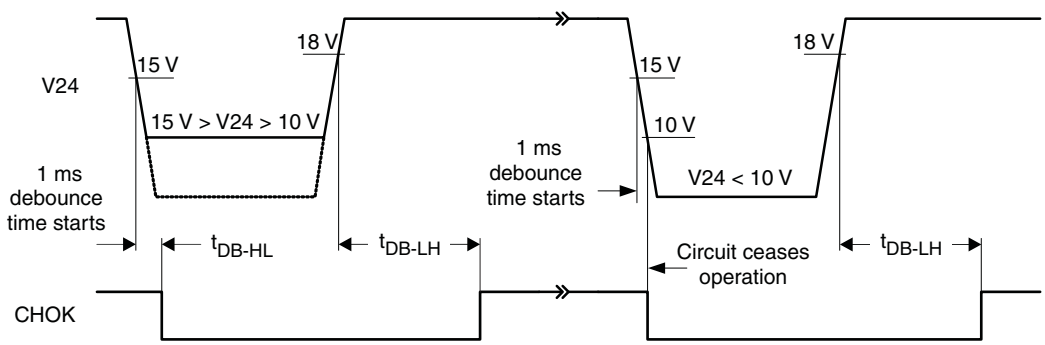


**Figure 16. CHOK Output Timing as a Function of Supply Voltage Drop at V24**

## 8.4 Device Functional Modes

The 2 functional modes of operation are Load mode and Shift mode.

Load mode enables information from the field inputs to latch into the shift register. To enter load mode, the $\overline{LD}$ pin must be held low, and the device remains in load mode regardless of the CLK, $\overline{CE}$, or serial (SIP) input levels. A high level at the $\overline{LD}$ pin switches the device into Shift mode.

When the device is in Shift mode, a low level at the $\overline{CE}$ pin causes the data stored in all registers of the parallel shift register except for the last register, to be serially shifted toward the serial output (SOP) on the rising edge of CLK. The final register in the shift register will be shifted toward the serial output (SOP) on the falling edge of CLK. A high level at the $\overline{CE}$ pin inhibits the serial shifting, which is demonstrated in Figure 21. After 8 consecutive CLK cycles, the serial output (SOP) remains at the level of the serial input (SIP) which is internally pulled to logic high. A logic high at the $\overline{CE}$ pin is required to signify the end of the serial data output. For of a daisy chained configuration, the serial output (SOP) of the SN65HVS883 can be connected to the serial input (SIP) of a following device, and additional clock cycles are required to shift the additional data out of the chain. The number of consecutive clock cycles will equal 8 times the number of devices in the chain. See Figure 22 for an example of a cascaded chain of 4x SN65HVS883.


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# 9 Application and Implementation

**NOTE**

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## 9.1 Application Information

### 9.1.1 System-Level EMC

The SN65HVS883 must operate reliably in harsh industrial environments. At a system level, the device is tested according to several international electromagnetic compatibility (EMC) standards.

In addition to the device internal ESD structures, external protection circuitry, such as the one in Figure 17, can be used to absorb as much energy from burst- and surge-transients as possible.

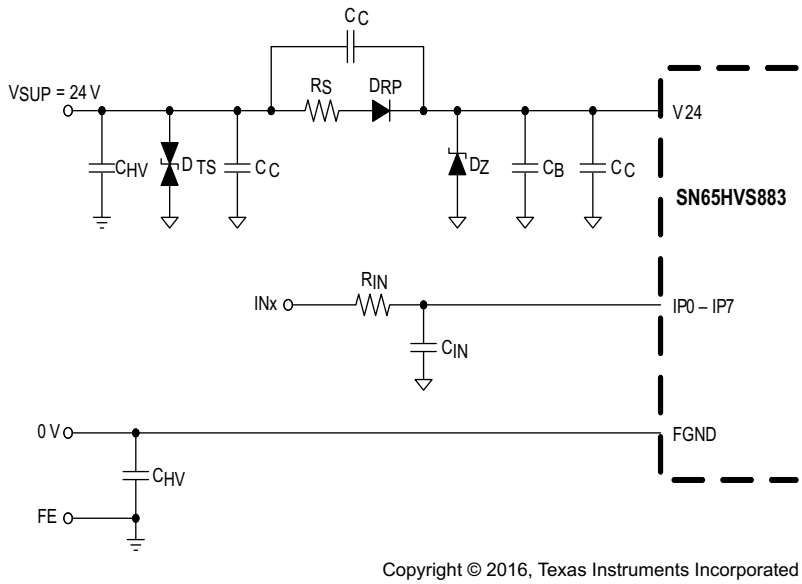


**Figure 17. Typical EMC Protection Circuitry for Supply and Signal Inputs**

**Table 3. Components**

| DESIGNATOR | DESCRIPTION |
|---|---|
| $D_{TS}$ | 39 V Transient Voltage Suppressor: SM15T39CA |
| $D_{RP}$ | Super Rectifier: BYM10-1000,<br>or General Purpose rectifier: 1N4007 |
| $D_Z$ | 33 V – 36 V fast Zener Diode, Z2SMB36 |
| $R_S$ | 56 Ω, 1/3 W MELF Resistor |
| $R_{IN}$ | 1.2 kΩ, 1/4 W MELF Resistor |
| $C_{IN}$ | 22 nF, 60 V Ceramic Capacitor |
| $C_{HV}$ | 4.7 nF, 2 kV Ceramic Capacitor |
| $C_C$ | n x 220 nF, 60 V Ceramic Capacitors |
| $C_B$ | 1 µF - 10 µF, 60 V Ceramic Capacitor |

### 9.1.2 Input Channel Switching Characteristics

The input stage of the SN65HVS883 is so designed, that for an input resistor $R_{IN}$ = 1.2 kΩ the trip point for signalling an ON-condition is at 9.4 V at 3.6 mA. This trip point satisfies the switching requirements of IEC61131-2 Type 1 and Type 3 switches.

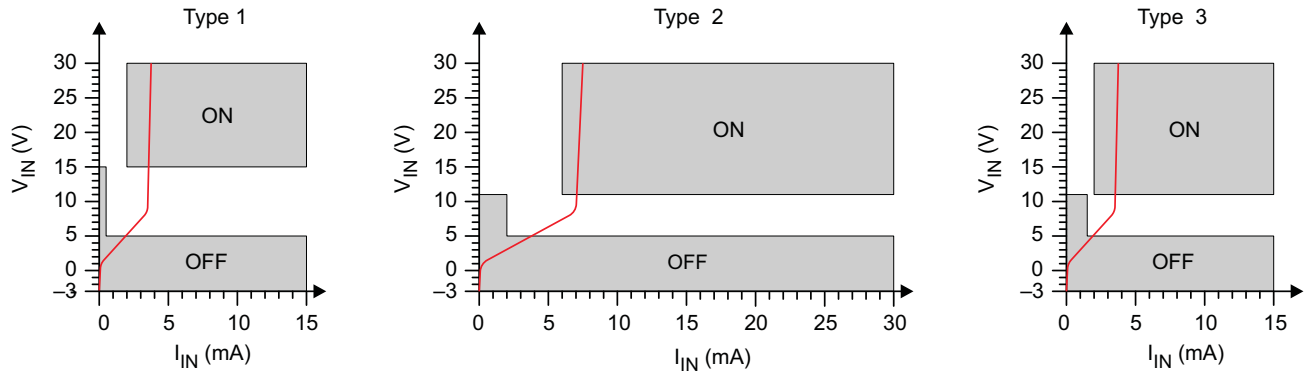


**Figure 18. Switching Characteristics for IEC61131-2 Type 1, 2, and 3 Proximity Switches**

For a Type 2 switch application, two inputs are connected in parallel. The current limiters then add to a total maximum current of 7.2 mA. While the return-path (RE-pin), of one input might be used to drive an indicator LED, the RE-pin of the other input channel should be connected to ground (FGND).

Paralleling input channels reduces the number of available input channels from an octal Type 1 or Type 3 input to a quad Type 2 input device. Note, that in this configuration output data of an input channel is represented by two shift register bits.

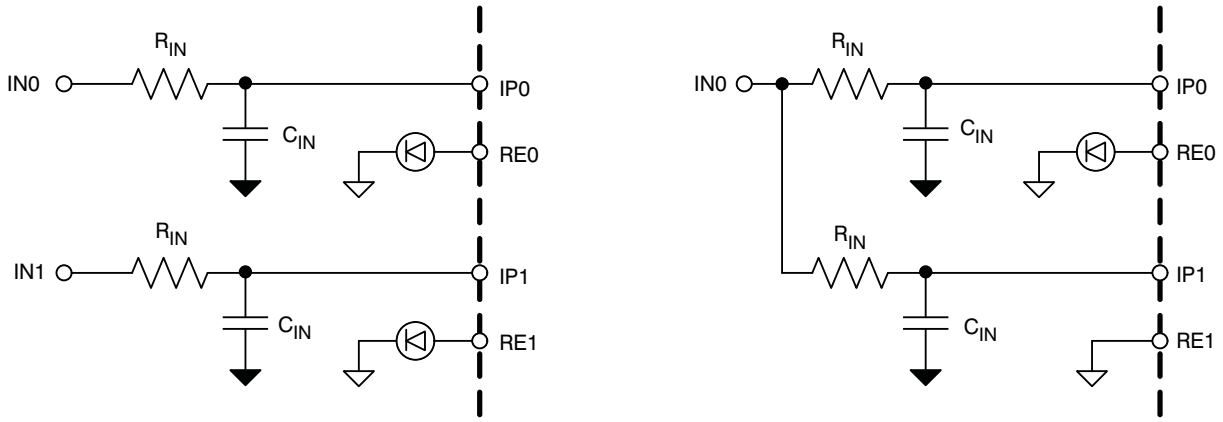


**Figure 19. Paralleling Two Type 1 or Type 3 Inputs Into One Type 2 Input**


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### 9.1.3 Digital Interface Timing

The digital interface of the SN65HVS883 is SPI compatible and interfaces, isolated or non-isolated, to a wide variety of standard micro controllers.

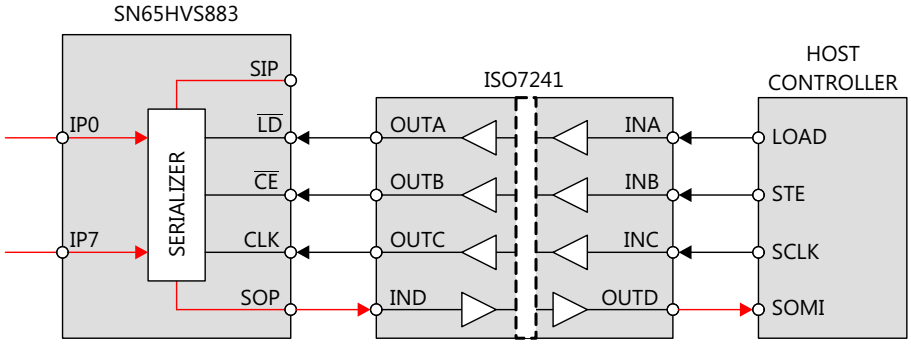


**Figure 20. Simple Isolation of the Shift Register Interface**

Upon a low-level at the load input, $\overline{LD}$, the information of the field inputs, IP0 to IP7 is latched into the shift register. Taking $\overline{LD}$ high again blocks the parallel inputs of the shift register from the field inputs. A low-level at the clock-enable input, $\overline{CE}$, enables the clock signal, CLK, to serially shift the data to the serial output, SOP. Data is clocked into the shift register at the rising edge of CLK and out of the shift register on the falling edge of CLK. Thus after eight consecutive clock cycles all field input data have been clocked out of the shift register and the information of the serial input, SIP, appears at the serial output, SOP.

The $\overline{CE}$ signal should only be transitioned low while the CLK signal is low which ensures that a rising edge of CLK occurs before a falling edge of CLK. This shifts the data into and through the shift register up until the final register before the first bit that was loaded into the final register is shifted out the serial output, SOP. If a falling edge of CLK is seen first following the transition of $\overline{CE}$ to low, the final register outputs the first bit, IP0, on the serial output, SOP, before shifting the rest of the bits through the shift register. The previous value of the second to last register prior to the $\overline{LD}$ event will then be shifted into the final register on the next rising CLK edge and output on the serial output, SOP, before the next valid bit, IP1, is output on the serial output, SOP. This appears as an erroneous bit in the serial data. Also, depending on how many falling CLK edges were seen before the $\overline{CE}$ signal is transitioned back high, the final bit, IP7, may not get shifted out of the shift register.

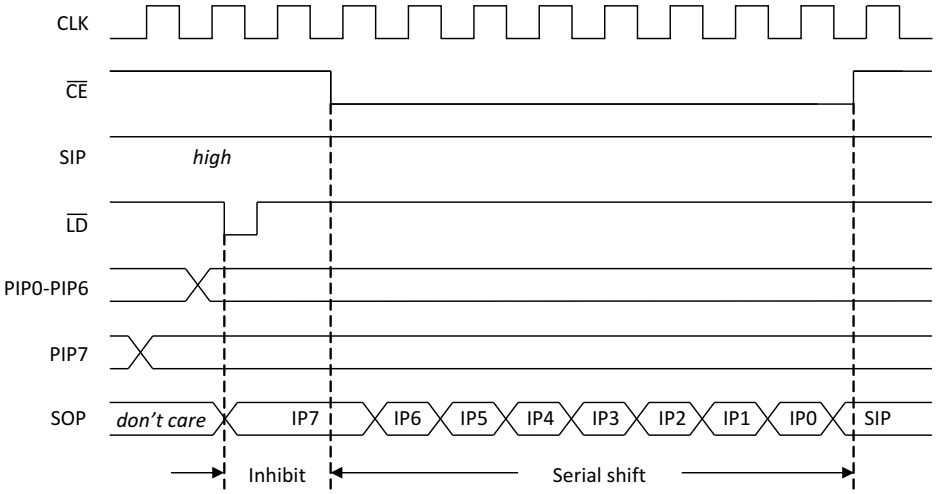


**Figure 21. Interface Timing for Parallel-Load and Serial-Shift Operation of the Shift Register**

### 9.1.4 Cascading for High Channel Count Input Modules

Designing high-channel count modules require cascading multiple SN65HVS883 devices. Simply connect the serial output (SOP) of a leading device with the serial input (SIP) of a following device without changing the processor interface.

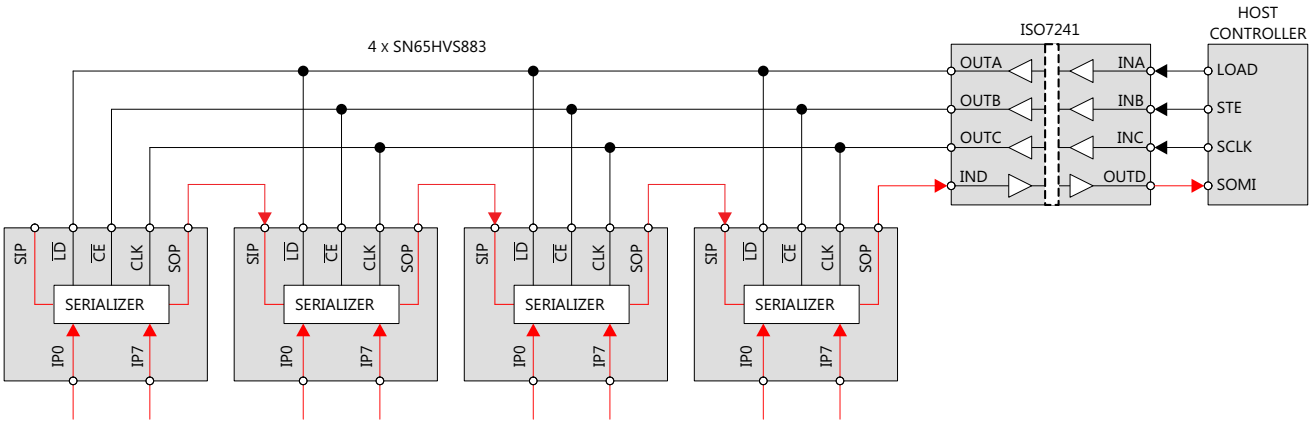


**Figure 22. Cascading Four SN65HVS883 for a 32-Channel Input Module**

**NOTE**

When daisy-chaining multiple devices, the maximum operating rate (CLK pulse width) may need to be restricted in order to maintain minimum set-up/hold timing relationships between the serial data (SIP/SOP) and the CLK line.

## 9.2 Typical Application

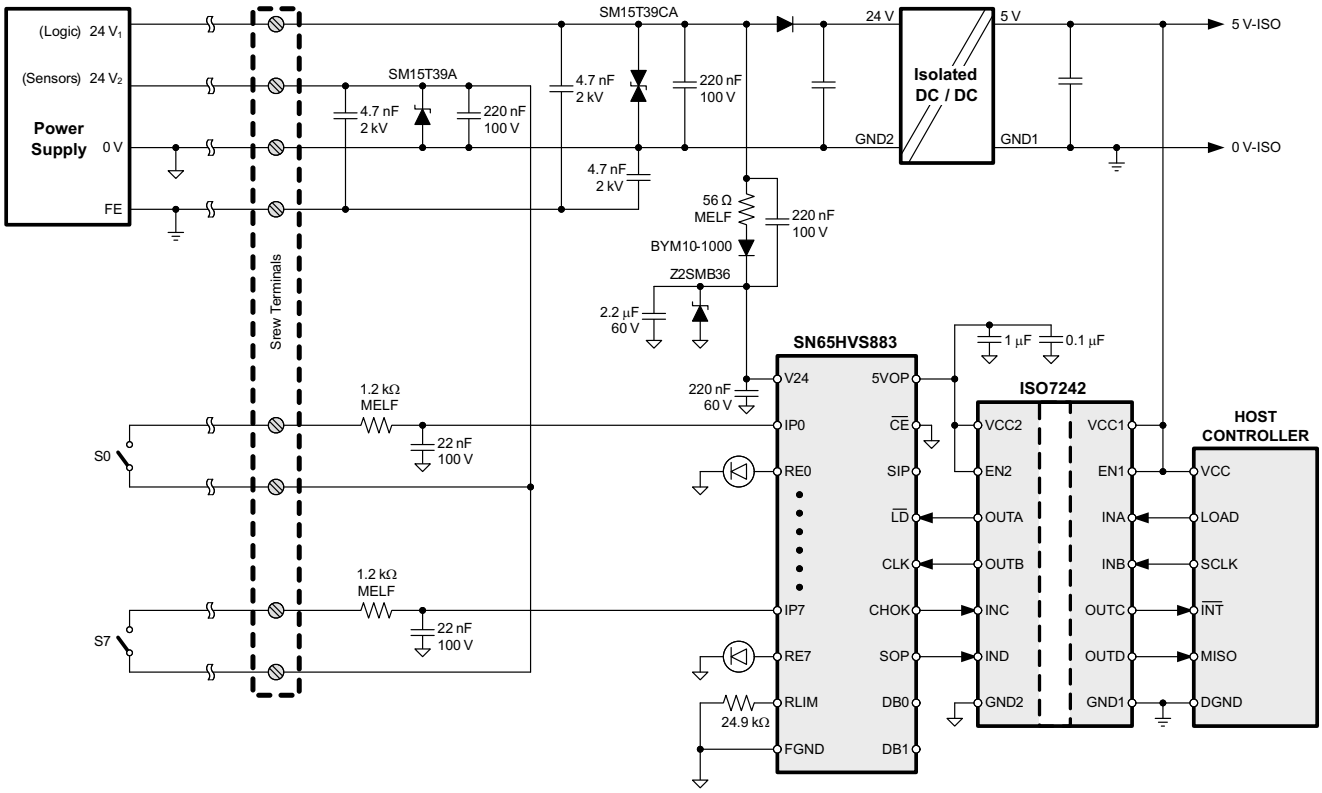


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**Figure 23. Typical Digital Input Module Application**


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## Typical Application (continued)

### 9.2.1 Design Requirements

The simplified schematic in Figure 23 demonstrates a typical application of the SN65HVS883 for sensing the state of digital switches with 24-V high logic levels. In this application, a 5-V host controller must receive the state of 8 switches as a serial input, while remaining isolated from the high voltage power supply.

### 9.2.2 Detailed Design Procedure

#### *9.2.2.1 Input Stage*

Selection of the current limiting resistor $R_{LIM}$ sets the input current limit $I_{LIM}$ for the device. *Digital Inputs* includes necessary equations for choosing the limiting resistor.

The On/Off voltage thresholds at the device pin $V_{TH(IP+)}$ and $V_{TH(IP-)}$ are fixed to 5.2 V and 4.3 V respectively, however the On/Off voltage thresholds of the field input $V_{TH(IN+)}$ and $V_{TH(IN-)}$ are determined by the value of the series resistor RIN placed between the field input and the device. The threshold voltage $V_{TH(IN+)}$ is determined with the following equation:

$$V_{TH(IN+)} = I_{IN} \times R_{IN} + V_{TH(IP+)} \tag{3}$$

Substituting Equation 1 and solving for $R_{IN}$ produces an equation for $R_{IN}$ given a desired on-threshold.

$$R_{IN} = \frac{(V_{TH(IN+)} - 5.2V) \times R_{LIM}}{90V} \tag{4}$$

The following equation can be used to calculate the off-threshold voltage given a value for $R_{IN}$

$$V_{TH(IN-)} = \frac{90V \times R_{IN}}{R_{LIM}} + V_{TH(IP-)} \tag{5}$$

Figure 24 contains an example input characteristic:

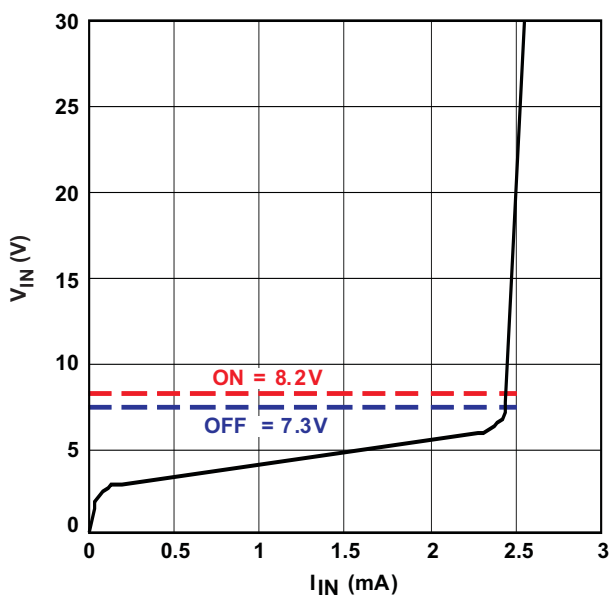


**Figure 24. SN65HVS883 Example Input Characteristic**

## Typical Application (continued)

#### *9.2.2.2 Setting Debounce Time*

The logic signals at the DB0 and DB1 pins determine the denounce times for the device according to the table in section 6.5. The DB0 and DB1 pins are internally pulled high. Connecting the pins to GND in different configurations allows for selection of 0, 1, or 3 ms debounce times. In noisy environments, it is recommended that unused DB pins should be connected externally to a 5 V supply.

#### *9.2.2.3 Example: High-Voltage Sensing Application*

For the high-voltage sensing application in Figure 23, inputs from each switch (S0-S7) are connected to the 8 parallel inputs (IP0-IP7) of the SN65HVS883 through 1.2 kΩ MELF resistors. Small capacitors (22 nF) are tied to ground at each input to provide noise protection for the signals. A resistor is added between the $R_{LIM}$ pin and GND to provide a device current limit according to the equation $I_{LIM}$ = 90 V / $R_{LIM}$. In this example, with a 24.9 kΩ resistor, the current limit for the device is set to 3.6 mA. LEDs are placed between pins RE0-RE7 to allow for external status observation of the parallel inputs. Finally the SN65HVS883 is connected through a digital isolation device to the host controller to provide galvanic isolation to the external interfaces and to allow for communication between the 5 V SN65HVS883 logic and the 5-V host controller. The host controller manages mode switching and clocking of the SN65HVS883 through the digital isolation device.

### 9.2.3 Application Curve

The application traces acquired in Figure 25 demonstrates the typical behavior of the SN65HVD883 when in shift mode (Load Pulse Input pulled high and Clock Enable Input pulled low). Channel 1 shows the SIP input, Channel 2 shows the CLK input, and Channel 3 shows the SOP output.

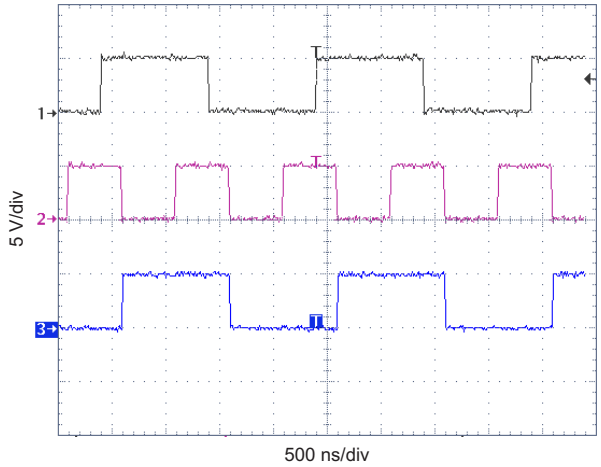


**Figure 25. SN65HVS883 Serial Input and Output Timing**


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# 10 Power Supply Recommendations

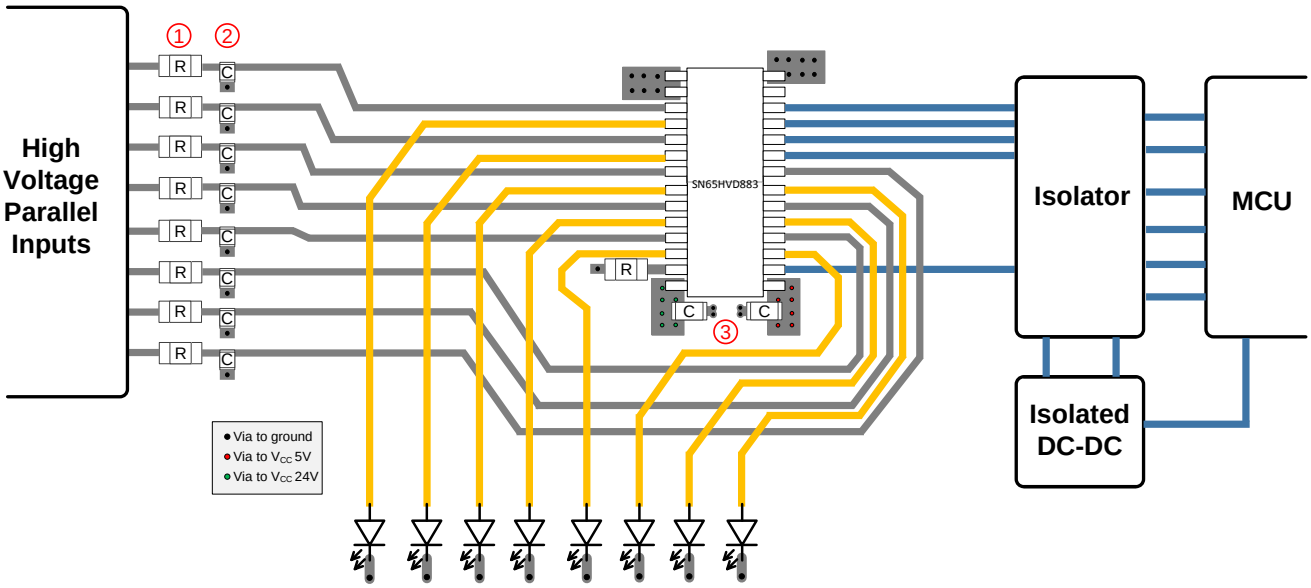
The SN65HVS883 operates within a recommended supply voltage range from 4.5 V to 5.5 V. A 0.1 µF or larger capacitor should be placed between $V_{CC}$ and ground to improve power supply noise immunity. A current limiting resistor can be used to reduce overall power consumption as described in *Digital Inputs*. The high voltage parallel field inputs can accept voltages ranging from 0 V to 34 V, however all other inputs must remain between 0 V to 5 V. Refer to the *Recommended Operating Conditions* table for more detailed voltage suggestions. High voltage field inputs should be buffered as shown in Figure 23 to improve input noise immunity.

# 11 Layout

## 11.1 Layout Guidelines

1. Place series MELF resistors between the field inputs and the device input pins.
2. Place small ~22 nF capacitors close to the field input pins to reduce noise.
3. Place a supply buffering 0.1-µF capacitor around as close to the $V_{CC}$ pin as possible.

## 11.2 Layout Example



# 12 デバイスおよびドキュメントのサポート

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## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN65HVS883PWPR | Active | Production | HTSSOP (PWP) \| 28 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | HVS883 |
| SN65HVS883PWPR.A | Active | Production | HTSSOP (PWP) \| 28 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | HVS883 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

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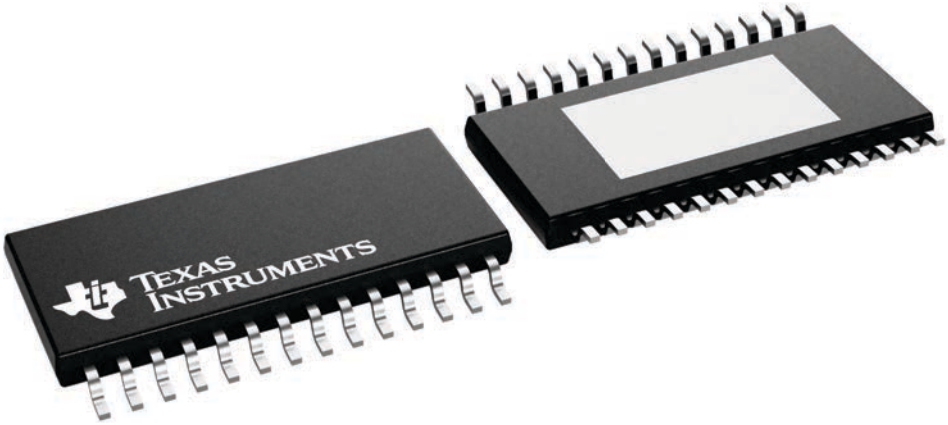
## PWP 28

## PowerPAD™ TSSOP - 1.2 mm max height

**4.4 x 9.7, 0.65 mm pitch**

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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