

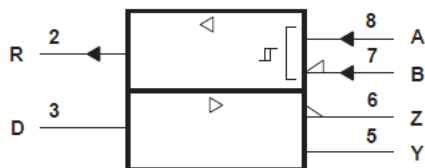
低消費電力、差動ライン・ドライバとレシーバのペア

1 特長

- 長いケーブルを使用する高速マルチポイント・データ伝送用に設計
- 最小 30ns のパルス幅で動作
- 低消費電流: 5mA 以下
- ANSI RS-485 と ISO 8482:1987(E) の規格要件を満たす、または上回る性能
- 7V~12V の同相電圧範囲
- 正と負の出力電流制限
- ドライバのサーマル・シャットダウン保護
- SN75179B とピン互換

2 概要

SN65LBC179、SN65LBC179Q、SN75LBC179 差動ドライバ/レシーバ・ペアは、伝送ラインの特性を考慮し、長いケーブルを使用する双方向データ通信向けに設計されたモノリシック IC です。本デバイスは、業界標準の ANSIRS-485 および ISO 8482:1987(E) の要件を満たすかそれを上回る、平衡型 (すなわち差動) 電圧モード・デバイスです。どちらのデバイスも、テキサス・インスツルメンツ独自の LinBiCMOS™ を使用して設計されており、CMOS の低消費電力とバイポーラ・トランジスタの高精度および堅牢性を同じ回路内で実現します。



A. この記号は ANSI/IEEE Std 91-1984 と IEC Publication 617-12 に準拠しています。

論理記号

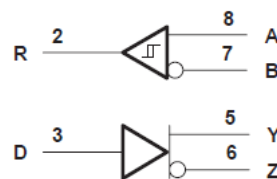
SN65LBC179、SN65LBC179Q、SN75LBC179 は、差動ライン・ドライバと差動ライン・レシーバを統合しており、5V 単電源で動作します。ドライバの差動出力とレシーバの差動入力、全二重動作のために個別の端子に接続されており、電源オフ ($V_{CC} = 0$) 時にバスの負荷が最小化されるように設計されています。これらのデバイスは同相電圧範囲が広いので、ポイント・ツー・ポイントまたはマルチポイントのデータ・バス・アプリケーションに適しています。またこれらのデバイスは、ライン・フォルト状態からの保護のために、正と負の電流制限機能とサーマル・シャットダウン機能を備えています。ライン・ドライバは、約 172°C の接合部温度でシャットダウンします。

SN65LBC179、SN65LBC179Q、SN75LBC179 は、8 ピンのデュアル・イン・ラインおよびスモール・アウトライン・パッケージで供給されます。動作温度範囲は、SN75LBC179 が 0°C ~ 70°C の商業用温度範囲、SN65LBC179 が -40°C ~ 85°C の産業用温度範囲、SN65LBC179Q が -40°C ~ 125°C の拡張産業用または車載用温度範囲です。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
SN75179B	D (SOIC)	4.9mm × 3.91mm
	P (PDIP)	9.81mm × 6.35mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



論理図 (正論理)



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3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision F (April 2006) to Revision G (October 2022)	Page
• 最新のデータシート・フォーマットに合わせてデータシートのフォーマットを変更.....	1
• Added the <i>Thermal Information</i> table.....	5

4 Pin Configuration and Functions

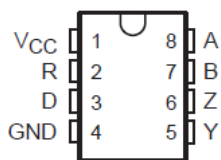


图 4-1. D or P Package (Top View)

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1	V _{CC}	P	5 V Voltage Supply
2	R	O	RS485 Logic Output
3	D	I	RS485 Logic Input
4	GND	G	Ground
5	Y	O	Non-Inverting RS485 Bus Output
6	Z	O	Inverted RS485 Bus Output
7	B	I	Inverted RS485 Bus Input
8	A	I	Non-Inverting RS485 Bus Input

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings

See note ⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.3	7	V
	Voltage range at A, B, Y, or Z ⁽²⁾	-10	15	V
	Voltage range at D or R ⁽²⁾	-0.3	V _{CC} + 0.5	V
I _O	Receiver output current		±10	mA
	Continuous total power dissipation ⁽³⁾	Internally limited		
P _(AVG)	Average power dissipation R _L = 54 Ω, input to D is 10 Mbps 50% duty cycle square wave, V _{CC} = 5.25 V, T _J = 130°C		330	mW
T _{SD}	Thermal shutdown junction temperature		165	°C
	Total power dissipation	See セクション 5.4		

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) The maximum operating junction temperature is internally limited. Uses the dissipation rating table to operate below this temperature.

5.2 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.75	5	5.25	V
V _{IH}	High-level input voltage	D	2			V
V _{IL}	Low-level input voltage	D			0.8	V
V _{ID}	Differential input voltage		-6 ⁽¹⁾		6	V
V _O , V _I , or V _{IC}	Voltage at any bus terminal (separately or common-mode)	A, B, Y, or Z	-7		12	V
I _{OH}	High-level output current	Y or Z			-60	mA
		R			-8	
I _{OL}	Low-level output current	Y or Z			60	mA
		R			8	
T _J	Junction temperature				140	°C
T _A	Operating free-air temperature	SN65LBC179	-40		85	°C
		SN65LBC179Q	-40		125	
		SN75LBC179	0		70	

- (1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for differential input voltage, voltage at any bus terminal (separately or common mode), operating temperature, input threshold voltage, and common-mode output voltage.

5.3 Thermal Information

THERMAL METRIC ⁽¹⁾		D (SOIC)	P (PDIP)	UNIT
		8 Pins	8 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	65.6.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.4	54.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.3	42.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.8	22.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62.6	41.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) See TI application note literature number [SZZA003](#), Package Thermal Characterization Methodologies, for an explanation of this parameter.

5.4 Dissipation Rating Table

PACKAGE	THERMAL MODEL	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	Low K ⁽¹⁾	526 mW	5.0 mW/°C	301 mW	226 mW
		882 mW	8.4 mW/°C	504 mW	378 mW
P	High K ⁽²⁾	840 mW	8.0 mW/°C	480 mW	360 mW

(1) In accordance with the low effective thermal conductivity metric definitions of EIA/JESD 51–3.

(2) In accordance with the high effective thermal conductivity metric definitions of EIA/JESD 51–7.

5.5 Electrical Characteristics - Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18\text{ mA}$				-1.5	V
$ V_{OD} $	Differential output voltage ⁽²⁾	$R_L = 54\ \Omega$ See 6-1	SN65LBC179, SN65LBC179Q	1.1	2.2	5	V
			SN75LBC179	1.5	2.2	5	
		$R_L = 60\ \Omega$ See 6-2	SN65LBC179, SN65LBC179Q	1.1	2.2	5	
			SN75LBC179	1.5	2.2	5	
$\Delta V_{OD} $	Change in magnitude of differential output voltage ⁽³⁾	See 6-1 and 6-2				± 0.2	V
V_{OC}	Common-mode output voltage	$R_L = 54\ \Omega$	See 6-1	1	2.5	3	V
$\Delta V_{OC} $	Change in magnitude of common-mode output voltage ⁽³⁾					± 0.2	V
I_O	Output current with power off	$V_{CC} = 0$,	$V_O = -7\text{ V to }12\text{ V}$			± 100	μA
I_{IH}	High-level input current	$V_I = 2.4\text{ V}$				-100	μA
I_{IL}	Low-level input current	$V_I = 0.4\text{ V}$				-100	μA
I_{OS}	Short-circuit output current	$-7\text{ V} \leq V_O \leq 12\text{ V}$				± 250	mA
I_{CC}	Supply current	No load	SN65LBC179, SN75LBC179		4.2	5	mA
			SN65LBC179Q		4.2	7	mA

(1) All typical values are at $V_{CC} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

(2) The minimum V_{OD} specification of the SN65179 may not fully comply with ANSI RS-485 at operating temperatures below 0°C . System designers should take the possibly lower output signal into account in determining the maximum signal transmission distance.

(3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in the steady-state magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

5.6 Switching Characteristics - Driver

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	$R_L = 54\ \Omega$	See 6-3	7	18	ns
$t_{t(OD)}$	Differential transition time			5	20	ns

5.7 Electrical Characteristics - Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$I_O = -8 \text{ mA}$				0.2	V
V_{IT-}	Negative-going input threshold voltage	$I_O = 8 \text{ mA}$		-0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				45		mV
V_{OH}	High-level output voltage	$V_{ID} = 200 \text{ mV}$,	$I_{OH} = -8 \text{ mA}$	3.5	4.5		V
V_{OL}	Low-level output voltage	$V_{ID} = -200 \text{ mV}$,	$I_{OL} = 8 \text{ mA}$		0.3	0.5	V
I_I	Bus input current	$V_I = 12 \text{ V}$, Other inputs at 0 V,	SN65LBC179, SN75LBC179		0.7	1	mA
		$V_{CC} = 5 \text{ V}$	SN65LBC179Q		0.7	1.2	mA
		$V_I = 12 \text{ V}$, Other inputs at 0 V,	SN65LBC179, SN75LBC179		0.8	1	mA
		$V_{CC} = 0 \text{ V}$	SN65LBC179Q		0.8	1.2	mA
		$V_I = -7 \text{ V}$, Other inputs at 0 V,	SN65LBC179, SN75LBC179		-0.5	-0.8	mA
		$V_{CC} = 5 \text{ V}$	SN65LBC179Q		-0.5	-1.0	mA
		$V_I = -7 \text{ V}$, Other inputs at 0 V,	SN65LBC179, SN75LBC179		-0.5	-0.8	mA
		$V_{CC} = 0 \text{ V}$	SN65LBC179Q		-0.5	-1.0	mA

5.8 Switching Characteristics - Receiver

$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PHL}	Propagation delay time, high- to low-level output	V _{ID} = −1.5 V to 1.5 V,	See 6-4	15		30	ns
t _{PLH}	Propagation delay time, low- to high-level output			15		30	ns
t _{sk(p)}	Pulse skew (t _{PHL} − t _{PLH})	See 6-4			3	6	ns
t _t	Transition time				3	5	ns

5.9 Typical Characteristics

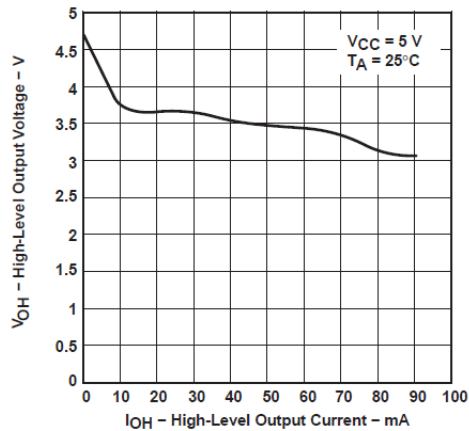


Figure 5-1. Driver High-Level Output Voltage vs High-Level Output Current

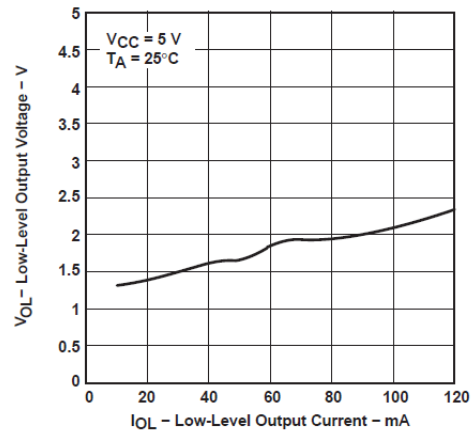


Figure 5-2. Driver Low-Level Output Voltage vs Low-Level Output Current

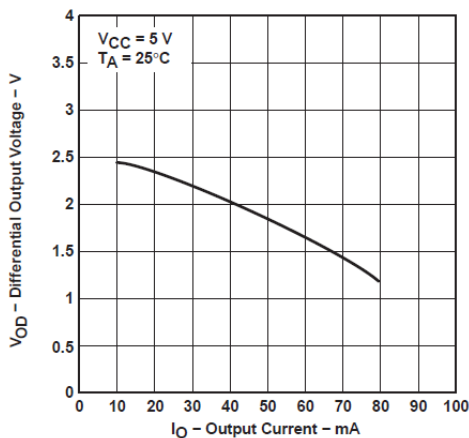


Figure 5-3. Driver Differential Output Voltage vs Output Current

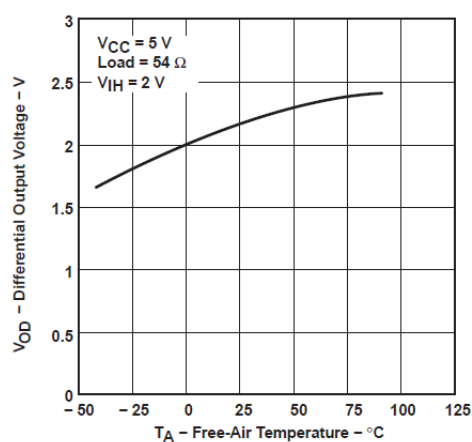


Figure 5-4. Driver Differential Output Voltage vs Free-Air Temperature

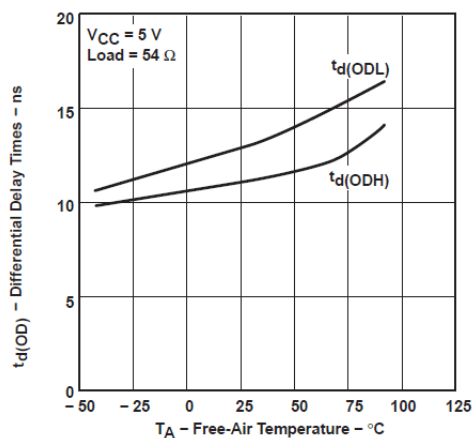


Figure 5-5. Driver Differential Delay Time vs Free-Air Temperature

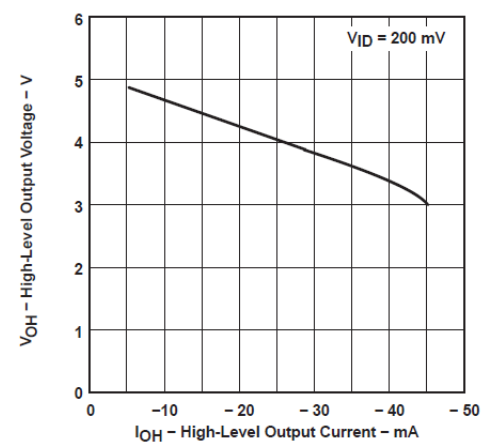


Figure 5-6. Receiver High-Level Output Voltage vs High-Level Output Current

5.9 Typical Characteristics (continued)

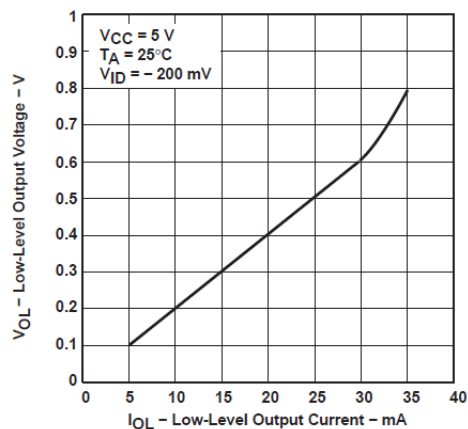


FIG 5-7. Receiver Low-Level Output Voltage vs Low-Level Output Current

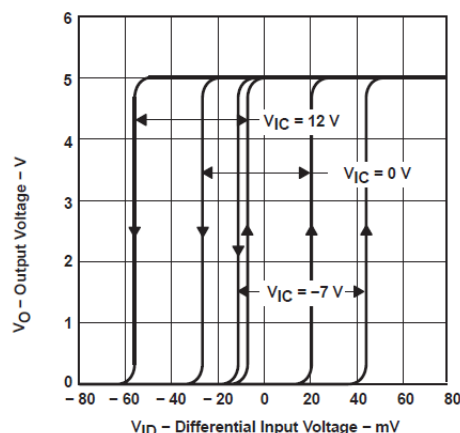


FIG 5-8. Receiver Output Voltage vs Differential Input Voltage

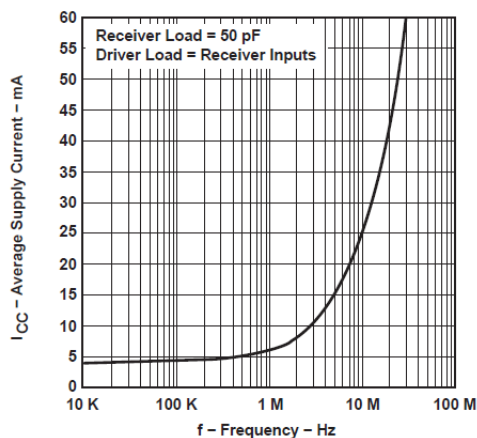


FIG 5-9. Average Supply Current vs Frequency

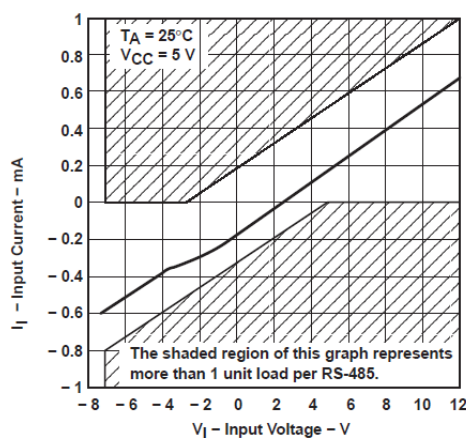


FIG 5-10. Receiver Input Current vs Input Voltage (Complementary Input at 0 V)

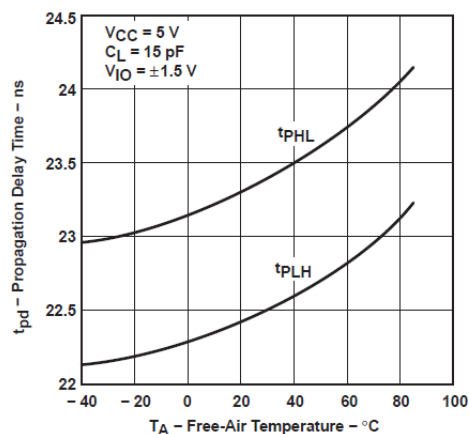


FIG 5-11. Receiver Propagation Delay Time vs Free-Air Temperature

6 Parameter Measurement Information

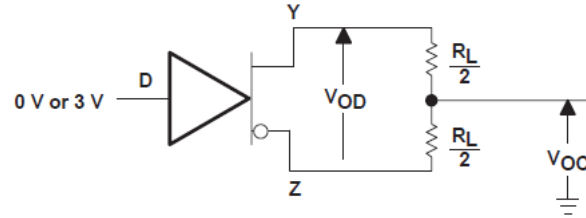


Figure 6-1. Differential and Common-Mode Output Voltage Test Circuit

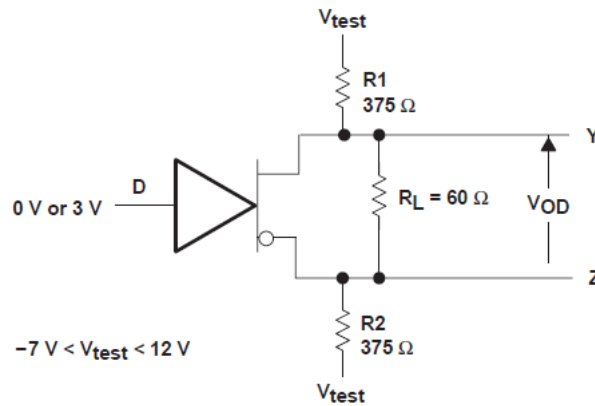
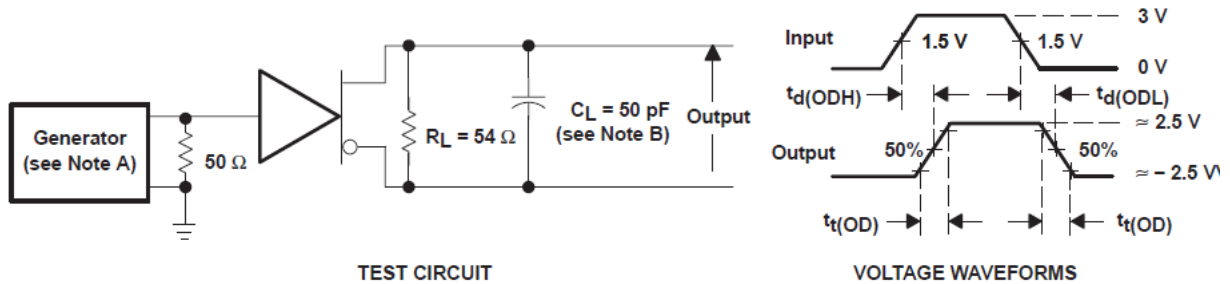
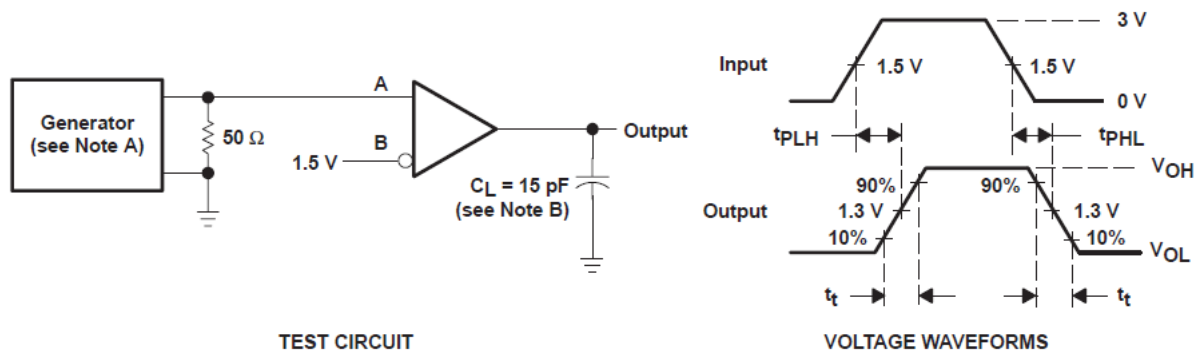


Figure 6-2. Differential Output Voltage Test Circuit



- A. The input pulse is supplied by a generator having the following characteristics: $\text{PRR} \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.
- B. C_L includes probe and jig capacitance.

Figure 6-3. Driver Test Circuits and Differential Output Delay and Transition Time Voltage Waveforms



- A. The input pulse is supplied by a generator having the following characteristics: $\text{PRR} \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.
- B. C_L includes probe and jig capacitance.

FIG 6-4. Receiver Test Circuit and Propagation Delay and Transition Time Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram

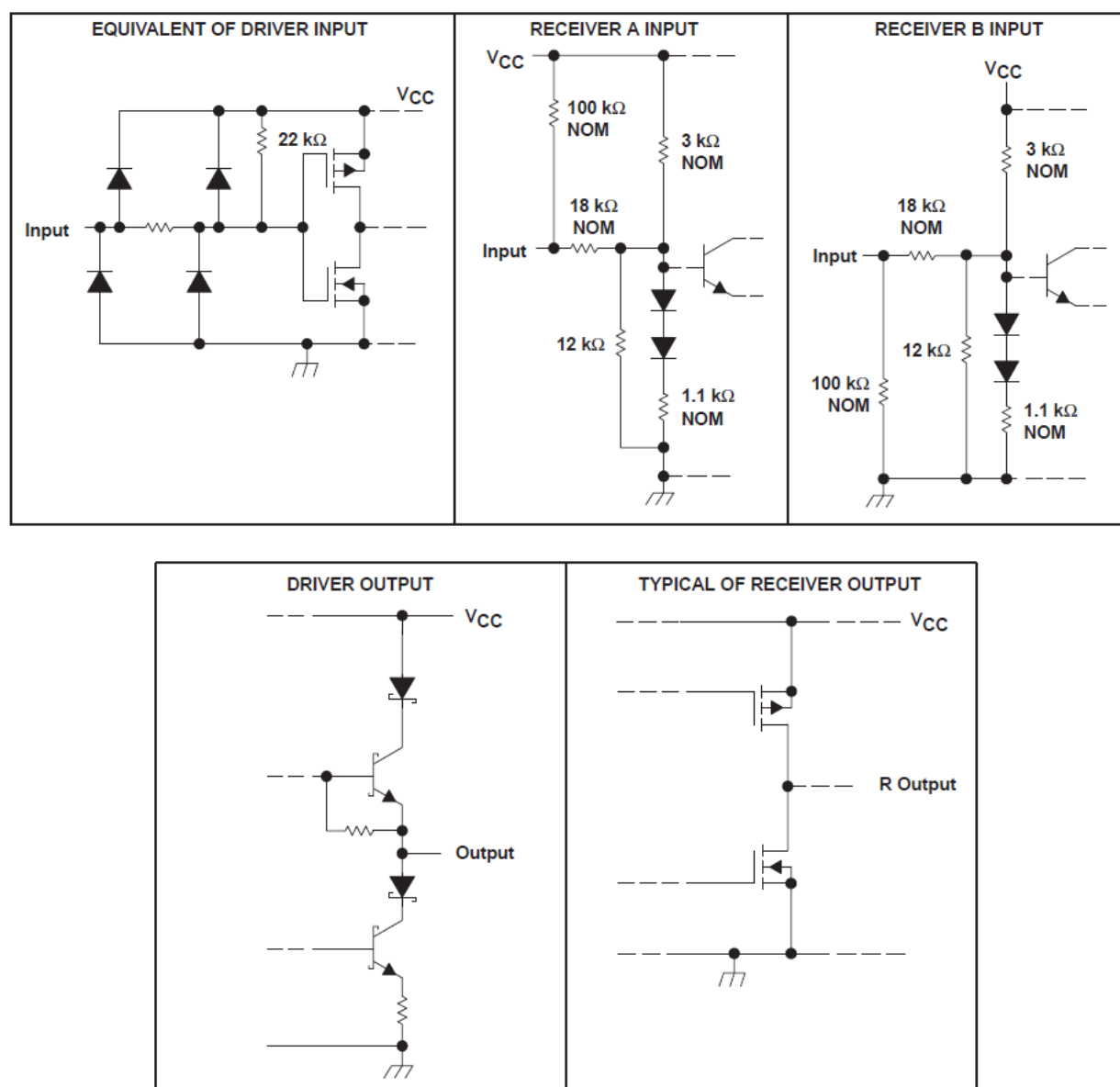


图 7-1. Schematics of Inputs and Outputs

7.2 Device Functional Modes

Function Tables

表 7-1. Driver⁽¹⁾

INPUT D	OUTPUTS	
	Y	Z
H	H	L
L	L	H

(1) H = high level, L = low level, ? = indeterminate

表 7-2. Receiver⁽¹⁾

DIFFERENTIAL INPUTS A-B	OUTPUT R
$V_{ID} \geq 0.2 \text{ V}$	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$	?
$V_{ID} \leq -0.2 \text{ V}$	L
Open circuit	H

(1) H = high level, L = low level, ? = indeterminate

7.3 Thermal Characteristics of IC Packages

θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power.

θ_{JA} is not a constant and is a strong function of:

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

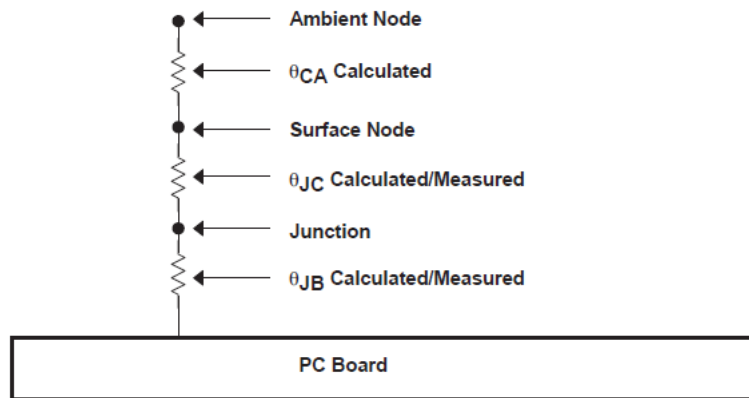
TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance and consists of a single trace layer 25 mm long and 2-oz thick copper. The high-k board gives *best case* in-use condition and consists of two 1-oz buried power planes with a single trace layer 25 mm long with 2-oz thick copper. A 4% to 50% difference in θ_{JA} can be measured between these two test cards.

θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is not a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with θ_{JB} in 1-dimensional thermal simulation of a package system.

θ_{JB} (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure. θ_{JB} is only defined for the high-k test card.

θ_{JB} provide an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGAs with thermal balls) and can be used for simple 1-dimensional network analysis of package system (see [Figure 7-2](#)).



7-2. Thermal Resistance

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device Support

8.2 Documentation Support

8.2.1 Related Documentation

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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8.5 Trademarks

LinBiCMOS™ is a trademark of LinBiCMOS.

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LBC179D	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	6LB179
SN65LBC179DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB179
SN65LBC179DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB179
SN65LBC179DRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB179
SN65LBC179P	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65LBC179
SN65LBC179P.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65LBC179
SN65LBC179QD	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 125	LB179Q
SN65LBC179QDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LB179Q
SN65LBC179QDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LB179Q
SN65LBC179QDRG4	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 125	LB179Q
SN75LBC179D	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	0 to 70	7LB179
SN75LBC179P	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75LBC179
SN75LBC179P.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75LBC179

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

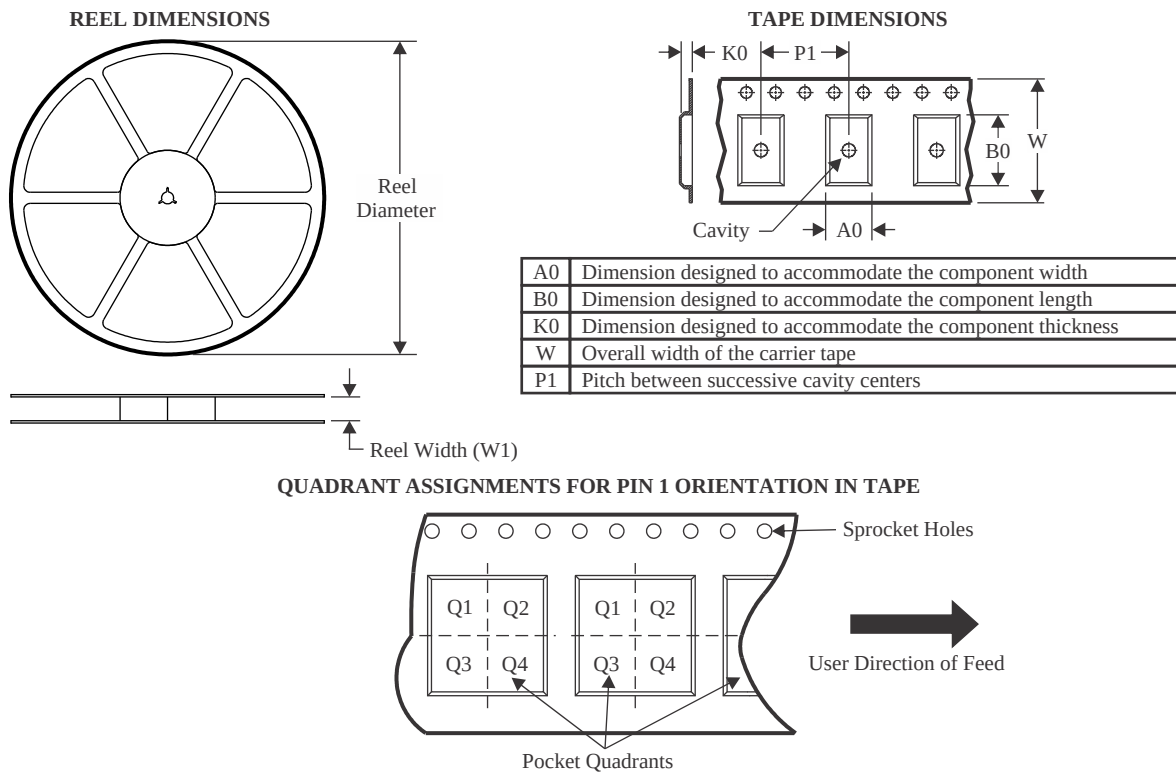
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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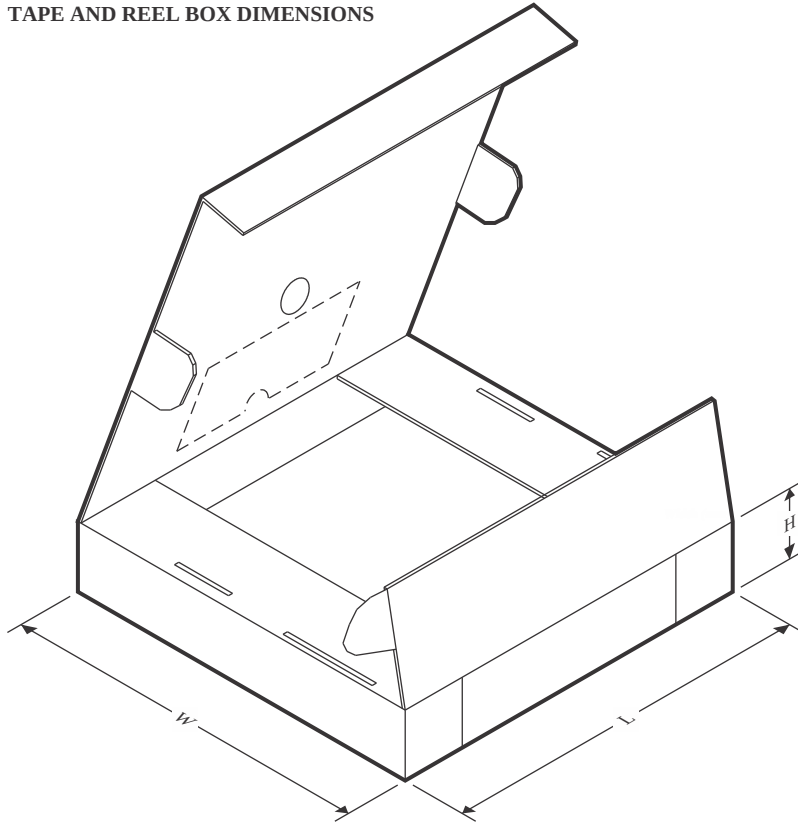
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC179DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

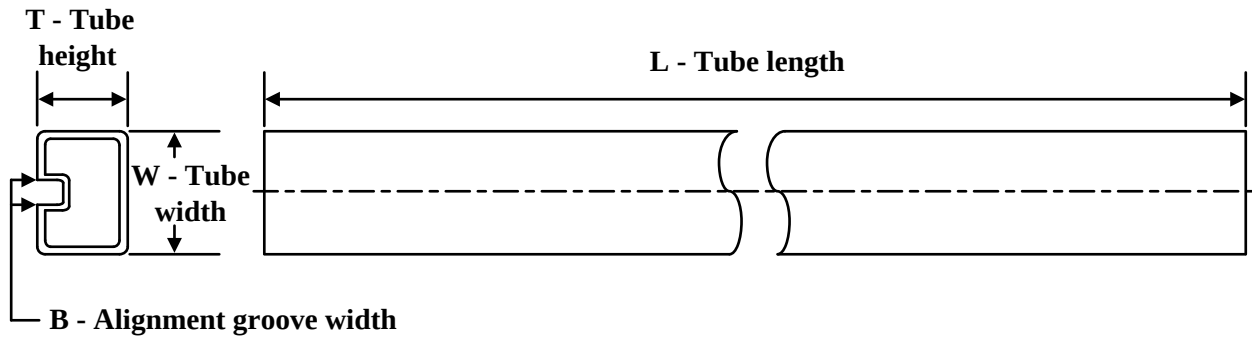
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC179DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

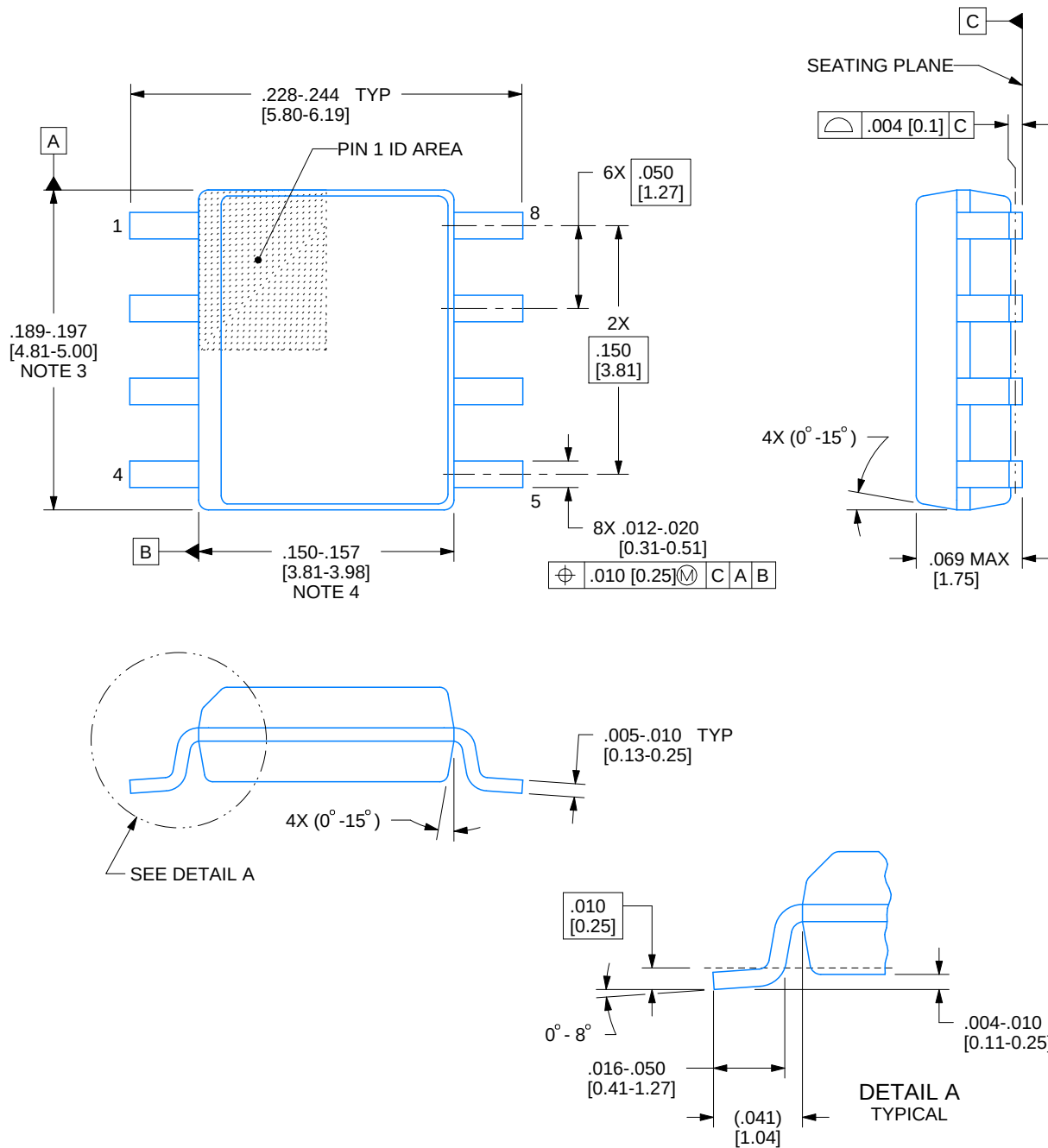
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65LBC179P	P	PDIP	8	50	506	13.97	11230	4.32
SN65LBC179P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75LBC179P	P	PDIP	8	50	506	13.97	11230	4.32
SN75LBC179P.A	P	PDIP	8	50	506	13.97	11230	4.32

D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

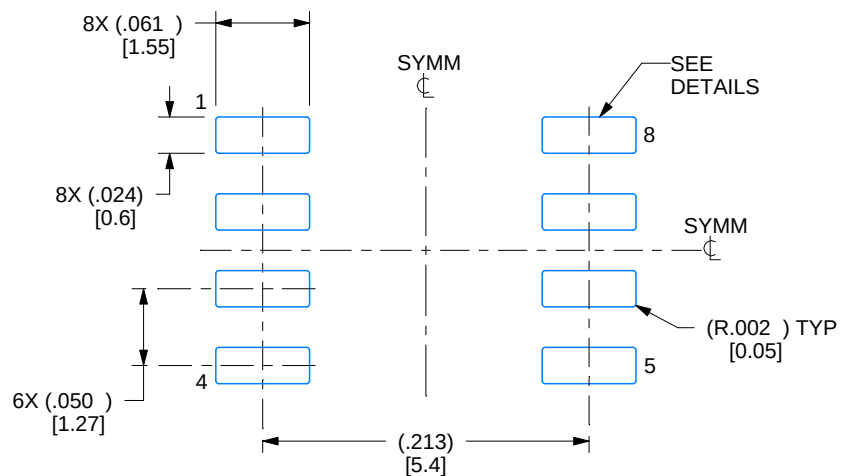
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

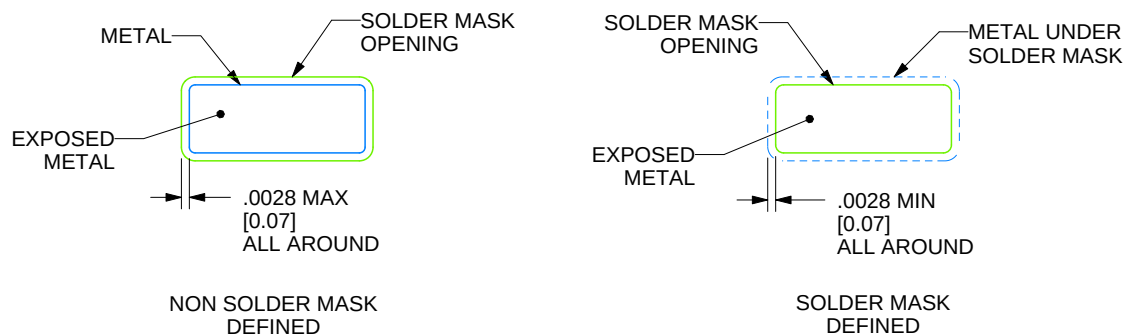
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

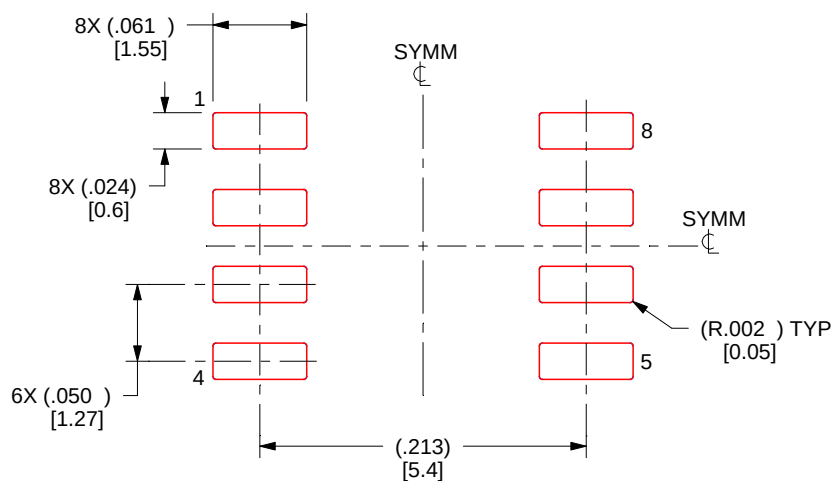
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

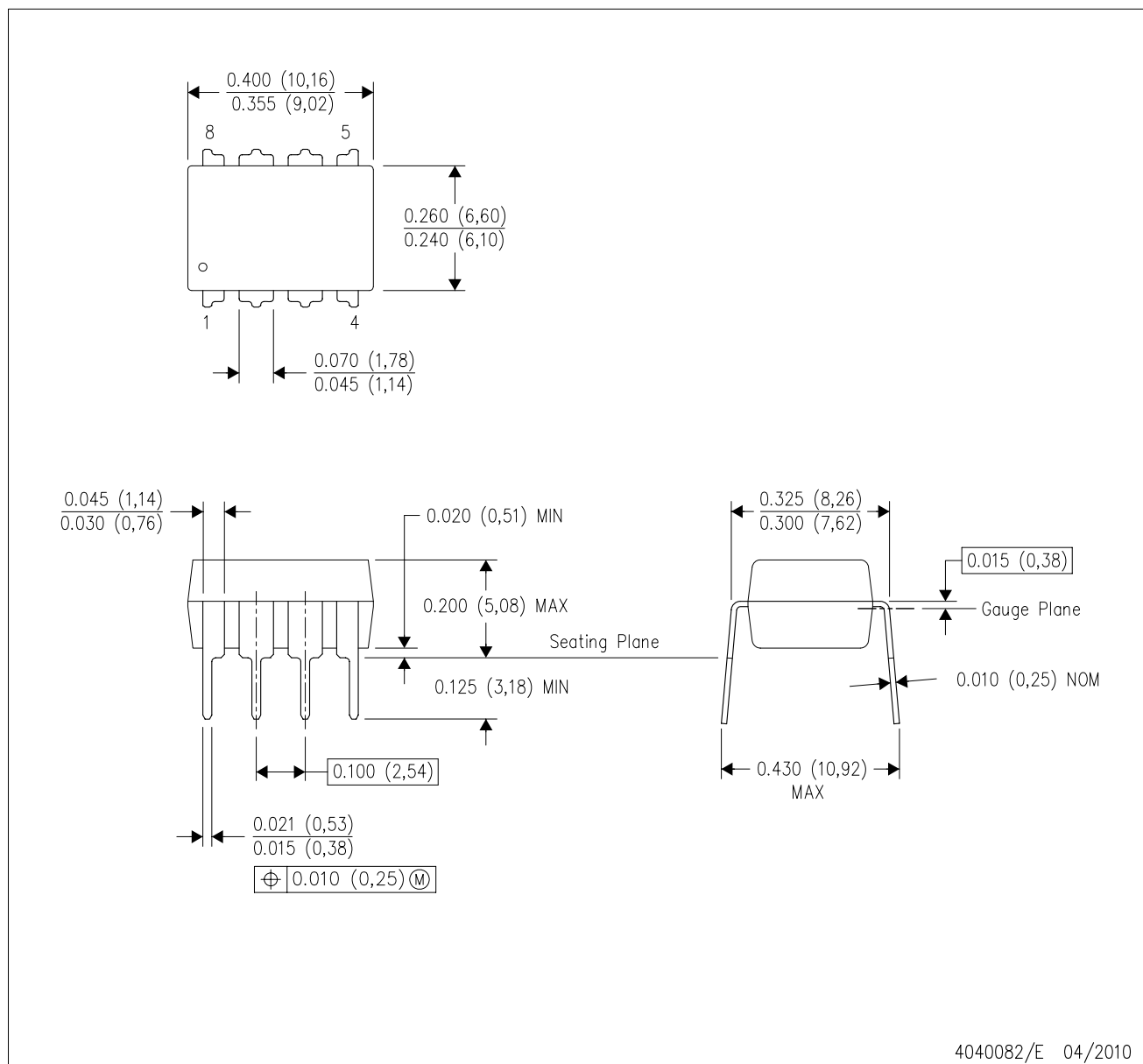
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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