TEXAS INSTRUMENTS
SN55LBC180, SN65LBC180, SN75LBC180
JAJSOF8I – FEBRUARY 1994 – REVISED OCTOBER 2022

低消費電力の RS-485 ライン・ドライバとレシーバのペア

1 特長

- 長いケーブルを使用する高速マルチポイント・データ伝送用に設計
- 最小 30ns のパルス持続時間で動作
- 低消費電流：5mA 以下
- ANSI 規格 RS-485 および ISO 8482：1987(E) の要件に適合またはそれを上回る性能
- パーティライン・バス用の 3 ステート出力
- -7V～12V の同相電圧範囲
- サーマル・シャットダウン保護機能により、バス競合によるドライバの損傷を防止
- 正および負の出力電流制限
- SN75ALS180 とピン互換

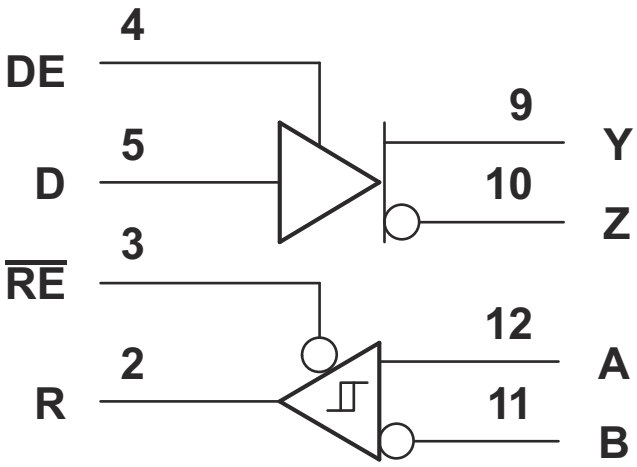
2 概要

SN55LBC180、SN65LBC180、SN75LBC180 差動ドライバとレシーバのペアは、伝送ラインの特性を考慮し、長いケーブルを使用する双方向データ通信向けに設計されたモノリシック IC です。これらのデバイスは、業界標準の ANSI RS-485 および ISO 8482：1987(E) の要件を満たすかそれを上回る、平衡型 (すなわち差動) 電圧モード・デバイスです。これらのデバイスは、テキサス・インスツルメンツ独自の LinBiCMOS™ を使用して設計されており、CMOS の低消費電力とバイポーラ・トランジスタの高精度および堅牢性を同じ回路内で実現します。

パッケージ情報

部品番号	パッケージ(1)	本体サイズ (公称)
SN75LBC180 SN65LBC180	N (PDIP)	19.3mm × 63.5mm
	D (SOIC)	8.65mm × 3.91mm
	RSA (QFN)	4mm × 4mm
SN55LBC180	RSA (QFN)	4mm × 4mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



論理図 (正論理)

Table of Contents

3 概要 (続き)

SN55LBC180、SN65LBC180、SN75LBC180 は、差動ライン・ドライバおよびレシーバと 3 ステート出力を組み合わせて 5V 単電源で動作します。ドライバとレシーバはそれぞれアクティブ HIGH、アクティブ LOW のイネーブルを備えており、それらのイネーブルを外部で接続することで、方向制御として機能させることができます。ドライバの差動出力とレシーバの差動入力は、全二重動作のために個別の端子に接続されており、ディセーブルまたは電源オフ (V_{CC} = 0) にかかわらず、バスに最小限の負荷を供給するように設計されています。これらのデバイスは同相電圧範囲が広いため、ポイント・ツー・ポイントまたはマルチポイントのデータ・バス・アプリケーションに適しています。

またこれらのデバイスは、ライン・フォルト状態からの保護のために、正および負の出力電流制限機能とサーマル・シャットダウン機能を備えています。ライン・ドライバは、約 172℃の接合部温度でシャットダウンします。

SN75LBC180 は 0℃～70℃の商用温度範囲で動作が規定されています。SN65LBC180 は –40℃～85℃の産業用温度範囲で動作が規定されています。

SN55LBC180 は –55℃～125℃の軍用温度範囲で動作が規定されています。

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision H (June 2022) to Revision I (October 2022) **Page**

- Changed RSA (QFN) values in the *Thermal Information Table* 6

Changes from Revision G (April 2009) to Revision H (June 2022) **Page**

- 「注文情報」表を「パッケージ情報」表に変更 1
- Added the *Pin Configuration and Functions* 4
- Added the *Thermal Information Table* 6
- Fixed the typo in the unit for the Receiver enable I_{IH} to change the unit from A to µA 7
- Updated 図 6-1, 図 6-2, and 図 6-3, limiting the x-axis to a maximum of 70 mA driver output current 9
- Updated 図 9-1 to remove legacy terminology 17

Changes from Revision F (March 2009) to Revision G (April 2009) **Page**

- Added 3 ESD rows to the *Absolute Maximum Ratings* 5

Changes from Revision E (February 2006) to Revision F (March 2009) **Page**

- データシートのタイトルで「差動」を「RS-485」に変更 1
- デバイス番号 SN55LBC180 を追加。 1
- 「両方」を「これら」に変更 1
- 「注文情報」表を追加 1
- 「概要 (続き)」セクションを変更 2
- 「機能表」を変更し、先頭ページから「概要（続き）」セクションに移動 2
- Deleted condition, moved cross reference 5
- Added all symbols in text that were not appearing in the PDF 5
- Deleted T_A row from the *Absolute Maximum Ratings* 5
- Added the last column to *Dissipation Rating Table* 5
- Added a row to T_A in the *Recommended Operating Conditions* for SN55LBC180 5
- Added SN55LB180 to the $|V_{OD}|$ row 6
- Change: moved 5 max values to the min column (-1.5, -50, -100, -0.8, -0.8) 7
- Added the *Switching Characteristics: SN55LBC180* table 8
- Changed moved schematics to the Typical Characteristics section 16

5 Pin Configuration and Functions

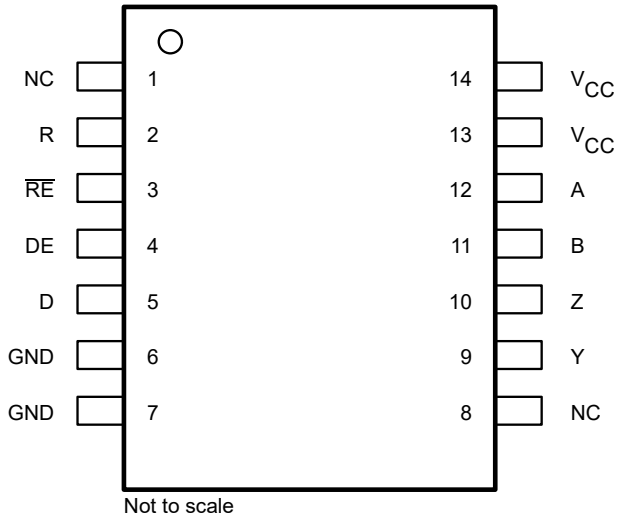


図 5-1. D OR N Package (SOIC)
(Top View)

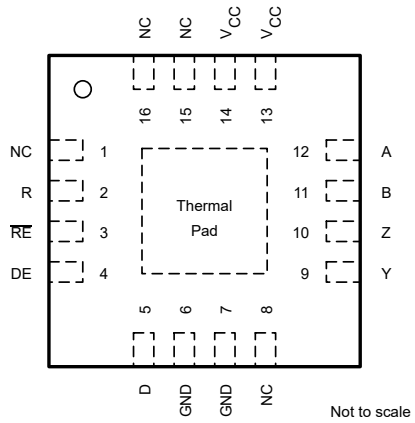


図 5-2. RSA Package (QFN)
(Top View)

表 5-1. Pin Functions

PIN NAME	PIN NO		TYPE(1)	DESCRIPTION
	D Or N	RSA		
NC	1	1	NC	No internal connection
R	2	2	O	Receiver output
$\overline{RE}$	3	3	I	Receiver enable input. Active low.
DE	4	4	I	Driver enable input. Active high
D	5	5	I	Driver input pin
GND	6, 7	6, 7	G	Ground connection. Pins 6 and 7 are connected together internally.
NC	8	8	NC	No internal connection
Y	9	9	O	Bus output port (complementary to Z)
Z	10	10	O	Bus output port (complementary to Y)
B	11	11	I	Bus input port (complementary to A)
A	12	12	I	Bus input port (complementary to B)
V_{CC}	13, 14	13, 14	P	Supply input pins. Pins 13 and 14 are connected together internally.
NC	N/A	15, 16	NC	No internal connection

(1) Signal Types: I = Input, O = Output, P= Power input,

6 Specifications

6.1 Absolute Maximum Ratings

See note (1)

				UNIT
V_{CC}	Supply voltage range (2)		–0.3 to 7	V
V_{BUS}	Bus voltage range (A, B, Y, Z)(2)		–10 to 15	V
	Voltage range at D, R, DE, $\overline{RE}$ (2)		–0.3 to V_{CC} + 0.5	V
	Continuous total power dissipation(3)		Internally limited	
	Total power dissipation		See Dissipation Rating Table	
T_{stg}	Storage temperature range		–65 to 150	°C
I_O	Receiver output current range		–50 to 50	mA
ESD	Electrostatic discharge	HBM (Human Body Model) EIA/JESD22-A114	±4	kV
		MM (Machine Model) EIA/JESD22-A115	400	V
		CDM (Charge Device Model) EIA/JESD22-C101	1.5	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

6.2 Dissipation Rating Table

PACKAGE(1)	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	—
N	1150 mW	9.2 mW/°C	736 mW	598 mW	—
RSA	3333 mW	26.67 mW/°C	2133 mW	1733 mW	400 mW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2			V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$			0.8	V
V_{ID}	Differential input voltage		–6(1)		6	V
V_O, V_I, or V_{IC}	Voltage at any bus terminal (separately or common mode)	A, B, Y, or Z	–7(1)		12	V
I_{OH}	High-level output current	Y or Z			–60	mA
		R			–8	
I_{OL}	Low-level output current	Y or Z			60	mA
		R			8	
T_A	Operating free-air temperature	SN55LBC180	–55		125	°C
		SN65LBC180	–40		85	
		SN75LBC180	0		70	

(1) The algebraic convention where the least positive (more negative) limit is designated minimum, is used in this data sheet for the differential input voltage, voltage at any bus terminal, operating temperature, input threshold voltage, and common-mode output voltage.

6.4 Thermal Information Table

THERMAL METRIC[1]		D (SOIC)	N (PDIP)	RSA (QFN)	UNIT
		14 Pins	14 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.2	53.4	38.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.5	40.0	35.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	33.2	17.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.2	19.0	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.9	32.9	17.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	7.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Driver Section

6.5.1 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = -18 mA				–1.5	V
$\lvert V_{OD} \rvert$	Differential output voltage magnitude[2]	R_L = 54 Ω, See 図 7-1	SN55LBC180	1	2.5	5	V
			SN65LBC180	1.1	2.5	5	
			SN75LBC180	1.5	2.5	5	
		R_L = 60 Ω, See 図 7-2	SN55LBC180	1	2.5	5	
			SN65LBC180	1.1	2	5	
			SN75LBC180	1.5	2	5	
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage[3]	See 図 7-1 and 図 7-2				±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω,	See 図 7-1	1	2.5	3	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage[3]					±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = –7 V to 12 V			±100	µA
I_{OZ}	High-impedance-state output current	V_O = –7 V to 12 V				±100	µA
I_{IH}	High-level input current	V_I = 2.4 V				100	µA
I_{IL}	Low-level input current	V_I = 0.4 V				100	µA
I_{OS}	Short-circuit output current	–7 V ≤ V_O ≤ 12 V				±250	mA
I_{CC}	Supply current	Receiver disabled	Outputs enabled			5	mA
			Outputs disabled			3	

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) The minimum V_{OD} specification may not fully comply with ANSI RS-485 at operating temperatures below 0°C. System designers should take the possibly lower output signal into account in determining the maximum signal-transmission distance.
(3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in the steady-state magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

6.5.2 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω,	See 図 7-3	7	12	18	ns
$t_{t(OD)}$	Differential output transition time			5	10	20	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See 図 7-4			35	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See 図 7-5			35	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See 図 7-4			50	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See 図 7-5			35	ns

6.5.3 Switching Characteristics: SN55LBC180

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω,	See 図 7-3		15		ns
$t_{t(OD)}$	Differential output transition time				21		ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See 図 7-4		32		ns
t_{PHZ}	Output disable time from high level				55		
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See 図 7-5		32		ns
t_{PLZ}	Output disable time from low level				20		

6.6 Receiver Section

6.6.1 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = –8 mA				0.2	V
$V_{IT–}$	Negative-going input threshold voltage	I_O = 8 mA		–0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT–}$)				45		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA		-1.5			V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = –8 mA	3.5	4.5		V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV,	I_{OL} = 8 mA		0.3	0.5	V
I_{OZ}	High-impedance-state output current	V_O = 0 V to V_{CC}				±20	µA
I_{IH}	High-level enable-input current	V_{IH} = 2.4 V		–50			µA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V		–100			µA
I_I	Bus input current	V_I = 12 V, V_{CC} = 5 V,	Other input at 0 V		0.7	1	mA
		V_I = 12 V, V_{CC} = 0 V,	Other input at 0 V		0.8	1	
		V_I = -7 V, V_{CC} = 5 V,	Other input at 0 V	–0.8	-0.5		
		V_I = -7 V, V_{CC} = 0 V,	Other input at 0 V	–0.8	–0.5		
I_{CC}	Supply current	Driver disabled	Outputs enabled			5	mA
			Outputs disabled			3	

6.6.2 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = –1.5 V to 1.5 V, See 図 7-6	11	22	33	ns
t_{PLH}	Propagation delay time, low- to high-level output		11	22	33	ns
$t_{sk(p)}$	Pulse skew (| t_{PHL} – t_{PLH}|)			3	6	ns
t_t	Transition time			5	8	ns
t_{PZH}	Output enable time to high level	See 図 7-7			35	ns
t_{PZL}	Output enable time to low level				30	ns
t_{PHZ}	Output disable time from high level				35	ns
t_{PLZ}	Output disable time from low level				30	ns

6.6.3 Switching Characteristics: SN55LBC180

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = –1.5 V to 1.5 V, See 図 7-6		26		ns
t_{PLH}	Propagation delay time, low- to high-level output			23		ns
$t_{sk(p)}$	Pulse skew (| t_{PHL} – t_{PLH}|)			3		ns
$t_{sk(p)t}$	Transition time			4		ns
t_{PZH}	Output enable time to high level	See 図 7-4		30		ns
t_{PHZ}	Output disable time from high level			26		ns
t_{PZL}	Output enable time to low level			30		ns
t_{PLZ}	Output disable time from low level			30		ns

6.7 Typical Characteristics

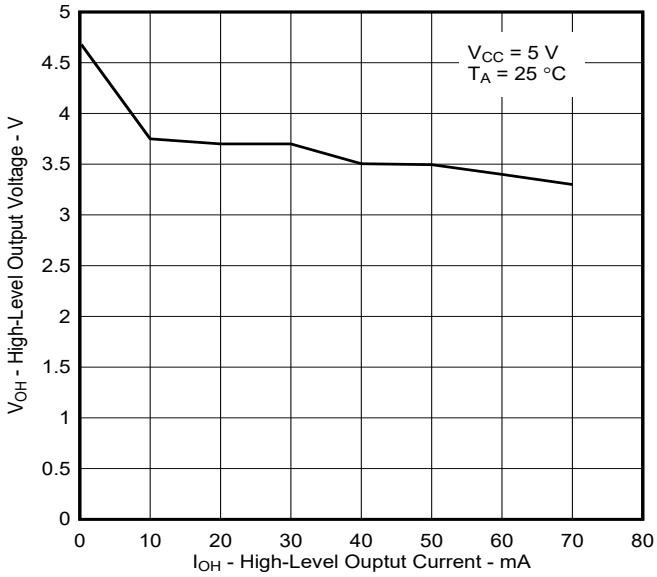


図 6-1. Driver High-Level Output Voltage vs High-Level Output Current

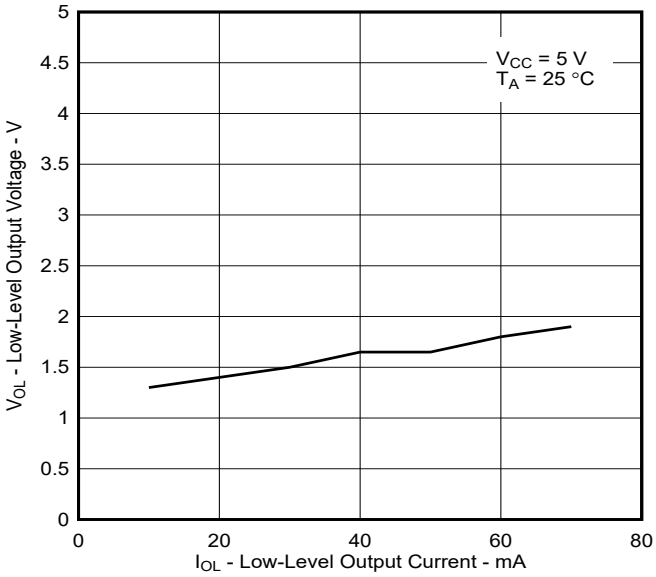


図 6-2. Driver Low-Level Output Voltage vs Low-Level Output Current

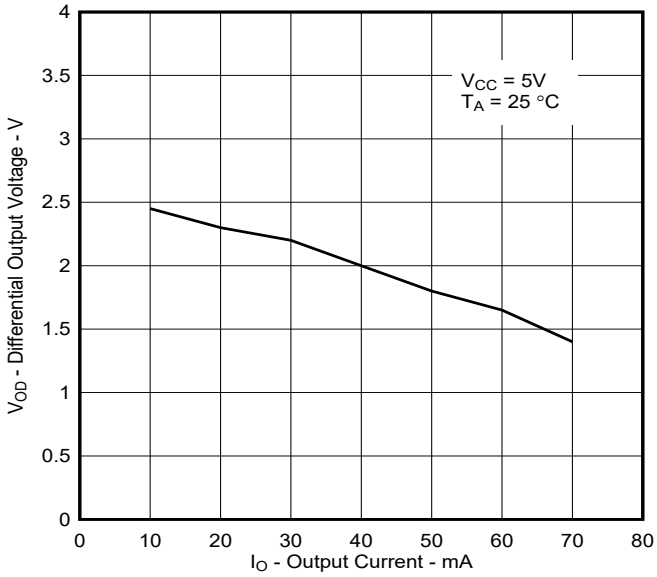


図 6-3. Driver Differential Output Voltage vs Output Current

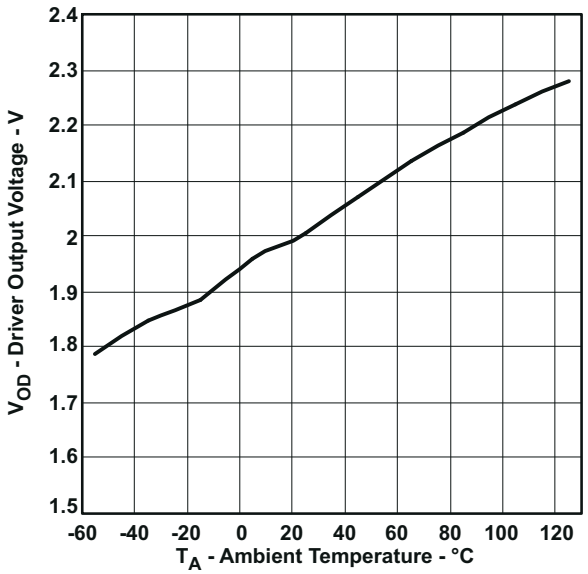


図 6-4. Driver Differential Output Voltage vs Free-Air Temperature

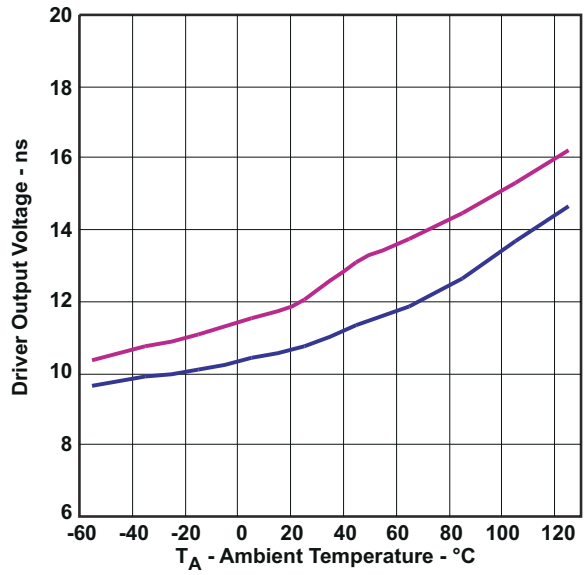


図 6-5. Driver Differential Delay Times vs Free-Air Temperature

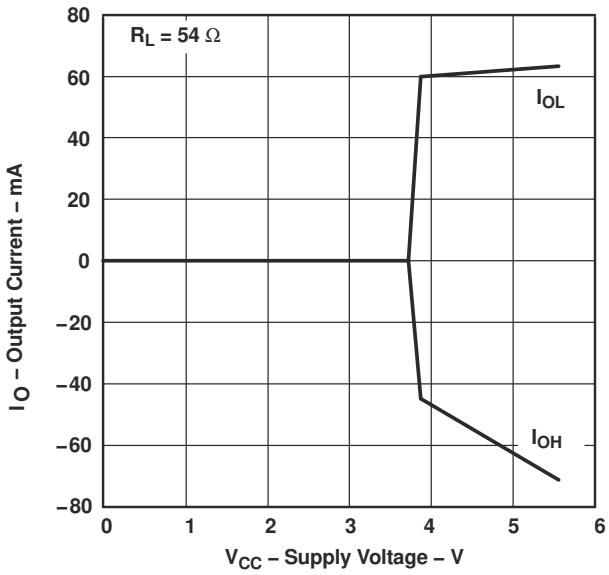


図 6-6. Driver Output Current vs Supply Voltage

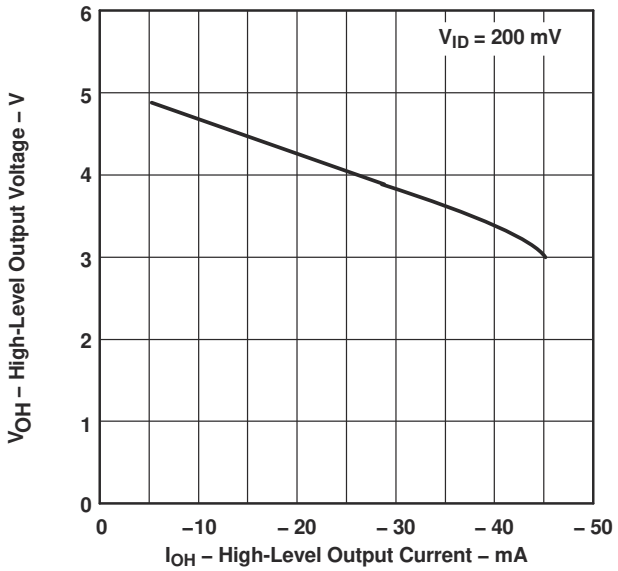


図 6-7. Receiver High-Level Output Voltage vs High-Level Output Current

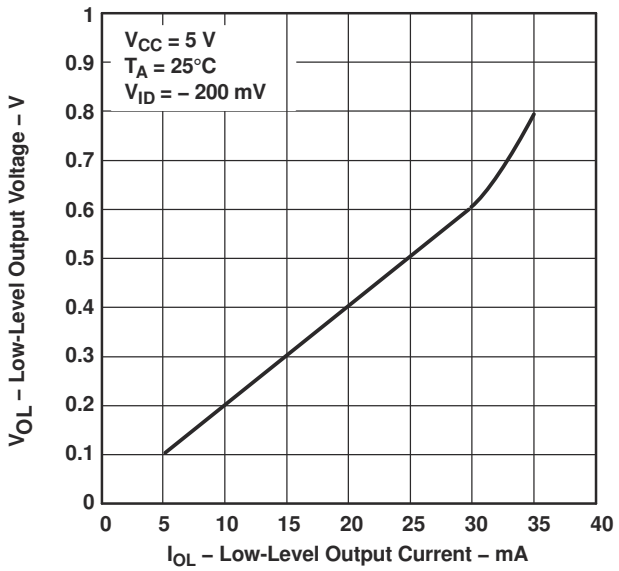


図 6-8. Receiver Low-Level Output Voltage vs Low-Level Output Current

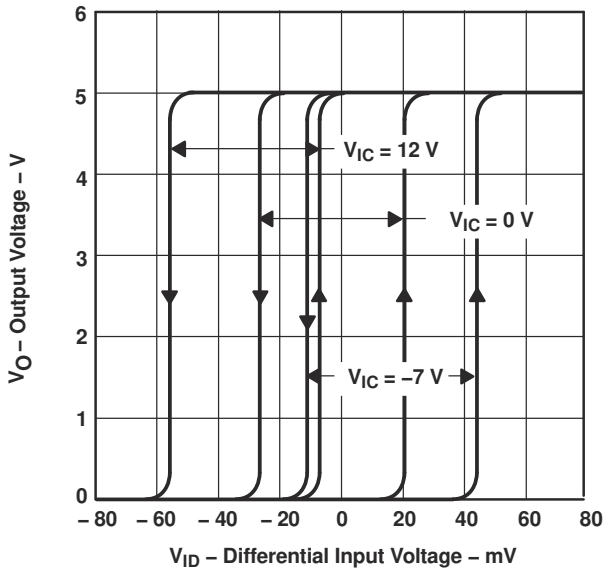


図 6-9. Receiver Output Voltage vs Differential Input Voltage

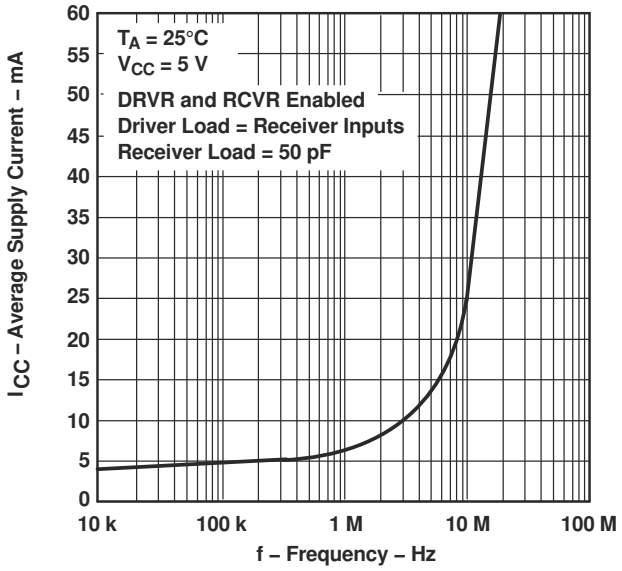


図 6-10. Average Supply Current vs Frequency

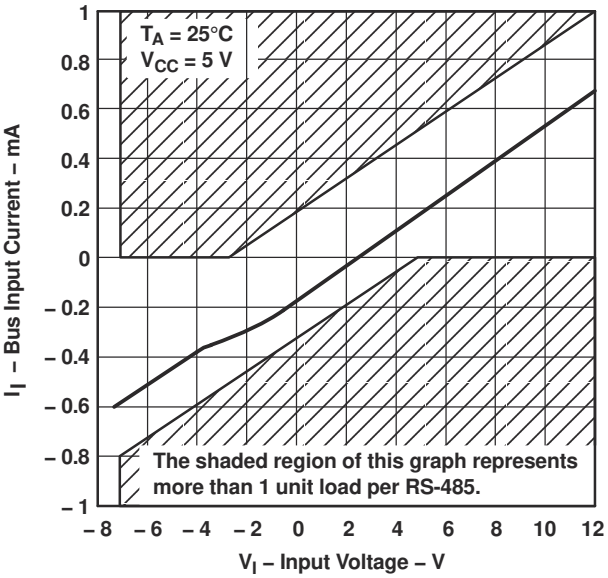


図 6-11. Receiver Bus Input Current vs Input Voltage (Complementary Input at 0 V)

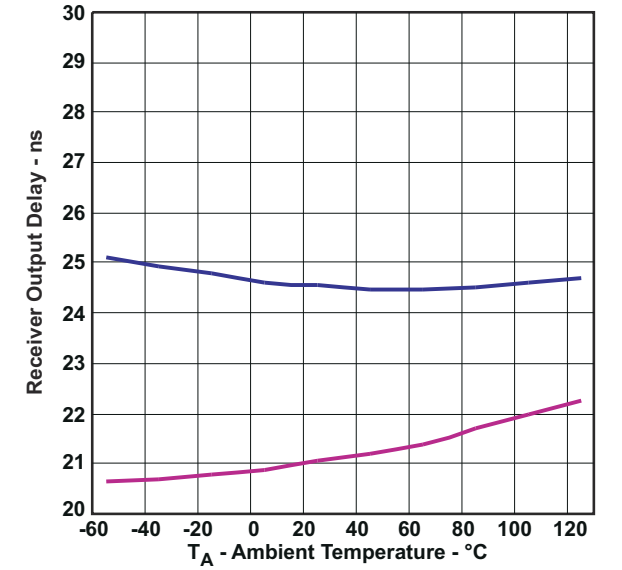


図 6-12. Receiver Propagation DELAY TI vs Free-Air Temperature

7 Parameter Measurement Information

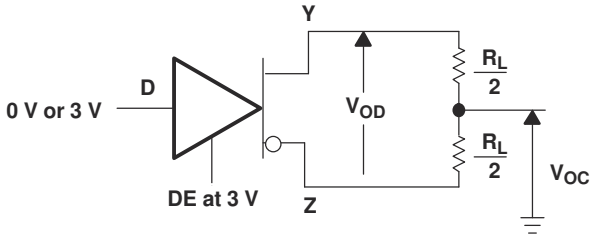


図 7-1. Differential and Common-Mode Output Voltages

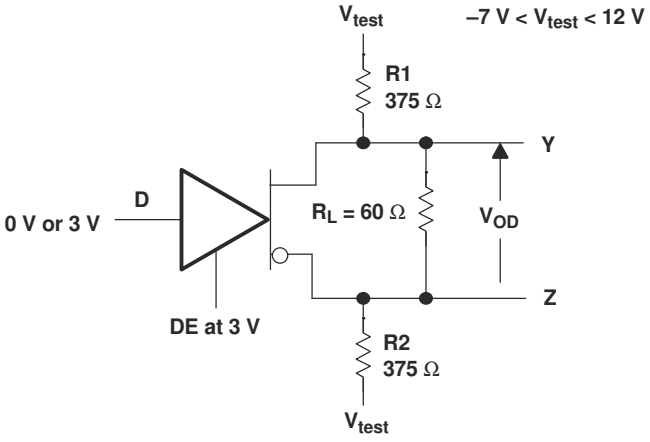
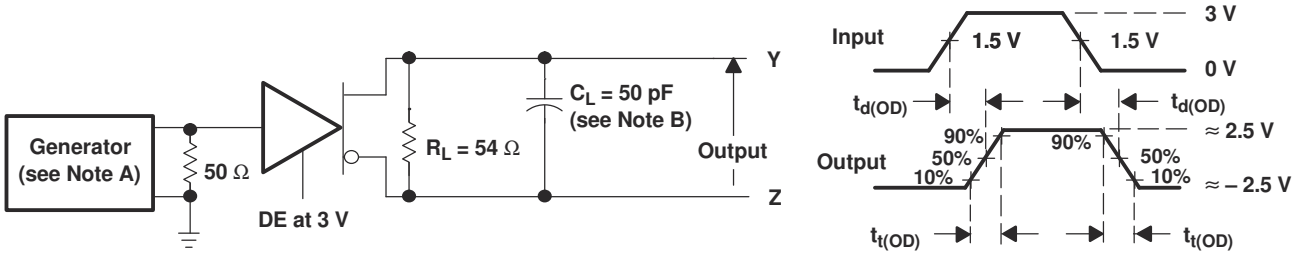


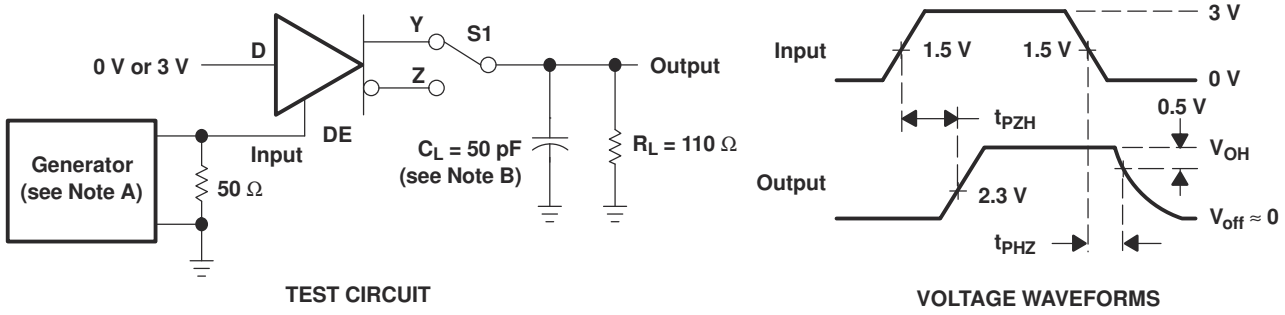
図 7-2. Driver V_{OD} Test Circuit



TEST CIRCUIT VOLTAGE WAVEFORMS

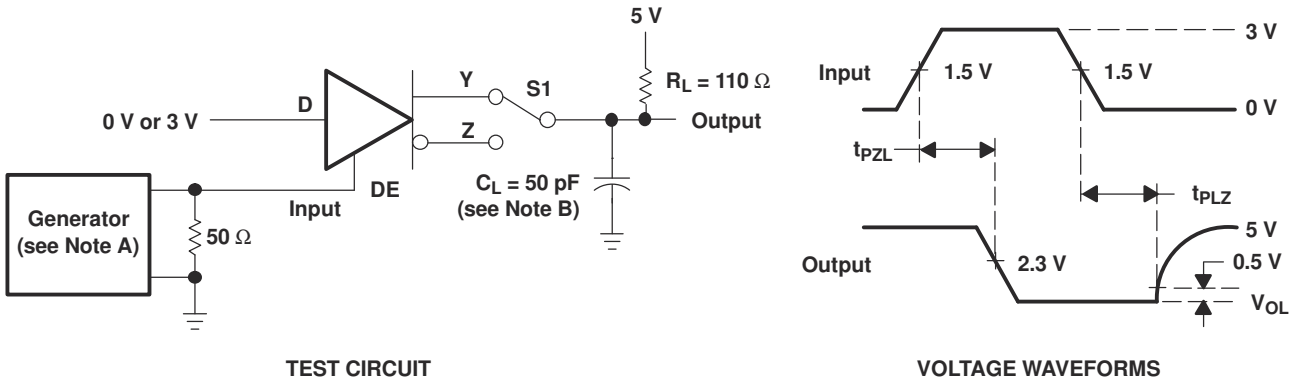
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR > 1 MHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

図 7-3. Driver Test Circuit and Differential Output Delay and Transition Time Voltage Waveforms



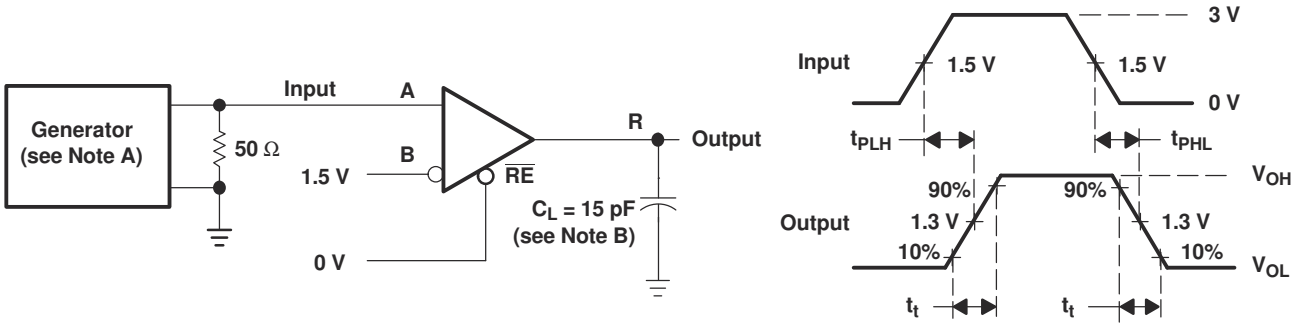
TEST CIRCUIT VOLTAGE WAVEFORMS

図 7-4. Driver Test Circuit and Enable and Disable Time Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

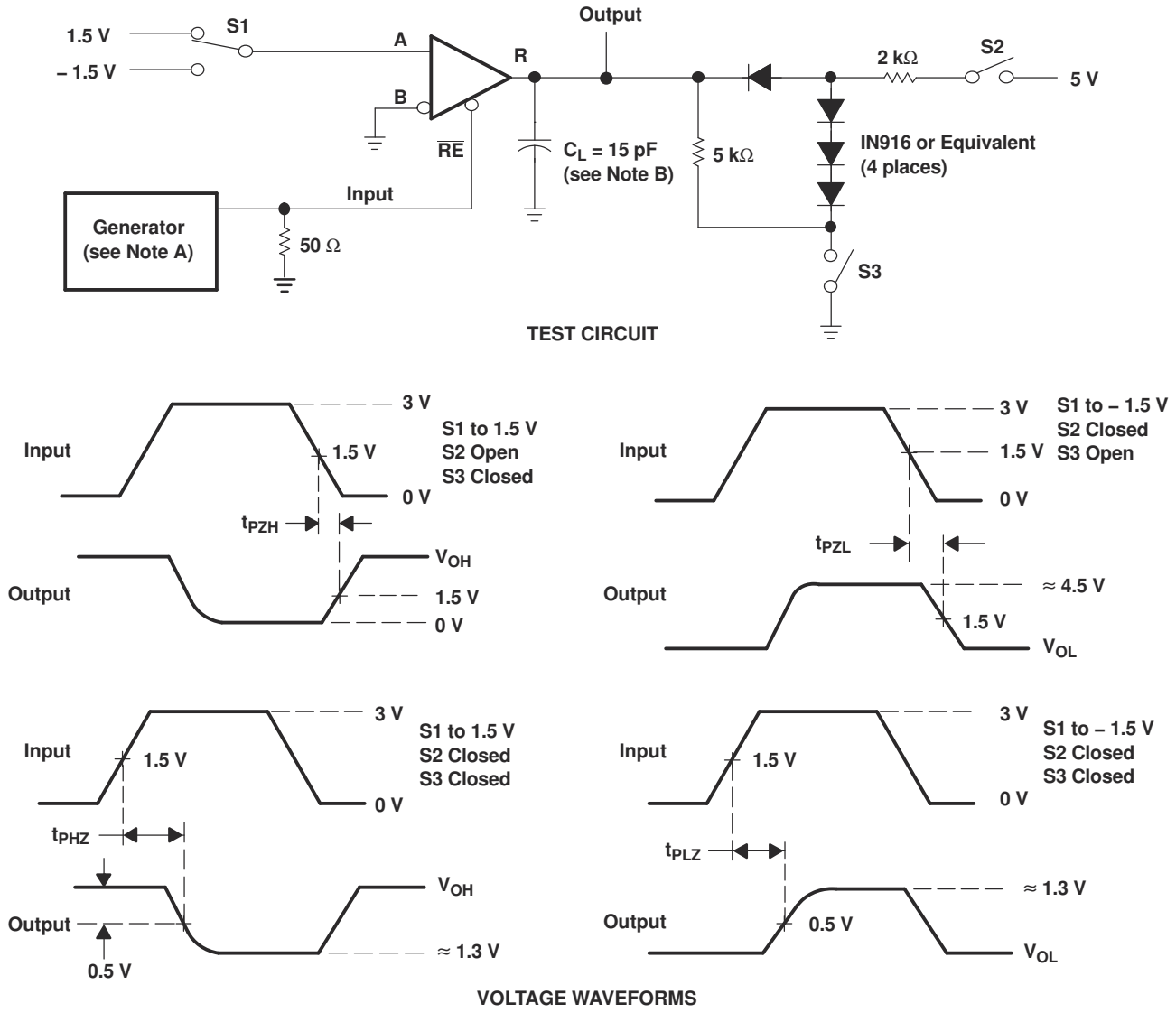
図 7-5. Driver Test Circuit and Enable and Disable Time Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

図 7-6. Receiver Test Circuit and Propagation Delay Time Voltage Waveforms



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

図 7-7. Receiver Output Enable and Disable Times

8 Detailed Description

8.1 Function Tables

表 8-1. DRIVER

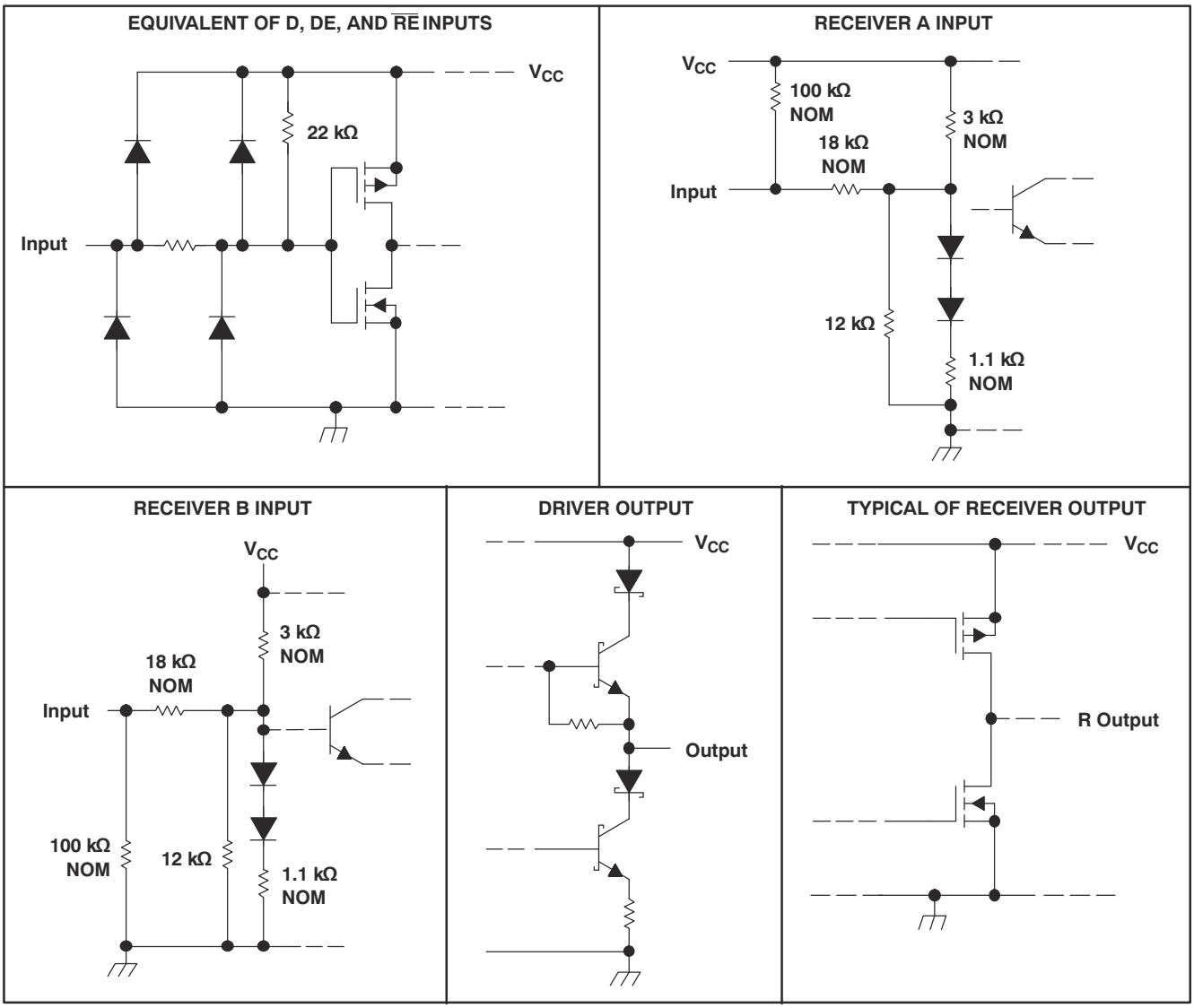
INPUT D[(1)]	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, ? = Indeterminate, X = irrelevant, Z = high impedance (off)

表 8-2. RECEIVER

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R	
		Y	Z
$V_{ID} \geq 0.2$ V	L	H	
–0.2 V < V_{ID} < 0.2 V	L	?	
$V_{ID} \leq$ –0.2 V	L	L	
X	H	Z	
Open circuit	L	H	

8.2 Schematics of Inputs and Outputs



9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

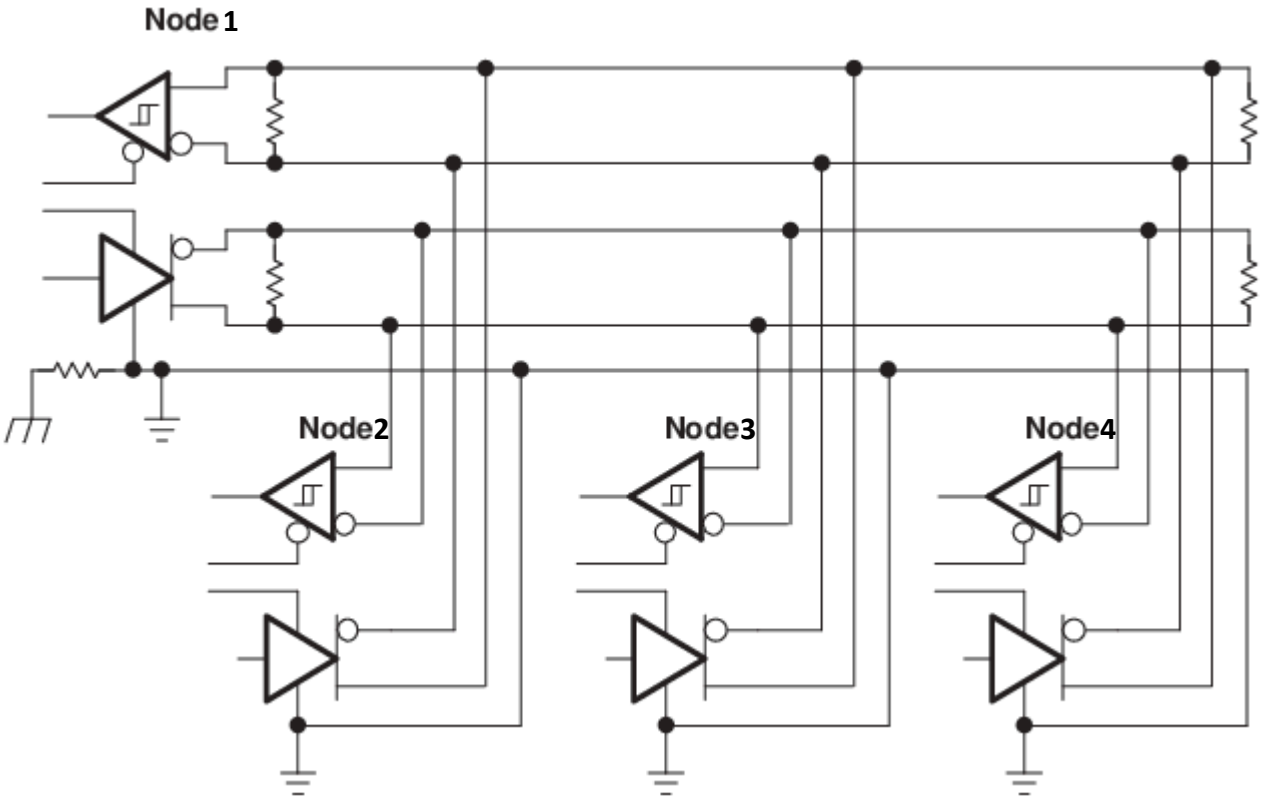


図 9-1. Full Duplex Application Circuit

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

10.3 商標

LinBiCMOS™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN55LBC180RSAR	Active	Production	QFN (RSA) | 16	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-55 to 125	SN55 LBC180
SN55LBC180RSAR.A	Active	Production	QFN (RSA) | 16	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-55 to 125	SN55 LBC180
SN55LBC180RSARG4	Active	Production	QFN (RSA) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	SN55 LBC180
SN55LBC180RSARG4.A	Active	Production	QFN (RSA) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	SN55 LBC180
SN65LBC180DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB180
SN65LBC180DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB180
SN65LBC180DRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB180
SN65LBC180N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN65LBC180N
SN65LBC180N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN65LBC180N
SN65LBC180RSAR	Active	Production	QFN (RSA) | 16	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	BL180
SN65LBC180RSAR.A	Active	Production	QFN (RSA) | 16	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	BL180
SN75LBC180N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75LBC180N
SN75LBC180N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75LBC180N
SN75LBC180RSAT	Obsolete	Production	QFN (RSA) | 16	-	-	Call TI	Call TI	0 to 70	LB180

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN55LBC180, SN75LBC180 :

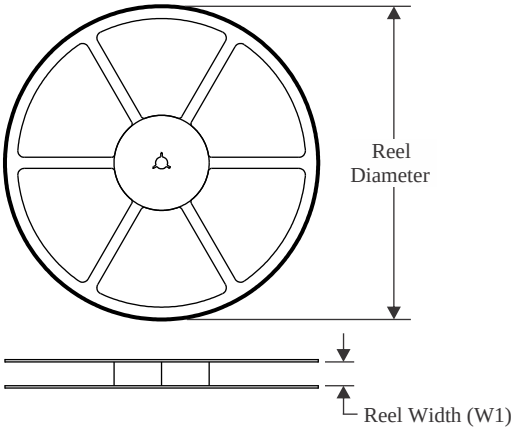
- Catalog : SN75LBC180
- Military : SN55LBC180

NOTE: Qualified Version Definitions:

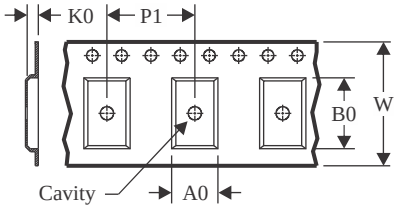
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

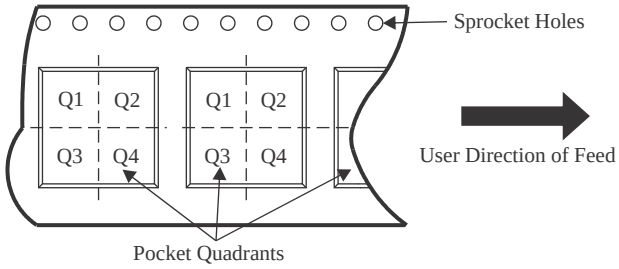


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

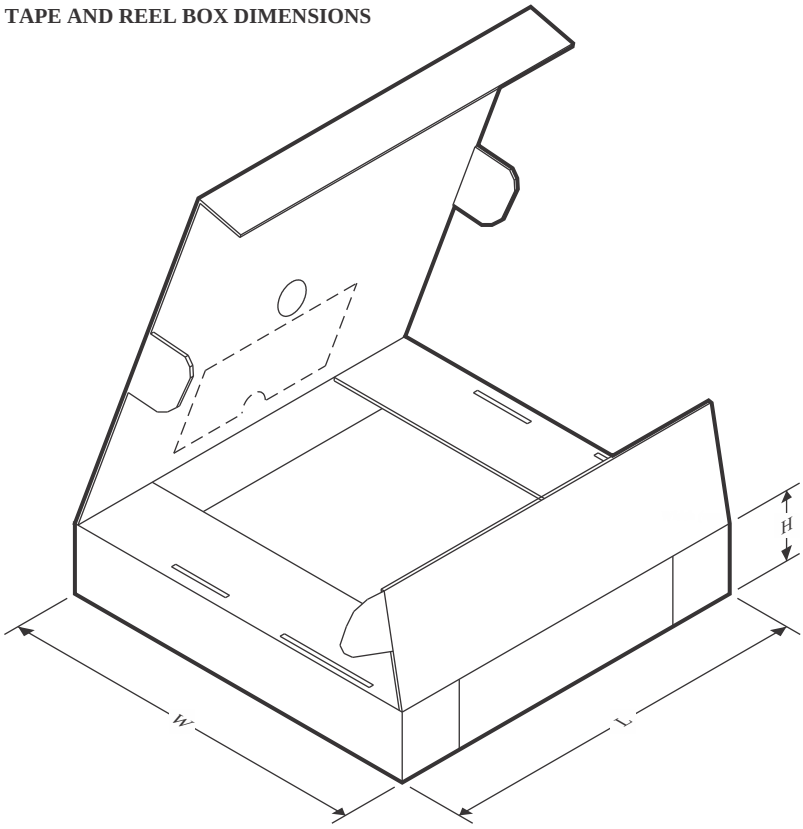
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN55LBC180RSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN55LBC180RSARG4	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN65LBC180DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65LBC180RSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

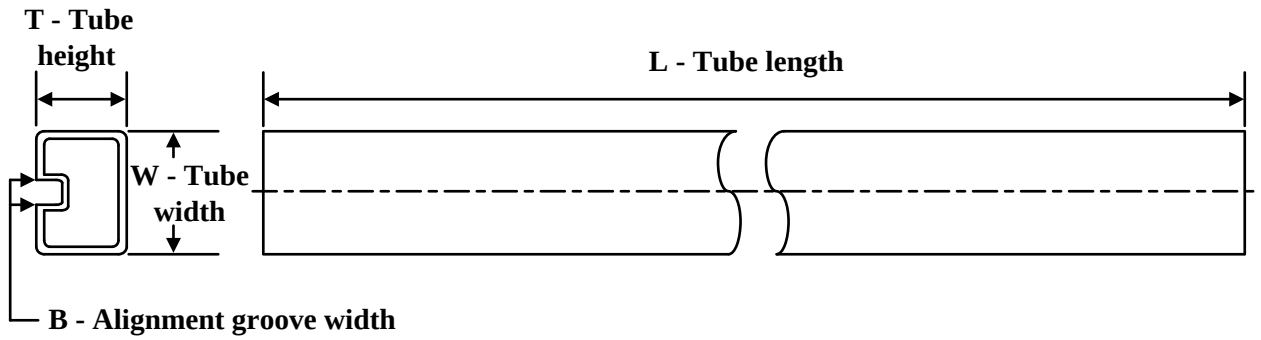
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

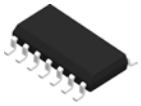
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN55LBC180RSAR	QFN	RSA	16	3000	367.0	367.0	35.0
SN55LBC180RSARG4	QFN	RSA	16	3000	367.0	367.0	35.0
SN65LBC180DR	SOIC	D	14	2500	340.5	336.1	32.0
SN65LBC180RSAR	QFN	RSA	16	3000	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LBC180N	N	PDIP	14	25	506	13.97	11230	4.32
SN65LBC180N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN75LBC180N	N	PDIP	14	25	506	13.97	11230	4.32
SN75LBC180N.A	N	PDIP	14	25	506	13.97	11230	4.32

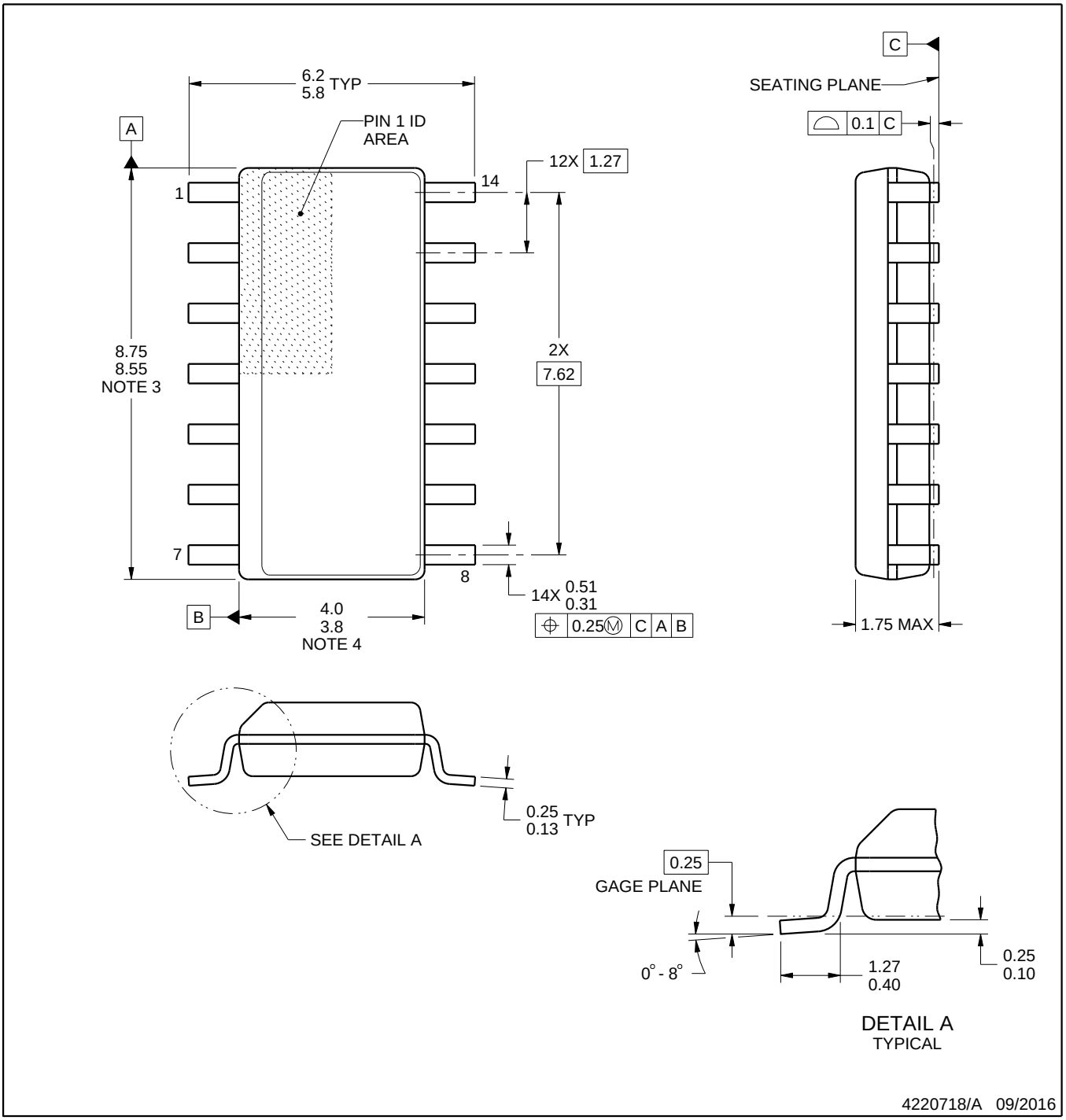


PACKAGE OUTLINE

D0014A

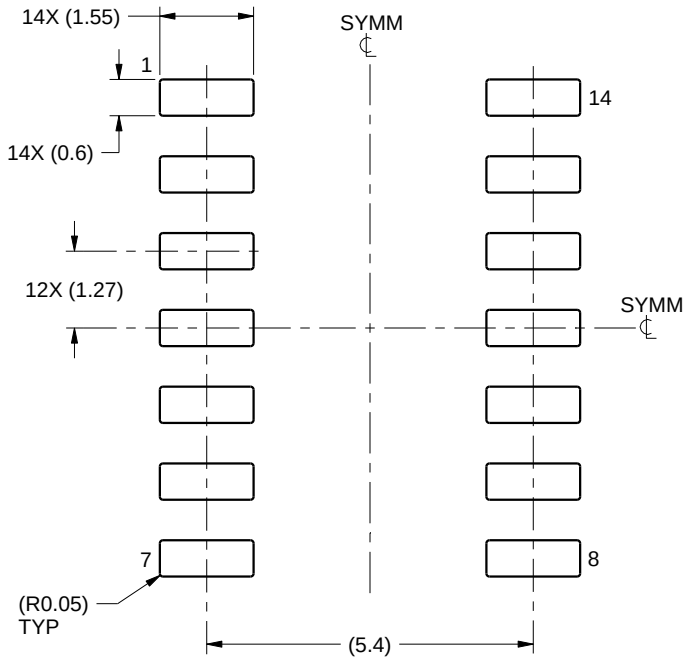
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

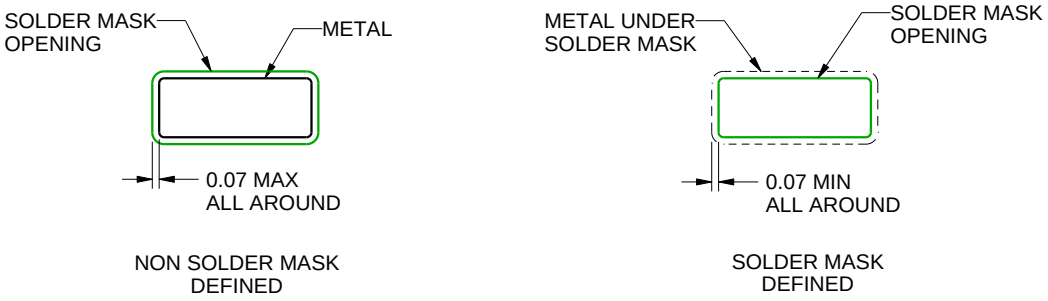


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

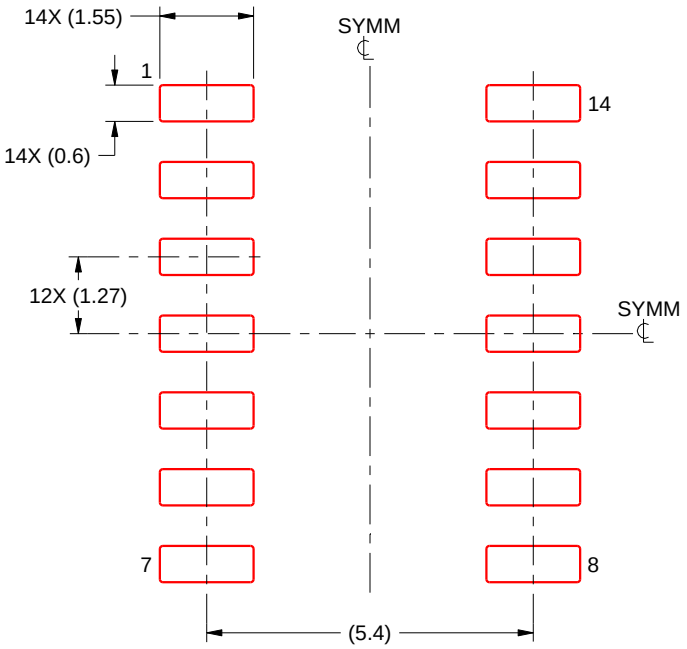
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

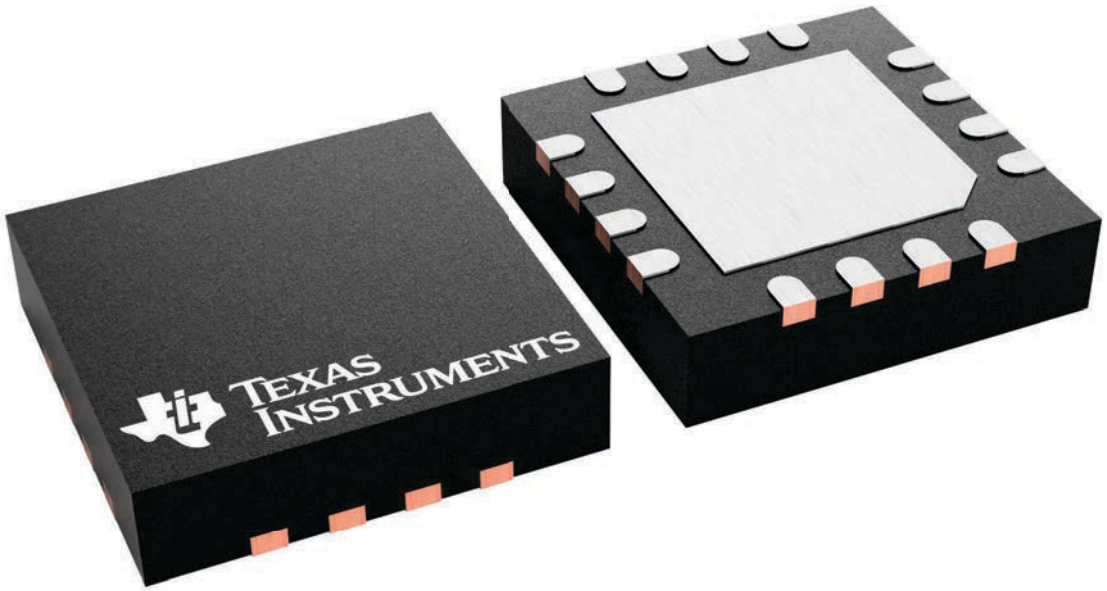
RSA 16

VQFN - 1 mm max height

4 x 4, 0.65 mm pitch

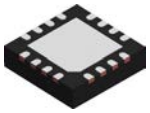
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4230969/A

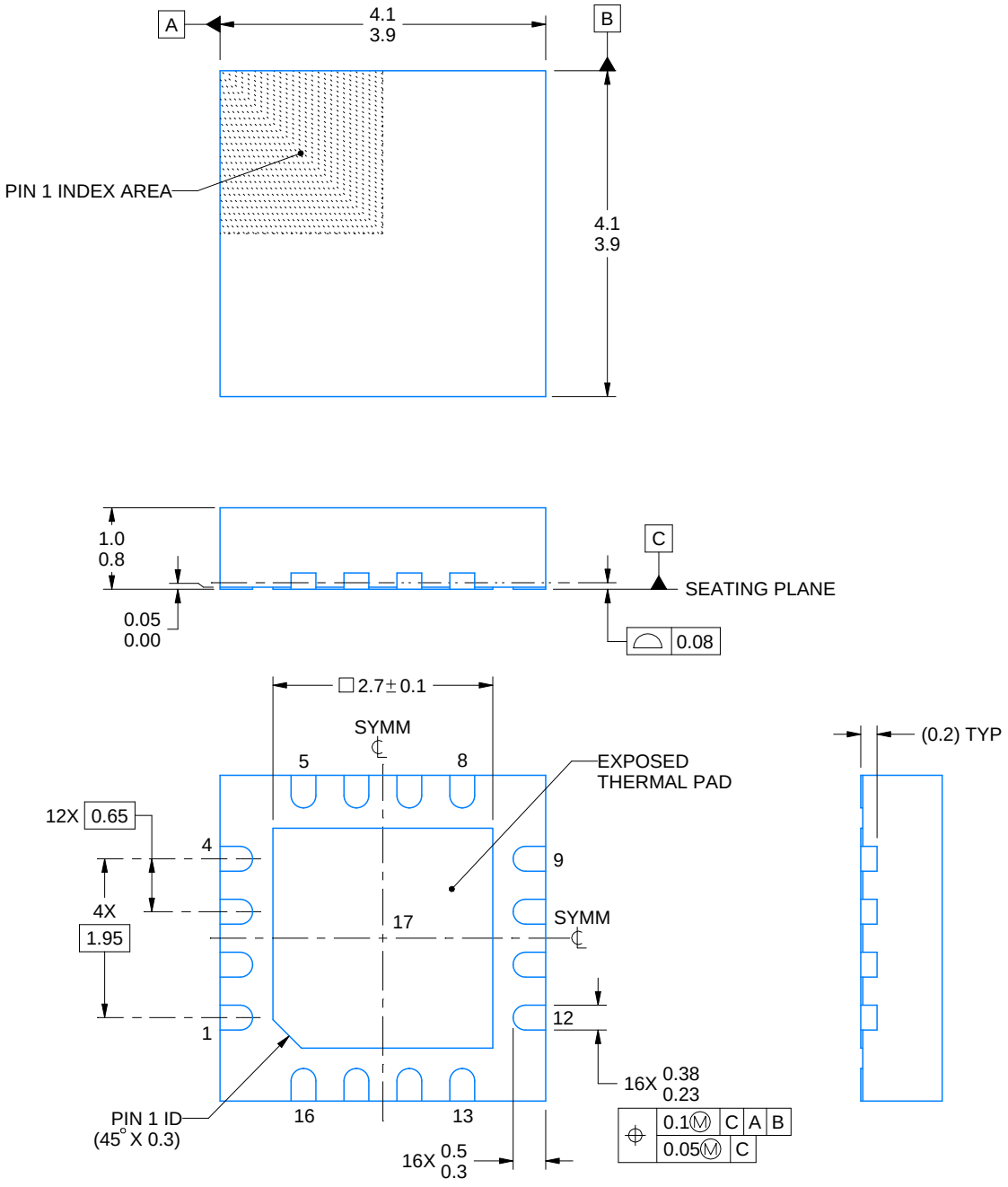
RSA0016B



PACKAGE OUTLINE

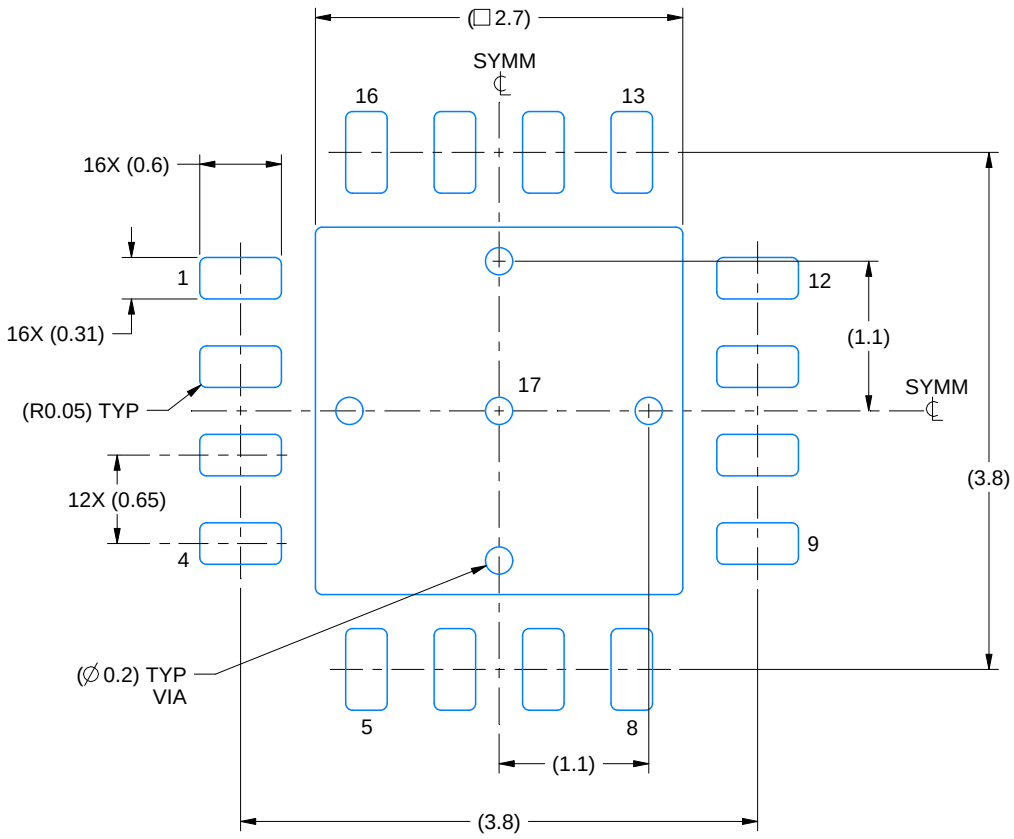
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

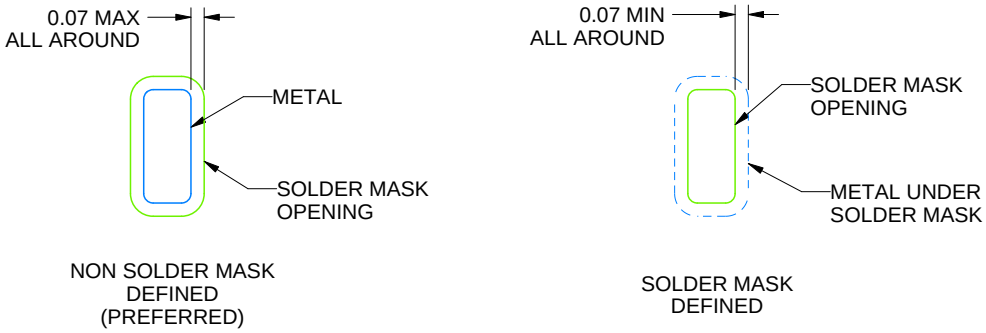


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

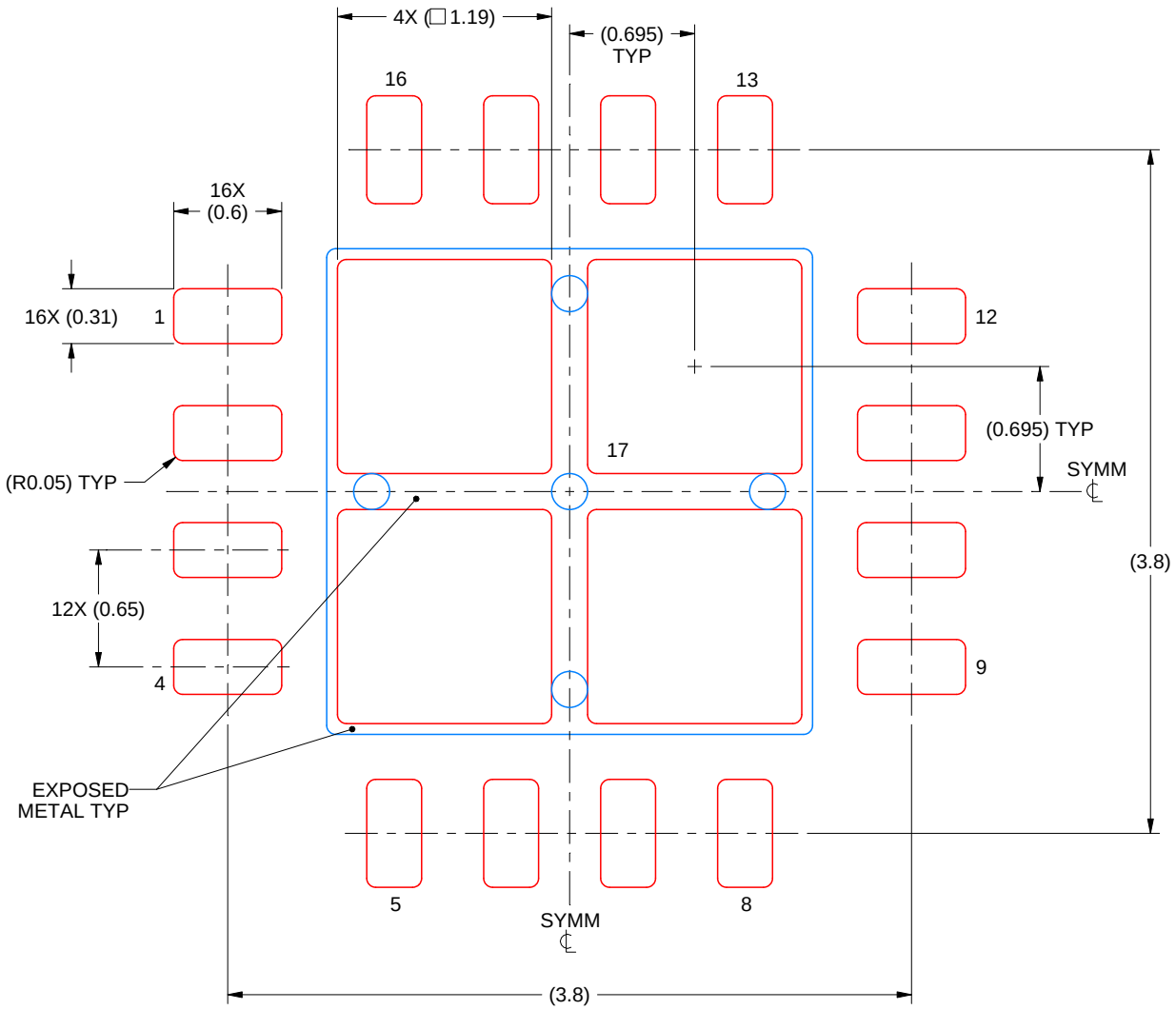


SOLDER MASK DETAILS

4219093/A 08/2021

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4219093/A 08/2021

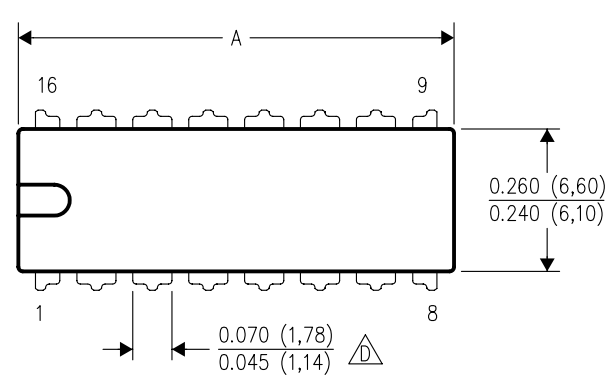
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

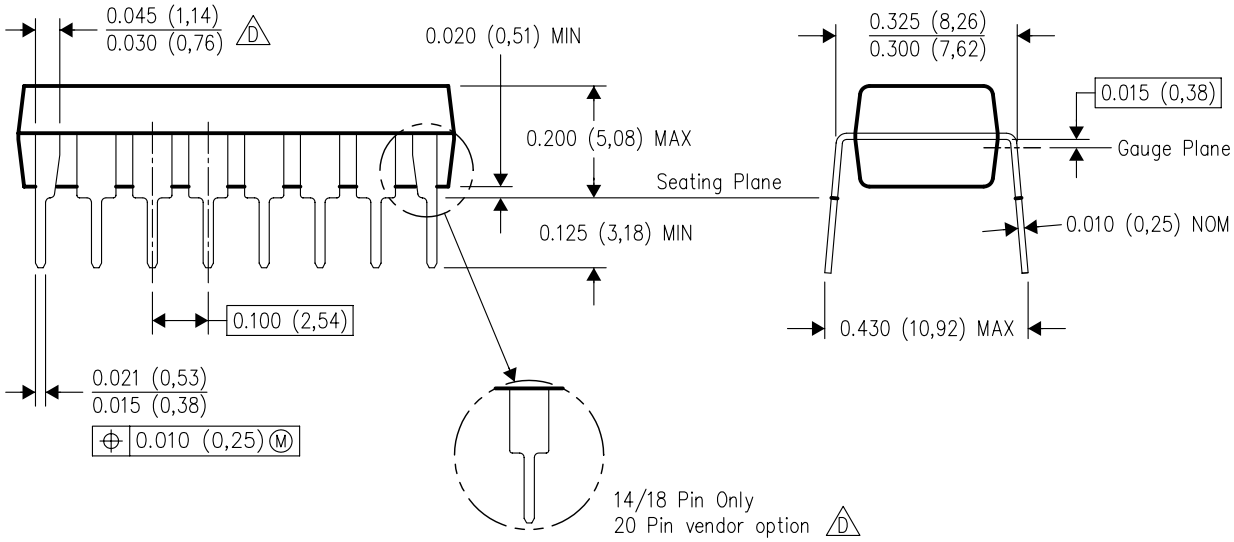
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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最終更新日：2025 年 10 月