TEXAS INSTRUMENTS
SN65LVDS301
JAJSQ88E – FEBRUARY 2006 – REVISED OCTOBER 2020

SN65LVDS301 プログラマブル 27 ビット・パラレル / シリアル・トランスミッタ

1 特長

- FlatLink™3G シリアル・インターフェイス・テクノロジー
- SN65LVDS302 などの FlatLink3G レシーバと互換性あり
- 入力は 24 ビット RGB ビデオ・モード・インターフェイスをサポート
- 24 ビット RGB データ、3 つの制御ビット、1 つのパリティ・ビット、および 1、2、または 3 つの差動ライン上で送信される 2 つの予約ビット
- SubLVDS 差動電圧レベル
- 最大 1755Mbps の実効データ・スループット
- 消費電力を節約するための 3 つの動作モード
  - アクティブ・モード QVGA 17.4mW (標準値)
  - アクティブ・モード VGA 28.8mW (標準値)
  - シャットダウン・モード 0.5µA (標準値)
  - スタンバイ・モード 0.5µA (標準値)
- バス・スワップにより PCB レイアウトの柔軟性を向上
- 1.8V の電源電圧
- ESD 定格 > 2kV (HBM)
- 4MHz～65MHz のピクセル・クロック範囲
- すべての CMOS 入力でのフェイルセーフ
- パッケージ:80 ピン、5mm × 5mm nFBGA®
- 非常に低い EMI は SAE J1752/3「M」仕様に適合

2 アプリケーション

- ウェアラブル (非医療用)
- タブレット
- 携帯電話 / スマートフォン
- 携帯電子機器
- ゲーム
- リテール・オートメーションおよびペイメント
- ビルディング・オートメーション

3 概要

SN65LVDS301 シリアライザ・デバイスは、27 のパラレル・データ入力を 1、2、または 3 つの SubLVDS (Sub-Low-Voltage Differential Signaling) シリアル出力に変換します。パラレル CMOS 入力インターフェイスから、24 のピクセル・ビットと 3 つの制御ビットを持つシフト・レジスタをロードします。27 のデータ・ビットに加えて、パリティ・ビットと 2 つの予約ビットが 30 ビットのデータ・ワードに追加されます。各ワードは、ピクセル・クロック (PCLK) によってデバイスにラッチされます。パリティ・ビット (奇数パリティ) により、レシーバはシングル・ビット・エラーを検出できます。シリアル・シフト・レジスタは、使用するシリアル・リンクの数に応じて、ピクセル・クロックのデータ・レートの 30 倍、15 倍、または 10 倍でアップロードされます。ピクセル・クロックのコピーは、別の差動出力に出力されます。

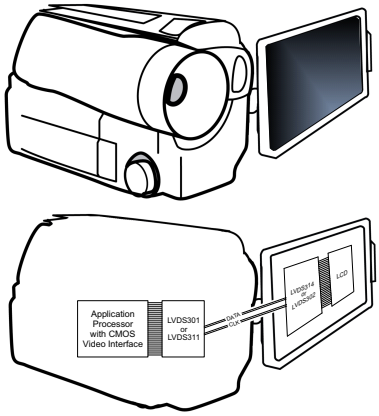
通常、FPC ケーブルは SN65LVDS301 とディスプレイを相互接続します。パラレル信号と比較して、LVDS301 の出力は相互接続の EMI を 20dB 以上大幅に低減します。デバイス自体の電磁放射は非常に低く、SAE J1752/3「M」仕様に適合しています。(図 6-22 を参照)

SN65LVDS301 は、-40℃～85℃の周囲温度での動作を特徴としています。すべての CMOS 入力にはフェイルセーフ機能があり、電源投入時の損傷から保護し、電源投入時にデバイス入力へ電流が流れるのを防ぎます。V_{DD} が 0V～1.65V であれば、すべての CMOS 入力に最大 2.165V の入力電圧を印加できます。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
SN65LVDS301	nFBGA (80)	5.00mm × 5.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 5
6.1 Absolute Maximum Ratings(1) ... 5
6.2 Thermal Information ... 5
6.3 Recommended Operating Conditions(1) ... 6
6.4 Device Electrical Characteristics ... 7
6.5 Output Electrical Characteristics ... 7
6.6 Input Electrical Characteristics ... 8
6.7 Switching Characteristics ... 8
6.8 Timing Characteristics ... 9
6.9 Device Power Dissipation ... 9
6.10 Typical characteristics ... 10
7 Parameter Measurement Information ... 14
8 Detailed Description ... 22
8.1 Overview ... 22
8.2 Functional Block Diagram ... 23
8.3 Feature Description ... 23
8.4 Device Functional Modes ... 25
9 Application information ... 30
9.1 Application Information ... 30
9.2 Preventing Increased Leakage Currents in Control Inputs ... 30
9.3 VGA Application ... 30
9.4 Dual LCD-Display Application ... 31
9.5 Typical Application Frequencies ... 31
10 Power Supply Design Recommendation ... 33
10.1 Decoupling Recommendation ... 33
11 Layout ... 34
11.1 Layout Guidelines ... 34
12 Device and Documentation Support ... 35
12.1 サポート・リソース ... 35
12.2 Trademarks ... 35
12.3 静電気放電に関する注意事項 ... 35
12.4 用語集 ... 35
13 Mechanical, Packaging, and Orderable Information ... 36

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (August 2012) to Revision E (October 2020)	Page

- 注：MicroStar Jr. BGA パッケージのデバイスは、ラミネート nFBGA パッケージを使用して再設計されています。この nFBGA パッケージは、データシート上、同等の電気的性能を実現します。また、MicroStar Jr. BGA と同等のフットプリントを実現しています。生産中止となったパッケージ識別子に代わる新しいパッケージ識別子が、データシート全体を通して更新されます。 ... 1
- u*jr ZQE を nFBGA ZXH に変更 ... 1
- Changed u*jr ZQE to nFBGA ZXH ... 3
- Changed u*jr ZQE to nFBGA ZXH, updated thermal information ... 5
- Added overview ... 22

Copyright © 2023 Texas Instruments Incorporated

5 Pin Configuration and Functions

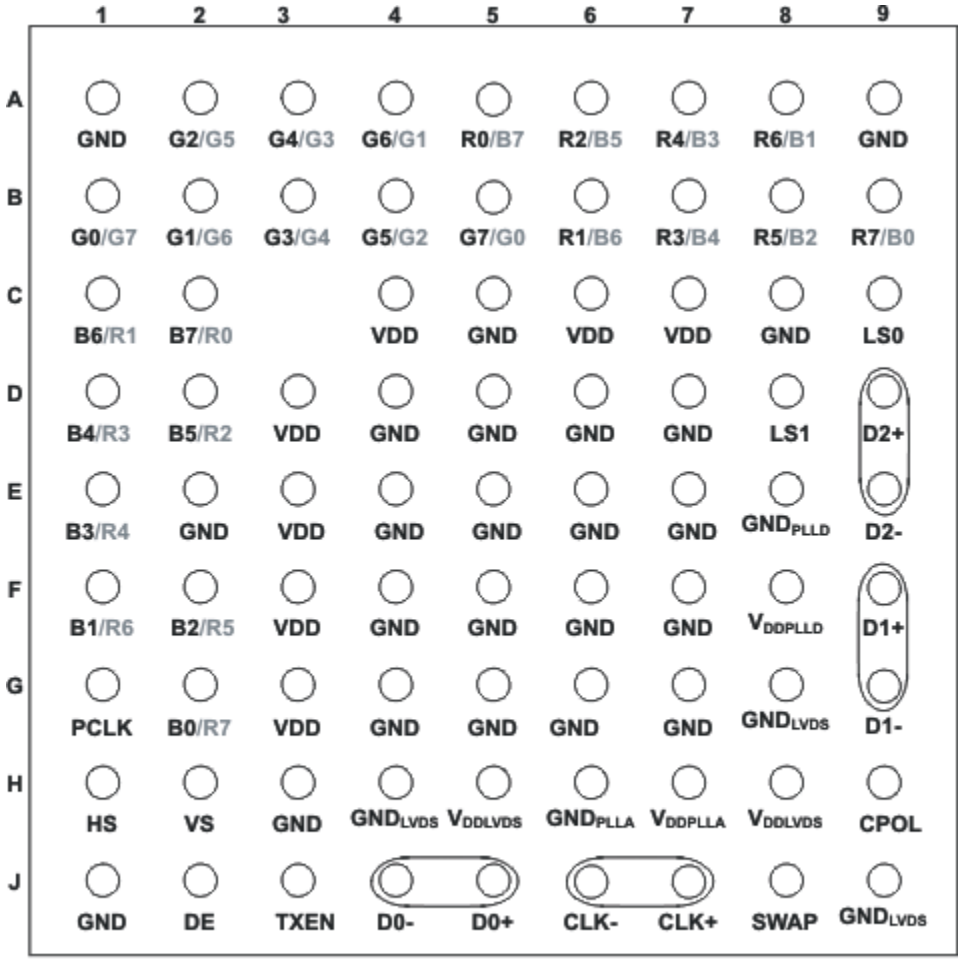


図 5-1. 80-Ball ZXH (Top View)

Pin Functions

NAME	PIN	I/O	DESCRIPTION
D0+, D0–	J5, J4	SubLVDS Out	SubLVDS Data Link (active during normal operation)
D1+, D1–	F9, G9		SubLVDS Data Link (active during normal operation when LS0 = high and LS1 = low, or LS0 = low and LS1=high; high impedance if LS0 = LS1 = low)
D2+, D2–	D9, E9		SubLVDS Data Link (active during normal operation when LS0 = low and LS1 = high, high-impedance when LS1 = low)
CLK+, CLK–	J7, J6		SubLVDS output Clock; clock polarity is fixed

Copyright © 2023 Texas Instruments Incorporated

Pin Functions (continued)

NAME	PIN	I/O	DESCRIPTION
R0–R7	A5/C2, B6/C1, A6/D2, B7/D1, A7/E1, B8/F2, A8/F1, B9/G2	CMOS IN	Red Pixel Data (8); pin assignment depends on SWAP pin setting
G0–G7	B1/B5, B2/A4, A2/B4, B3/A3, A3/B3, B4/A2, A4/B2, B5/B1		Green Pixel Data (8); pin assignment depends on SWAP pin setting
B0–B7	B9/G2, A8/F1, B8/F2, A7/E1, B7/D1, A6/D2, B6/C1, A5/C2		Blue Pixel Data (8); pin assignment depends on SWAP pin setting
HS	H1		Horizontal Sync
VS	H2		Vertical Sync
DE	J2		Data Enable
PCLK	G1		Input Pixel Clock; rising or falling clock polarity is selected by control input CPOL
LS0, LS1	C9, D8		Link Select (Determines active SubLVDS Data Links and PLL Range) See 表 8-2
TXEN	J3		Disables the CMOS Drivers and Turns Off the PLL, putting device in shutdown mode 1 – Transmitter enabled 0 – Transmitter disabled (Shutdown) Note: The TXEN input incorporates glitch-suppression logic to avoid device malfunction on short input spikes. It is necessary to pull TXEN high for longer than 10 µs to enable the transmitter. It is necessary to pull the TXEN input low for longer than 10 µs to disable the transmitter. At power up, the transmitter is enabled immediately if TXEN = 1 and disabled if TXEN = 0
CPOL	H9	CMOS In	Input Clock Polarity Selection 0 – rising edge clocking 1 – falling edge clocking
SWAP	J8	CMOS In	Bus Swap swaps the bus pins to allow device placement on top or bottom of pcb. See pinout drawing for pin assignments. 0 – data input from B0...R7 1 – data input from R7...B0
V_{DD}	C4	Power Supply(1)	Supply Voltage
GND	A1, A9, C5, C8, D4, D5, D6, D7, E2, E4, E5, E6, E7, F4, F5, F6, F7, G4, G5, G6, G7, H3, J1		Supply Ground
V_{DDLVDS}	H5, H8		SubLVDS I/O supply Voltage
GND_{LVDS}	G8, H4		SubLVDS Ground
V_{DDPLLA}	H7		PLL analog supply Voltage
GND_{PLLA}	H6		PLL analog GND
V_{DDPLLD}	F8		PLL digital supply Voltage
GND_{PLLD}	E8		PLL digital GND

(1) For a multilayer pcb, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane.

Copyright © 2023 Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply voltage range, V_{DD} (2), V_{DDPLLA}, V_{DDPLLD}, V_{DDLVDS}		-0.3 to 2.175	V
Voltage range at any input or output terminal	When V_{DDx} > 0 V	-0.5 to 2.175	V
	When V_{DDx} ≤ 0 V	-0.5 to V_{DD} + 2.175	V
Electrostatic discharge	Human Body Model(3) (all Pins)	±3	kV
	Charged-Device Mode(4)l (all Pins)	±500	V
	Machine Model(5) (all pins)	±200	
Continuous power dissipation		See Dissipation Rating Table	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminals.
(3) In accordance with JEDEC Standard 22, Test Method A114-A.
(4) In accordance with JEDEC Standard 22, Test Method C101.
(5) In accordance with JEDEC Standard 22, Test Method A115-A

6.2 Thermal Information

THERMAL METRIC(1)		SN65LVDS301 ZXH (nFBGA) 80 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Copyright © 2023 Texas Instruments Incorporated

6.3 Recommended Operating Conditions(1)

			MIN	NOM	MAX	UNIT
V_{DD} V_{DDPLLA} V_{DDPLLD} V_{DDLVDS}	Supply voltages		1.65	1.8	1.95	V
$V_{DDn(PP)}$	Supply voltage noise magnitude (all supplies)	Test set-up see 図 7-5				mV
		f(PCLK) ≤ 50 MHz; f(noise) = 1 Hz to 2 GHz			100	
		f(PCLK) > 50 MHz; f(noise) = 1 Hz to 1 MHz			100	
		f(PCLK) > 50 MHz; f(noise) > 1 MHz			40	
f_{PCLK}	Pixel clock frequency	1-Channel transmit mode, see 図 8-4	4		15	MHz
		2-Channel transmit mode, see 図 8-5	8		30	
		3-Channel transmit mode, see 図 8-6	20		65	
		Frequency threshold Standby mode to active mode(2), see 図 7-9	0.5		3	
$t_H \times f_{PCLK}$	PCLK input duty cycle		0.33		0.67	
T_A	Operating free-air temperature		–40		85	°C
$t_{jit(per)PCLK}$	PCLK RMS period jitter(3)	Measured on PCLK input			5	ps-rms
$t_{jit(TJ)PCLK}$	PCLK total jitter				$0.05/f_{PCLK}$	s
$t_{jit(CC)PCLK}$	PCLK peak cycle-to-cycle jitter(4)				$0.02/f_{PCLK}$	s
PCLK, R[0:7], G[0:7], B[0:7], VS, HS, DE, PCLK, LS[1:0], CPOL, TXEN, SWAP						
V_{IH}	High-level input voltage		$0.7\times V_{DD}$		V_{DD}	V
V_{IL}	Low-level input voltage				$0.3\times V_{DD}$	V
t_{DS}	Data set up time prior to PCLK transition	f (PCLK) = 65 MHz; see 図 7-1	2.0			ns
t_{DH}	Data hold time after PCLK transition		2.0			ns

(1) Unused single-ended inputs must be held high or low to prevent them from floating.
(2) PCLK input frequencies lower than 500 kHz force the SN65LVDS301into standby mode. Input frequencies between 500 kHz and 3 MHz may or may not activate the SN65LVDS301. Input frequencies beyond 3 MHz activate the SN65LVDS301.
(3) Period jitter is the deviation in cycle time of a signal with respect to the ideal period over a random sample of 100,000 cycles.
(4) Cycle-to-cycle jitter is the variation in cycle time of a signal between adjacent cycles; over a random sample of 1,000 adjacent cycle pairs.

Copyright © 2023 Texas Instruments Incorporated

6.4 Device Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
I_{DD}	1ChM	V_{DD} =V_{DDPLLA}=V_{DDPLLD}=V_{DDLVDS}, $R_{L(CLK)}$=$R_{L(D0)}$=100 Ω, V_{IH}=V_{DD}, V_{IL}=0 V, TXEN at V_{DD}, alternating 1010 serial bit pattern	f_{PCLK} = 4 MHz		9.0	11.4	mA
			f_{PCLK} = 6 MHz		10.6	12.6	
			f_{PCLK} = 15 MHz		16	18.8	
		V_{DD} =V_{DDPLLA}=V_{DDPLLD}=V_{DDLVDS}, $R_{L(PCLK)}$=$R_{L(D0)}$=100 Ω, V_{IH}=V_{DD}, V_{IL}=0 V, TXEN at V_{DD}, typical power test pattern (see 表 7-2)	f_{PCLK} = 4 MHz		8.0		mA
			f_{PCLK} = 6 MHz		8.9		
			f_{PCLK} = 15 MHz		14.0		
	2ChM	V_{DD} =V_{DDPLLA}=V_{DDPLLD}=V_{DDLVDS}, $R_{L(CLK)}$=$R_{L(Dx)}$=100 Ω, V_{IH}=V_{DD}, V_{IL}=0 V, TXEN at V_{DD}, alternating 1010 serial bit pattern;	f_{PCLK} = 8 MHz		13.7	15.9	mA
			f_{PCLK} = 22 MHz		18.4	22.0	
			f_{PCLK} = 30 MHz		21.4	25.8	
		V_{DD} =V_{DDPLLA}=V_{DDPLLD}=V_{DDLVDS}, $R_{L(PCLK)}$=$R_{L(D0)}$=100 Ω, V_{IH}=V_{DD}, V_{IL}=0 V, TXEN at V_{DD}, typical power test pattern (see 表 7-3)	f_{PCLK} = 8 MHz		11.5		mA
			f_{PCLK} = 22 MHz		16.0		
			f_{PCLK} = 30 MHz		19.1		
	3ChM	V_{DD} =V_{DDPLLA}=V_{DDPLLD}=V_{DDLVDS}, $R_{L(PCLK)}$=$R_{L(D0)}$=100 Ω, V_{IH}=V_{DD}, V_{IL}=0 V, TXEN at V_{DD}, alternating 1010 serial bit pattern	f_{PCLK} = 20 MHz		20.0	22.5	mA
			f_{PCLK} = 65 MHz		29.1	36.8	
		V_{DD} =V_{DDPLLA}=V_{DDPLLD}=V_{DDLVDS}, $R_{L(PCLK)}$=$R_{L(D0)}$=100 Ω, V_{IH}=V_{DD}, V_{IL}=0 V, TXEN at V_{DD}, typical power test pattern (see 表 7-4)	f_{PCLK} = 20 MHz		15.9		mA
			f_{PCLK} = 65 MHz		24.7		
	Standby Mode		V_{DD} = V_{DDPLLA} = V_{DDPLLD} = V_{DDLVDS}, $R_{L(PCLK)}$=$R_{L(D0)}$=100 Ω, V_{IH}=V_{DD}, V_{IL}=0 V, all inputs held static high or static low		0.61	10	µA
	Shutdown Mode				0.55	10	µA

(1) All typical values are at 25°C and with 1.8 V supply unless otherwise noted.

6.5 Output Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
subLVDS output (D0+, D0–, D1+, D1–, D2+, D1–, CLK+, and CLK–)						
$V_{OCM(SS)}$	Steady-state common-mode output voltage	Output load see 図 7-3	0.8	0.9	1.0	V
$V_{OCM(SS)}$	Change in steady-state common-mode output voltage		–10		10	mV
$V_{OCM(PP)}$	Peak-to-peak common mode output voltage				75	mV
$\|V_{OD}\|$	Differential output voltage magnitude $\|V_{Dx+} - V_{Dx-}\|$, $\|V_{CLK+} - V_{CLK-}\|$		100	150	200	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage between logic states		–10		10	mV
$Z_{OD(CLK)}$	Differential small-signal output impedance	TXEN at V_{DD}		210		Ω
I_{OSD}	Differential short-circuit output current	V_{OD} = 0 V, f_{PCLK} = 28 MHz			10	mA
I_{OS}	Short circuit output current(2)	V_O = 0 V or V_{DD}		5		
I_{OZ}	High-impedance state output current	V_O = 0 V or V_{DD}(max), TXEN at GND	–3		3	µA

(1) All typical values are at 25°C and with 1.8 V supply unless otherwise noted.
(2) All SN65LVDS301 outputs tolerate shorts to GND or V_{DD} without permanent device damage.

Copyright © 2023 Texas Instruments Incorporated

6.6 Input Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
PCLK, R[0:7], G[0:7], B[0:7], VS, HS, DE, PCLK, LS[1:0], CPOL, TXEN, SWAP						
I_{IH}	High-level input current	V_{IN} = 0.7 × V_{DD}	–200		200	nA
I_{IL}	Low-level input current	V_{IN} = 0.3 × V_{DD}	–200		200	
C_{IN}	Input capacitance			1.5		pF

(1) All typical values are at 25°C and with 1.8 V supply unless otherwise noted.

6.7 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_r	20%-to-80% differential output signal rise time	See 図 7-2 and 図 7-3		250		500	ps
t_f	20%-to-80% differential output signal fall time	See 図 7-2 and 図 7-3		250		500	
f_{BW}	PLL bandwidth (3dB cutoff frequency)	Tested from PCLK input to CLK output, See 図 6-1 (3)	f_{PCLK} = 22 MHz			0.082 × f_{PCLK}	MHz
			f_{PCLK} = 65 MHz			0.07 × f_{PCLK}	
$t_{pd(L)}$	Propagation delay time, input to serial output (data latency 図 7-4)	TXEN at V_{DD}, V_{IH}=V_{DD}, V_{IL}=GND, R_L=100 Ω	1-channel mode	0.8/f_{PCLK}	1/f_{PCLK}	1.2/f_{PCLK}	s
			2-channel mode	1.0/f_{PCLK}	1.21/f_{PCLK}	1.5/f_{PCLK}	
			3-channel mode	1.1/f_{PCLK}	1.31/f_{PCLK}	1.6/f_{PCLK}	
t_H × f_{CLK0}	Output CLK duty cycle		1-channel and 3-channel mode	0.45	0.50	0.55	
			2-channel mode	0.49	0.53	0.58	
t_{GS}	TXEN Glitch suppression pulse width(2)	V_{IH}=V_{DD}, V_{IL}=GND, TXEN toggles between V_{IL} and V_{IH}, see 図 7-7 and 図 7-8		3.8		10	µs
t_{pwrup}	Enable time from power down (↑ TXEN)	Time from TXEN pulled high to CLK and Dx outputs enabled and transmit valid data; see 図 7-8			0.24	2	ms
t_{pwrdn}	Disable time from active mode (↓ TXEN)	TXEN is pulled low during transmit mode; time measurement until output is disabled and PLL is Shutdown; see 図 7-8			0.5	11	µs
t_{wakup}	Enable time from Standby (↕ PCLK)	TXEN at V_{DD}; device in standby; time measurement from PCLK starts switching to CLK and Dx outputs enabled and transmit valid data; see 図 7-8			0.23	2	ms
t_{sleep}	Disable time from Active mode (PCLK stopping)	TXEN at V_{DD}; device is transmitting; time measurement from PCLK input signal stops until CLK + Dx outputs are disabled and PLL is disabled; see 図 7-8			0.4	100	µs

(1) All typical values are at 25°C and with 1.8 V supply unless otherwise noted.
(2) The TXEN input incorporates glitch-suppression circuitry to disregard short input pulses. t_{GS} is the duration of either a high-to-low or low-to-high transition that is suppressed.
(3) The Maximum Limit is based on statistical analysis of the device performance over process, voltage, and temp ranges. This parameter is functionality tested only on Automatic Test Equipment (ATE).

Copyright © 2023 Texas Instruments Incorporated

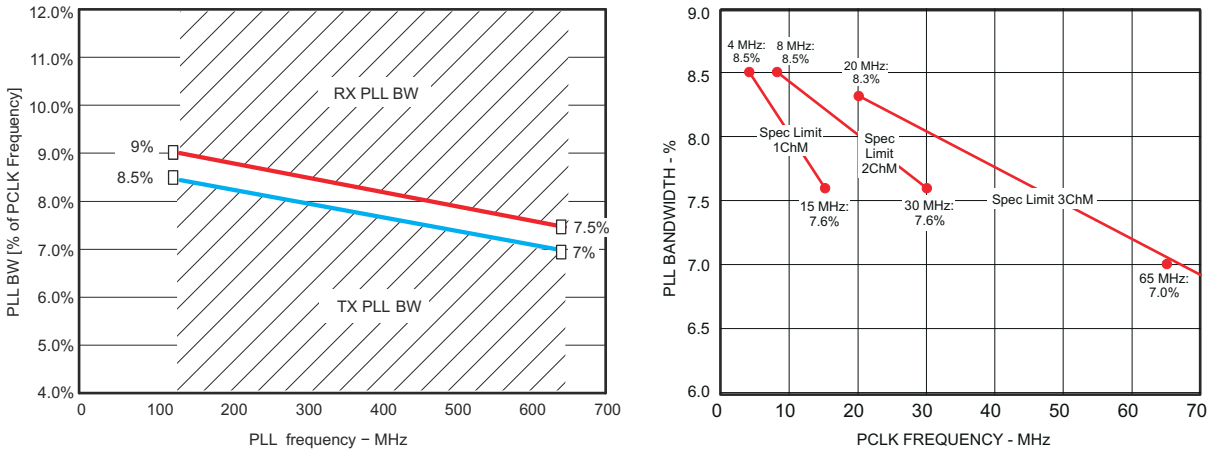


図 6-1. LVDS301 PLL Bandwidth (also showing the LVDS302 PLL bandwidth)

6.8 Timing Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PPOSX}	Output Pulse Position, ⇅serial data to ↑ CLK; see (1) (2)and 図 7-6	1ChM: x=0..29, f_{PCLK}=15 MHz; TXEN at V_{DD}, V_{IH}=V_{DD}, V_{IL}=GND, R_L=100 Ω, test pattern as in 表 7-7 (3)	$\frac{x}{30 \cdot f_{PCLK}} - 330\ ps$		$\frac{x}{30 \cdot f_{PCLK}} + 330\ ps$	ps
		1ChM: x=0..29, f_{PCLK}=4 MHz to 15 MHz (4)	$\frac{x - 0.1845}{30 \cdot f_{PCLK}}$		$\frac{x + 0.1845}{30 \cdot f_{PCLK}}$	
		2ChM: x = 0..14, f_{PCLK} = 30 MHz TXEN at V_{DD}, V_{IH}=V_{DD}, V_{IL}=GND, R_L=100 Ω, test pattern as in 表 7-8 (3)	$\frac{x}{15 \cdot f_{PCLK}} - 330\ ps$		$\frac{x}{15 \cdot f_{PCLK}} + 330\ ps$	
		2ChM: x=0..14, f_{PCLK}= 8 MHz to 30 MHz (4)	$\frac{x - 0.1845}{15 \cdot f_{PCLK}}$		$\frac{x + 0.1845}{15 \cdot f_{PCLK}}$	
		3ChM: x=0..9, f_{PCLK}=65 MHz, TXEN at V_{DD}, V_{IH}=V_{DD}, V_{IL}=GND, R_L=100 Ω, test pattern as in 表 7-9 (3)	$\frac{x}{10 \cdot f_{PCLK}} - 210\ ps$		$\frac{x}{10 \cdot f_{PCLK}} + 210\ ps$	
		3ChM: x=0..9, f_{PCLK}=20 MHz to 65 MHz (4)	$\frac{x - 0.153}{10 \cdot f_{PCLK}}$		$\frac{x + 0.153}{10 \cdot f_{PCLK}}$	

(1) This number also includes the high-frequency random and deterministic PLL clock jitter that is not traceable by the SN65LVDS302 receiver PLL; tPPosx represents the total timing uncertainty of the transmitter necessary to calculate the jitter budget when combined with the SN65LVDS302 receiver;
(2) The pulse position min/max variation is given with a bit error rate target of 10^{-12}; The measurement estimates the random jitter contribution to the total jitter contribution by multiplying the random RMS jitter by the factor 14; Measurements of the total jitter are taken over a sample amount of > 10^{-12} samples.
(3) The Minimum and Maximum Limits are based on statistical analysis of the device performance over process, voltage, and temp ranges. This parameter is functionality tested only on Automatic Test Equipment (ATE).
(4) These Minimum and Maximum Limits are simulated only.

6.9 Device Power Dissipation

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
P_D	Device Power Dissipation	V_{DDx} = 1.8 V, T_A = 25°C	f_{CLK} = 4 MHz	14.4		mW
			f_{CLK} = 65 MHz	44.5		
		V_{DDx} = 1.95 V, T_A = –40°C	f_{CLK} = 4 MHz		22.3	mW
			f_{CLK} = 65 MHz		71.8	

Copyright © 2023 Texas Instruments Incorporated

6.10 Typical characteristics

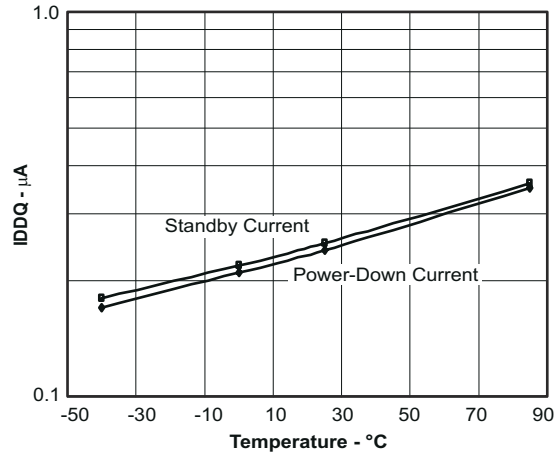


図 6-2. Powerdown, Standby Supply Current vs Temperature

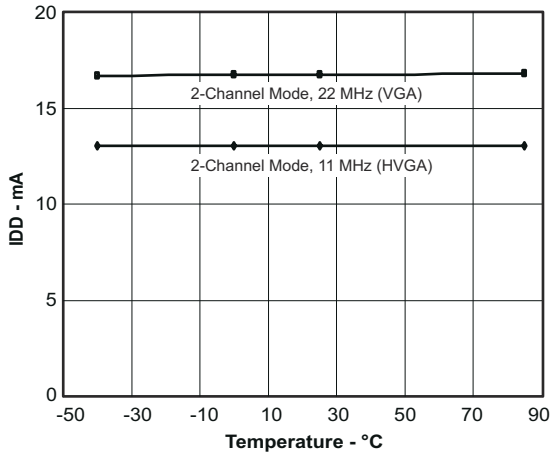


図 6-3. Supply Current I_{DD} vs Temperature

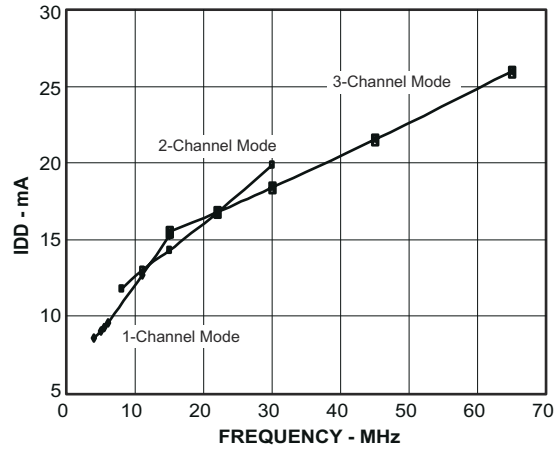


図 6-4. Supply Current vs PCLK Frequency

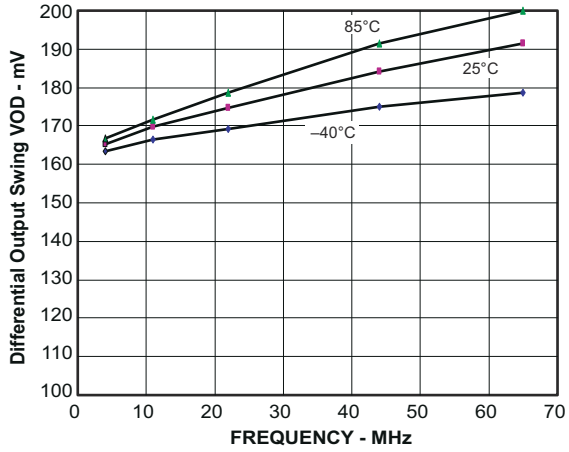


図 6-5. Differential Output Swing vs PCLK Frequency

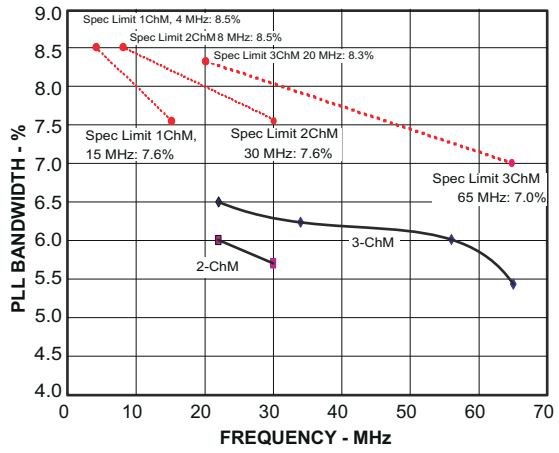


図 6-6. PLL Bandwidth

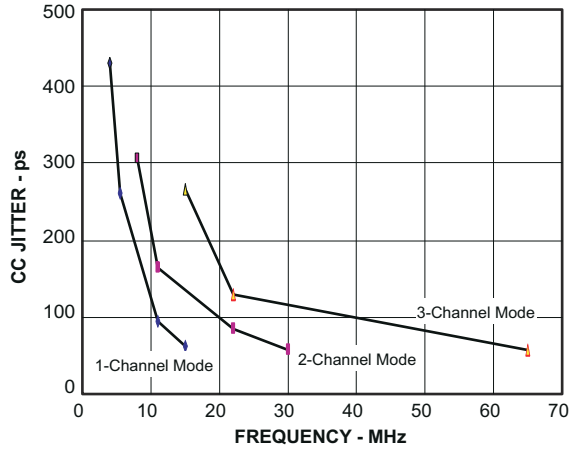


図 6-7. Cycle-to-cycle Output Jitter vs PCLK Frequency

Copyright © 2023 Texas Instruments Incorporated

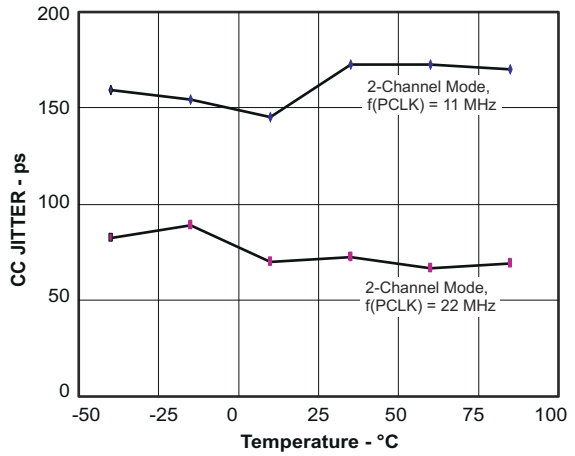


図 6-8. Cycle-to-cycle Output Jitter vs Temperature

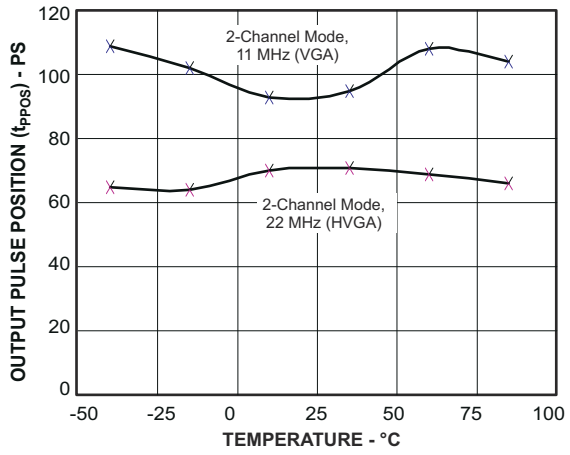


図 6-9. Output Pulse Position vs Temperature

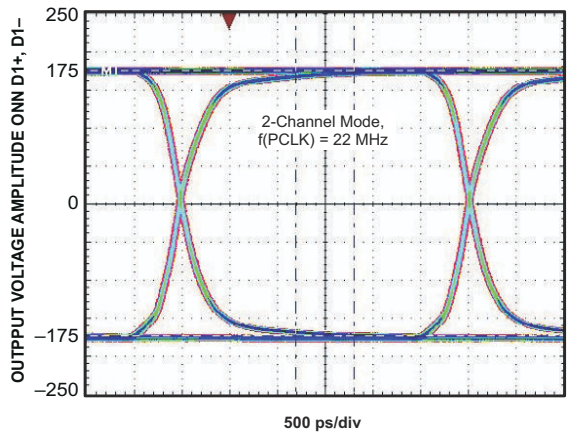


図 6-10. Data Eye Pattern, 2-channel Mode

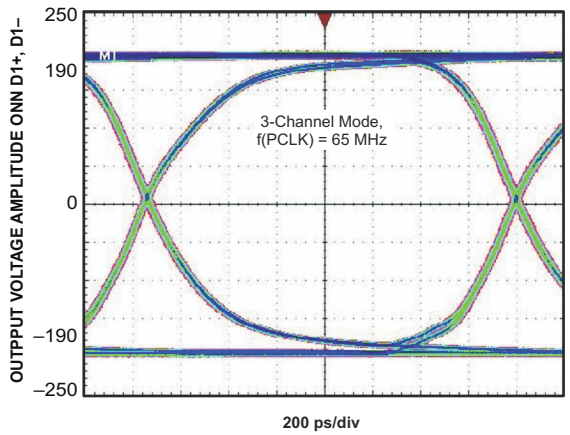


図 6-11. Data Eye Pattern, 3-channel Mode

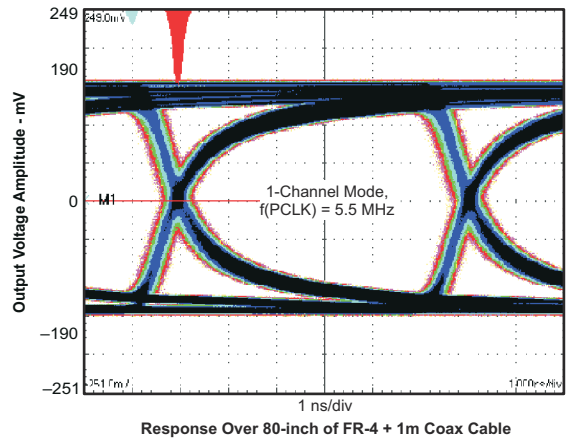


図 6-12. QVGA Output Waveform

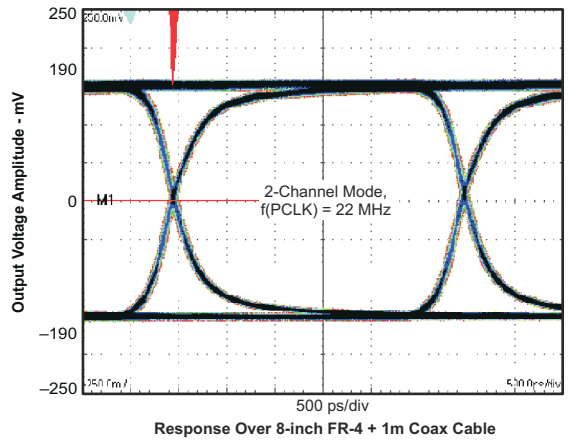


図 6-13. VGA 2-channel Output Waveform

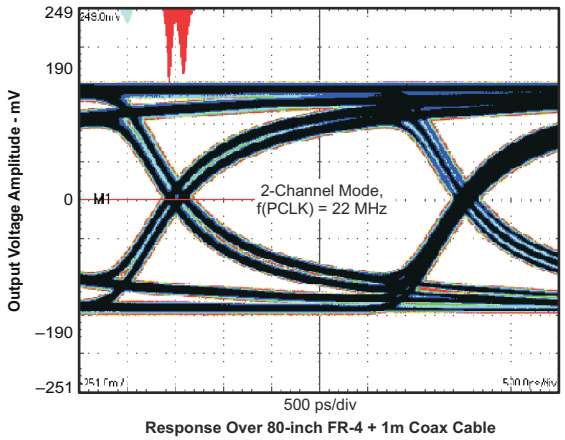


図 6-14. VGA 2-channel Output Waveform

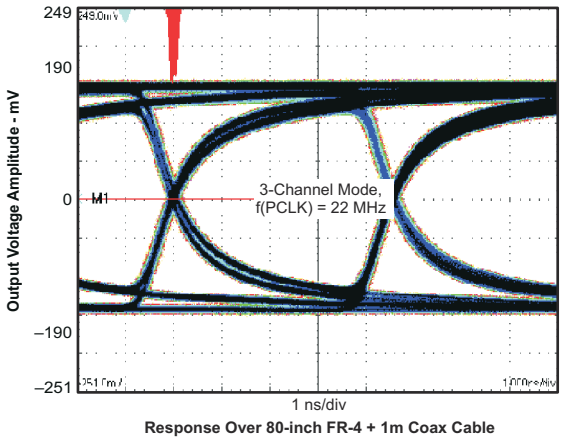


図 6-15. VGA 3-channel Output Waveform

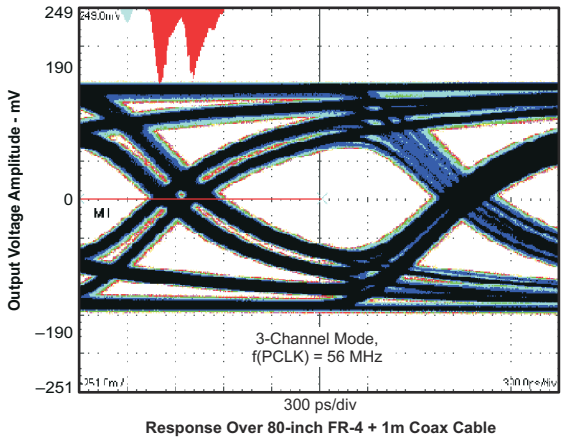


図 6-16. XGA 3-channel Output Waveform

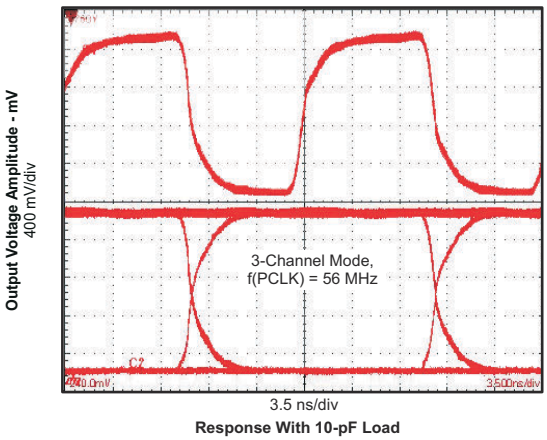


図 6-17. XGA 3-channel Output Waveform on the SN65LVDS302 when driven by the SN65LVDS301

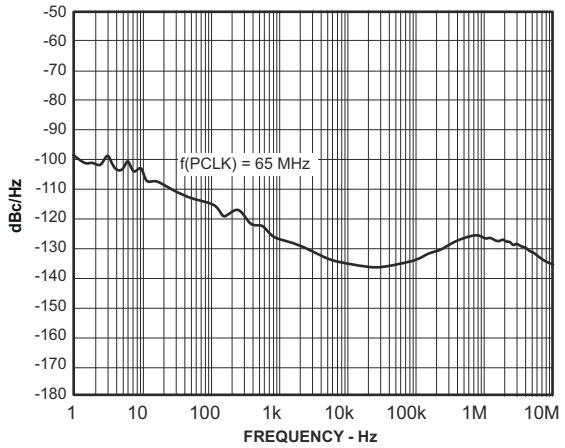


図 6-18. PLL Phase Noise

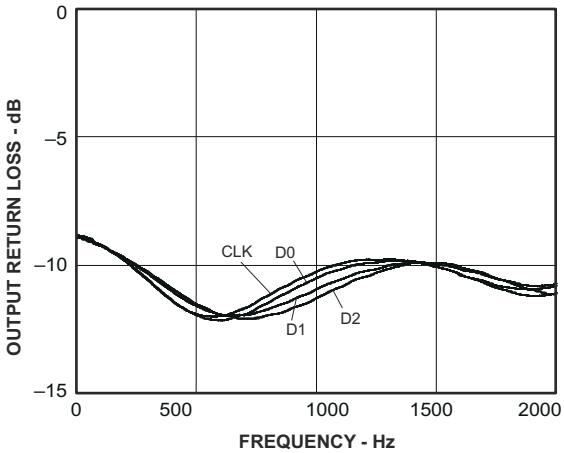


図 6-19. Output Return Loss

Copyright © 2023 Texas Instruments Incorporated

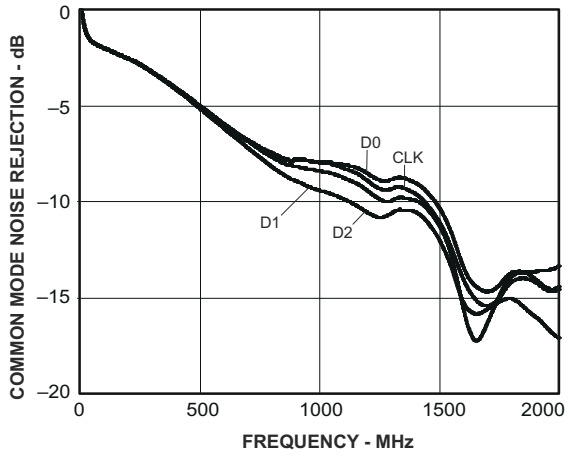


図 6-20. Output Common Mode Noise Rejection

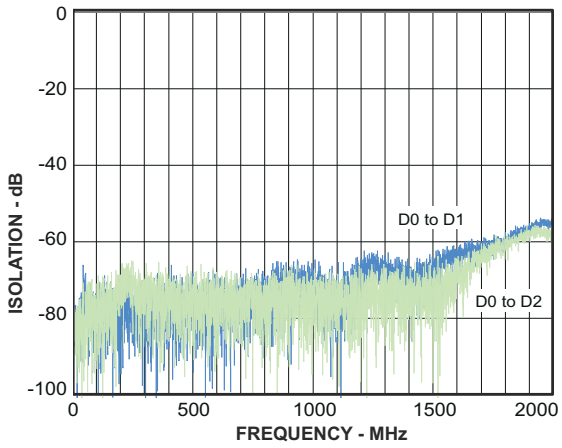


図 6-21. Crosstalk

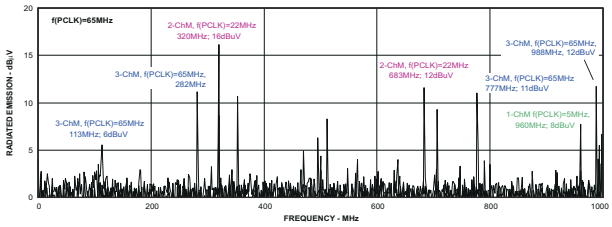


図 6-22. GTEM SAE J1752/3 EMI Test

7 Parameter Measurement Information

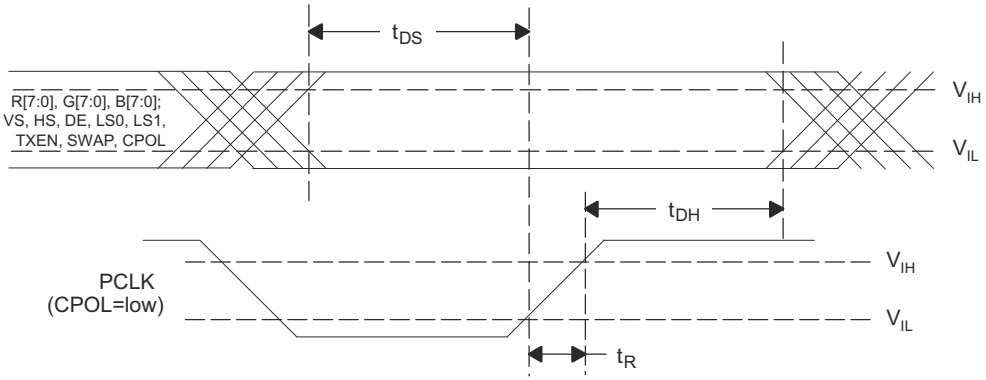


図 7-1. Setup/Hold Time

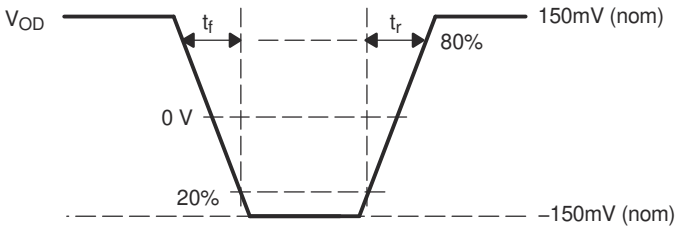
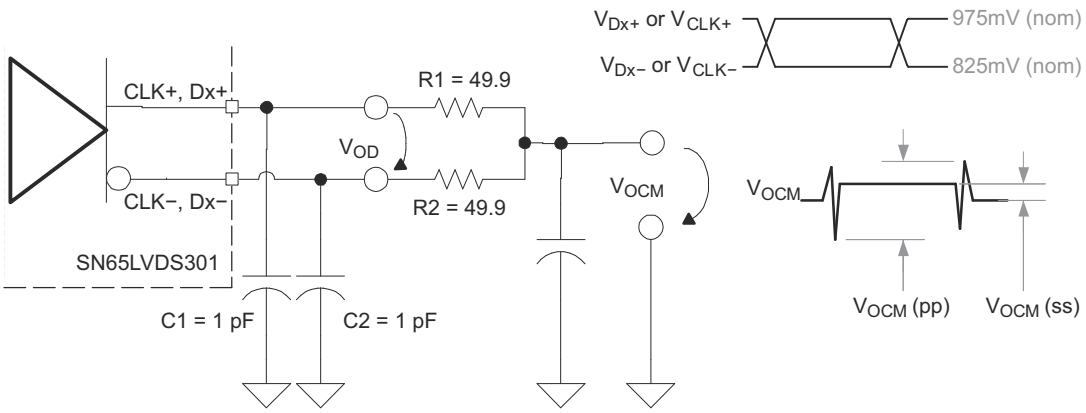


図 7-2. Rise and Fall Time Definitions



NOTES:
A. 20 MHz output test pattern on all differental outputs (CLK, D0, D1, and D2):
this is achieved by: 1. Device is set to 3-channel-mode;
2. f_{PCLK} = 20 MHz
3. Inputs R[7:3] = B[7:3] connected to V_{DD}, all other data inputs set to GND.
B. C1, C2 and C3 includes instrumentation and fixture capacitance; tolerance ± 20%; C, R1 and R2 tolerance ± 1%.
C. The measurement of V_{OCM}(pp) and V_{OC}(ss) are taken with test equipment bandwidth >1 GHz.

図 7-3. Driver Output Voltage Test Circuit and Definitions

Copyright © 2023 Texas Instruments Incorporated

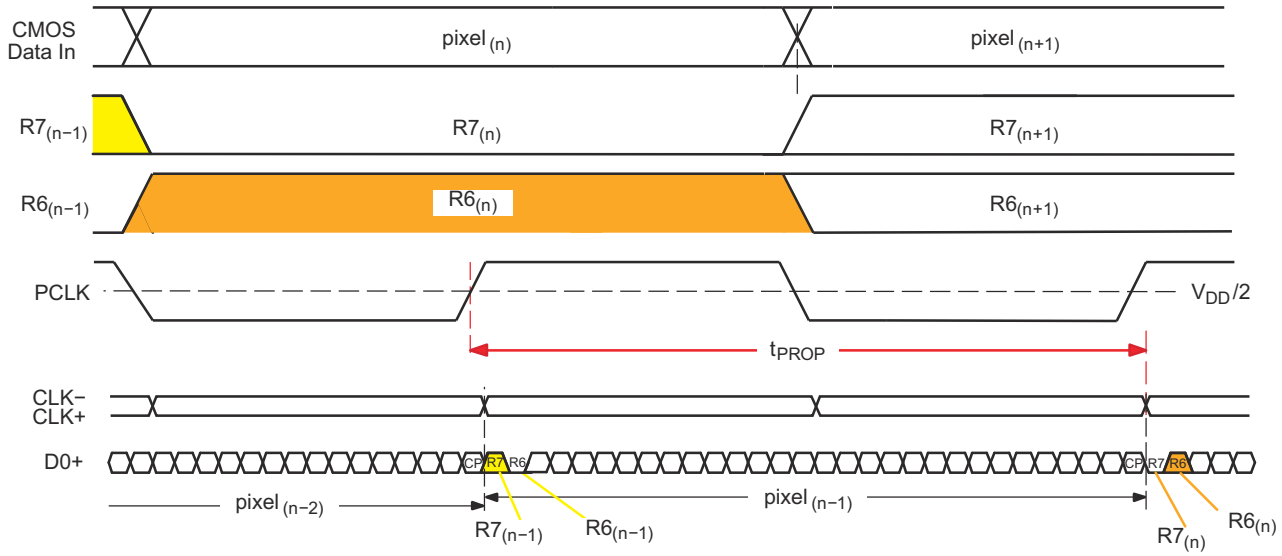


図 7-4. $t_{pd(L)}$ Propagation Delay Input to Output (LS0 = LS1 = 0; CPOL = 0)

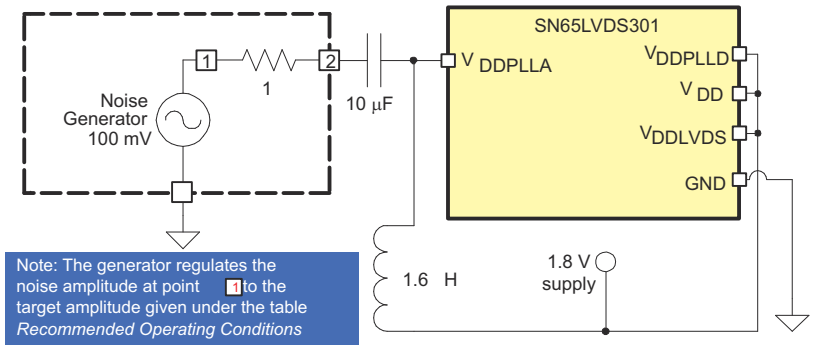


図 7-5. Power Supply Noise Test Set-Up

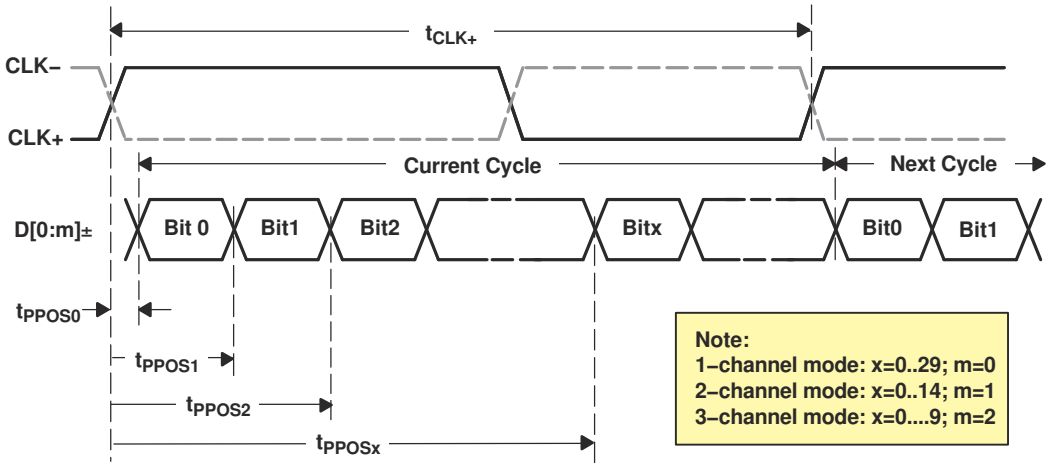


図 7-6. $t_{SK(0)}$ SubLVDS Output Pulse Position Measurement

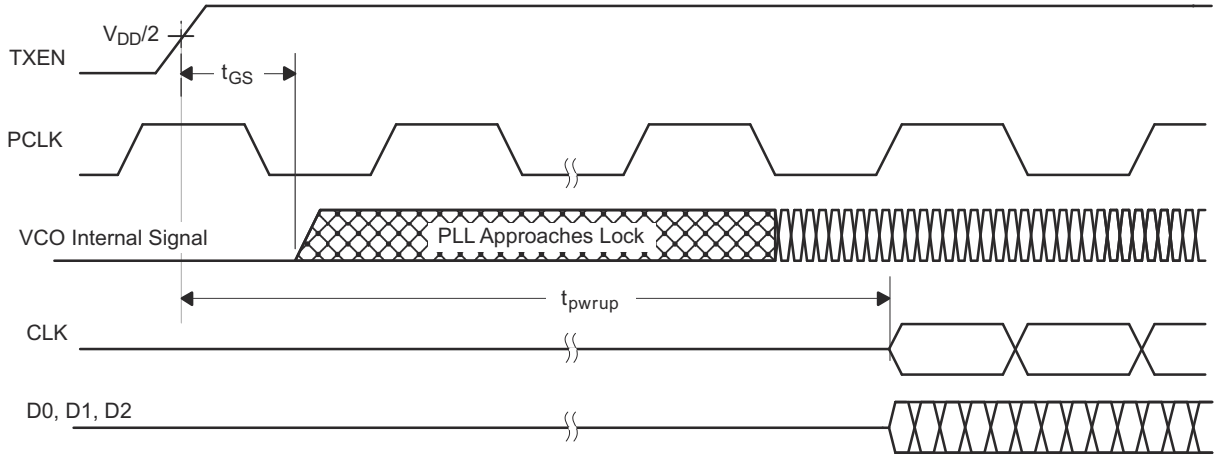


図 7-7. Transmitter Behavior While Approaching Sync

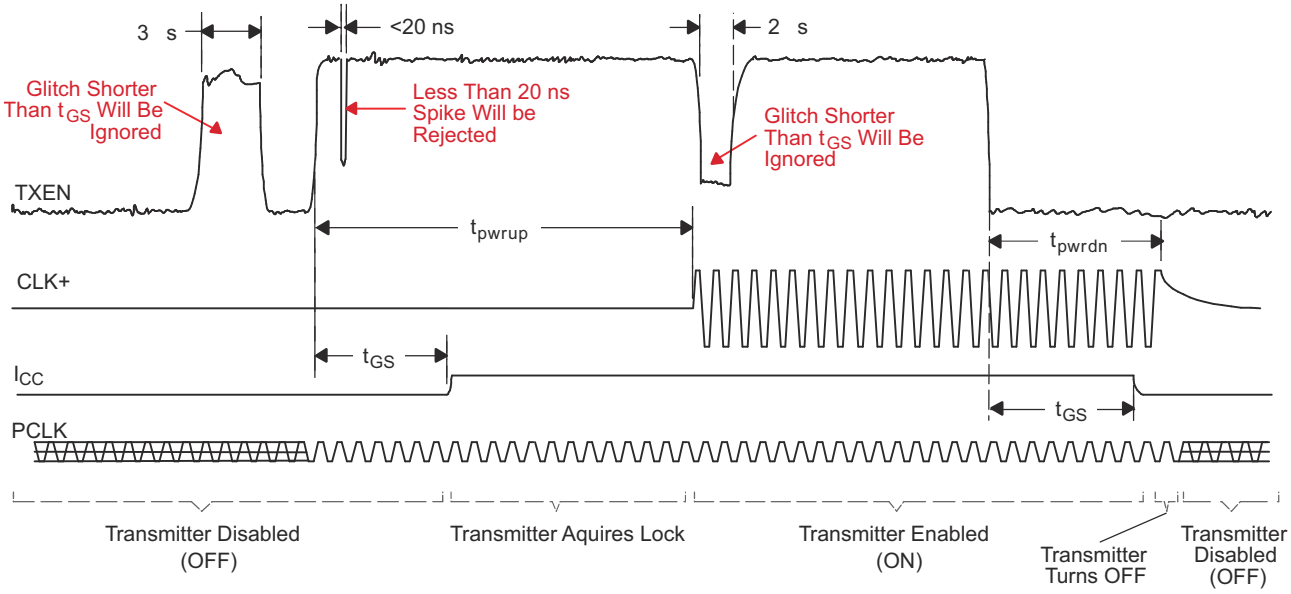


図 7-8. Transmitter Enable Glitch Suppression Time

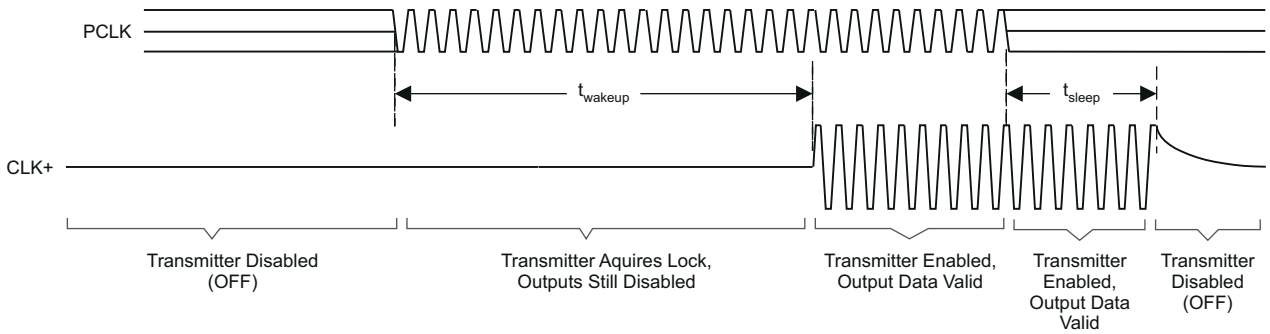


図 7-9. Standby Detection

7.1.1 Power Consumption Tests

表 7-1 shows an example test pattern word.

Copyright © 2023 Texas Instruments Incorporated

表 7-1. Example Test Pattern Word

Word	R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0x7C3E1E7

7				C				3				E				1				E				7			
R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	0	VS	HS	DE
0	1	1	1	1	1	0	0	0	0	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	1	1

7.1.1.1 Typical IC Power Consumption Test Pattern

The typical power consumption test patterns consists of sixteen 30-bit transmit words in 1-channel mode, eight 30-bit transmit words in 2-channel mode and five 30-bit transmit words in 3-channel mode. The pattern repeats itself throughout the entire measurement. It is assumed that every possible transmit code on RGB inputs has the same probability to occur during typical device operation.

7.1.1.2

表 7-2. Typical IC Power Consumption Test Pattern, 1-Channel Mode

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0x0000007
2	0xFFF0007
3	0x01FFF47
4	0xF0E07F7
5	0x7C3E1E7
6	0xE707C37
7	0xE1CE6C7
8	0xF1B9237
9	0x91BB347
10	0xD4CCC67
11	0xAD53377
12	0xACB2207
13	0xAAB2697
14	0x5556957
15	0xAAAAAB3
16	0xAAAAAA5

Copyright © 2023 Texas Instruments Incorporated

表 7-3. Typical IC Power Consumption Test Pattern, 2-Channel Mode

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0x0000001
2	0x03F03F1
3	0xBFFBFF1
4	0x1D71D71
5	0x4C74C71
6	0xC45C451
7	0xA3aA3A5
8	0x5555553

表 7-4. Typical IC Power Consumption Test Pattern, 3-Channel Mode

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0xFFFFFF1
2	0x0000001
3	0xF0F0F01
4	0xCCCCCC1
5	0xAAAAAA7

7.1.2 Maximum Power Consumption Test Pattern

The maximum (or worst-case) power consumption of the SN65LVDS301 is tested using the two different test patterns shown in 表 7-5 and 表 7-6. The test patterns consist of sixteen 30-bit transmit words in 1-channel mode, eight 30-bit transmit words in 2-channel mode and five 30-bit transmit words in 3-channel mode. The pattern repeats itself throughout the entire measurement. It is assumed that every possible transmit code on RGB inputs has the same probability to occur during typical device operation.

表 7-5. Worst-Case Power Consumption Test Pattern

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0xAAAAAA5
2	0x5555555

表 7-6. Worst-Case Power Consumption Test Pattern

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0x0000000
2	0xFFFFFF7

Copyright © 2023 Texas Instruments Incorporated

7.1.3 Output Skew Pulse Position & Jitter Performance

The following test patterns are used to measure the output-skew pulse position and the jitter performance of the SN65LVDS301. The jitter test pattern stresses the interconnect, particularly to test for ISI. Very long run-lengths of consecutive bits incorporate very high and low data rates, maximinges switching noise. Each pattern is self-repeating for the duration of the test.

表 7-7. Transmit Jitter Test Pattern, 1-Channel Mode

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0x0000001
2	0x0000031
3	0x00000F1
4	0x00003F1
5	0x0000FF1
6	0x0003FF1
7	0x000FFF1
8	0x0F0F0F1
9	0x0C30C31
10	0x0842111
11	0x1C71C71
12	0x18C6311
13	0x1111111
14	0x3333331
15	0x2452413
16	0x22A2A25
17	0x5555553
18	0xDB6DB65
19	0xCCCCCC1
20	0xEEEEEE1
21	0xE739CE1
22	0xE38E381
23	0xF7BDEE1
24	0xF3CF3C1
25	0xF0F0F01
26	0xFFF0001
27	0xFFFC001
28	0xFFFF001
29	0xFFFFC01
30	0xFFFFF01
31	0xFFFFFC1
32	0xFFFFFF1

Copyright © 2023 Texas Instruments Incorporated

表 7-8. Transmit Jitter Test Pattern, 2-Channel Mode

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0x0000001
2	0x000FFF3
3	0x8008001
4	0x0030037
5	0xE00E001
6	0x00FF001
7	0x007E001
8	0x003C001
9	0x0018001
10	0x1C7E381
11	0x3333331
12	0x555AAA5
13	0x6DBDB61
14	0x7777771
15	0x555AAA3
16	0xAAAAAA5
17	0x5555553
18	0xAAA5555
19	0x8888881
20	0x9242491
21	0xAAA5571
22	0xCCCCCC1
23	0xE3E1C71
24	0xFFE7FF1
25	0xFFC3FF1
26	0xFF81FF1
27	0xFE00FF1
28	0x1FF1FF1
29	0xFFCFFC3
30	0x7FF7FF1
31	0xFFF0007
32	0xFFFFFF1

Copyright © 2023 Texas Instruments Incorporated

表 7-9. Transmit Jitter Test Pattern, 3-Channel Mode

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0x0000001
2	0x0000001
3	0x0000003
4	0x0101013
5	0x0303033
6	0x0707073
7	0x1818183
8	0xE7E7E71
9	0x3535351
10	0x0202021
11	0x5454543
12	0xA5A5A51
13	0xADADAD1
14	0x5555551
15	0xA6A2AA3
16	0xA6A2AA5
17	0x5555553
18	0x5555555
19	0xAAAAAA1
20	0x5252521
21	0x5A5A5A1
22	0xABABAB1
23	0xFDFCFD1
24	0xCAAACA1
25	0x1818181
26	0xE7E7E71
27	0xF8F8F81
28	0xFCFCFC1
29	0xFEFEFE1
30	0xFFFFFF1
31	0xFFFFFF5
32	0xFFFFFF5

Copyright © 2023 Texas Instruments Incorporated

8 Detailed Description

8.1 Overview

The SN65LVDS301 is a serialising device where the input paralle data is converted to Sub Low-Voltage Differential Signaling (SubLVDS) serial outputs. The SN65LVDS301 supports three power modes (Shutdown, Standby and Active) to conserve power. When transmitting, the PLL locks to the incoming pixel clock PCLK and generates an internal high-speed clock at the line rate of the data lines. The parallel data are latched on the rising or falling edge of PCLK as selected by the external control signal CPOL. The serialized data is presented on the serial outputs D0, D1, D2 with a recreated PCLK generated from the internal high-speed clock, output on the CLK output. If PCLK stops, the device enters a standby mode to conserve power

The parallel (CMOS) input bus offers a bus-swap feature. The SWAP pin configures the input order of the pixel data to be either R[7:0]. G[7:0], B[7:0], VS, HS, DE or B[0:7]. G[0:7], R[0:7], VS, HS, DE. This gives a PCB designer the flexibility to better match the bus to the host controller pinout or to put the transmitter device on the top side or the bottom side of the PCB.

Two Link Select lines LS0 and LS1 control whether 1, 2 or 3 serial links are used. The TXEN input may be used to put the SN65LVDS301 in a shutdown mode. The SN65LVDS301 enters an active Standby mode if the input clock PCLK stops.

Copyright © 2023 Texas Instruments Incorporated

8.2 Functional Block Diagram

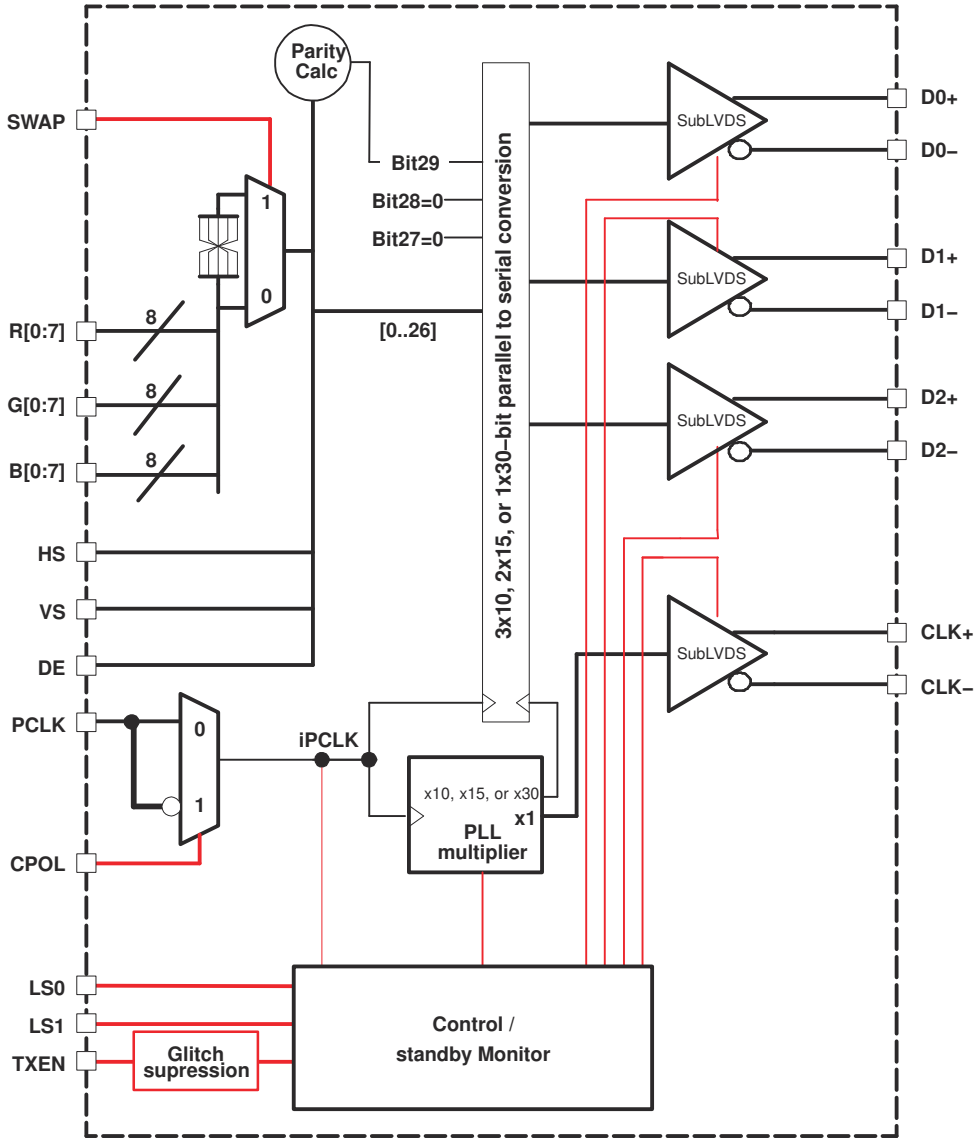


図 8-1. Functional Block Diagram

8.3 Feature Description

8.3.1 Swap Pin Functionality

The SWAP pin allows the pcb designer to reverse the RGB bus to minimize potential signal crossovers in the PCB routing. The two drawings beneath show the RGB signal pin assignment based on the SWAP-pin setting.

Copyright © 2023 Texas Instruments Incorporated

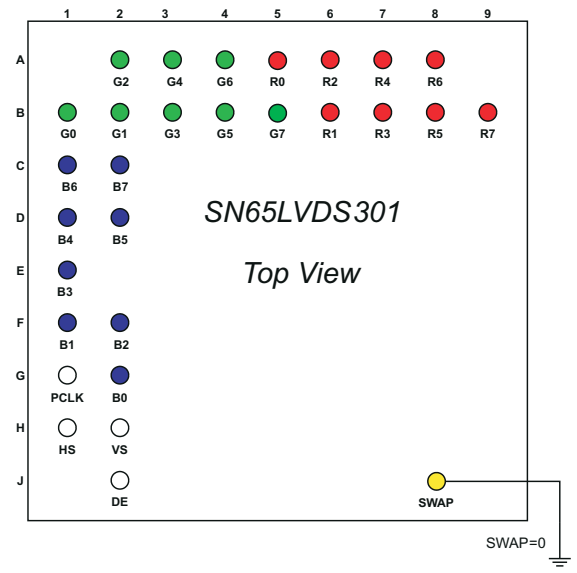


図 8-2. SWAP PIN = 0

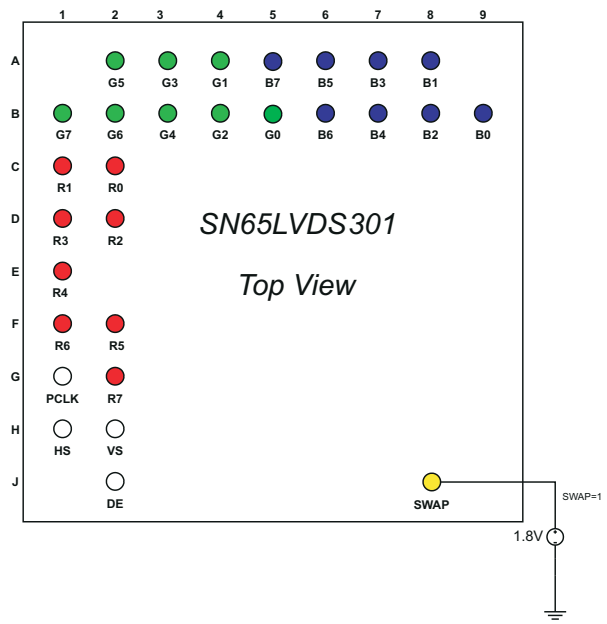


図 8-3. SWAP PIN = 1

表 8-1. NUMERIC PIN LIST

PIN	SWAP	SIGNAL	PIN	SWAP	SIGNAL	PIN	SWAP	SIGNAL
A1	—	GND	C1	0	B6	F1	0	B1
A2	0	G2		1	R1		1	R6
	1	G5	C2	0	B7	F2	0	B2
A3	0	G4		1	R0		1	R5
	1	G3	C3	UNPOPULATED		F3	—	VDD
A4	0	G6	C4	—	VDD	F4	—	GND
	1	G1	C5	—	GND	F5	—	GND
A5	0	R0	C6	—	VDD	F6	—	GND
	1	B7	C7	—	VDD	F7	—	GND
A6	0	R2	C8	—	GND	F8	—	V_{DDPLLD}
	1	B5	C9	—	LS0	F9	—	D1+
A7	0	R4	D1	0	B4	G1	—	PCLK
	1	B3		1	R3	G2	0	B0
A8	0	R6	D2	0	B5		1	R7
	1	B1		1	R2	G3	—	V_{DD}
A9	—	GND	D3	—	VDD	G4	—	GND
B1	0	G0	D4	—	GND	G5	—	GND
	1	G7	D5	—	GND	G6	—	GND
B2	0	G1	D6	—	GND	G7	—	GND
	1	G6	D7	—	GND	G8	—	GND_{LVDS}
B3	0	G3	D8	—	LS1	G9	—	D1–
	1	G4	D9	—	D2+	H1	—	HS
B4	0	G5	E1	0	B3	H2	—	VS
	1	G2		1	R4	H3	—	GND
B5	0	G7	E2	—	GND	H4	—	GND_{LVDS}
	1	G0	E3	—	VDD	H5	—	V_{DDLVDS}

Copyright © 2023 Texas Instruments Incorporated

表 8-1. NUMERIC PIN LIST (continued)

PIN	SWAP	SIGNAL	PIN	SWAP	SIGNAL	PIN	SWAP	SIGNAL
B6	0	R1	E4	—	GND	H6	—	GND_{PLLA}
	1	B6	E5	—	GND	H7	—	V_{DDPLLA}
B7	0	R3	E6	—	GND	H8	—	V_{DDLVDS}
	1	B4	E7	—	GND	H9	—	CPOL
B8	0	R5	E8	—	GND_{PLLD}	J1	—	GND
	1	B2	E9	—	D2–	J2	—	DE
B9	0	R7				J3	—	TXEN
	1	B0				J4	—	D0–
						J5	—	D0+
						J6	—	CLK–
						J7	—	CLK+
						J8	—	SWAP
						J9	—	GND_{LVDS}

8.3.2 Parity Bit Generation

The SN65LVDS301 transmitter calculates the parity of the transmit data word and sets the parity bit accordingly. The parity bit covers the 27 bit data payload consisting of 24 bits of pixel data plus VS, HS and DE. The two reserved bits are not included in the parity generation. ODD Parity bit signaling is used. The transmitter sets the Parity bit if the sum of the 27 data bits result in an even number of ones. The Parity bit is cleared otherwise. This allows the receiver to verify Parity and detect single bit errors.

8.4 Device Functional Modes

8.4.1 Serialization Modes

The SN65LVDS301 transmitter has three modes of operation controlled by link-select pins LS0 and LS1. 表 8-2 shows the serializer modes of operation.

表 8-2. Logic Table: Link Select Operating Modes

LS1	LS0		Mode of Operation	Data Links Status
0	0	1ChM	1-channel mode (30-bit serialization rate)	D0 active; D1, D2 high-impedance
0	1	2ChM	2-channel mode (15-bit serialization rate)	D0, D1 active; D2 high-impedance
1	0	3ChM	3-channel mode (10-bit serialization rate)	D0, D1, D2 active
1	1		Reserved	Reserved

8.4.1.1 1-Channel Mode

While LS0 and LS1 are held low, the SN65LVDS301 transmits payload data over a single SubLVDS data pair, D0. The PLL locks to PCLK and internally multiplies the clock by a factor of 30. The internal high-speed clock is used to serialize (shift out) the data payload on D0. Two reserved bits and the parity bit are added to the data frame. 図 8-4 illustrates the timing and the mapping of the data payload into the 30-bit frame. The internal high-speed clock is divided by a factor of 30 to recreate the pixel clock, and presented on the SubLVDS CLK output. While in this mode, the PLL can lock to a clock that is in the range of 4 MHz through 15 MHz. This mode is intended for smaller video display formats (e.g. QVGA to HVGA) that do not require the full bandwidth capabilities of the SN65LVDS301.

Copyright © 2023 Texas Instruments Incorporated

図 8-4. Data and Clock Output in 1-Channel Mode (LS0 and LS1 = low).

8.4.1.2 2-Channel Mode

While LS0 is held high and LS1 is held low, the SN65LVDS301 transmits payload data over two SubLVDS data pairs, D0 and D1. The PLL locks to PCLK and internally multiplies it by a factor of 15. The internal high-speed clock is used to serialize the data payload on D0, and D1. Two reserved bits and the parity bit are added to the data frame. 図 8-5 illustrates the timing and the mapping of the data payload into the 30-bit frame and how the frame becomes split into the two output channels. The internal high-speed clock is divided by 15 to recreate the pixel clock, and presented on SubLVDS CLK. The PLL can lock to a clock that is in the range of 8 MHz through 30 MHz in this mode. Typical applications for using the 2-channel mode are HVGA and VGA displays.

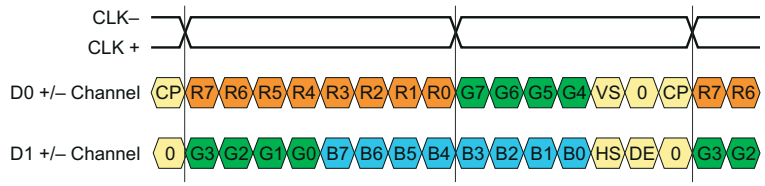


図 8-5. Data and Clock Output in 2-Channel Mode (LS0 = high; LS1 = low).

Copyright © 2023 Texas Instruments Incorporated

8.4.1.3 3-Channel Mode

While LS0 is held low and LS1 is held high, the SN65LVDS301 transmits payload data over three SubLVDS data pairs D0, D1, and D2. The PLL locks to PCLK, and internally multiplies it by 10. The internal high-speed clock is used to serialize the data payload on D0, D1, and D2. Two reserved bits and the parity bit are added to the data frame. 図 8-6 illustrates the timing and the mapping of the data payload into the 30-bit frame and how the frame becomes split over the three output channels. The internal high speed clock is divided back down by a factor of 10 to recreate the pixel clock and presented on SubLVDS CLK output. While in this mode, the PLL can lock to a clock in the range of 20 MHz through 65 MHz. The 3-channel mode supports applications with very large display resolutions such as VGA or XGA.

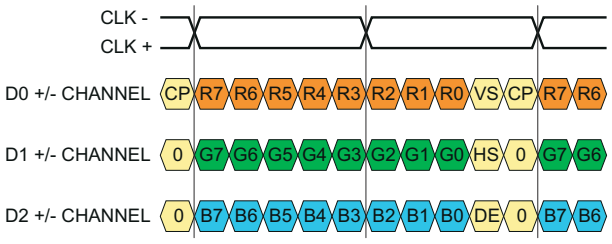


図 8-6. Data and Clock Output in 3-Channel Mode (LS0 = low; LS1 = high).

8.4.2 Powerdown Modes

The SN65LVDS301 Transmitter has two powerdown modes to facilitate efficient power management.

8.4.3 Shutdown Mode

The SN65LVDS301 enters Shutdown mode when the TXEN pin is asserted low. This turns off all transmitter circuitry, including the CMOS input, PLL, serializer, and SubLVDS transmitter output stage. All outputs are high-impedance. Current consumption in Shutdown mode is nearly zero.

8.4.4 Standby Mode

The SN65LVDS301 enters the Standby mode if TXEN is high and the PCLK input signal frequency is less than 500kHz. All circuitry except the PCLK input monitor is shut down, and all outputs enter high-impedance mode. The current consumption in Standby mode is very low. When the PCLK input signal is completely stopped, the I_{DD} current consumption is less than 10 µA. The PCLK input must not be left floating.

注

A floating (left open) CMOS input allows leakage currents to flow from V_{DD} to GND. To prevent large leakage current, a CMOS gate must be kept at a valid logic level, either V_{IH} or V_{IL}. This can be achieved by applying an external voltage of V_{IH} or V_{IL} to all SN65LVDS301 inputs.

Copyright © 2023 Texas Instruments Incorporated

8.4.5 Active Modes

When TXEN is high and the PCLK input clock signal is faster than 3 MHz, the SN65LVDS301 enters Active mode. Current consumption in Active mode depends on operating frequency and the number of data transitions in the data payload.

8.4.6 Acquire Mode (PLL approaches lock)

The PLL is enabled and attempts to lock to the input Clock. All outputs remain in high-impedance mode. When the PLL monitor detects stable PLL operation, the device switches from Acquire to Transmit mode. For proper device operation, the pixel clock frequency must fall within the valid f_{PCLK} range specified under recommended operating conditions. If the pixel clock frequency is larger than 3 MHz but smaller than f_{PCLK}(min), the SN65LVDS301 PLL is enabled. Under such conditions, it is possible for the PLL to lock temporarily to the pixel clock, causing the PLL monitor to release the device into transmit mode. If this happens, the PLL may or may not be properly locked to the pixel clock input, potentially causing data errors, frequency oscillation, and PLL deadlock (loss of VCO oscillation).

8.4.7 Transmit Mode

After the PLL achieves lock, the device enters the normal transmit mode. The CLK pin outputs a copy of PCLK. Based on the selected mode of operation, the D0, D1, and D2 outputs carry the serialized data. In 1-channel mode, outputs D1 and D2 remain high-impedance. In the 2-channel mode, output D2 remains high-impedance.

8.4.8 Status Detect and Operating Modes Flow diagram

The SN65LVDS301 switches between the power saving and active modes in the following way:

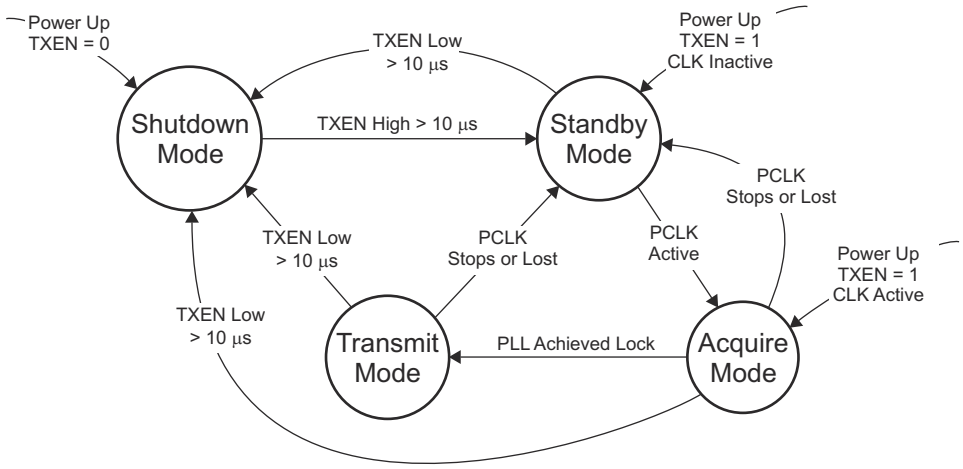


図 8-7. Status Detect and Operating Modes Flow Diagram

Copyright © 2023 Texas Instruments Incorporated

表 8-3. Status Detect and Operating Modes Descriptions

Mode	Characteristics	Conditions
Shutdown Mode	Least amount of power consumption(1) (most circuitry turned off); All outputs are high-impedance	TXEN is low(1) (2)
Standby Mode	Low power consumption (only clock activity circuit active; PLL is disabled to conserve power); All outputs are high-impedance	TXEN is high; PCLK input signal is missing or inactive(2)
Acquire Mode	PLL tries to achieve lock; All outputs are high-impedance	TXEN is high; PCLK input monitor detected input activity
Transmit Mode	Data transfer (normal operation); Transmitter serializes data and transmits data on serial output; unused outputs remain high-impedance	TXEN is high and PLL is locked to incoming clock

(1) In Shutdown Mode, all SN65LVDS301 internal switching circuits (e.g., PLL, serializer, etc.) are turned off to minimize power consumption. The input stage of any input pin remains active.
(2) Leaving inputs unconnected can cause random noise to toggle the input stage and potentially harm the device. All inputs must be tied to a valid logic level V_{IL} or V_{IH} during Shutdown or Standby Mode.

表 8-4. Operating Mode Transitions

MODE TRANSITION	USE CASE	TRANSITION SPECIFICS
Shutdown → Standby	Drive TXEN high to enable transmitter	1. TXEN high > 10 µs 2. Transmitter enters standby mode a. All outputs are high-impedance b. Transmitter turns on clock input monitor
Standby → Acquire	Transmitter activity detected	1. PCLK input monitor detects clock input activity; 2. Outputs remain high-impedance; 3. PLL circuit is enabled
Acquire → Transmit	Link is ready to transfer data	1. PLL is active and approaches lock 2. PLL achieved lock within 2 ms 3. Parallel Data input latches into shift register 4. CLK output turns on 5. selected Data outputs turn on and send out first serial data bit
Transmit → Standby	Request Transmitter to enter Standby mode by stopping PCLK	1. PCLK Input monitor detects missing PCLK 2. Transmitter indicates standby, putting all outputs into high-impedance; 3. PLL shuts down; 4. PCLK activity input monitor remains active
Transmit/Standby → Shutdown	Turn off Transmitter	1. TXEN pulled low for longer than 10us 2. Transmitter indicates standby, putting output CLK+ and CLK– into high-impedance state; 3. Transmitter puts all other outputs into high-impedance state 4. Most IC circuitry is shut down for least power consumption

Copyright © 2023 Texas Instruments Incorporated

9 Application information

9.1 Application Information

General application guidelines and hints for LVDS drivers and receivers may be found in the LVDS application notes and design guides.

9.2 Preventing Increased Leakage Currents in Control Inputs

A floating (left open) CMOS input allows leakage currents to flow from V_{DD} to GND. Do not leave any CMOS Input unconnected or floating. Every input must be connected to a valid logic level V_{IH} or V_{OL} while power is supplied to V_{DD}. This also minimizes the power consumption of standby and power down mode.

9.3 VGA Application

図 9-1 shows a possible implementation of a VGA display. The LVDS301 interfaces to the SN65LVDS302, which is the corresponding receiver device to deserialize the data and drive the display driver. The pixel clock rate of 22 MHz assumes ~10% blanking overhead and 60 Hz display refresh rate. The application assumes 24-bit color resolution. It is also shown, how the application processor provides a powerdown (reset) signal for both serializer and the display driver. The signal count over the FPC could be further decreased by using the standby option on the SN65LVDS302 and pulling RXEN high with a 30 kΩ resistor to V_{DD}.

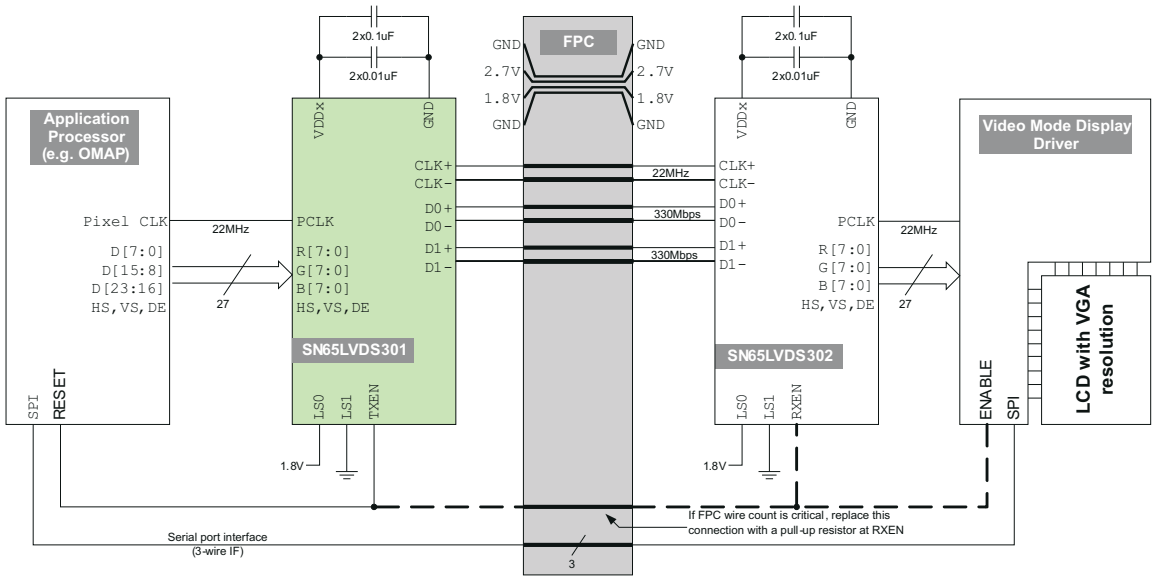


図 9-1. Typical VGA Display Application

Copyright © 2023 Texas Instruments Incorporated

9.4 Dual LCD-Display Application

The example in 図 9-2 shows a possible application setup driving two video mode displays from one application processor. The data rate of 330 Mbps at a pixel clock rate of 5.5 MHz corresponds to QVGA resolution at 60 Hz refresh rate and 10% blanking overhead.

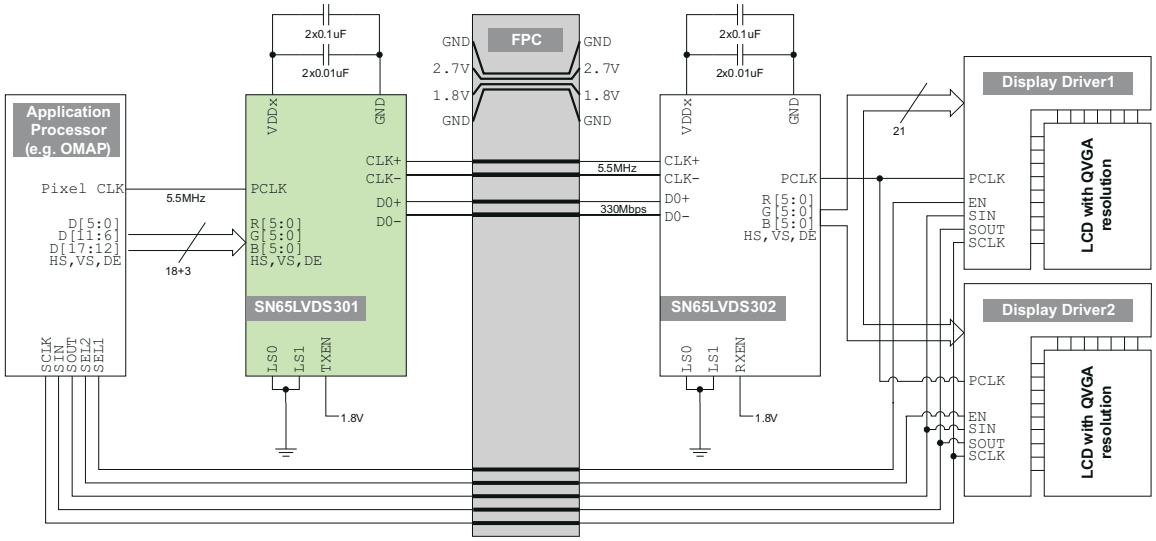


図 9-2. Example Dual-QVGA Display Application

9.5 Typical Application Frequencies

The SN65LVDS301 supports pixel clock frequencies from 4 MHz to 65 MHz over 1, 2, or 3 data lanes. 表 9-1 provides a few typical display resolution examples and shows the number of data lanes necessary to connect the LVDS301 with the display. The blanking overhead is assumed to be 20%. Often, blanking overhead is smaller, resulting in a lower data rate. Furthermore, the examples in the table assumes a display frame refresh rate of 60 Hz or 90 Hz. The actual refresh rate may differ depending on the application-processor clock implementation.

表 9-1. Typical Application Data Rates & Serial Lane Usage

Display Screen Resolution	Visible Pixel Count	Blanking Overhead	Display Refresh Rate	Pixel Clock Frequency [MHz]	Serial Data Rate Per Lane		
					1-ChM	2-ChM	3-ChM
176x220 (QCIF+)	38,720	20%	90 Hz	4.2 MHz	125 Mbps		
240x320 (QVGA)	76,800		60 Hz	5.5 MHz	166 Mbps		
640x200	128,000			9.2 MHz	276 Mbps	138 Mbps	
352x416 (CIF+)	146,432			10.5 MHz	316 Mbps	158 Mbps	
352x440	154,880			11.2 MHz	335 Mbps	167 Mbps	
320x480 (HVGA)	153,600			11.1 MHz	332 Mbps	166 Mbps	
800x250	200,000			14.4 MHz	432 Mbps	216 Mbps	
640x320	204,800			14.7 MHz	442 Mbps	221 Mbps	
640x480 (VGA)	307,200			22.1 MHz		332 Mbps	221 Mbps
1024x320	327,680			23.6 MHz		354 Mbps	236 Mbps
854x480 (WVGA)	409,920			29.5 MHz		443 Mbps	295 Mbps
800x600 (SVGA)	480,000			34.6 MHz			346 Mbps
1024x768 (XGA)	786,432			56.6 MHz			566 Mbps

Copyright © 2023 Texas Instruments Incorporated

9.5.1 Calculation Example: HVGA Display

This example calculation shows a typical Half-VGA display with these parameters:

Display Resolution:	480 x 320
Frame Refresh Rate:	58.4 Hz
Horizontal Visible Pixel:	480 columns
Horizontal Front Porch:	20 columns
Horizontal Sync:	5 columns
Horizontal Back Porch:	3 columns
Vertical Visible Pixel:	320 lines
Vertical Front Porch:	10 lines
Vertical Sync:	5 lines
Vertical Back Porch:	3 lines

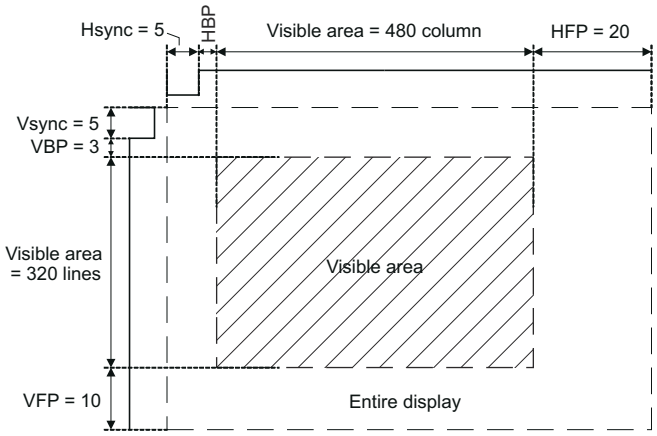


図 9-3. HVGA Display Parameters

Calculation of the total number of pixel and Blanking overhead:

Visible Area Pixel Count:	480 × 320 = 153600 pixel
Total Frame Pixel Count:	(480+20+5+3) × (320+10+5+3) = 171704 pixel
Blanking Overhead:	(171704-153600) ÷ 153600 = 11.8 %

The application requires following serial-link parameters:

Pixel Clk Frequency:	171704 × 58.4 Hz = 10.0 MHz
Serial Data Rate:	1-channel mode: 10.0 MHz × 30 bit/channel = 300 Mbps
	2-channel mode: 10.0 MHz × 15 bit/channel = 150 Mbps

Copyright © 2023 Texas Instruments Incorporated

10 Power Supply Design Recommendation

For a multilayer pcb, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane.

10.1 Decoupling Recommendation

The SN65LVDS301 was designed to operate reliably in a constricted environment with other digital switching ICs. In many designs, the SN65LVDS301 often shares a power supply with the application processor. The SN65LVDS301 can operate with power supply noise as specified in *Recommend Device Operating Conditions*. To minimize the power supply noise floor, provide good decoupling near the SN65LVDS301 power pins. The use of four ceramic capacitors (2×0.01 µF and 2×0.1 µF) provides good performance. At the very least, it is recommended to install one 0.1 µF and one 0.01 µF capacitor near the SN65LVDS301. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and IC power inputs pins must be minimized. Placing the capacitor underneath the SN65LVDS301 on the bottom of the pcb is often a good choice.

Copyright © 2023 Texas Instruments Incorporated

11 Layout

11.1 Layout Guidelines

Use chamfered corners (45° bends) instead of right-angle (90°) bends. Right-angle bends increase the effective trace width, which changes the differential trace impedance creating large discontinuities. A 45° bend is seen as a smaller discontinuity.

When routing traces next to a via or between an array of vias, make sure that the via clearance section does not interrupt the path of the return current on the ground plane below.

Avoid metal layers and traces underneath or between the pads of the LVDS connectors for better impedance matching. Otherwise they cause the differential impedance to drop below 75 Ω and fail the board during TDR testing.

Use solid power and ground planes for 100 Ω impedance control and minimum power noise.

For a multilayer PCB, TI recommends keeping one common GND layer underneath the device and connect all ground terminals directly to this plane. For 100 Ω differential impedance, use the smallest trace spacing possible, which is usually specified by the PCB vendor.

Keep the trace length as short as possible to minimize attenuation.

Place bulk capacitors (10 µF) close to power sources, such as voltage regulators or where the power is supplied to the PCB.

Copyright © 2023 Texas Instruments Incorporated

12 Device and Documentation Support

12.1 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

12.2 Trademarks

FlatLink™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
nFBGA® is a registered trademark of Tessera, Inc..
すべての商標は、それぞれの所有者に帰属します。

12.3 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.4 用語集

TI 用語集　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2023 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDS301ZXH	Active	Production	NFBGA (ZXH) | 80	576 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	LVDS301
SN65LVDS301ZXH.A	Active	Production	NFBGA (ZXH) | 80	576 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	LVDS301
SN65LVDS301ZXHR	Active	Production	NFBGA (ZXH) | 80	2500 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	LVDS301
SN65LVDS301ZXHR.A	Active	Production	NFBGA (ZXH) | 80	2500 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	LVDS301

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

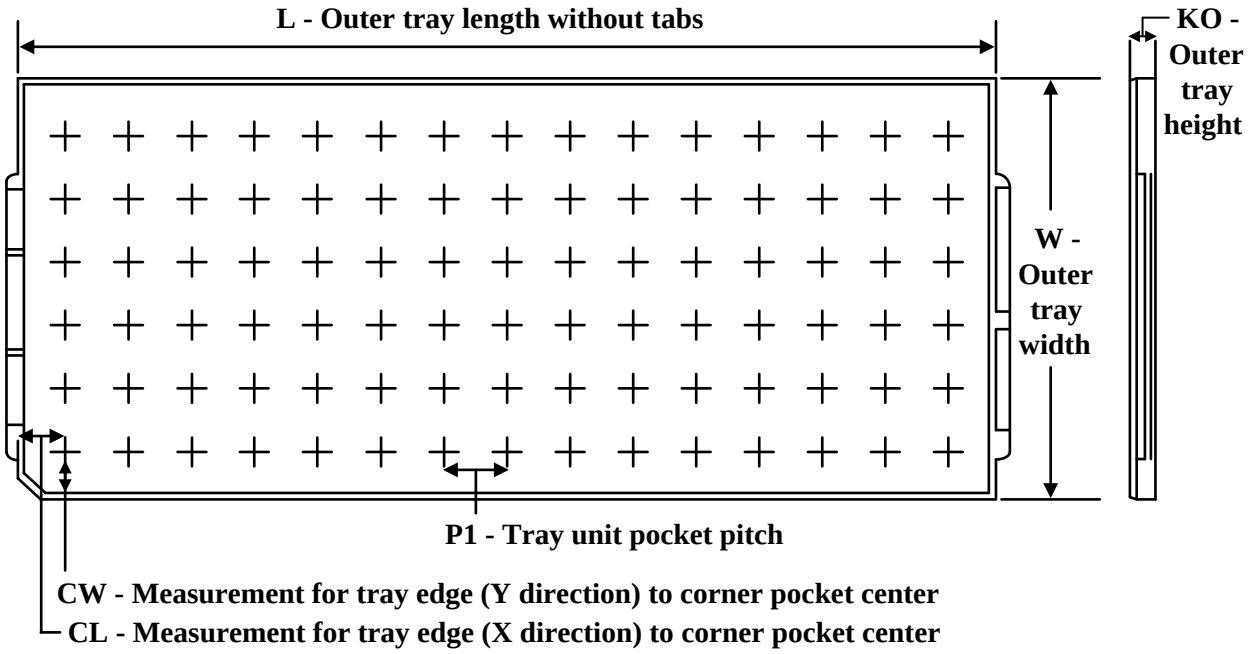
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

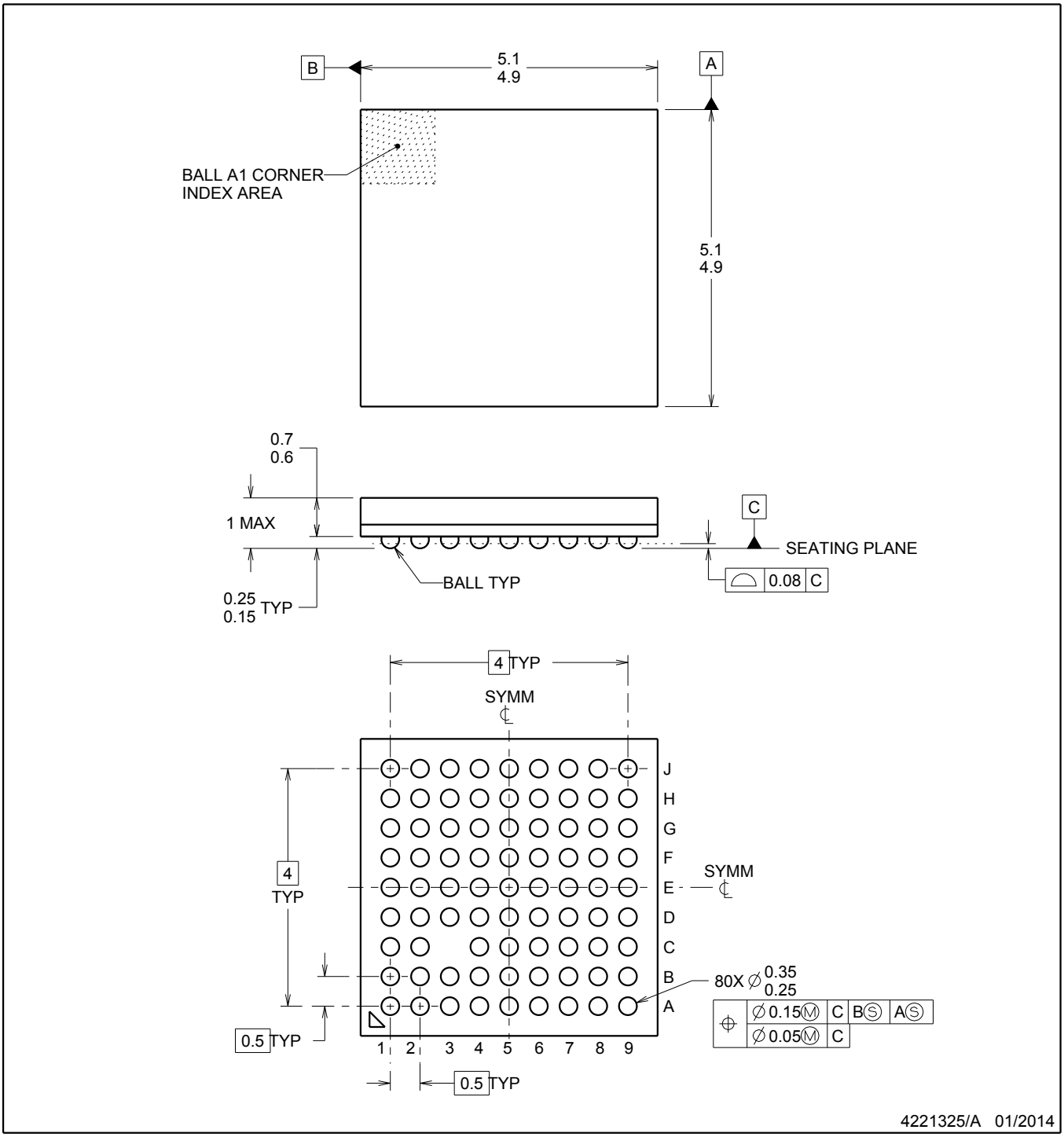
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
SN65LVDS301ZXH	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7
SN65LVDS301ZXH.A	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7

PACKAGE OUTLINE

ZXH0080A

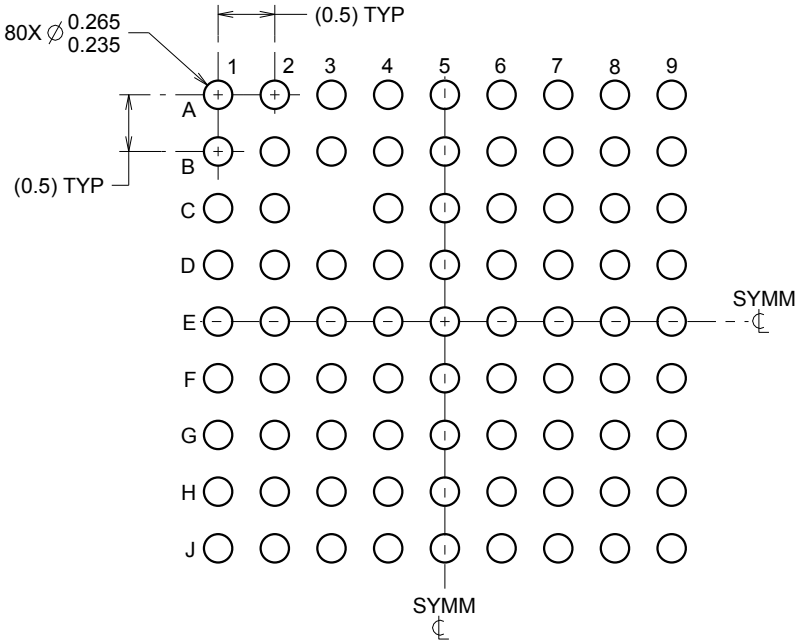
NFBGA - 1 mm max height

BALL GRID ARRAY

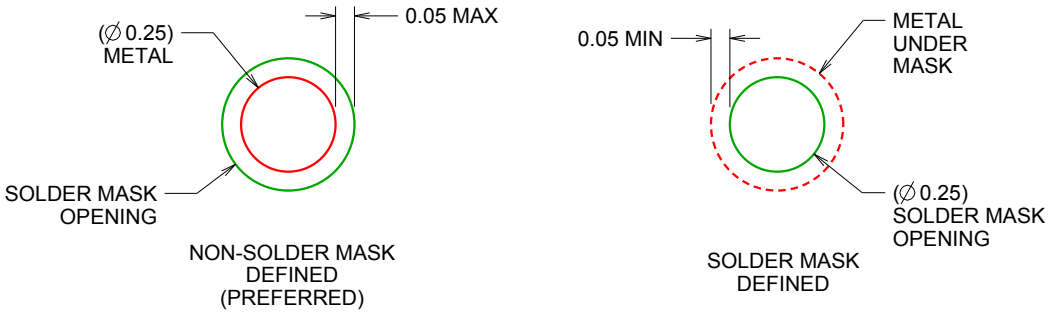


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis is for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This is a Pb-free solder ball design.



LAND PATTERN EXAMPLE
SCALE:15X

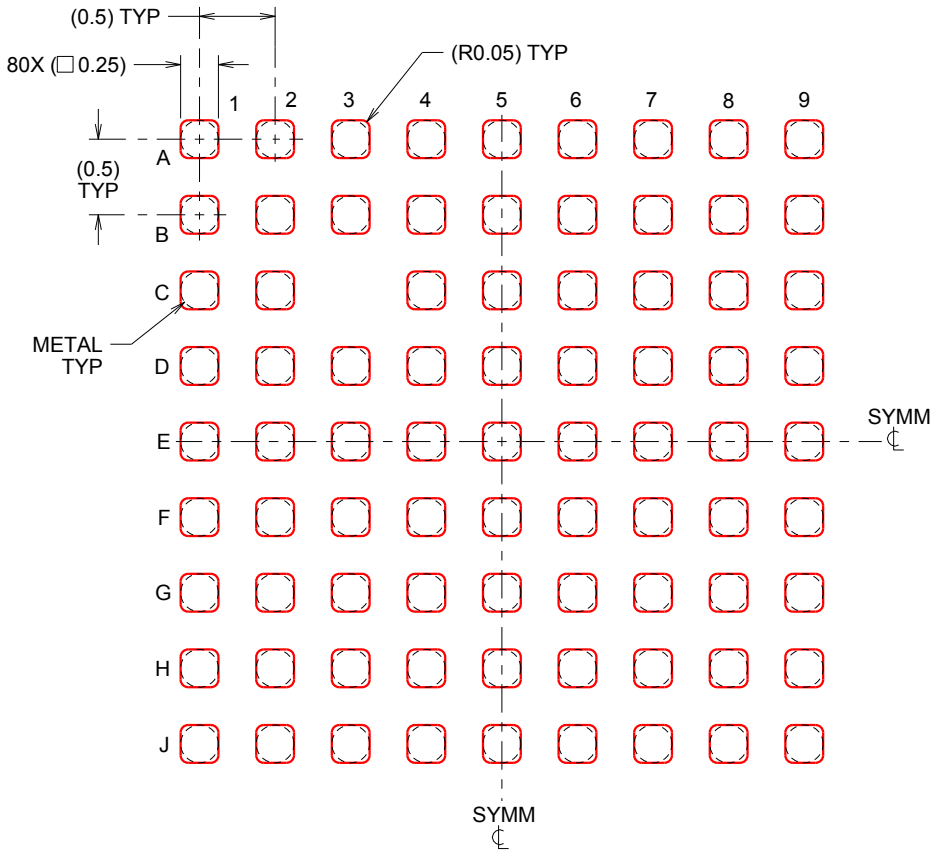


SOLDER MASK DETAILS
NOT TO SCALE

4221325/A 01/2014

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X

4221325/A 01/2014

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月