SN65MLVD203B IEC ESD 保護機能搭載 全二重、Type-1 マルチポイント LVDS トランシーバ

1 特長

- マルチポイント・データ交換の M-LVDS 規格 TIA / EIA-899 と互換性あり
- 最高 200Mbps までの信号速度[1]、最高 100MHz のクロック周波数に対応した低電圧の差動 30Ω～55Ω ライン・ドライバおよびレシーバ
  - Type-1 レシーバは 25mV のヒステリシス付き
- バス I/O 保護
  - ±8kV HBM
  - ±8kV IEC 61000-4-2 接触放電
- ドライバ出力電圧の遷移時間制御による信号品質の向上
- -1V～3.4V の同相電圧範囲により、2V のグランド・ノイズでもデータ転送が可能
- ディセーブル時または V_{CC} ≤ 1.5V 時にバス・ピンが高インピーダンス
- 100Mbps デバイスも提供 (SN65MLVD202B)
- SN65MLVD203 への代替改善 [1]

2 アプリケーション

- 低消費電力、高速、短距離での TIA / EIA-485 の代替
- バックプレーンまたはケーブルによるマルチポイント・データおよびクロック転送
- 携帯基地局
- 中央局向けスイッチ
- ネットワーク・スイッチおよびルータ

3 概要

SN65MLVD203B デバイスは、最高 200Mbps の信号速度で動作するように最適化されたマルチポイント低電圧差動信号方式 (M-LVDS) ライン・ドライバおよびレシーバです。このデバイスは、堅牢な 3.3V ドライバおよびレシーバを標準の QFN フットプリントに搭載しており、要求の厳しい産業用アプリケーション向きです。バスのピンは ESD イベントに対して強化されており、人体モデルおよび IEC 接触放電仕様について高いレベルの保護を実現しています。

本デバイスは、差動ドライバと差動レシーバ (トランシーバ) を組み合わせた製品であり、3.3V の単一電源で動作します。このトランシーバは最高 200Mbps の信号速度で動作するように最適化されています。

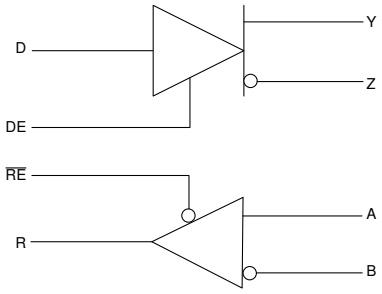
SN65MLVD203B は類似のデバイスよりも機能拡張されています。改良部分として、ドライバ出力のスルー・レート制御により無終端スタブからの反射を最小化し、シグナル・インテグリティ(信号品質)を強化する機能が挙げられます。これらのデバイスは、-40℃～125℃での動作が規定されています。

SN65MLVD203B M-LVDS トランシーバは、テキサス・インスツルメンツの幅広い M-LVDS ポートフォリオの一部です。

パッケージ情報[1]

部品番号	パッケージ	本体サイズ (公称)
SN65MLVD203B	RUM (WQFN、16)	4.00mm × 4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図、 SN65MLVD203B

[1] ラインの信号速度は 1 秒間に行われる電圧遷移回数で、bps (Bits Per Second) 単位で表されます。

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (November 2020) to Revision B (November 2022) — **Page**

- 製品情報表を「パッケージ情報」に変更 ... 1
- 「絶対最大定格」セクションの表の注を更新 ... 4
- 「ESD 定格」セクションで CDM テストを更新 ... 4
- Added *RX Maximum Jitter While DE Toggling* section ... 16
- Moved the *Power Supply Recommendations* and *Layout* sections to the *Application and Implementation* section ... 23

Changes from Revision * (September 2020) to Revision A (November 2020) — **Page**

- デバイスのステータスを「量産データ」に更新 ... 1
- 「電気的特性 - ドライバ」で、I_{IL} (min) を 0μA から -1μA に変更 ... 5
- 「電気的特性 - レシーバ」で、I_{IH} (max) を 0μA から 1μA に変更。 ... 7
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- 「スイッチング特性 – レシーバ」で、$t_{sk(p)}$ パルス・スキューの最大値を 300ps か 600ps に変更し、標準値を 100ps から 80ps に変更。 ... 8

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5 Pin Configuration and Functions

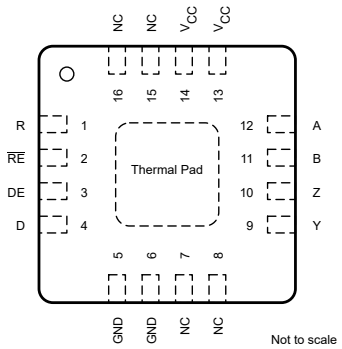

図 5-1. RUM Package, 16-Pin WQFN (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
R	1	Output	Receiver output
$\overline{RE}$	2	Input	Receiver enable pin; High = Disable, Low = Enable
DE	3	Input	Driver enable pin; High = Enable, Low = Disable
D	4	Input	Driver input
GND	5	Power	Supply ground
GND	6	Power	Supply ground
NC	7	NC	No internal connection
NC	8	NC	No internal connection
Y	9	Output	Differential output
Z	10	Output	Differential output
B	11	Input	Differential input
A	12	Input	Differential input
V_{CC}	13	Power	Power supply, 3.3 V
V_{CC}	14	Power	Power supply, 3.3 V
NC	15	NC	No internal connection
NC	16	NC	No internal connection
Thermal Pad		Power	Thermal pad. Connect to a solid ground plane.

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6 Specifications

6.1 絶対最大定格

自由気流での動作温度範囲内 (特に記述のない限り)(1)

		最小値	最大値	単位
電源電圧範囲、V_{CC} (2)		-0.5	4	V
入力電圧範囲	D、DE、$\overline{RE}$	-0.5	4	V
	A、B	-4	6	V
出力電圧範囲	R	-0.3	4	V
	Y、Z	-1.8	4	V
連続消費電力		熱に関する情報表を参照		
保存温度、T_{stg}		-65	150	℃

(1) 絶対最大定格の範囲外の動作は、デバイスの永続的な損傷の原因となる可能性があります。絶対最大定格は、このような条件や、「推奨動作条件」に記載されている条件を超える条件でデバイスが機能するということを意味するわけではありません。推奨動作条件の範囲外で絶対最大定格の範囲内で使用すると、デバイスが完全に機能しなくなる可能性があり、デバイスの信頼性、機能、性能に影響を及ぼし、デバイスの寿命を短縮する可能性があります。
(2) 差動 I/O バス電圧を除くすべての電圧値は、ネットワーク・グランド端子を基準にしています。

6.2 ESD 定格

				値	単位
$V_{(ESD)}$	静電放電	接触放電、IEC 61000-4-2 に準拠	A、B、Y、Z	±8000	V
		人体モデル (HBM)、ANSI / ESDA / JEDEC JS-001 に準拠、すべてのピン(1)	A、B、Y、Z	±8000	
			A、B、Y、Z を除くすべてのピン	±4000	
		デバイス帯電モデル (CDM)、JEDEC JS-002 準拠、すべてのピン(2)	すべてのピン	±1500	

(1) JEDEC のドキュメント JEP155 には、500V HBM であれば標準的な ESD 管理プロセスで安全な製造が可能であると記載されています。
(2) JEDEC のドキュメント JEP157 には、250V HBM であれば標準的な ESD 管理プロセスで安全な製造が可能であると記載されています。

6.3 推奨動作条件

自由気流での動作温度範囲内 (特に記述のない限り)

		最小値	公称値	最大値	単位
V_{CC}	電源電圧	3	3.3	3.6	V
V_{IH}	High レベル入力電圧	2		V_{CC}	V
V_{IL}	Low レベル入力電圧	0		0.8	V
	任意のバス端子 V_A、V_B、V_Y または V_Z の電圧	-1.4		3.8	V
$\|V_{ID}\|$	差動入力電圧の大きさ			V_{CC}	V
R_L	差動入力抵抗	30	50		Ω
$1/t_{UI}$	信号速度			200	Mbps
T_A	RUM パッケージの自由気流での動作温度	-40		125	℃

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6.4 熱に関する情報

熱評価基準(1)		SN65MLVD203B RUM (WQFN) 16 ピン	単位
$R_{\theta JA}$	接合部から周囲への熱抵抗	39.0	°C/W
$R_{\theta JC(top)}$	接合部からケース (上面) への熱抵抗	34.7	
$R_{\theta JB}$	接合部から基板への熱抵抗	17.7	
ψ_{JT}	接合部から上面への熱特性パラメータ	0.6	
ψ_{JB}	接合部から基板への熱特性パラメータ	17.7	
$R_{\theta JC(bot)}$	接合部からケース (底面) への熱抵抗	7.5	

(1) 従来および最新の熱評価基準の詳細については、『半導体および IC パッケージの熱評価基準』アプリケーション・レポートを参照してください。

6.5 電気的特性

推奨動作条件範囲内 (特に記述のない限り)(1)

パラメータ			テスト条件	最小値	代表値	最大値	単位
I_{CC}	電源電流	ドライバのみ	V_{CC} で $\overline{RE}$ および DE、R_L = 50Ω、その他はすべてオープン		13	22	mA
		両方ディセーブル	V_{CC} で $\overline{RE}$、0V で DE、R_L =無負荷、その他はすべてオープン		1	4	
		両方がイネーブル	0V で $\overline{RE}$、V_{CC} で DE、R_L = 50Ω、その他はすべてオープン		16	24	
		レシーバのみ	0V で $\overline{RE}$、0V で DE、その他はすべてオープン		4	13	
P_D	デバイス消費電力		R_L = 50Ω、D への入力は 50MHz 50% デューティ・サイクルの方形波、DE = High、$\overline{RE}$ = Low、T_A = 85℃			100	mW

(1) 標準値はすべて 25℃で、3.3V の電源電圧を使用します。

6.6 電気特性 - ドライバ

推奨動作条件範囲内 (特に記述のない限り)

パラメータ		テスト条件	最小値(1)	代表値(2)	最大値	単位
$\lvert V_{YZ}\rvert$	差動出力電圧の大きさ(4)	図 7-2 を参照	480		650	mV
$\Delta\lvert V_{YZ}\rvert$	ロジック状態間の差動出力電圧の大きさの変化		-50		50	mV
$V_{OS(SS)}$	定常同相出力電圧	図 7-3 を参照	0.8		1.2	V
$\Delta V_{OS(SS)}$	ロジック状態間での定常同相出力電圧の変化		-50		50	mV
$V_{OS(PP)}$	ピーク・ツー・ピークの同相出力電圧				150	mV
$V_{Y(OC)}$	最大定常断線出力電圧	図 7-7 を参照	0		2.4	V
$V_{Z(OC)}$	最大定常断線出力電圧		0		2.4	V
$V_{P(H)}$	電圧オーバーシュート、Low レベルから High レベルへの出力	図 7-5 を参照			$1.2V_{SS}$	V
$V_{P(L)}$	電圧オーバーシュート、High レベルから Low レベルへの出力		$-0.2\ V_{SS}$			V
I_{IH}	High レベル入力電流 (D、DE)	V_{IH} = 2V～V_{CC}	0		10	μA
I_{IL}	Low レベル入力電流 (D、DE)	V_{IL} = GND～0.8V	-1		10	μA
$\lvert I_{OS}\rvert$	差動短絡出力電流の大きさ	図 7-4 を参照			24	mA
I_{OZ}	高インピーダンス状態の出力電流 (ドライバのみ)	–1.4V ≤ (V_Y または V_Z) ≤ 3.8V、その他の出力 = 1.2V	-15		10	μA
$I_{O(OFF)}$	電源オフ出力電流	–1.4V ≤ (V_Y または V_Z) ≤ 3.8V、その他の出力 = 1.2V、0V ≤ V_{CC}≤ 1.5V	-10		10	μA

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推奨動作条件範囲内 (特に記述のない限り)

パラメータ		テスト条件	最小値(1)	代表値(2)	最大値	単位
C_Y または C_Z	出力容量	V_I = 0.4sin (30E6πt) + 0.5 V、(3) その他の入力は 1.2V、ドライバはディセーブル		6		pF
C_{YZ}	差動出力容量	V_{AB} = 0.4sin (30E6πt) V、(3) ドライバはディセーブル		4.5		pF
$C_{Y/Z}$	出力容量バランス、(C_Y/C_Z)		0.98		1.02	

(1) このデータシートでは、最も小さい正 (最も大きな負の) 制限を最小として指定する代数的規約を使用します。
(2) 標準値はすべて 25℃で、3.3V の電源電圧を使用します。
(3) HP4194A インピーダンス・アナライザ (または同等のもの)
(4) 測定機器の精度は、-40℃で 10mV です

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6.7 電気特性 - レシーバ

推奨動作条件範囲内 (特に記述のない限り)

パラメータ			テスト条件	最小値	代表値 (1)	最大値	単位
V_{IT+}	正方向の差動入力電圧スレッショルド(2)	タイプ 1	図 7-9 および表 7-1 を参照			50	mV
V_{IT-}	負方向の差動入力電圧スレッショルド(2)	タイプ 1		-50			mV
V_{HYS}	差動入力電圧ヒステリシス ($V_{IT+} – V_{IT–}$)	タイプ 1			25		mV
V_{OH}	High レベル出力電圧 (R)		I_{OH} = –8mA	2.4			V
V_{OL}	Low レベル出力電圧 (R)		I_{OL} = 8mA			0.4	V
I_{IH}	High レベル入力電流 ($\overline{RE}$)		V_{IH} = 2V～V_{CC}	-10		1	µA
I_{IL}	Low レベル入力電流 ($\overline{RE}$)		V_{IL} = GND～0.8V	-10		0	µA
I_{OZ}	高インピーダンス出力電流 (R)		V_O = 0V または 3.6V	-10		15	µA
C_A または C_B	入力容量		$_I$ = 0.4sin (30E6πt) + 0.5 V(3)、その他の入力は 1.2V		6		pF
C_{AB}	差動入力容量		V_{AB} = 0.4sin (30E6πt) V(3)		4.5		pF
$C_{A/B}$	入力容量バランス、(C_A/C_B)			0.94		1.06	

(1) 標準値はすべて 25℃で、3.3V の電源電圧を使用します。
(2) 測定機器の精度は、-40℃で 10mV です
(3) HP4194A インピーダンス・アナライザ (または同等のもの)

6.8 スイッチング特性 – ドライバ

推奨動作条件範囲内 (特に記述のない限り)

パラメータ		テスト条件	最小値	代表値 (1)	最大値	単位
t_{pLH}	伝搬遅延時間、出力立ち上がり	図 7-5 を参照	2	2.5	3.5	ns
t_{pHL}	伝搬遅延時間、出力立ち下がり		2	2.5	3.5	ns
t_r	差動出力信号の立ち上がり時間			2.0		ns
t_f	差動出力信号の立ち下がり時間			2.0		ns
$t_{sk(pp)}$	部品間スキュー(2)				0.9	ns
$t_{jit(per)}$	周期ジッタ、rms (1 標準偏差)(3)	62.5MHz クロック入力(4)			5	ps
$t_{jit(per)}$	周期ジッタ、rms (1 標準偏差)(3)	100MHz クロック入力(4)			2	ps
$t_{jit(pp)}$	ピーク・ツー・ピーク・ジッタ(3) (6)	125Mbps 8b10b 入力(5)			250	ps
$t_{jit(pp)}$	ピーク・ツー・ピーク・ジッタ(3) (6)	200Mbps 8b10b 入力(5)			325	ps
$t_{jit(pp)}$	ピーク・ツー・ピーク・ジッタ(3) (6)	200Mbps 2^{15} –1 PRBS 入力(5)			325	ps
t_{PHZ}	ディセーブル時間、High レベルから高インピーダンスへの出力	図 7-6 を参照		5	7	ns
t_{PLZ}	ディセーブル時間、Low レベルから高インピーダンスへの出力			5	7	ns
t_{PZH}	イネーブル時間、高インピーダンスから High レベルへの出力			4	7	ns
t_{PZL}	イネーブル時間、高インピーダンスから Low レベルへの出力			4	7	ns

(1) 標準値はすべて 25℃で、3.3V の電源電圧を使用します。
(2) 部品間スキューは、同じ V / T 条件で動作する 2 つのデバイス間の伝搬遅延の差として定義されます。
(3) ジッタは、設計と特性によって保証されています。スティミュラスのジッタがこの数値から減算されました。
(4) t_r = t_f = 0.5ns (10%～90%)、30K を超えるサンプルで測定。
(5) t_r = t_f = 0.5ns (10%～90%)、100K を超えるサンプルで測定。
(6) ピーク・ツー・ピーク・ジッタには、パルス・スキュー ($t_{sk(p)}$) によるジッタが含まれます。

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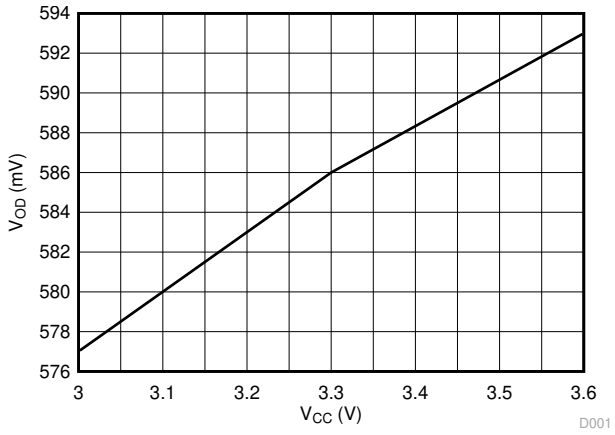
6.9 スイッチング特性 – レシーバ

推奨動作条件範囲内 (特に記述のない限り)

パラメータ			テスト条件	最小値	代表値 (1)	最大値	単位
t_{PLH}	伝搬遅延時間、出力立ち上がり		C_L = 15pF、図 7-10 を参照	2	6	10	ns
t_{PHL}	伝搬遅延時間、出力立ち下がり			2	6	10	ns
t_r	出力信号の立ち上がり時間					2.3	ns
t_f	出力信号の立ち下がり時間					2.3	ns
$t_{sk(p)}$	パルス・スキュー ($\lvert t_{pHL} - t_{pLH} \rvert$)	タイプ 1	C_L = 15pF、図 7-10 を参照		80	600	ps
$t_{sk(pp)}$	部品間スキュー(2)		C_L = 15pF、図 7-10 を参照			1	ns
$t_{jit(per)}$	周期ジッタ、rms (1 標準偏差)(3)		62.5MHz クロック入力(4)			5	ps
$t_{jit(per)}$	周期ジッタ、rms (1 標準偏差)(3)		100MHz クロック入力(4)			3	ps
$t_{jit(pp)}$	ピーク・ツー・ピーク・ジッタ(3) (6)	タイプ 1	125Mbps 8b10b 入力(5)			130	ps
$t_{jit(pp)}$	ピーク・ツー・ピーク・ジッタ(3) (6)	タイプ 1	200Mbps 8b10b 入力(5)			250	ps
$t_{jit(pp)}$	ピーク・ツー・ピーク・ジッタ(3) (6)	タイプ 1	200Mbps 2^{15} –1 PRBS 入力(5)			300	ps
t_{PHZ}	ディセーブル時間、High レベルから高インピーダンスへの出力		図 7-11 を参照		6	10	ns
t_{PLZ}	ディセーブル時間、Low レベルから高インピーダンスへの出力				6	10	ns
t_{PZH}	イネーブル時間、高インピーダンスから High レベルへの出力				10	15	ns
t_{PZL}	イネーブル時間、高インピーダンスから Low レベルへの出力				10	15	ns

(1) 標準値はすべて 25℃で、3.3V の電源電圧を使用します。
(2) 部品間スキューは、同じ V / T 条件で動作する 2 つのデバイス間の伝搬遅延の差として定義されます。
(3) ジッタは、設計と特性によって保証されています。スティミュラスのジッタがこの数値から減算されました。
(4) V_{ID} = 200mV_{pp} 、V_{cm} = 1V、t_r = t_f = 0.5ns (10%～90%)、30K を超えるサンプルで測定。
(5) V_{ID} = 200mV_{pp} 、V_{cm} = 1 V、t_r = t_f = 0.5ns (10%～90%)、100K を超えるサンプルで測定。
(6) ピーク・ツー・ピーク・ジッタには、パルス・スキュー ($t_{sk(p)}$) によるジッタが含まれます

6.10 Typical Characteristics



T_A = 25°C

図 6-1. Differential Output Voltage vs Supply Voltage

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7 Parameter Measurement Information

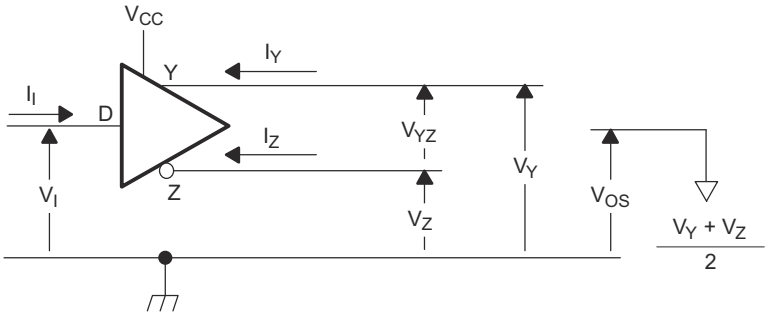
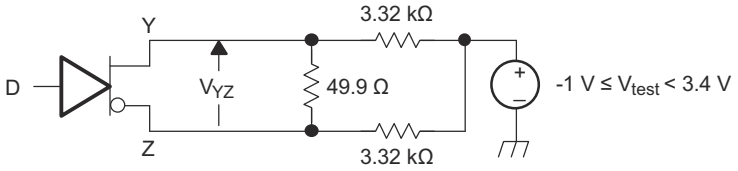
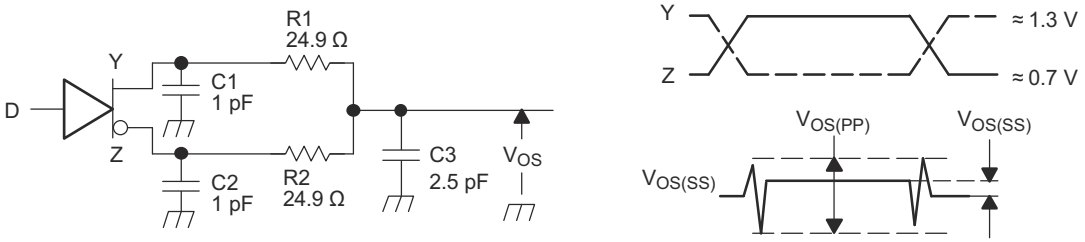


図 7-1. Driver Voltage and Current Definitions



A. All resistors are 1% tolerance.

図 7-2. Differential Output Voltage Test Circuit



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f≤ 1 ns, pulse frequency = 1 MHz, duty cycle = 50 ± 5%.
B. C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.
C. R1 and R2 are metal film, surface mount, ±1%, and located within 2 cm of the D.U.T.
D. The measurement of $V_{OS(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

図 7-3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

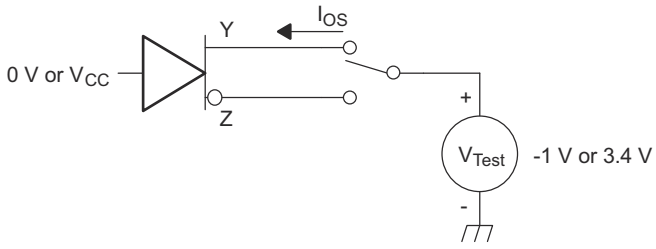


図 7-4. Driver Short-Circuit Test Circuit

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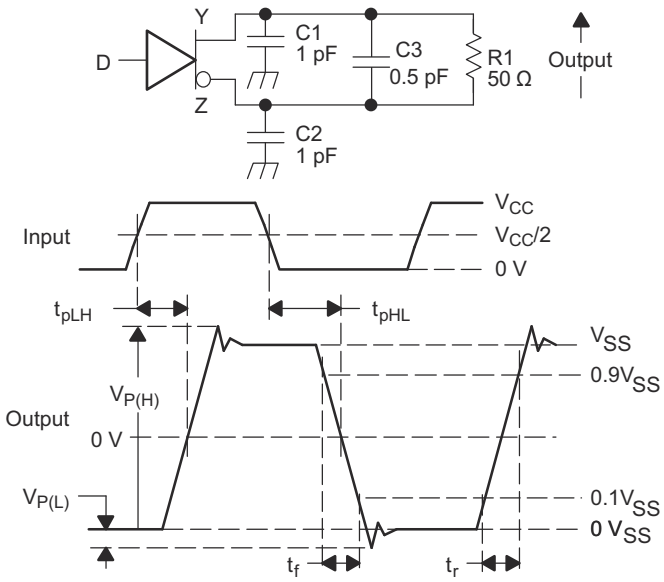
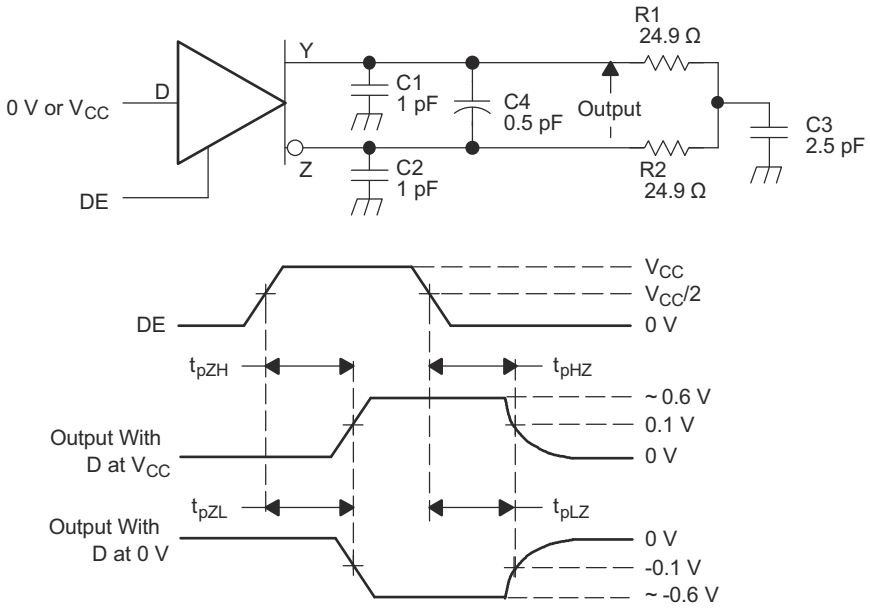


A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f≤ 1 ns, frequency = 1 MHz, duty cycle = 50 ± 5%.
B. C1, C2, and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.
C. R1 is a metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
D. The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

図 7-5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f≤ 1 ns, frequency = 1 MHz, duty cycle = 50 ± 5%.
B. C1, C2, C3, and C4 includes instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.
C. R1 and R2 are metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
D. The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

図 7-6. Driver Enable and Disable Time Circuit and Definitions

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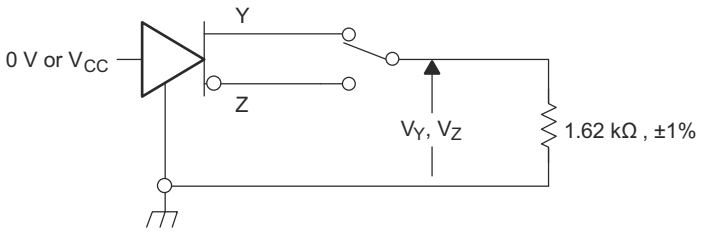
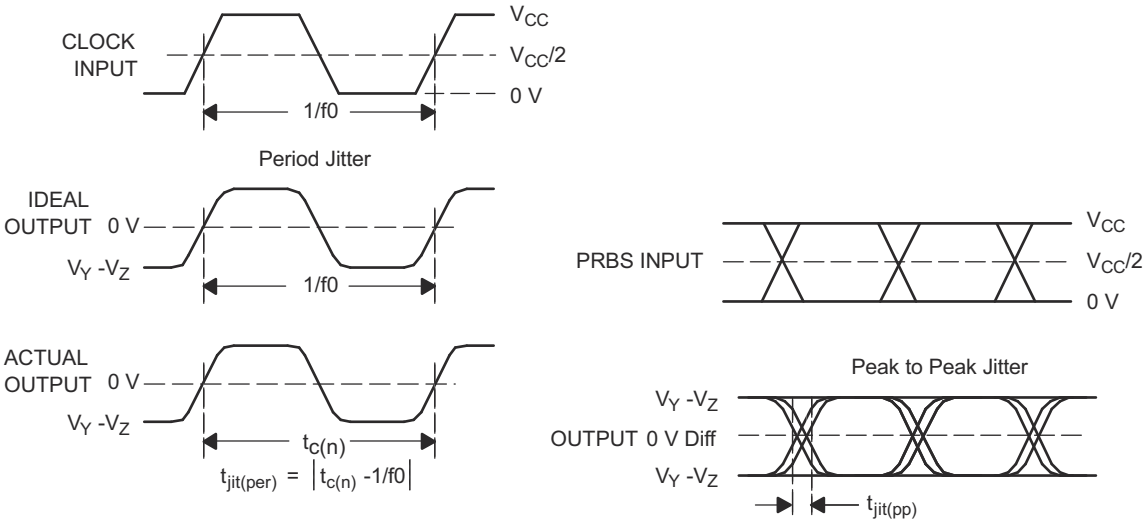


図 7-7. Maximum Steady State Output Voltage



A. All input pulses are supplied by an Agilent 81250 Stimulus System.
B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
C. Period jitter is measured using a 100 MHz 50 ±1% duty cycle clock input.
D. Peak-to-peak jitter is measured using a 200 Mbps 2^{15}–1 PRBS input.

図 7-8. Driver Jitter Measurement Waveforms

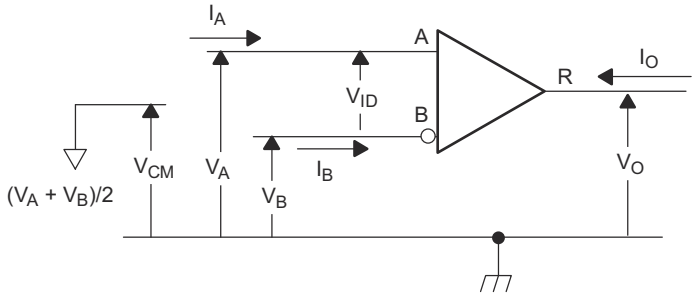


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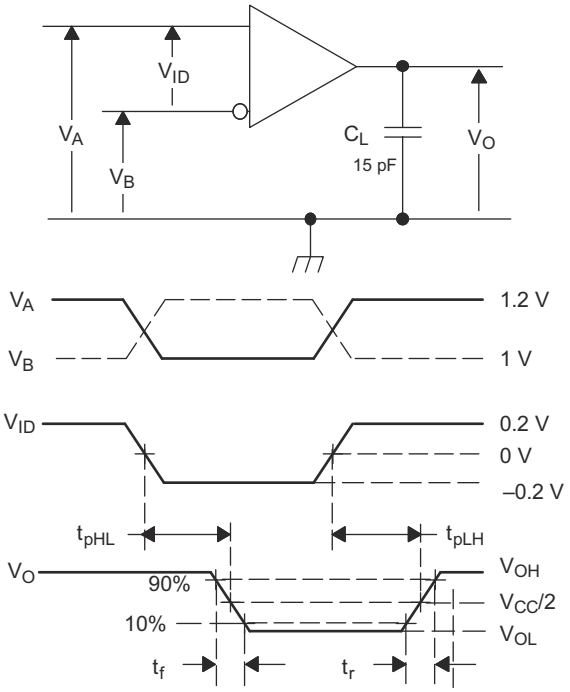
図 7-9. Receiver Voltage and Current Definitions

表 7-1. Type-1 Receiver Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	RECEIVER OUTPUT
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	–2.400	1.200	L
3.425	3.375	0.050	3.4	H
3.375	3.425	–0.050	3.4	L
–0.975	–1.025	0.050	–1	H
–1.025	–0.975	–0.050	–1	L



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, frequency = 1 MHz, duty cycle = 50 ± 5%. C_L is a combination of a 20%-tolerance, low-loss ceramic, surface-mount capacitor and fixture capacitance within 2 cm of the D.U.T.

B. The measurement is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

図 7-10. Receiver Timing Test Circuit and Waveforms

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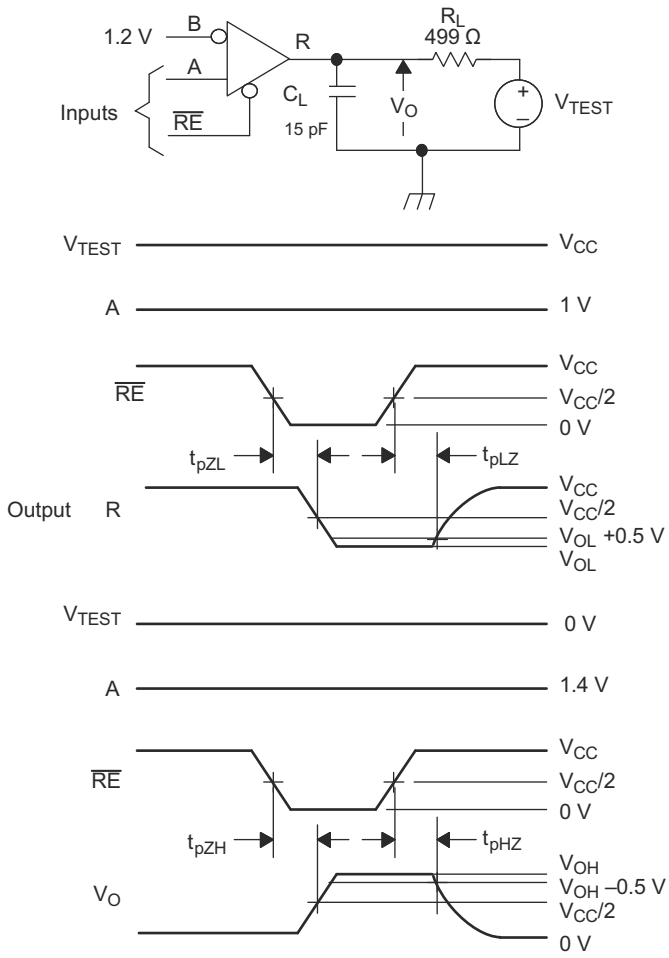

A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, frequency = 1 MHz, duty cycle = 50 ± 5%.
B. R_L is 1% tolerance, metal film, surface mount, and located within 2 cm of the D.U.T.
C. C_L is the instrumentation and fixture capacitance within 2 cm of the DUT and ±20%.

図 7-11. Receiver Enable and Disable Time Test Circuit and Waveforms

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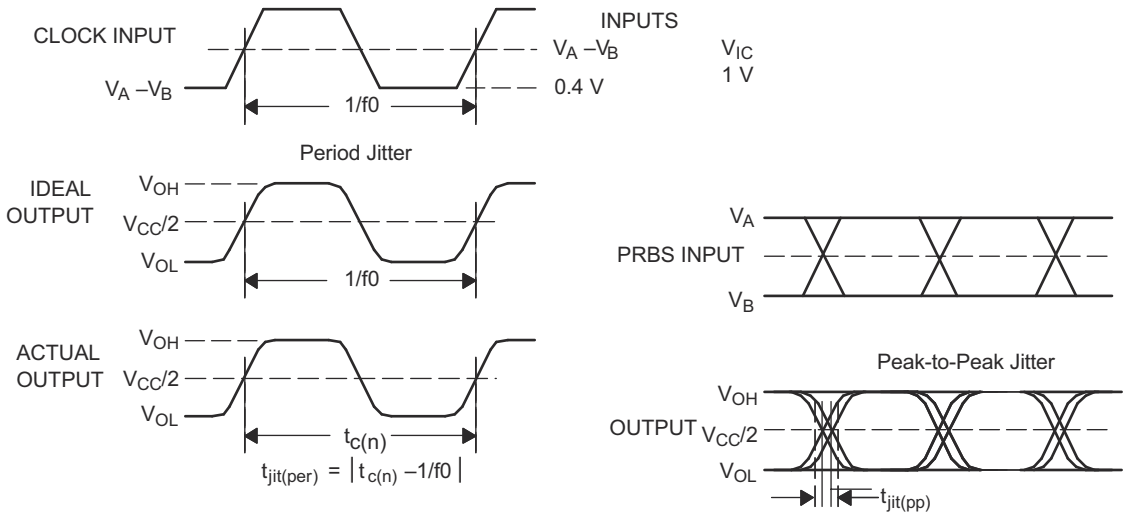

A. All input pulses are supplied by an Agilent 8304A Stimulus System.
B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
C. Period jitter is measured using a 10 MHz 50 ±1% duty cycle clock input.
D. Peak-to-peak jitter is measured using a 200 Mbps 2^{15}-1 PRBS input.

図 7-12. Receiver Jitter Measurement Waveforms

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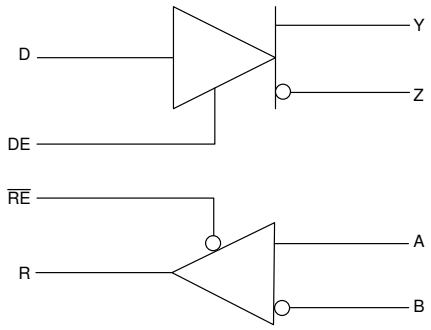
8 Detailed Description

8.1 Overview

The SN65MLVD203B is a multipoint-low-voltage differential (M-LVDS) line driver and receiver, which is optimized to operate at signaling rates up to 200 Mbps. the device complies with the multipoint low-voltage differential signaling (M-LVDS) standard TIA/EIA-899. These circuit is similar to the TIA/EIA-644 standard compliant LVDS counterpart, with added features to address multipoint applications. The driver output has been designed to support multipoint buses presenting loads as low as 30 Ω, and incorporates controlled transition times to allow for stubs off of the backbone transmission line.

The SN65MLVD203B has a Type-1 receivers exhibit 25 mV of differential input voltage hysteresis to prevent output oscillations with slowly changing signals or loss of input.

8.2 Functional Block Diagrams



8.3 Feature Description

8.3.1 Power-On-Reset

The SN65MLVD203B operates and meets all the specified performance requirements for supply voltages in the range of 3 V to 3.6 V. When the supply voltage drops below 1.5 V (or is turning on and has not yet reached 1.5 V), power-on reset circuitry set the driver output to a high-impedance state.

8.3.2 ESD Protection

The bus terminals of the SN65MLVD203B possess on-chip ESD protection against ±8-kV human body model (HBM) and ±8-kV IEC61000-4-2 contact discharge. The IEC-ESD test is far more severe than the HBM-ESD test. The 50% higher charge capacitance, CS, and 78% lower discharge resistance, R_D of the IEC model produce significantly higher discharge currents than the HBM-model.

As stated in the IEC 61000-4-2 standard, contact discharge is the preferred test method; although IEC air-gap testing is less repeatable than contact testing, air discharge protection levels are inferred from the contact discharge test results.

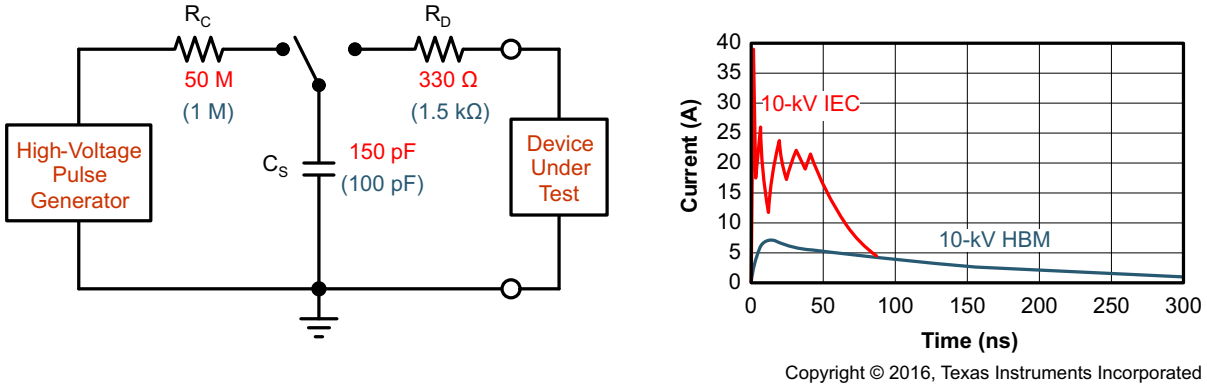


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図 8-1. HBM and IEC-ESD Models and Currents in Comparison (HBM Values in Parenthesis)

8.3.3 RX Maximum Jitter While DE Toggling

Due to the internal circuitry of the Receiver and Driver Enable/Disable (DE), toggling the DE pin disrupts the biasing of the receiver and results in a current change. This current change adds jitter to the receiver. If the DE pin is toggled, the maximum peak-to-peak jitter of the receiver is estimated to be 2.1 ns.

8.4 Device Functional Modes

8.4.1 Operation with V_{CC} < 1.5 V

Bus pins are high impedance under this condition.

8.4.2 Operations with 1.5 V ≤ V_{CC} < 3 V

Operation with supply voltages in the range of 1.5 V ≤ V_{CC} < 3 V is undefined and no specific device performance is guaranteed in this range.

8.4.3 Operation with 3 V ≤ V_{CC} < 3.6 V

Operation with the supply voltages greater than or equal to 3 V and less than or equal to 3.6 V is normal operation.

8.4.4 Device Function Tables

表 8-1. Type-1 Receiver

INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
V_{ID} ≥ 50 mV	L	H
-50 mV < V_{ID} < 50 mV	L	?
V_{ID} ≤ -50 mV	L	L
X	H	Z
X	Open	Z

表 8-2. Driver

INPUTS	ENABLE	OUTPUTS	
D	DE	X	Y
L	H	L	H
H	H	H	L
Open	H	L	H
X	Open	Z	Z
X	L	Z	Z

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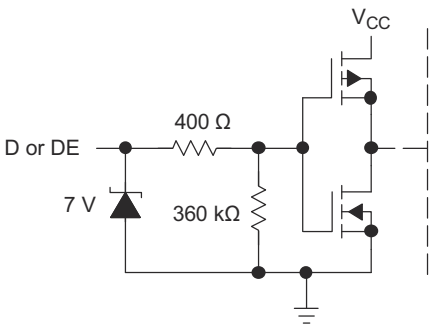
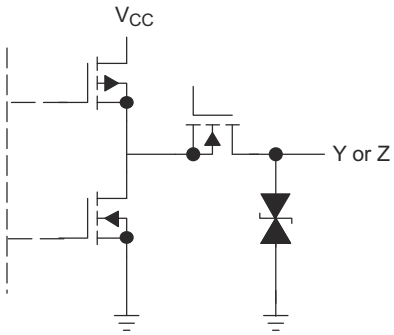
8.4.5 Equivalent Input and Output Schematic Diagrams

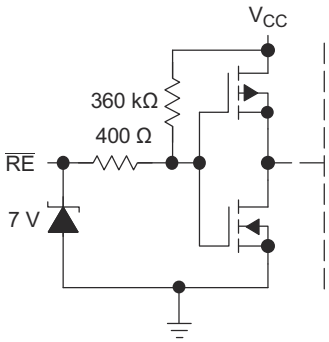
DRIVER INPUT AND DRIVER ENABLE



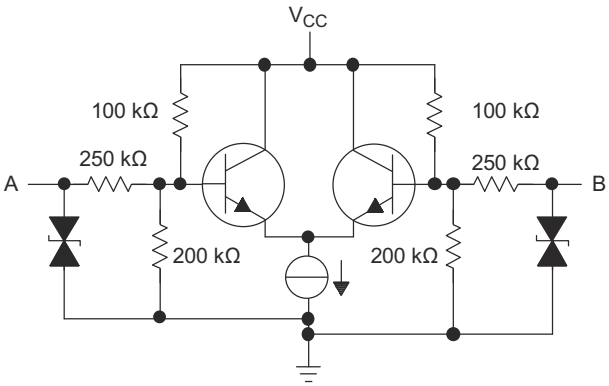
DRIVER OUTPUT



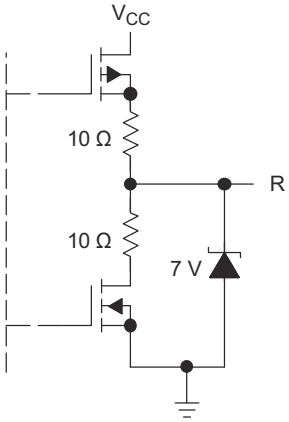
RECEIVER ENABLE



RECEIVER INPUT



RECEIVER OUTPUT



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9 Application and Implementation

注

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9.1 Application Information

The SN65MLVD203B is a multipoint line driver and receiver. The functionality of the device is simple, yet extremely flexible, leading to their use in designs ranging from wireless base stations to desktop computers.

9.2 Typical Application

9.2.1 Multipoint Communications

In a multipoint configuration many transmitters and many receivers can be interconnected on a single transmission line. The key difference compared to multi-drop is the presence of two or more drivers. Such a situation creates contention issues that need not be addressed with point-to-point or multidrop systems. Multipoint operation allows for bidirectional, half-duplex communication over a single balanced media pair. To support the location of the various drivers throughout the transmission line, double termination of the transmission line is now necessary.

The major challenge that system designers encounter are the impedance discontinuities that device loading and device connections (stubs) introduce on the common bus. Matching the impedance of the loaded bus and using signal drivers with controlled signal edges are the keys to error-free signal transmissions in multipoint topologies.

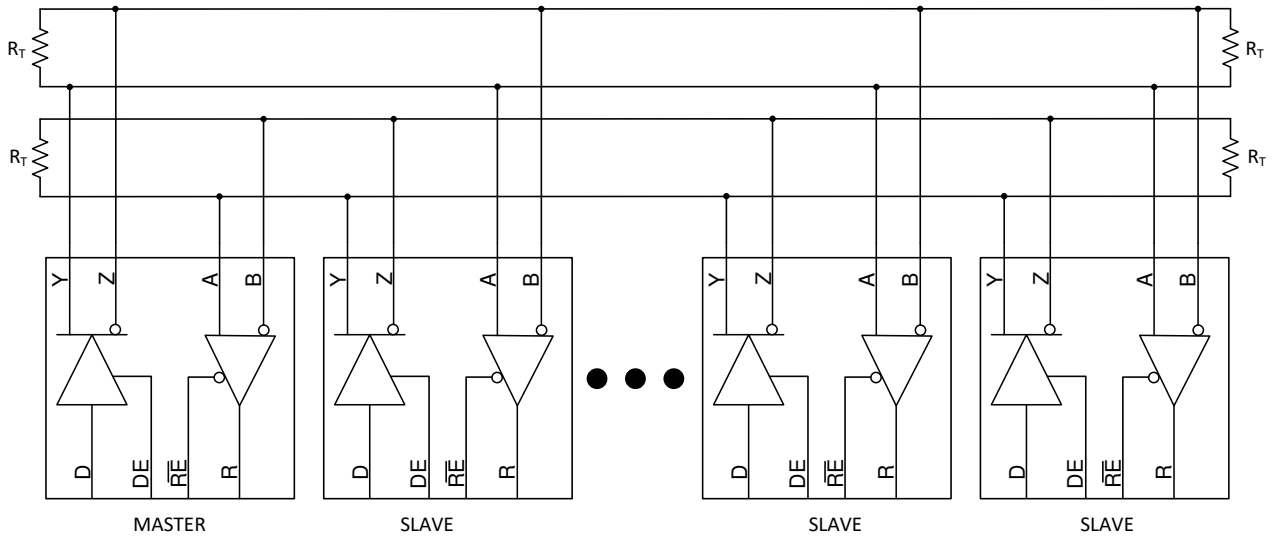

図 9-1. Multipoint Configuration

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9.2.2 Design Requirements

For this design example, use the parameters listed in 表 9-1.

表 9-1. Design Parameters

PARAMETERS	VALUES
Driver supply voltage	3 to 3.6 V
Driver input voltage	0.8 to 3.3 V
Driver signaling rate	DC to 200 Mbps
Interconnect characteristic impedance	100 Ω
Termination resistance (differential)	100 Ω
Number of receiver nodes	2 to 32
Receiver supply voltage	3 to 3.6 V
Receiver input voltage	0 to (V_{CC} – 0.8) V
Receiver signaling rate	DC to 200 Mbps
Ground shift between driver and receiver	±1 V

9.2.3 Detailed Design Procedure

9.2.3.1 Supply Voltage

The SN65MLVD203B is operated from a single supply. The device can support operations with a supply as low as 3 V and as high as 3.6 V.

9.2.3.2 Supply Bypass Capacitance

Bypass capacitors play a key role in power distribution circuitry. At low frequencies, power supply offers very low-impedance paths between its terminals. However, as higher frequency currents propagate through power traces, the source is often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10 µF to 1000 µF) at the board level do a good job up into the kHz range. Due to their size and length of their leads, large capacitors tend to have large inductance values at the switching frequencies. To solve this problem, smaller capacitors (in the nF to µF range) must be installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because their lead inductance is about 1 nH. For comparison purposes, a typical capacitor with leads has a lead inductance around 5 nH.

The value of the bypass capacitors used locally with M-LVDS chips can be determined by 式 1 and 式 2, according to *High Speed Digital Design – A Handbook of Black Magic* by Howard Johnson and Martin Graham (1993). A conservative rise time of 4 ns and a worst-case change in supply current of 100 mA covers the whole range of M-LVDS devices offered by Texas Instruments. In this example, the maximum power supply noise tolerated is 100 mV; however, this figure varies depending on the noise budget available for the design.

$$C_{chip} = \left(\frac{\Delta I_{\text{Maximum Step Change Supply Current}}}{\Delta V_{\text{Maximum Power Supply Noise}}} \right) \times T_{\text{Rise Time}} \tag{1}$$

$$C_{MLVDS} = \left(\frac{100\ \text{mA}}{100\ \text{mV}} \right) \times 4\,\text{ns} = 0.004\ \mu\text{F} \tag{2}$$

図 9-2 shows a configuration that lowers lead inductance and covers intermediate frequencies between the board-level capacitor (>10 µF) and the value of capacitance found above (0.004 µF). Place the smallest value of capacitance as close as possible to the chip.

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図 9-2. Recommended M-LVDS Bypass Capacitor Layout

9.2.3.3 Driver Input Voltage

The input stage accepts LVTTL signals. The driver operates with a decision threshold of approximately 1.4 V.

9.2.3.4 Driver Output Voltage

The driver outputs a steady state common mode voltage of 1 V with a differential signal of 540 mV under nominal conditions.

9.2.3.5 Termination Resistors

As shown earlier, an M-LVDS communication channel employs a current source driving a transmission line which is terminated with two resistive loads. These loads serve to convert the transmitted current into a voltage at the receiver input. To ensure good signal integrity, the termination resistors should be matched to the characteristic impedance of the transmission line. The designer should ensure that the termination resistors are within 10% of the nominal media characteristic impedance. If the transmission line is targeted for 100-Ω impedance, the termination resistors should be between 90 Ω and 110 Ω. The line termination resistors are typically placed at the ends of the transmission line.

9.2.3.6 Receiver Input Signal

The M-LVDS receivers herein comply with the M-LVDS standard and correctly determine the bus state. These devices have Type-1 and Type-2 receivers that detect the bus state with as little as 50 mV of differential voltage over the common mode range of –1 V to 3.4 V.

9.2.3.7 Receiver Input Threshold (Failsafe)

The MLVDS standard defines a Type-1 and Type-2 receiver. Type-1 receivers have their differential input voltage thresholds near zero volts. Type-2 receivers have their differential input voltage thresholds offset from 0 V to detect the absence of a voltage difference. The impact to receiver output by the offset input can be seen in 表 9-2 and 図 9-3.

表 9-2. Receiver Input Voltage Threshold Requirements

RECEIVER TYPE	OUTPUT LOW	OUTPUT HIGH
Type 1	$-2.4\ V \le V_{ID} \le -0.05\ V$	$0.05\ V \le V_{ID} \le 2.4\ V$
Type 2	$-2.4\ V \le V_{ID} \le 0.05\ V$	$0.15\ V \le V_{ID} \le 2.4\ V$

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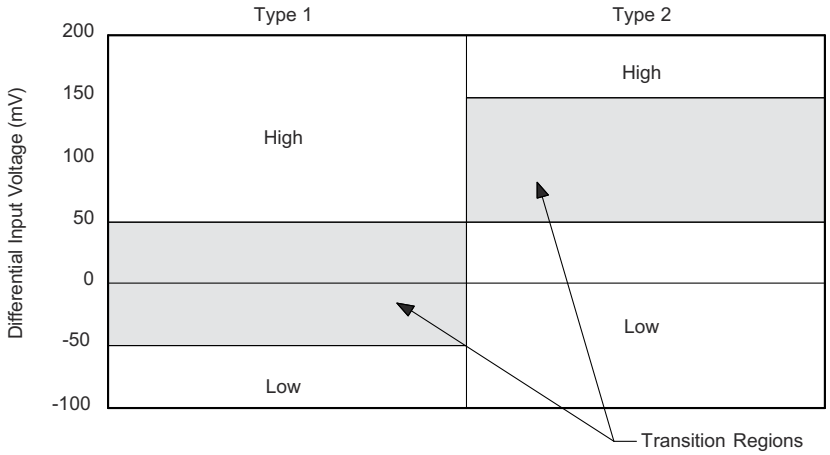

図 9-3. Expanded Graph of Receiver Differential Input Voltage Showing Transition Region

9.2.3.8 Receiver Output Signal

Receiver outputs comply with LVTTL output voltage standards when the supply voltage is within the range of 3 V to 3.6 V.

9.2.3.9 Interconnecting Media

The physical communication channel between the driver and the receiver may be any balanced paired metal conductors meeting the requirements of the M-LVDS standard, the key points which will be included here. This media may be a twisted pair, twinax, flat ribbon cable, or PCB traces.

The nominal characteristic impedance of the interconnect should be between 100 Ω and 120 Ω with variation no more than 10% (90 Ω to 132 Ω).

9.2.3.10 PCB Transmission Lines

As per SNLA187, 図 9-4 depicts several transmission line structures commonly used in printed-circuit boards (PCBs). Each structure consists of a signal line and a return path with uniform cross-section along its length. A microstrip is a signal trace on the top (or bottom) layer, separated by a dielectric layer from its return path in a ground or power plane. A stripline is a signal trace in the inner layer, with a dielectric layer in between a ground plane above and below the signal trace. The dimensions of the structure along with the dielectric material properties determine the characteristic impedance of the transmission line (also called controlled-impedance transmission line).

When two signal lines are placed close by, they form a pair of coupled transmission lines. 図 9-4 shows examples of edge-coupled microstrips, and edge-coupled or broad-side-coupled striplines. When excited by differential signals, the coupled transmission line is referred to as a differential pair. The characteristic impedance of each line is called odd-mode impedance. The sum of the odd-mode impedances of each line is the differential impedance of the differential pair. In addition to the trace dimensions and dielectric material properties, the spacing between the two traces determines the mutual coupling and impacts the differential impedance. When the two lines are immediately adjacent; for example, if S is less than 2 × W, the differential pair is called a tightly-coupled differential pair. To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length, as well as maintain good symmetry between the two lines.

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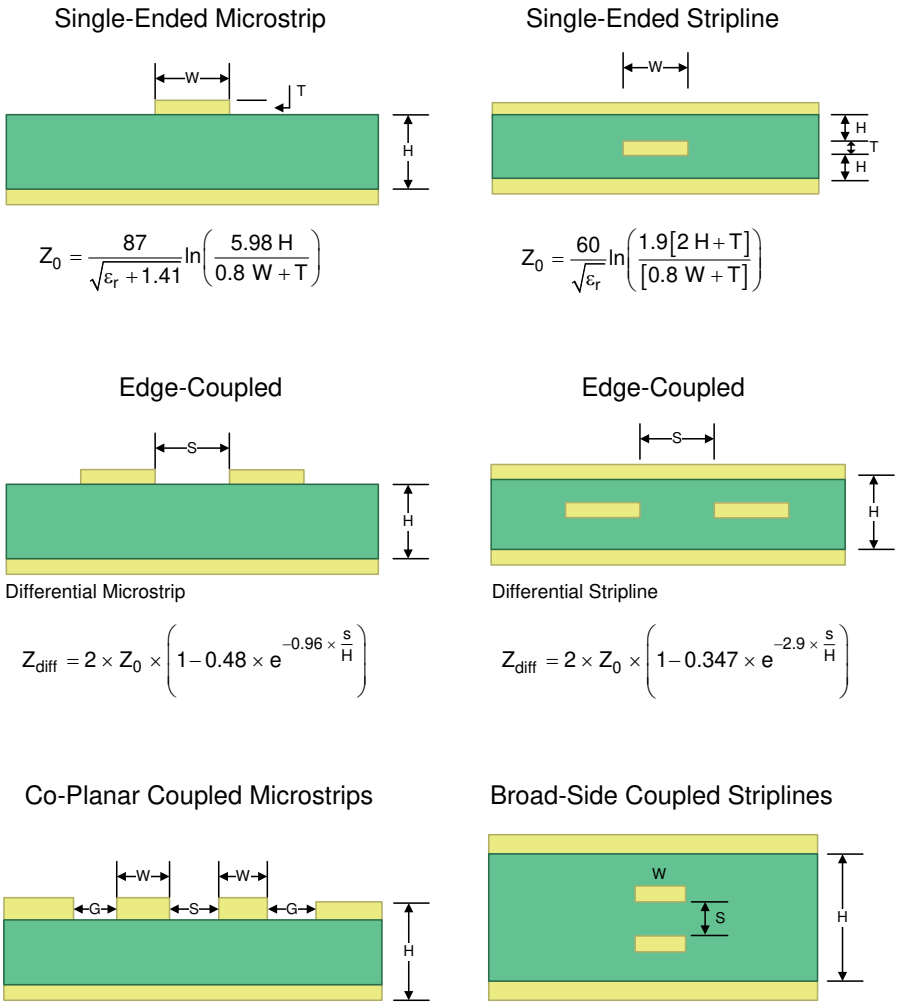
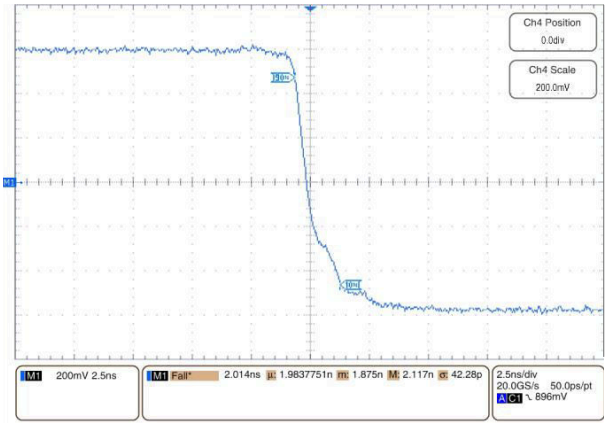


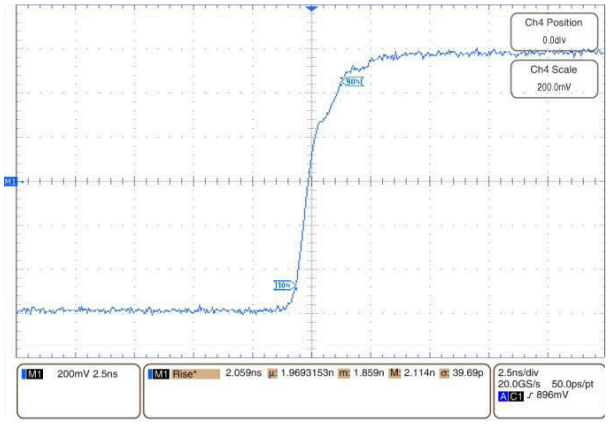
図 9-4. Controlled-Impedance Transmission Lines

9.2.4 Application Curves



V_{CC} = 3.3 V T_A = 25°C

図 9-5. Driver Fall Time



V_{CC} = 3.3 V T_A = 25°C

図 9-6. Driver Rise Time

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9.3 Power Supply Recommendations

The M-LVDS driver and receivers in this data sheet are designed to operate from a single power supply. Both drivers and receivers operate with supply voltages in the range of 3 V to 3.6 V. In a typical application, a driver and a receiver may be on separate boards, or even separate equipment. In these cases, separate supplies would be used at each location. The expected ground potential difference between the driver power supply and the receiver power supply would be less than ±1 V. Board level and local device level bypass capacitance should be used and are covered Supply Bypass Capacitance.

9.4 Layout

9.4.1 Layout Guidelines

9.4.1.1 Microstrip vs. Stripline Topologies

As per SLLD009, printed-circuit boards usually offer designers two transmission line options: Microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in 図 9-7.

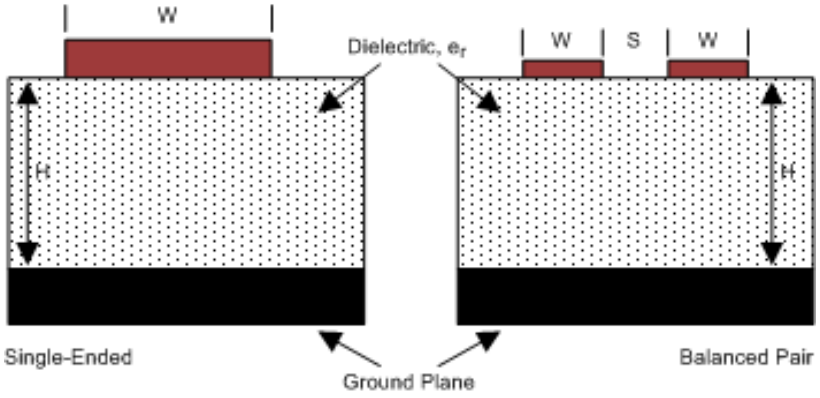

図 9-7. Microstrip Topology

On the other hand, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing M-LVDS signals on microstrip transmission lines if possible. The PCB traces allow designers to specify the necessary tolerances for Z_O based on the overall noise budget and reflection allowances. Footnotes 1[2], 2[3], and 3[4] provide formulas for Z_O and t_{PD} for differential and single-ended traces. [2] [3] [4]

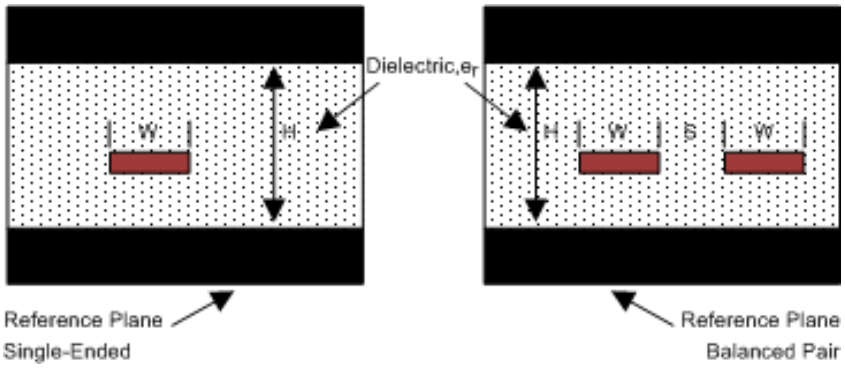

図 9-8. Stripline Topology

[2] Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.
[3] Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.
[4] Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

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9.4.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with M-LVDS signals. If rise or fall times of TTL/CMOS signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited. Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving M-LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz
- All exposed circuitry should be solder-plated (60/40) to 7.62 µm or 0.0003 in (minimum).
- Copper plating should be 25.4 µm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

9.4.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, you must decide how many levels to use in the stack. To reduce the TTL/CMOS to M-LVDS crosstalk, it is a good practice to have at least two separate signal planes as shown in 図 9-9.

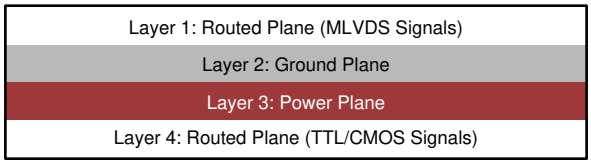

図 9-9. Four-Layer PCB Board

注

The separation between layers 2 and 3 should be 127 µm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

One of the most common stack configurations is the six-layer board, as shown in 図 9-10.

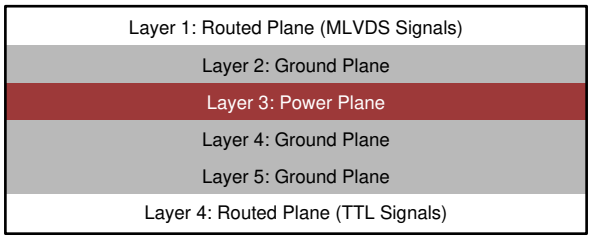

図 9-10. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity; however, fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

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9.4.1.4 Separation Between Traces

The separation between traces depends on several factors; however, the amount of coupling that can be tolerated usually dictates the actual separation. Low noise coupling requires close coupling between the differential pair of an M-LVDS link to benefit from the electromagnetic field cancellation. The traces should be 100-Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

In the case of two adjacent single-ended traces, one should use the 3-W rule, which stipulates that the distance between two traces must be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent M-LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

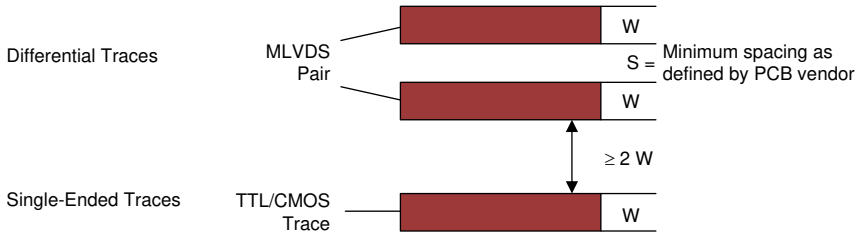

図 9-11. 3-W Rule for Single-Ended and Differential Traces (Top View)

You should exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

9.4.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

9.4.1.6 Decoupling

Each power or ground lead of a high-speed device should be connected to the PCB through a low inductance path. For best results, one or more vias are used to connect a power or ground pin to the nearby plane. Ideally, via placement is immediately adjacent to the pin to avoid adding trace inductance. Placing a power plane closer to the top of the board reduces the effective via length and its associated inductance.

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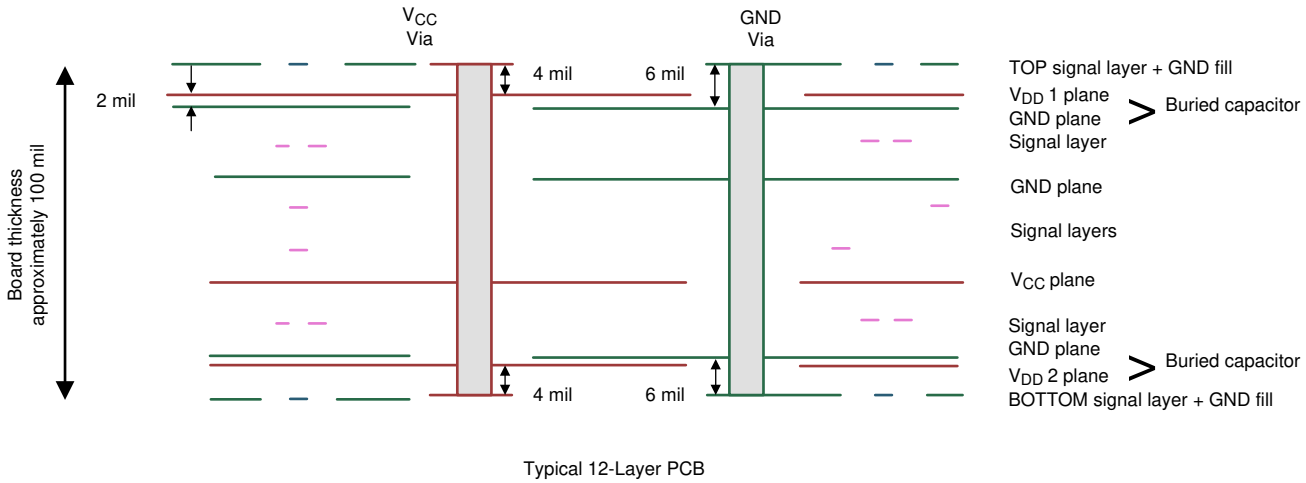
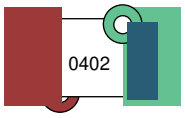


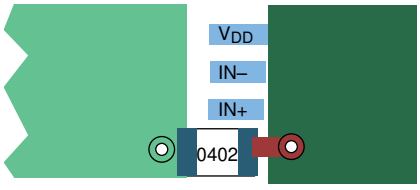
図 9-12. Low Inductance, High-Capacitance Power Connection

Bypass capacitors should be placed close to V_{DD} pins. They can be placed conveniently near the corners or underneath the package to minimize the loop area. This extends the useful frequency range of the added capacitance. Small-physical-size capacitors, such as 0402, 0201, or X7R surface-mount capacitors should be used to minimize body inductance of capacitors. Each bypass capacitor is connected to the power and ground plane through vias tangent to the pads of the capacitor as shown in 図 9-13(a).

An X7R surface-mount capacitor of size 0402 has about 0.5 nH of body inductance. At frequencies above 30 MHz or so, X7R capacitors behave as low-impedance inductors. To extend the operating frequency range to a few hundred MHz, an array of different capacitor values like 100 pF, 1 nF, 0.03 µF, and 0.1 µF are commonly used in parallel. The most effective bypass capacitor can be built using sandwiched layers of power and ground at a separation of 2 to 3 mils. With a 2-mil FR4 dielectric, there is approximately 500 pF per square inch of PCB. Many high-speed devices provide a low-inductance GND connection on the backside of the package. This center pad must be connected to a ground plane through an array of vias. The via array reduces the effective inductance to ground and enhances the thermal performance of the small Surface Mount Technology (SMT) package. Placing vias around the perimeter of the pad connection ensures proper heat spreading and the lowest possible die temperature. Placing high-performance devices on opposing sides of the PCB using two GND planes (as shown in 図 9-4) creates multiple paths for heat transfer. Often thermal PCB issues are the result of one device adding heat to another, resulting in a very high local temperature. Multiple paths for heat transfer minimize this possibility. In many cases the GND pad makes the optimal decoupling layout impossible to achieve due to insufficient pad-to-pad spacing as shown in 図 9-13(b). When this occurs, placing the decoupling capacitor on the backside of the board keeps the extra inductance to a minimum. It is important to place the V_{DD} via as close to the device pin as possible while still allowing for sufficient solder mask coverage. If the via is left open, solder may flow from the pad and into the via barrel. This will result in a poor solder connection.



Typical Decoupling Capacitor Layouts(a)



Typical Decoupling Capacitor Layouts(b)

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9.4.2 Layout Example

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in 図 9-13.

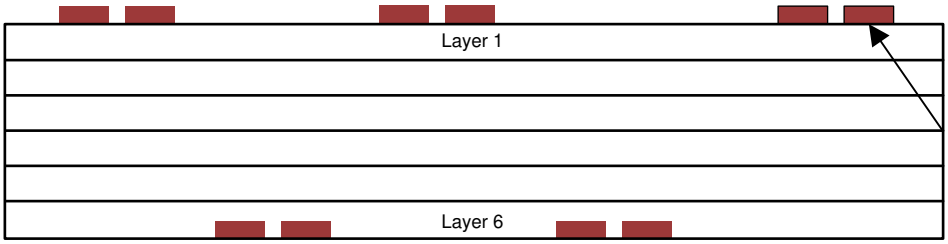

図 9-13. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers; thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in 図 9-14. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

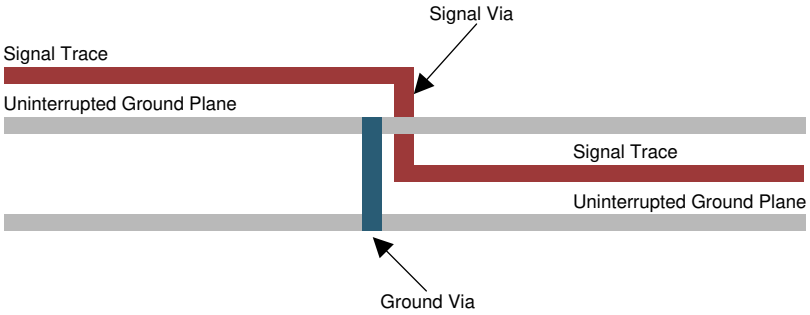

図 9-14. Ground Via Location (Side View)

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For releated documentation, see the following:

1. Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.
2. Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.
3. Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65MLVD203BRUMR	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	MLVD 203B
SN65MLVD203BRUMR.B	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	MLVD 203B
SN65MLVD203BRUMRG4	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MLVD 203B
SN65MLVD203BRUMRG4.B	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MLVD 203B
SN65MLVD203BRUMT	Active	Production	WQFN (RUM) | 16	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	MLVD 203B
SN65MLVD203BRUMT.B	Active	Production	WQFN (RUM) | 16	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	MLVD 203B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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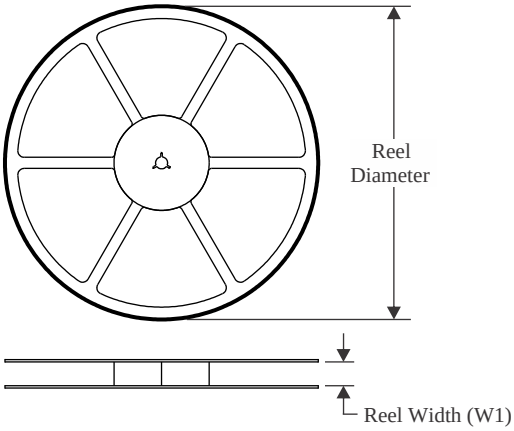
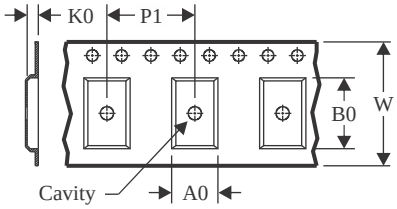
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

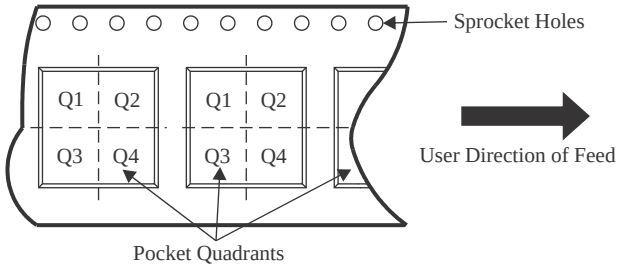


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

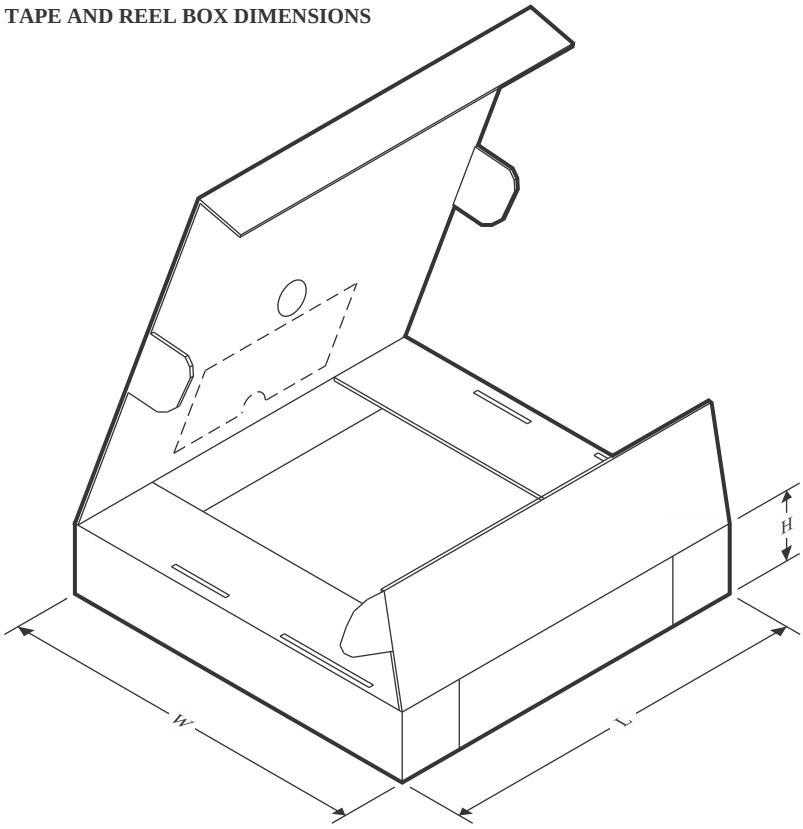
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65MLVD203BRUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN65MLVD203BRUMRG4	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN65MLVD203BRUMT	WQFN	RUM	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65MLVD203BRUMR	WQFN	RUM	16	3000	360.0	360.0	36.0
SN65MLVD203BRUMRG4	WQFN	RUM	16	3000	367.0	367.0	35.0
SN65MLVD203BRUMT	WQFN	RUM	16	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

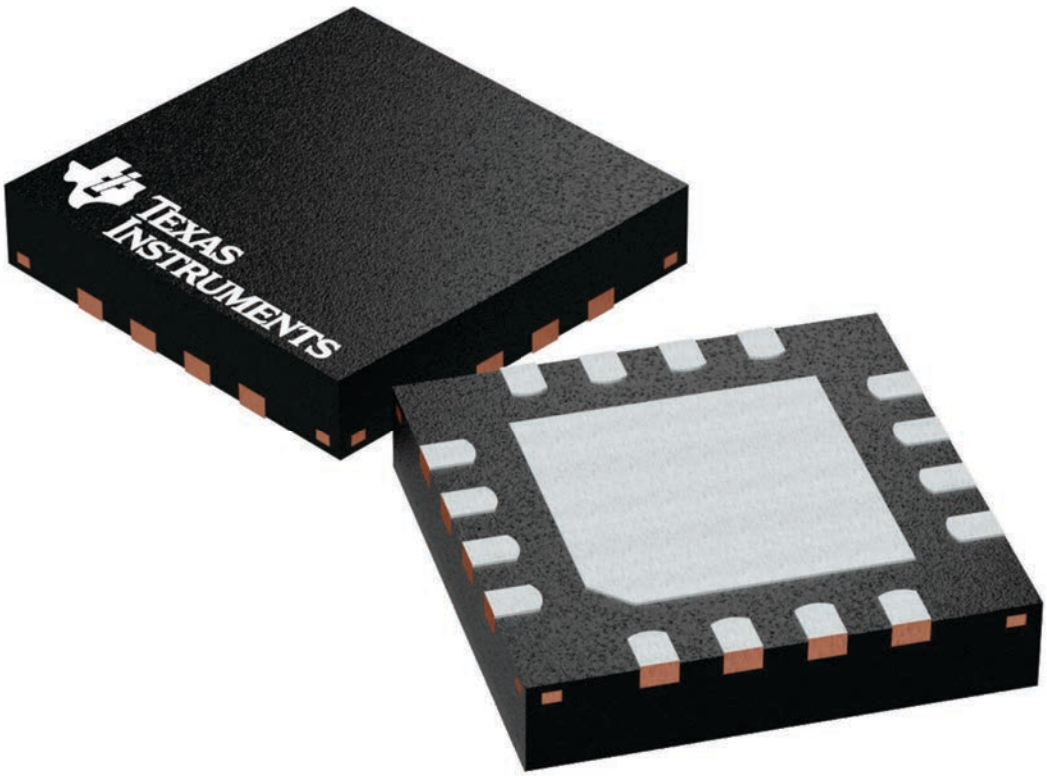
RUM 16

WQFN - 0.8 mm max height

4 x 4, 0.65 mm pitch

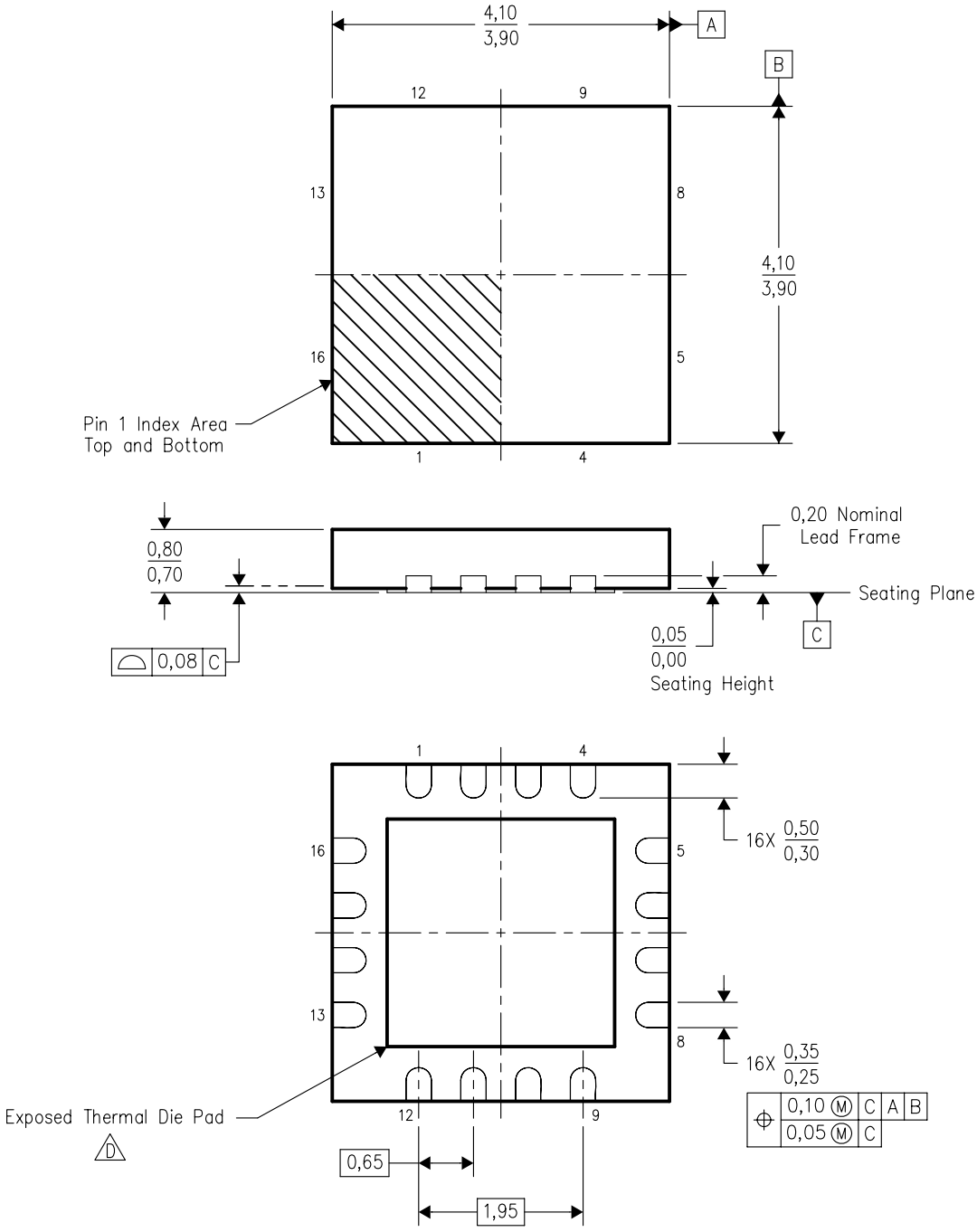
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224843/A

RUM (S–PQFP–N16) PLASTIC QUAD FLATPACK



4209092/A 10/2007

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–220 variation WGGC–3.

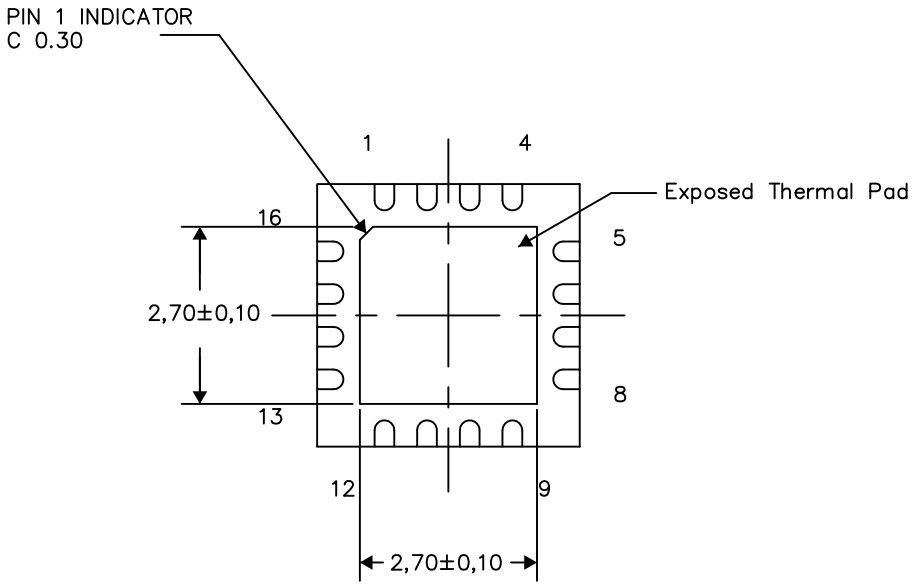
RUM (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4209093–2/F 09/15

NOTES: All linear dimensions are in millimeters

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