TEXAS INSTRUMENTS
SN54AHC574, SN74AHC574
JAJSV21K – OCTOBER 1995 – REVISED JULY 2024

# SNx4AHC574 3 ステート出力、オクタル エッジ トリガ D タイプ フリップ フロップ

## 1 特長

- 2V～5.5V の $V_{CC}$ で動作
- 3 ステート出力はバス ラインを直接駆動
- JESD 17 準拠で 250mA 超のラッチアップ性能
- MIL-PRF-38535 準拠の製品については、特に記述のない限り、すべてのパラメータはテスト済みです。その他のすべての製品については、量産プロセスにすべてのパラメータのテストが含まれているとは限りません。
- JESD 22 を超える ESD 保護
  - 人体モデルで 2000V
  - 荷電デバイス モデルで 1000V

## 2 アプリケーション

- スマート グリッド
- テレビ
- セットトップ ボックス
- オーディオ
- サーバー
- 監視カメラ
- ネットワーク スイッチ
- インフォテインメント

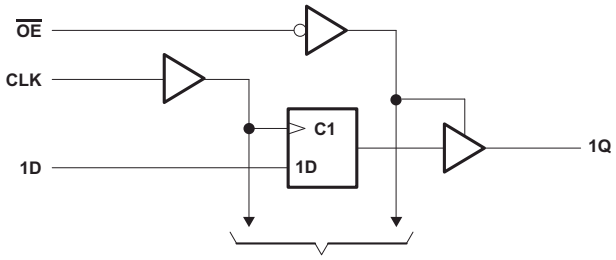
## 3 概要

SNx4AHC574 デバイスは、オクタル エッジ トリガ D タイプ フリップフロップで、大きい容量性負荷または比較的低いインピーダンスの負荷の駆動用に設計された 3 ステート出力を備えています。特に、バッファ レジスタ、I/O ポート、双方向バスドライバ、作業レジスタの実装に適しています。

**製品情報**

| 部品番号 | パッケージ (1) | パッケージ サイズ(2) | 本体サイズ (3) |
|---|---|---|---|
| SNx4AHC574 | DB (SSOP、20) | 7.2mm × 7.8mm | 7.50mm × 5.30mm |
| | DGV (TVSOP、20) | 5.00mm × 6.4mm | 5.00mm × 4.40mm |
| | DW (SOIC、20) | 12.80mm × 10.3mm | 12.8mm × 7.5mm |
| | N (PDIP、20) | 24.33mm × 9.4mm | 25.40mm × 6.35mm |
| | PW (TSSOP、20) | 6.50mm × 6.4mm | 6.50mm × 4.40mm |

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。




**概略回路図**

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

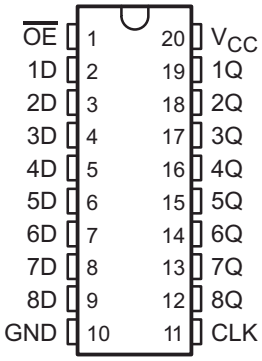
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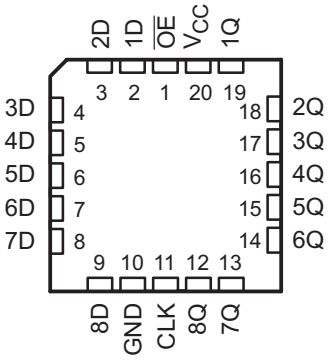

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# 4 Pin Configuration and Functions

**SN54AHC574 . . . J OR W PACKAGE**
**SN74AHC574 . . . DB, DGV, DW, N, NS, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC574 . . . FK PACKAGE**
**(TOP VIEW)**




| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | $\overline{OE}$ | I | Output Enable Pin |
| 2 | 1D | I | 1D Input |
| 3 | 2D | I | 2D Input |
| 4 | 3D | I | 3D Input |
| 5 | 4D | I | 4D Input |
| 6 | 5D | I | 5D Input |
| 7 | 6D | I | 6D Input |
| 8 | 7D | I | 7D Input |
| 9 | 8D | I | 8D Input |
| 10 | GND | — | Ground Pin |
| 11 | CLK | I | Clock Pin |
| 12 | 8Q | O | 8Q Output |
| 13 | 7Q | O | 7Q Output |
| 14 | 6Q | O | 6Q Output |
| 15 | 5Q | O | 5Q Output |
| 16 | 4Q | O | 4Q Output |
| 17 | 3Q | O | 3Q Output |
| 18 | 2Q | O | 2Q Output |
| 19 | 1Q | O | 1Q Output |
| 20 | $V_{CC}$ | — | Power Pin |

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 7 | V |
| $V_O$ | Output voltage range(2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 or $V_O$ > $V_{CC}$ | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±75 | mA |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *セクション 5.3* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | SN54AHC574 | | SN74AHC574 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level Input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | µA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | µA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |


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over operating free-air temperature range (unless otherwise noted)(1)

| | | SN54AHC574 | | SN74AHC574 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

## 5.4 Thermal Information

| THERMAL METRIC(1) | | SN74AHC574 | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | DB | DGV | DW | N | NS | PW | |
| | | 20 PINS | | | | | | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 97.9 | 117.2 | 81.1 | 53.3 | 79.2 | 116.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 59.6 | 32.7 | 48.9 | 40.0 | 45.7 | 58.5 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 53.1 | 58.7 | 53.8 | 34.2 | 46.8 | 78.7 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 21.3 | 1.15 | 19.5 | 26.4 | 19.3 | 12.6 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 52.7 | 58.0 | 53.1 | 34.1 | 46.4 | 77.9 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | N/A | N/A | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC574 | | SN74AHC574 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | –40°C to 85°C | | –40°C to 85°C | | –40°C to 125°C | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 2 V | | | 0.1 | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OH}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | | 0.44 | |
| | $I_{OH}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | | 0.44 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1(1) | | ±1 | | ±1 | µA |
| $I_{OZ}$ (2) | $V_O = V_{CC}$ or GND<br>$V_I$ ( $\overline{OE}$) = $V_{IL}$ or $V_{IH}$ | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | | ±2.5 | µA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | | 40 | µA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 3 | 10 | | | | 10 | | 10 | pF |
| $C_O$ | $V_O = V_{CC}$ or GND | 5 V | | 3 | | | | | | | | pF |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC}$ = 0 V.
(2) For input and output pins, $I_{OZ}$ includes the input leakage current.

## 5.6 Timing Requirements, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | | $T_A$ = 25°C | | SN54AHC574 | | SN74AHC574 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | –40°C to 85°C | | –40°C to 85°C | | –40°C to 125°C | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, CLK high or low | 5 | | 5 | | 5 | | 5.5 | | ns |

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over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | | $T_A$ = 25°C | | SN54AHC574 | | SN74AHC574 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | –40°C to 85°C | | –40°C to 85°C | | –40°C to 125°C | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{su}$ | Setup time, data before CLK ↑ | 3.5 | | 3.5 | | 3.5 | | 4 | | ns |
| $t_h$ | Hold time, data after CLK ↑ | 1.5 | | 1.5 | | 1.5 | | 2 | | ns |

## 5.7 Timing Requirements, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | | $T_A$ = 25°C | | SN54AHC574 | | SN74AHC574 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | –40°C to 85°C | | –40°C to 85°C | | –40°C to 125°C | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, CLK high or low | 5 | | 5 | | 5 | | 5.5 | | ns |
| $t_{su}$ | Setup time, data before CLK ↑ | 3 | | 3 | | 3 | | 3.5 | | ns |
| $t_h$ | Hold time, data after CLK ↑ | 1.5 | | 1.5 | | 1.5 | | 2 | | ns |

## 5.8 Switching Characteristics, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC574 | | SN74AHC574 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | –40°C to 85°C | | –40°C to 85°C | | –40°C to 125°C | | |
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{MAX}$ | | | $C_L$ = 15 pF | 80[1] | 125[1] | | 65[1] | | 65 | | 65 | | MHz |
| | | | $C_L$ = 50 pF | 50 | 75 | | 45 | | 45 | | 45 | | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15 pF | | 8.5[1] | 13.2[1] | 1[1] | 15.5[1] | 1 | 15.5 | 1 | 17 | ns |
| $t_{PHL}$ | | | | | 8.5[1] | 13.2[1] | 1[1] | 15.5[1] | 1 | 15.5 | 1 | 17 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 8.2[1] | 12.8[1] | 1[1] | 15[1] | 1 | 15 | 1 | 16 | ns |
| $t_{PZL}$ | | | | | 8.2[1] | 12.8[1] | 1[1] | 15[1] | 1 | 15 | 1 | 16 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 8.5[1] | 13[1] | 1[1] | 15[1] | 1 | 15 | 1 | 16 | ns |
| $t_{PLZ}$ | | | | | 8.5[1] | 13[1] | 1[1] | 15[1] | 1 | 15 | 1 | 16 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 11 | 16.7 | 1 | 19 | 1 | 19 | 1 | 20.5 | ns |
| $t_{PHL}$ | | | | | 11 | 16.7 | 1 | 19 | 1 | 19 | 1 | 20.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 10.7 | 16.3 | 1 | 18.5 | 1 | 18.5 | 1 | 19.5 | ns |
| $t_{PZL}$ | | | | | 10.7 | 16.3 | 1 | 18.5 | 1 | 18.5 | 1 | 19.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 11 | 15 | 1 | 17 | 1 | 17 | 1 | 18 | ns |
| $t_{PLZ}$ | | | | | 11 | 15 | 1 | 17 | 1 | 17 | 1 | 18 | |
| $t_{sk(o)}$ | | | $C_L$ = 50 pF | | | 1.5[2] | | | | | | 1.5 | ns |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

## 5.9 Switching Characteristics, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC574 | | SN74AHC574 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | –40°C to 85°C | | –40°C to 85°C | | –40°C to 125°C | | |
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{MAX}$ | | | $C_L$ = 15 pF | 130[1] | 180[1] | | 110[1] | | 110 | | 110 | | MHz |
| | | | $C_L$ = 50 pF | 85 | 115 | | 75 | | 75 | | 75 | | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15 pF | | 5.6[1] | 8.6[1] | 1[1] | 10[1] | 1 | 10 | 1 | 11 | ns |
| $t_{PHL}$ | | | | | 5.6[1] | 8.6[1] | 1[1] | 10[1] | 1 | 10 | 1 | 11 | |


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over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC574 | | SN74AHC574 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | –40°C to 85°C | | –40°C to 85°C | | –40°C to 125°C | | |
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5.9[1] | 9[1] | 1[1] | 10.5[1] | 1 | 10.5 | 1 | 11.5 | ns |
| $t_{PZL}$ | | | | | 5.9[1] | 9[1] | 1[1] | 10.5[1] | 1 | 10.5 | 1 | 11.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5.5[1] | 9[1] | 1[1] | 10.5[1] | 1 | 10.5 | 1 | 11.5 | ns |
| $t_{PLZ}$ | | | | | 5.5[1] | 9[1] | 1[1] | 10.5[1] | 1 | 10.5 | 1 | 11.5 | |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 7.1 | 10.6 | 1 | 12 | 1 | 12 | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 7.1 | 10.6 | 1 | 12 | 1 | 12 | 1 | 13 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 7.4 | 11 | 1 | 12.5 | 1 | 12.5 | 1 | 13.5 | ns |
| $t_{PZL}$ | | | | | 7.4 | 11 | 1 | 12.5 | 1 | 12.5 | 1 | 13.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 7.1 | 10.1 | 1 | 11.5 | 1 | 11.5 | 1 | 12.5 | ns |
| $t_{PLZ}$ | | | | | 7.1 | 10.1 | 1 | 11.5 | 1 | 11.5 | 1 | 12.5 | |
| $t_{sk(o)}$ | | | $C_L$ = 50 pF | | | 1[2] | | | | 1 | | 1 | ns |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

## 5.10 Noise Characteristics

$V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C[1]

| PARAMETER | | SN74AHC574 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.2 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 1.5 | V |

(1) Characteristics are for surface-mount packages only.

## 5.11 Operating Characteristics

$V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 28 | pF |

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## 5.12 Typical Characteristics

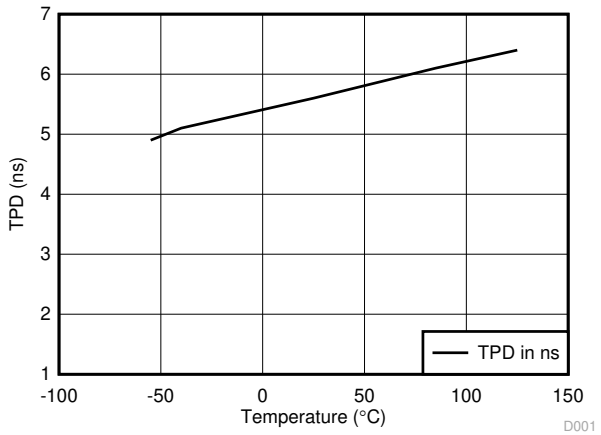



**図 5-1. TPD vs Temperature**

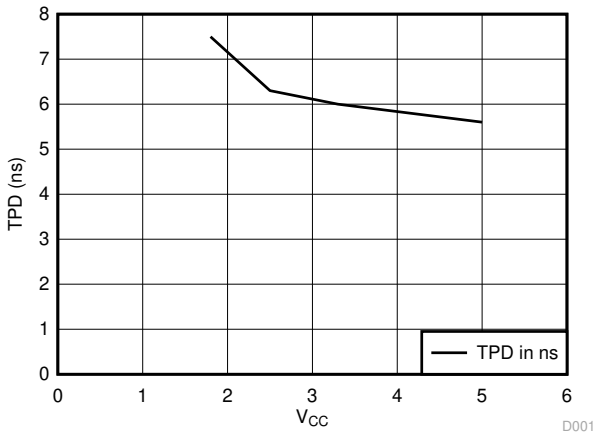
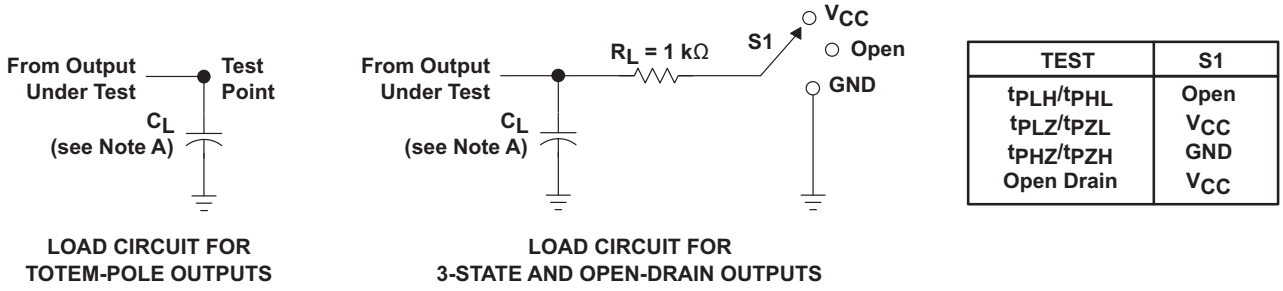



**図 5-2. TPD vs $V_{CC}$ at 25°C**

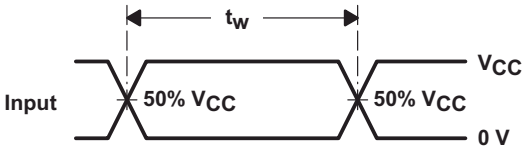

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# 6 Parameter Measurement Information

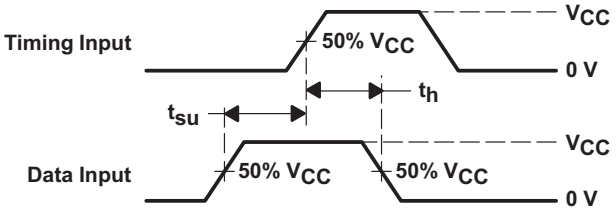



LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

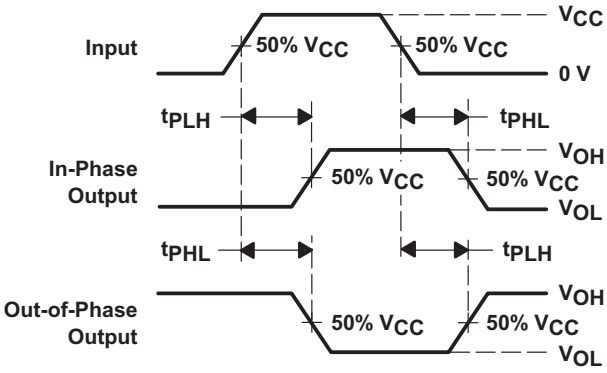
LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



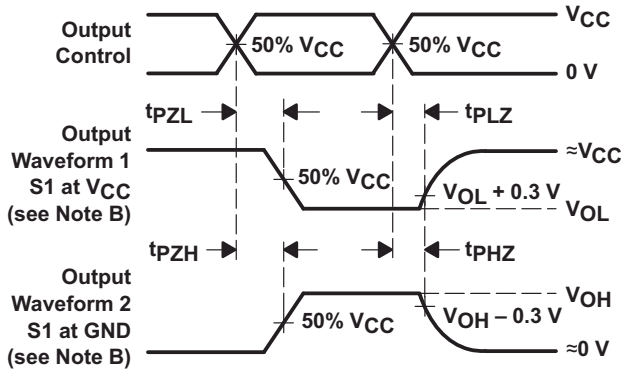

VOLTAGE WAVEFORMS PULSE DURATION




VOLTAGE WAVEFORMS SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

**図 6-1. Load Circuit and Voltage Waveforms**

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# 7 Detailed Description

## 7.1 Overview

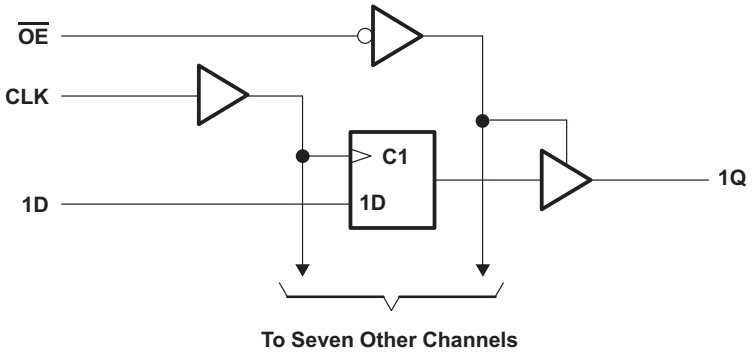
The SNx4AHC574 devices are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

The states of the Q outputs are not predictable until the first valid clock.

A buffered output-enable ( $\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pull-up components.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

- 5.5-V tolerant input allows for 5 V to 3.3 V voltage translation
- Slow edges reduce output ringing

## 7.4 Device Functional Modes

**表 7-1. Function Table (Each Flip-Flop)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | $Q_0$ |
| H | X | X | Z |


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# 8 Application and Implementation

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## 8.1 Application Information

SN74AHC574 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid $V_{CC}$ making it Ideal for down translation

## 8.2 Typical Application

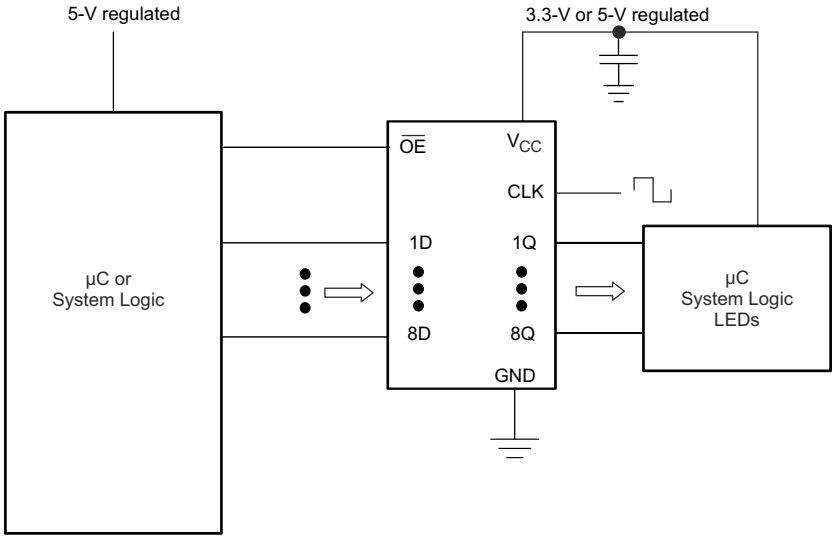



**図 8-1. Typical Application Schematic**

### *8.2.1 Design Requirements*

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

### *8.2.2 Detailed Design Procedure*

1. Recommended Input Conditions
   - For rise time and fall time specifications, see Δt/ΔV in the *セクション 5.3* table.
   - For specified High and low levels, see $V_{IH}$ and $V_{IL}$ in the *セクション 5.3* table.
2. Recommend Output Conditions
   - Load currents should not exceed 25 mA per output and 75 mA total for the part.
   - Outputs should not be pulled above $V_{CC}$.

### 8.2.3 Application Curves

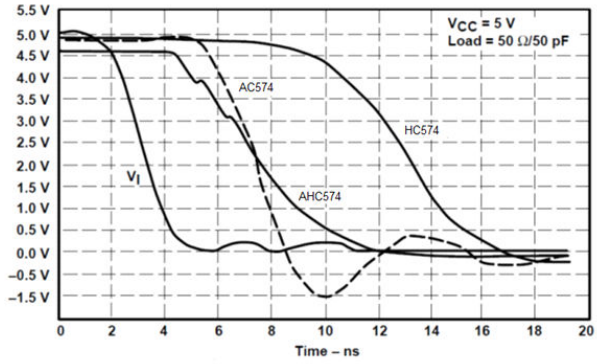



**図 8-2. Switching Charactersitics Comparison**

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *セクション 5.3* table.

Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple $V_{CC}$ pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 8.4 Layout

### 8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in 図 8-3 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

### 8.4.2 Layout Example

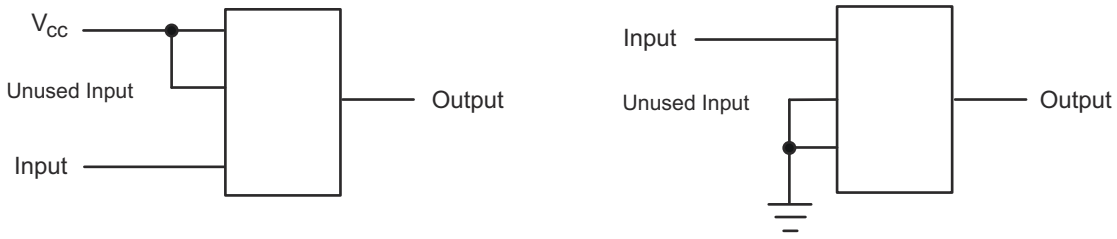



**図 8-3. Layout Diagram**


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# 9 Device and Documentation Support

## 9.1 Documentation Support

### 9.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN54AHC574 | Click here | Click here | Click here | Click here | Click here |
| SN74AHC574 | Click here | Click here | Click here | Click here | Click here |

## 9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

# 10 Revision History

**Changes from Revision J (December 2014) to Revision K (July 2024)** **Page**

- 「特長」セクションと「ESD 定格」表からマシン モデルを削除 ..... 1
- Updated RθJA values: PW = 103.3 to 116.8, DW = 79.4 to 81.1; Updated PW and DW packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W ..... 5

**Changes from Revision I (July 2003) to Revision J (December 2014)** **Page**

- 「アプリケーション」、「製品情報」の表、「ピンの機能」表、「ESD 定格」表、「熱に関する情報」表、「代表的特性」、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクショ

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ン、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、および「メカニカル、パッケージ、および注文情報」セクションを追加。 ..... 1
- 「注文情報」表を削除。 ..... 1
- 「*特長*」の一覧に軍事利用についての免責事項を追加。 ..... 1
- Changed MAX operating temperature to 125°C in *Recommended Operating Conditions* table. ..... 4

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-9685401Q2A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9685401Q2A SNJ54AHC574FK |
| 5962-9685401QRA | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9685401QRA SNJ54AHC574J |
| 5962-9685401QSA | Active | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9685401QSA SNJ54AHC574W |
| SN74AHC574DBR | Active | Production | SSOP (DB) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA574 |
| SN74AHC574DBR.A | Active | Production | SSOP (DB) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA574 |
| SN74AHC574DGSR | Active | Production | VSSOP (DGS) \| 20 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC574 |
| SN74AHC574DGVR | Active | Production | TVSOP (DGV) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA574 |
| SN74AHC574DGVR.A | Active | Production | TVSOP (DGV) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA574 |
| SN74AHC574DWR | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC574 |
| SN74AHC574DWR.A | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC574 |
| SN74AHC574DWRE4 | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC574 |
| SN74AHC574N | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 125 | SN74AHC574N |
| SN74AHC574N.A | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 125 | SN74AHC574N |
| SN74AHC574NSR | Active | Production | SOP (NS) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC574 |
| SN74AHC574NSR.A | Active | Production | SOP (NS) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC574 |
| SN74AHC574PW | Obsolete | Production | TSSOP (PW) \| 20 | - | - | Call TI | Call TI | -40 to 125 | HA574 |
| SN74AHC574PWR | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA574 |
| SN74AHC574PWR.A | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA574 |
| SN74AHC574RKSR | Active | Production | VQFN (RKS) \| 20 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC574 |
| SNJ54AHC574FK | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9685401Q2A SNJ54AHC574FK |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SNJ54AHC574FK.A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9685401Q2A SNJ54AHC 574FK |
| SNJ54AHC574J | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9685401QRA SNJ54AHC574J |
| SNJ54AHC574J.A | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9685401QRA SNJ54AHC574J |
| SNJ54AHC574W | Active | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9685401QSA SNJ54AHC574W |
| SNJ54AHC574W.A | Active | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9685401QSA SNJ54AHC574W |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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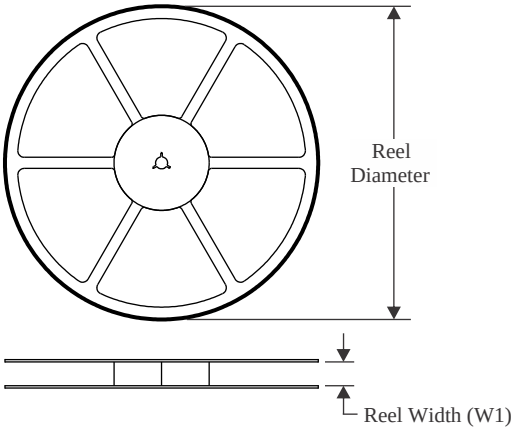
- Catalog : SN74AHC574
- Military : SN54AHC574

NOTE: Qualified Version Definitions:

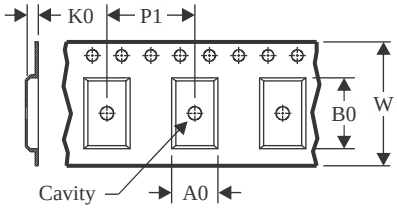
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

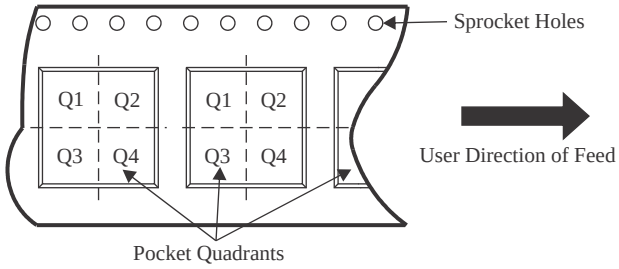



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

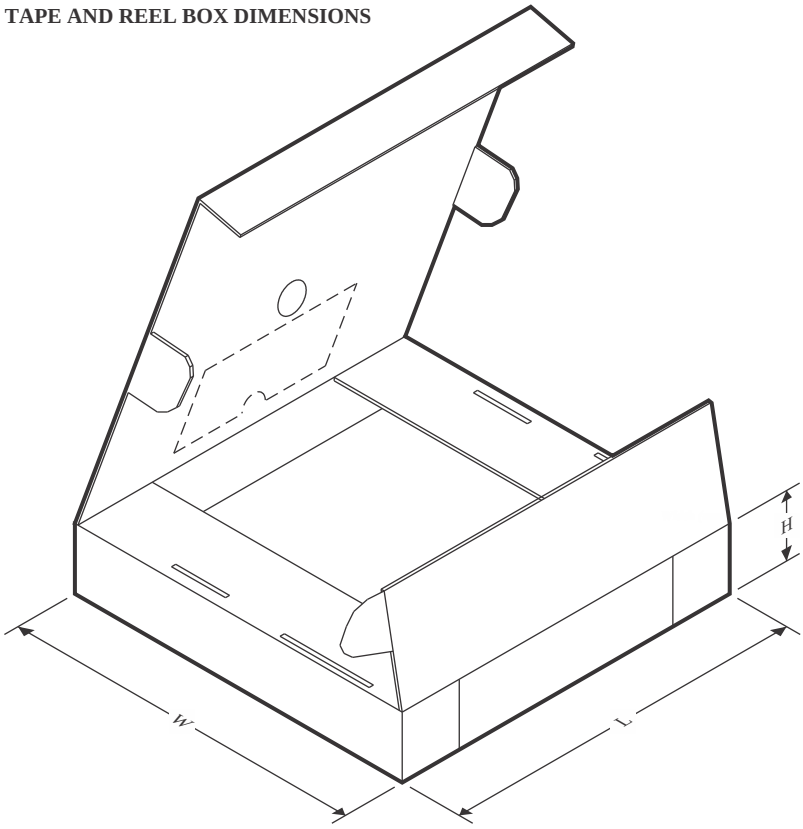
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AHC574DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AHC574DGSR | VSSOP | DGS | 20 | 5000 | 330.0 | 16.4 | 5.4 | 5.4 | 1.45 | 8.0 | 16.0 | Q1 |
| SN74AHC574DGVR | TVSOP | DGV | 20 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHC574DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AHC574DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AHC574NSR | SOP | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74AHC574PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74AHC574RKSR | VQFN | RKS | 20 | 3000 | 180.0 | 12.4 | 2.8 | 4.8 | 1.2 | 4.0 | 12.0 | Q1 |

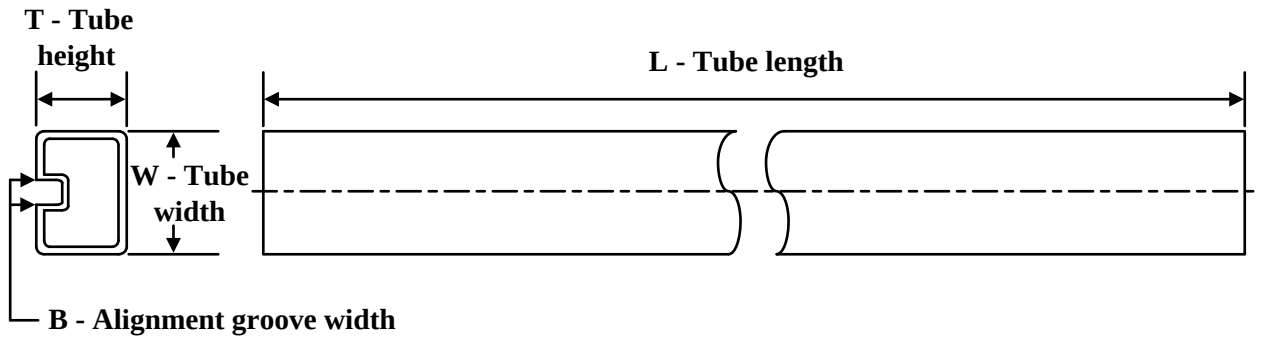
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AHC574DBR | SSOP | DB | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHC574DGSR | VSSOP | DGS | 20 | 5000 | 353.0 | 353.0 | 32.0 |
| SN74AHC574DGVR | TVSOP | DGV | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHC574DWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74AHC574DWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74AHC574NSR | SOP | NS | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74AHC574PWR | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHC574RKSR | VQFN | RKS | 20 | 3000 | 210.0 | 185.0 | 35.0 |

## TUBE



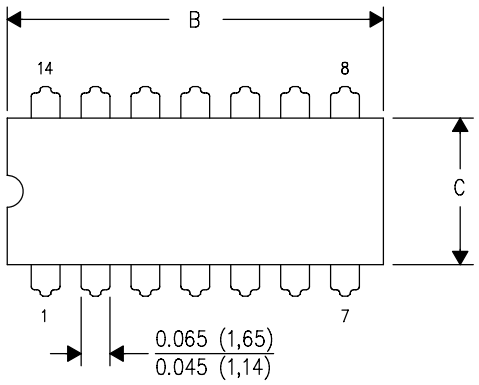

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-9685401Q2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-9685401QSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74AHC574N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74AHC574N.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54AHC574FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54AHC574FK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54AHC574W | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54AHC574W.A | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |

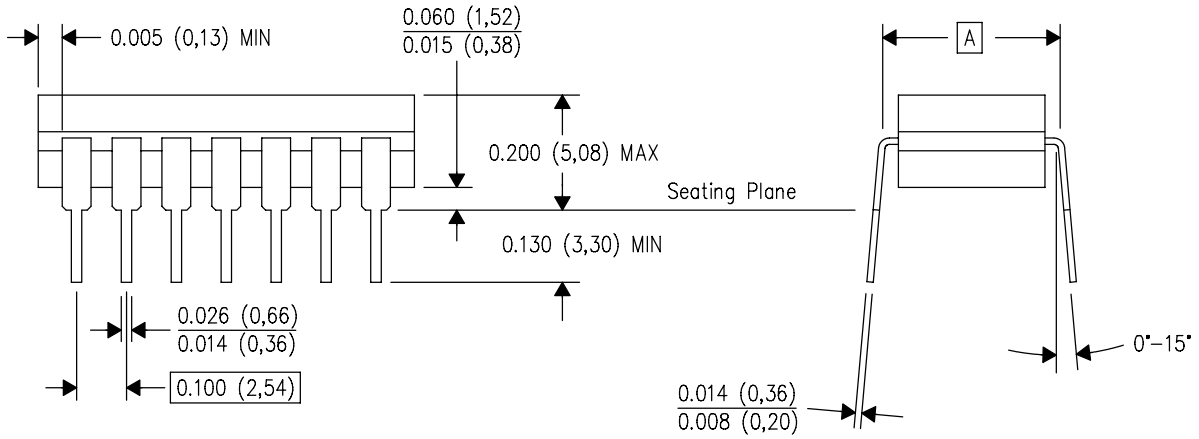
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

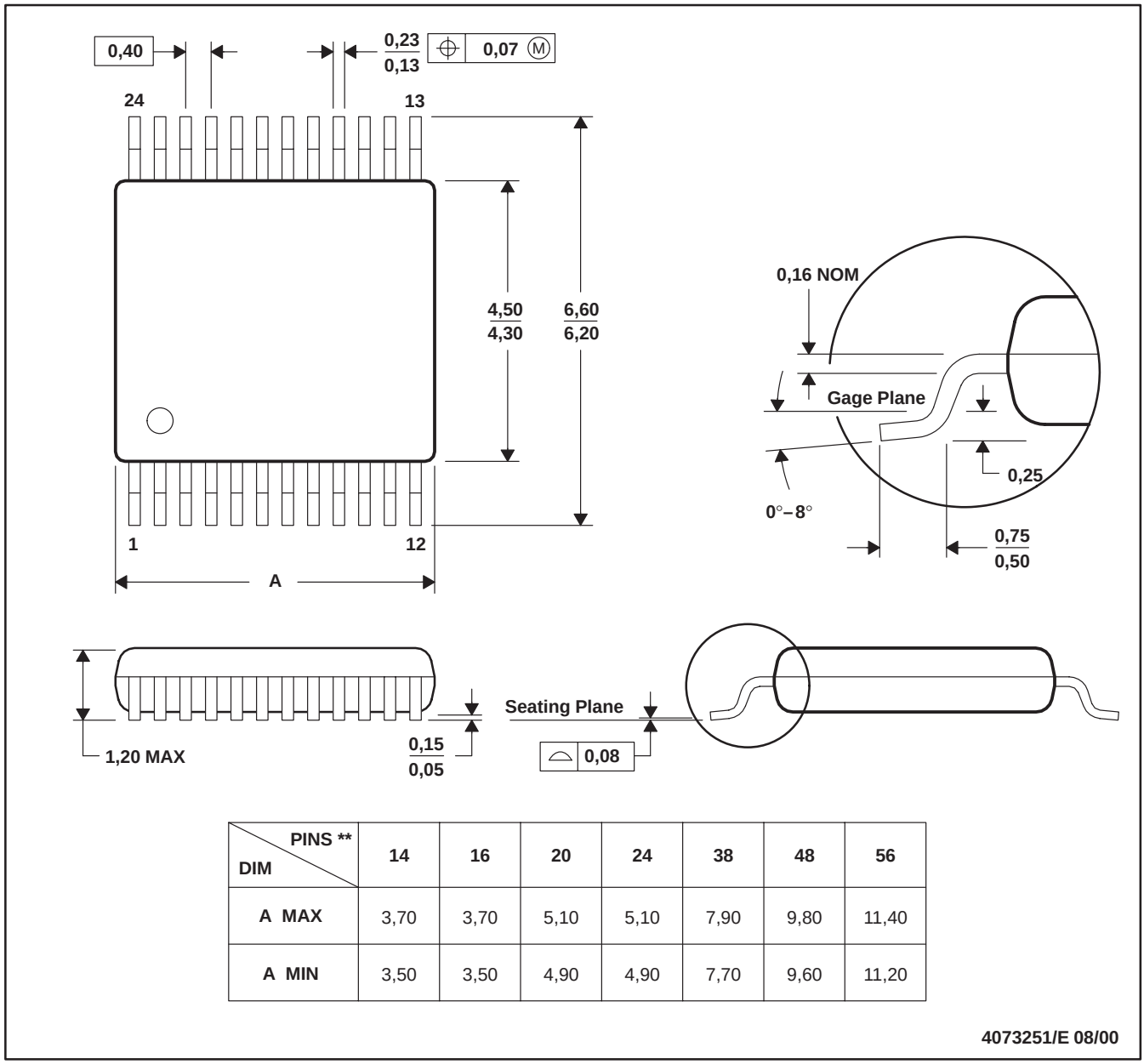



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

# GENERIC PACKAGE VIEW

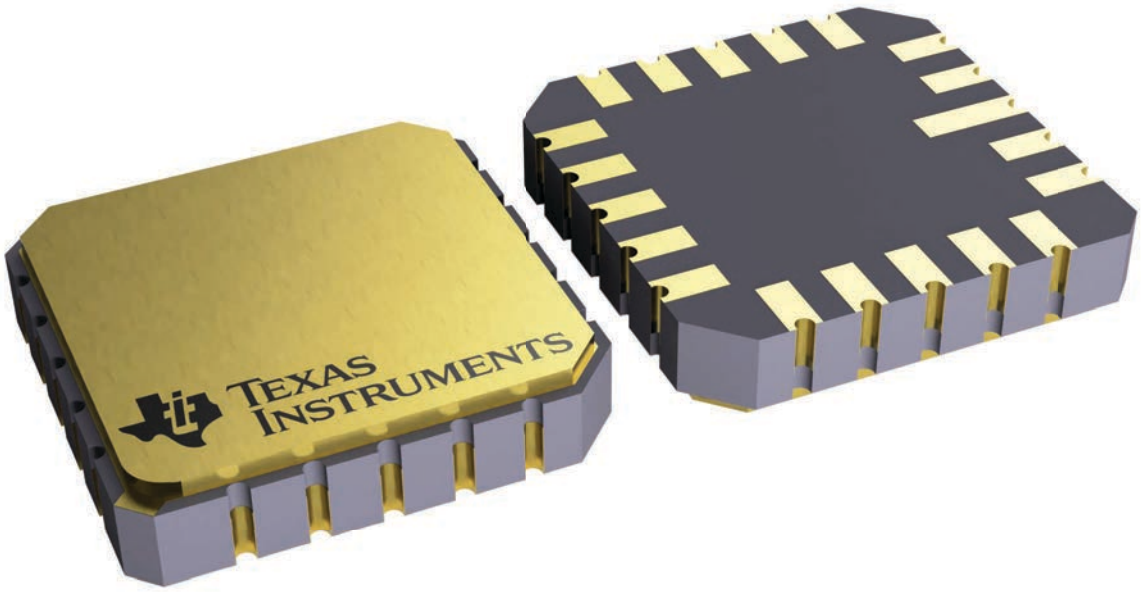
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

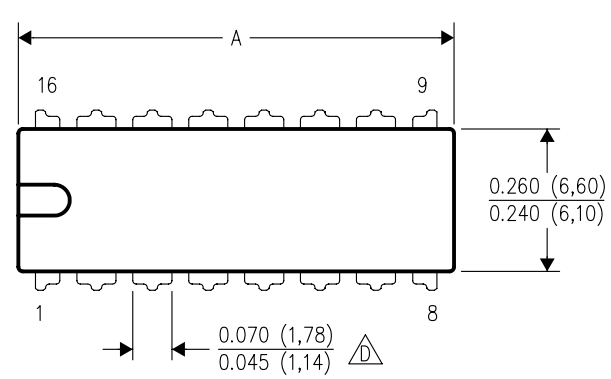



4229370VA\

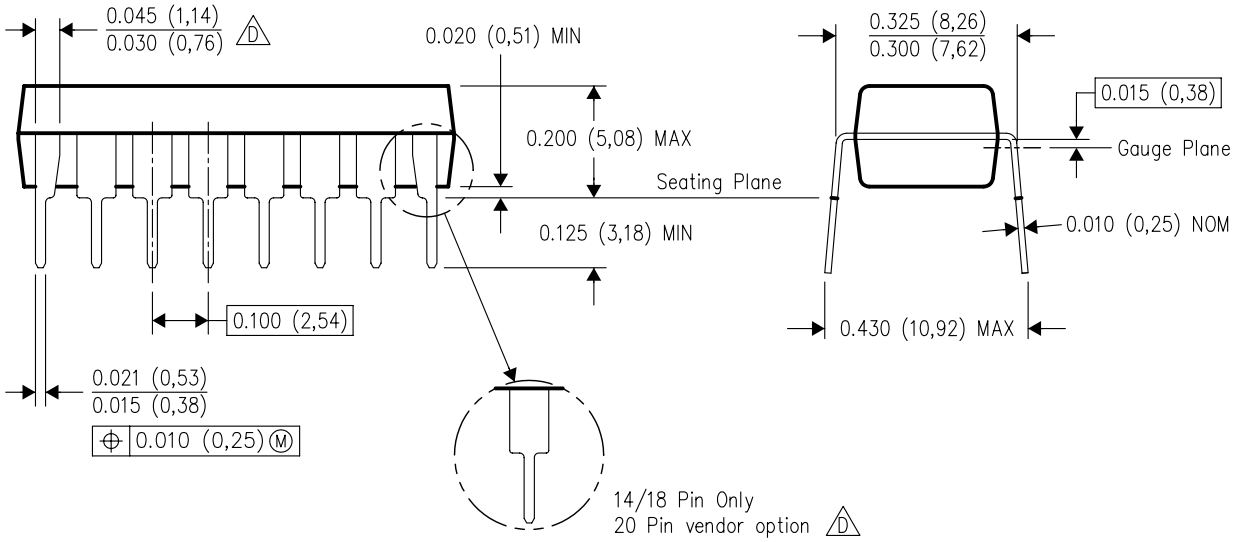
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

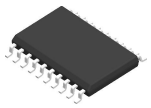



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

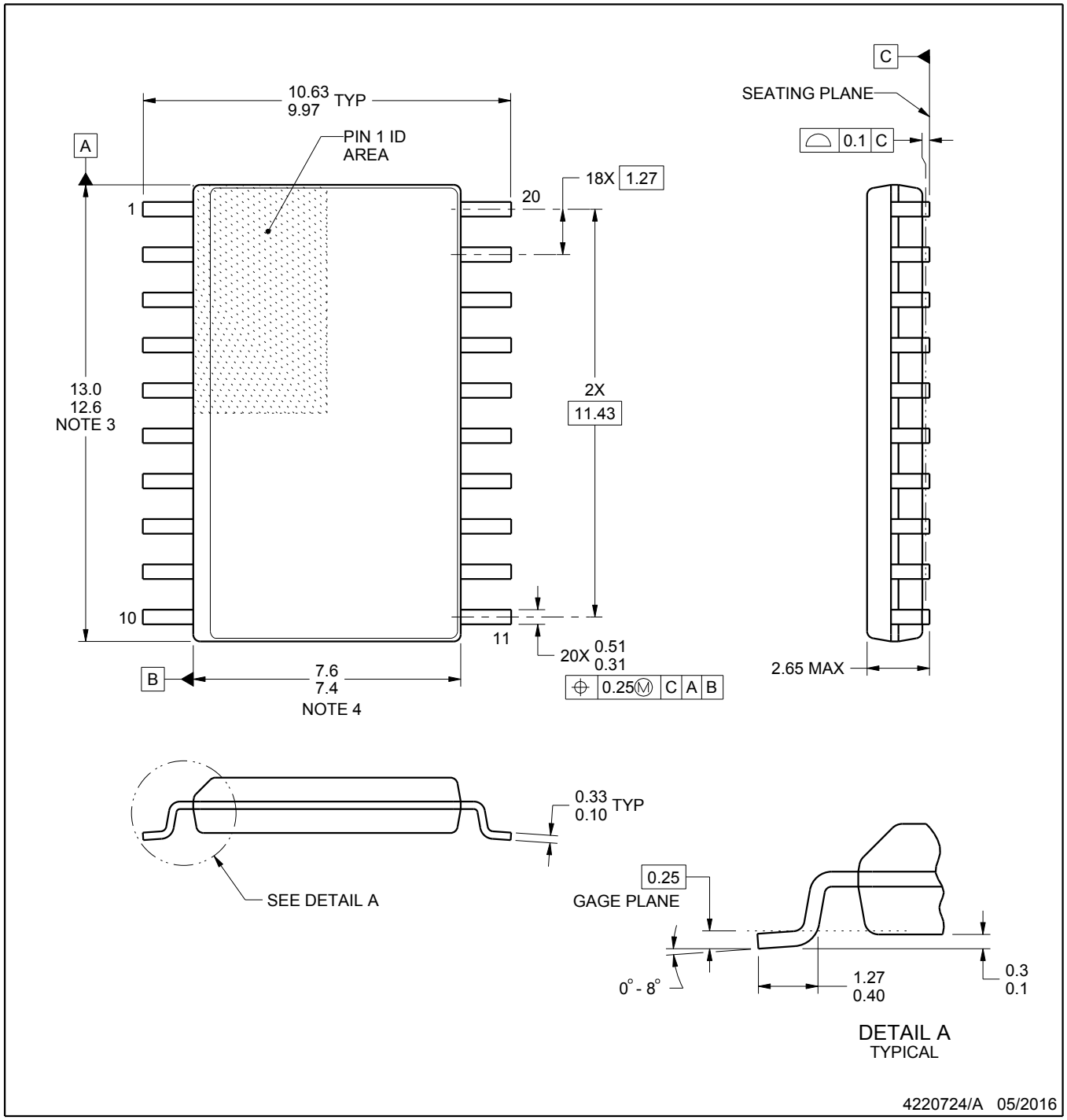


# PACKAGE OUTLINE

## DW0020A

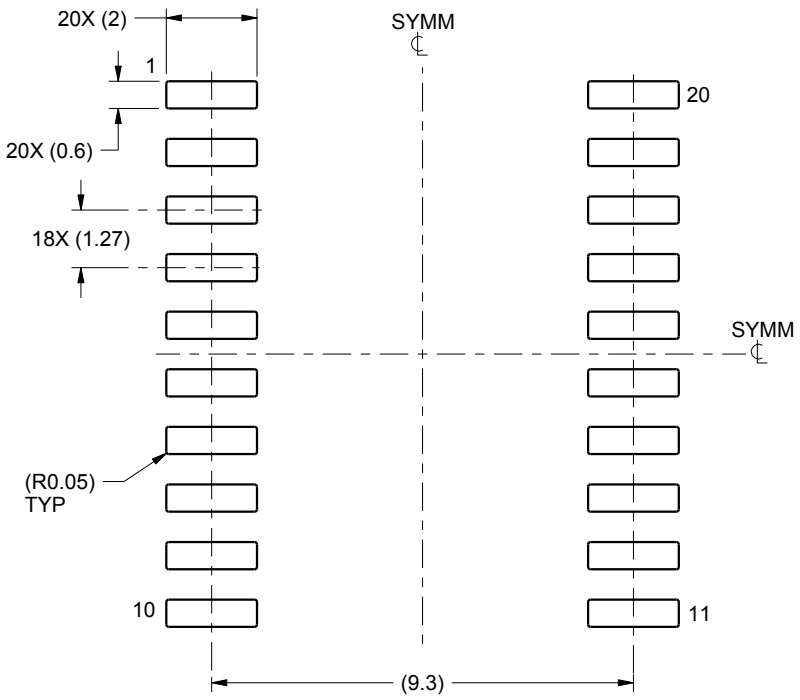
## SOIC - 2.65 mm max height

SOIC

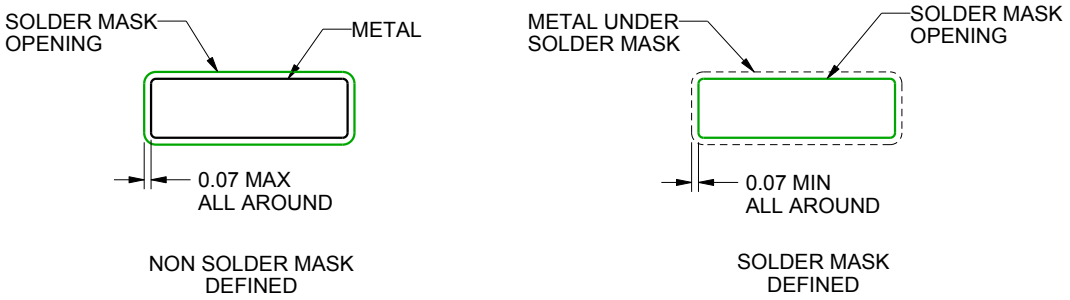



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

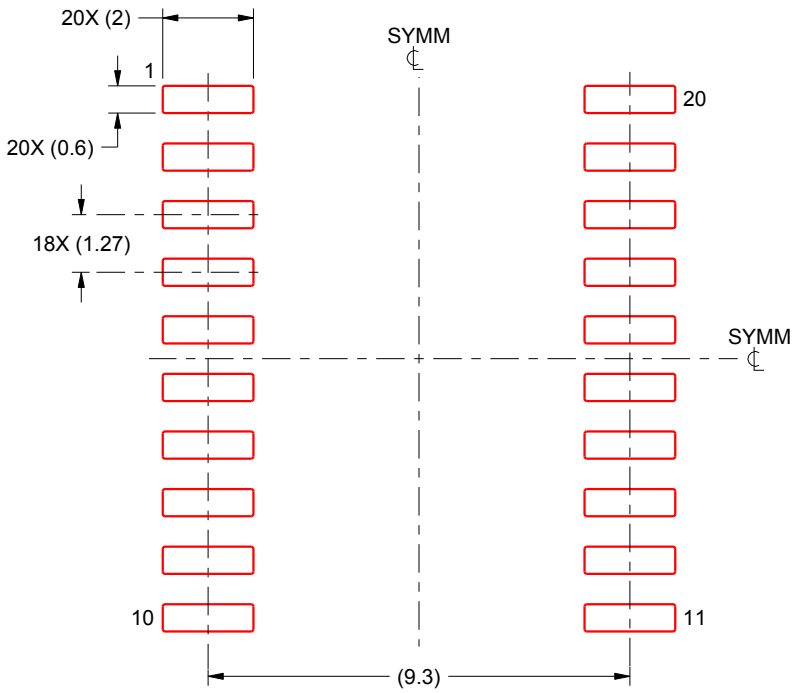



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



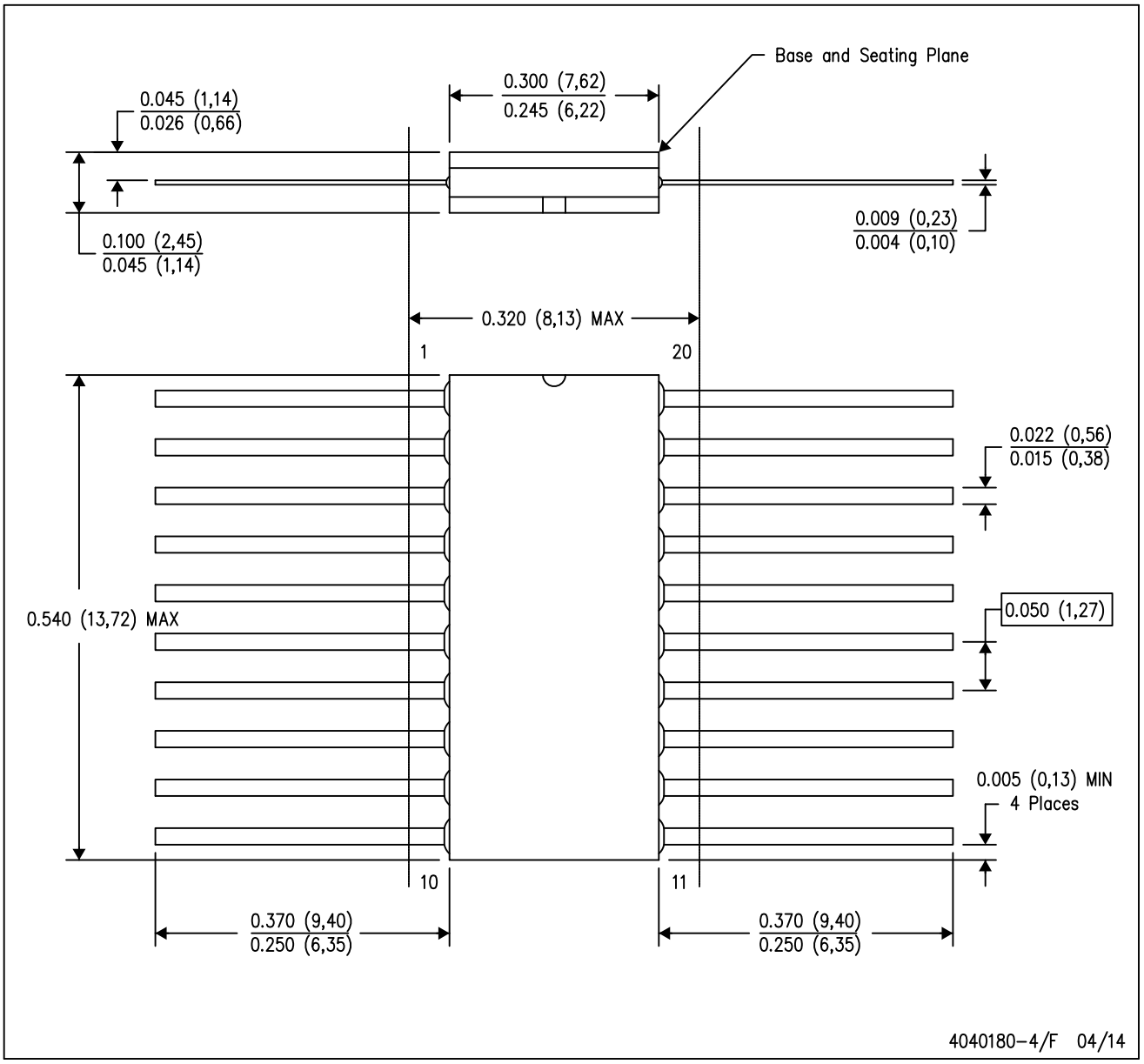

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



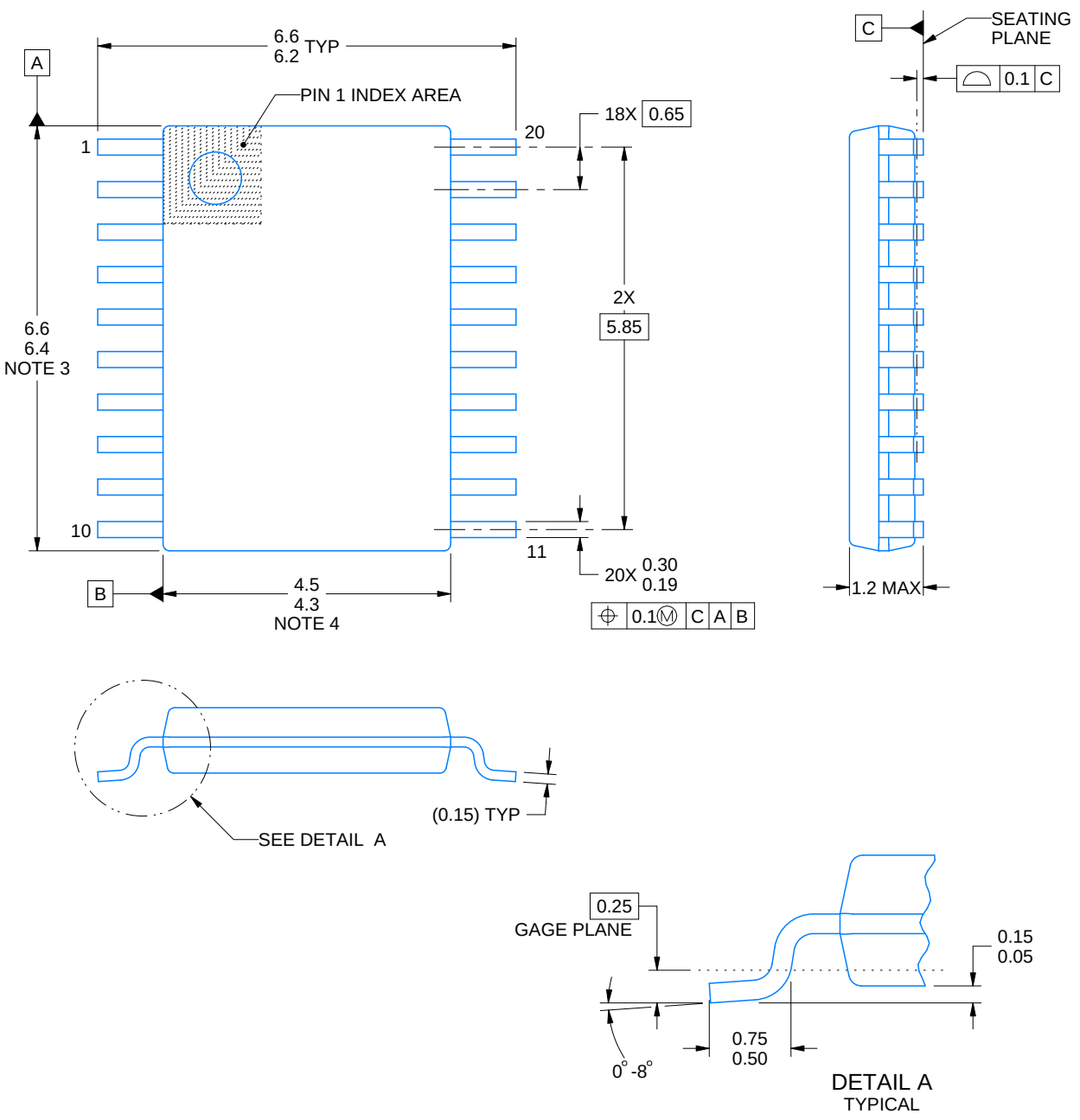

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

# PACKAGE OUTLINE

## PW0020A

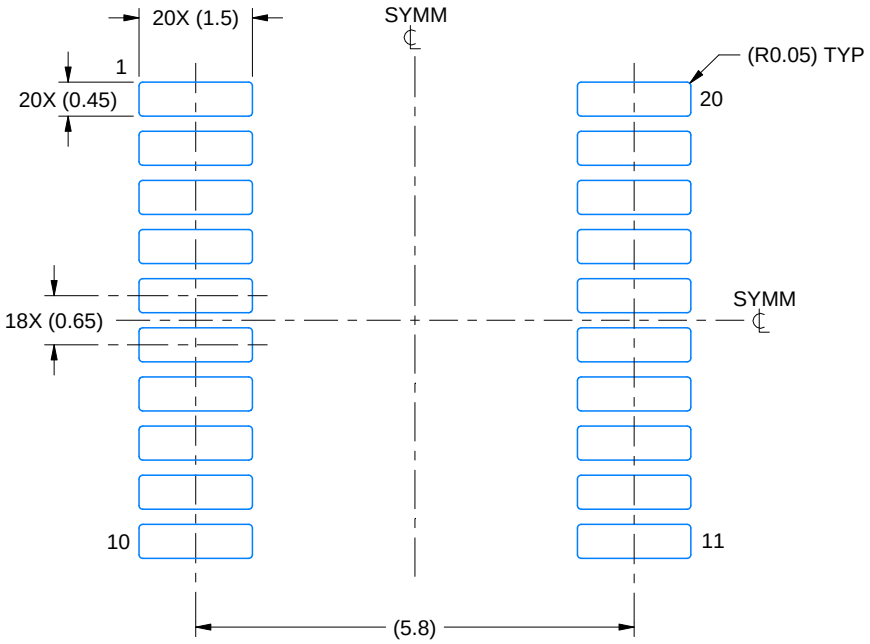
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

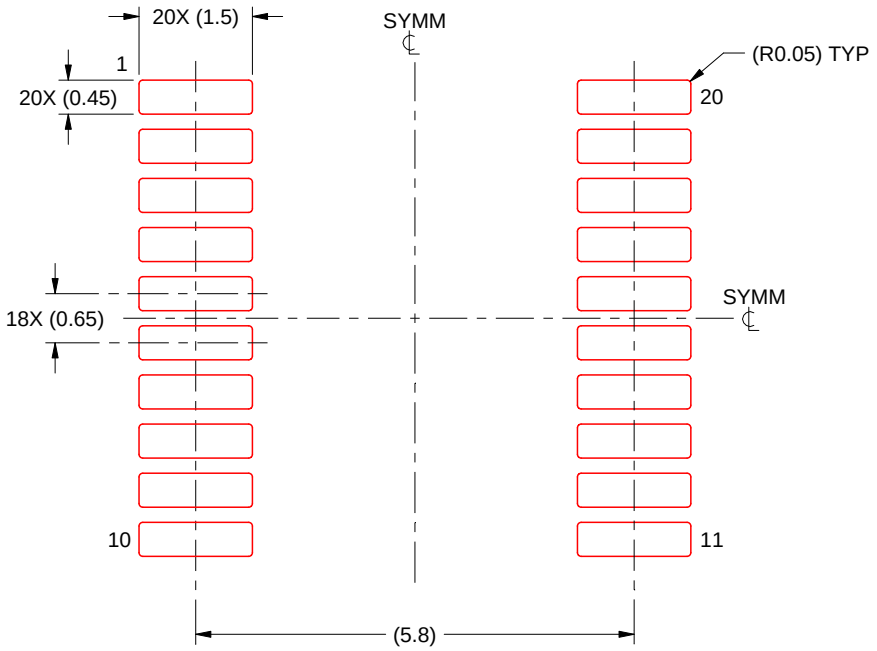



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

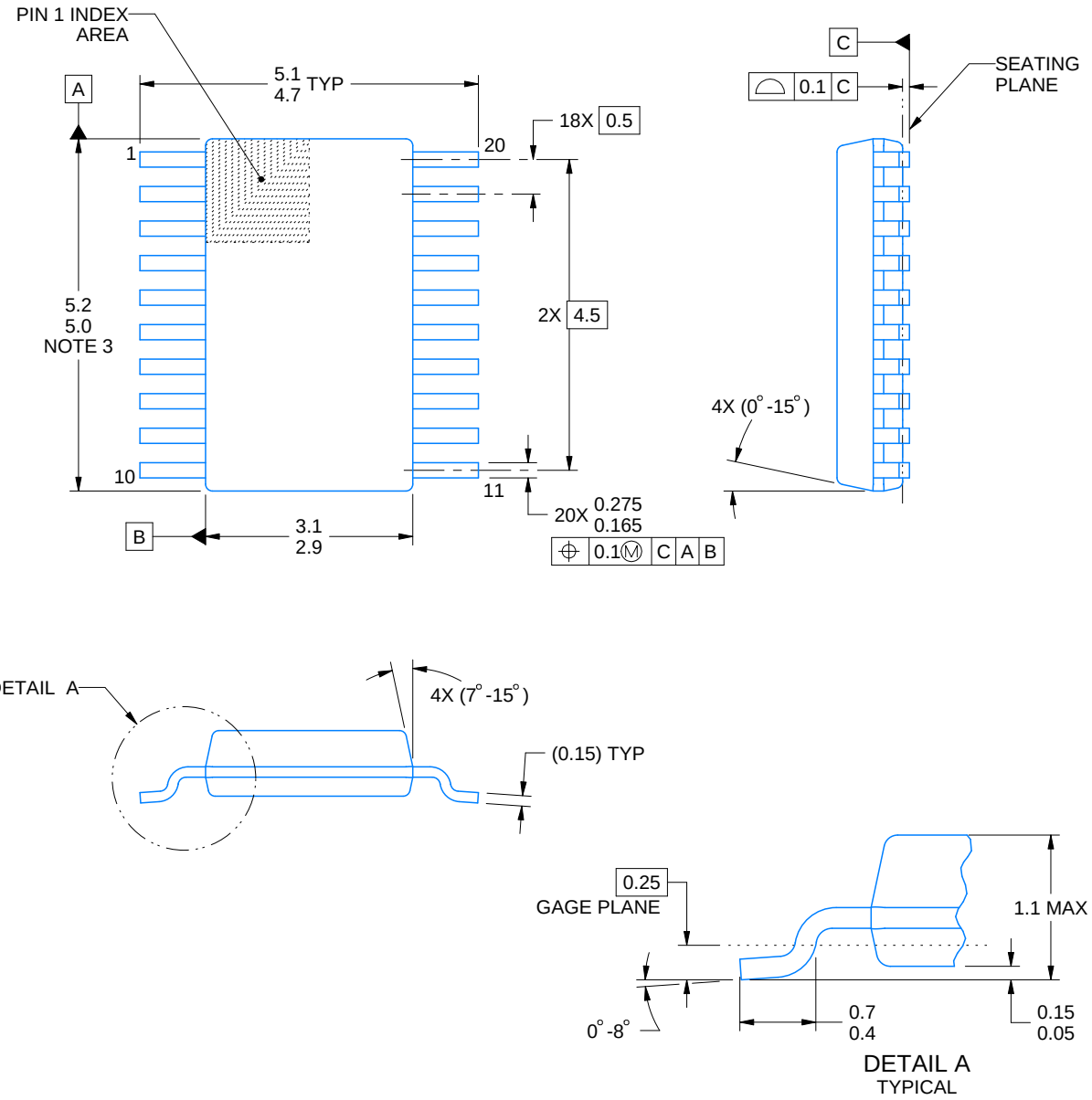
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DGS0020A

## VSSOP - 1.1 mm max height

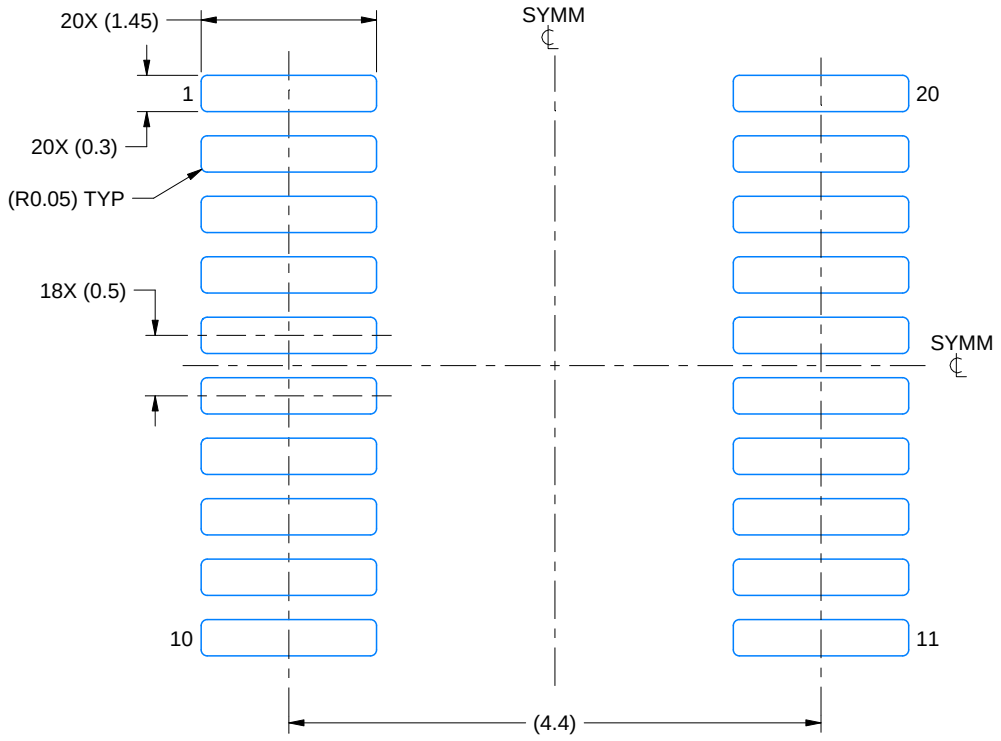
SMALL OUTLINE PACKAGE



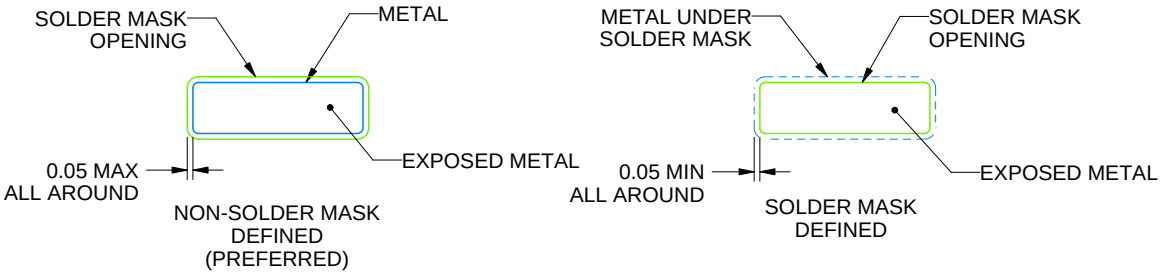

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.




LAND PATTERN EXAMPLE
SCALE: 16X

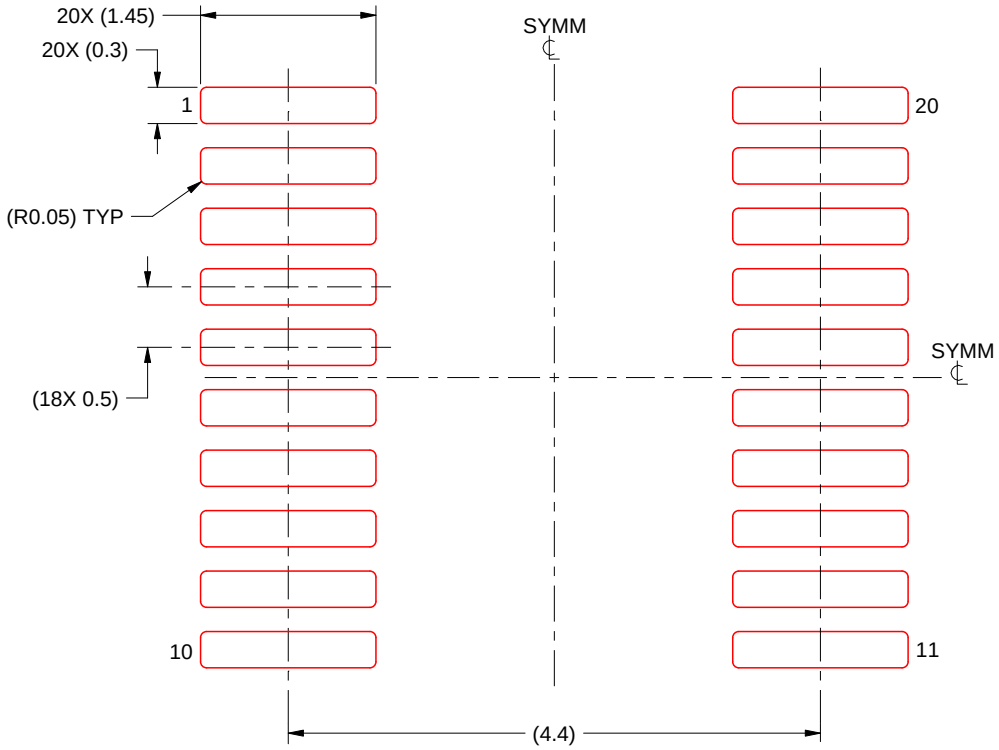



SOLDER MASK DETAILS

4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

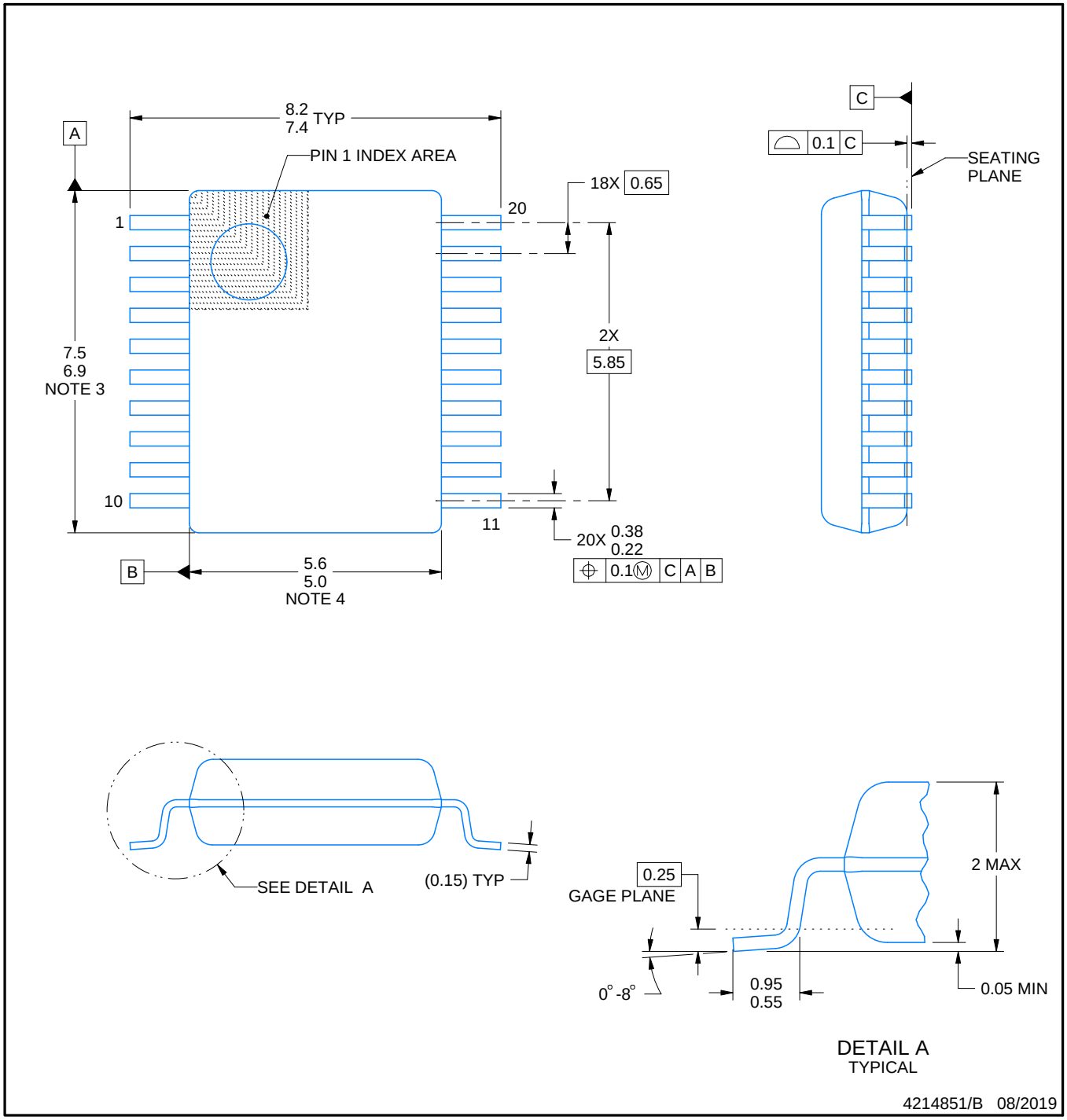
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DB0020A

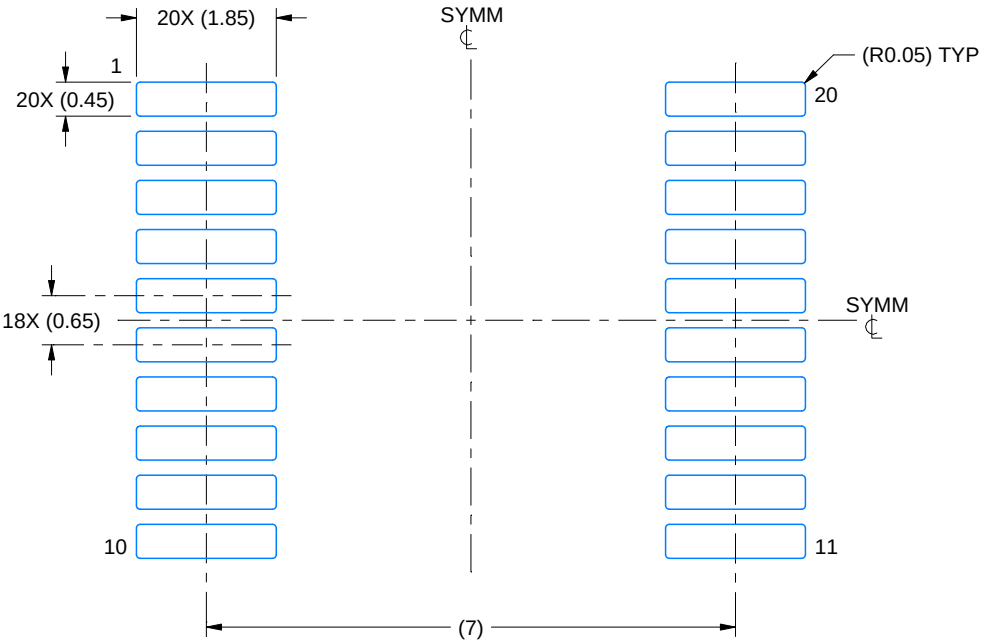
## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

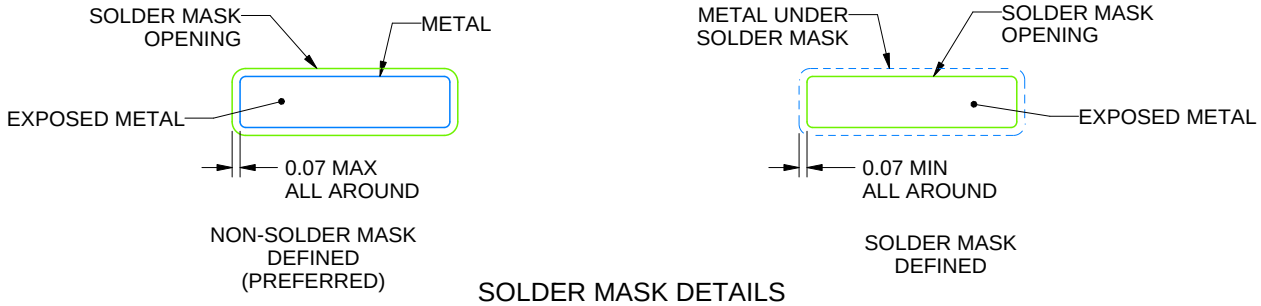



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

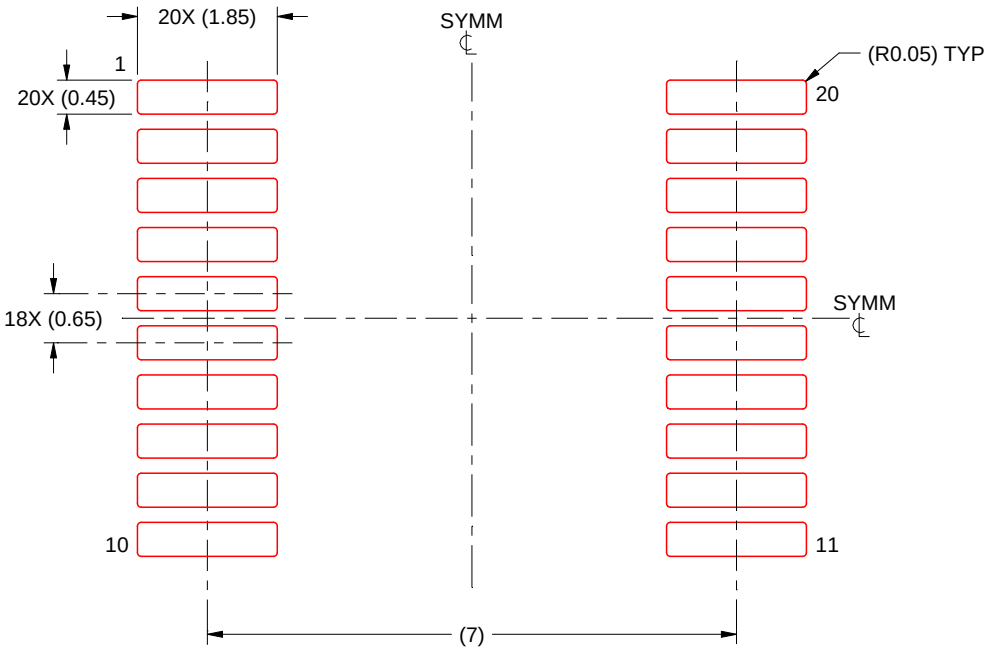
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DB0020A

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

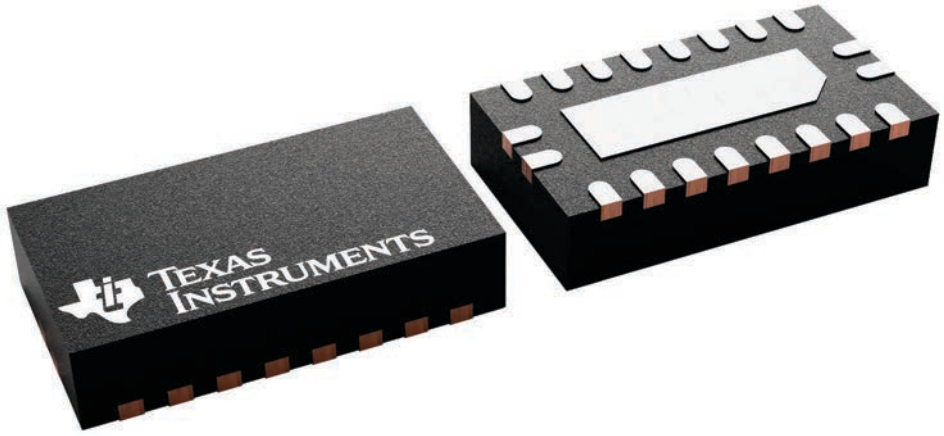
## RKS 20

## VQFN - 1 mm max height

**2.5 x 4.5, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

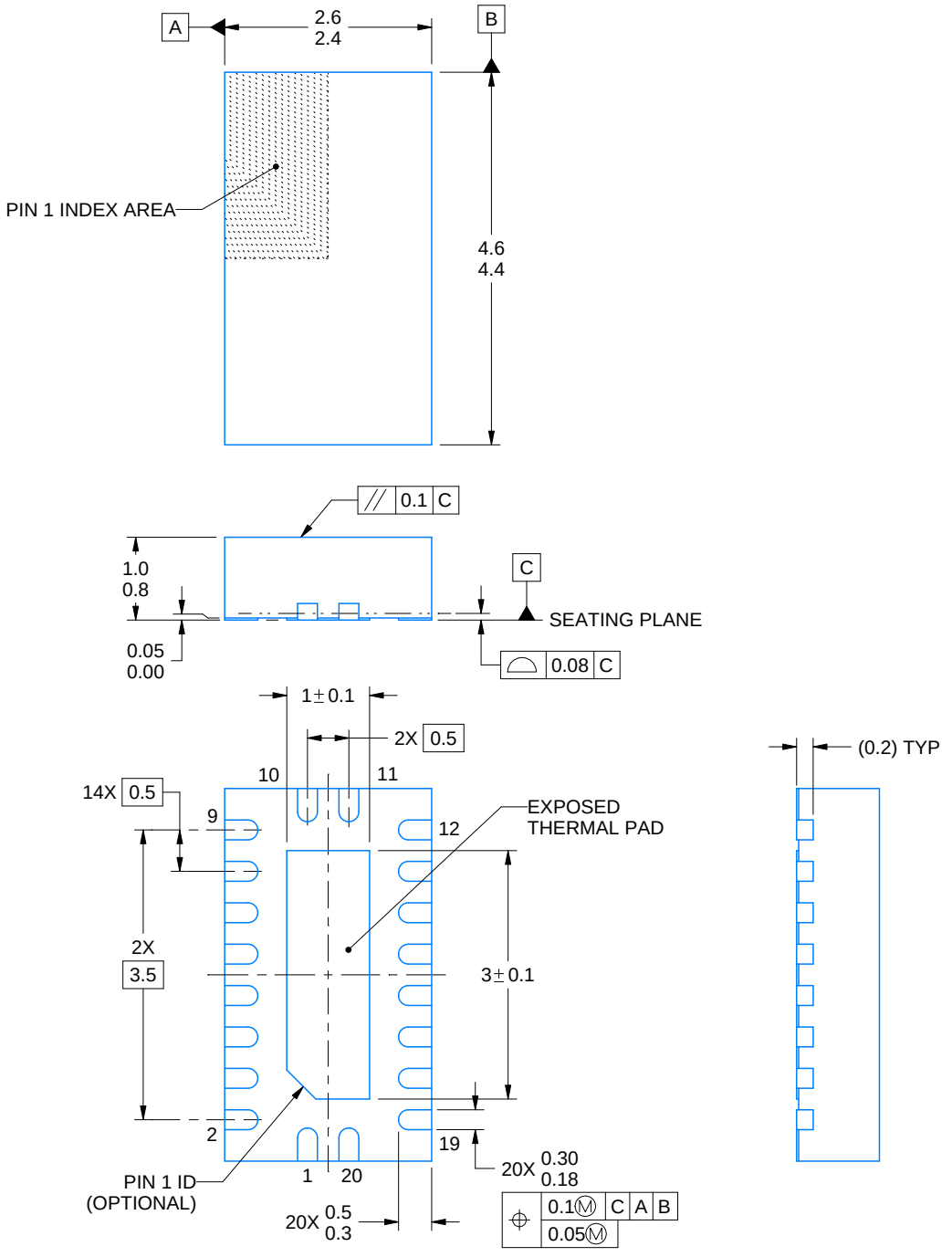


# PACKAGE OUTLINE

## RKS0020A

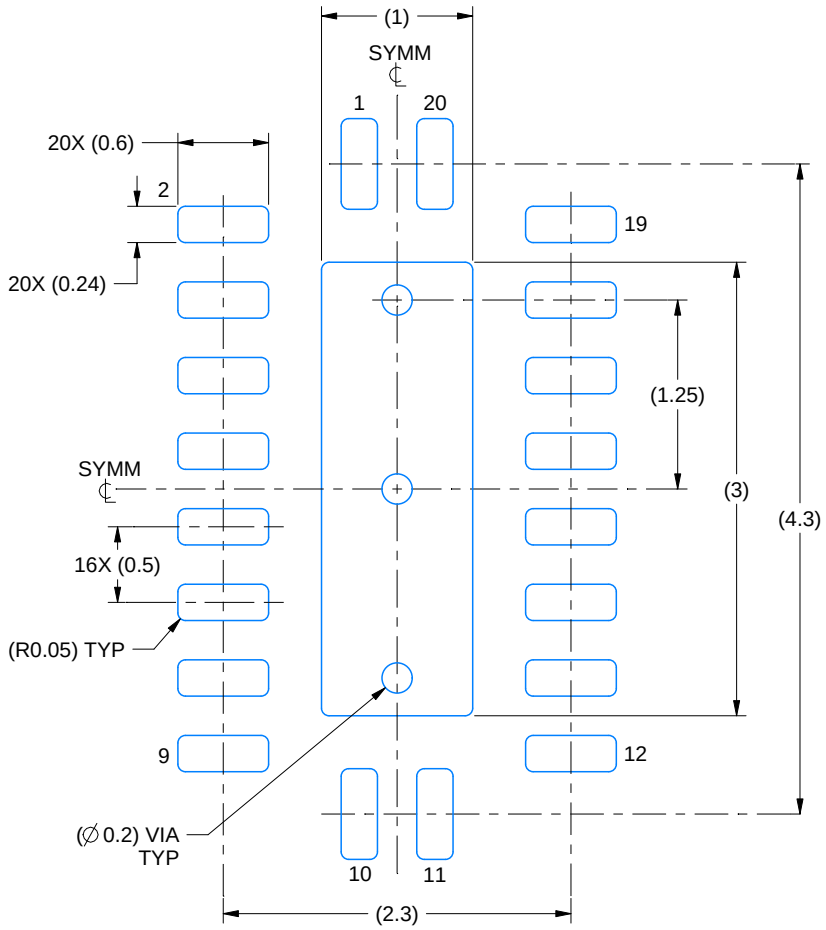
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

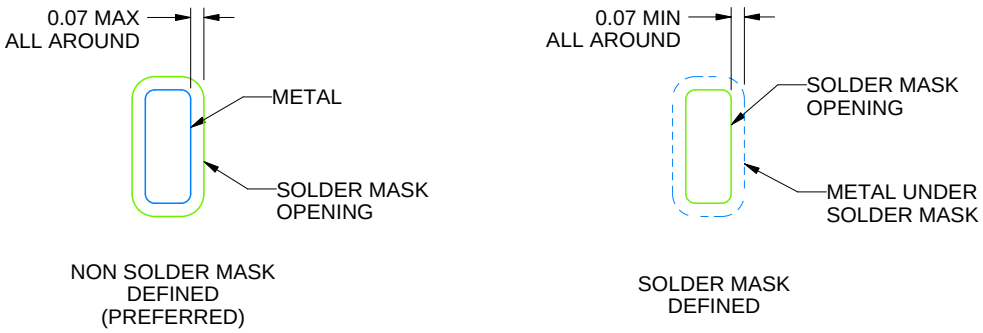



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:20X

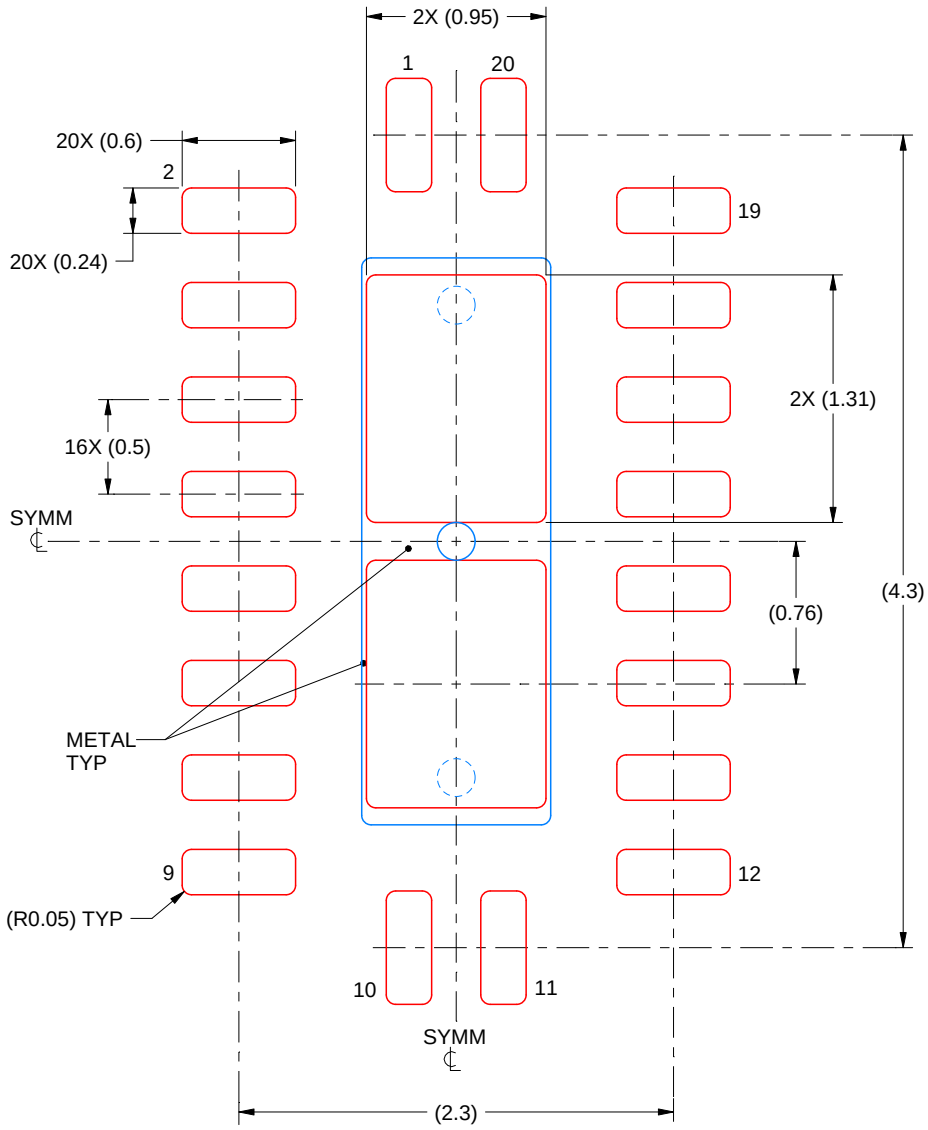



SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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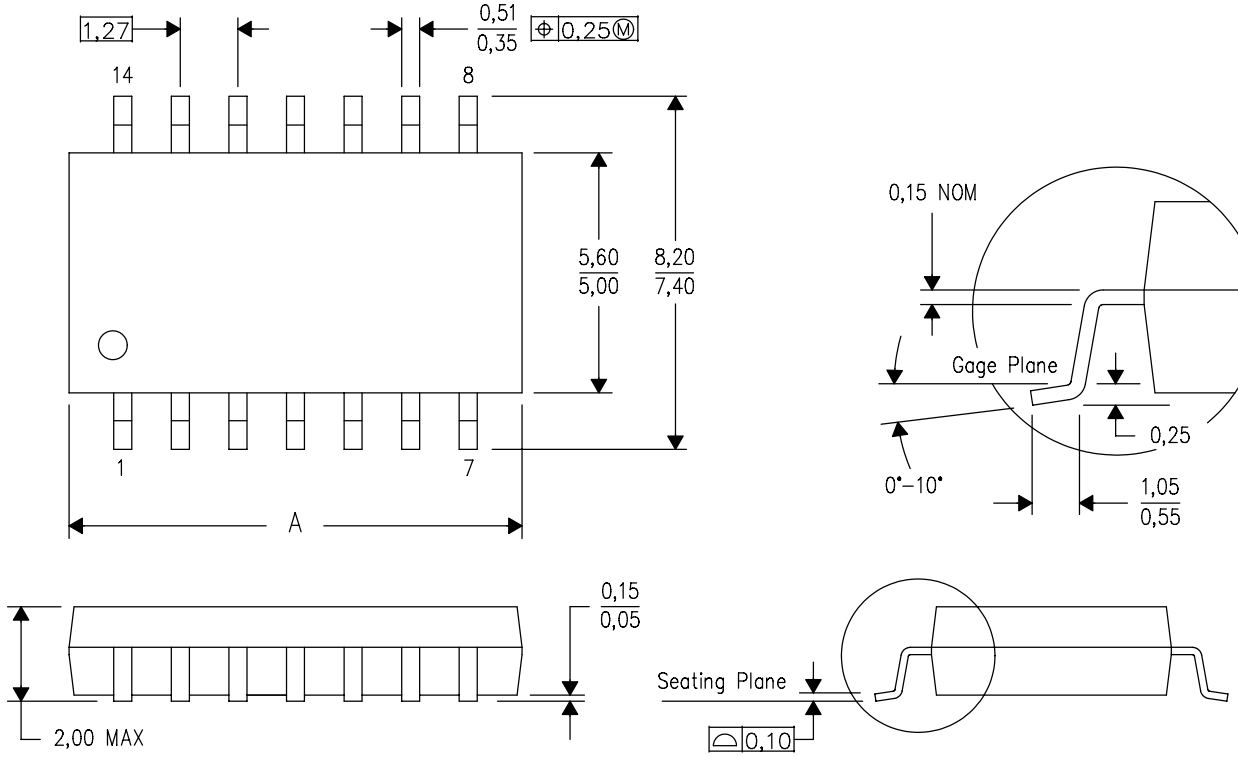
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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