TEXAS INSTRUMENTS
SN54AHC594, SN74AHC594
JAJSUA6H – JUNE 1998 – REVISED APRIL 2024

SNx4AHC594 出力レジスタ搭載、8 ビット シフト レジスタ

1 特長

- 2V～5.5V の V_{CC} で動作
- 8 ビット、シリアル入力、パラレル出力、ストレージ付きシフト レジスタ
- シフトおよびストレージ レジスタの独立した直接オーバーライド クリア
- シフトおよびストレージ レジスタ用の独立したクロック
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護
  - 2000V、人体モデル (A114-A)
  - 1000V、デバイス帯電モデル (C101)

2 アプリケーション

- ネットワーク スイッチ
- 電源インフラストラクチャ
- PC およびノートパソコン
- LED ディスプレイ
- サーバー

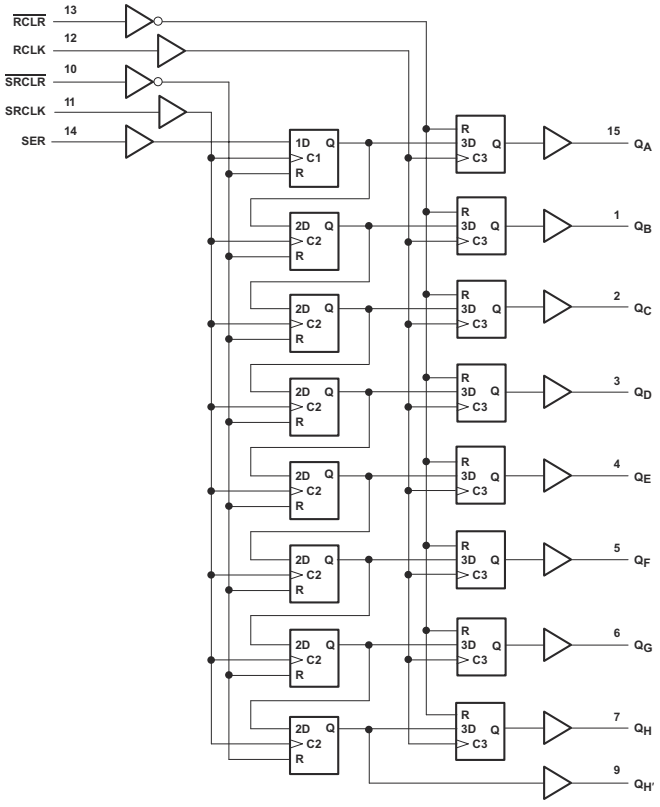
3 概要

SNx4AHC594 デバイスには 8 ビットのシリアル イン / パラレル アウトのシフト レジスタが搭載されており、8 ビットの D タイプ ストレージ レジスタへデータを供給します。シフト レジスタとストレージ レジスタに、それぞれ独立したクロックとダイレクト オーバーライディング クリア ($\overline{SRCLR}$、$\overline{RCLR}$) 入力が用意されています。カスケード接続用にシリアル ($Q_{H'}$) 出力が用意されています。

製品情報

部品番号	パッケージ (1)	パッケージ サイズ (2)	本体サイズ (3)
SNx4AHC594	D (SOIC、16)	9.90 mm × 6mm	9.90 mm × 3.90 mm
	DB (SSOP、16)	6.20 mm × 7.8mm	6.20 mm × 5.30 mm
	N (PDIP、16)	19.31 mm × 9.4mm	19.31 mm × 6.35 mm
	NS (SOP、16)	5mm × 6.4mm	5mm × 4.4mm
	PW (TSSOP、16)	5.00 mm × 6.4mm	5.00 mm × 4.40 mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

概略回路図

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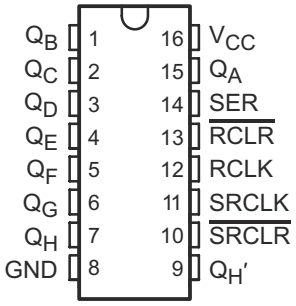
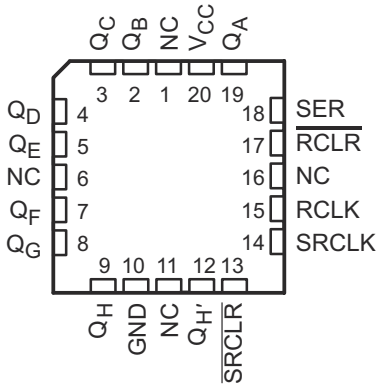
4 Pin Configuration and Functions

SN54AHC594 . . . J OR W PACKAGE
SN74AHC594 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHC594 . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

表 4-1. Pin Functions

Pin				I/O	Description
Name	SN54AHC594		SN74AHC594		
	FK	J, W	D, DB, N, NS, PW		
GND	10	8	8	—	Ground Pin
NC	1	—	—	—	No connect
	6				
	11				
	16				
Q_A	19	15	15	O	Q_A Output
Q_B	2	1	1	O	Q_B Output
Q_C	3	2	2	O	Q_C Output
Q_D	4	3	3	O	Q_D Output
Q_E	5	4	4	O	Q_E Output
Q_F	7	5	5	O	Q_F Output
Q_G	8	6	6	O	Q_G Output
Q_H	9	7	7	O	Q_H Output
$Q_{H'}$	12	9	9	O	$Q_{H'}$ Output
RCLK	15	12	12	I	RCLK Input
$\overline{RCLR}$	17	13	13	I	$\overline{RCLR}$ Input
SER	18	14	14	I	SER Input
SRCLK	14	11	11	I	SRCLK Input
$\overline{SRCLR}$	13	10	10	I	$\overline{SRCLR}$ Input
V_{CC}	20	16	16	—	Power pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Output voltage range(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±75	mA
T_{stg}	Storage temperature range		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN54AHC594(2)		SN74AHC594		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	µA
		V_{CC} = 3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5.5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	µA
		V_{CC} = 3 V ± 0.3 V		4		4	mA
		V_{CC} = 5.5 V ± 0.5 V		8		8	
Δt/Δv	Input transition rise and fall time	V_{CC} = 3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5.5 V ± 0.5 V		20		20	

over operating free-air temperature range (unless otherwise noted)(1)

		SN54AHC594(2)		SN74AHC594		UNIT
		MIN	MAX	MIN	MAX	
T_A	Operating free-air temperature	–55	125	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, (SCBA004).
(2) Product Preview

5.4 Thermal Information

THERMAL METRIC(1)		SN74AHC594					UNIT
		D	DB	N	NS	PW	
		16 PINS					
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.2	97.5	47.5	79.1	135.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.1	47.7	34.9	35.4	70.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	27.7	48.1	27.5	39.9	81.3	
ψ_{JT}	Junction-to-top characterization parameter	9.9	9.8	19.8	5.4	22.5	
ψ_{JB}	Junction-to-board characterization parameter	37.4	47.6	27.4	39.5	80.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the TI application report *IC Package Thermal Metrics* (SPRA953).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC594(2)		SN74AHC594		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 µA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
	Q_A – Q_H I_{OH} = –8 mA		3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 µA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
					0.36		0.5		0.44	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±0.1		±1(1)		±1	µA
I_{CC}	V_I = V_{CC} or GND I_O = 0	5.5 V			4		40		40	µA
C_i	V_I = V_{CC} or GND	5 V		2	10				10	pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.
(2) Product Preview

5.6 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

			T_A = 25°C		SN54AHC594(2)		SN74AHC594		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse Duration	$\overline{RCLK}$ or SRCLK high or low	5.5		5.5		5.5		ns
		$\overline{RCLR}$ or $\overline{SRCLR}$ low	5		5		5		
t_{su}	Setup time	SER before SRCLK ↑	3.5		3.5		3.5		ns
		SRCLK ↑ before RCLK ↑ (1)	8		8.5		8.5		
		$\overline{SRCLR}$ low before SRCLK ↑	8		9		9		
		$\overline{SRCLR}$ high (inactive) before SRCLK ↑	4.2		4.8		4.8		
		$\overline{RCLR}$ high (inactive) before RCLK ↑	4.6		5.3		5.3		
t_h	Hold time, data after CLK ↑	SER after SRCLK ↑	1.5		1.5		1.5		ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.
(2) Product Preview

5.7 Timing Requirements, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

			T_A = 25°C		SN54AHC594(2)		SN74AHC594		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse Duration	$\overline{RCLK}$ or SRCLK high or low	5		5		5		ns
		$\overline{RCLR}$ or $\overline{SRCLR}$ low	5.2		5.2		5.2		
t_{su}	Setup time	SER before SRCLK ↑	3		3		3		ns
		SRCLK ↑ before RCLK ↑ (1)	5		5		5		
		$\overline{SRCLR}$ low before SRCLK ↑	5		5		5		
		$\overline{SRCLR}$ high (inactive) before SRCLK ↑	2.9		3.3		3.3		
		$\overline{RCLR}$ high (inactive) before RCLK ↑	3.2		3.7		3.7		
t_h	Hold time, data after CLK ↑	SER after SRCLK ↑	2		2		2		ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.
(2) Product Preview

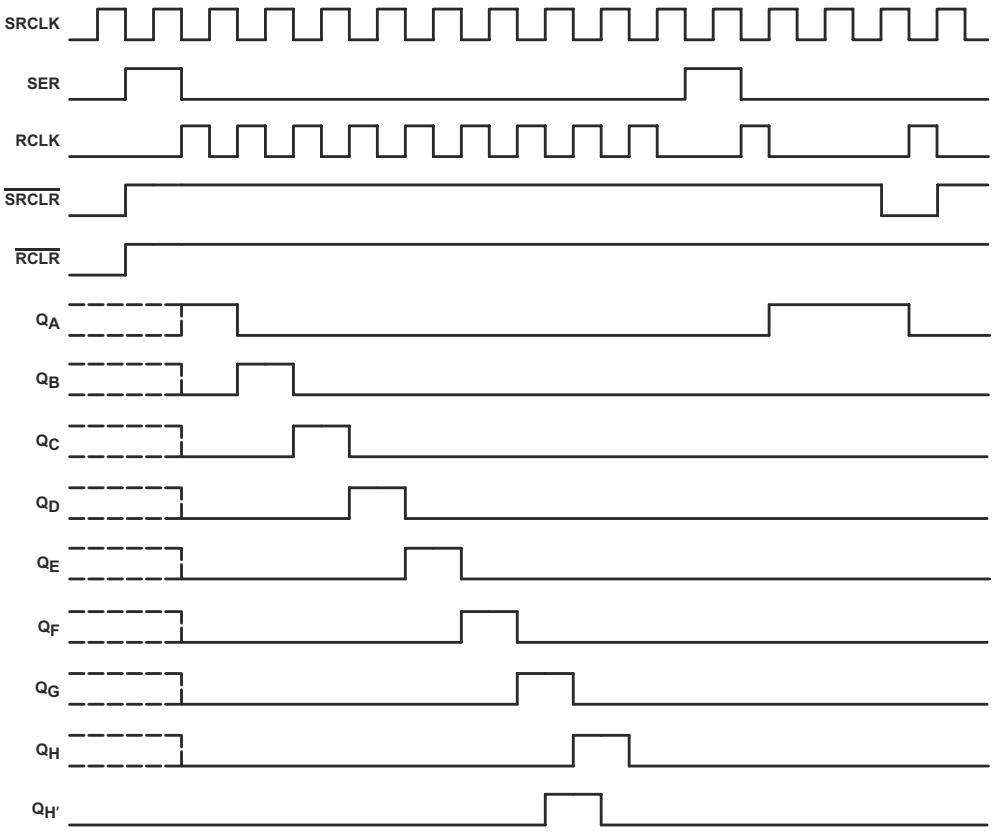


図 5-1. Timing Diagram

5.8 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC594[2]		SN74AHC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	80[1]	120[2]		70[1]		70		MHz
			C_L = 50 pF	55	105		50		50		
t_{PLH}	RCLK	Q_A – Q_H	C_L = 15 pF		4.6[1]	8[1]	1[1]	8.5[1]	1	8.5	ns
t_{PHL}					4.9[1]	8.2[1]	1[1]	8.8[1]	1	8.8	
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 15 pF		5.4[1]	9.1[1]	1[1]	9.7[1]	1	9.7	ns
t_{PHL}					5.5[1]	9.2[1]	1[1]	9.9[1]	1	9.9	
t_{PHL}	$\overline{RCLR}$	Q_A – Q_H	C_L = 15 pF		6[1]	9.8[1]	1[1]	10.6[1]	1	10.6	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 15 pF		5.6[1]	9.2[1]	1[1]	10[1]	1	10	ns
t_{PLH}	RCLK	Q_A – Q_H	C_L = 50 pF		6.9	10.5	1	11.1	1	11.1	ns
t_{PHL}					8.1	11.9	1	13.1	1	13.1	
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 50 pF		7.7	11.7	1	12.4	1	12.4	ns
t_{PHL}					8.4	12.5	1	13.9	1	13.9	
t_{PHL}	$\overline{RCLR}$	Q_A – Q_H	C_L = 50 pF		9.1	13.1	1	14.4	1	14.4	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 50 pF		8.5	12.4	1	14	1	14	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) Product Preview

5.9 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC594[2]		SN74AHC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	135[1]	170[1]		115[1]		115		MHz
			C_L = 50 pF	120	140		95		95		
t_{PLH}	RCLK	Q_A – Q_H	C_L = 15 pF		3.3[1]	6.2[1]	1[1]	6.5[1]	1	6.5	ns
t_{PHL}					3.7[1]	6.5[1]	1[1]	6.9[1]	1	6.9	
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 15 pF		3.7[1]	6.8[1]	1[2]	7.2[1]	1	7.2	ns
t_{PHL}					4.1[1]	7.2[1]	1[1]	7.6[1]	1	7.6	
t_{PHL}	$\overline{RCLR}$	Q_A – Q_H	C_L = 15 pF		4.5[1]	7.6[1]	1[1]	8.2[1]	1	8.2	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 15 pF		4.1[1]	7.1[1]	1[1]	7.6[1]	1	7.6	ns
t_{PLH}	RCLK	Q_A – Q_H	C_L = 50 pF		4.9	7.8	1	8.3	1	8.3	ns
t_{PHL}					5.8	8.9	1	9.7	1	9.7	
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 50 pF		5.5	8.6	1	9.1	1	9.1	ns
t_{PHL}					6	9.2	1	10.1	1	10.1	
t_{PHL}	$\overline{RCLR}$	Q_A – Q_H	C_L = 50 pF		6.6	10	1	10.7	1	10.7	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 50 pF		6	9.2	1	10.1	1	10.1	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) Product Preview

5.10 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C[1]

PARAMETER		SN74AHC594			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		1		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.6		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.8		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

(1) Characteristics are for surface-mount packages only.

5.11 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	112	pF

5.12 Typical Characteristics

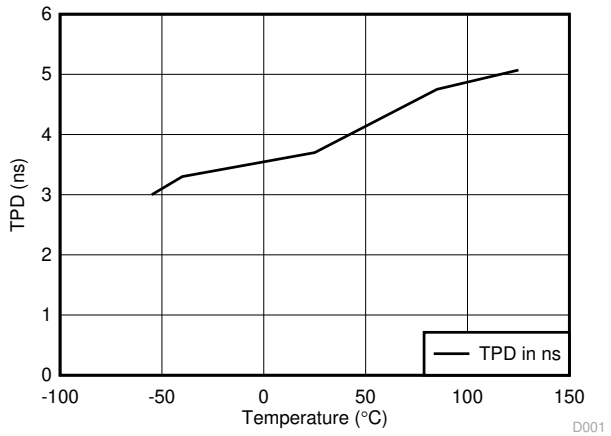


図 5-2. SN74AHC594 TPD vs Temperature, 15 pF Load RCLK to Q

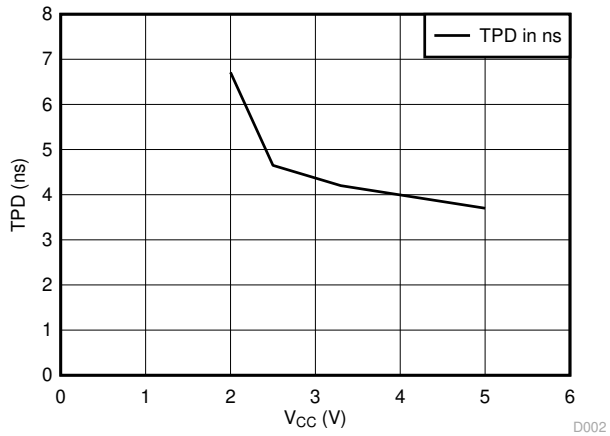
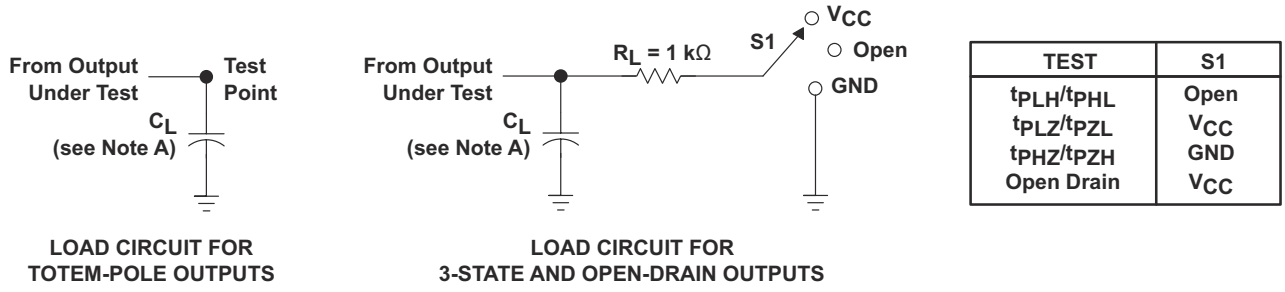


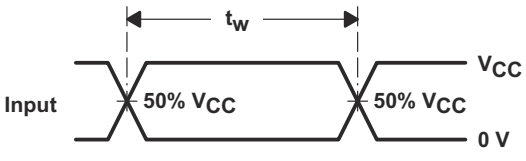
図 5-3. TPD vs V_{CC}

6 Parameter Measurement Information

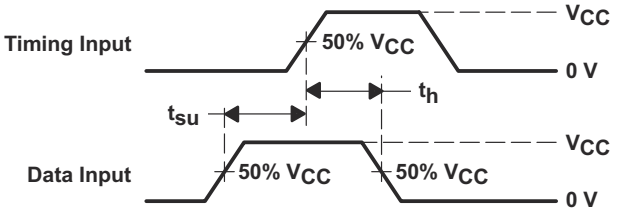


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

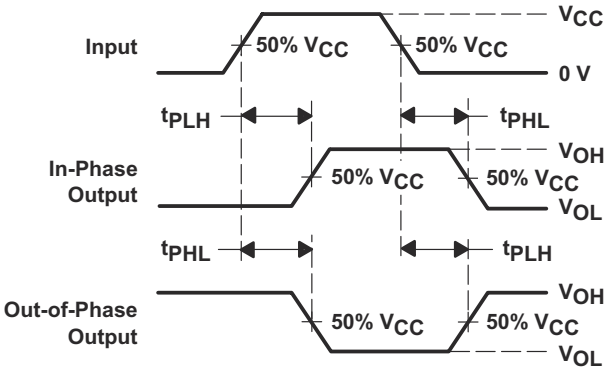
LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



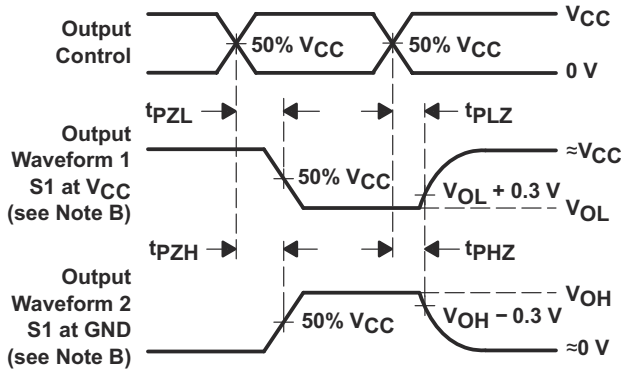
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

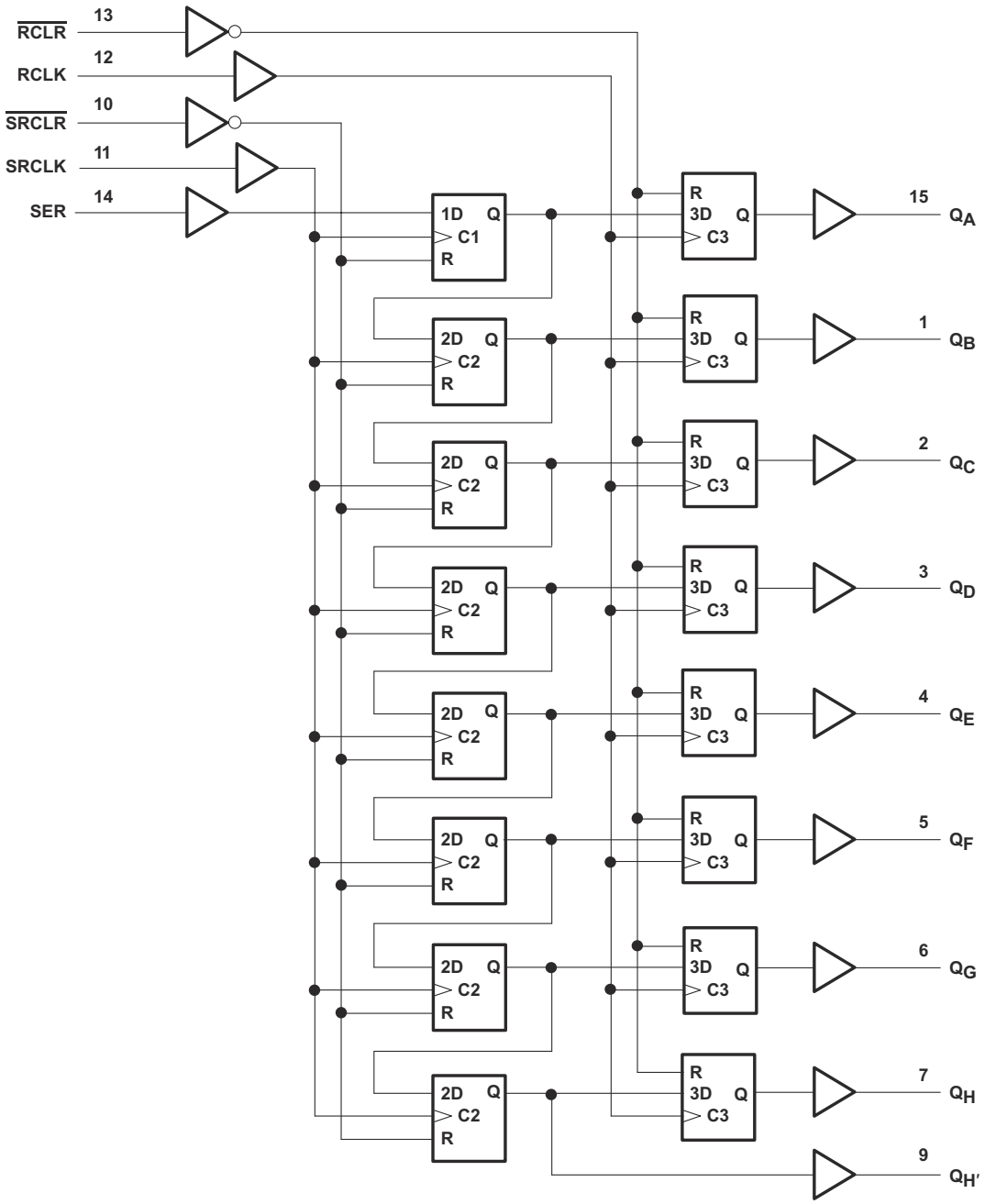
図 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SNx4AHC594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear ($\overline{SRCLR}$, $\overline{RCLR}$) inputs are provided on the shift and storage registers. A serial ($Q_{H'}$) output is provided for cascading purposes. The shift register (SRCLK) and storage register (RCLK) clocks are positive-edge triggered. If the clocks are tied together, the shift register always is one clock pulse ahead of the storage register.

7.2 Functional Block Diagram



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

7.3 Feature Description

- Allows for down translation
  - Inputs are tolerant up to 5.5 V
- Slow edges for reduced noise
- Low power

7.4 Device Functional Modes

表 7-1. Function Table

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{RCLR}}$	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift register data is stored in the storage register.
X	X	X	↓	H	Storage register state is not changed.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The SN74AHC594 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs accept voltages up to 5.5 V allowing down translation to the V_{CC} level. 図 8-2 shows how the slower edges can reduce ringing on the output compared to higher drive parts like AC.

8.2 Typical Application

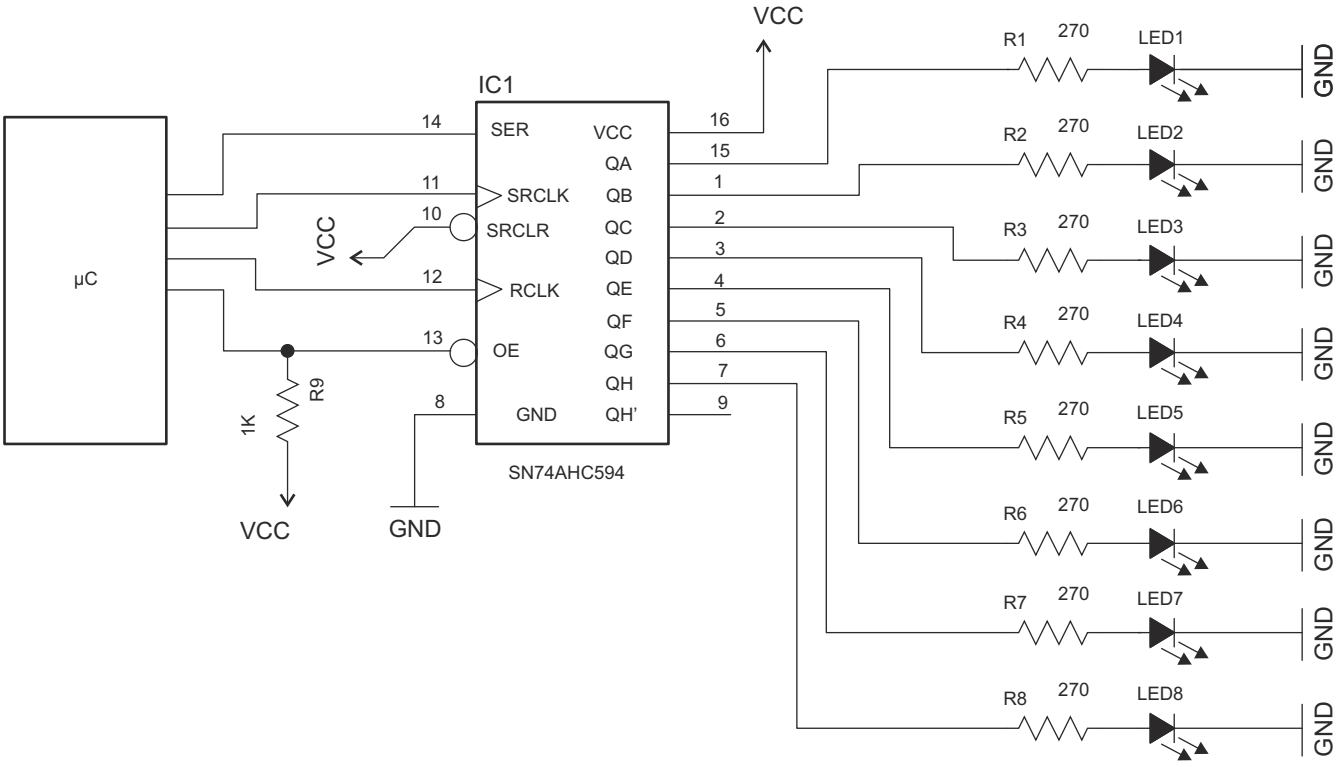


図 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads, so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs: See (Δt/ΔV) in the *Recommended Operating Conditions* table.
   - Specified high and low levels: See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.

2. Recommend Output Conditions
   - Load currents should not exceed 25 mA per output and 75 mA total for the part.
   - Outputs should not be pulled above V_{CC}.

8.2.3 Application Curves

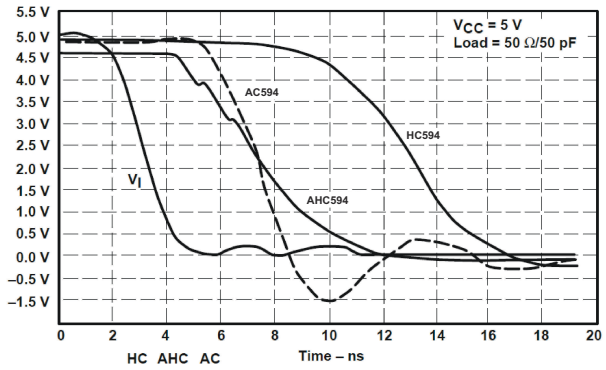


図 8-2. Switching Characteristics Comparison

8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended; if there are multiple V_{CC} pins, then 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and a 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. 図 8-3 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

8.4.2 Layout Example

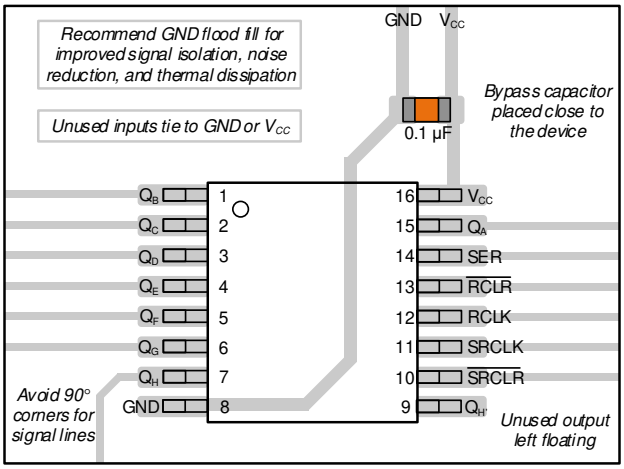


図 8-3. Example Layout for the SN74AHC594

9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHC594	Click here	Click here	Click here	Click here	Click here
SN74AHC594	Click here	Click here	Click here	Click here	Click here

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision G (July 2014) to Revision H (April 2024) — **Page**

- 「製品情報」表にパッケージサイズを追加 、マシン モデルに関する記述を削除、現行のデータシート標準に合わせてレイアウト構造を更新 1
- Updated thermal values for PW package from RθJA = 105.7 to 135.9, RθJC(top) = 40.4 to 70.3, RθJB = 50.7 to 81.3, ΨJT = 3.7 to 22.5 ΨJB = 50.1 to 80.8, all values in °C/W 5

Changes from Revision F (September 2003) to Revision G (July 2014) — **Page**

- ドキュメントを テキサス・インスツルメンツの新しいデータシート規格に更新 1

- 「注文情報」表を削除。 1
- 「アプリケーション」を追加。 1
- Added Pin Functions table. 3
- Added Handling Ratings table. 4
- Changed MAX operating temperature from 85°C to 125°C in Recommended Operating Conditions table. 4
- Added Typical Characteristics section. 9
- Added Detailed Description section. 11
- Added Application and Implementation section. 13
- Added Power Supply Recommendations and Layout sections. 14

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHC594D	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 125	AHC594
SN74AHC594DBR	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA594
SN74AHC594DBR.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA594
SN74AHC594DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC594
SN74AHC594DR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC594
SN74AHC594DRG4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC594
SN74AHC594N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC594N
SN74AHC594N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC594N
SN74AHC594NSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC594
SN74AHC594NSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC594
SN74AHC594PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 125	HA594
SN74AHC594PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HA594
SN74AHC594PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA594

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74AHC594 :

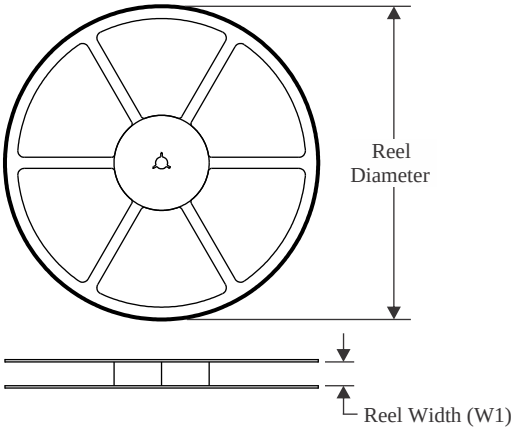
- Automotive : SN74AHC594-Q1

NOTE: Qualified Version Definitions:

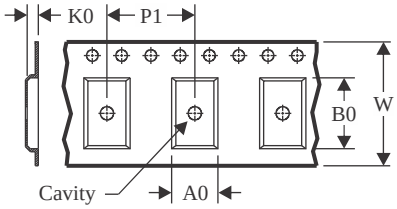
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

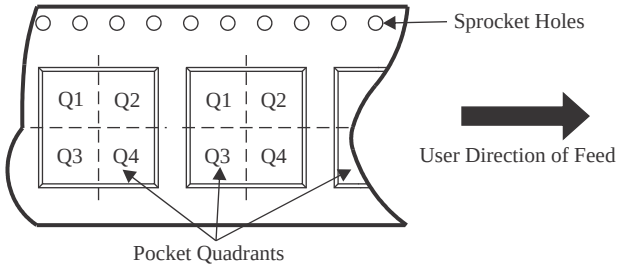


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

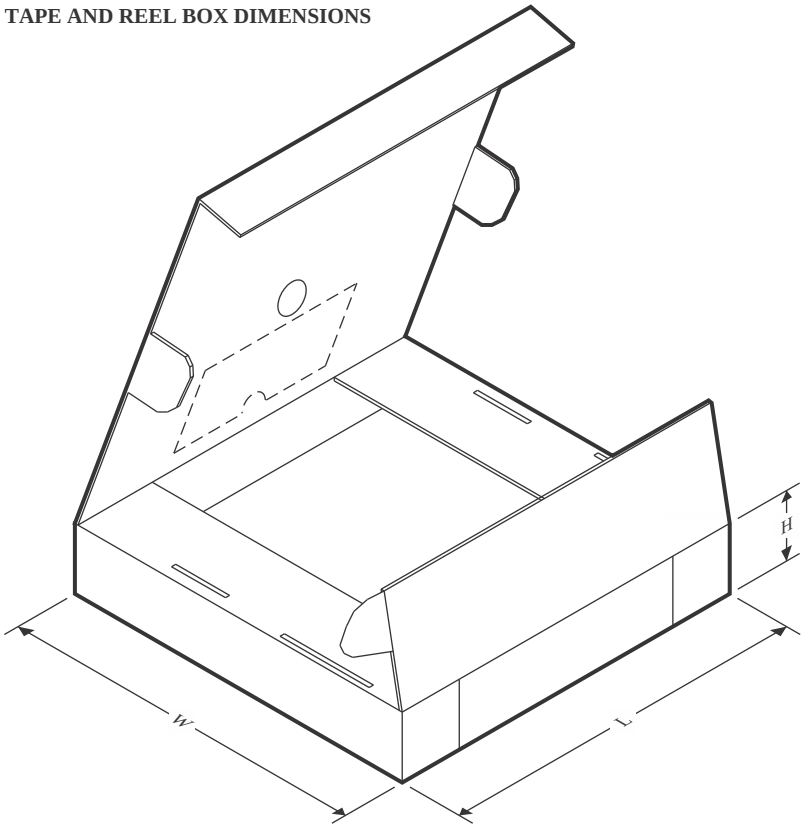
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC594DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC594DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHC594NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74AHC594PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC594PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

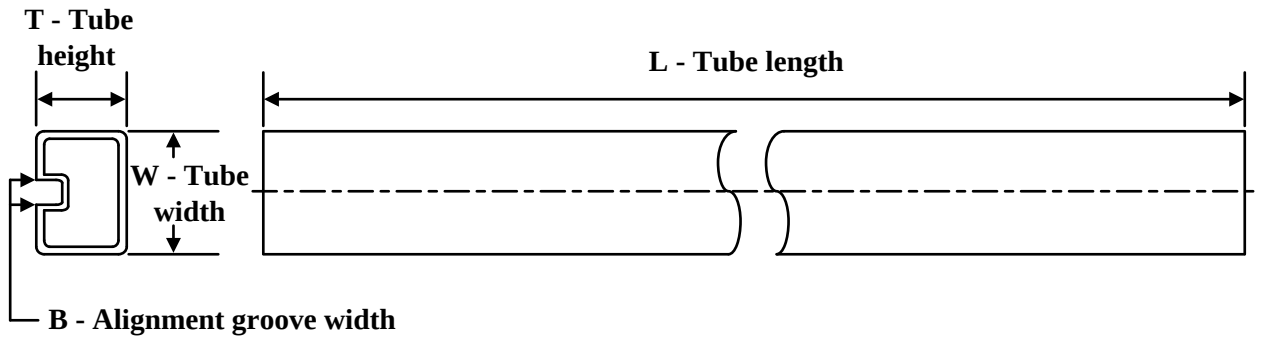
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

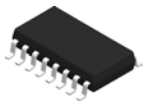
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC594DBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74AHC594DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74AHC594NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74AHC594PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74AHC594PWR	TSSOP	PW	16	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74AHC594N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC594N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC594N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC594N.A	N	PDIP	16	25	506	13.97	11230	4.32

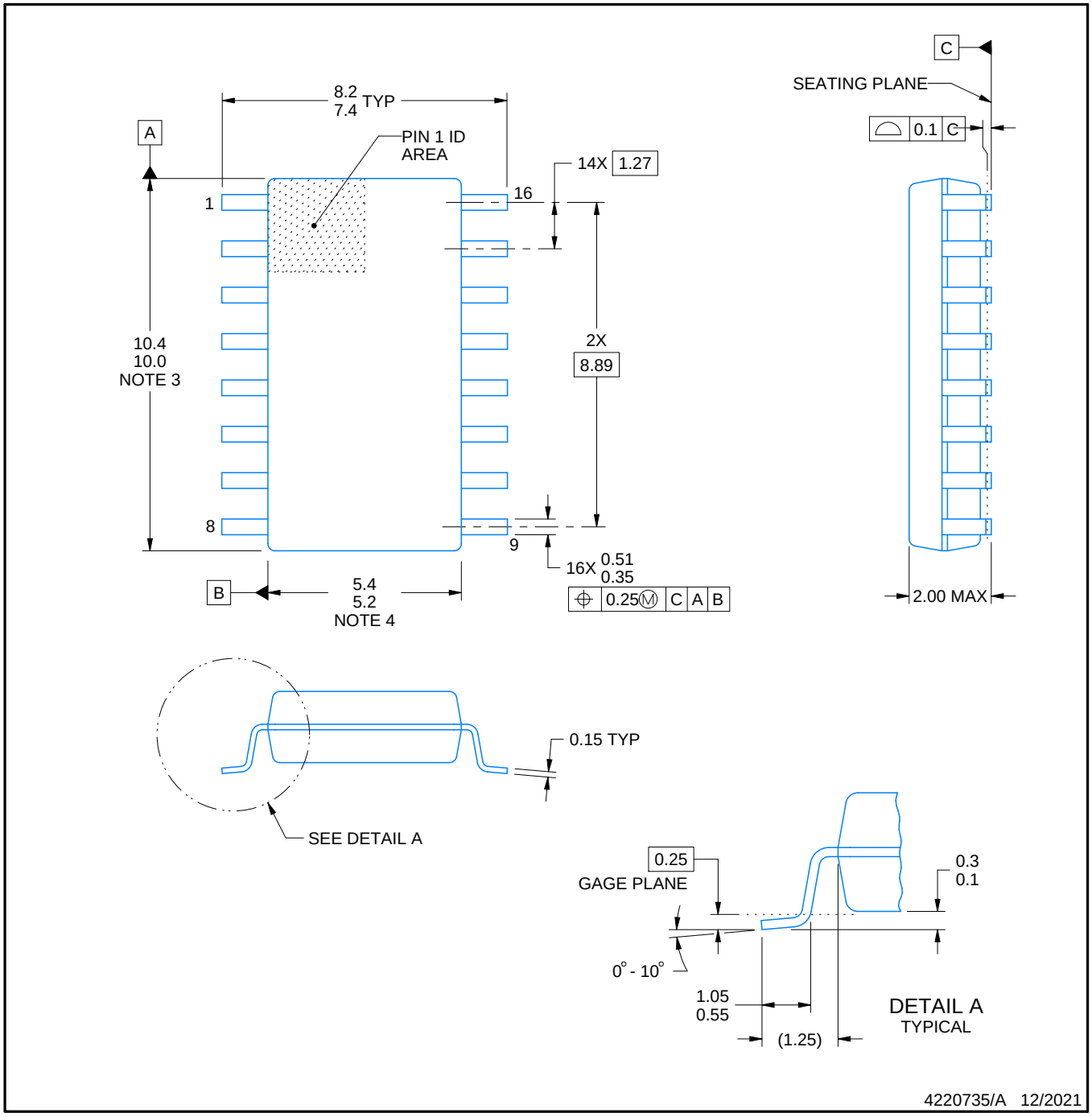


PACKAGE OUTLINE

NS0016A

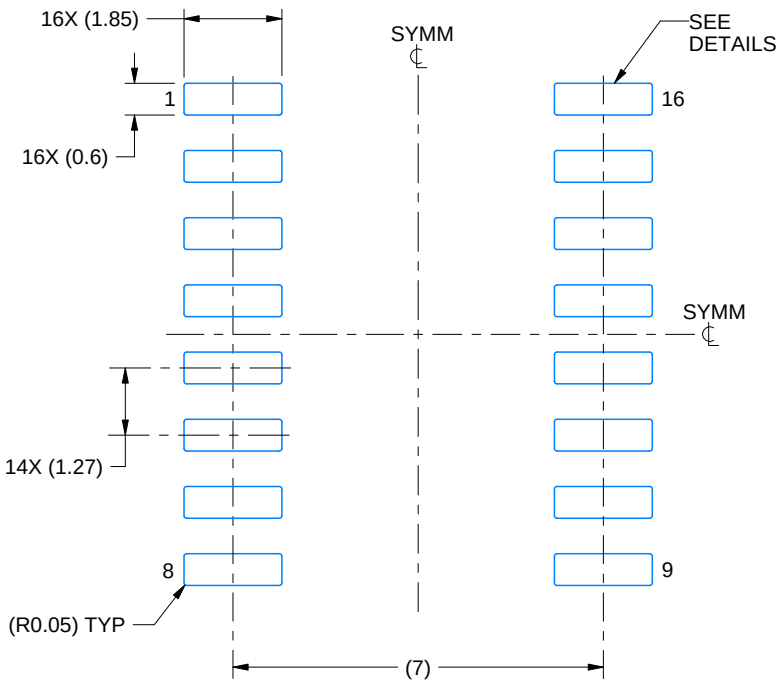
SOP - 2.00 mm max height

SOP

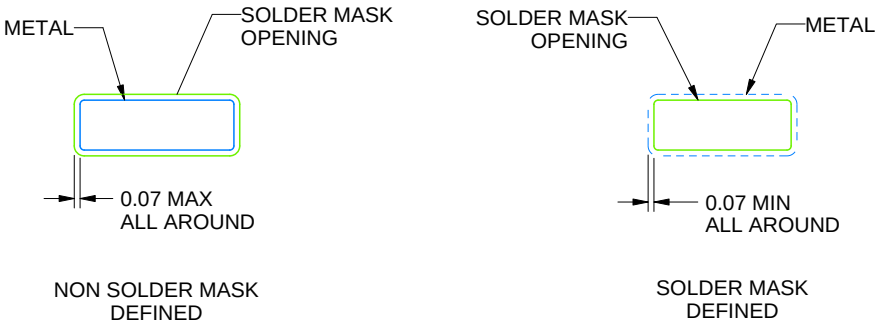


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

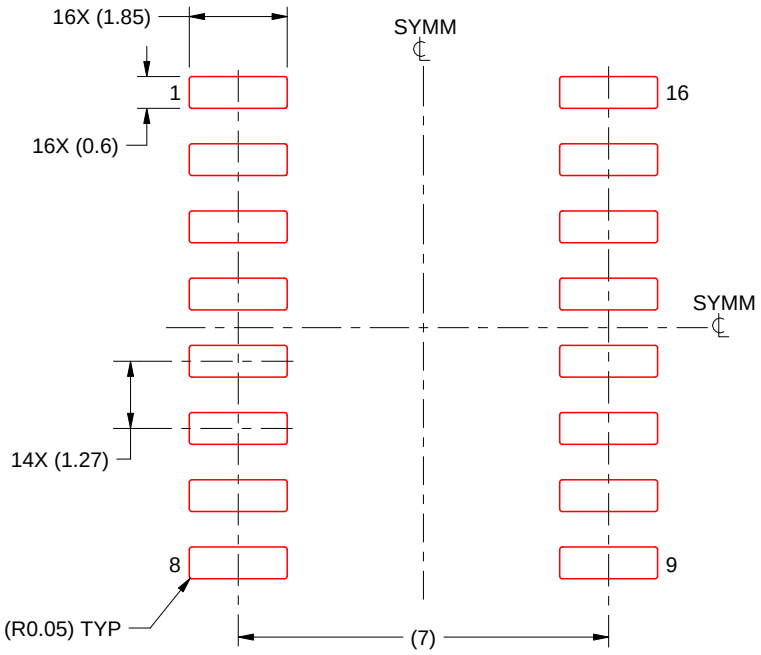
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



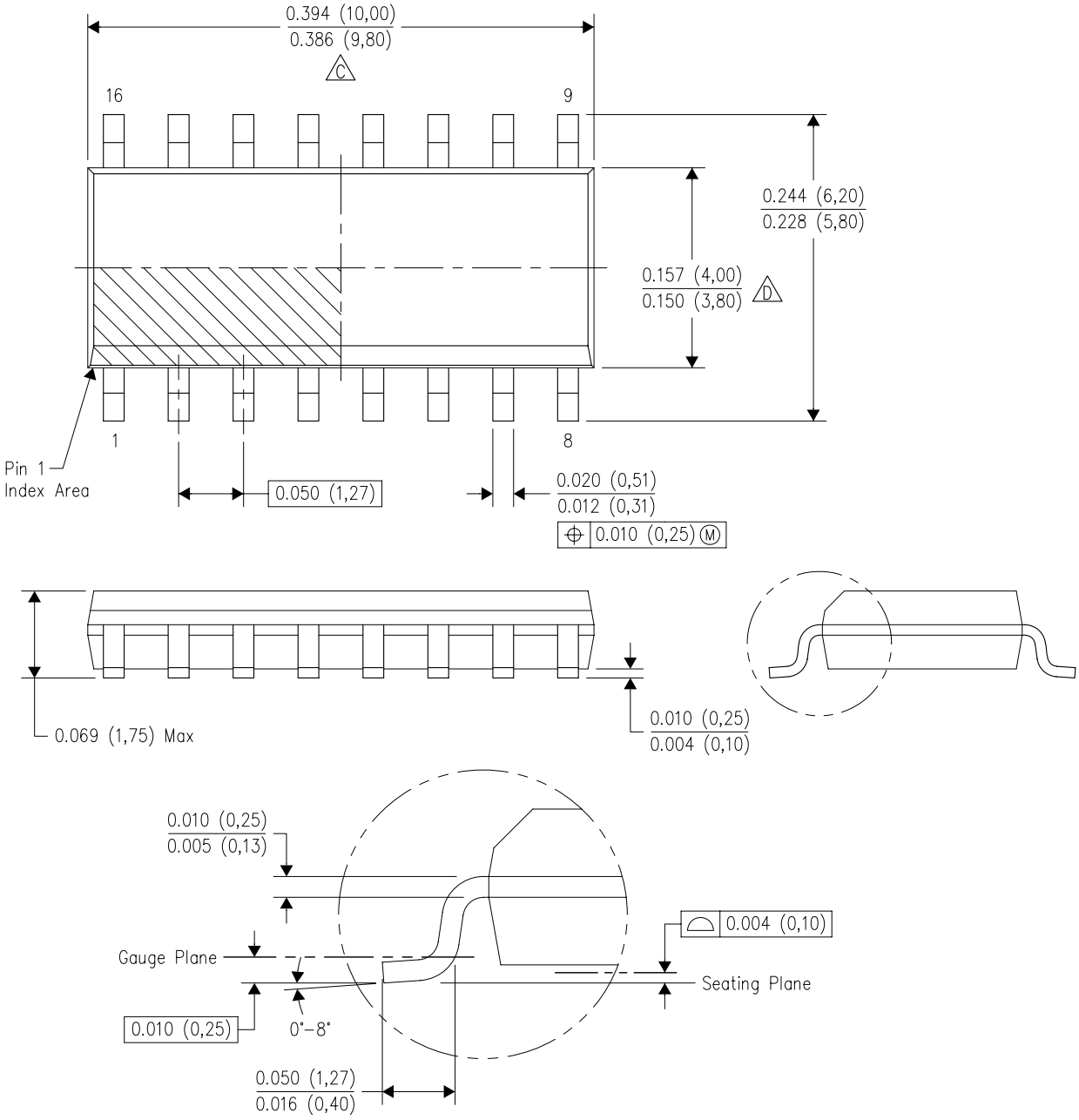
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



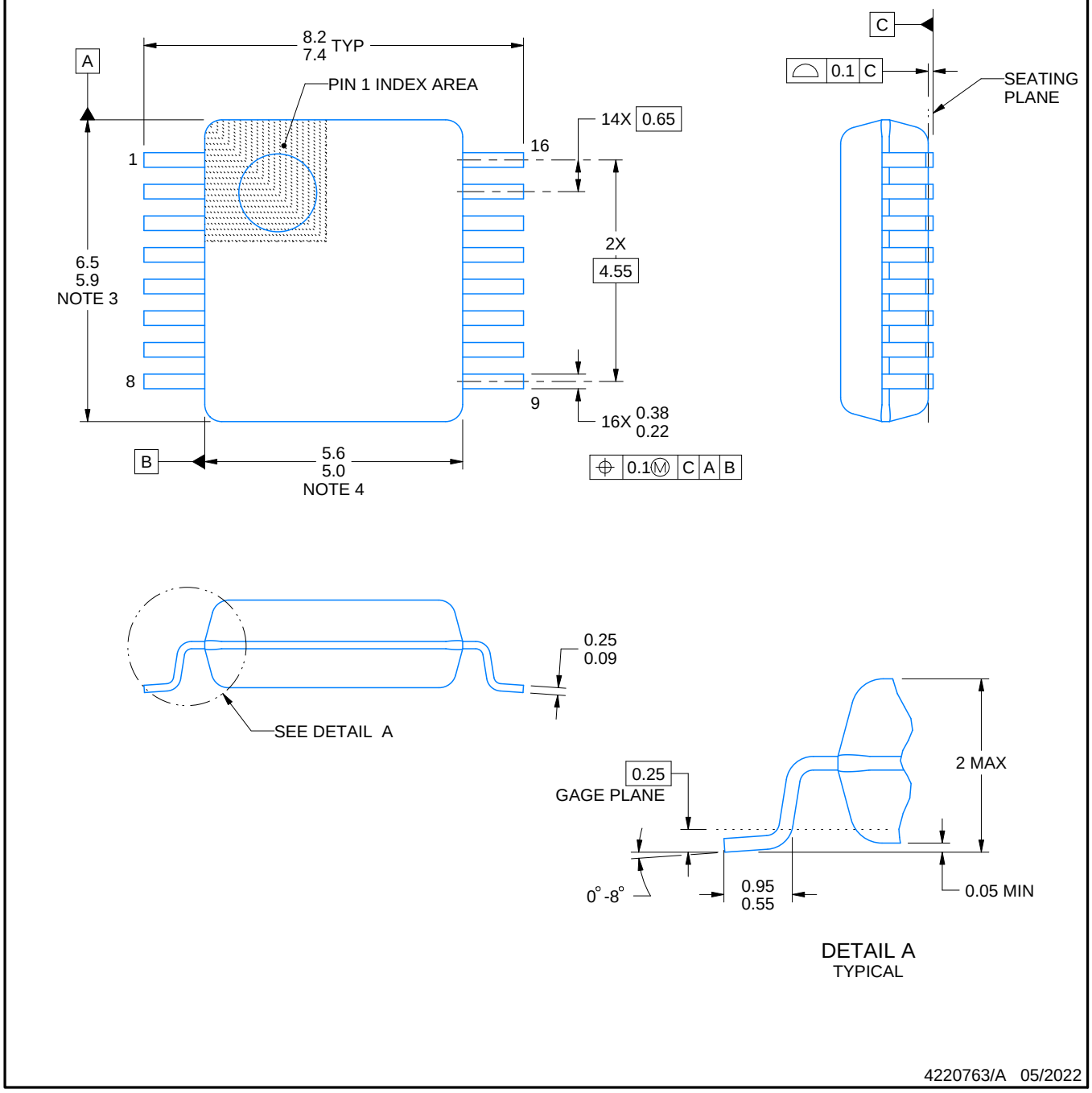
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

DB0016A

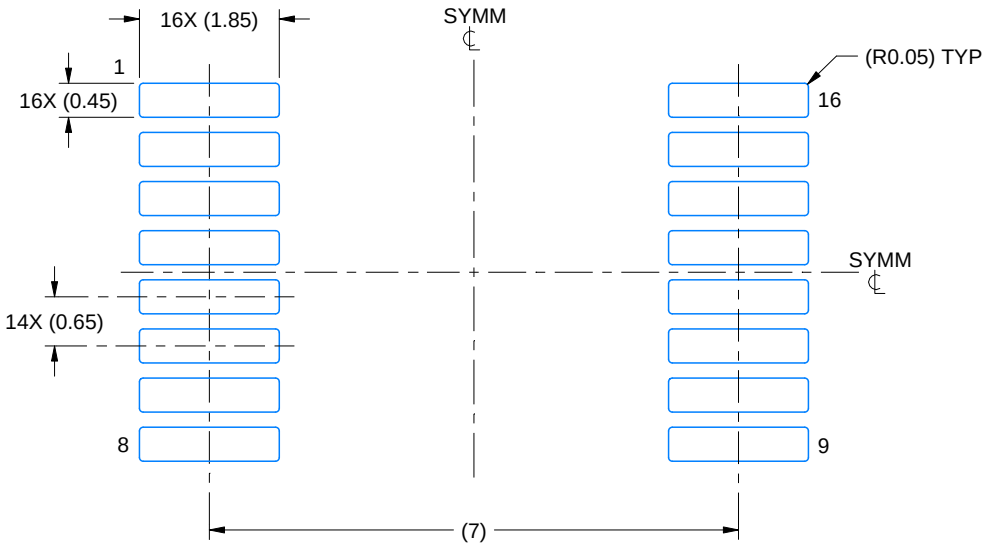
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

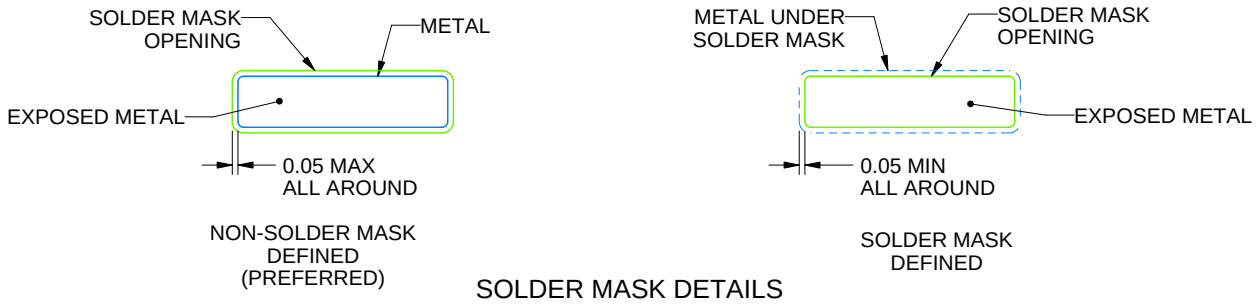


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

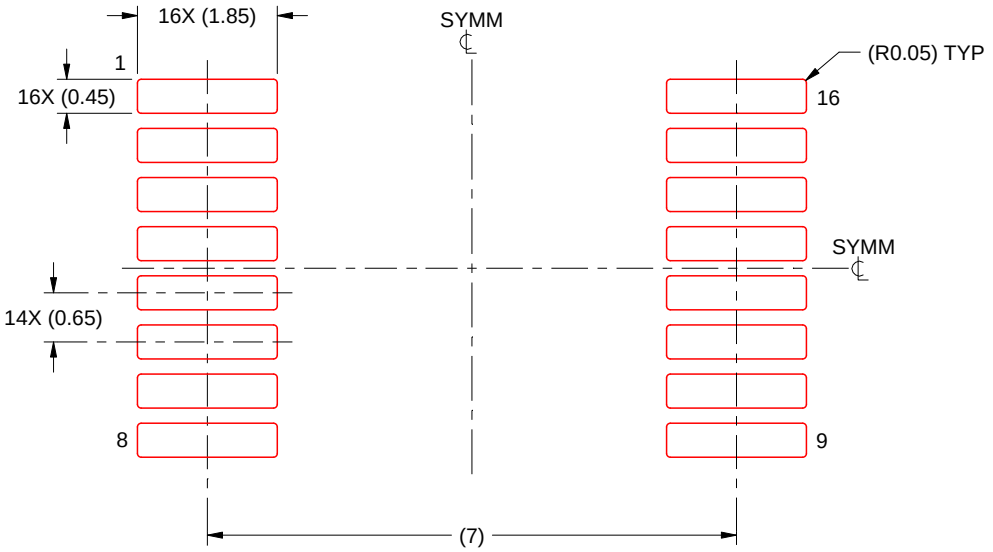


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

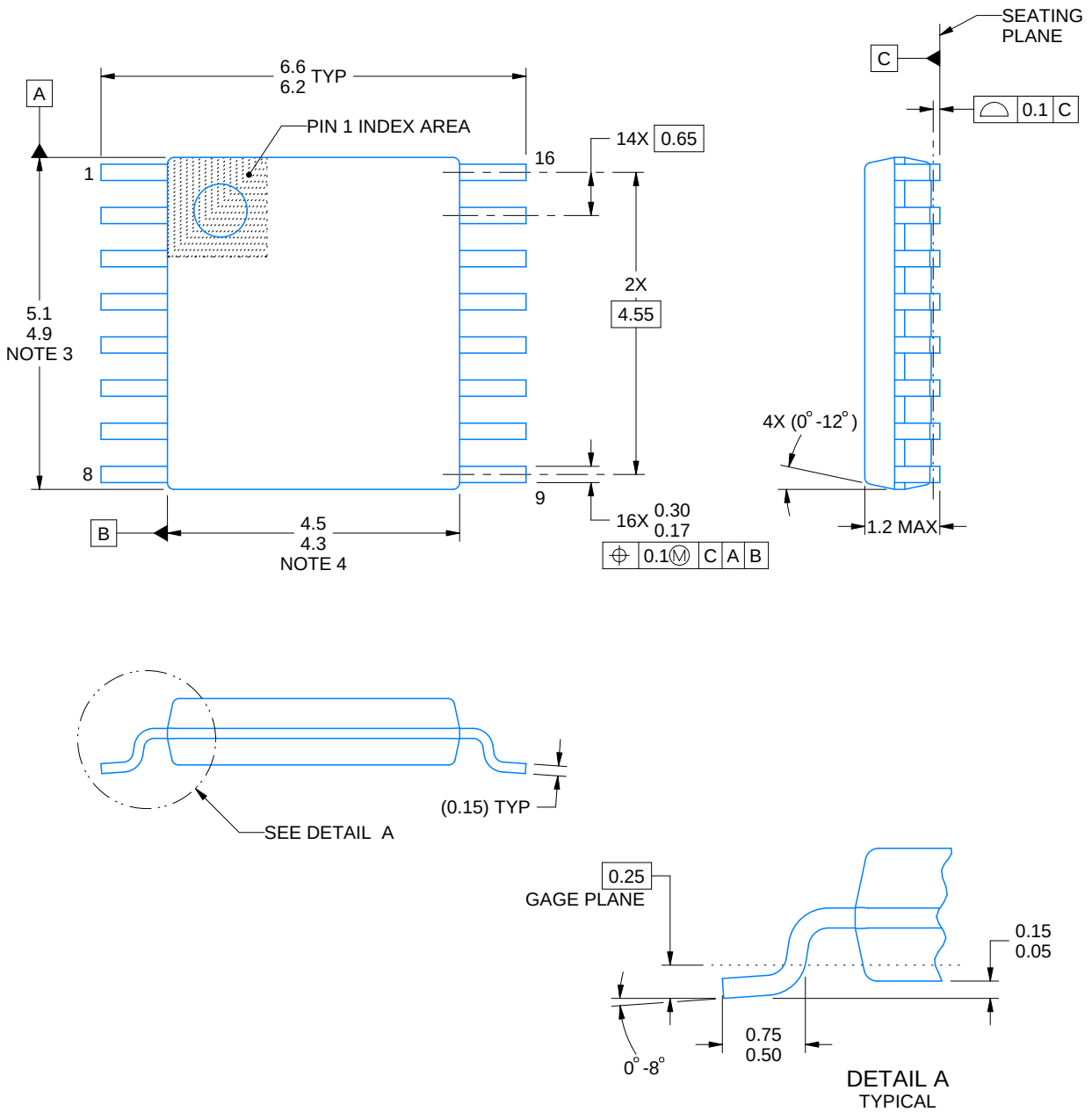
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0016A

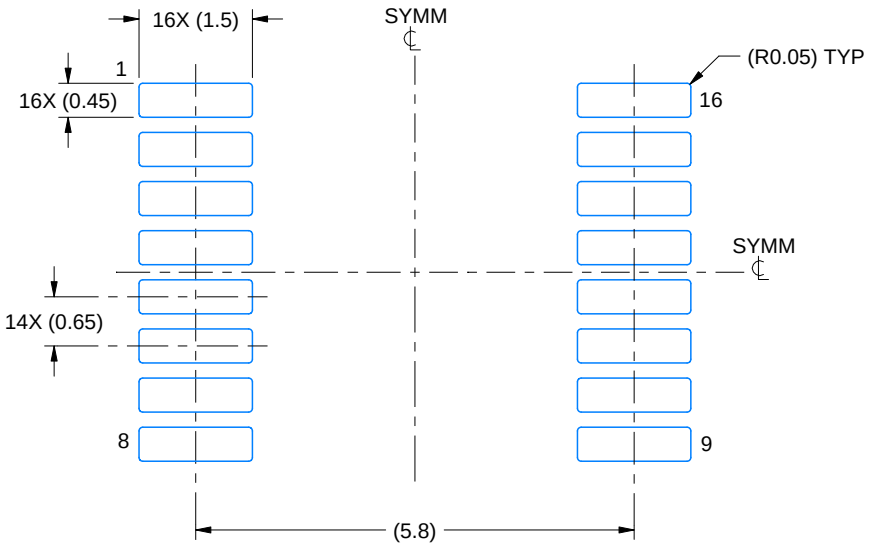
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



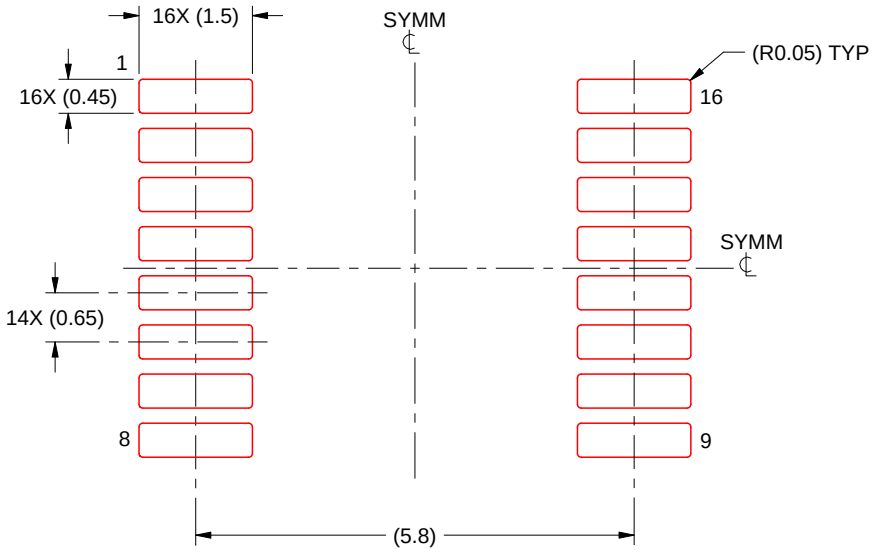
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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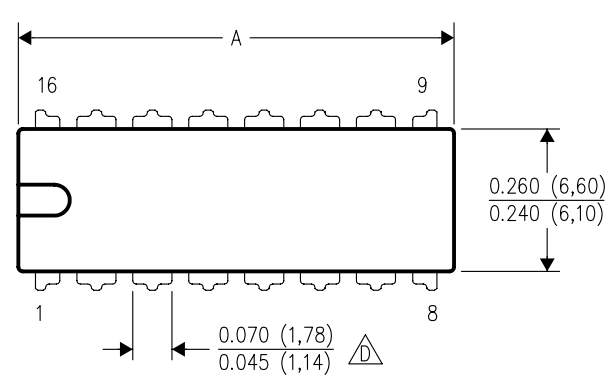
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

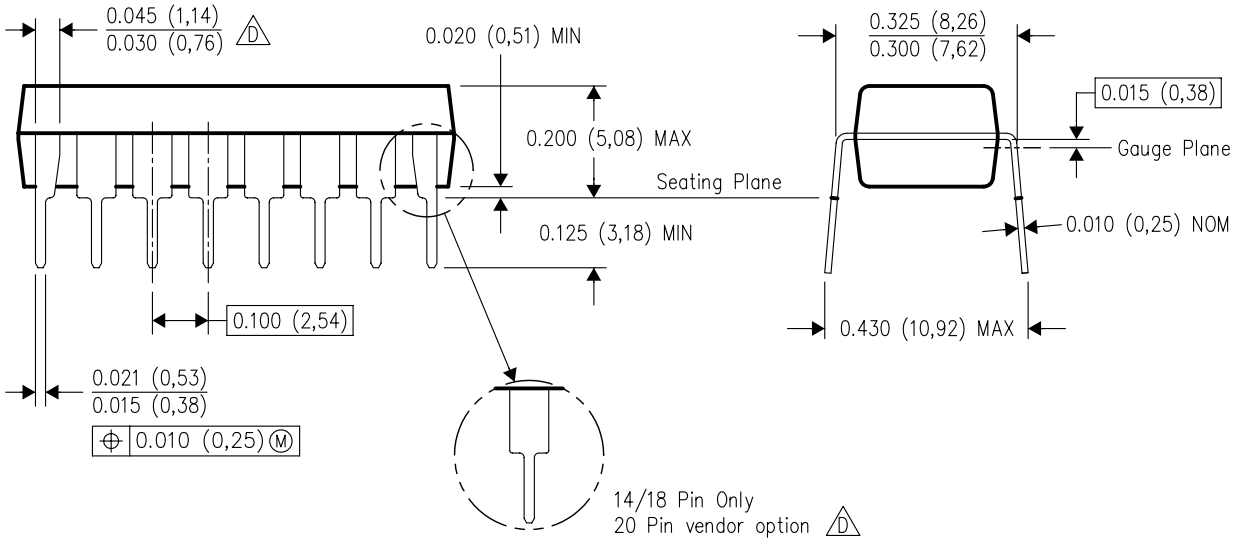
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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最終更新日：2025 年 10 月