SN74AHCT1G125 3 ステート出力搭載シングルバス バッファ ゲート

1 特長

- 動作範囲:4.5V～5.5V
- 最大 t_{pd} 6ns (5V 時)
- 低消費電力、最大 I_{CC}:10µA
- 5V で ±8mA の出力駆動能力
- 入力は TTL 電圧互換
- JESD 17 準拠
  250mA 超のラッチアップ性能

2 アプリケーション

- ワイヤレス・インフラストラクチャ
- サーバー
- 電力インフラストラクチャ
- PC とノート PC
- プログラマブル・ロジック・コントローラ
- 試験および測定機器

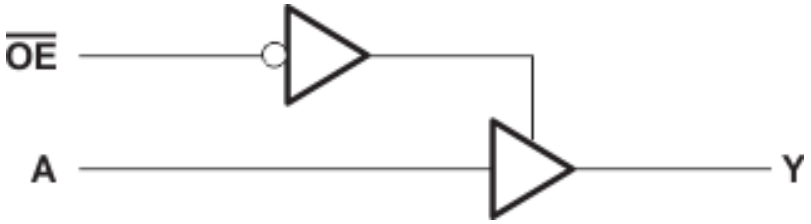
3 概要

SN74AHCT1G125 デバイスは、3 ステート出力を搭載したシングル バス バッファ ゲート / ライン ドライバです。出力イネーブル ($\overline{OE}$) 入力が High の場合、出力はディセーブルされます。$\overline{OE}$ が Low の場合、データが A 入力から Y 出力に渡されます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)	本体サイズ (3)
SN74AHCT1G125	DBV (SOT-23、5)	2.9mm x 2.8mm	2.9mm x 1.6mm
	DCK (SC-70、5)	2mm x 2.1mm	2mm x 1.25mm
	DRL (SOT-553、5)	1.6mm x 1.6mm	1.6mm x 1.2mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。



概略回路図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

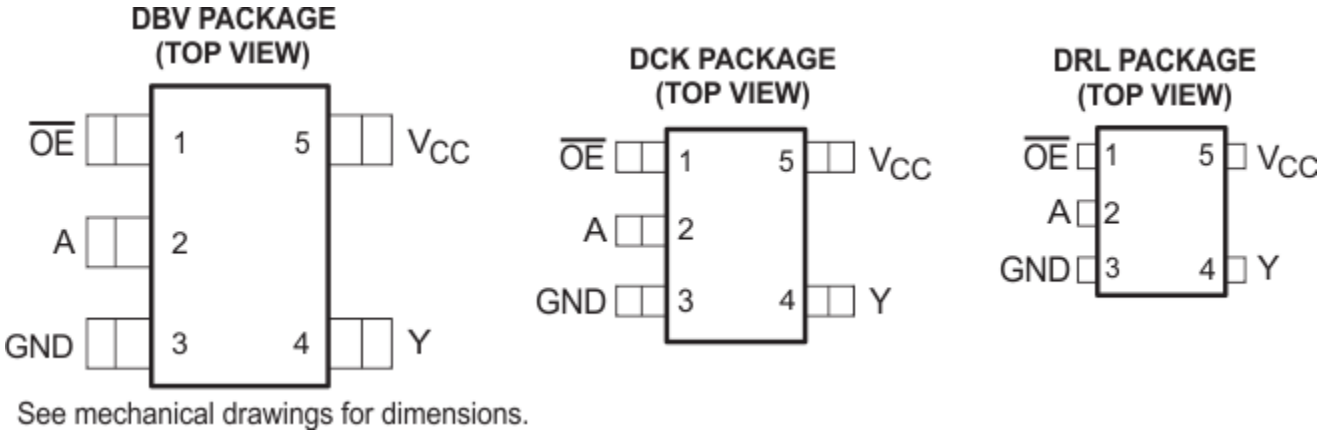


表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	$\overline{OE}$	I	Output Enable
2	A	I	Input A
3	GND	—	Ground Pin
4	Y	O	Output Y
5	V_{CC}	—	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I (2)	Input voltage range		–0.5	7	V
V_O (2)	Output voltage range		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous channel current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		–65	150	°C
T_j	Junction temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *セクション 5.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

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5.4 Thermal Information

THERMAL METRIC[1]		DBV	DCK	DRL	UNIT
		5 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	278	289.2	328.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	180.5	205.8	105.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	184.4	176.2	150.3	
ψ_{JT}	Junction-to-top characterization parameter	115.4	117.6	6.9	
ψ_{JB}	Junction-to-board characterization parameter	183.4	175.1	148.4	
$R_{\theta JC(bot)}$	Junction-to-case (bot) thermal resistance	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High level output voltage	I_{OH} = –50 µA	4.5 V	4.4	4.5		4.4		4.4		V
		I_{OH} = –8 mA		3.94			3.8		3.8		
V_{OL}	Low level output voltage	I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
		I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	Input leakage current	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1		±1	µA
I_{OZ}	Off-State (High-Impedance State) Output Current (of a 3-State Output)	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5		±2.5	µA
I_{CC}	Supply current	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			1		10		10	µA
ΔI_{CC} [1]	Supply-current change	One input at 3.4 V, Other input at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C_i	Input capacitance	$V_I = V_{CC}$ or GND	5 V		4	10		10		10	pF
C_o	Output capacitance	$V_O = V_{CC}$ or GND	5 V		10						pF

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

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5.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		3.8	5.5	1	6.5	1	7	ns
t_{PHL}					3.8	5.5	1	6.5	1	7	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		3.6	5.1	1	6	1	6.5	ns
t_{PZL}					3.6	5.1	1	6	1	6.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		4.6	6.8	1	8	1	8.5	ns
t_{PLZ}					4.6	6.8	1	8	1	8.5	
t_{PLH}	A	Y	C_L = 50 pF		5.3	7.5	1	8.5	1	9.5	ns
t_{PHL}					5.3	7.5	1	8.5	1	9.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		5.1	7.1	1	8	1	9	ns
t_{PZL}					5.1	7.1	1	8	1	9	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6.1	8.8	1	10	1	11	ns
t_{PLZ}					6.1	8.8	1	10	1	11	

5.7 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	14	pF

5.8 Typical Characteristics

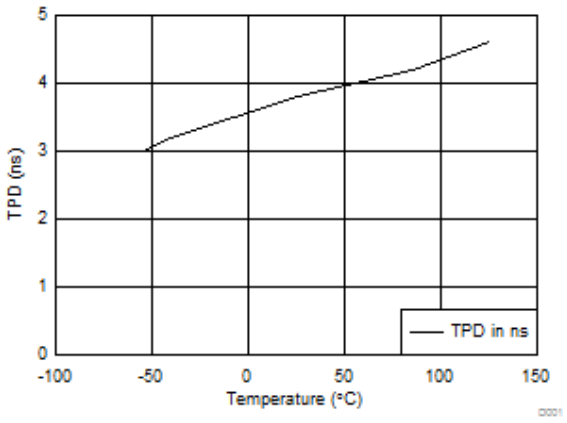
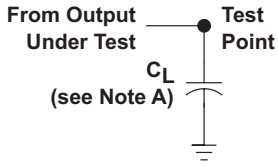


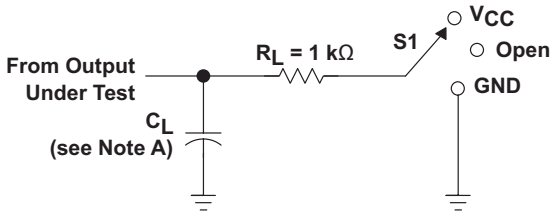
図 5-1. TPD vs Temperature

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6 Parameter Measurement Information

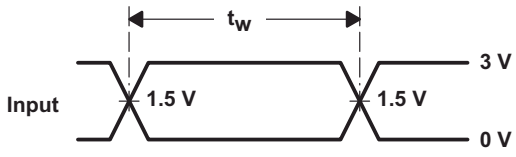


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

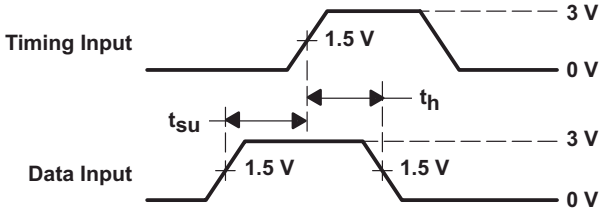


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

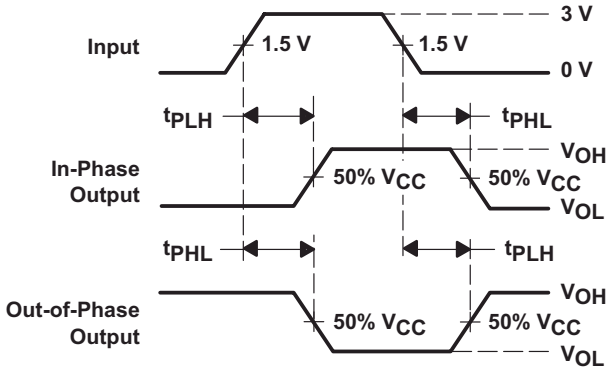
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



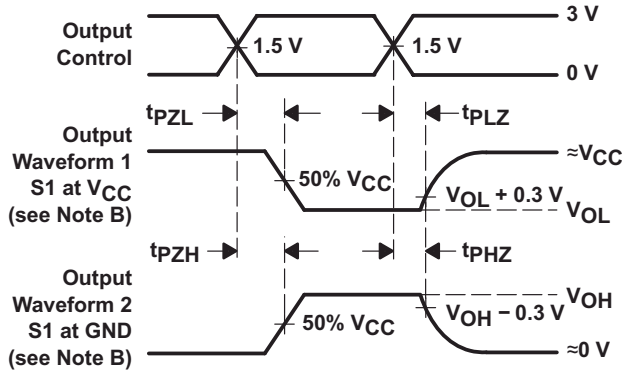
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

図 6-1. Load Circuit and Voltage Waveforms

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7 Detailed Description

7.1 Overview

The SN74AHCT1G125 device is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable ($\overline{OE}$) input is high. When $\overline{OE}$ is low, data is passed from the A input to the Y output.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram

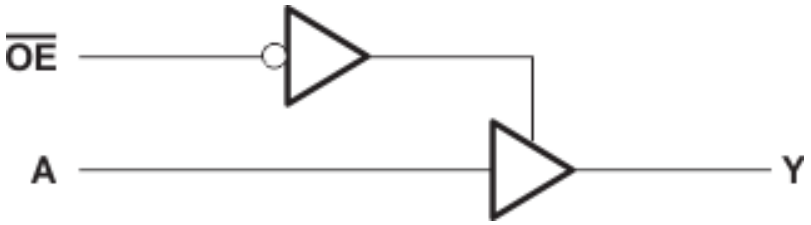


図 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

- TTL inputs
  - Lowered switching threshold allows up translation 3.3 V to 5 V
- Slow edges reduce output ringing

7.4 Device Functional Modes

表 7-1. Function Table

INPUTS(1)		OUTPUT(2)
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

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8 Application and Implementation

注

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8.1 Application Information

The SN74AHCT1G125 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8 V V_{IL} and 2V V_{IH}. This feature makes it Ideal for translating up from 3.3 V to 5 V. 図 8-1 shows this type of translation.

8.2 Typical Application

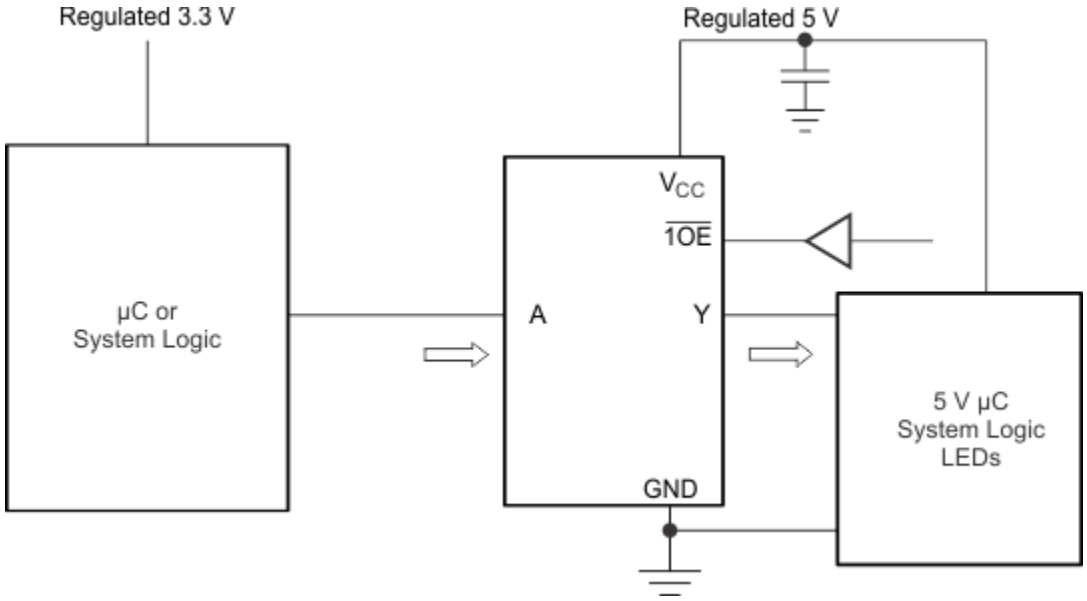


図 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For rise time and fall time specifications, see Δt/ΔV in the *セクション 5.3* table.
   - For specified High and low levels, see V_{IH} and V_{IL} in the *セクション 5.3* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommend Output Conditions
   - Load currents should not exceed 25 mA per output and 50 mA total for the part.
   - Outputs should not be pulled above V_{CC}.

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8.2.3 Application Curves

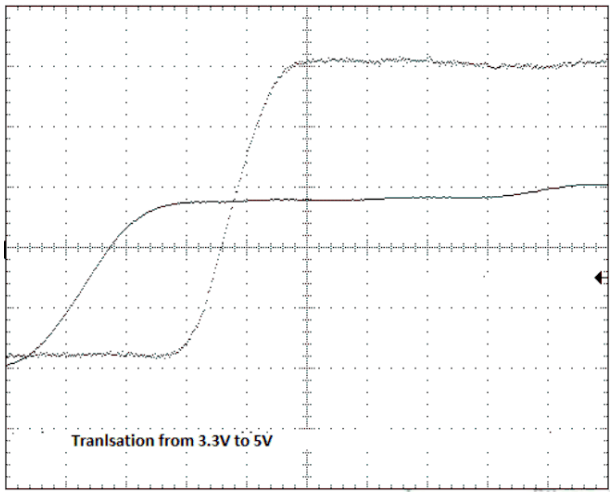


図 8-2. Translation from 3.3 V to 5 V

8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *セクション 5.3* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple V_{CC} pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in 図 8-3 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

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8.4.1.1 Layout Example

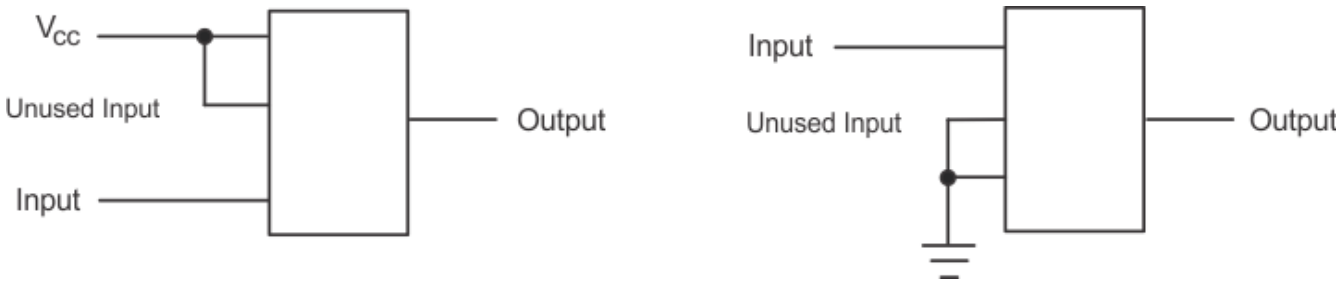


図 8-3. Layout Diagram

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.3 Trademarks

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9.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

Changes from Revision O (October 2023) to Revision P (March 2024)	Page
• パッケージ情報表に本体サイズを追加	1
• Updated thermal values for DBV package from RθJA = 231.3 to 278, RθJC(top) = 119.9 to 180.5, RθJB = 60.6 to 184.4, ΨJT = 17.8 to 115.4, ΨJB = 60.1 to 183.4, RθJC(bot) = N/A, all values in °C/W	5

Changes from Revision N (January 2016) to Revision O (October 2023)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• Updated thermal values for DCK package from RθJA = 287.6 to 289.2, RθJC(top) = 97.7 to 205.8, RθJB = 65 to 176.2, ΨJT = 2.0 to 117.6, ΨJB = 64.2 to 175.1, RθJC(bot) = N/A, all values in °C/W	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74AHCT1G125DBVRG4	Last Time Buy	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B25G
74AHCT1G125DBVRG4.A	Last Time Buy	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B25G
74AHCT1G125DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B25G
74AHCT1G125DBVTG4.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B25G
74AHCT1G125DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BM3
74AHCT1G125DCKRG4.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BM3
74AHCT1G125DCKTE4	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BM3
74AHCT1G125DCKTG4	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BM3
74AHCT1G125DCKTG4.A	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BM3
SN74AHCT1G125DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	(37QH, 3BEF, B253, B25G, B25J, B 25L, B25S)
SN74AHCT1G125DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(37QH, 3BEF, B253, B25G, B25J, B 25L, B25S)
SN74AHCT1G125DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	(B253, B25G, B25J, B25S)
SN74AHCT1G125DCK3	Last Time Buy	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 85	BMY
SN74AHCT1G125DCK3.A	Last Time Buy	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 85	BMY
SN74AHCT1G125DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1QK, BM3, BMG, BM J, BML, BMS)
SN74AHCT1G125DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1QK, BM3, BMG, BM J, BML, BMS)
SN74AHCT1G125DCKT	Obsolete	Production	SC70 (DCK) | 5	-	-	Call TI	Call TI	-40 to 125	(BM3, BMG, BMJ, BM S)
SN74AHCT1G125DRLR	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(BMB, BMS)
SN74AHCT1G125DRLR.A	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(BMB, BMS)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74AHCT1G125 :

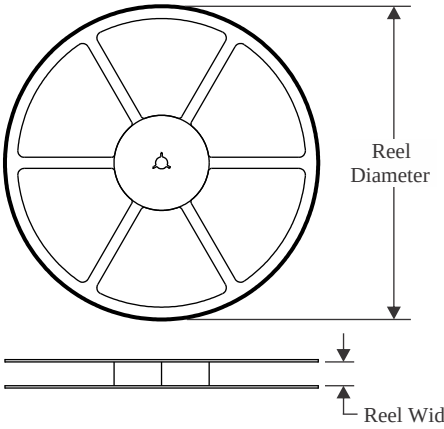
- Automotive : SN74AHCT1G125-Q1

NOTE: Qualified Version Definitions:

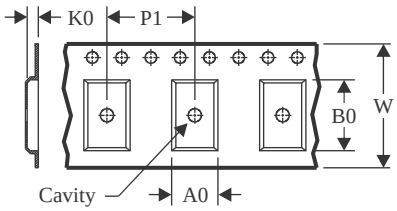
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

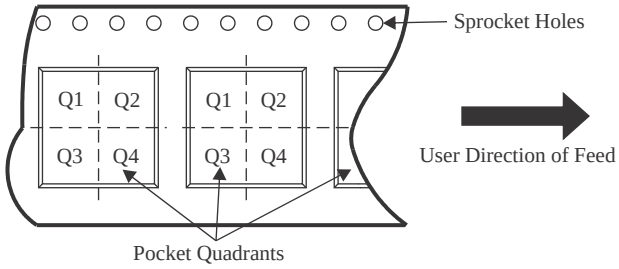


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

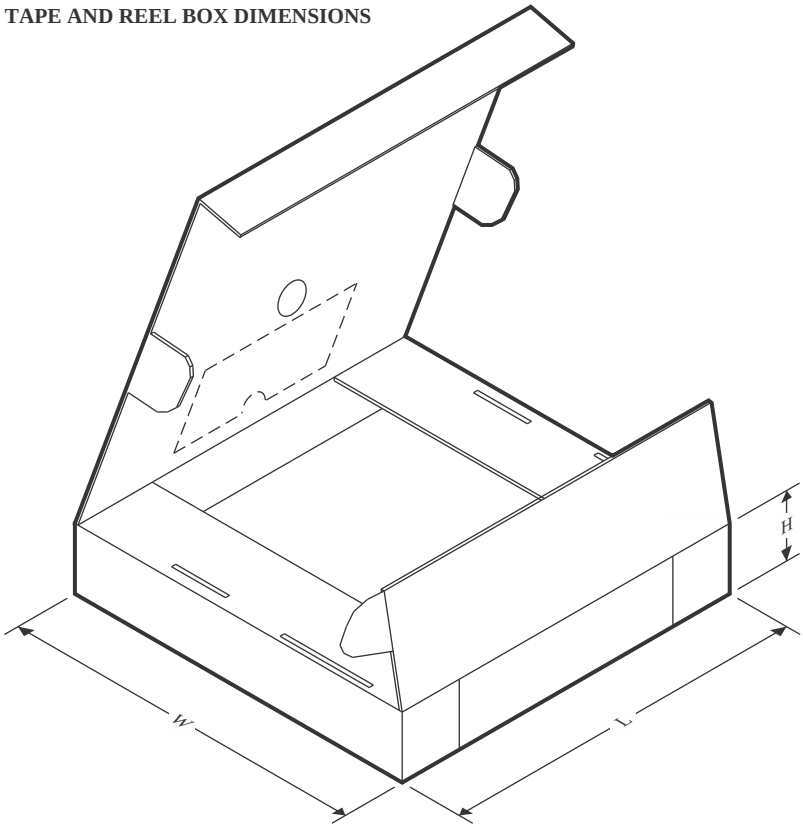
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AHCT1G125DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
74AHCT1G125DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
74AHCT1G125DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
74AHCT1G125DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHCT1G125DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHCT1G125DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHCT1G125DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHCT1G125DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74AHCT1G125DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

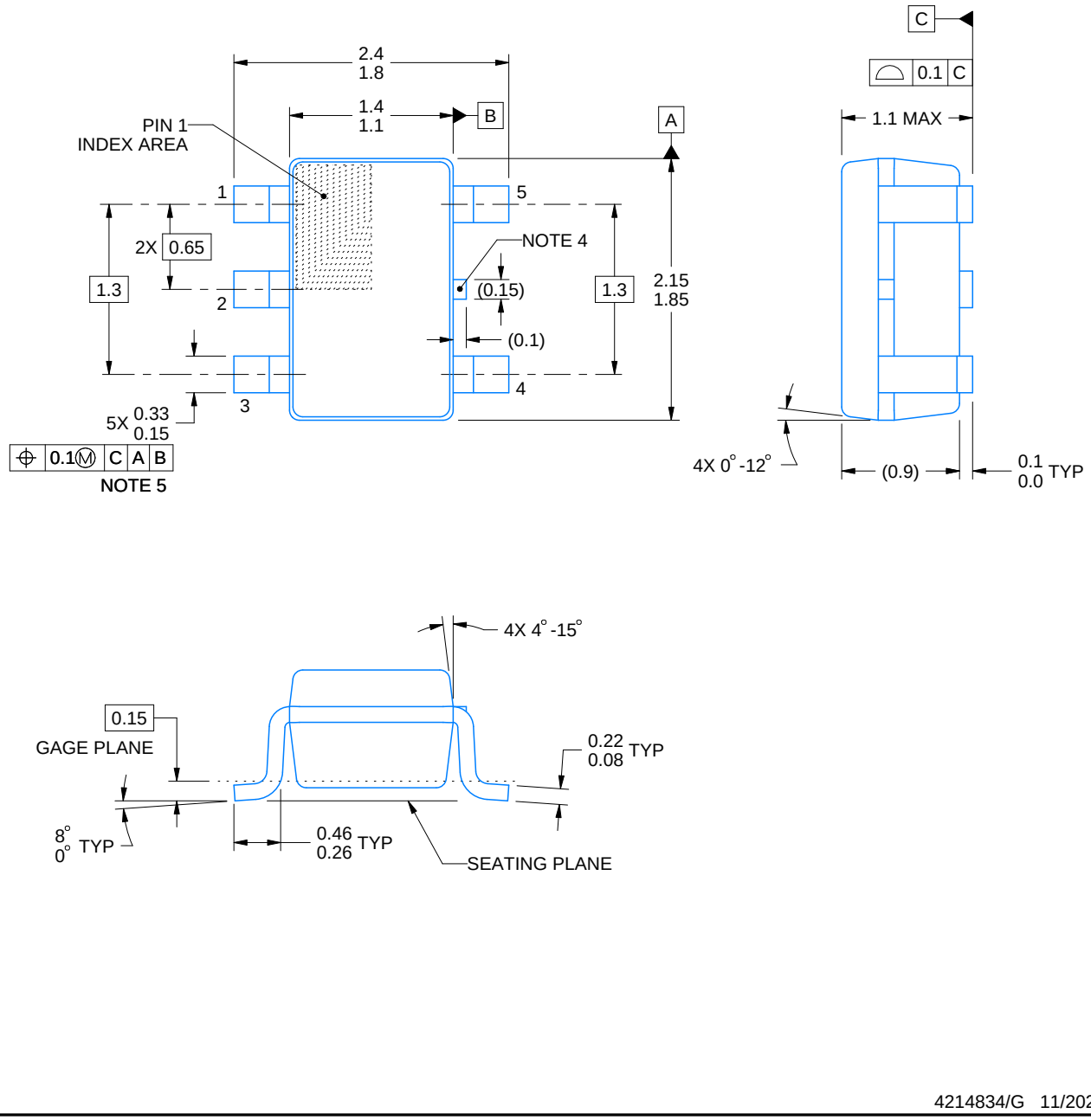
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AHCT1G125DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
74AHCT1G125DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
74AHCT1G125DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
74AHCT1G125DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHCT1G125DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AHCT1G125DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74AHCT1G125DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AHCT1G125DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74AHCT1G125DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

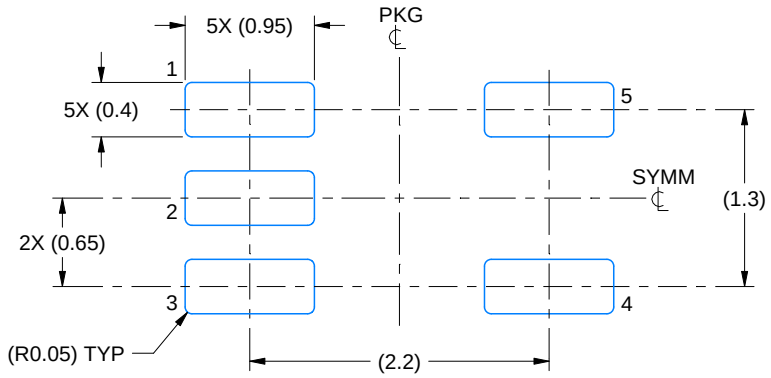
SMALL OUTLINE TRANSISTOR



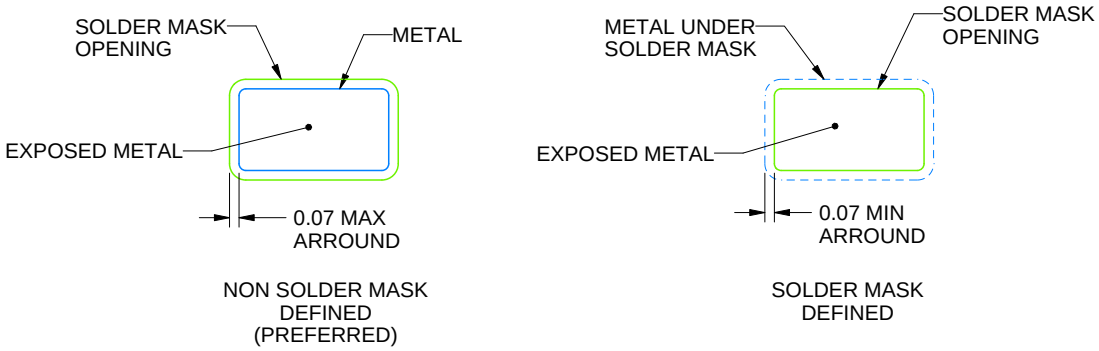
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

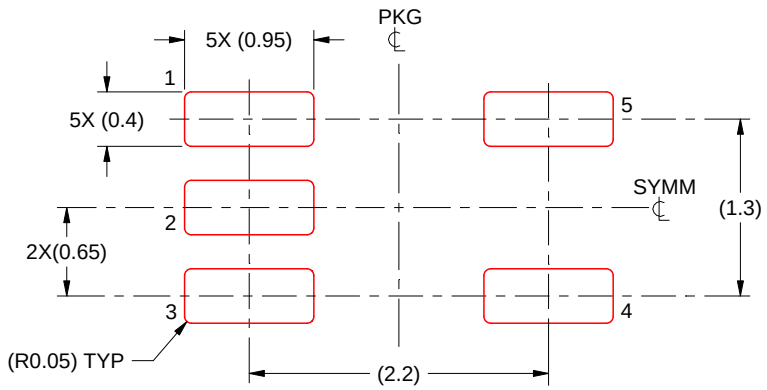


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

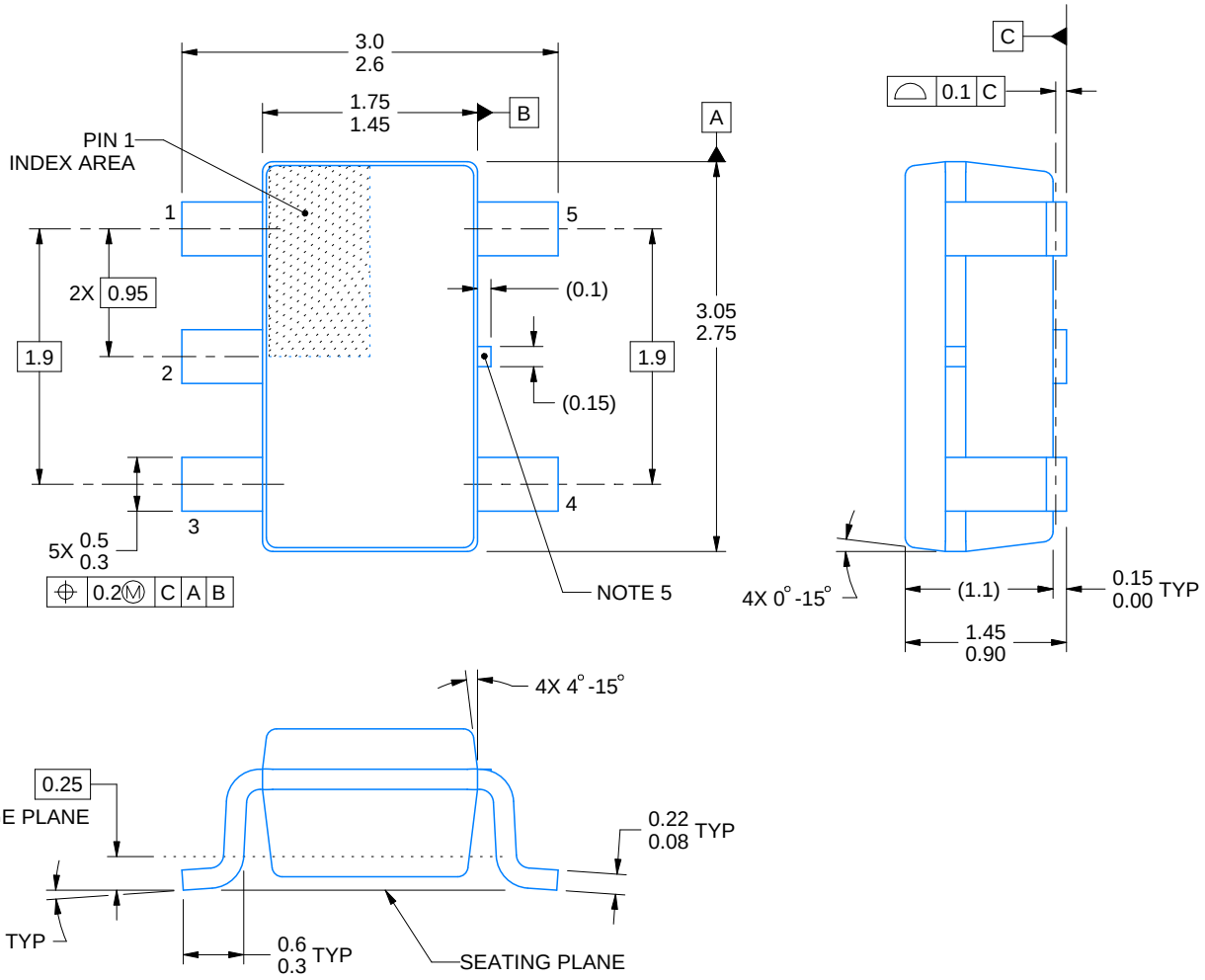
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

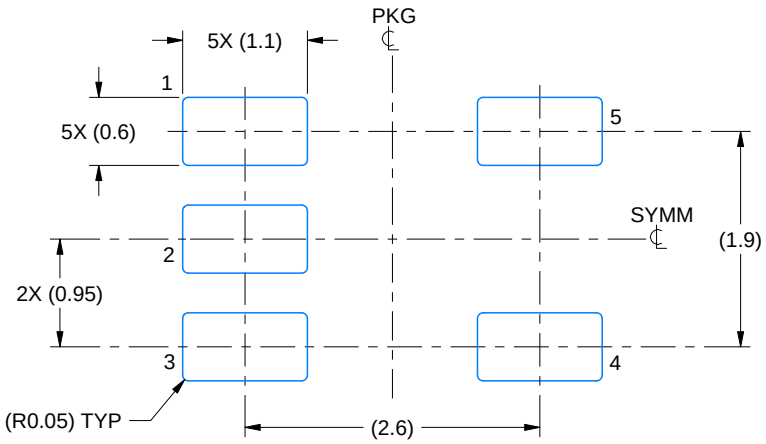
SMALL OUTLINE TRANSISTOR



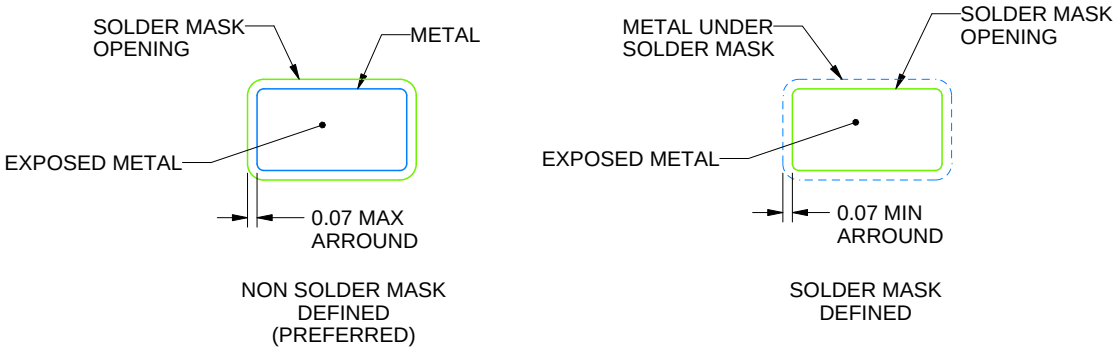
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

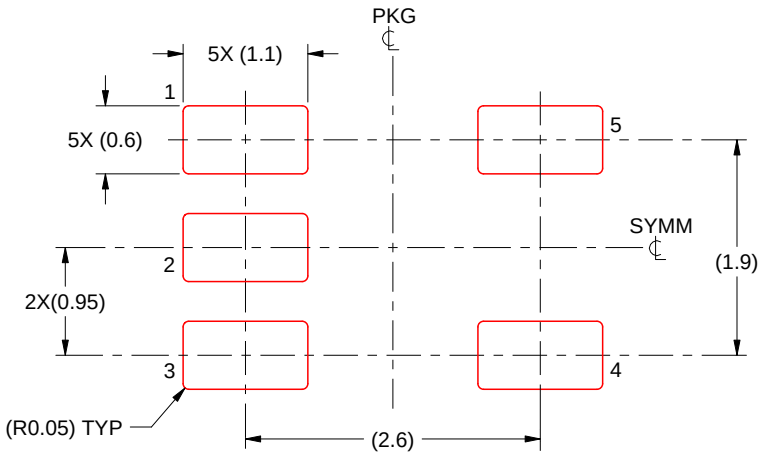


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

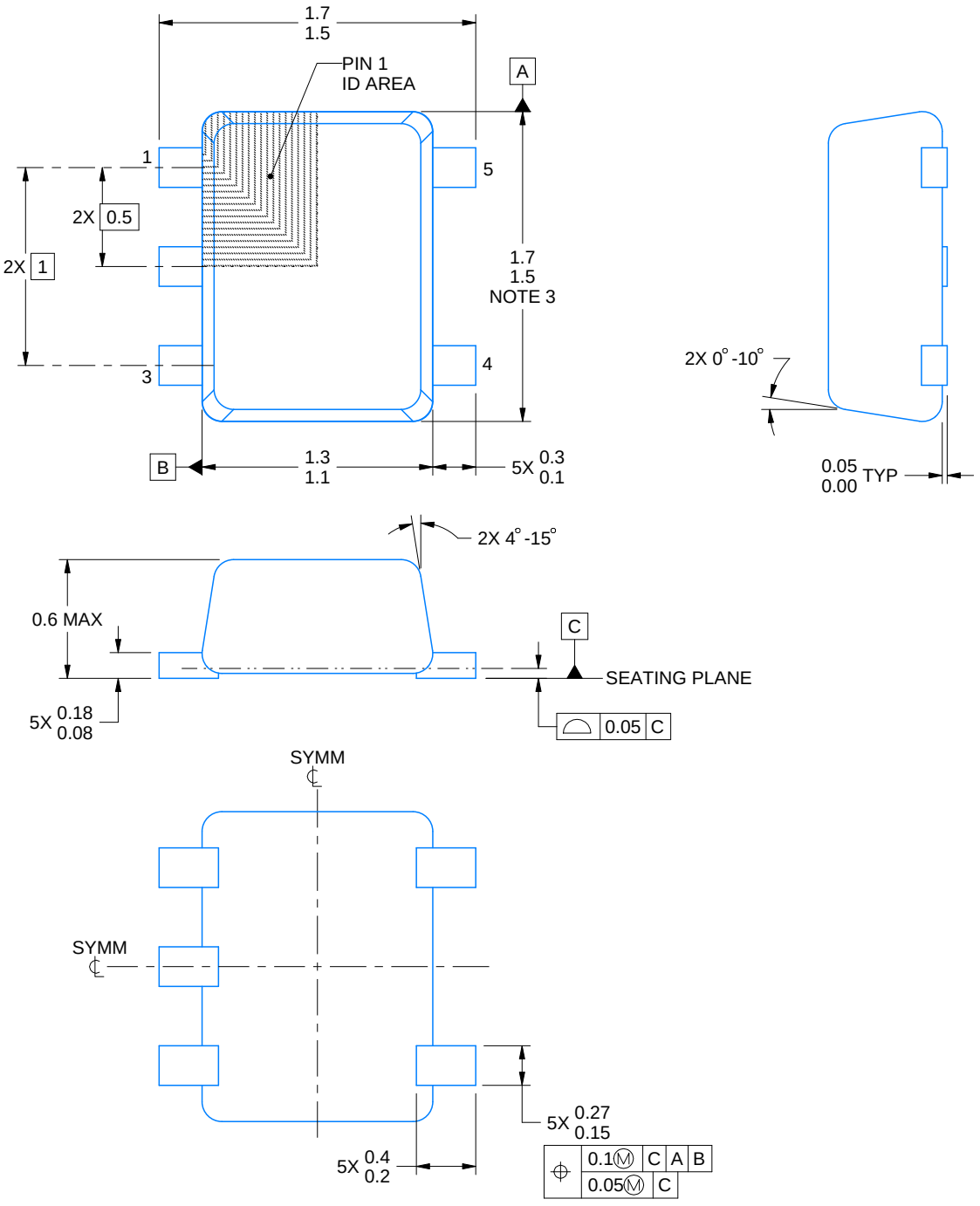
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DRL0005A

SOT - 0.6 mm max height

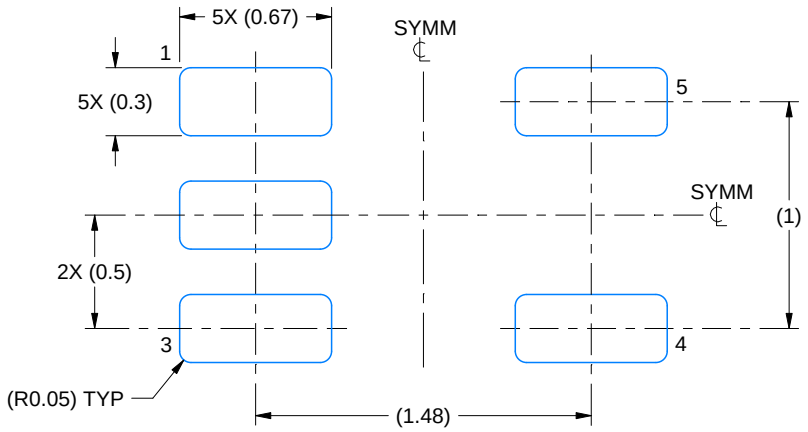
PLASTIC SMALL OUTLINE



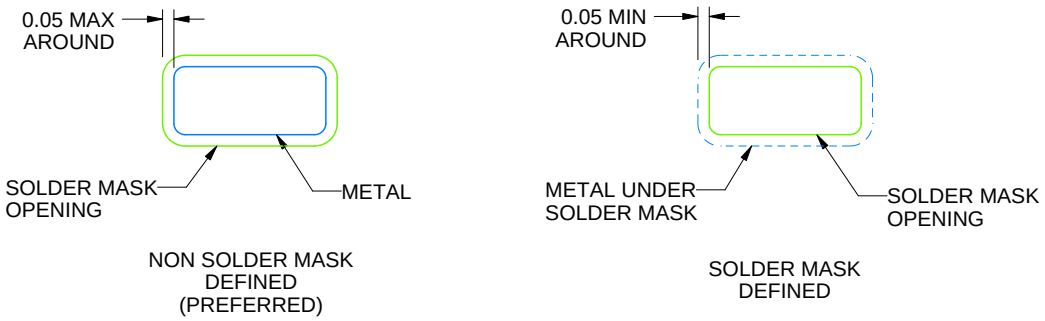
4220753/E 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1



LAND PATTERN EXAMPLE
SCALE:30X

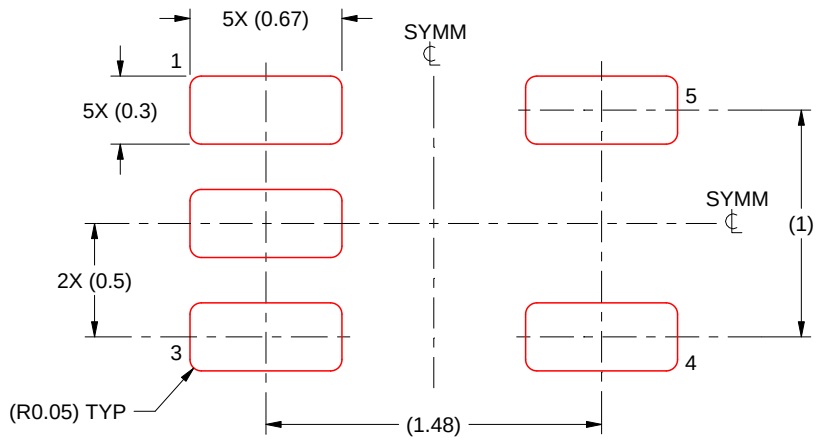


SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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