

SNx4AHCT86 クワッド、2 入力排他 OR (EXOR) ゲート

1 特長

- 入力は TTL 電圧互換
- JESD 17 準拠で 250mA 超のラッチアップ性能
- MIL-PRF-38535 準拠の製品については、特に記述のない限り、すべてのパラメータはテスト済みです。
その他のすべての製品については、量産プロセスにすべてのパラメータのテストが含まれているとは限りません。
- JESD 22 を超える ESD 保護
 - 2000V、人体モデル (A114-A)
 - 200V、マシン・モデル (A115-A)

2 アプリケーション

- サーバー
- PC およびノートパソコン
- ネットワーク・スイッチ
- ウェアラブルなヘルスケア / フィットネス機器
- テレコム・インフラストラクチャ
- レジ用電子機器

3 概要

SNx4AHCT86 デバイスは、クワッド 2 入力排他 OR ゲートです。これらのデバイスは、ブール関数 $Y = A \times B$ または $Y = \overline{A}B + A\overline{B}$ を正論理で実行します。

パッケージ情報 (1)

部品番号	パッケージ	本体サイズ (公称)
SN54AHCT86	J (CDIP, 14)	19.56mm × 6.67mm
	W (CFP, 14)	13.09mm × 6.92mm
	FK (LCCC, 20)	8.89mm × 8.89mm
SN74AHCT86	N (PDIP, 14)	19.3mm × 6.35mm
	D (SOIC, 14)	8.65mm × 3.91mm
	NS (SOP, 14)	10.30mm × 5.30mm
	DB (SSOP, 14)	6.20mm × 5.30mm
	PW (TSSOP, 14)	5.00mm × 4.40mm
	DGV (TVSOP, 14)	3.60mm × 4.40mm
	RGY (VQFN, 14)	3.50mm × 3.50mm
	BQA (WQFN, 14)	3.00mm × 2.50mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



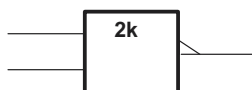
These are five equivalent exclusive-OR symbols valid for an SN74AHCT86 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



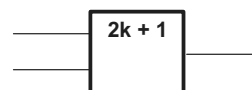
The output is active (low) if all inputs stand at the same logic level (that is, $A = B$).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (that is, 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (that is, only 1 of the 2) are active.

概略回路図



Table of Contents

1 特長	1	8.1 Overview.....	9
2 アプリケーション	1	8.2 Functional Block Diagram.....	9
3 概要	1	8.3 Feature Description.....	9
4 Revision History	2	8.4 Device Functional Modes.....	9
5 Pin Configuration and Functions	3	9 Application and Implementation	10
6 Specifications	5	9.1 Application Information.....	10
6.1 Absolute Maximum Ratings.....	5	9.2 Typical Application.....	10
6.2 ESD Ratings.....	5	9.3 Power Supply Recommendations.....	11
6.3 Recommended Operating Conditions.....	5	9.4 Layout.....	11
6.4 Thermal Information.....	6	10 Device and Documentation Support	12
6.5 Electrical Characteristics.....	6	10.1 ドキュメントの更新通知を受け取る方法.....	12
6.6 Switching Characteristics.....	6	10.2 サポート・リソース.....	12
6.7 Noise Characteristics.....	7	10.3 Trademarks.....	12
6.8 Operating Characteristics.....	7	10.4 静電気放電に関する注意事項.....	12
6.9 Typical Characteristics.....	7	10.5 用語集.....	12
7 Parameter Measurement Information	8	11 Mechanical, Packaging, and Orderable Information	12
8 Detailed Description	9		

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision O (May 2023) to Revision P (October 2023)	Page
Updated RθJA values: D = 97.5 to 124.5, PW = 125.1 to 147.7; Updated D and PW packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W	6
Changes from Revision N (August 2014) to Revision O (May 2023)	Page
- ドキュメント全体にわたって表、図、相互参照の採番方法を更新..... 「パッケージ情報」表を更新 - データシートに BQA パッケージを追加	1 1 1

5 Pin Configuration and Functions

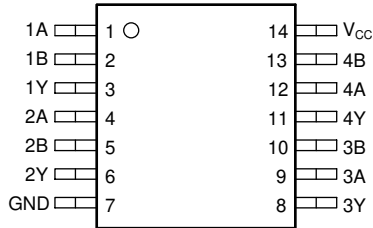


図 5-1. SN54AHCT86 J or W Package, 14-Pin (Top View)
SN74AHCT86 D, DB, DGV, N, NS, or PW Package, 14-Pin (Top View)

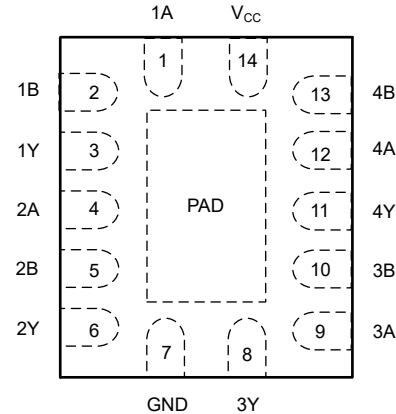


図 5-2. SN74AHCT86 RGY or BQA Package, 14-Pin (Top View)

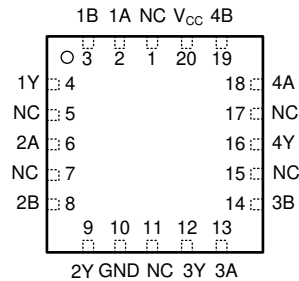


図 5-3. SN54AHCT86 FK Package, 20-Pin (Top View)

表 5-1. Pin Functions

PIN					TYPE ⁽¹⁾	DESCRIPTION
NAME	SN74AHCT86		SN54AHCT86			
	D, DB, DGV, N, NS, PW	RGY, BQA	J, W	FK		
1A	1	1	1	2	I	1A Input
1B	2	2	2	3	I	1B Input
1Y	3	3	3	4	O	1Y Output
2A	4	4	4	6	I	2A Input
2B	5	5	5	8	I	2B Input
2Y	6	6	6	9	O	2Y Output
3Y	8	8	8	12	O	3Y Output
3A	9	9	9	13	I	3A Input
3B	10	10	10	14	I	3B Input
4Y	11	11	11	16	O	4Y Output
4A	12	12	12	18	I	4A Input
4B	13	13	13	19	I	4B Input
GND	7	7	7	10	—	Ground Pin
NC	—	—	—	1, 5, 7, 11, 15, 17	—	No Connection
V _{CC}	14	14	14	20	—	Power Pin

表 5-1. Pin Functions (続き)

PIN					TYPE ⁽¹⁾	DESCRIPTION
NAME	SN74AHCT86		SN54AHCT86			
	D, DB, DGV, N, NS, PW	RGY, BQA	J, W	FK		
Thermal Pad	—	PAD	—	—	—	Thermal Pad

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	−0.5	7	V
V _I	Input voltage range ⁽²⁾	−0.5	7	V
V _O	Output voltage range ⁽²⁾	−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		−20 mA
I _{OK}	Output clamp current	V _O < 0 or V _O > V _{CC}		±20 mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±25 mA
	Continuous current through V _{CC} or GND			±50 mA

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			MIN	MAX	UNIT
T _{stg}	Storage temperature range		−65	150	°C
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins ⁽²⁾	0	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN54AHCT86		SN74AHCT86		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		−8		−8	mA
I _{OL}	Low-level output current		8		8	mA
Δt/Δv	Input transition rise or fall rate		20		20	ns/V
T _A	Operating free-air temperature	−55	125	−40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SNx4AHCT86								UNIT
		D	DB	DGV	N	NS	PW	RGY	BQA	
		14 PINS								
R _{θJA}	Junction-to-ambient thermal resistance	124.5	109.5	133.3	59.7	92.2	147.7	59.0	88.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	78.8	62.1	55.6	47.3	49.8	77.4	72.5	90.9	
R _{θJB}	Junction-to-board thermal resistance	81	56.9	66.3	39.5	51.0	90.9	35.0	56.8	
Ψ _{JT}	Junction-to-top characterization parameter	37	22.6	7.8	32.4	15.7	27.2	3.9	9.9	
Ψ _{JB}	Junction-to-board characterization parameter	80.6	56.3	56.6	39.4	50.6	90.2	35.1	56.7	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	15.4	33.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHCT86		–40°C to 85°C SN74AHCT86		–40°C to 125°C SN74AHCT86		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –50 μA	4.5 V	4.4	4.5		4.4		4.4		4.4		V
	I _{OH} = –8 mA		3.94			3.8		3.8		3.8		
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1	0.1		0.1		0.1		V
	I _{OL} = 8 mA				0.36	0.44		0.44		0.44		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1	±1 ⁽¹⁾		±1		±1		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			2	20		20		20		μA
ΔI _{CC} ⁽²⁾	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35	1.5		1.5		1.5		mA
C _I	V _I = V _{CC} or GND	5 V			4	10		10				pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

6.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			–55°C to 125°C SN54AHCT86		–40°C to 85°C SN74AHCT86		–40°C to 125°C SN74AHCT86		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	C _L = 15 pF		5 ⁽¹⁾	6.9 ⁽¹⁾	1 ⁽¹⁾	8 ⁽¹⁾	1	8	1	9	ns
t _{PHL}					5 ⁽¹⁾	6.9 ⁽¹⁾	1 ⁽¹⁾	8 ⁽¹⁾	1	8	1	9	
t _{PLH}	A or B	Y	C _L = 50 pF		5.5	8.8	1	10	1	9	1	11	ns
t _{PHL}					5.5	8.8	1	10	1	9	1	11	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.7 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER		SN74AHCT86			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.4	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4			V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

(1) Characteristics are for surface-mount packages only.

6.8 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance No load, $f = 1\text{ MHz}$	18	pF

6.9 Typical Characteristics

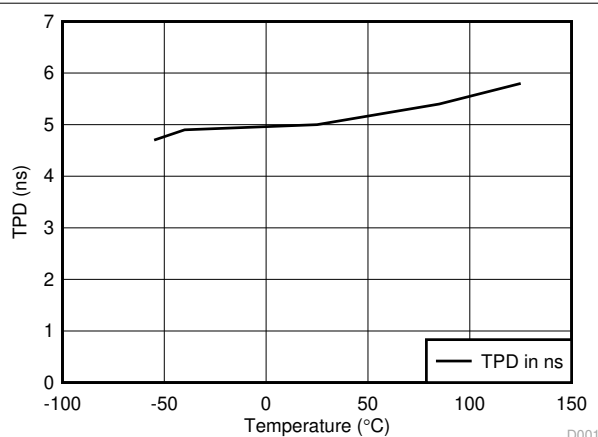
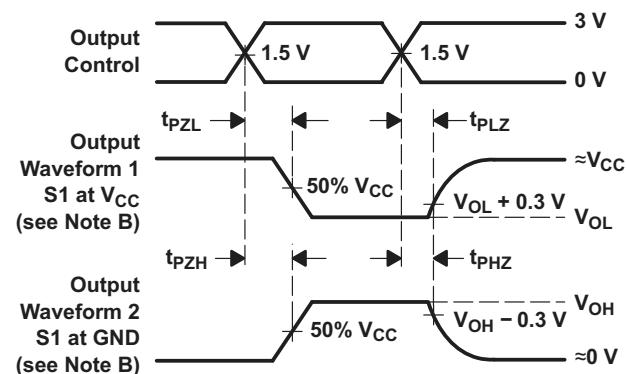
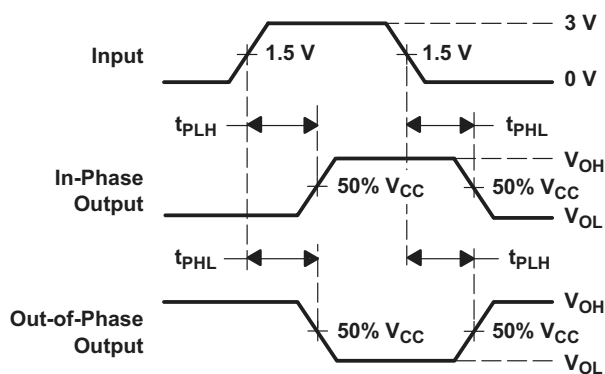
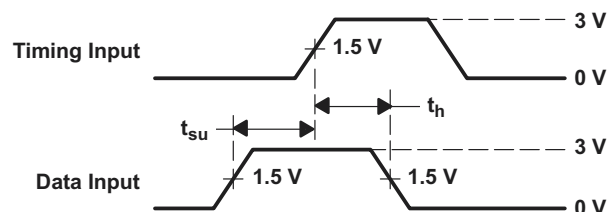
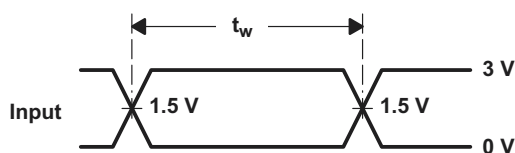
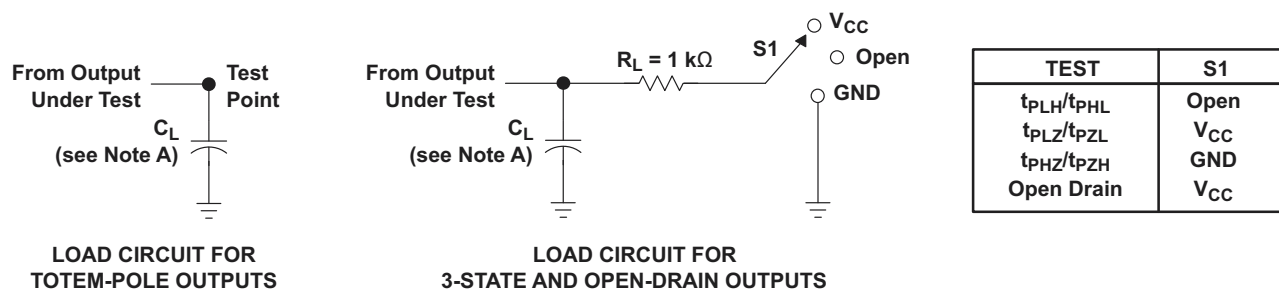


图 6-1. TPD vs Temperature

7 Parameter Measurement Information



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

图 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SNx4AHCT86 devices are quadruple 2-input exclusive-OR gates. These devices perform the Boolean function $Y = A \times B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

The inputs are TTL compatible allowing 3.3 V to 5 V translation.

8.2 Functional Block Diagram

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



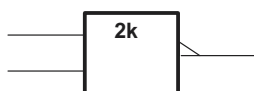
These are five equivalent exclusive-OR symbols valid for an SN74AHCT86 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



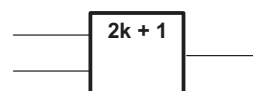
The output is active (low) if all inputs stand at the same logic level (that is, $A = B$).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (that is, 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (that is, only 1 of the 2) are active.

图 8-1. Exclusive-OR Logic

8.3 Feature Description

- TTL inputs
 - Lowered switching threshold allows up translation 3.3 V to 5 V
- Slow edges reduce output ringing

8.4 Device Functional Modes

**表 8-1. Function Table
(Each Gate)**

INPUTS		OUTPUT Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The SNx4AHCT86 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8-V V_{IL} and 2-V V_{IH} . This feature makes the device ideal for translating up from 3.3 V to 5 V. [図 9-2](#) shows this type of translation.

9.2 Typical Application

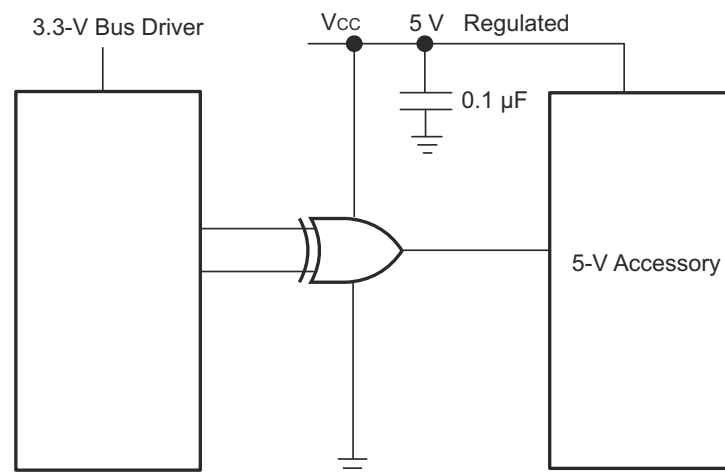


図 9-1. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

- Recommended input conditions:
 - Rise time and fall time specs: see $(\Delta t/\Delta V)$ in the [Recommended Operating Conditions](#) table.
 - Specified High and low levels: see $(V_{IH}$ and $V_{IL})$ in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
- Recommend output conditions:
 - Load currents should not exceed 25 mA per output and 75 mA total for the part
 - Outputs should not be pulled above V_{CC}

9.2.3 Application Curves

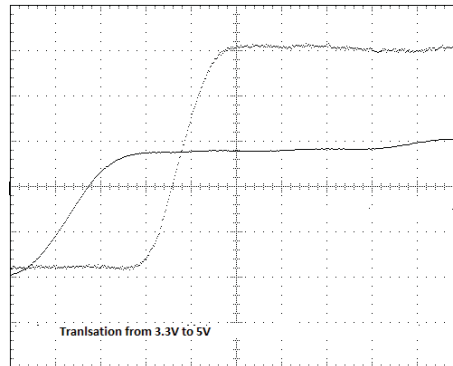


図 9-2. Up Translation

9.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in 図 9-3 are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} ; whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs so they cannot float when disabled.

9.4.2 Layout Example

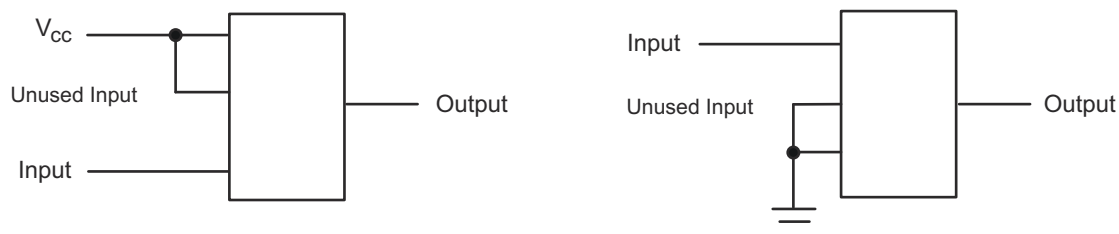


図 9-3. Layout Diagram

10 Device and Documentation Support

10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9681701Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9681701Q2A SNJ54AHCT 86FK
5962-9681701QCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681701QC A SNJ54AHCT86J
SN74AHCT86BQAR	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AHCT86
SN74AHCT86BQAR.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AHCT86
SN74AHCT86D	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 85	AHCT86
SN74AHCT86DBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB86
SN74AHCT86DBR.A	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB86
SN74AHCT86DGVR	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB86
SN74AHCT86DGVR.A	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB86
SN74AHCT86DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT86
SN74AHCT86DR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT86
SN74AHCT86N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHCT86N
SN74AHCT86N.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHCT86N
SN74AHCT86NSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT86
SN74AHCT86NSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT86
SN74AHCT86PW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 125	HB86
SN74AHCT86PWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	HB86
SN74AHCT86PWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB86
SN74AHCT86RGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HB86
SN74AHCT86RGYR.A	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HB86
SN74AHCT86RGYRG4	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HB86
SNJ54AHCT86FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9681701Q2A SNJ54AHCT 86FK

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54AHCT86FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9681701Q2A SNJ54AHCT 86FK
SNJ54AHCT86J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681701QC A SNJ54AHCT86J
SNJ54AHCT86J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681701QC A SNJ54AHCT86J

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHCT86, SN74AHCT86 :

- Catalog : [SN74AHCT86](#)
- Military : [SN54AHCT86](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT86BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHCT86DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHCT86DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHCT86DR	SOIC	D	14	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AHCT86NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74AHCT86PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT86RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



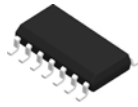
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT86BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHCT86DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74AHCT86DGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74AHCT86DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AHCT86NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74AHCT86PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHCT86RGYR	VQFN	RGY	14	3000	353.0	353.0	32.0

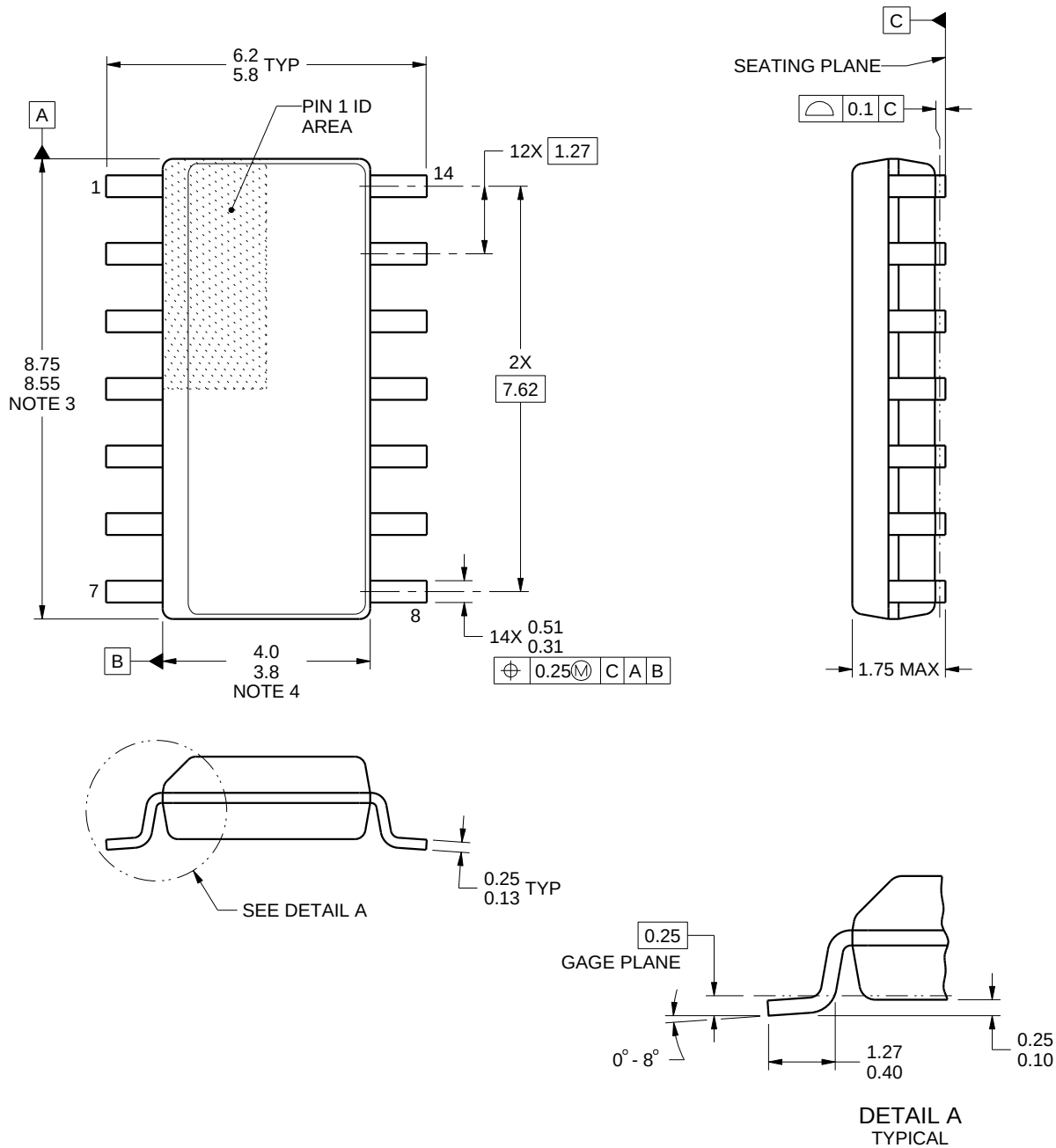
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9681701Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74AHCT86N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHCT86N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHCT86N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHCT86N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHCT86FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHCT86FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

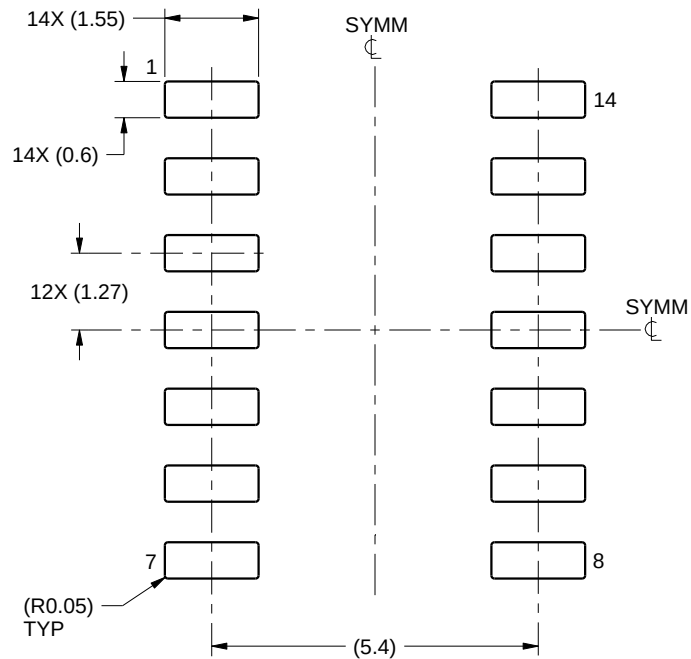
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

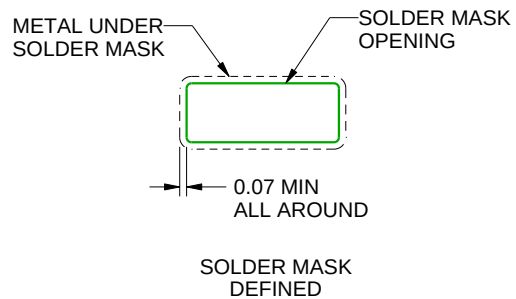
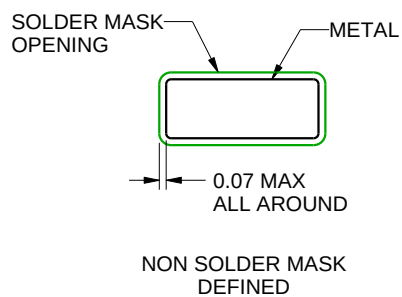
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

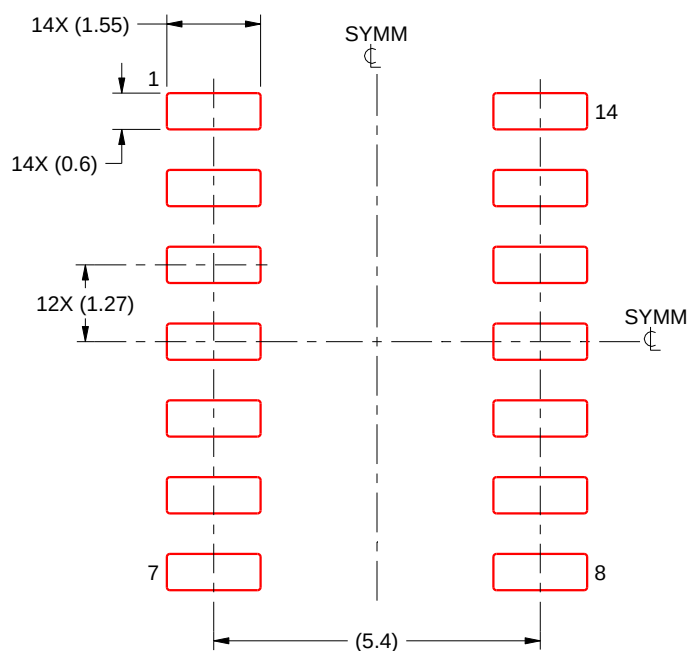
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

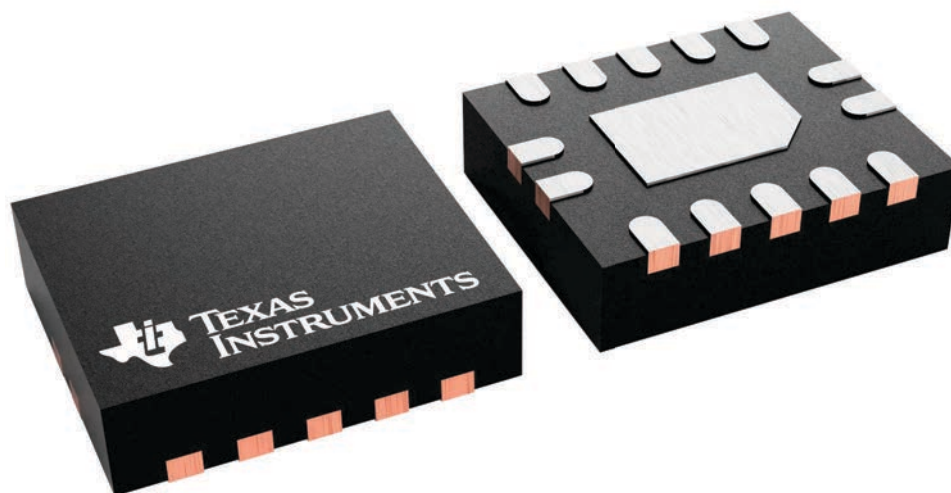
BQA 14

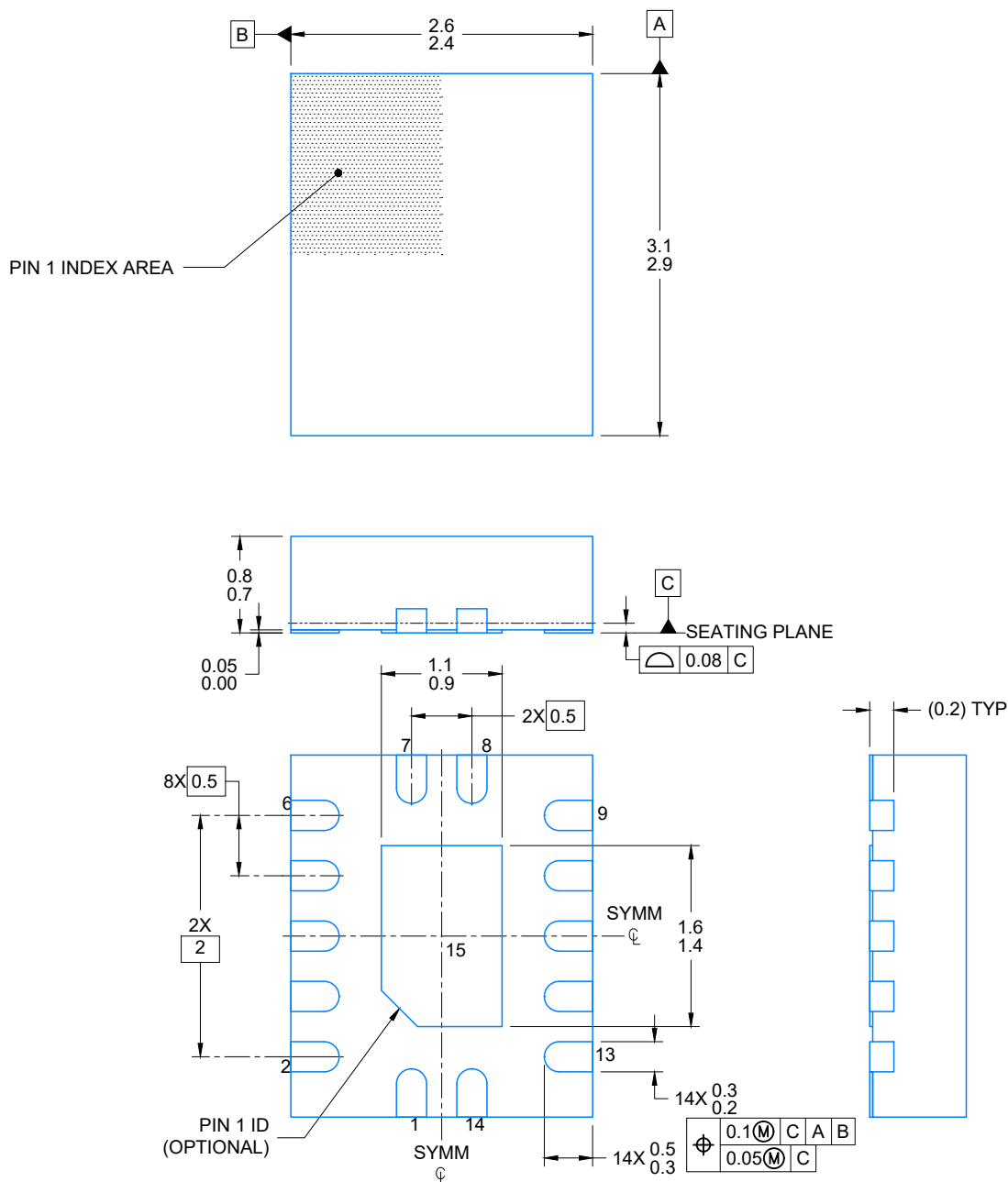
WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

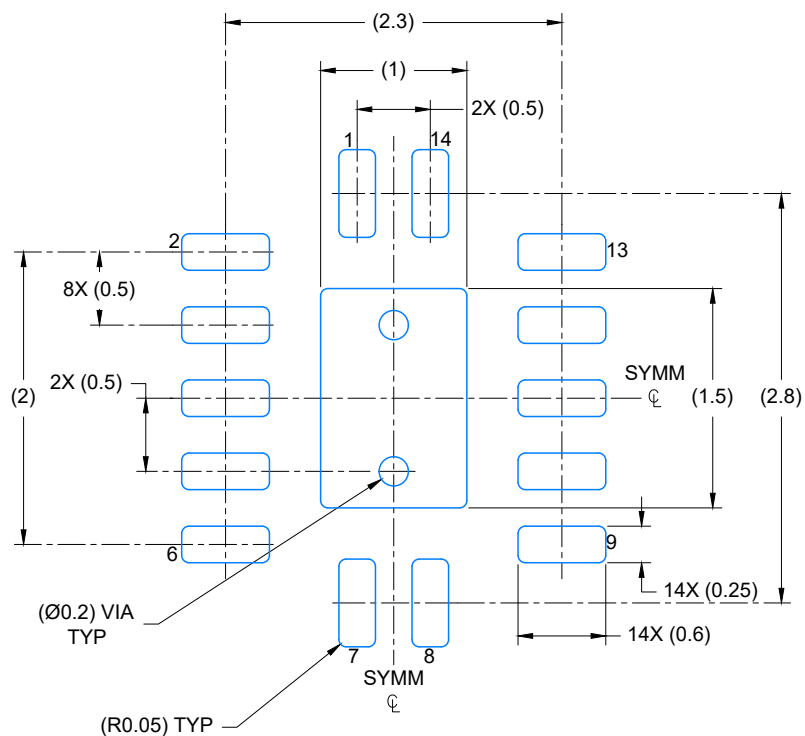




4224636/A 11/2018

NOTES:

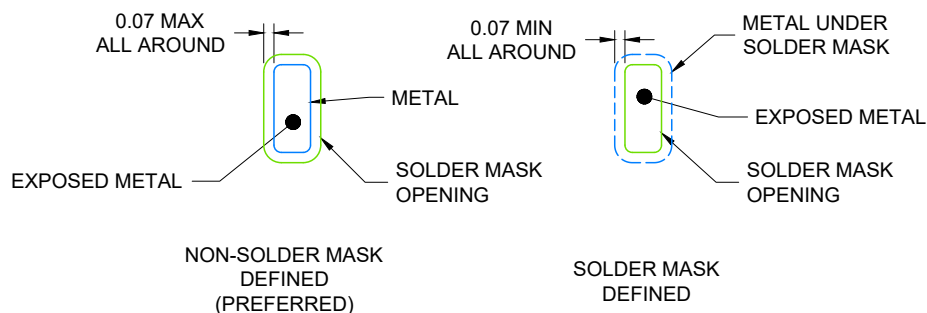
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

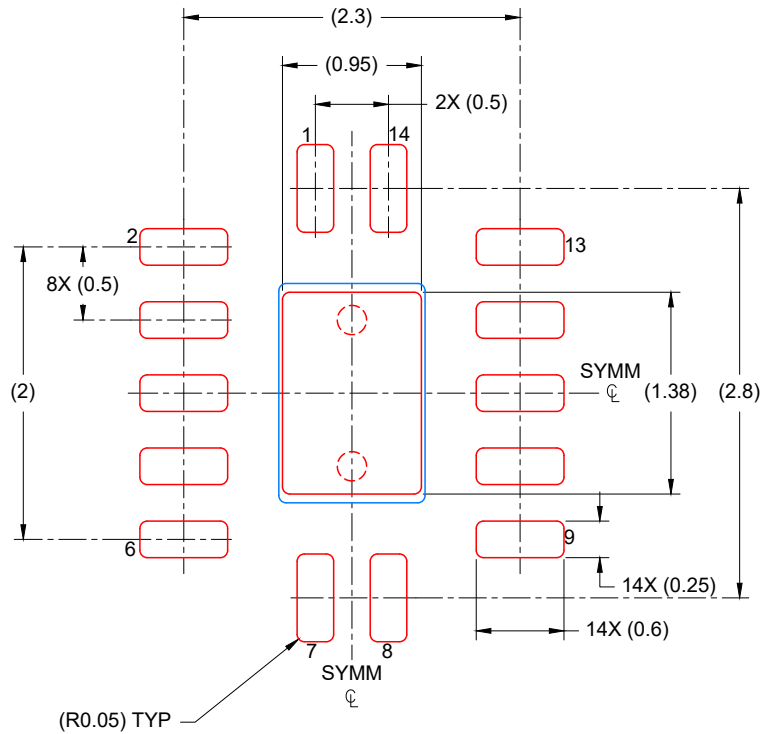
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 88% PRINTED COVERAGE BY AREA
 SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

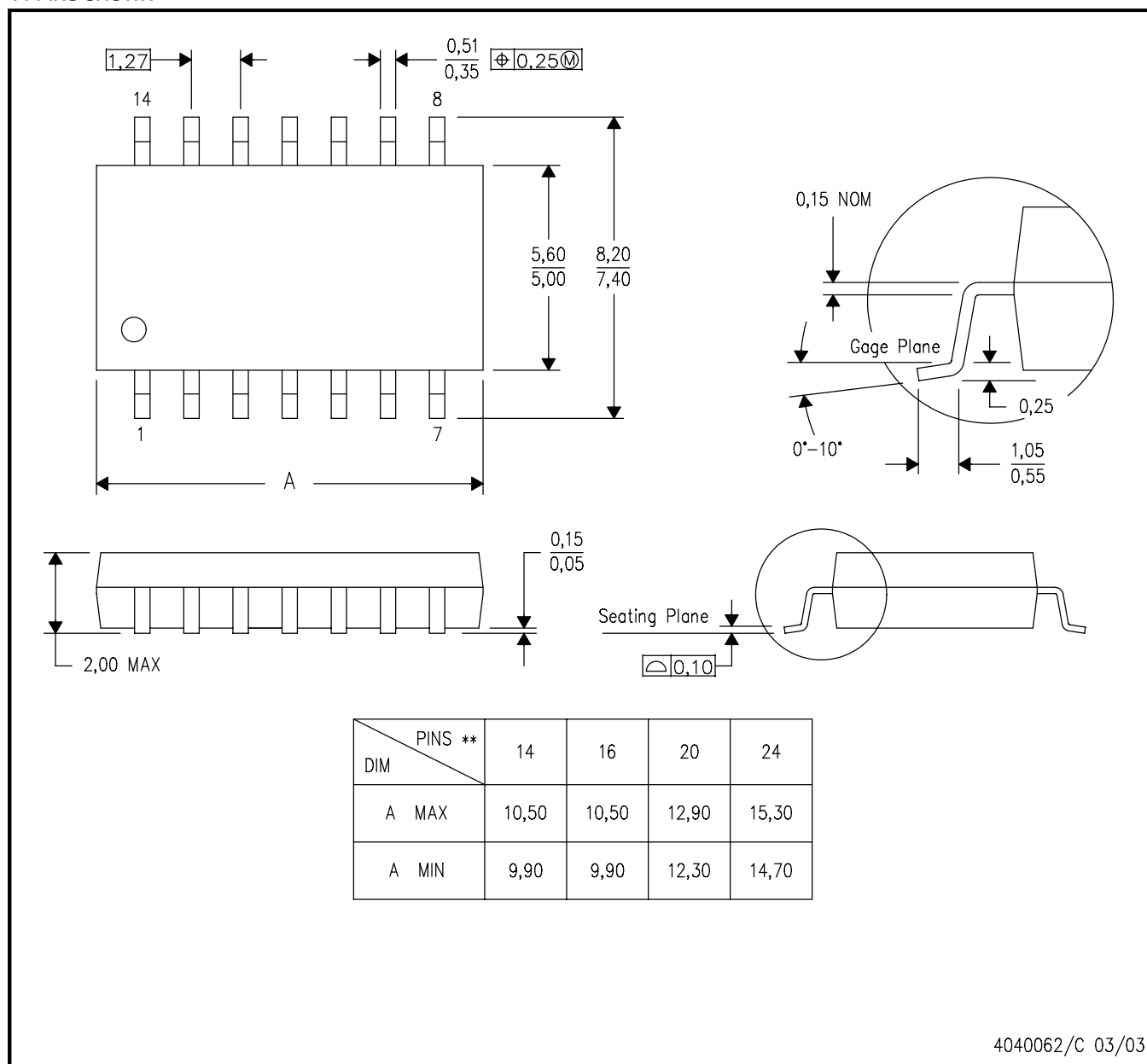
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

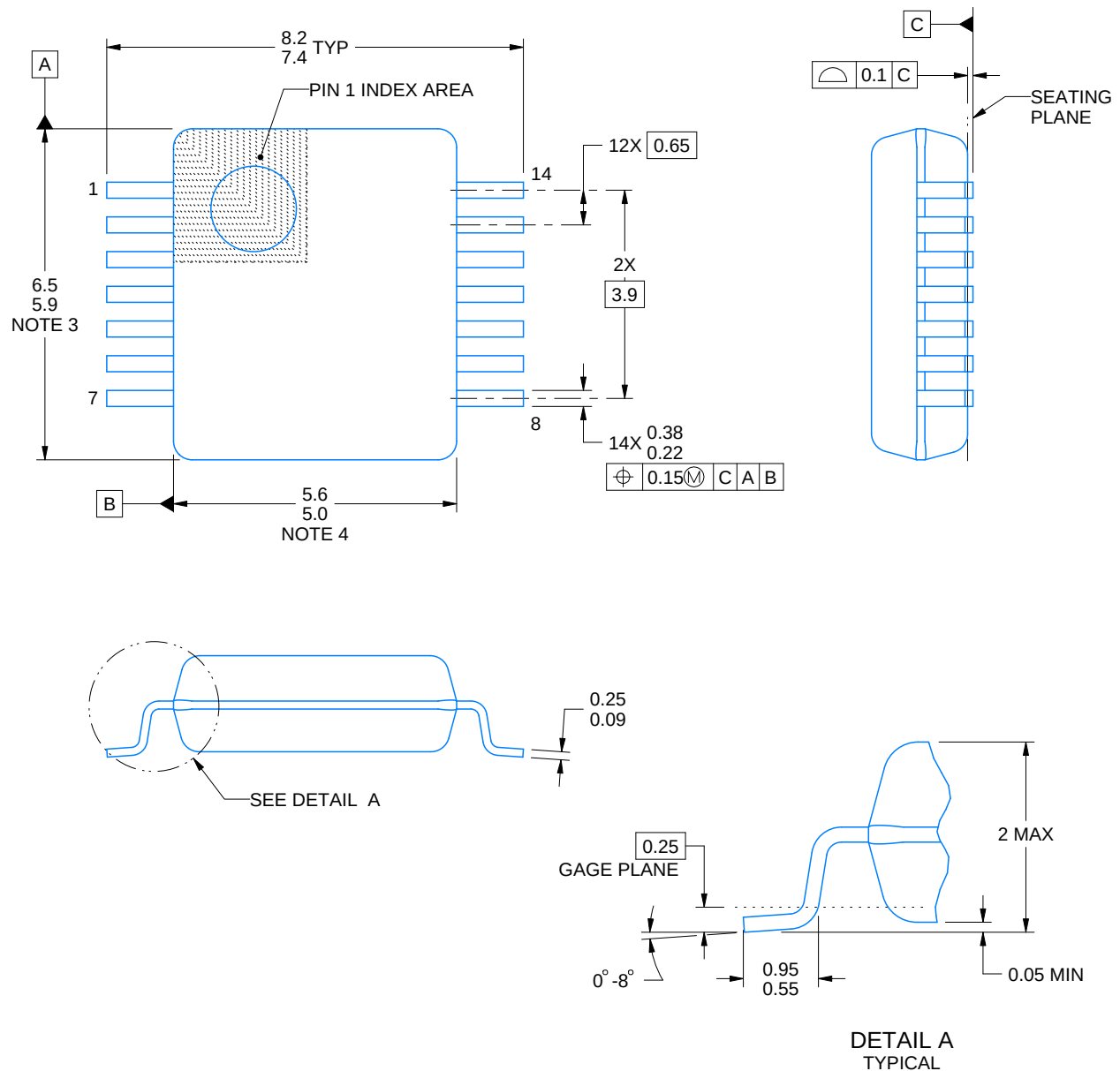
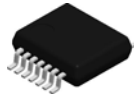
NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



4220762/A 05/2024

NOTES:

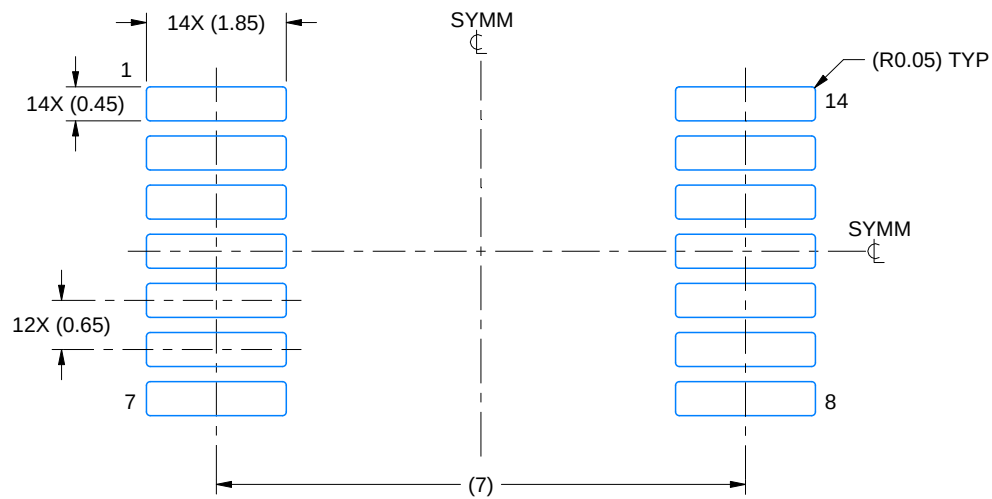
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

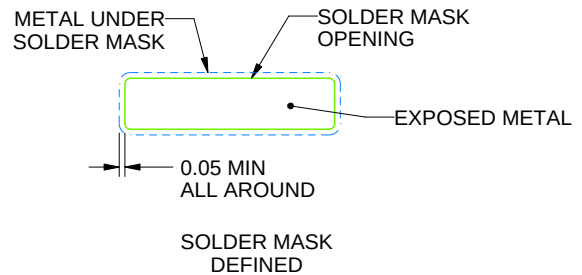
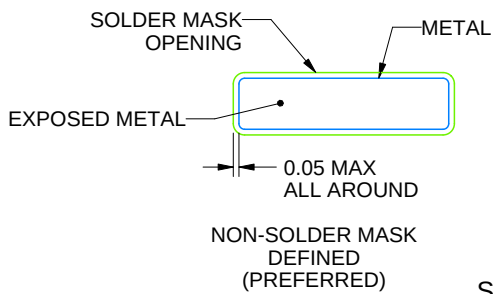
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

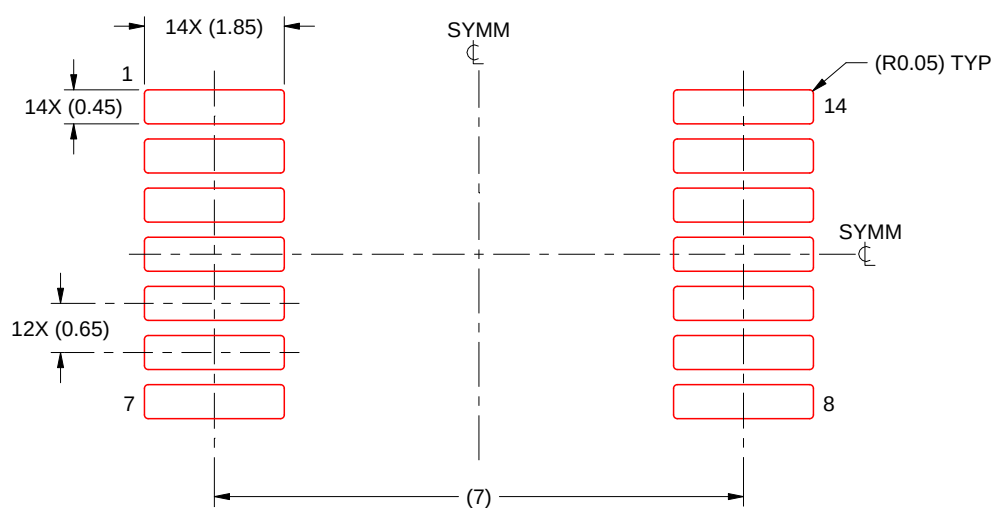
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

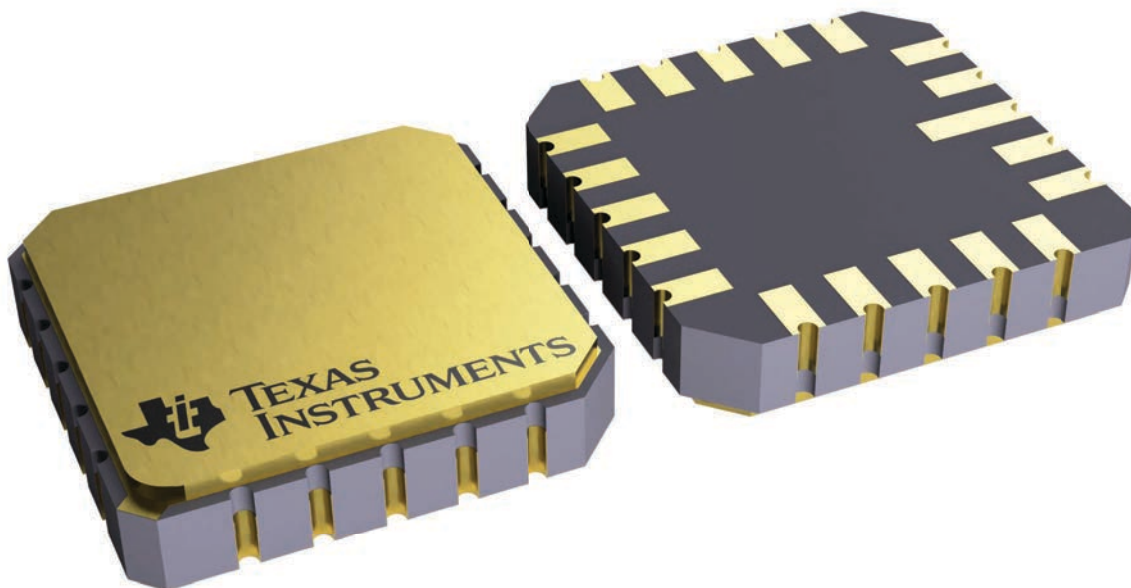
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



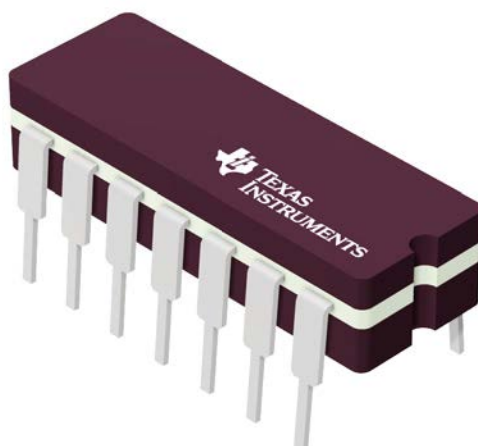
4229370VA\

J 14

GENERIC PACKAGE VIEW

CDIP - 5.08 mm max height

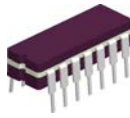
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

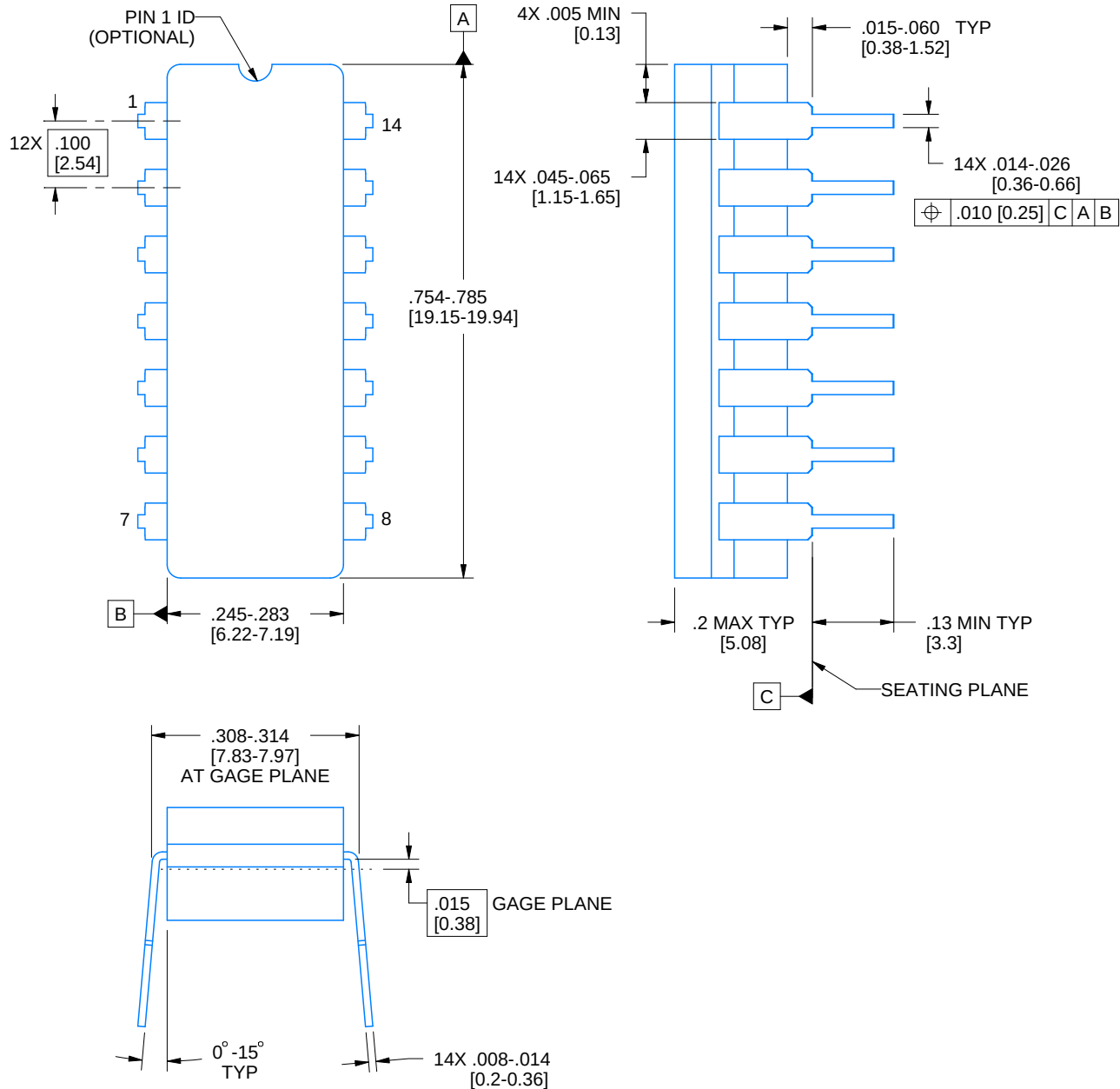
J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

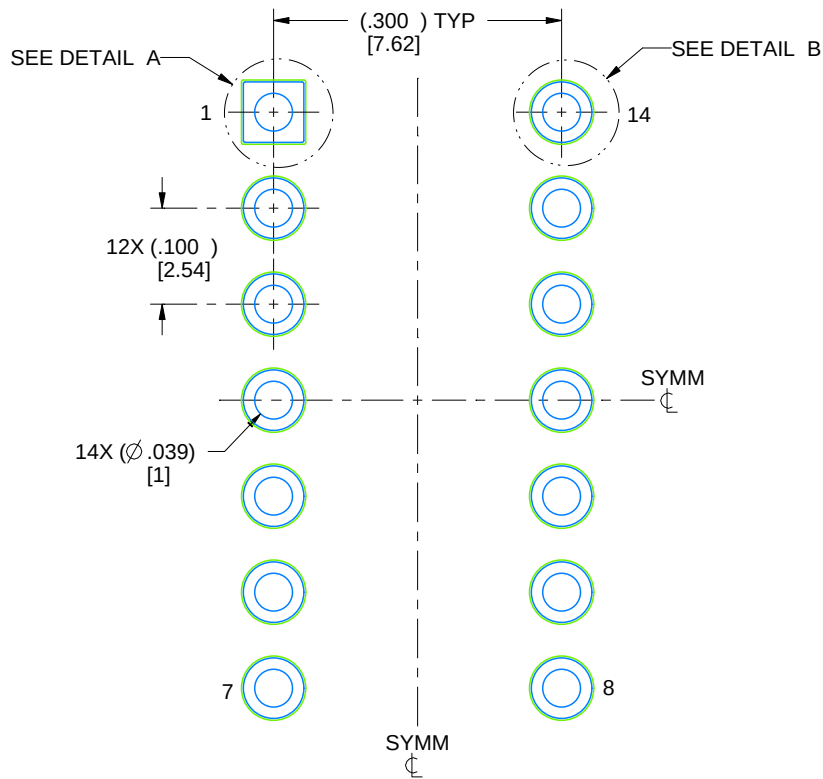
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

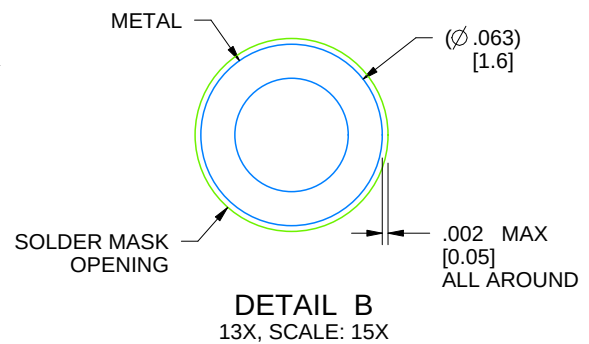
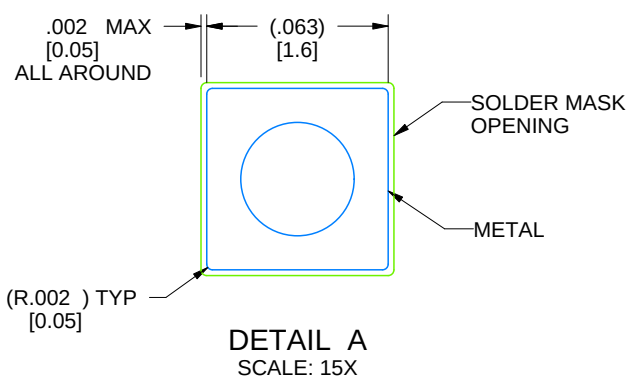
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

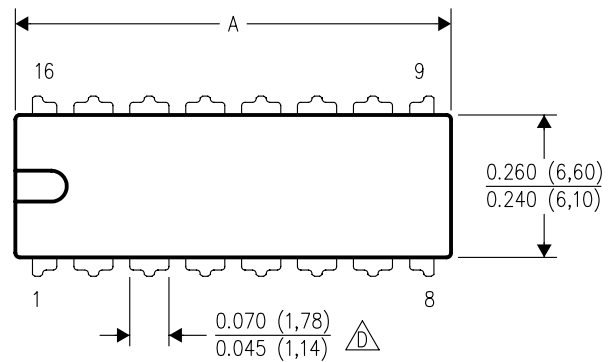


4214771/A 05/2017

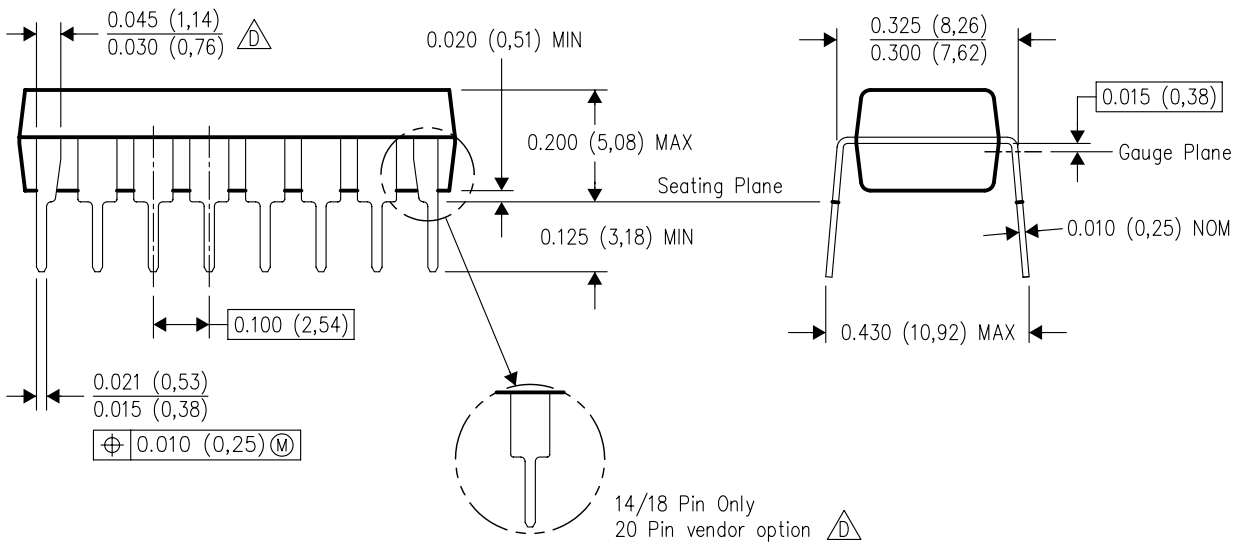
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

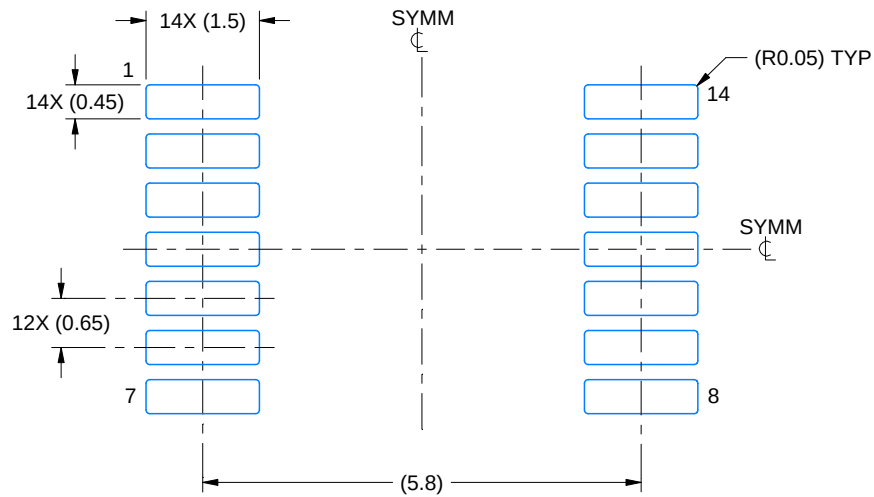
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

EXAMPLE BOARD LAYOUT

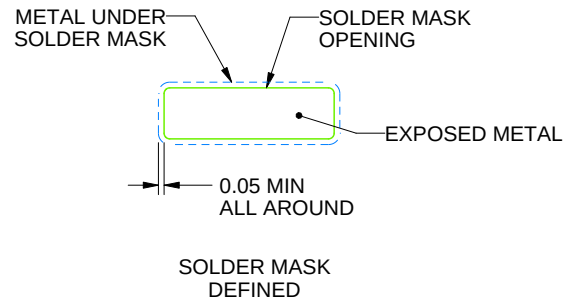
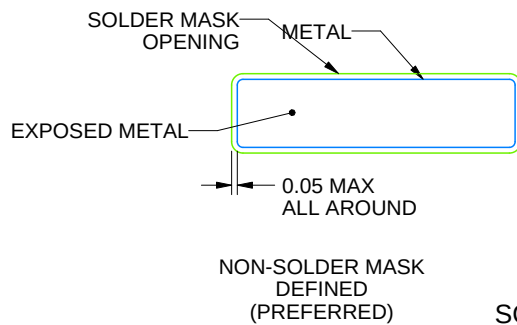
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

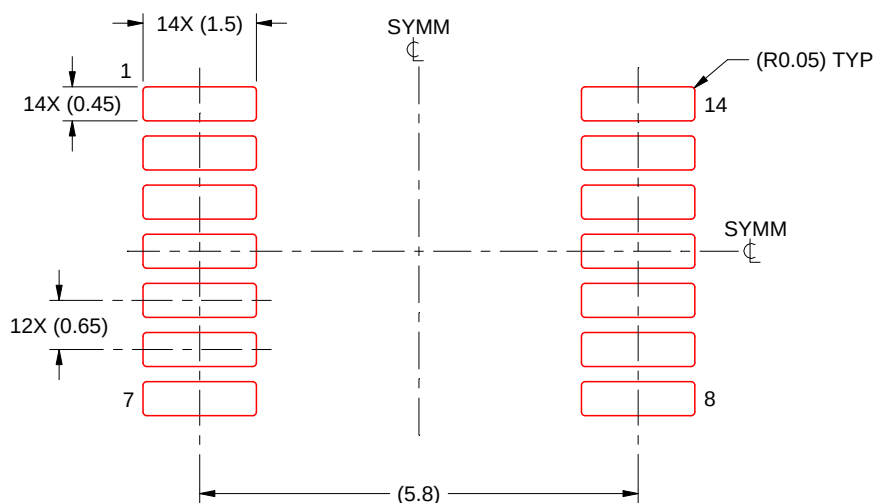
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

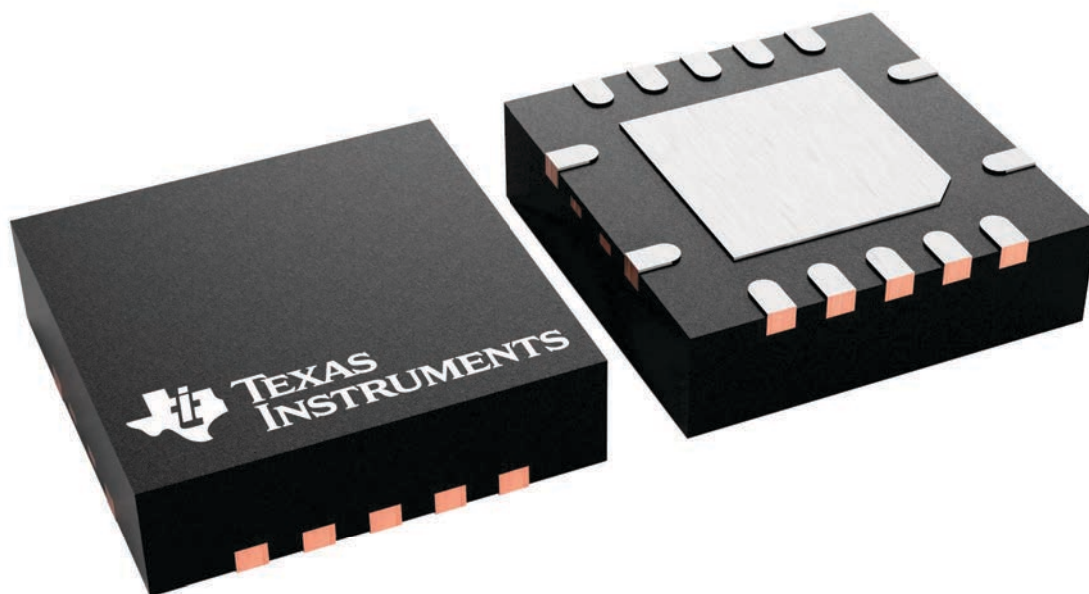
RGY 14

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231541/A

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含みいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](https://www.ti.com) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月