SN74AUP2G07 低消費電力、デュアル・バッファ / ドライバ、オープンドレイン出力

1 特長

- 低い静的消費電力 (I_{CC} = 0.9μA、最大値)
- 低い動的消費電力 (3.3V で C_{pd} = 1pF、標準値)
- 低い入力容量 (C_i = 1.5pF、標準値)
- 低いノイズ - オーバーシュートおよびアンダーシュートは V_{CC} の 10% 未満
- I_{off} により活線挿抜、部分的パワーダウン・モード、バック・ドライブ保護をサポート
- 入力ヒステリシスにより低速の入力遷移が可能で、入力におけるスイッチング・ノイズ耐性が向上 (3.3V で V_{hys} = 250mV、標準値)
- 広い動作 V_{CC} 範囲:0.8V～3.6V
- 3.3 V 動作に最適化
- 3.6V I/O 許容で混在モードの信号動作に対応
- 3.3V で t_{pd} = 3.3ns (最大値)
- ポイント・ツー・ポイントのアプリケーションに好適
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 準拠で ESD 性能を試験済み
  - 人体モデルで 4500V
  - 荷電デバイス・モデルで 1500V

2 アプリケーション

- アクティブ・ノイズ・キャンセレーション (ANC)
- バーコード・スキャナ
- 血圧計
- CPAP 機器
- ケーブル・ソリューション
- DLP 3D マシン・ビジョン、ハイパースペクトル画像処理、光ネットワーク、分光法
- eBook (電子書籍) およびスマートフォン
- 組み込み用 PC
- フィールド・トランスミッタ:温度または圧力センサ
- 指紋認証
- HVAC:暖房、換気、空調
- ネットワーク接続ストレージ (NAS)
- サーバーのマザーボードと PSU
- ソフトウェア無線 (SDR)
- テレビ:高解像度 (HDTV)、LCD、デジタル
- ビデオ通信システム
- ワイヤレス・データ・アクセス・カード、ヘッドセット、キーボード、マウス、LAN カード
- X 線:手荷物スキャナ、医療用、歯科用

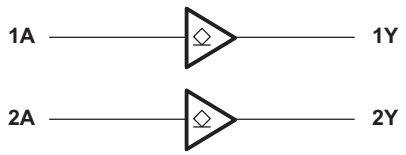
3 概要

SN74AUP2G07 デバイスは、0.8V～3.6V で動作するオープン・ドレイン出力のデュアル・バッファ・ゲートです。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
SN74AUP2G07	SC70 (6)	3.00mm × 1.25mm
	SON (6)	1.45mm × 1.00mm
	SON (6)	1.00mm × 1.00mm
	DSBGA (6)	1.16mm × 0.76mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



ブロック概略図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (February 2016) to Revision E (October 2021) — **Page**

- Changed pinout images style and formatting, removed overlapping letters in YZP package drawing, corrected BGA pin numbers in the *Pin Functions* table, changed V_{CC} and GND pin TYPE From: "—" To: "P" in the *Pin Functions* table and added footnote to the *Pin Functions* table to define pin types ... 3
- Changed maximum output voltage in the low state in the *セクション 6.1* table to 4.6 V ... 4
- Changed the V_O Output voltage in the *セクション 6.3* table from 'V_{CC}' to '3.6' ... 5
- Updated $R_{\theta JA}$ values to more accurately reflect device characteristics: YFP 132 to 125.4, DCK 252 to 302.4, DRY 234 to 338, DSF 300 to 372.5, added standard thermal characteristics for all packages ($R_{\theta JC(top)}$, $R_{\theta JB}$, Ψ_{JT}, Ψ_{JB}, $R_{\theta JC(bot)}$) ... 5

Changes from Revision C (November 2014) to Revision D (February 2016) — **Page**

- Changed the V_{CC} pin TYPE From: "I" To: "—" in the *Pin Functions* table ... 3
- Added "Junction temperature" to the *セクション 6.1* table ... 4
- Deleted the I_{OH} High-level output current from the *セクション 6.3* table ... 5
- Deleted V_{OH} PARAMETER from the *セクション 6.5* table, these specifications do not pertain to open drain devices ... 6

Changes from Revision B (September 2009) to Revision C (November 2014) — **Page**

- 「*注文情報*」表を削除 ... 1
- 「*アプリケーション*」セクション、「*製品情報*」表、「*ピン機能*」表、「*取り扱いに関する定格*」表、「*熱に関する情報*」表、「*代表的特性*」セクション、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1
- 「*特長*」の I_{off} を更新 ... 1

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5 Pin Configuration and Functions

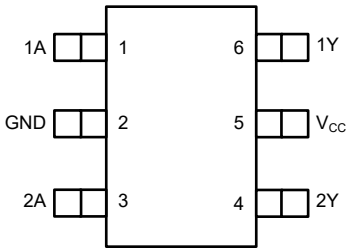


図 5-1. DCK Package 6-Pin SC70 Top View

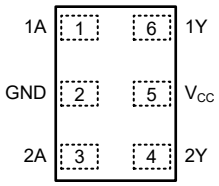


図 5-2. DRY Package 6-Pin SON Transparent Top View

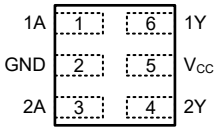


図 5-3. DSF Package 6-Pin SON Transparent Top View

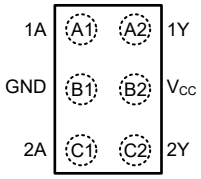


図 5-4. YFP Package 6-Pin DSBGA Transparent Top View

See the mechanical drawings for dimensions.

表 5-1. Pin Functions

PIN			TYPE (1)	DESCRIPTION
NAME	DCK, DSF, DRY, YFP	(BGA) YFP		
1A	1	A1	I	Input 1
1Y	6	A2	O	Output 1
2A	3	C1	I	Input 2
2Y	4	C2	O	Output 2
GND	2	B1	P	Ground
V_{CC}	5	B2	P	Power Pin

(1) I = Input, O = Output, P = Power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range(1)		–0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(1)		–0.5	4.6	V
V_O	Output voltage range in the low state(1)		–0.5	4.6	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	0.65 × V_{CC}		
		V_{CC} = 2.3 V to 2.7 V	1.6		
		V_{CC} = 3 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		0.35 × V_{CC}	
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.9	
V_I	Input voltage		0	3.6	V
V_O	Output voltage		0	3.6	V
I_{OL}	Low-level output current	V_{CC} = 0.8 V		20	μA
		V_{CC} = 1.1 V		1.1	mA
		V_{CC} = 1.4 V		1.7	
		V_{CC} = 1.65 V		1.9	
		V_{CC} = 2.3 V		3.1	
		V_{CC} = 3 V		4	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 0.8 V to 3.6 V		200	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs,* literature number SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		YFP	DCK	DRY	DSF	UNIT
		6 PINS	6 PINS	6 PINS	6 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	125.4	302.4	338.0	372.5	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	1.9	219.5	228.9	179.9	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	37.2	106.7	203.5	231.2	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	0.5	84.2	62.4	28.6	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	37.5	106.0	203.6	230.9	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{OL}		I_{OL} = 20 µA	0.8 V to 3.6 V			0.1		0.1	V
		I_{OL} = 1.1 mA	1.1 V			0.3 × V_{CC}		0.3 × V_{CC}	
		I_{OL} = 1.7 mA	1.4 V			0.31		0.37	
		I_{OL} = 1.9 mA	1.65 V			0.31		0.35	
		I_{OL} = 2.3 mA	2.3 V			0.31		0.33	
		I_{OL} = 3.1 mA				0.44		0.45	
		I_{OL} = 2.7 mA	3 V			0.31		0.33	
		I_{OL} = 4 mA				0.44		0.45	
I_I	A or B input	V_I = GND to 3.6 V	0 V to 3.6 V			0.1		0.5	µA
I_{off}		V_I or V_O = 0 V to 3.6 V	0 V			0.2		0.6	µA
ΔI_{off}		V_I or V_O = 0 V to 3.6 V	0 V to 0.2 V			0.2		0.6	µA
I_{CC}		V_I = GND or (V_{CC} to 3.6 V), I_O = 0	0.8 V to 3.6 V			0.5		0.9	µA
ΔI_{CC}		V_I = V_{CC} – 0.6 V(1), I_O = 0	3.3 V			40		50	µA
C_i		V_I = V_{CC} or GND	0 V		1.5				pF
			3.6 V		1.5				
C_o		V_O = GND	0 V		3				pF

(1) One input at V_{CC} – 0.6 V, other input at V_{CC} or GND.

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6.6 Switching Characteristics, C_L = 5 pF

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1 and 図 7-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		12.2				ns
			1.2 V ± 0.1 V	3.4	5.1	7.5	1.5	14.7	
			1.5 V ± 0.1 V	2.3	3.6	5.1	1.3	8.3	
			1.8 V ± 0.15 V	2.4	3.1	4	1	6.3	
			2.5 V ± 0.2 V	1.5	2.1	2.9	0.9	4.1	
			3.3 V ± 0.3 V	1.8	2.2	2.8	1.1	3.3	

6.7 Switching Characteristics, C_L = 10 pF

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1 and 図 7-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		15				ns
			1.2 V ± 0.1 V	4	6.2	9	2.4	16.2	
			1.5 V ± 0.1 V	3.1	4.4	6.1	2	9.4	
			1.8 V ± 0.15 V	3.3	3.9	4.8	1.6	7.1	
			2.5 V ± 0.2 V	2.1	2.8	3.5	1.3	4.8	
			3.3 V ± 0.3 V	2.3	3	4	1.4	4.5	

6.8 Switching Characteristics, C_L = 15 pF

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1 and 図 7-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		18.2				ns
			1.2 V ± 0.1 V	4.9	7.3	10.4	3.2	17.6	
			1.5 V ± 0.1 V	3.8	5.2	6.8	2.6	10.2	
			1.8 V ± 0.15 V	3.4	4.8	6.7	2.2	7.9	
			2.5 V ± 0.2 V	2.4	3.4	4.5	1.9	5.3	
			3.3 V ± 0.3 V	2.2	3.7	5.4	1.8	6.1	

6.9 Switching Characteristics, C_L = 30 pF

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1 and 図 7-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		26.5				ns
			1.2 V ± 0.1 V	8.1	10.7	14.4	4.5	21.9	
			1.5 V ± 0.1 V	6.5	7.7	9.4	3.8	13	
			1.8 V ± 0.15 V	5.8	7.5	9.7	3.2	11	
			2.5 V ± 0.2 V	4.5	5.4	6.7	3	7.1	
			3.3 V ± 0.3 V	3.9	6.3	9.7	2.8	10.4	

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6.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	0.8 V	4	pF
			1.2 V ± 0.1 V	4	
			1.5 V ± 0.1 V	4	
			1.8 V ± 0.15 V	4	
			2.5 V ± 0.2 V	4.1	
			3.3 V ± 0.3 V	4.3	

6.11 Typical Characteristics

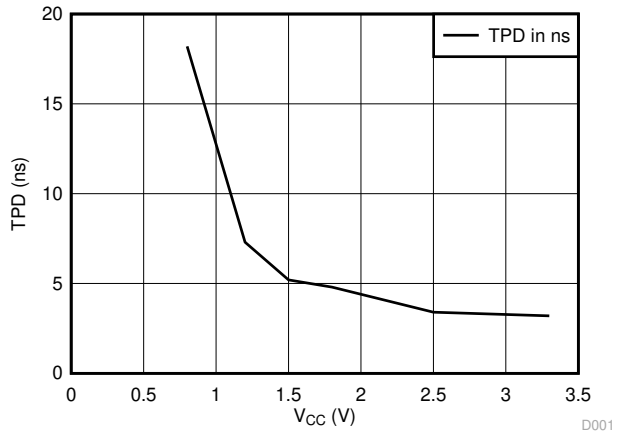


図 6-1. TPD vs V_{CC}

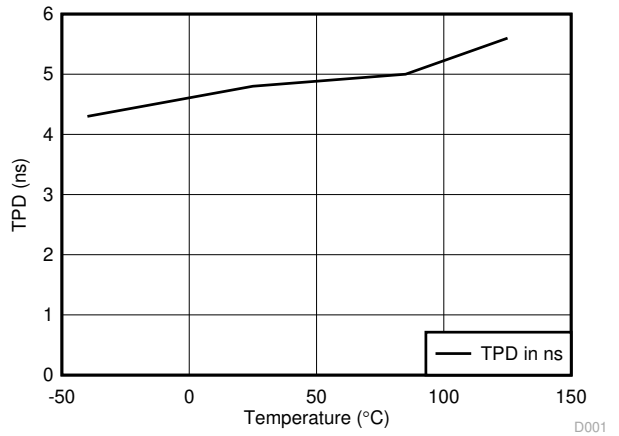
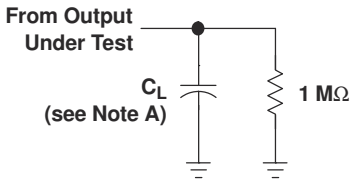


図 6-2. TPD vs Temperature

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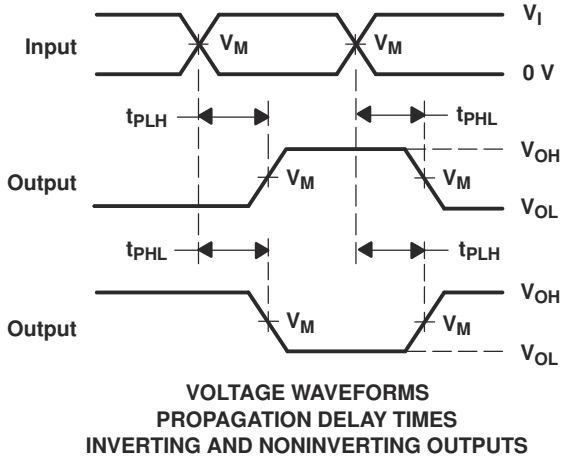
7 Parameter Measurement Information

7.1 Propagation Delays, Setup and Hold Times, and Pulse Duration

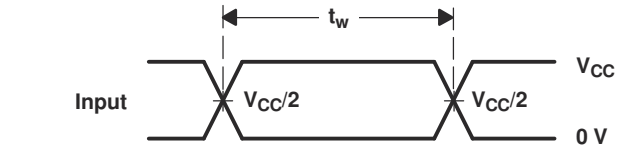


LOAD CIRCUIT

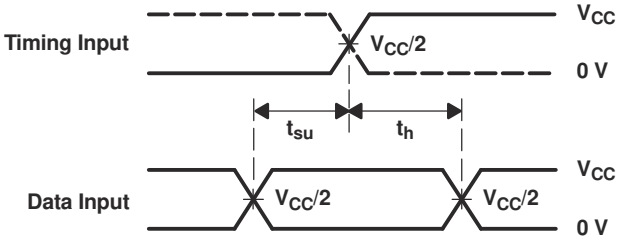
	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATION



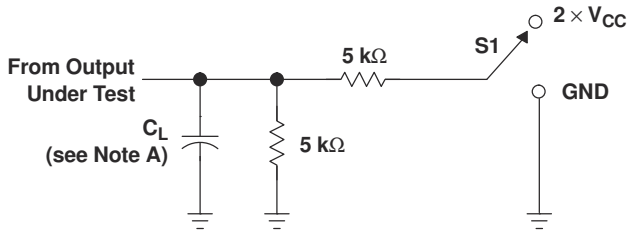
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. All parameters and waveforms are not applicable to all devices.

図 7-1. Load Circuit and Voltage Waveforms

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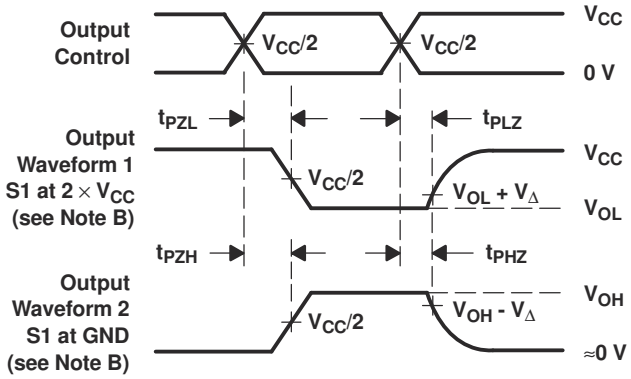
7.2 Enable and Disable Times



LOAD CIRCUIT

TEST	S1
t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	2 × V_{CC} GND

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. All parameters and waveforms are not applicable to all devices.

図 7-2. Load Circuit and Voltage Waveforms

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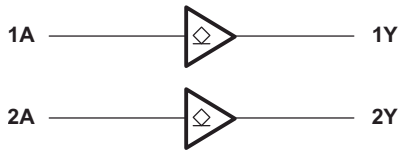
8 Detailed Description

8.1 Overview

The SN74AUP2G07 device is a dual buffer gate with open-drain outputs that operate from 0.8 V to 3.6 V. The output of this dual buffer/driver is open-drain, and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.The I_{off} feature also allows for live insertion.

8.2 Functional Block Diagram



8.3 Feature Description

- Wide operating V_{CC} range of 0.8 V to 3.6 V
- 3.6-V I/O tolerant to support down translation
- Input hysteresis allows slow input transition and better switching noise immunity at the input
- I_{off} feature allows voltages on the inputs and outputs when V_{CC} is 0 V
- Low noise due to slower edge rates

8.4 Device Functional Modes

表 8-1 is the function table for SN74AUP2G07.

表 8-1. Function Table

INPUT(1) A	OUTPUT(2) Y
H	Z
L	L

(1) L = Input low, H = Input high
(2) L = Output low, Z = High impedance

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in increased battery life. This product also maintains excellent signal integrity. It has a small amount of hysteresis built in, allowing for slower or noisy input signals. The lowered drive produces slower edges and prevents overshoot and undershoot on the outputs.

9.2 Typical Application

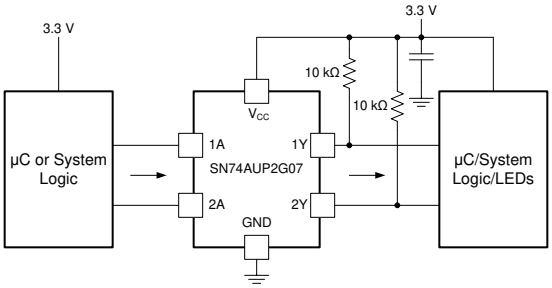


図 9-1. Typical Application Schematic

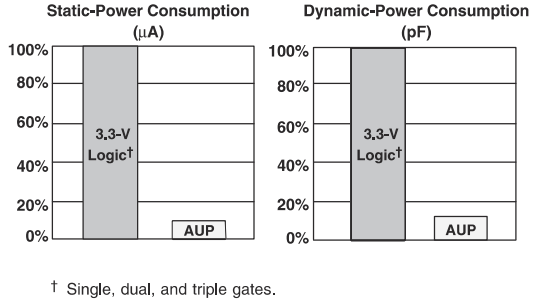
9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits.

9.2.2 Detailed Design Procedure

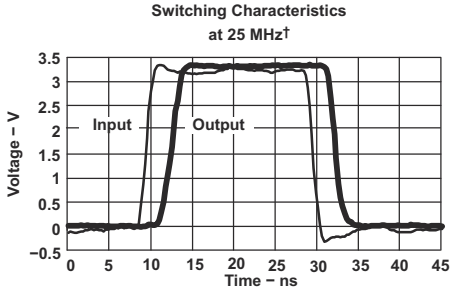
1. Recommended Input Conditions:
   - For rise time and fall time specifications, see Δt/ΔV in the *セクション 6.3* table.
   - For specified high and low levels. See V_{IH} and V_{IL} in the *セクション 6.3* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 3.6 V at any valid V_{CC}.
2. Recommend Output Conditions:
   - Load currents should not exceed 20 mA on the output and 50 mA total for the part.

9.2.3 Application Curves



† Single, dual, and triple gates.

図 9-2. AUP – The Lowest-Power Family



† AUP1G08 data at C_L = 15 pF

図 9-3. Excellent Signal Integrity

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The AUP family of single gate logic makes excellent translators for the new lower voltage microprocessors that typically are powered from 0.8 V to 1.2 V. They can drop the voltage of peripheral drivers and accessories that are still powered by 3.3 V to the new uC power levels.

10 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the *セクション 6.3* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended; if there are multiple V_{CC} pins, then 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 µF and a 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used, or when only 3 of the 4 buffer gates are used.

Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. 図 11-1 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

11.2 Layout Example

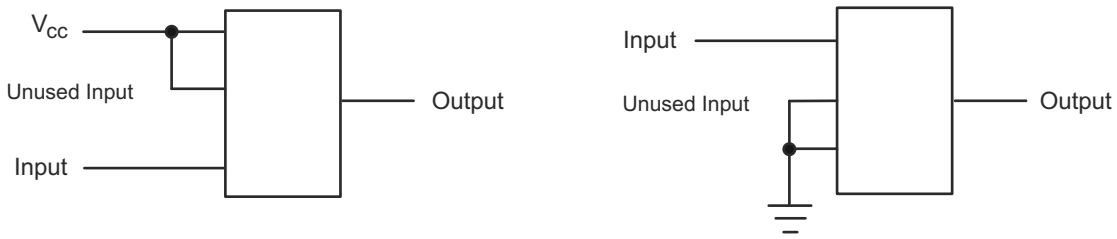


図 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AUP2G07DCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(H55, H5F)
SN74AUP2G07DCKR.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(H55, H5F)
SN74AUP2G07DRYR	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	H5
SN74AUP2G07DRYR.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	H5
SN74AUP2G07DSFR	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	H5
SN74AUP2G07DSFR.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H5
SN74AUP2G07DSFRG4	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H5
SN74AUP2G07DSFRG4.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H5
SN74AUP2G07YFPR	Active	Production	DSBGA (YFP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HVN
SN74AUP2G07YFPR.B	Active	Production	DSBGA (YFP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HVN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

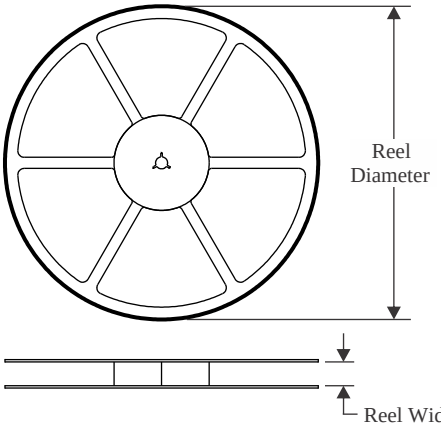
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

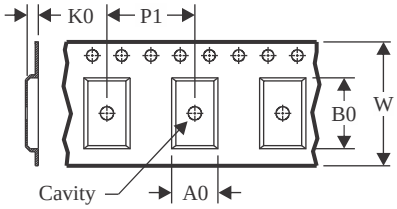
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

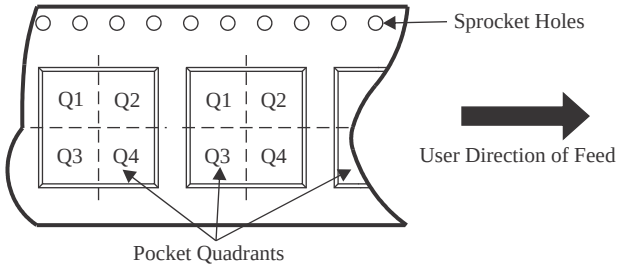


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

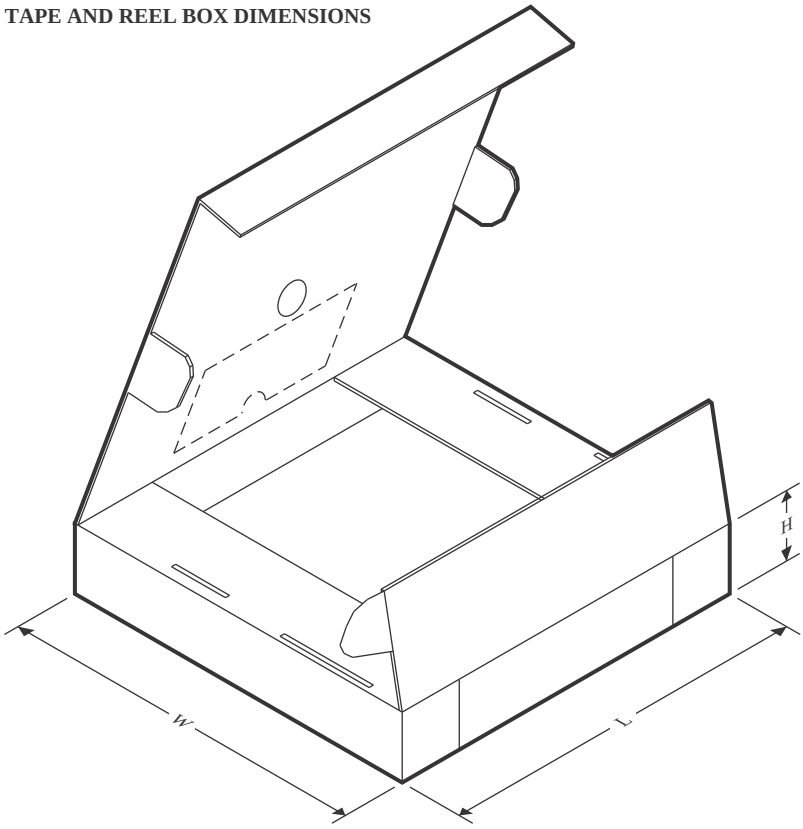
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP2G07DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AUP2G07DCKR	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP2G07DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74AUP2G07DCKR	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74AUP2G07DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
SN74AUP2G07DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP2G07DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP2G07DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
SN74AUP2G07DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP2G07DSFRG4	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP2G07YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

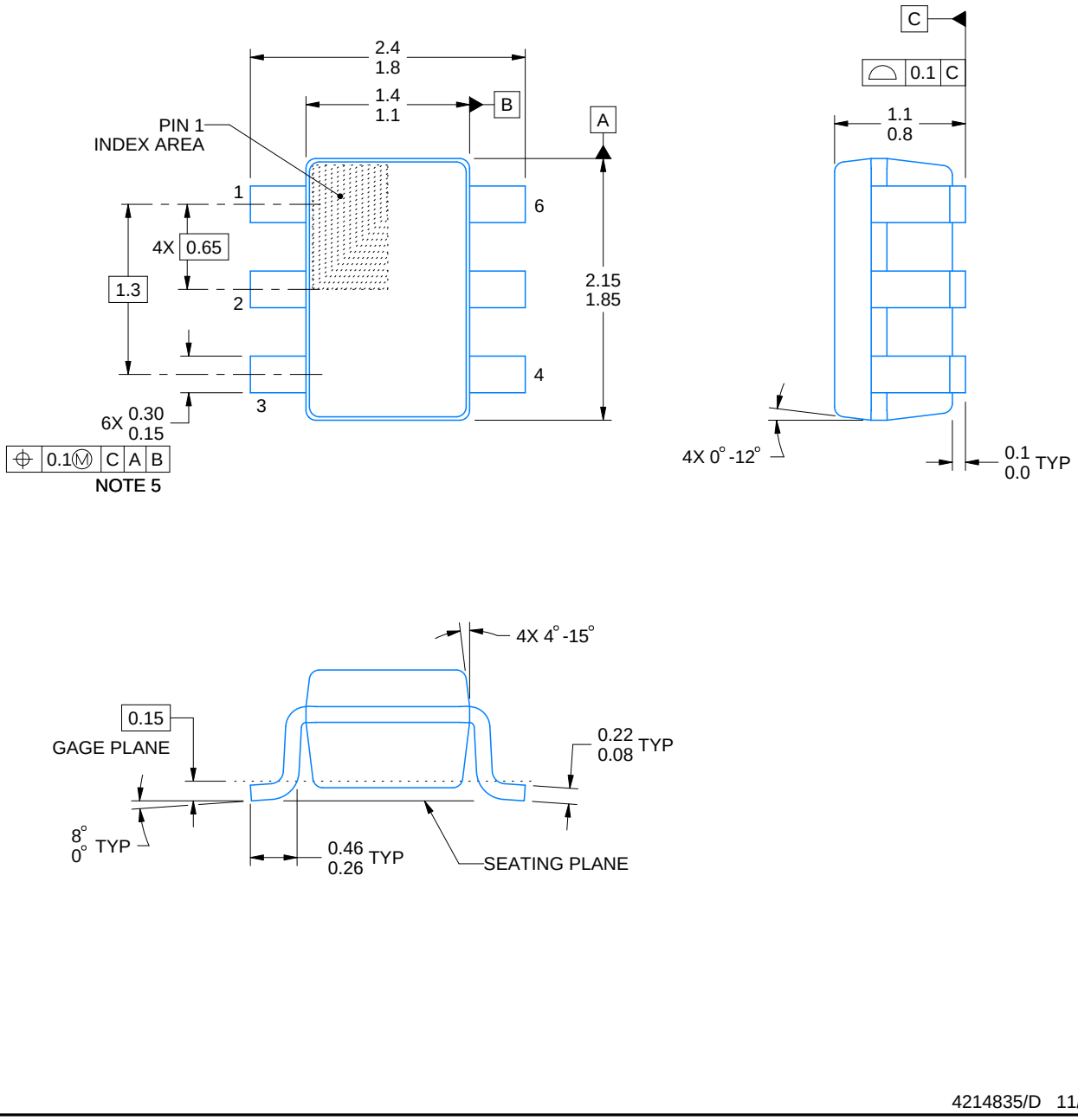
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP2G07DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74AUP2G07DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74AUP2G07DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
SN74AUP2G07DCKR	SC70	DCK	6	3000	208.0	191.0	35.0
SN74AUP2G07DRYR	SON	DRY	6	5000	202.0	201.0	28.0
SN74AUP2G07DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP2G07DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP2G07DSFR	SON	DSF	6	5000	202.0	201.0	28.0
SN74AUP2G07DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP2G07DSFRG4	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP2G07YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

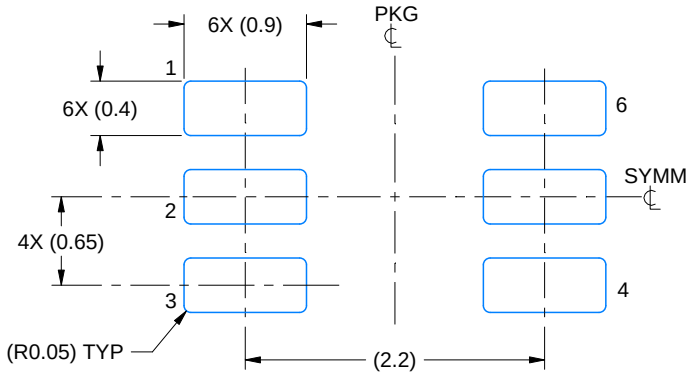
SMALL OUTLINE TRANSISTOR



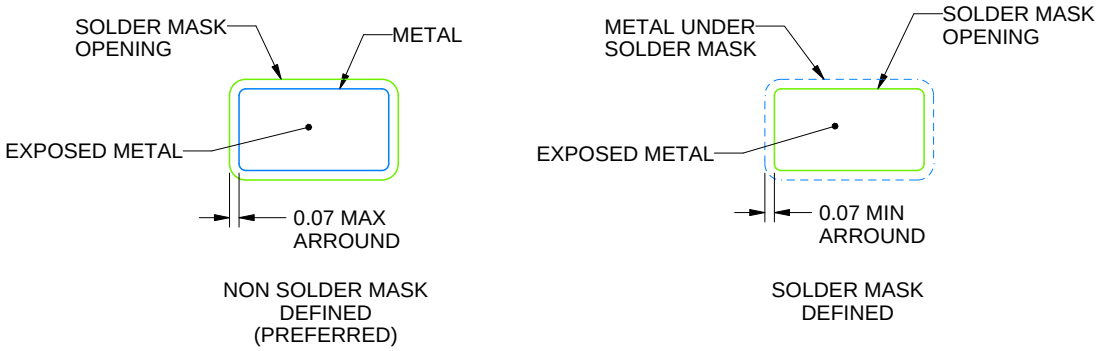
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

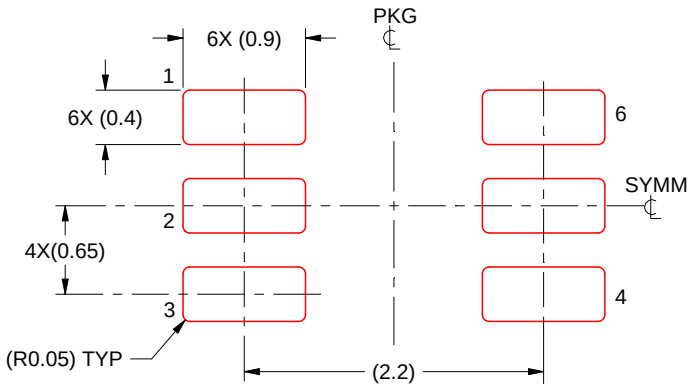


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

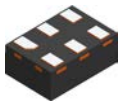
DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

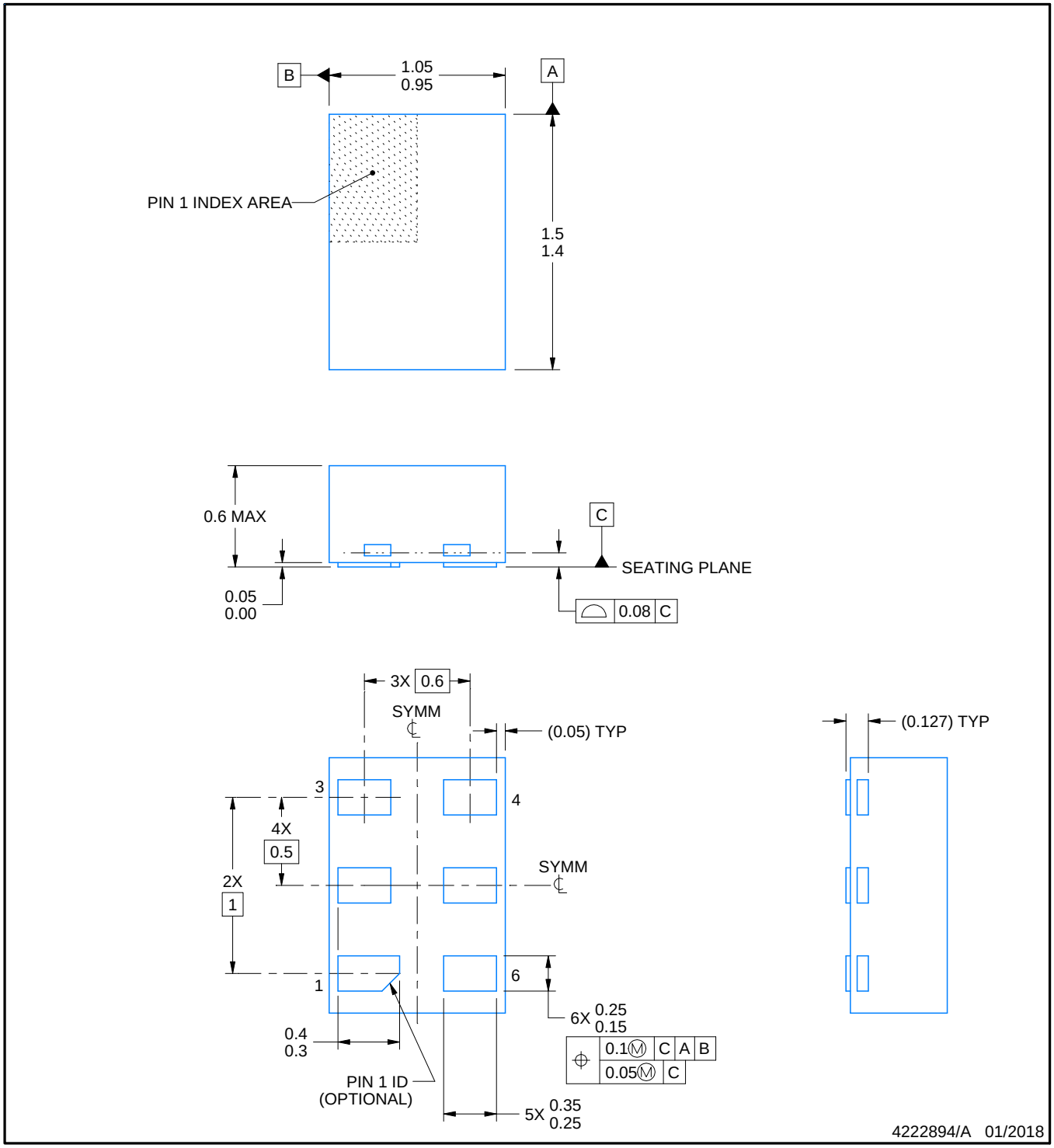
DRY0006A



PACKAGE OUTLINE

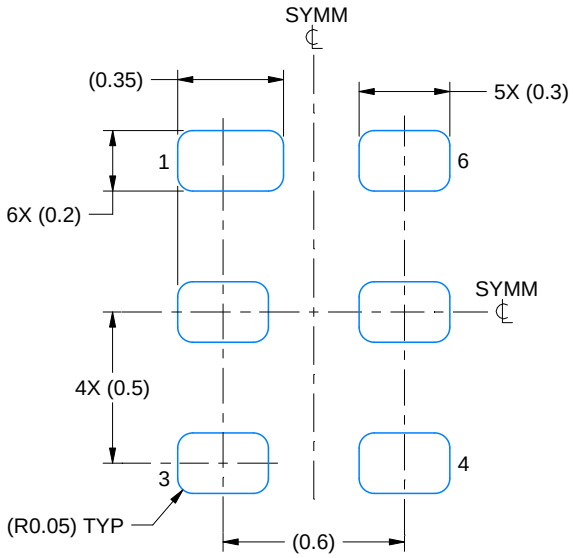
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

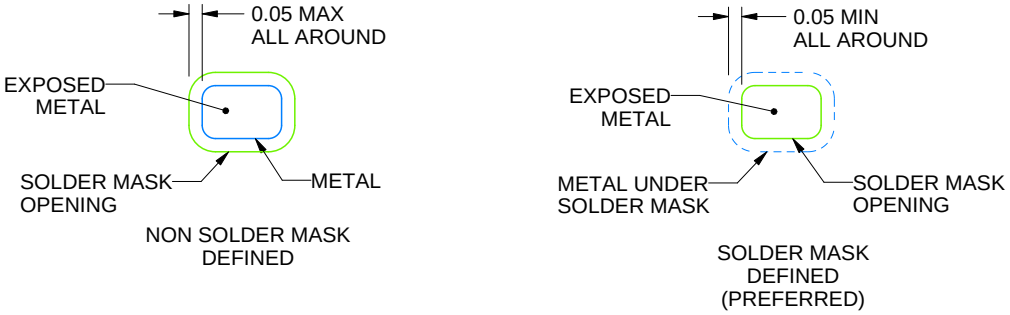


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

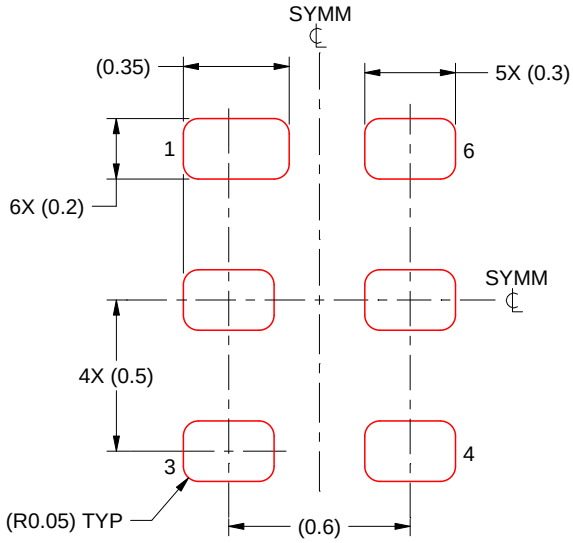
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

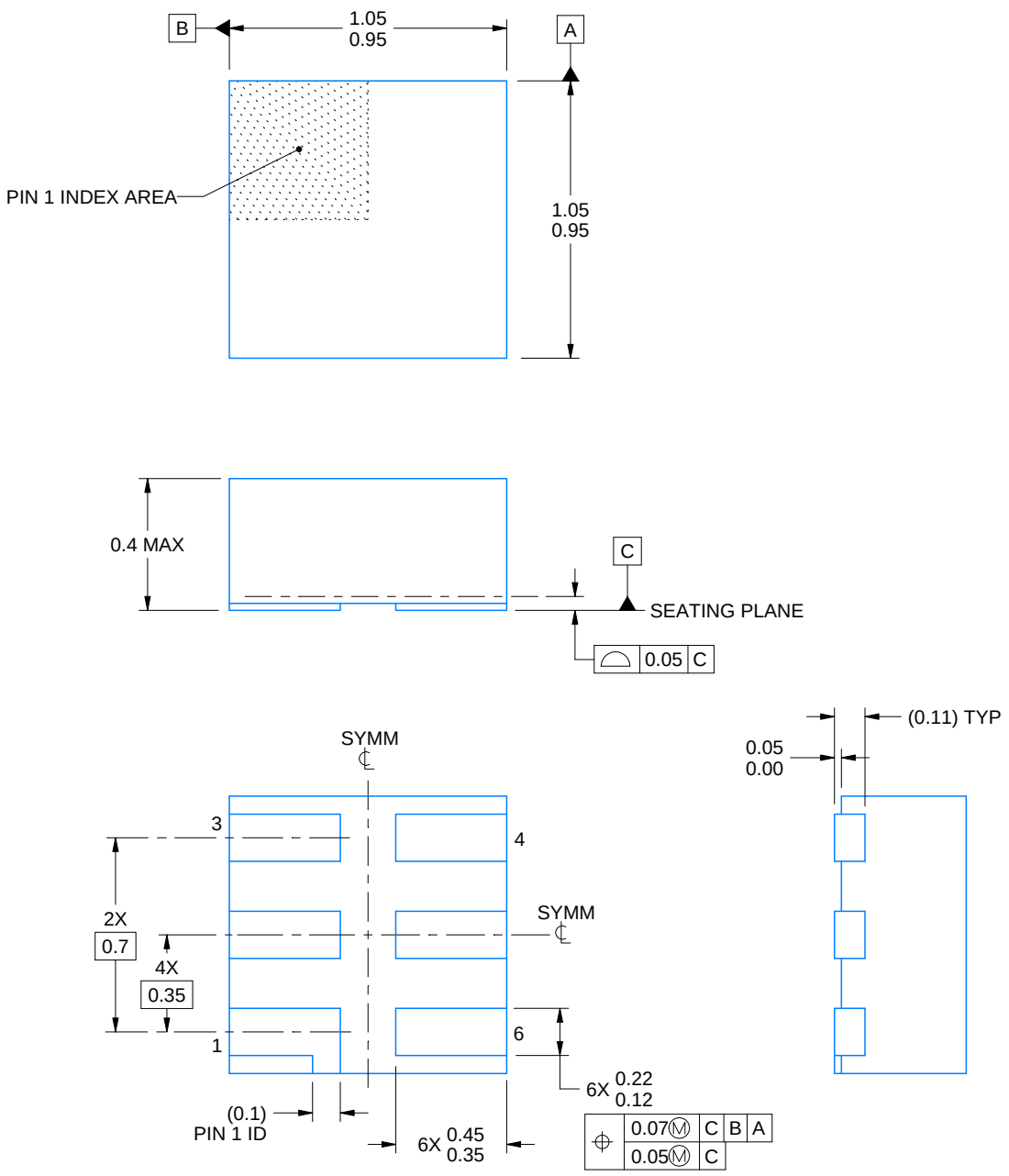
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DSF0006A

X2SON - 0.4 mm max height

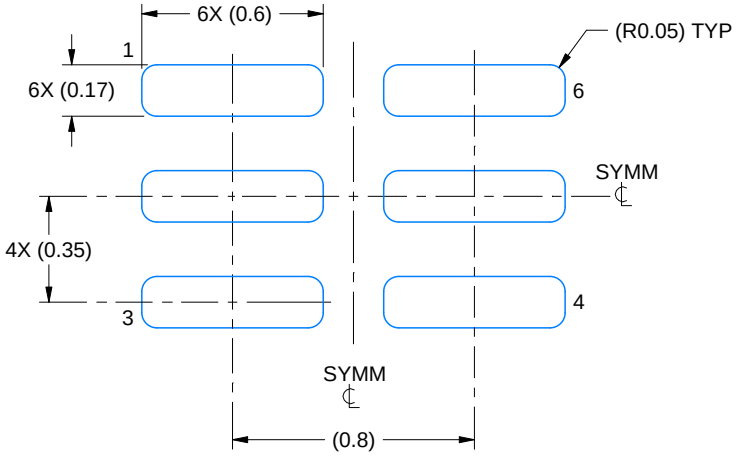
PLASTIC SMALL OUTLINE - NO LEAD



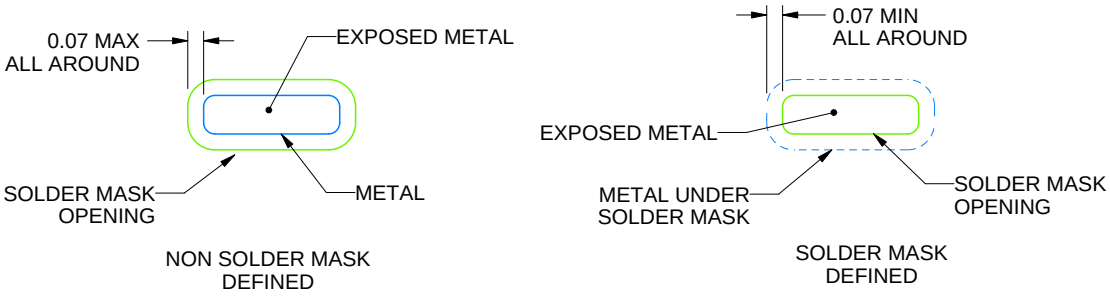
4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

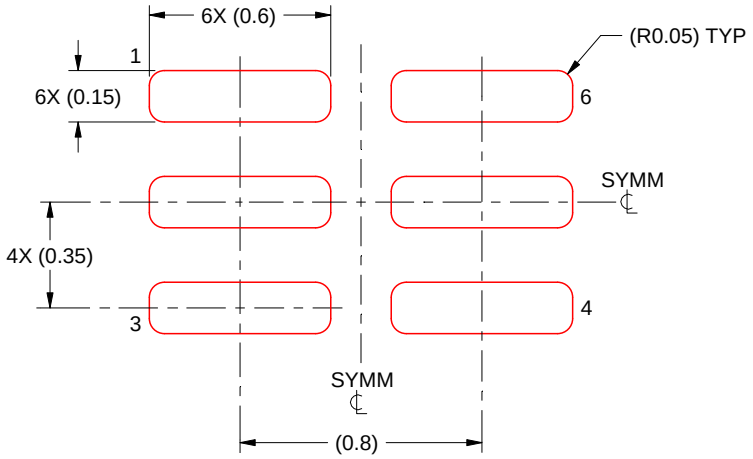
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

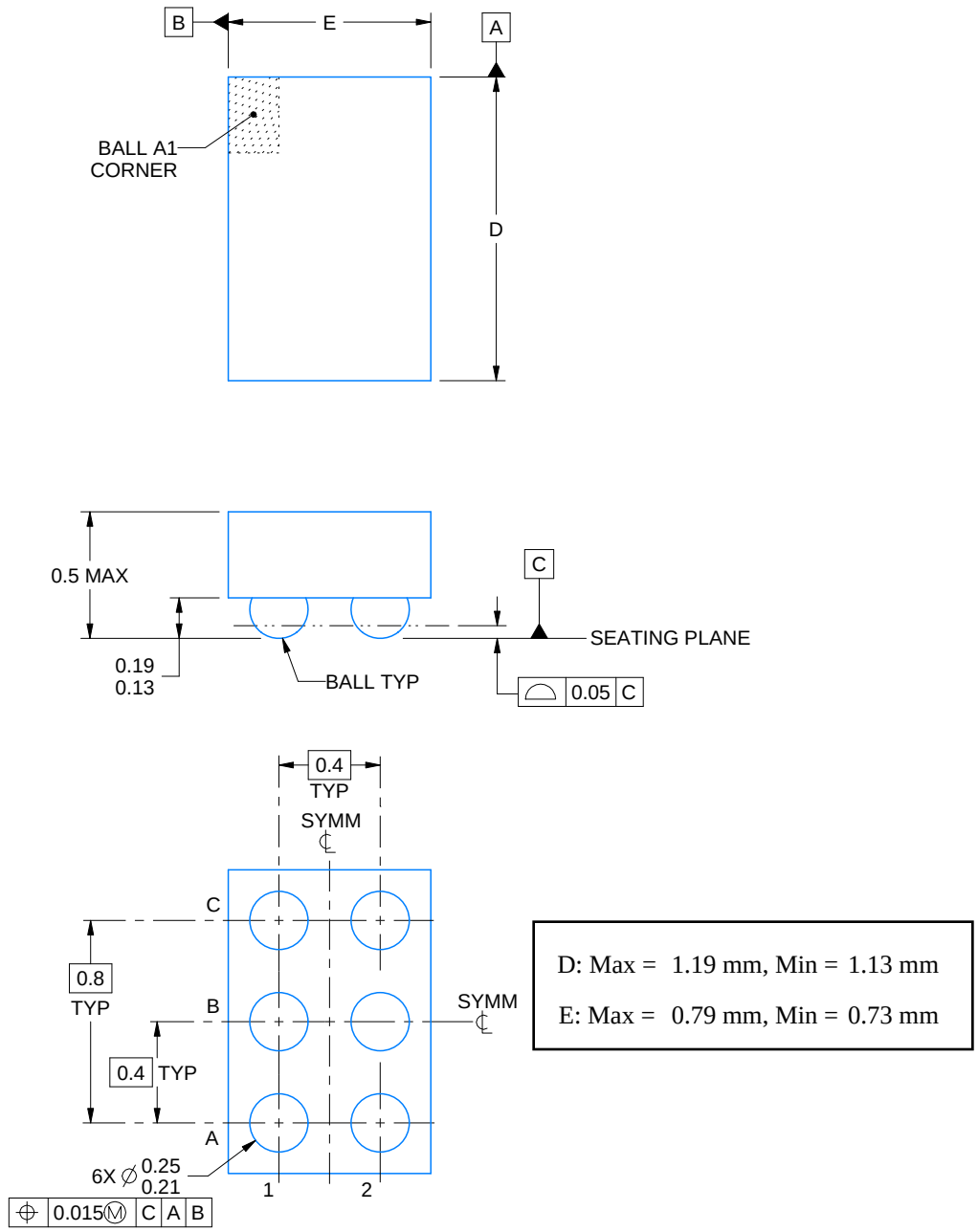
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

YFP0006

DSBGA - 0.5 mm max height

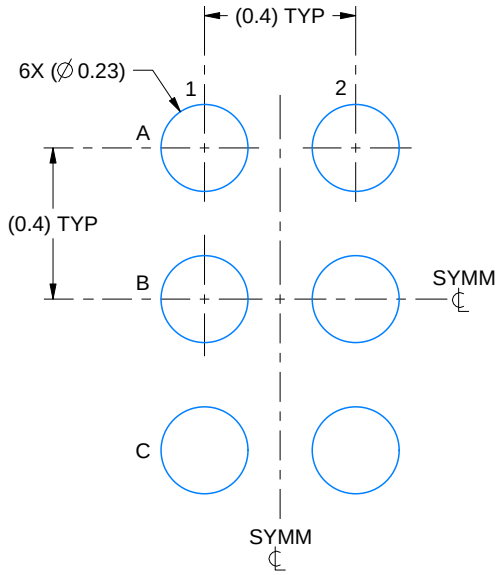
DIE SIZE BALL GRID ARRAY



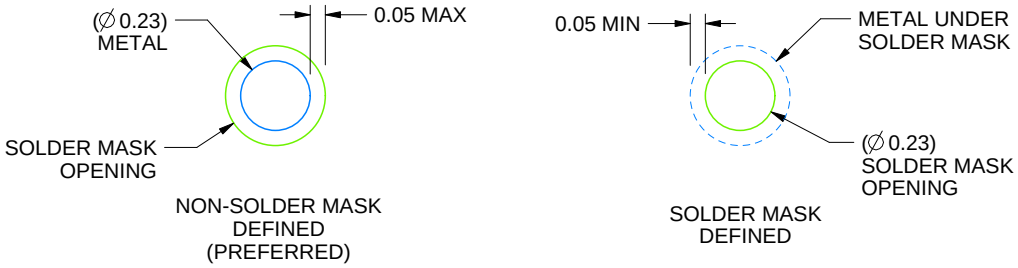
4223410/A 11/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:50X

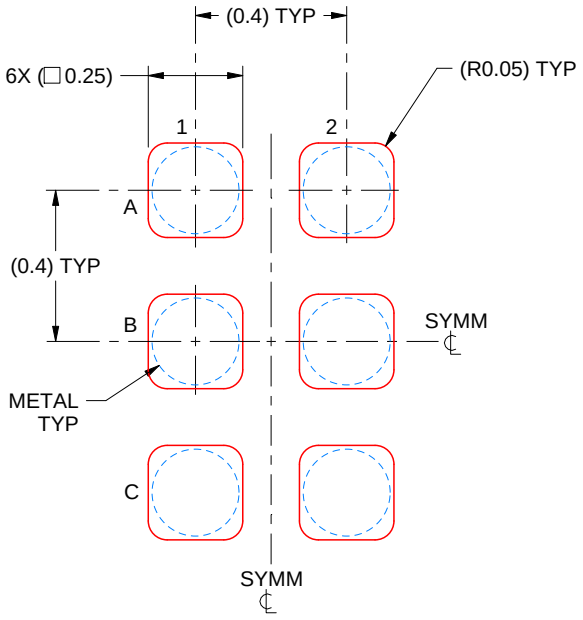


SOLDER MASK DETAILS
NOT TO SCALE

4223410/A 11/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223410/A 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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