

SN74AUP2G07 低消費電力、デュアル・バッファ/ドライバ、オープンドレイン出力

1 特長

- 低い静的消費電力 ($I_{CC} = 0.9\mu A$ 、最大値)
- 低い動的消費電力 (3.3V で $C_{pd} = 1pF$ 、標準値)
- 低い入力容量 ($C_i = 1.5pF$ 、標準値)
- 低いノイズ - オーバーシュートおよびアンダーシュートは V_{CC} の 10% 未満
- I_{off} により活線挿抜、部分的パワーダウン・モード、バック・ドライブ保護をサポート
- 入力ヒステリシスにより低速の入力遷移が可能で、入力におけるスイッチング・ノイズ耐性が向上 (3.3V で $V_{hys} = 250mV$ 、標準値)
- 広い動作 V_{CC} 範囲: 0.8V~3.6V
- 3.3V 動作に最適化
- 3.6V I/O 許容で混在モードの信号動作に対応
- 3.3V で $t_{pd} = 3.3ns$ (最大値)
- ポイント・ツー・ポイントのアプリケーションに好適
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 準拠で ESD 性能を試験済み
 - 人体モデルで 4500V
 - 荷電デバイス・モデルで 1500V

2 アプリケーション

- アクティブ・ノイズ・キャンセレーション (ANC)
- バーコード・スキャナ
- 血圧計
- CPAP 機器
- ケーブル・ソリューション
- DLP 3D マシン・ビジョン、ハイパースペクトル画像処理、光ネットワーク、分光法
- eBook (電子書籍) およびスマートフォン
- 組み込み用 PC
- フィールド・トランスミッタ: 温度または圧力センサ
- 指紋認証
- HVAC: 暖房、換気、空調
- ネットワーク接続ストレージ (NAS)
- サーバーのマザーボードと PSU
- ソフトウェア無線 (SDR)
- テレビ: 高解像度 (HDTV)、LCD、デジタル
- ビデオ通信システム
- ワイヤレス・データ・アクセス・カード、ヘッドセット、キーボード、マウス、LAN カード
- X 線: 手荷物スキャナ、医療用、歯科用

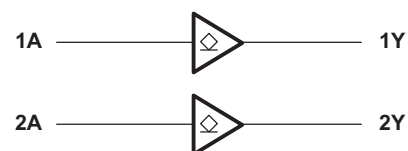
3 概要

SN74AUP2G07 デバイスは、0.8V~3.6V で動作するオープン・ドレイン出力のデュアル・バッファ・ゲートです。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
SN74AUP2G07	SC70 (6)	3.00mm × 1.25mm
	SON (6)	1.45mm × 1.00mm
	SON (6)	1.00mm × 1.00mm
	DSBGA (6)	1.16mm × 0.76mm

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



ブロック概略図



Table of Contents

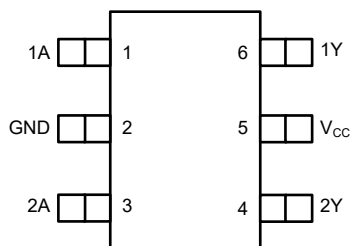
1 特長	1	8 Detailed Description	11
2 アプリケーション	1	8.1 Overview.....	11
3 概要	1	8.2 Functional Block Diagram.....	11
4 Revision History	2	8.3 Feature Description.....	11
5 Pin Configuration and Functions	3	8.4 Device Functional Modes.....	11
6 Specifications	4	9 Application and Implementation	12
6.1 Absolute Maximum Ratings	4	9.1 Application Information.....	12
6.2 ESD Ratings.....	4	9.2 Typical Application.....	12
6.3 Recommended Operating Conditions.....	5	10 Power Supply Recommendations	13
6.4 Thermal Information.....	5	11 Layout	13
6.5 Electrical Characteristics.....	6	11.1 Layout Guidelines.....	13
6.6 Switching Characteristics, $C_L = 5$ pF.....	7	11.2 Layout Example.....	13
6.7 Switching Characteristics, $C_L = 10$ pF.....	7	12 Device and Documentation Support	14
6.8 Switching Characteristics, $C_L = 15$ pF.....	7	12.1 Receiving Notification of Documentation Updates..	14
6.9 Switching Characteristics, $C_L = 30$ pF.....	7	12.2 サポート・リソース.....	14
6.10 Operating Characteristics.....	8	12.3 Trademarks.....	14
6.11 Typical Characteristics.....	8	12.4 Electrostatic Discharge Caution.....	14
7 Parameter Measurement Information	9	12.5 Glossary.....	14
7.1 Propagation Delays, Setup and Hold Times, and Pulse Duration.....	9	13 Mechanical, Packaging, and Orderable Information	14
7.2 Enable and Disable Times.....	10		

4 Revision History

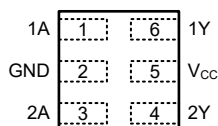
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (February 2016) to Revision E (October 2021)	Page
• Changed pinout images style and formatting, removed overlapping letters in YZP package drawing, corrected BGA pin numbers in the <i>Pin Functions</i> table, changed V_{CC} and GND pin TYPE From: "—" To: "P" in the <i>Pin Functions</i> table and added footnote to the <i>Pin Functions</i> table to define pin types.....	3
• Changed maximum output voltage in the low state in the セクション 6.1 table to 4.6 V.....	4
• Changed the V_O Output voltage in the セクション 6.3 table from ' V_{CC} ' to '3.6'.....	5
• Updated $R_{\theta JA}$ values to more accurately reflect device characteristics: YFP 132 to 125.4, DCK 252 to 302.4, DRY 234 to 338, DSF 300 to 372.5, added standard thermal characteristics for all packages ($R_{\theta JC(top)}$, $R_{\theta JB}$, Ψ_{JT} , Ψ_{JB} , $R_{\theta JC(bot)}$).....	5
Changes from Revision C (November 2014) to Revision D (February 2016)	Page
• Changed the V_{CC} pin TYPE From: "I" To: "—" in the <i>Pin Functions</i> table.....	3
• Added "Junction temperature" to the セクション 6.1 table	4
• Deleted the I_{OH} High-level output current from the セクション 6.3 table	5
• Deleted V_{OH} PARAMETER from the セクション 6.5 table, these specifications do not pertain to open drain devices.....	6
Changes from Revision B (September 2009) to Revision C (November 2014)	Page
• 「注文情報」表を削除.....	1
• 「アプリケーション」セクション、「製品情報」表、「ピン機能」表、「取り扱いに関する定格」表、「熱に関する情報」表、「代表的特性」セクション、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加.....	1
• 「特長」の I_{off} を更新.....	1

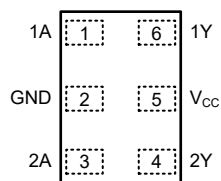
5 Pin Configuration and Functions



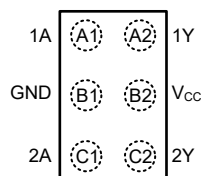
**5-1. DCK Package
6-Pin SC70
Top View**



**5-3. DSF Package
6-Pin SON
Transparent Top View**



**5-2. DRY Package
6-Pin SON
Transparent Top View**



**5-4. YFP Package
6-Pin DSBGA
Transparent Top View**

See the mechanical drawings for dimensions.

表 5-1. Pin Functions

NAME	PIN		TYPE ⁽¹⁾	DESCRIPTION
	DCK, DSF, DRY, YFP	(BGA) YFP		
1A	1	A1	I	Input 1
1Y	6	A2	O	Output 1
2A	3	C1	I	Input 2
2Y	4	C2	O	Output 2
GND	2	B1	P	Ground
V _{CC}	5	B2	P	Power Pin

(1) I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		−0.5	4.6	V
V _I	Input voltage range ⁽¹⁾		−0.5	4.6	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽¹⁾		−0.5	4.6	V
V _O	Output voltage range in the low state ⁽¹⁾		−0.5	4.6	V
I _{IK}	Input clamp current	V _I < 0		−50	mA
I _{OK}	Output clamp current	V _O < 0		−50	mA
I _O	Continuous output current			±20	mA
	Continuous current through V _{CC} or GND			±50	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature range		−65	150	°C

(1) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4500
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT	
V _{CC}	Supply voltage		0.8	3.6	V	
V _{IH}	High-level input voltage	V _{CC} = 0.8 V	V _{CC}		V	
		V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}			
		V _{CC} = 2.3 V to 2.7 V	1.6			
		V _{CC} = 3 V to 3.6 V	2			
V _{IL}	Low-level input voltage	V _{CC} = 0.8 V		0	V	
		V _{CC} = 1.1 V to 1.95 V		0.35 × V _{CC}		
		V _{CC} = 2.3 V to 2.7 V		0.7		
		V _{CC} = 3 V to 3.6 V		0.9		
V _I	Input voltage		0	3.6	V	
V _O	Output voltage		0	3.6	V	
I _{OL}	Low-level output current	V _{CC} = 0.8 V		20	μA	
		V _{CC} = 1.1 V		1.1		mA
		V _{CC} = 1.4 V		1.7		
		V _{CC} = 1.65 V		1.9		
		V _{CC} = 2.3 V		3.1		
		V _{CC} = 3 V		4		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 0.8 V to 3.6 V		200	ns/V	
T _A	Operating free-air temperature		−40	85	°C	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		YFP	DCK	DRY	DSF	UNIT
		6 PINS	6 PINS	6 PINS	6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	125.4	302.4	338.0	372.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	1.9	219.5	228.9	179.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	37.2	106.7	203.5	231.2	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.5	84.2	62.4	28.6	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	37.5	106.0	203.6	230.9	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V _{OL}	I _{OL} = 20 μA		0.8 V to 3.6 V	0.1			0.1		V
	I _{OL} = 1.1 mA		1.1 V	0.3 × V _{CC}			0.3 × V _{CC}		
	I _{OL} = 1.7 mA		1.4 V	0.31			0.37		
	I _{OL} = 1.9 mA		1.65 V	0.31			0.35		
	I _{OL} = 2.3 mA		2.3 V	0.31			0.33		
	I _{OL} = 3.1 mA			0.44			0.45		
	I _{OL} = 2.7 mA		3 V	0.31			0.33		
	I _{OL} = 4 mA			0.44			0.45		
I _I	A or B input	V _I = GND to 3.6 V	0 V to 3.6 V	0.1			0.5		μA
I _{off}		V _I or V _O = 0 V to 3.6 V	0 V	0.2			0.6		μA
ΔI _{off}		V _I or V _O = 0 V to 3.6 V	0 V to 0.2 V	0.2			0.6		μA
I _{CC}		V _I = GND or (V _{CC} to 3.6 V), I _O = 0	0.8 V to 3.6 V	0.5			0.9		μA
ΔI _{CC}		V _I = V _{CC} − 0.6 V ⁽¹⁾ , I _O = 0	3.3 V	40			50		μA
C _i		V _I = V _{CC} or GND	0 V	1.5					pF
			3.6 V	1.5					
C _o		V _O = GND	0 V	3					pF

(1) One input at $V_{CC} - 0.6\ \text{V}$, other input at V_{CC} or GND.

6.6 Switching Characteristics, $C_L = 5 \text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted) (see [7-1](#) and [7-2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		12.2				ns
			1.2 V $\pm$ 0.1 V	3.4	5.1	7.5	1.5	14.7	
			1.5 V $\pm$ 0.1 V	2.3	3.6	5.1	1.3	8.3	
			1.8 V $\pm$ 0.15 V	2.4	3.1	4	1	6.3	
			2.5 V $\pm$ 0.2 V	1.5	2.1	2.9	0.9	4.1	
			3.3 V $\pm$ 0.3 V	1.8	2.2	2.8	1.1	3.3	

6.7 Switching Characteristics, $C_L = 10 \text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted) (see [7-1](#) and [7-2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		15				ns
			1.2 V $\pm$ 0.1 V	4	6.2	9	2.4	16.2	
			1.5 V $\pm$ 0.1 V	3.1	4.4	6.1	2	9.4	
			1.8 V $\pm$ 0.15 V	3.3	3.9	4.8	1.6	7.1	
			2.5 V $\pm$ 0.2 V	2.1	2.8	3.5	1.3	4.8	
			3.3 V $\pm$ 0.3 V	2.3	3	4	1.4	4.5	

6.8 Switching Characteristics, $C_L = 15 \text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted) (see [7-1](#) and [7-2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		18.2				ns
			1.2 V $\pm$ 0.1 V	4.9	7.3	10.4	3.2	17.6	
			1.5 V $\pm$ 0.1 V	3.8	5.2	6.8	2.6	10.2	
			1.8 V $\pm$ 0.15 V	3.4	4.8	6.7	2.2	7.9	
			2.5 V $\pm$ 0.2 V	2.4	3.4	4.5	1.9	5.3	
			3.3 V $\pm$ 0.3 V	2.2	3.7	5.4	1.8	6.1	

6.9 Switching Characteristics, $C_L = 30 \text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted) (see [7-1](#) and [7-2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		26.5				ns
			1.2 V $\pm$ 0.1 V	8.1	10.7	14.4	4.5	21.9	
			1.5 V $\pm$ 0.1 V	6.5	7.7	9.4	3.8	13	
			1.8 V $\pm$ 0.15 V	5.8	7.5	9.7	3.2	11	
			2.5 V $\pm$ 0.2 V	4.5	5.4	6.7	3	7.1	
			3.3 V $\pm$ 0.3 V	3.9	6.3	9.7	2.8	10.4	

6.10 Operating Characteristics

 $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$f = 10\text{ MHz}$	0.8 V	4	pF
		1.2 V $\pm$ 0.1 V	4	
		1.5 V $\pm$ 0.1 V	4	
		1.8 V $\pm$ 0.15 V	4	
		2.5 V $\pm$ 0.2 V	4.1	
		3.3 V $\pm$ 0.3 V	4.3	

6.11 Typical Characteristics

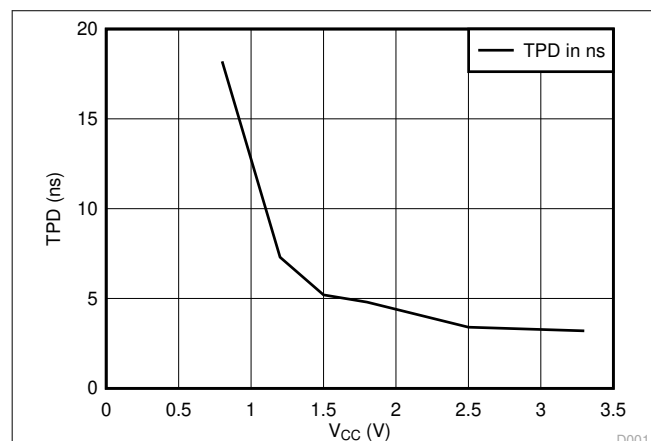


FIG 6-1. TPD vs V_{CC}

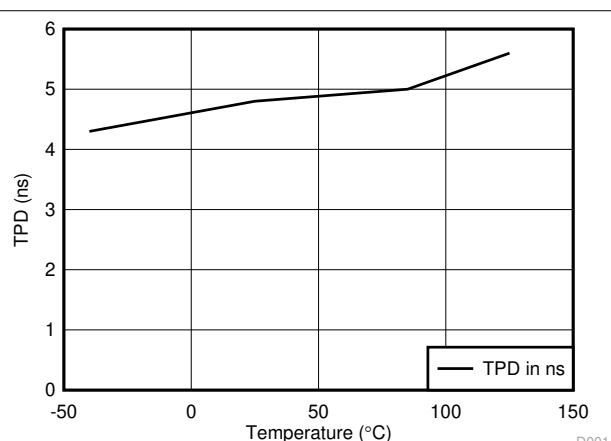
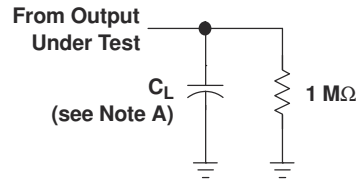


FIG 6-2. TPD vs Temperature

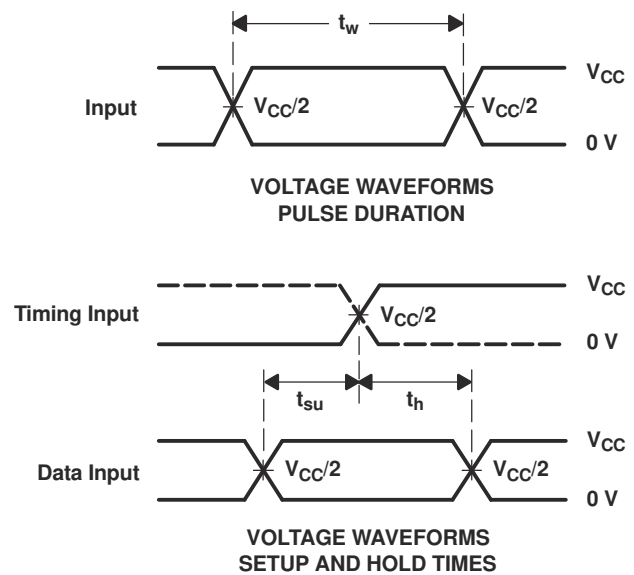
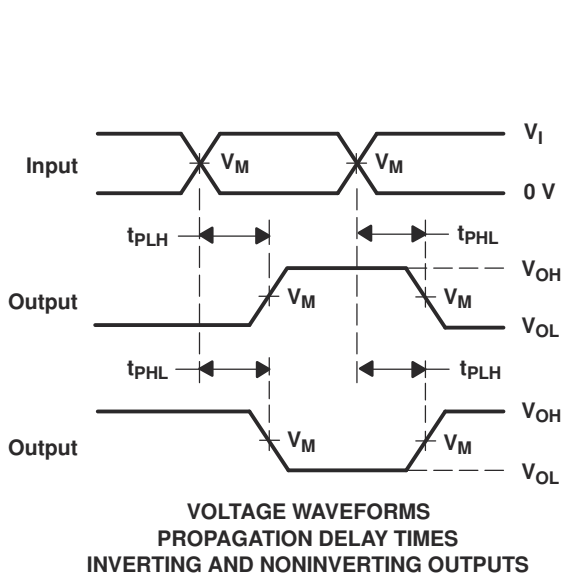
7 Parameter Measurement Information

7.1 Propagation Delays, Setup and Hold Times, and Pulse Duration



LOAD CIRCUIT

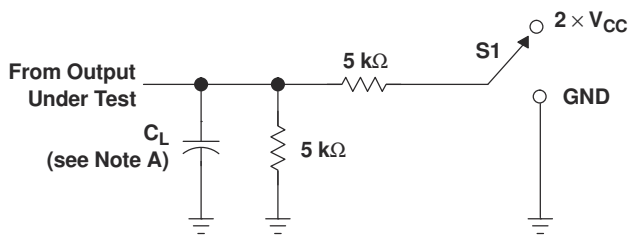
	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r/t_f = 3 \text{ ns}$.
 - C. The outputs are measured one at a time, with one transition per measurement.
 - D. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - E. All parameters and waveforms are not applicable to all devices.

FIG 7-1. Load Circuit and Voltage Waveforms

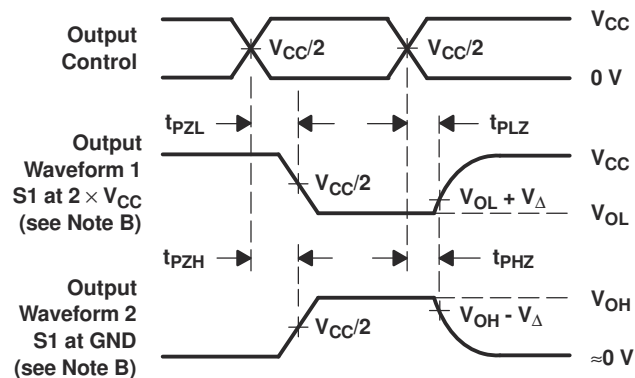
7.2 Enable and Disable Times



LOAD CIRCUIT

TEST	S1
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHL}	GND

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_{Δ}	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r/t_f = 3 \text{ ns}$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PHL} are the same as t_{en} .
 - G. All parameters and waveforms are not applicable to all devices.

7-2. Load Circuit and Voltage Waveforms

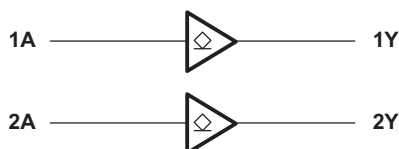
8 Detailed Description

8.1 Overview

The SN74AUP2G07 device is a dual buffer gate with open-drain outputs that operate from 0.8 V to 3.6 V. The output of this dual buffer/driver is open-drain, and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The I_{off} feature also allows for live insertion.

8.2 Functional Block Diagram



8.3 Feature Description

- Wide operating V_{CC} range of 0.8 V to 3.6 V
- 3.6-V I/O tolerant to support down translation
- Input hysteresis allows slow input transition and better switching noise immunity at the input
- I_{off} feature allows voltages on the inputs and outputs when V_{CC} is 0 V
- Low noise due to slower edge rates

8.4 Device Functional Modes

表 8-1 is the function table for SN74AUP2G07.

表 8-1. Function Table

INPUT ⁽¹⁾ A	OUTPUT ⁽²⁾ Y
H	Z
L	L

(1) L = Input low, H = Input high

(2) L = Output low, Z = High impedance

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in increased battery life. This product also maintains excellent signal integrity. It has a small amount of hysteresis built in, allowing for slower or noisy input signals. The lowered drive produces slower edges and prevents overshoot and undershoot on the outputs.

9.2 Typical Application

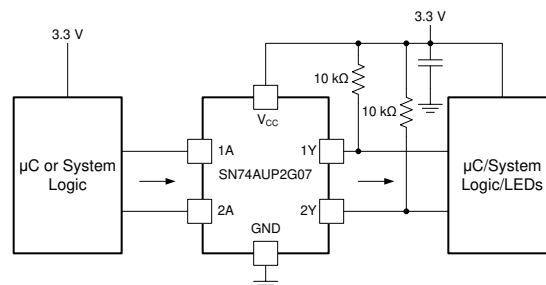


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits.

9.2.2 Detailed Design Procedure

- Recommended Input Conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the [セクション 6.3](#) table.
 - For specified high and low levels. See V_{IH} and V_{IL} in the [セクション 6.3](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 3.6 V at any valid V_{CC} .
- Recommend Output Conditions:
 - Load currents should not exceed 20 mA on the output and 50 mA total for the part.

9.2.3 Application Curves

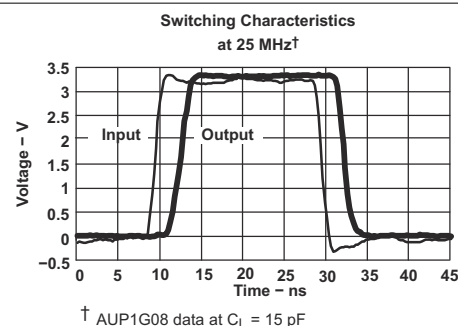
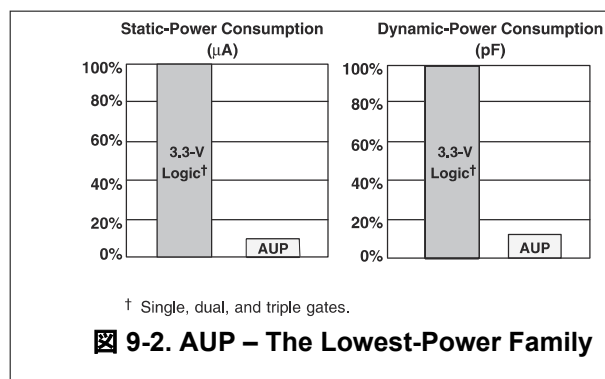


Figure 9-3. Excellent Signal Integrity

The AUP family of single gate logic makes excellent translators for the new lower voltage microprocessors that typically are powered from 0.8 V to 1.2 V. They can drop the voltage of peripheral drivers and accessories that are still powered by 3.3 V to the new uC power levels.

10 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the [セクション 6.3](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended; if there are multiple V_{CC} pins, then 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 μF and a 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used, or when only 3 of the 4 buffer gates are used.

Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [図 11-1](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

11.2 Layout Example

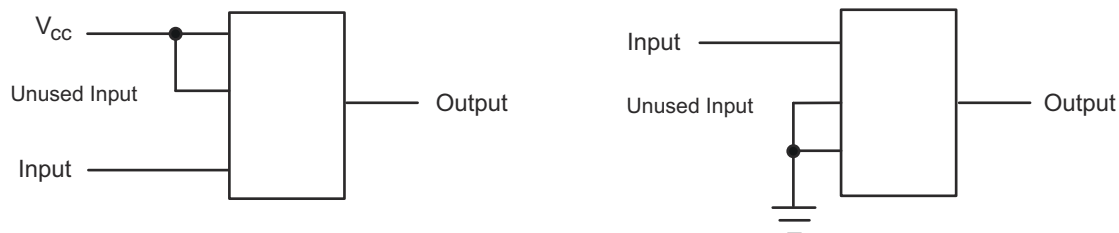


図 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 サポート・リソース

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12.3 Trademarks

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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AUP2G07DCKR	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(H55, H5F)
SN74AUP2G07DCKR.B	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(H55, H5F)
SN74AUP2G07DRYR	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	H5
SN74AUP2G07DRYR.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	H5
SN74AUP2G07DSFR	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	H5
SN74AUP2G07DSFR.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H5
SN74AUP2G07DSFRG4	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H5
SN74AUP2G07DSFRG4.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H5
SN74AUP2G07YFPR	Active	Production	DSBGA (YFP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HVN
SN74AUP2G07YFPR.B	Active	Production	DSBGA (YFP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HVN

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP2G07DCKR	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP2G07DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74AUP2G07DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AUP2G07DCKR	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74AUP2G07DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
SN74AUP2G07DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP2G07DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP2G07DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP2G07DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
SN74AUP2G07DSFRG4	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP2G07YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP2G07DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74AUP2G07DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
SN74AUP2G07DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74AUP2G07DCKR	SC70	DCK	6	3000	208.0	191.0	35.0
SN74AUP2G07DRYR	SON	DRY	6	5000	202.0	201.0	28.0
SN74AUP2G07DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP2G07DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP2G07DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP2G07DSFR	SON	DSF	6	5000	202.0	201.0	28.0
SN74AUP2G07DSFRG4	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP2G07YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0

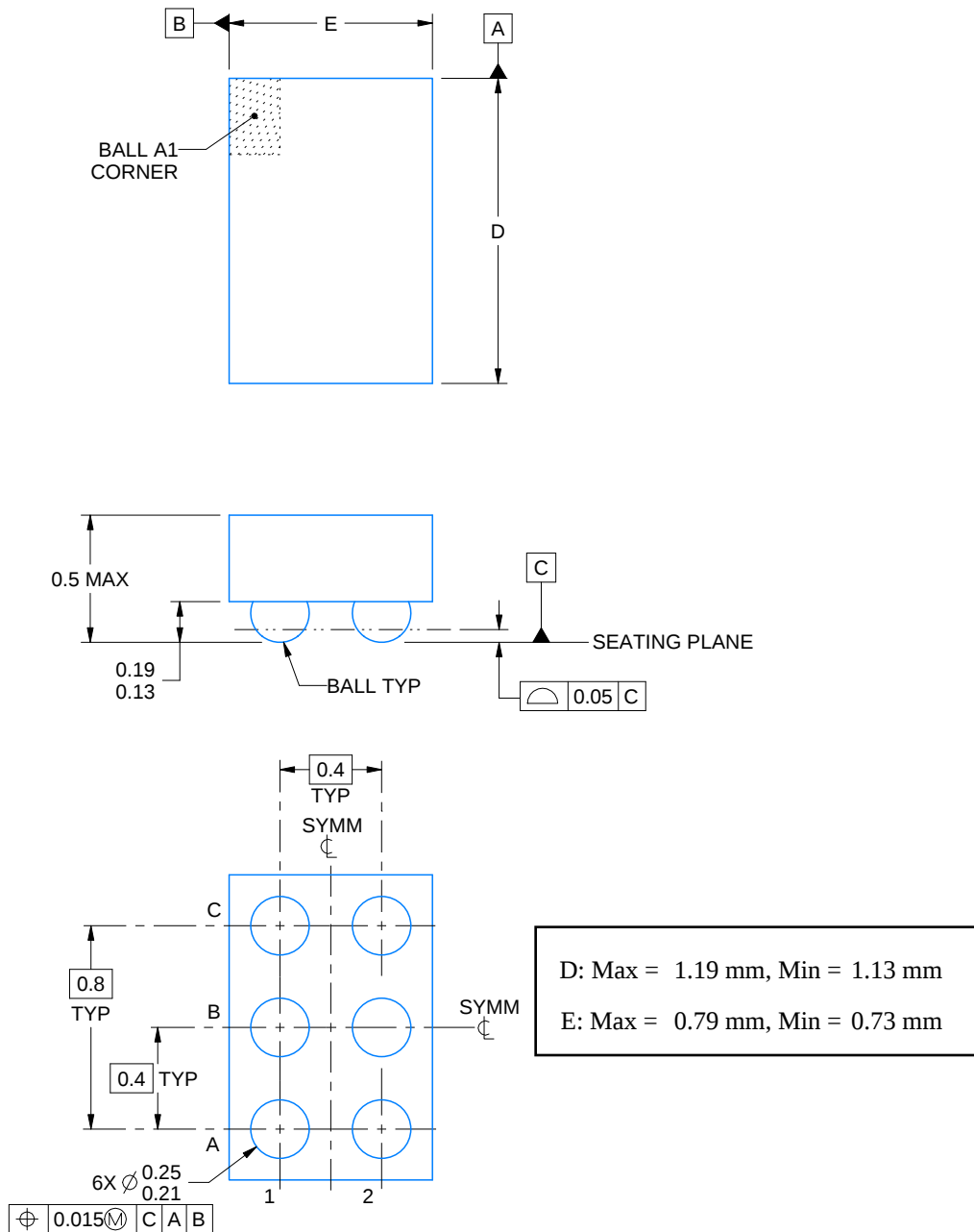
YFP0006



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

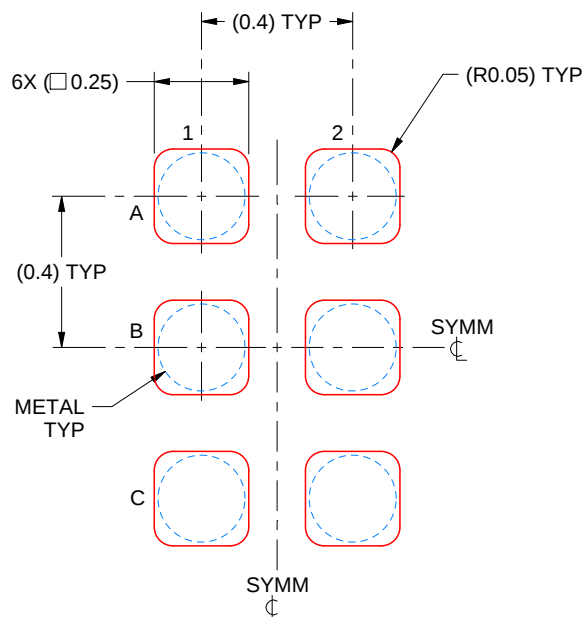
DIE SIZE BALL GRID ARRAY



4223410/A 11/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

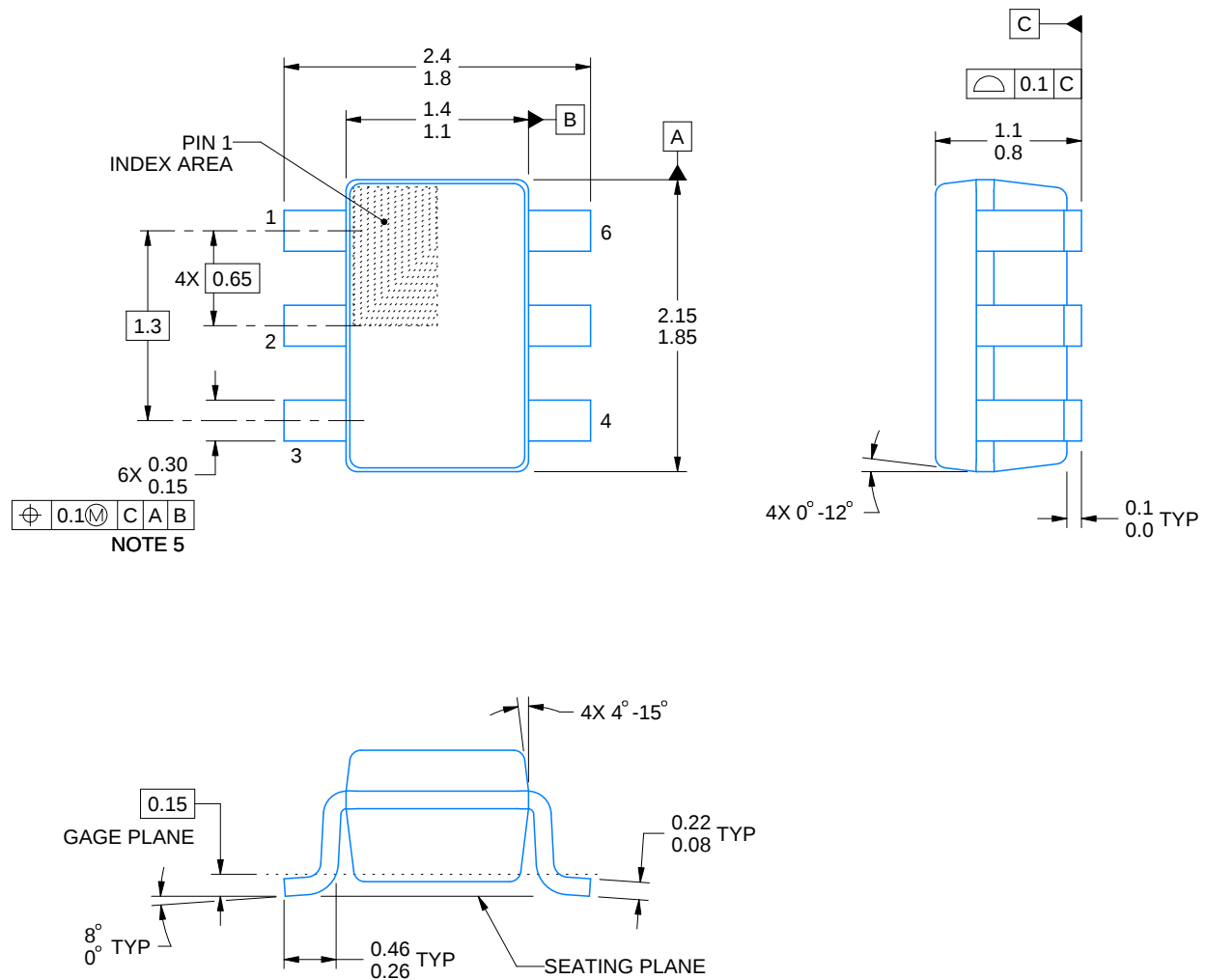


SOLDER PASTE EXAMPLE
 BASED ON 0.1 mm THICK STENCIL
 SCALE:50X

4223410/A 11/2016

NOTES: (continued)

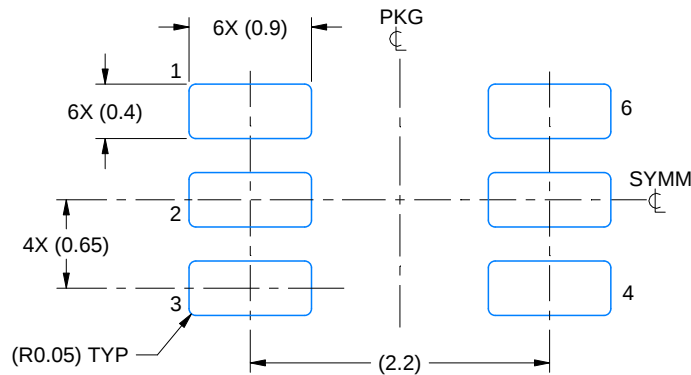
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



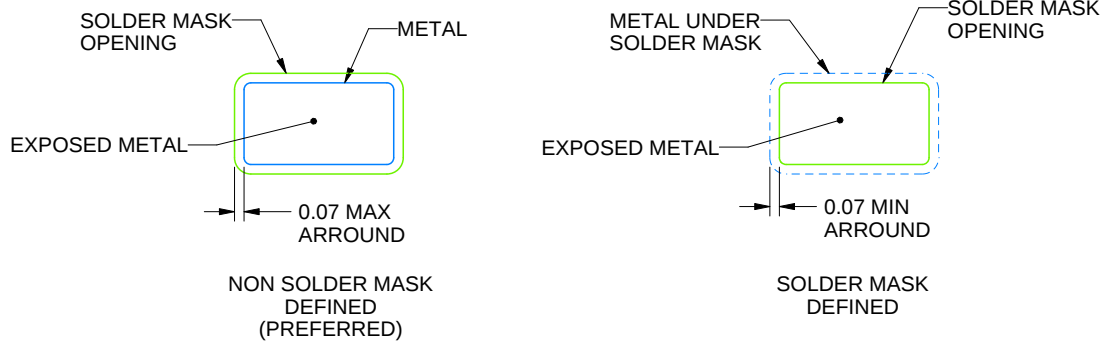
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

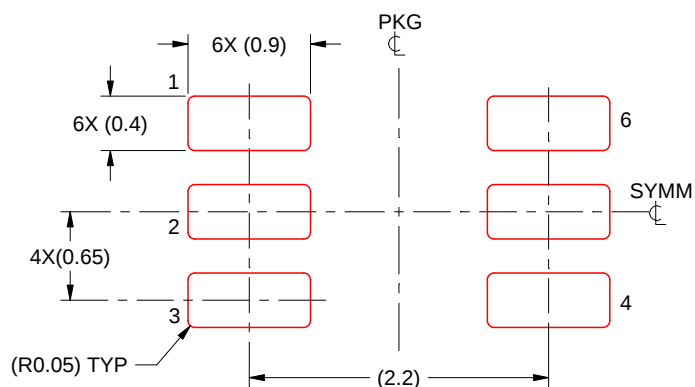


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRY 6

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

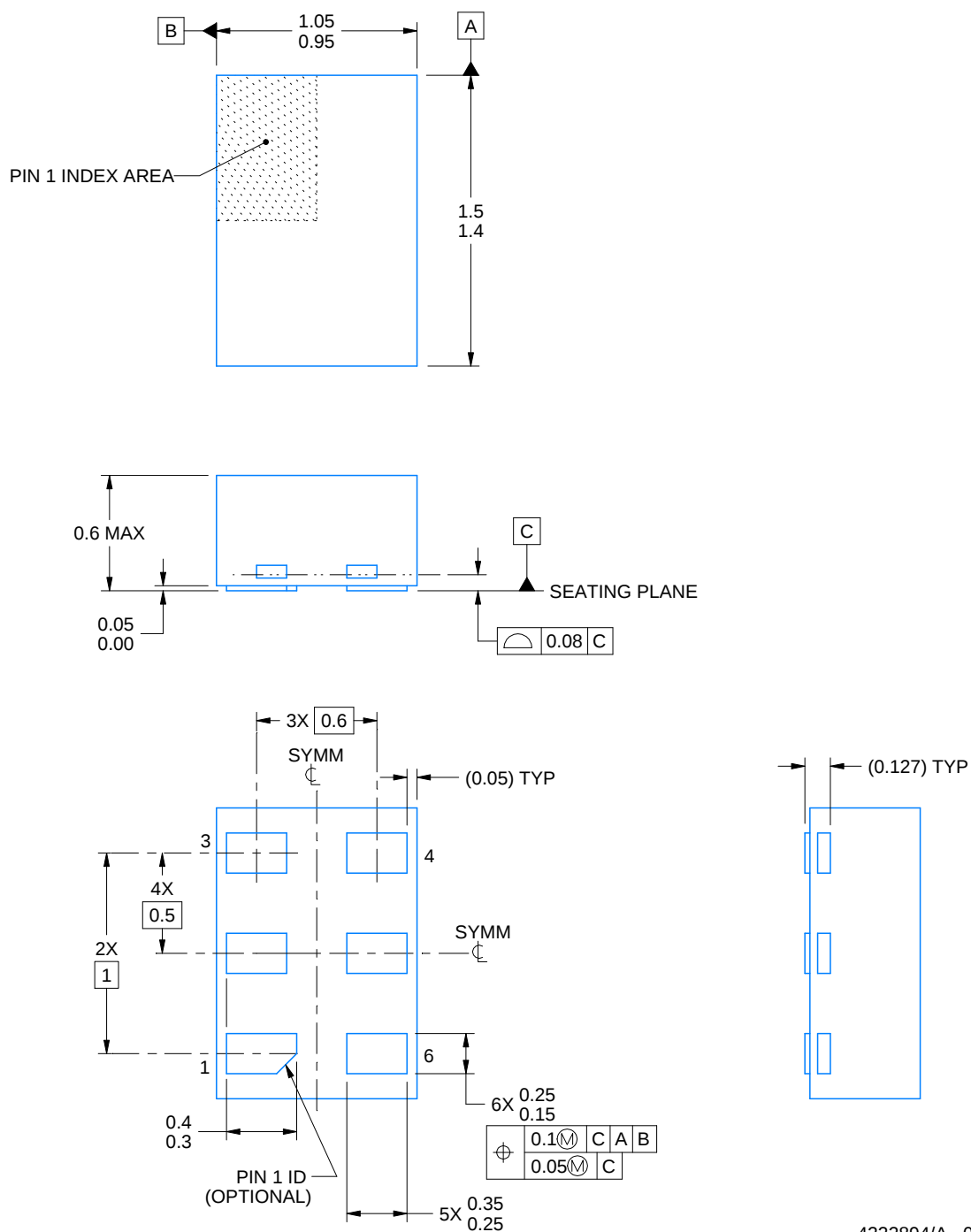
4207181/G



PACKAGE OUTLINE

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4222894/A 01/2018

NOTES:

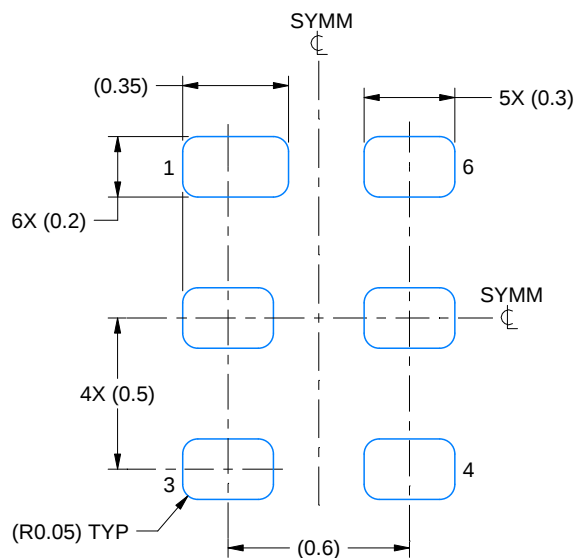
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

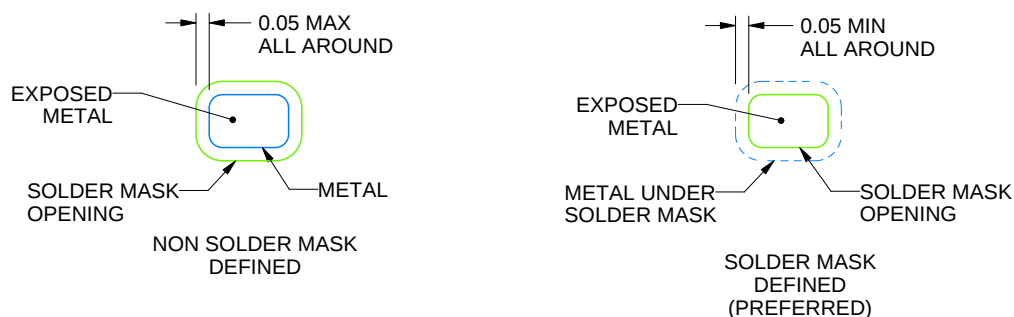
DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

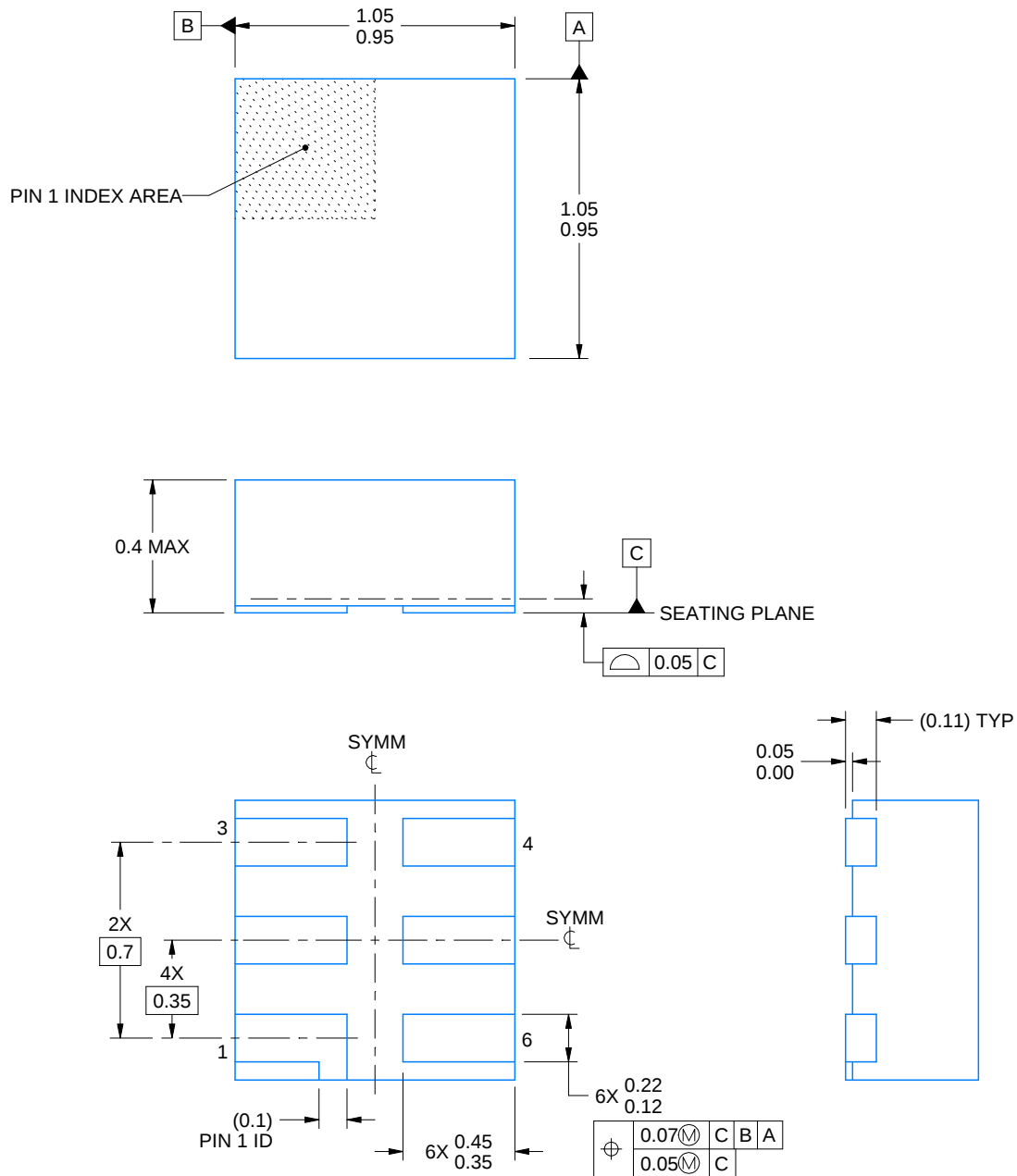


DSF0006A

PACKAGE OUTLINE

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220597/B 06/2022

NOTES:

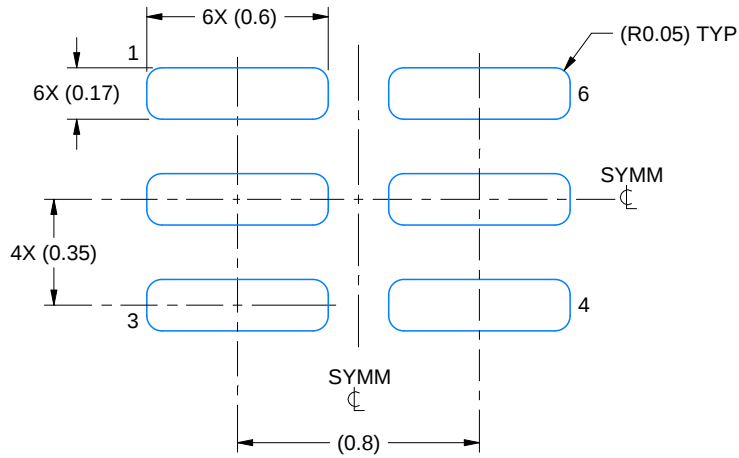
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

EXAMPLE BOARD LAYOUT

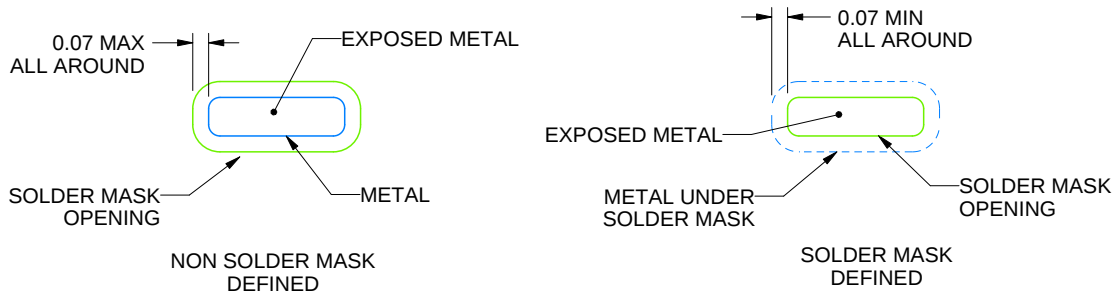
DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

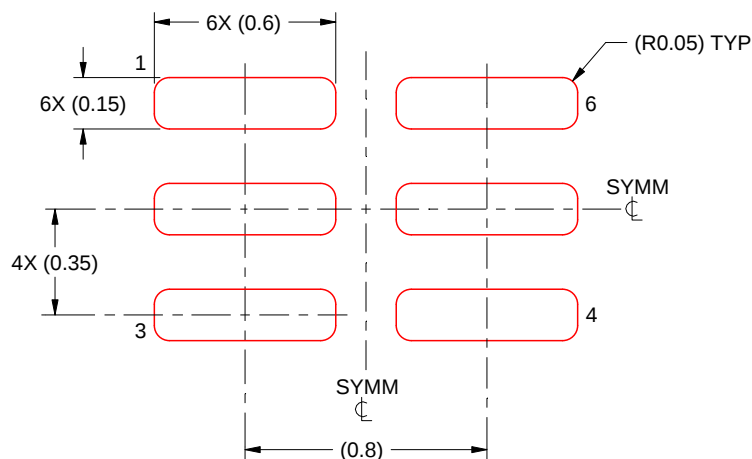
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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