SN74AVC2T45 構成可能なレベル シフトおよび変換機能搭載、2 ビット、デュアル電源、バス トランシーバ

1 特長

- テキサス・インスツルメンツの NanoFree™ パッケージで提供
- V_{CC} 絶縁機能:どちらかの V_{CC} 入力が GND レベルになると、両方のポートがハイ インピーダンス状態になる
- デュアル電源レール設計
- 4.6V 過電圧入力トレラントの I/O
- I_{off} により部分的パワーダウン モード動作をサポート
- 最大データ速度
  - 500Mbps (1.8V～3.3V)
  - 320Mbps (1.8V 未満から 3.3V にレベルシフト)
  - 320Mbps (2.5V または 1.8V にレベルシフト)
  - 280Mbps (1.5V にレベルシフト)
  - 240Mbps (1.2V にレベルシフト)
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を超える ESD 保護

2 アプリケーション

- スマートフォン
- サーバー
- デスクトップ PC とノートパソコン
- その他の携帯機器

3 概要

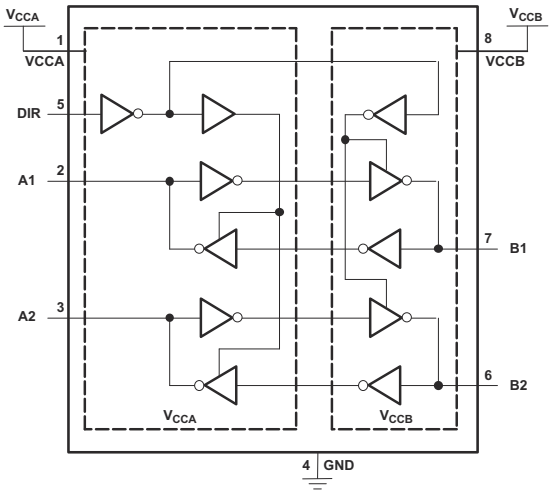
この 2 ビット非反転バス トランシーバは、設定可能な 2 本の独立した電源レールを使用します。A ポートは V_{CCA} (1.2V～3.6V の任意の電源電圧を入力できます) に追従するように設計されています。B ポートは V_{CCB} (1.2V～3.6V の任意の電源電圧を入力できます) に追従するように設計されています。これにより、1.2V、1.5V、1.8V、2.5V、3.3V の任意の電圧ノード間での自在な低電圧双方向変換およびレベルシフトが可能です。

SN74AVC2T45 は、データ バス間の非同期通信用に設計されています。方向制御 (DIR ピン) 入力のロジック レベルにより、B ポート出力と A ポート出力のどちらかがアクティブになります。本デバイスは、B ポート出力をアクティブにした場合、A バスから B バスにデータを送信し、A ポート出力をアクティブにした場合、B バスから A バスにデータを送信します。A ポートと B ポートの入力回路はどちらも常にアクティブであるため、内部 CMOS 構造にリーク電流が流れすぎないように、論理 High または Low レベルを印加する必要があります。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
SN74AVC2T45DCT	DCT (SSOP、8)	2.95mm × 2.80mm
SN74AVC2T45DCU	DCU (VSSOP、8)	2.30mm × 2.00mm
SN74AVC2T45YZP	YZP (DSBGA、8)	1.89mm × 0.89mm
SN74AVC2T45DDF	DDF (SOT-23、8)	2.90mm × 1.60mm

(1) 供給されているすべてのパッケージについては、セクション 11 を参照してください。



A. ピン番号は DCT および DCU パッケージのみのものです。

論理図 (正論理)

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

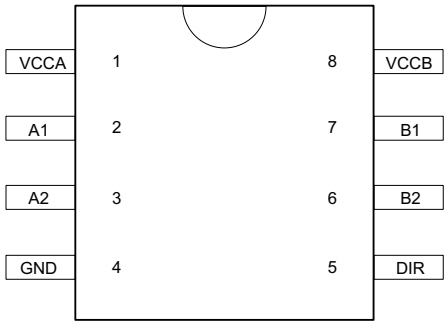


図 4-1. DCT or DCU Package 8-Pin SM8 or VSSOP Top View

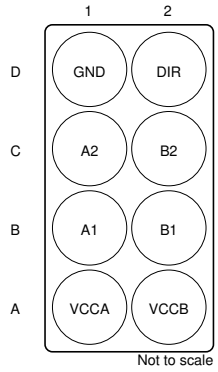


図 4-2. YZP Package 8-Pin DSBGA Bottom View

Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	NO. (SM8, VSSOP)	NO. (DSBGA)		
VCCA	1	A1	—	Supply Voltage A
VCCB	8	A2	—	Supply Voltage B
GND	4	D1	—	Ground
A1	2	B1	I/O	Output or input depending on state of DIR. Output level depends on V_{CCA}.
A2	3	C1	I/O	Output or input depending on state of DIR. Output level depends on V_{CCA}.
B1	7	B2	I/O	Output or input depending on state of DIR. Output level depends on V_{CCB}.
B2	6	C2	I/O	Output or input depending on state of DIR. Output level depends on V_{CCB}.
DIR	5	D2	I	Direction Pin, Connect to GND or to VCCA

(1) I = Input; O = Output; I/O = Input or Output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage		–0.5	4.6	V
V_I	Input voltage(2)	IO ports (A port)	–0.5	4.6	V
		IO ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through VCCA, VCCB, or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input negative-voltage and output voltage ratings can be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating can be exceeded up to 4.6 V maximum if the output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine Model (MM), Per JEDEC specification JESD22-A115-A	±200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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5.3 Recommended Operating Conditions

See(3) (4) (5)

			V_{CCI} (1)	V_{CCO} (2)	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs(4)	1.2V to 1.95V		V_{CCI} (1) × 0.65		V
			1.95V to 2.7V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs(4)	1.2V to 1.95V			V_{CCI} (1) × 0.35	V
			1.95V to 2.7V			0.7	
			2.7V to 3.6V			0.8	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})(5)	1.2V to 1.95V		V_{CCA} × 0.65		V
			1.95V to 2.7V		1.6		
			2.7V to 3.6V		2		
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})(5)	1.2V to 1.95V			V_{CCA} × 0.35	V
			1.95V to 2.7V			0.7	
			2.7V to 3.6V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO} (2)	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.2V		–3	mA
				1.4V to 1.6V		–6	
				1.65V to 1.95V		–8	
				2.3V to 2.7V		–9	
				3V to 3.6V		–12	
I_{OL}	Low-level output current			1.2V		3	mA
				1.4V to 1.6V		6	
				1.65V to 1.95V		8	
				2.3V to 2.7V		9	
				3V to 3.6V		12	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the voltage associated with the input port supply VCCA or VCCB.
(2) V_{CCO} is the voltage associated with the output port supply VCCA or VCCB.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to provide proper device operation. See *Implications of Slow or Floating CMOS Inputs*.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7V, V_{IL} max = V_{CCI} × 0.3V.
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7V, V_{IL} max = V_{CCA} × 0.3V.

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5.4 Thermal Information

THERMAL METRIC (1)		SN74AVC2T45				UNIT
		DCT (SM8)	DCU (VSSOP)	DDF (SOT-23)	YZP (DSBGA)	
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	183.1	246.9	203.2	105.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	101.5	95.2	121.5	1.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	111.0	158.4	99.8	10.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.6	34.1	21.4	3.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	109.2	157.5	99.5	10.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to +85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
V_{OH} (3)		I_{OH} = –100µA	$V_I = V_{IH}$	1.2V to 3.6V	1.2V to 3.6V				V_{CCO} – 0.2V		V
		I_{OH} = –3mA		1.2V	1.2V		0.95				
		I_{OH} = –6mA		1.4V	1.4V				1.05		
		I_{OH} = –8mA		1.65V	1.65V				1.2		
		I_{OH} = –9mA		2.3V	2.3V				1.75		
		I_{OH} = –12mA		3V	3V				2.3		
V_{OL} (3)		I_{OL} = 100µA	$V_I = V_{IL}$	1.2V to 3.6V	1.2V to 3.6V					0.2	V
		I_{OL} = 3mA		1.2V	1.2V		0.25				
		I_{OL} = 6mA		1.4V	1.4V					0.35	
		I_{OL} = 8mA		1.65V	1.65V					0.45	
		I_{OL} = 9mA		2.3V	2.3V					0.55	
		I_{OL} = 12mA		3V	3V					0.7	
I_I	DIR	$V_I = V_{CCA}$ or GND		1.2V to 3.6V	1.2V to 3.6V		±0.025	±0.25		±1	µA
I_{off}	A port	V_I or V_O = 0 to 3.6V		0V	0 to 3.6 V		±0.1	±1		±5	µA
	B port			0 to 3.6V	0V		±0.1	±1		±5	
I_{OZ} (3)	B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND		0V	3.6V		±0.5	±2.5		±5	µA
	A port			3.6V	0V		±0.5	±2.5		±5	
I_{CCA} (3)		$V_I = V_{CCI}$ or GND, I_O = 0		1.2V to 3.6V	1.2V to 3.6V					10	µA
				0V	3.6V					–2	
				3.6V	0V					10	
I_{CCB} (3)		$V_I = V_{CCI}$ or GND, I_O = 0		1.2V to 3.6V	1.2V to 3.6V					10	µA
				0V	3.6V					10	
				3.6V	0V					–2	
I_{CCA} + I_{CCB} (see 表 5-1)		$V_I = V_{CCI}$ or GND, I_O = 0		1.2V to 3.6V	1.2V to 3.6V					20	µA
C_I	Control inputs	V_I = 3.3V or GND		3.3V	3.3V		2.5				pF
C_{io}	A or B port	V_O = 3.3V or GND		3.3V	3.3V		6				pF

(1) V_{CCO} is the voltage associated with the output port supply VCCA or VCCB.
(2) V_{CCI} is the voltage associated with the input port supply VCCA or VCCB.
(3) V_{OH}: Output High Voltage; V_{OL}: Output Low Voltage; I_{OZ}: Hi-Z Output Current; I_{CCA}: Supply A Current; I_{CCB}: Supply B Current

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5.6 Switching Characteristics: V_{CCA} = 1.2V

over recommended operating free-air temperature range, V_{CCA} = 1.2V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2V	V_{CCB} = 1.5V	V_{CCB} = 1.8V	V_{CCB} = 2.5V	V_{CCB} = 3.3V	UNIT
			TYP	TYP	TYP	TYP	TYP	
t_{PLH} (2)	A	B	3.1	2.6	2.4	2.2	2.2	ns
t_{PHL} (2)			3.1	2.6	2.4	2.2	2.2	
t_{PLH} (2)	B	A	3.4	3.1	3	2.9	2.9	ns
t_{PHL} (2)			3.4	3.1	3	2.9	2.9	
t_{PHZ} (2)	DIR	A	5.2	5.2	5.1	5	4.8	ns
t_{PLZ} (2)			5.2	5.2	5.1	5	4.8	
t_{PHZ} (2)	DIR	B	5	4	3.8	2.8	3.2	ns
t_{PLZ} (2)			5	4	3.8	2.8	3.2	
t_{PZH} (2) (1)	DIR	A	8.4	7.1	6.8	5.7	6.1	ns
t_{PZL} (2) (1)			8.4	7.1	6.8	5.7	6.1	
t_{PZH} (2) (1)	DIR	B	8.3	7.8	7.5	7.2	7	ns
t_{PZL} (2) (1)			8.3	7.8	7.5	7.2	7	

(1) The enable time is a calculated value, derived using the formula shown in the *セクション 8.2.2.2.1* section.
(2) t_{PLH}: Low-to-high Propagation Delay; t_{PHL}: High-to-Low Propagation Delay; t_{PHZ}: High-to-Hi-Z Propagation Delay; t_{PLZ}: Low-to-Hi-Z Propagation Delay; t_{PZH}: Hi-Z-to-High Propagation Delay; t_{PZL}: Hi-Z-to-Low Propagation Delay

5.7 Switching Characteristics: V_{CCA} = 1.5V ±0.1V

over recommended operating free-air temperature range, V_{CCA} = 1.5V ± 0.1V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2V	V_{CCB} = 1.5V ± 0.1V		V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} (2)	A	B	2.8	0.7	5.4	0.5	4.6	0.4	3.7	0.3	3.5	ns
t_{PHL} (2)			2.8	0.7	5.4	0.5	4.6	0.4	3.7	0.3	3.5	
t_{PLH} (2)	B	A	2.7	0.8	5.4	0.7	5.2	0.6	4.9	0.5	4.7	ns
t_{PHL} (2)			2.7	0.8	5.4	0.7	5.2	0.6	4.9	0.5	4.7	
t_{PHZ} (2)	DIR	A	3.9	1.3	8.5	1.3	7.8	1.1	7.7	1.4	7.6	ns
t_{PLZ} (2)			3.9	1.3	8.5	1.3	7.8	1.1	7.7	1.4	7.6	
t_{PHZ} (2)	DIR	B	4.7	1.1	7	1.4	6.9	1.2	6.9	1.7	7.1	ns
t_{PLZ} (2)			4.7	1.1	7	1.4	6.9	1.2	6.9	1.7	7.1	
t_{PZH} (2) (1)	DIR	A	7.4		12.4		12.1		11.8		11.8	ns
t_{PZL} (2) (1)			7.4		12.4		12.1		11.8		11.8	
t_{PZH} (2) (1)	DIR	B	6.7		13.9		12.4		11.4		11.1	ns
t_{PZL} (2) (1)			6.7		13.9		12.4		11.4		11.1	

(1) The enable time is a calculated value, derived using the formula shown in the *セクション 8.2.2.2.1* section.
(2) t_{PLH}: Low-to-high Propagation Delay; t_{PHL}: High-to-Low Propagation Delay; t_{PHZ}: High-to-Hi-Z Propagation Delay; t_{PLZ}: Low-to-Hi-Z Propagation Delay; t_{PZH}: Hi-Z-to-High Propagation Delay; t_{PZL}: Hi-Z-to-Low Propagation Delay

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5.8 Switching Characteristics: V_{CCA} = 1.8V ±0.15V

over recommended operating free-air temperature range, V_{CCA} = 1.8V ± 0.15V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2V	V_{CCB} = 1.5V ± 0.1V		V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} (2)	A	B	2.7	0.5	5.2	0.4	4.3	0.2	3.4	0.2	3.1	ns
t_{PHL} (2)			2.7	0.5	5.2	0.4	4.3	0.2	3.4	0.2	3.1	
t_{PLH} (2)	B	A	2.4	0.7	4.7	0.5	4.4	0.5	4	0.4	3.8	ns
t_{PHL} (2)			2.4	0.7	4.7	0.5	4.4	0.5	4	0.4	3.8	
t_{PHZ} (2)	DIR	A	3.7	1.3	8.1	0.7	6.9	1.4	5.3	1.1	5.2	ns
t_{PLZ} (2)			3.7	1.3	8.1	0.7	6.9	1.4	5.3	1.1	5.2	
t_{PHZ} (2)	DIR	B	4.4	1.3	5.8	1.3	5.9	0.8	5.7	1.5	5.9	ns
t_{PLZ} (2)			4.4	1.3	5.8	1.3	5.9	0.8	5.7	1.5	5.9	
t_{PZH} (2) (1)	DIR	A	6.8		10.5		10.3		9.7		9.7	ns
t_{PZL} (2) (1)			6.8		10.5		10.3		9.7		9.7	
t_{PZH} (2) (1)	DIR	B	6.4		13.3		11.2		8.7		8.3	ns
t_{PZL} (2) (1)			6.4		13.3		11.2		8.7		8.3	

(1) The enable time is a calculated value, derived using the formula shown in the *セクション 8.2.2.2.1* section.
(2) t_{PLH}: Low-to-high Propagation Delay; t_{PHL}: High-to-Low Propagation Delay; t_{PHZ}: High-to-Hi-Z Propagation Delay; t_{PLZ}: Low-to-Hi-Z Propagation Delay; t_{PZH}: Hi-Z-to-High Propagation Delay; t_{PZL}: Hi-Z-to-Low Propagation Delay

5.9 Switching Characteristics: V_{CCA} = 2.5V ±0.2V

over recommended operating free-air temperature range, V_{CCA} = 2.5V ± 0.2V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2V	V_{CCB} = 1.5V ± 0.1V		V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} (2)	A	B	2.6	0.4	4.9	0.2	4	0.2	3	0.2	2.6	ns
t_{PHL} (2)			2.6	0.4	4.9	0.2	4	0.2	3	0.2	2.6	
t_{PLH} (2)	B	A	2.1	0.6	3.8	0.5	3.4	0.4	3	0.3	2.8	ns
t_{PHL} (2)			2.1	0.6	3.8	0.5	3.4	0.4	3	0.3	2.8	
t_{PHZ} (2)	DIR	A	2.4	0.7	7.9	0.8	6.4	0.8	5	0.5	4.3	ns
t_{PLZ} (2)			2.4	0.7	7.9	0.8	6.4	0.8	5	0.5	4.3	
t_{PHZ} (2)	DIR	B	3.8	1	4.3	0.6	4.3	0.5	4.2	1.1	4.1	ns
t_{PLZ} (2)			3.8	1	4.3	0.6	4.3	0.5	4.2	1.1	4.1	
t_{PZH} (2) (1)	DIR	A	5.9		8.5		7.7		7.2		6.9	ns
t_{PZL} (2) (1)			5.9		8.5		7.7		7.2		6.9	
t_{PZH} (2) (1)	DIR	B	5		12.8		10.4		8		6.9	ns
t_{PZL} (2) (1)			5		12.8		10.4		8		6.9	

(1) The enable time is a calculated value, derived using the formula shown in the *セクション 8.2.2.2.1* section.
(2) t_{PLH}: Low-to-high Propagation Delay; t_{PHL}: High-to-Low Propagation Delay; t_{PHZ}: High-to-Hi-Z Propagation Delay; t_{PLZ}: Low-to-Hi-Z Propagation Delay; t_{PZH}: Hi-Z-to-High Propagation Delay; t_{PZL}: Hi-Z-to-Low Propagation Delay

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5.10 Switching Characteristics: V_{CCA} = 3.3V ±0.3V

over recommended operating free-air temperature range, V_{CCA} = 3.3V ± 0.3V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2V	V_{CCB} = 1.5V ± 0.1V		V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} (2)	A	B	2.5	0.3	4.7	0.2	3.8	0.2	2.8	0.2	2.4	ns
t_{PHL} (2)			2.5	0.3	4.7	0.2	3.8	0.2	2.8	0.2	2.4	
t_{PLH} (2)	B	A	2.1	0.6	3.6	0.4	3.1	0.3	2.6	0.3	2.4	ns
t_{PHL} (2)			2.1	0.6	3.6	0.4	3.1	0.3	2.6	0.3	2.4	
t_{PHZ} (2)	DIR	A	2.9	1.1	8	1	6.5	1.3	4.7	1.2	4	ns
t_{PLZ} (2)			2.9	1.1	8	1	6.5	1.3	4.7	1.2	4	
t_{PHZ} (2)	DIR	B	3.4	0.5	6.6	0.3	5.6	0.3	4.6	1.1	4.2	ns
t_{PLZ} (2)			3.4	0.5	6.6	0.3	5.6	0.3	4.6	1.1	4.2	
t_{PZH} (2) (1)	DIR	A	5.5		10.2		8.7		7.2		6.6	ns
t_{PZL} (2) (1)			5.5		10.2		8.7		7.2		6.6	
t_{PZH} (2) (1)	DIR	B	5.4		12.7		10.3		7.5		6.4	ns
t_{PZL} (2) (1)			5.4		12.7		10.3		7.5		6.4	

(1) The enable time is a calculated value, derived using the formula shown in the section.
(2) t_{PLH}: Low-to-high Propagation Delay; t_{PHL}: High-to-Low Propagation Delay; t_{PHZ}: High-to-Hi-Z Propagation Delay; t_{PLZ}: Low-to-Hi-Z Propagation Delay; t_{PZH}: Hi-Z-to-High Propagation Delay; t_{PZL}: Hi-Z-to-Low Propagation Delay

5.11 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.2V	V_{CCA} = V_{CCB} = 1.5V	V_{CCA} = V_{CCB} = 1.8V	V_{CCA} = V_{CCB} = 2.5V	V_{CCA} = V_{CCB} = 3.3V	UNIT
			TYP	TYP	TYP	TYP	TYP	
C_{pdA} (1)	A-port input, B-port output	C_L = 0, f = 10MHz, t_r (2) = t_f (2) = 1ns	3	3	3	3	4	pF
	B-port input, A-port output		12	13	13	14	15	
C_{pdB} (1)	A-port input, B-port output	C_L = 0, f = 10MHz, t_r (2) = t_f (2) = 1ns	12	13	13	14	15	pF
	B-port input, A-port output		3	3	3	3	4	

(1) Power-dissipation capacitance per transceiver
(2) t_r: Rise time; t_f: Fall time

5.12 Typical Characteristics

表 5-1. Typical Total Static Power Consumption (I_{CCA} + I_{CCB})

V_{CCB}	V_{CCA}						UNIT
	0V	1.2V	1.5V	1.8V	2.5V	3.3V	
0V	0	<0.5	<0.5	<0.5	<0.5	<0.5	μA
1.2V	<0.5	<1	<1	<1	<1	1	
1.5V	<0.5	<1	<1	<1	<1	1	
1.8V	<0.5	<1	<1	<1	<1	<1	
2.5V	<0.5	1	<1	<1	<1	<1	
3.3V	<0.5	1	<1	<1	<1	<1	

5.12.1 Typical Propagation Delay (A to B) vs Load Capacitance, T_A = 25°C, V_{CCA} = 1.2V

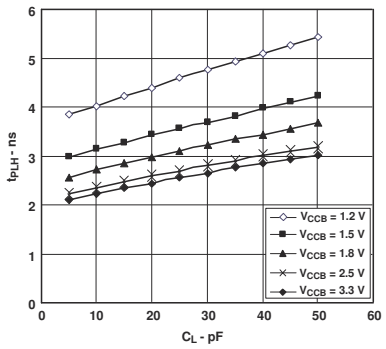


図 5-1. Typical A-to-B Propagation Delay, Low to High

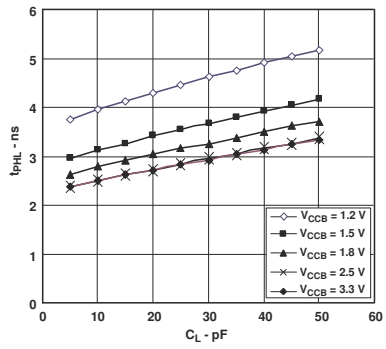


図 5-2. Typical A-to-B Propagation Delay, High to Low

5.12.2 Typical Propagation Delay (A to B) vs Load Capacitance, T_A = 25°C, V_{CCA} = 1.5V

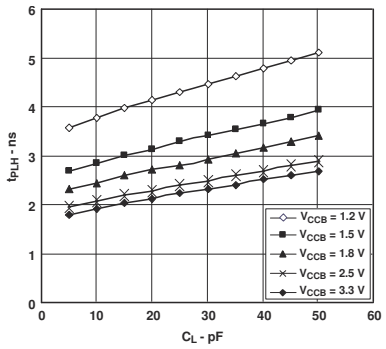


図 5-3. Typical A-to-B Propagation Delay, Low to High

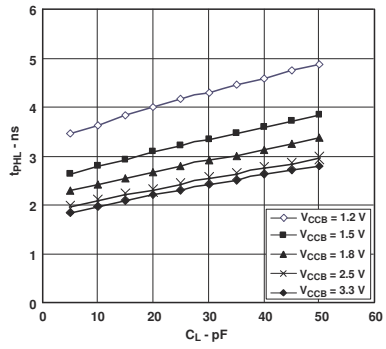


図 5-4. Typical A-to-B Propagation Delay, High to Low

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5.12.3 Typical Propagation Delay (A-to-B) vs Load Capacitance, T_A = 25°C, V_{CCA} = 1.8V

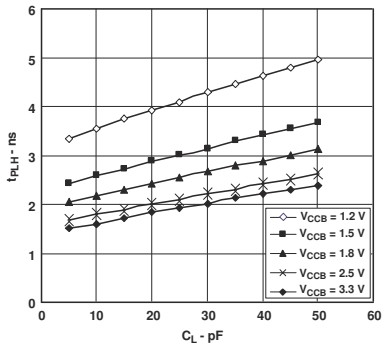


図 5-5. Typical A-to-B Propagation Delay, Low to High

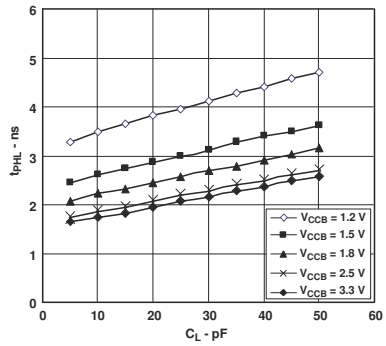


図 5-6. Typical A-to-B Propagation Delay, High to Low

5.12.4 Typical Propagation Delay (A to B) vs Load Capacitance, T_A = 25°C, V_{CCA} = 2.5V

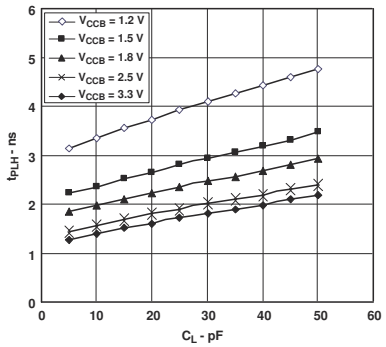


図 5-7. Typical A-to-B Propagation Delay, Low to High

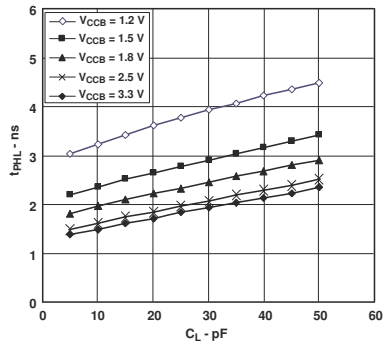


図 5-8. Typical A-to-B Propagation Delay, High to Low

5.12.5 Typical Propagation Delay (A to B) vs Load Capacitance, T_A = 25°C, V_{CCA} = 3.3V

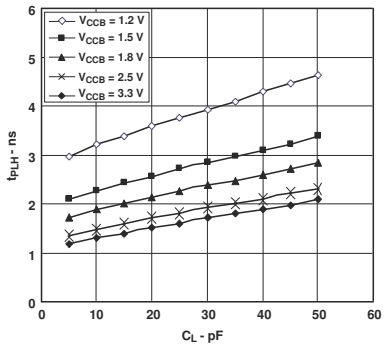


図 5-9. Typical A-to-B Propagation Delay, Low to High

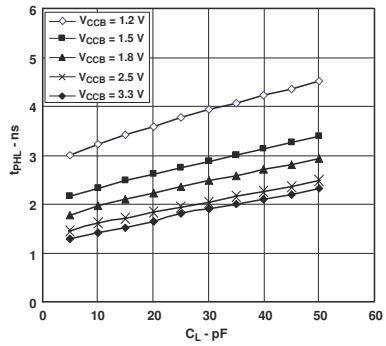
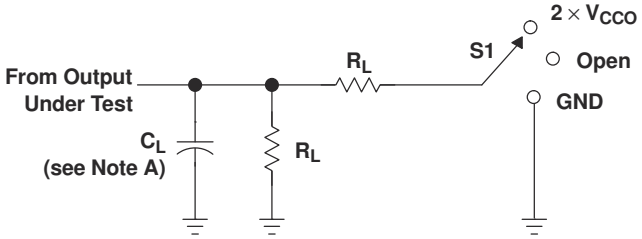


図 5-10. Typical A-to-B Propagation Delay, High to Low

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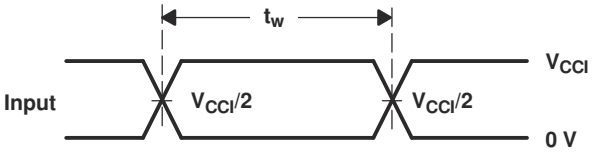
6 Parameter Measurement Information



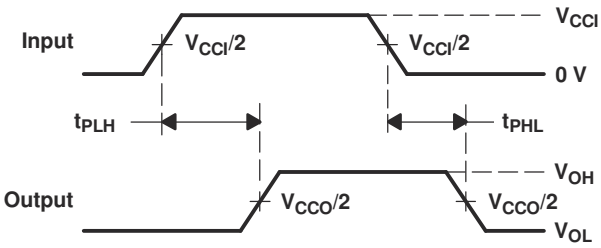
LOAD CIRCUIT

TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open $2 \times V_{CCO}$ GND

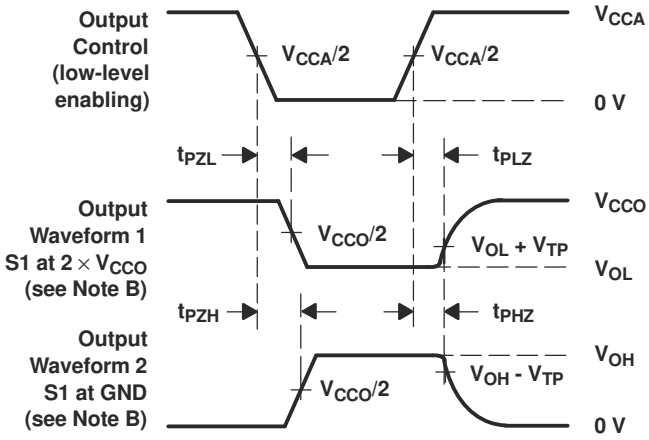
V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.

図 6-1. Load Circuit and Voltage Waveforms

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7 Detailed Description

7.1 Overview

This dual-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA} and accepts any supply voltage from 1.2V to 3.6V. The B port is designed to track V_{CCB} and accepts any supply voltage from 1.2V to 3.6V. This allows for universal low-voltage bidirectional translation and level-shifting between any of the 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V voltage nodes.

The device is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess internal leakage of the CMOS.

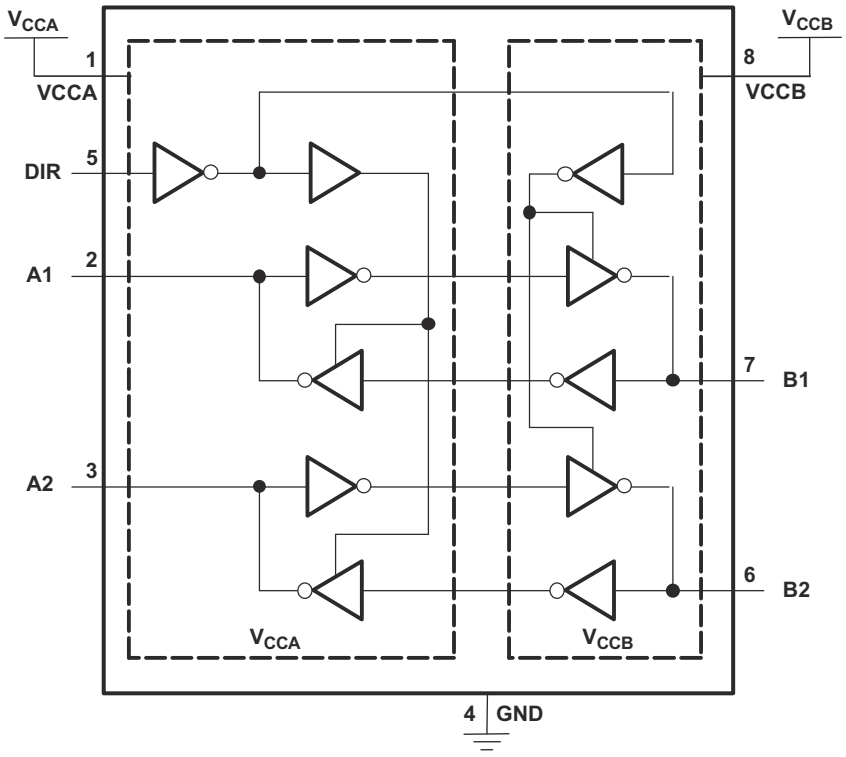
The device is designed so that the DIR input is powered by supply voltage from VCCA.

This device is fully specified for partial-power-down applications using off output current (I_{off}). The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when powered down.

The V_{CC} isolation feature makes sure that if either VCC input is at GND, both ports are put in a high-impedance state. This action prevents a false high or low logic being presented at the output.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

7.2 Functional Block Diagram



Pin numbers are for the DCT and DCU packages only.

7.3 Feature Description

7.3.1 VCC Isolation

The V_{CC} isolation feature make sure that if either V_{CCA} or V_{CCB} are at GND, both ports are in a high-impedance state (I_{OZ} shown in *Electrical Characteristics*). This action prevents false logic levels from being presented to either bus.

7.3.2 2-Rail Design

Fully configurable 2-rail design allows each port to operate over the full 1.2V to 3.6V power-supply range.

7.3.3 IO Ports are 4.6-V Tolerant

The IO ports are up to 4.6 V tolerant.

7.3.4 Partial-Power-Down Mode

This device is fully specified for partial-power-down applications using off output current (I_{off}). The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when the device is powered down.

7.4 Device Functional Modes

表 7-1 shows the functional modes of the SN74AVC2T45-Q1.

表 7-1. Function Table
(Each Transceiver)

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SN74AVC2T45 is used to shift IO voltage levels from one voltage domain to another. Bus A and bus B have independent power supplies, and a direction pin is used to control the direction of data flow. Unused data ports must not be floating; tie the unused port input and output to ground directly.

8.2 Typical Applications

8.2.1 Unidirectional Logic Level-Shifting Application

図 8-1 is an example circuit of the SN74AVC2T45 used in a unidirectional logic level-shifting application.

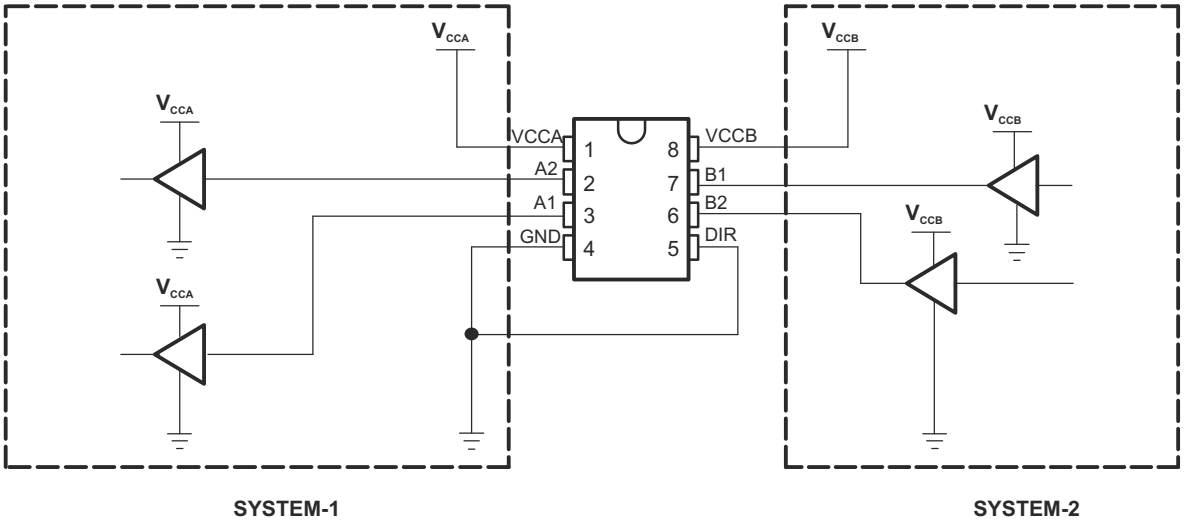


図 8-1. Unidirectional Logic Level-Shifting Application

8.2.1.1 Design Requirements

表 8-1 lists the pins and pin descriptions of the SN74AVC2T45 connections with SYSTEM-1 and SYSTEM-2.

表 8-1. SN74AVC2T45 Pin Connections With SYSTEM-1 and SYSTEM-2

PIN	NAME	DESCRIPTION
1	VCCA	SYSTEM-1 supply voltage (1.2V to 3.6V)
2	A1	Output level depends on V_{CCA}.
3	A2	Output level depends on V_{CCA}.
4	GND	Device GND
5	DIR	The GND (low-level) determines B-port to A-port direction.
6	B2	Input threshold value depends on V_{CCB}.
7	B1	Input threshold value depends on V_{CCB}.
8	VCCB	SYSTEM-2 supply voltage (1.2V to 3.6V)

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8.2.1.2 Detailed Design Procedure

This device uses drivers which are enabled depending on the state of the DIR pin. The designer must know the intended flow of data and take care not to violate any of the high or low logic levels. Unused data inputs must not be floating, as this can cause excessive internal leakage on the input CMOS structure. Make sure to tie any unused input and output ports directly to ground.

8.2.1.3 Application Curve

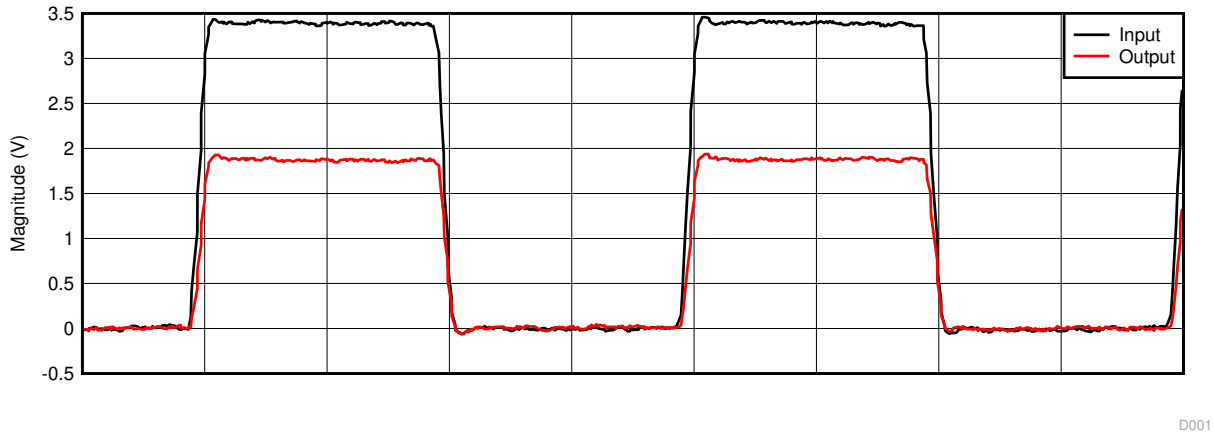


図 8-2. 3.3 V to 1.8 V Level-Shifting With 1-MHz Square Wave

8.2.2 Bidirectional Logic Level-Shifting Application

図 8-3 shows the SN74AVC2T45 used in a bidirectional logic level-shifting application.

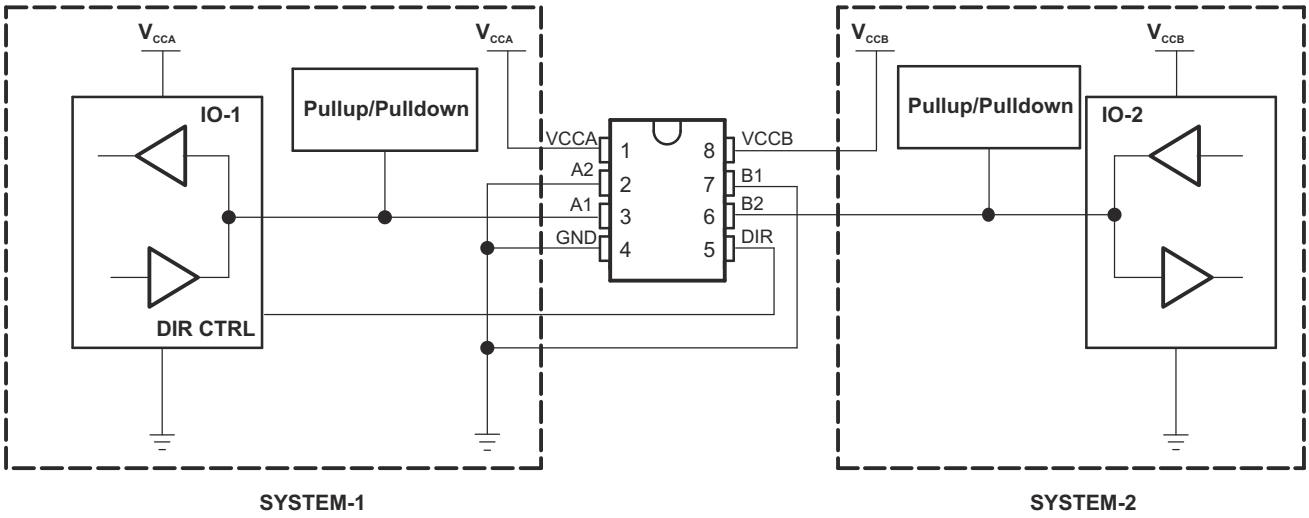


図 8-3. Bidirectional Logic Level-Shifting Application

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8.2.2.1 Design Requirements

The SN74AVC2T45 does not have an output-enable (OE) pin, the system designer must take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.

8.2.2.2 Detailed Design Procedure

表 8-2 shows a sequence that illustrates data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

表 8-2. Data Transmission Sequence

STATE	DIR CTRL	IO-1	IO-2	DESCRIPTION
1	H	Output	Input	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. IO-1 and IO-2 are disabled. The bus-line state depends on pullup or pulldown.(1)
3	L	Hi-Z	Hi-Z	DIR bit is flipped. IO-1 and IO-2 still are disabled. The bus-line state depends on pullup or pulldown.(1)
4	L	Input	Output	SYSTEM-2 data to SYSTEM-1

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, that is, both pullup or both pulldown.

8.2.2.2.1 Enable Times

Calculate the enable times for the SN74AVC2T45 using the following formulas:

- t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A)
- t_{PZL} (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A)
- t_{PZH} (DIR to B) = t_{PLZ} (DIR to A) + t_{PLH} (A to B)
- t_{PZL} (DIR to B) = t_{PHZ} (DIR to A) + t_{PHL} (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74AVC2T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting the device with an input. After the B port has been disabled, an input signal applied to the port appears on the corresponding A port after the specified propagation delay.

8.3 Power Supply Recommendations

A proper power-up sequence must always be followed to avoid excessive current on the supply pin, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

1. Connect ground before any supply voltage is applied.
2. Power up V_{CCA}.
3. V_{CCB} can be ramped up along with or after V_{CCA}.

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8.4 Layout

8.4.1 Layout Guidelines

To verify the reliability of the device, follow common printed-circuit board layout guidelines.

- Bypass capacitors can be used on power supplies. Place the capacitors as close as possible to the VCCA, VCCB pin and GND pin.
- Short trace lengths can be used to avoid excessive loading.

8.4.2 Layout Example

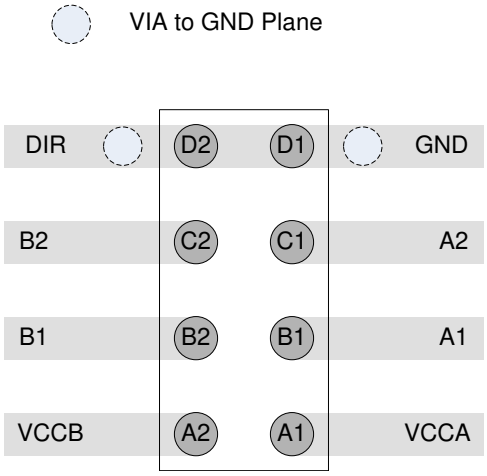


図 8-4. Layout Example for YZP Package

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9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision M (September 2024) to Revision N (February 2025)	Page
• Updated DCT and DDF *Thermal Information*	6

Changes from Revision L (May 2017) to Revision M (September 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• DDF パッケージを追加	1
• Deleted the *Community Resources* section	19
• Added the *Support Resources*, *Receiving Notification of Documentation Updates*, *Electrostatic Discharge Statement*, and *Glossary* sections	19

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Changes from Revision K (April 2015) to Revision L (May 2017)	Page
• データシートのタイトルを変更	1
• Changed YZP package pinout diagram to bottom view	3
• Added Type column to *Pin Functions* table	3
• Added Junction temperature, T_J	4

Changes from Revision J (June 2007) to Revision K (April 2015)	Page
• 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AVC2T45DCTR	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	DT2 Z
SN74AVC2T45DCTR.A	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2 Z
SN74AVC2T45DCTR.B	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2 Z
SN74AVC2T45DCTRE4	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2 Z
SN74AVC2T45DCTRG4	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DT2 Z
SN74AVC2T45DCTRG4.A	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DT2 Z
SN74AVC2T45DCTRG4.B	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DT2 Z
SN74AVC2T45DCTT	Last Time Buy	Production	SSOP (DCT) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2 Z
SN74AVC2T45DCTT.B	Last Time Buy	Production	SSOP (DCT) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2 Z
SN74AVC2T45DCUR	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(DT2R, T2) DZ
SN74AVC2T45DCUR.A	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(DT2R, T2) DZ
SN74AVC2T45DCUR.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(DT2R, T2) DZ
SN74AVC2T45DCURG4	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2R
SN74AVC2T45DCURG4.A	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2R
SN74AVC2T45DCURG4.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2R
SN74AVC2T45DCUT	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2R
SN74AVC2T45DCUT.B	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2R
SN74AVC2T45DCUTG4	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2R
SN74AVC2T45DCUTG4.B	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2R
SN74AVC2T45DDFR	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A2T45

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AVC2T45DDFR.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A2T45
SN74AVC2T45YZPR	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TDN
SN74AVC2T45YZPR.B	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TDN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74AVC2T45 :

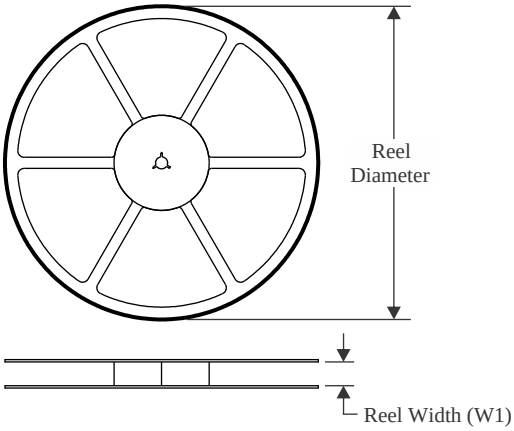
- Automotive : SN74AVC2T45-Q1

NOTE: Qualified Version Definitions:

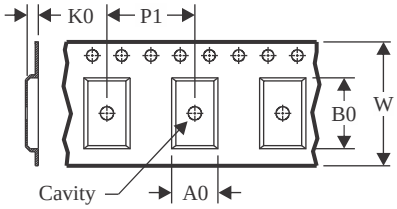
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

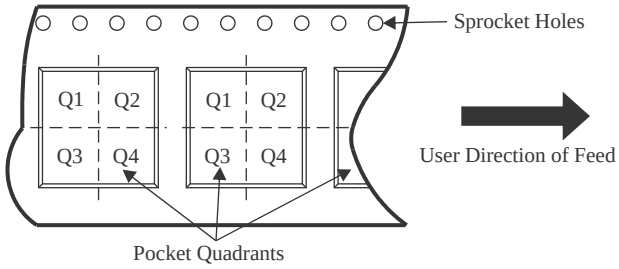


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

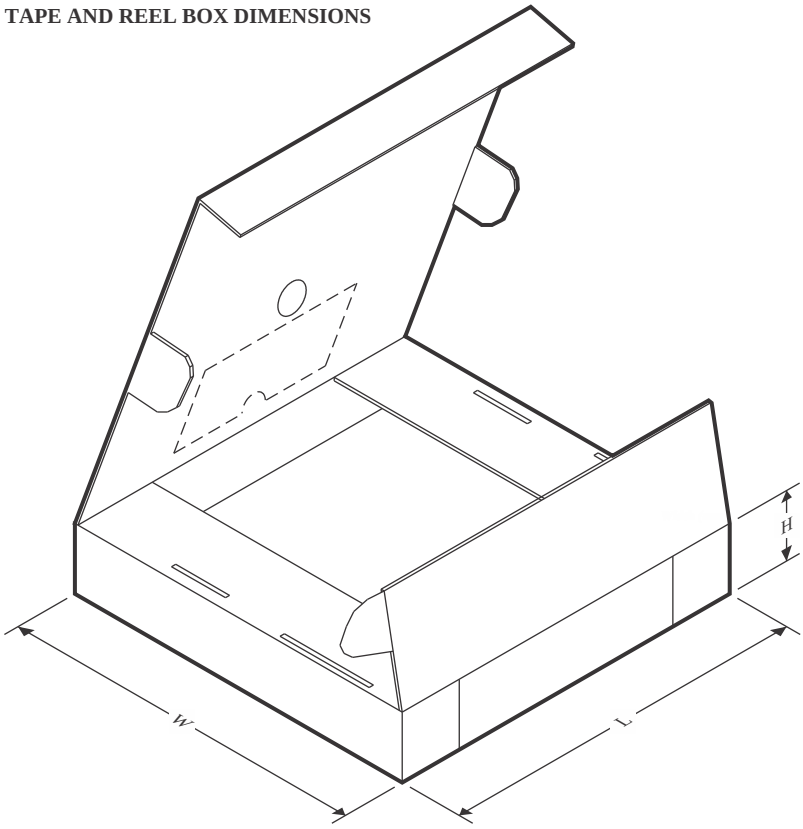
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC2T45DCTR	SSOP	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74AVC2T45DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AVC2T45DCTRG4	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AVC2T45DCTT	SSOP	DCT	8	250	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AVC2T45DCTT	SSOP	DCT	8	250	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
SN74AVC2T45DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AVC2T45DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.25	3.4	1.0	4.0	8.0	Q3
SN74AVC2T45DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74AVC2T45DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AVC2T45DCURG4	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74AVC2T45DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AVC2T45DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.1	1.25	4.0	8.0	Q3
SN74AVC2T45YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

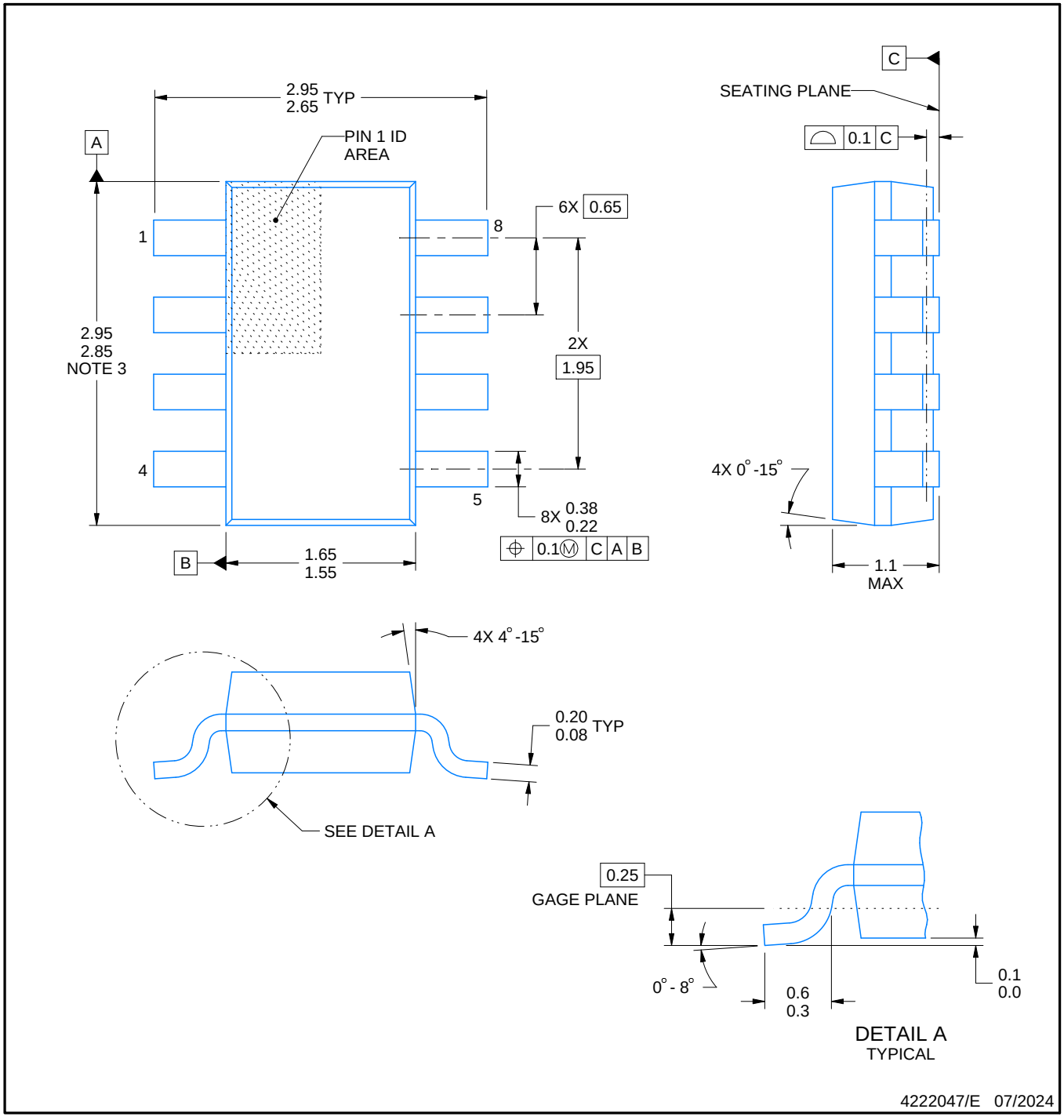
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC2T45DCTR	SSOP	DCT	8	3000	190.0	190.0	30.0
SN74AVC2T45DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
SN74AVC2T45DCTRG4	SSOP	DCT	8	3000	182.0	182.0	20.0
SN74AVC2T45DCTT	SSOP	DCT	8	250	182.0	182.0	20.0
SN74AVC2T45DCTT	SSOP	DCT	8	250	183.0	183.0	20.0
SN74AVC2T45DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AVC2T45DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0
SN74AVC2T45DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74AVC2T45DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AVC2T45DCURG4	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74AVC2T45DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74AVC2T45DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
SN74AVC2T45YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DDF0008A

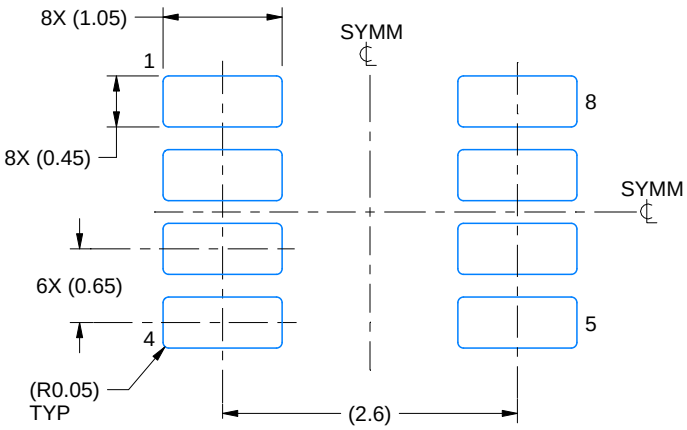
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

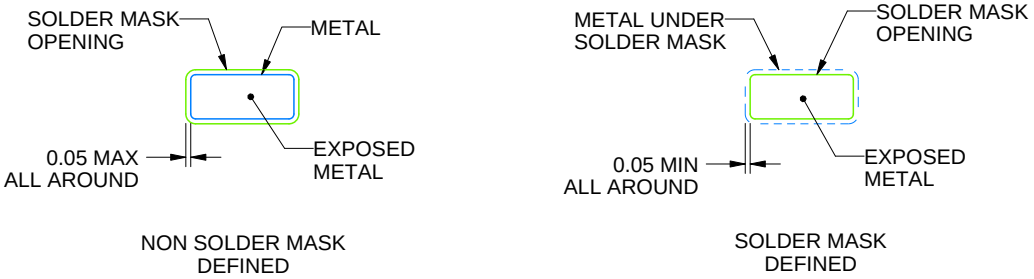


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

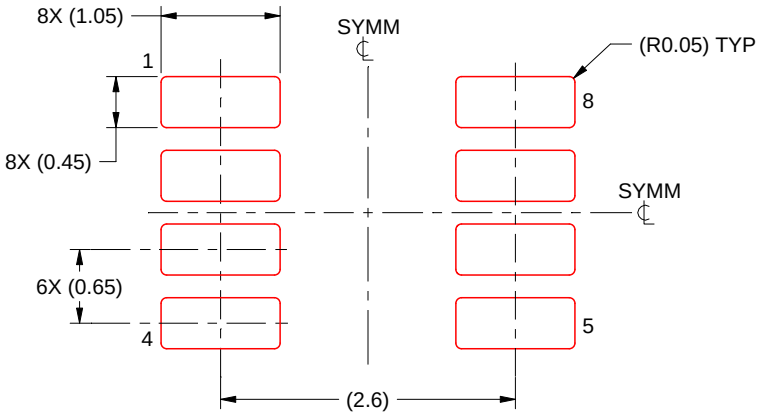
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

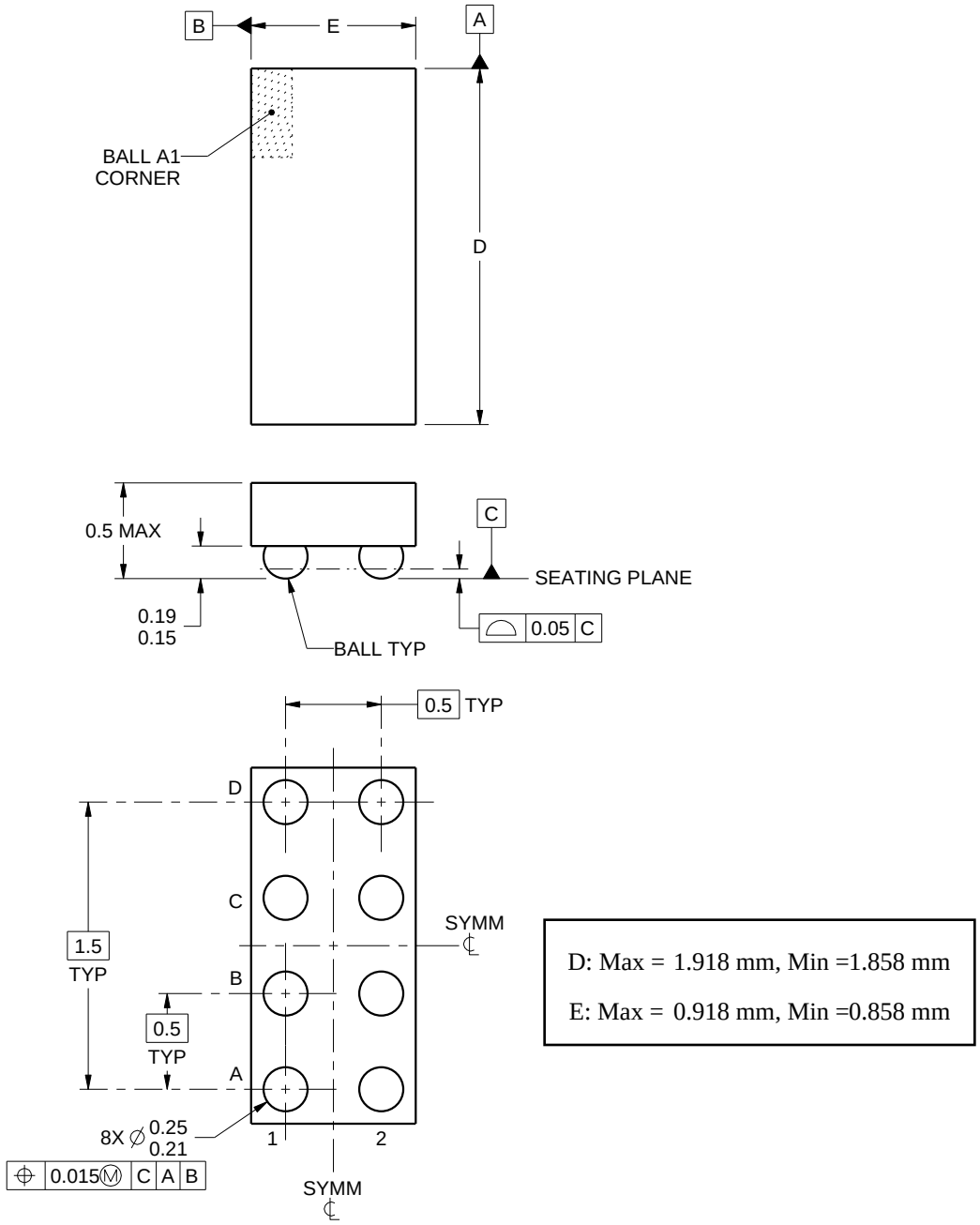
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0008

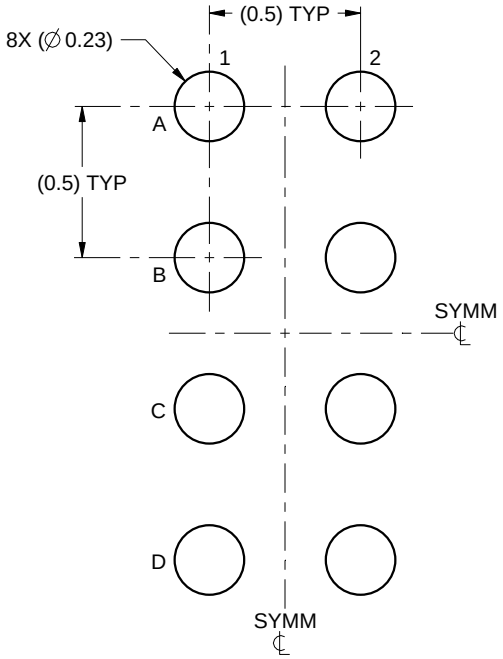
DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

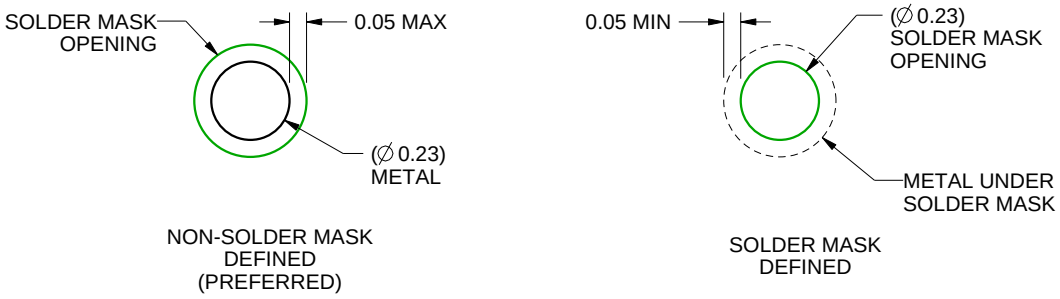


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

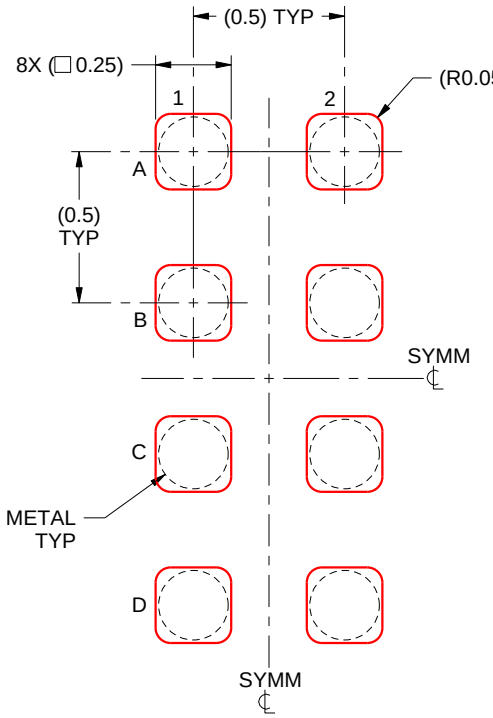


SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

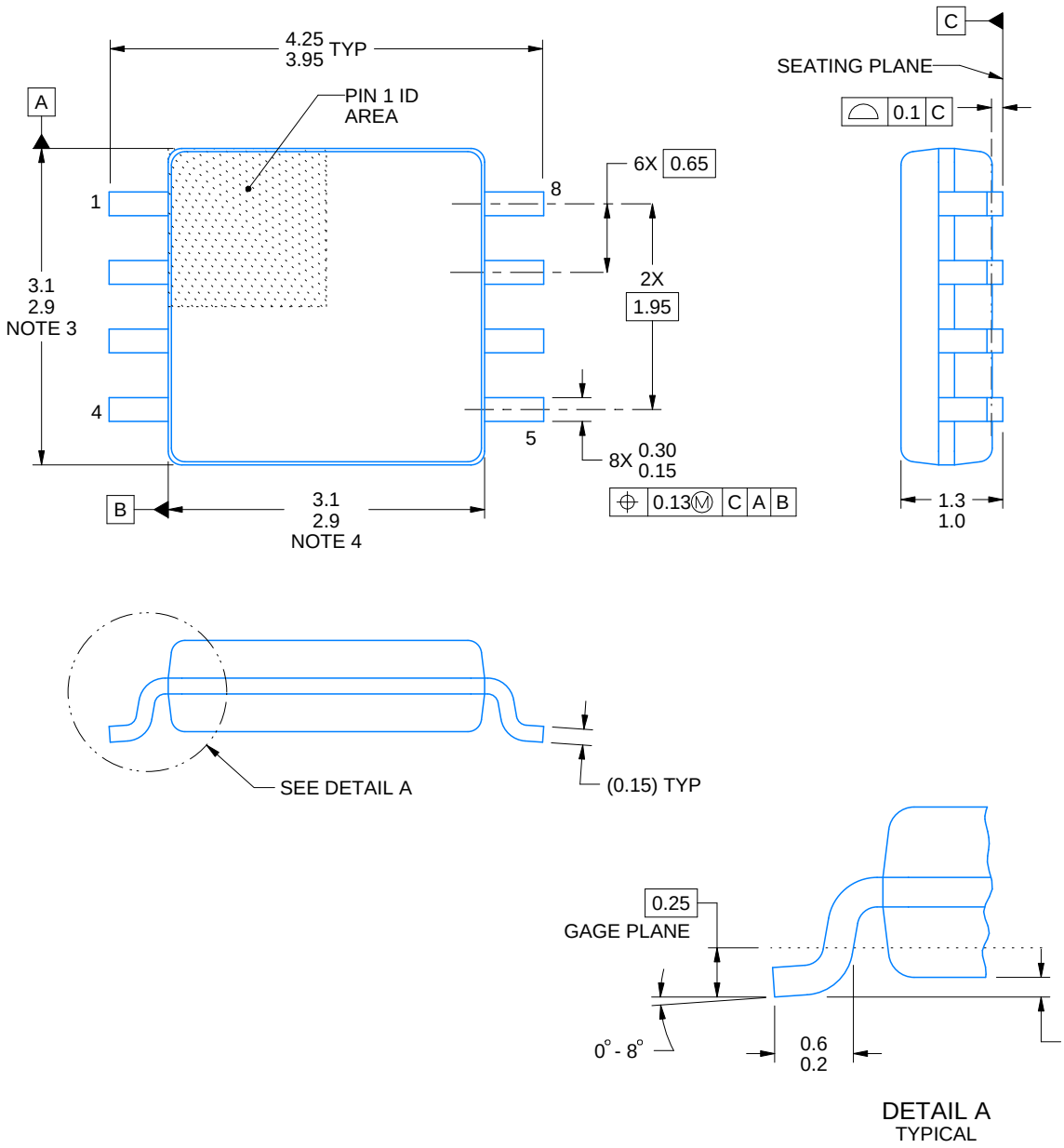
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DCT0008A

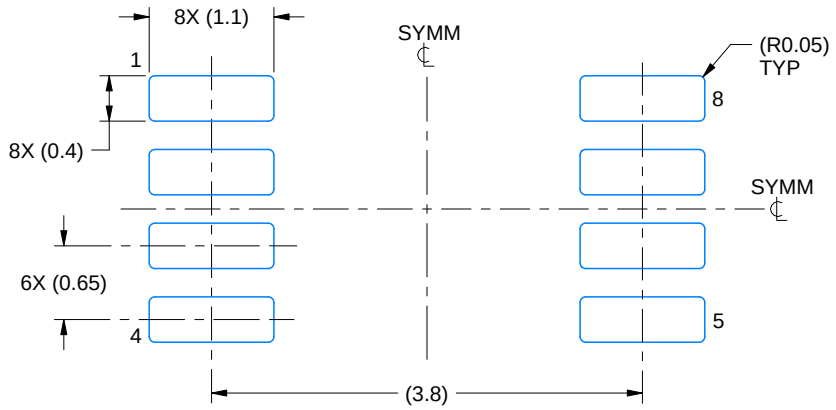
SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE

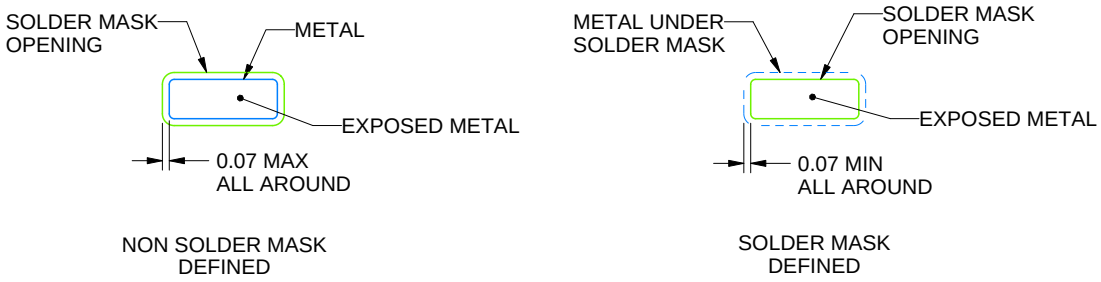


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

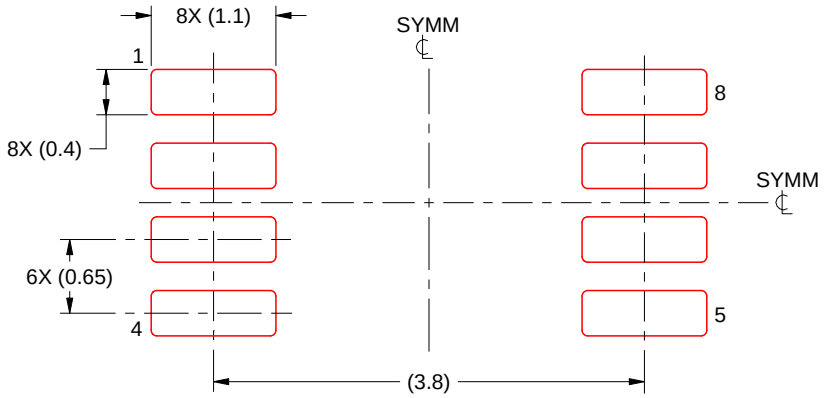


SOLDER MASK DETAILS

4220784/D 10/2025

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/D 10/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

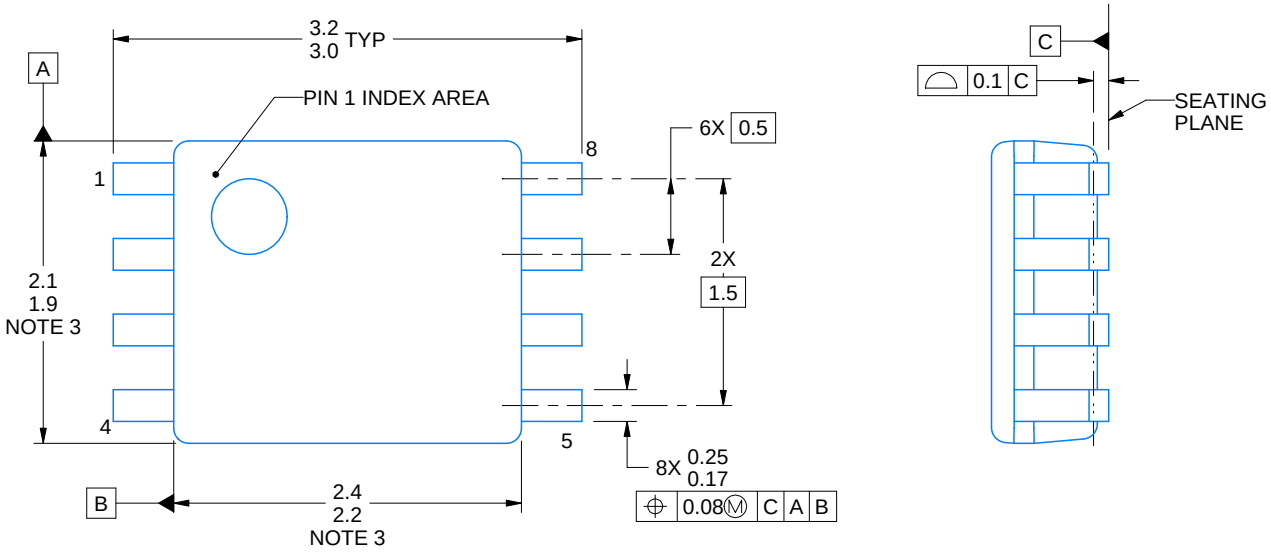
DCU0008A

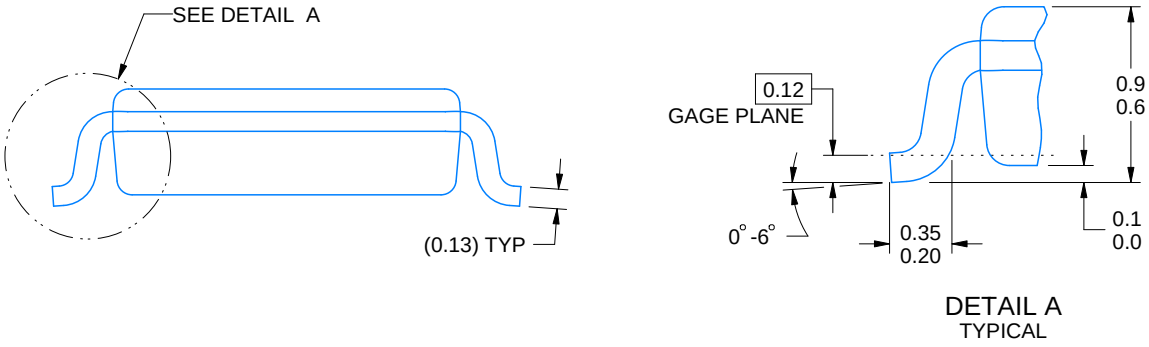


PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

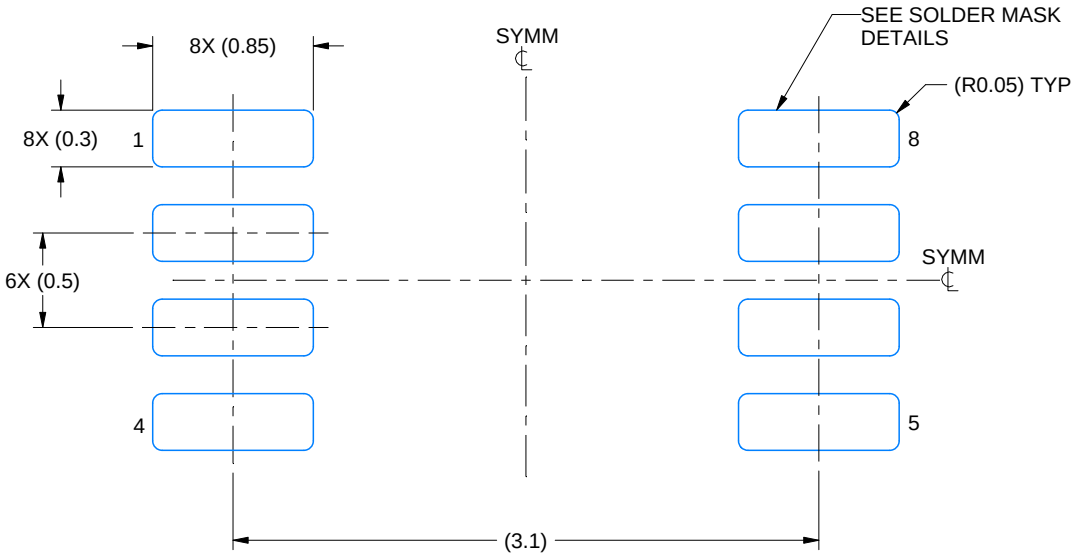




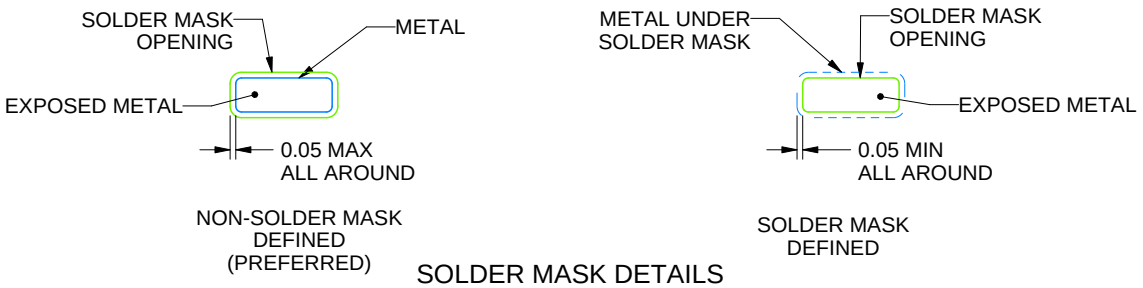
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

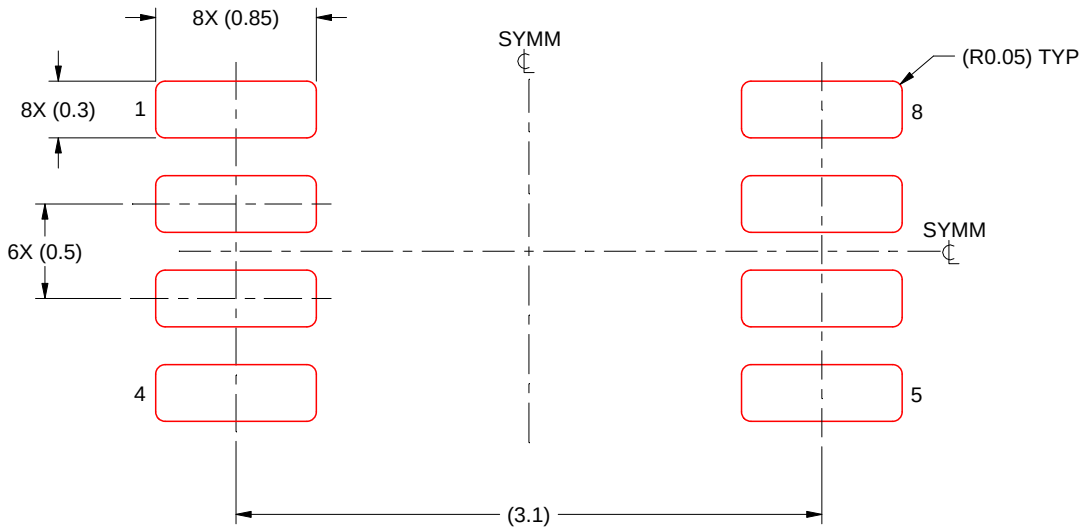


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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