SN74AVC8T245 8 ビット デュアル電源 バス・トランシーバ、構成可能電圧変換、3 ステート出力

1 特長

- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護:
  - 8000V、人体モデル (A114-A)
  - 200V マシン・モデル (A115-A)
  - 1000V デバイス帯電モデル (C101)
- 制御入力の V_{IH}/V_{IL} レベルは V_{CCA} 電圧を基準
- V_{CC} 絶縁機能:いずれかの V_{CC} 入力が GND レベルになると、すべての出力がハイ・インピーダンス状態に移行
- I_{off} により部分的パワーダウン・モードをサポート
- 完全に構成可能なデュアル・レール設計により、1.4V～3.6V の電源電圧の全範囲にわたって各ポートが動作可能
- 4.6V 許容の I/O
- 最大データ・レート:
  - 170Mbps (V_{CCA} < 1.8V または V_{CCB} < 1.8V)
  - 320Mbps (V_{CCA} ≥ 1.8V および V_{CCB} ≥ 1.8V)

2 アプリケーション

- パーソナル・エレクトロニクス
- 産業用
- エンタープライズ
- テレコム

3 概要

この 8 ビット非反転バス・トランシーバは、設定可能な 2 本の独立した電源レールを使用します。SN74AVC8T245 は V_{CCA}/V_{CCB} を 1.4V～3.6V に設定して動作するように最適化されています。本デバイスは最低 1.2V の V_{CCA}/V_{CCB} で動作します。A ポートは V_{CCA} に追従する設計です。V_{CCA} は 1.2V～3.6V の電源電圧に対応します。B ポートは V_{CCB} に追従する設計です。V_{CCB} には 1.2 V～3.6 V の電源電圧に対応します。このため 1.2V、1.5V、1.8V、2.5V、3.3V の任意の電圧ノード間で、低電圧の双方向変換を自在に行うことが可能になります。

SN74AVC8T245 は、データ・バス間の非同期通信用に設計されています。このデバイスは、方向制御 (DIR) 入力の論理レベルに応じて、A バスから B バス、または B バスから A バスへデータを転送します。出力イネーブル ($\overline{OE}$) 入力を使用すると、出力をディセーブルにして、バスを実質的に絶縁できます。

SN74AVC8T245 は、制御ピン (DIR および $\overline{OE}$) が V_{CCA} から電源を供給されるように設計されています。

SN74AVC8T245 は単一電源システムと互換性があり、後で '245 機能に置き換えることができ、プリント基板の再設計を最小限に抑えることができます。

このデバイスは、I_{off} を使った部分的パワーダウン・アプリケーション向けに完全に動作が規定されています。I_{off} 回路が出力をディセーブルにするため、電源切断時にデバイスに電流が逆流して損傷に至ることを回避できます。

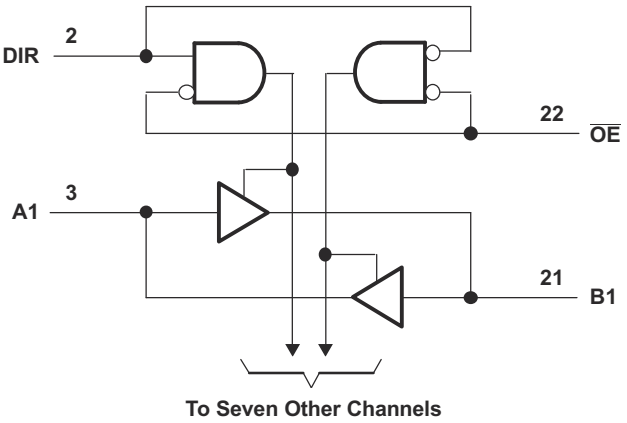
V_{CC} 絶縁機能により、どちらかの V_{CC} 入力が GND レベルになると、両方のポートをハイ・インピーダンス状態にできます。

電源オンまたは電源オフ時にデバイスをハイ・インピーダンス状態にするには、$\overline{OE}$ をプルアップ抵抗経由で V_{CC} に接続します。この抵抗の最小値は、ドライバの電流シンク能力によって決まります。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
SN74AVC8T245	RHL (VQFN、24)	5.5mm × 3.5mm
	PW (TSSOP、24)	7.8mm × 6.4mm
	DGV (TVSOP、24)	5mm × 6.4mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



論理図 (正論理)

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4 Pin Configuration and Functions

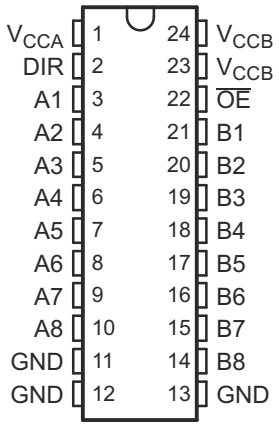


図 4-1. DGV or PW Package, 24-Pin TVSOP or TSSOP (Top View)

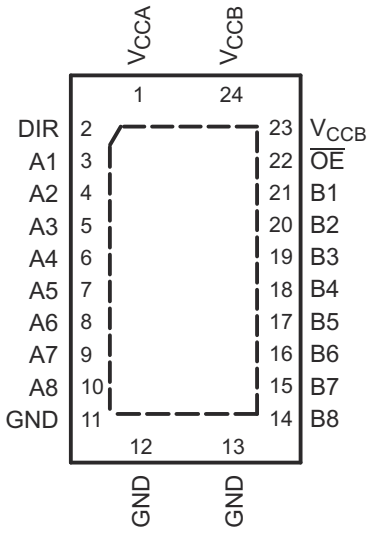


図 4-2. RHL Package, 24-Pin VQFN (Top View)

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A1	3	I/O	Input/output A1. Referenced to V_{CCA}.
A2	4	I/O	Input/output A2. Referenced to V_{CCA}.
A3	5	I/O	Input/output A3. Referenced to V_{CCA}.
A4	6	I/O	Input/output A4. Referenced to V_{CCA}.
A5	7	I/O	Input/output A5. Referenced to V_{CCA}.
A6	8	I/O	Input/output A6. Referenced to V_{CCA}.
A7	9	I/O	Input/output A7. Referenced to V_{CCA}.
A8	10	I/O	Input/output A8. Referenced to V_{CCA}.
B1	21	I/O	Input/output B1. Referenced to V_{CCB}.
B2	20	I/O	Input/output B2. Referenced to V_{CCB}.
B3	19	I/O	Input/output B3. Referenced to V_{CCB}.
B4	18	I/O	Input/output B4. Referenced to V_{CCB}.
B5	17	I/O	Input/output B5. Referenced to V_{CCB}.
B6	16	I/O	Input/output B6. Referenced to V_{CCB}.
B7	15	I/O	Input/output B7. Referenced to V_{CCB}.
B8	14	I/O	Input/output B8. Referenced to V_{CCB}.
DIR	2	I	Direction-control signal
GND	11, 12, 13	—	Ground
$\overline{OE}$	22	I	3-state output-mode enables. Pull $\overline{OE}$ high to place all outputs in 3-state mode. Referenced to V_{CCA}.
V_{CCA}	1	—	A-port supply voltage. 1.2 V ≤ V_{CCA} ≤ 3.6 V
V_{CCB}	23, 24	—	B-port supply voltage. 1.2 V ≤ V_{CCA} ≤ 3.6 V

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CCA}, V_{CCB}	Supply voltage		–0.5	4.6	V
V_I	Input voltage(2)	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage range applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current		–50	50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND		–100	100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

See (1) (2) (3)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs	1.2 V to 1.95 V		V_{CCI} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs	1.2 V to 1.95 V			V_{CCI} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})	1.2 V to 1.95 V		V_{CCA} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})	1.2 V to 1.95 V			V_{CCA} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.2 V		–3	mA
				1.4 V to 1.6 V		–6	
				1.65 V to 1.95 V		–8	
				2.3 V to 2.7 V		–9	
				3 V to 3.6 V		–12	
I_{OL}	Low-level output current			1.2 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

5.4 Thermal Information

THERMAL METRIC[1]		SN74AVC8T245			UNIT
		DGV	PW	RHL	
		24 PINS	24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	93.1	36.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.5	36.7	32.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.1	48.4	15.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.0	93.1	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.6	48.0	15.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	5.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)[2] [1]

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to +85°C		–40°C to +125°C		UNIT
						MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –100 µA	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V				V_{CCO} – 0.2		V_{CCO} – 0.2		V
		I_{OH} = –3 mA		1.2 V	1.2 V		0.95						
		I_{OH} = –6 mA		1.4 V	1.4 V				1.05		1		
		I_{OH} = –8 mA		1.65 V	1.65 V				1.2		1.2		
		I_{OH} = –9 mA		2.3 V	2.3 V				1.75		1.75		
		I_{OH} = –12 mA		3 V	3 V				2.3		2.3		
V_{OL}		I_{OL} = 100 µA	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V					0.2		0.2	V
		I_{OL} = 3 mA		1.2 V	1.2 V		0.15						
		I_{OL} = 6 mA		1.4 V	1.4 V					0.35		0.35	
		I_{OL} = 8 mA		1.65 V	1.65 V					0.45		0.45	
		I_{OL} = 9 mA		2.3 V	2.3 V					0.55		0.55	
		I_{OL} = 12 mA		3 V	3 V					0.7		0.7	
I_I	Control inputs	$V_I = V_{CCA}$ or GND		1.2 V to 3.6 V	1.2 V to 3.6 V	–0.25	±0.025	0.25	–1	1		±1	µA
I_{off}	A or B port	V_I or V_O = 0 to 3.6 V		0 V	0 V to 3.6 V	–1	±0.1	1	–5	5		±5	µA
				0 V to 3.6 V	0 V	–1	±0.1	1	–5	5		±5	
I_{OZ} [3]	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$		3.6 V	3.6 V		±0.5	±2.5		±5		±5	µA
I_{CCA}		$V_I = V_{CCI}$ or GND,	I_O = 0	1.2 V to 3.6 V	1.2 V to 3.6 V					15		15	µA
				0 V	3.6 V					–2		–2	
				3.6 V	0 V					15		15	
I_{CCB}		$V_I = V_{CCI}$ or GND,	I_O = 0	1.2 V to 3.6 V	1.2 V to 3.6 V					15		15	µA
				0 V	3.6 V					15		15	
				3.6 V	0 V					–2		–2	
I_{CCA} + I_{CCB}		$V_I = V_{CCI}$ or GND,	I_O = 0	1.2 V to 3.6 V	1.2 V to 3.6 V					25		25	µA
C_i	Control inputs	V_I = 3.3 V or GND		3.3 V	3.3 V		3.5			4.5			pF
C_{io}	A or B port	V_O = 3.3 V or GND		3.3 V	3.3 V		6			7			pF

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

5.6 Switching Characteristics, V_{CCA} = 1.2 V

over recommended operating free-air temperature range, V_{CCA} = 1.2 V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	T_A = –40°C to +85°C	T_A = –40°C to +125°C	UNIT
				TYP	TYP	
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2 V	3.1	3.1	ns
			V_{CCB} = 1.5 V	2.6	2.6	
			V_{CCB} = 1.8 V	2.5	2.5	
			V_{CCB} = 2.5 V	3	3	
			V_{CCB} = 3.3 V	3.5	3.5	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2 V	3.1	3.1	ns
			V_{CCB} = 1.5 V	2.7	2.7	
			V_{CCB} = 1.8 V	2.5	2.5	
			V_{CCB} = 2.5 V	2.4	2.4	
			V_{CCB} = 3.3 V	2.3	2.3	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2 V	5.3	5.3	ns
			V_{CCB} = 1.5 V			
			V_{CCB} = 1.8 V			
			V_{CCB} = 2.5 V			
			V_{CCB} = 3.3 V			
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2 V	5.1	5.1	ns
			V_{CCB} = 1.5 V	4	4	
			V_{CCB} = 1.8 V	3.5	3.5	
			V_{CCB} = 2.5 V	3.2	3.2	
			V_{CCB} = 3.3 V	3.1	3.1	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2 V	4.8	4.8	ns
			V_{CCB} = 1.5 V			
			V_{CCB} = 1.8 V			
			V_{CCB} = 2.5 V			
			V_{CCB} = 3.3 V			
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2 V	4.7	4.7	ns
			V_{CCB} = 1.5 V	4	4	
			V_{CCB} = 1.8 V	4.1	4.1	
			V_{CCB} = 2.5 V	4.3	4.3	
			V_{CCB} = 3.3 V	5.1	5.1	

5.7 Switching Characteristics, V_{CCA} = 1.5 V ± 0.1 V

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	T_A = –40°C to +85°C			T_A = –40°C to +125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2 V		2.7			3.1		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		5.4	0.5		14.7	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		4.6	0.5		13.3	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		4.9	0.5		13.9	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		6.8	0.5		17.2	

5.7 Switching Characteristics, V_{CCA} = 1.5 V ± 0.1 V (続き)

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	T_A = –40°C to +85°C			T_A = –40°C to +125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2 V		2.6			3.1		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		5.4	0.5		14.7	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		5.1	0.5		14.2	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		4.7	0.5		13.5	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		4.5	0.5		13.2	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2 V		3.7			5.3		ns
			V_{CCB} = 1.5 V ± 0.1 V	1.1		8.7	0.5		20.5	
			V_{CCB} = 1.8 V ± 0.15 V	1.1		8.7	0.5		20.5	
			V_{CCB} = 2.5 V ± 0.2 V	1.1		8.7	0.5		20.5	
			V_{CCB} = 3.3 V ± 0.3 V	1.1		8.7	0.5		20.5	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2 V		4.8			5.1		ns
			V_{CCB} = 1.5 V ± 0.1 V	1.1		7.6	0.5		18.6	
			V_{CCB} = 1.8 V ± 0.15 V	1.1		7.1	0.5		17.7	
			V_{CCB} = 2.5 V ± 0.2 V	1		5.6	0.5		15.1	
			V_{CCB} = 3.3 V ± 0.3 V	1		5.2	0.5		14.4	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2 V		3.1			4.8		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		8.6	0.5		20.3	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		8.6	0.5		20.3	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		8.6	0.5		20.3	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		8.6	0.5		20.3	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2 V		4.1			4.7		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		8.4	0.5		20	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		7.6	0.5		18.6	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		7.2	0.5		17.9	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		7.8	0.5		18.9	

5.8 Switching Characteristics, V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	T_A = –40°C to +85°C			T_A = –40°C to +125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2 V		2.5			2.5		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		5.1	0.5		14.2	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		4.4	0.5		13	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		4	0.5		12.3	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		3.9	0.5		12.1	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2 V		2.5			2.5		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		4.6	0.5		13.3	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		4.4	0.5		13	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		3.9	0.5		12.1	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		3.7	0.5		11.8	

5.8 Switching Characteristics, V_{CCA} = 1.8 V ± 0.15 V (続き)

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	T_A = –40°C to +85°C			T_A = –40°C to +125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2 V		3			3		ns
			V_{CCB} = 1.5 V ± 0.1 V	1		6.8	0.5		17.2	
			V_{CCB} = 1.8 V ± 0.15 V	1		6.8	0.5		17.2	
			V_{CCB} = 2.5 V ± 0.2 V	1		6.8	0.5		17.2	
			V_{CCB} = 3.3 V ± 0.3 V	1		6.8	0.5		17.2	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2 V		4.6			4.6		ns
			V_{CCB} = 1.5 V ± 0.1 V	1.1		8.2	0.5		19.6	
			V_{CCB} = 1.8 V ± 0.15 V	1		6.7	0.5		17	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		5.1	0.5		14.2	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		4.5	0.5		13.2	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2 V		2.8			2.8		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		7.1	0.5		17.7	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		7.1	0.5		17.7	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		7.1	0.5		17.7	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		7.1	0.5		17.7	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2 V		3.9			3.9		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		7.8	0.5		18.9	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		6.9	0.5		17.3	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		6	0.5		15.8	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		5.8	0.5		15.4	

5.9 Switching Characteristics, V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	T_A = –40°C to +85°C			T_A = –40°C to +125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2 V		2.4			2.4		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		4.7	0.5		13.5	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		3.9	0.5		12.1	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		3.1	0.5		10.7	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		2.8	0.5		10.2	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2 V		3			3		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		4.9	0.5		13.9	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		4	0.5		12.3	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		3.1	0.5		10.7	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		2.9	0.5		10.4	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2 V		2.2			2.2		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		4.8	0.5		13.7	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		4.8	0.5		13.7	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		4.8	0.5		13.7	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		4.8	0.5		13.7	

5.9 Switching Characteristics, V_{CCA} = 2.5 V ± 0.2 V (続き)

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	T_A = –40°C to +85°C			T_A = –40°C to +125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2 V		4.5			4.5		ns
			V_{CCB} = 1.5 V ± 0.1 V	1.1		7.9	0.5		19.1	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		6.4	0.5		16.5	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		4.6	0.5		13.3	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		4	0.5		12.3	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2 V		1.8			1.8		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		5.1	0.5		14.2	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		5.1	0.5		14.2	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		5.1	0.5		14.2	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		5.1	0.5		14.2	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2 V		3.6			3.6		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		7.1	0.5		17.7	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		6.3	0.5		16.3	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		5.1	0.5		14.2	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		3.9	0.5		12.1	

5.10 Switching Characteristics, V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}		T_A = –40°C to +85°C			T_A = –40°C to +125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2 V			2.3			2.3		ns
			V_{CCB} = 1.5 V ± 0.1 V		0.5		4.5	0.5		13.2	
			V_{CCB} = 1.8 V ± 0.15 V	t_{PLH}	0.5		3.7	0.5		11.1	
				t_{PHL}	0.5		3.3	0.5		11.1	
			V_{CCB} = 2.5 V ± 0.2 V		0.5		2.9	0.5		10.4	
			V_{CCB} = 3.3 V ± 0.3 V		0.5		2.5	0.5		9.7	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2 V			3.5			3.5		ns
			V_{CCB} = 1.5 V ± 0.1 V		0.5		6.8	0.5		17.2	
			V_{CCB} = 1.8 V ± 0.15 V		0.5		3.9	0.5		12.1	
			V_{CCB} = 2.5 V ± 0.2 V		0.5		2.8	0.5		10.2	
			V_{CCB} = 3.3 V ± 0.3 V		0.5		2.5	0.5		9.7	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2 V			2			2		ns
			V_{CCB} = 1.5 V ± 0.1 V		0.5		4	0.5		12.3	
			V_{CCB} = 1.8 V ± 0.15 V		0.5		4	0.5		12.3	
			V_{CCB} = 2.5 V ± 0.2 V		0.5		4	0.5		12.3	
			V_{CCB} = 3.3 V ± 0.3 V		0.5		4	0.5		12.3	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2 V			4.5			4.5		ns
			V_{CCB} = 1.5 V ± 0.1 V		1.1		7.8	0.5		18.9	
			V_{CCB} = 1.8 V ± 0.15 V		0.5		6.2	0.5		16.1	
			V_{CCB} = 2.5 V ± 0.2 V		0.5		4.5	0.5		13.2	
			V_{CCB} = 3.3 V ± 0.3 V		0.5		3.9	0.5		12.3	

5.10 Switching Characteristics, V_{CCA} = 3.3 V ± 0.3 V (続き)

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	T_A = –40°C to +85°C			T_A = –40°C to +125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2 V		1.7			1.7		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		4	0.5		12.3	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		4	0.5		12.3	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		4	0.5		12.3	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		4	0.5		12.3	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2 V		3.4			3.4		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		6.9	0.5		17.4	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		6	0.5		15.8	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		4.8	0.5		13.7	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		4.2	0.5		12.6	

5.11 Operating Characteristics

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.2 V	V_{CCA} = V_{CCB} = 1.5 V	V_{CCA} = V_{CCB} = 1.8 V	V_{CCA} = V_{CCB} = 2.5 V	V_{CCA} = V_{CCB} = 3.3 V	UNIT
				TYP	TYP	TYP	TYP	TYP	
C_{pdA} (1)	A to B	Outputs enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	1	1	1	1	1	pF
		Outputs disabled		1	1	1	1	1	
	B to A	Outputs enabled		12	12	12	13	14	
		Outputs disabled		1	1	1	1	1	
C_{pdB} (1)	A to B	Outputs enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	12	12	12	13	14	pF
		Outputs disabled		1	1	1	1	1	
	B to A	Outputs enabled		1	1	1	1	1	
		Outputs disabled		1	1	1	1	1	

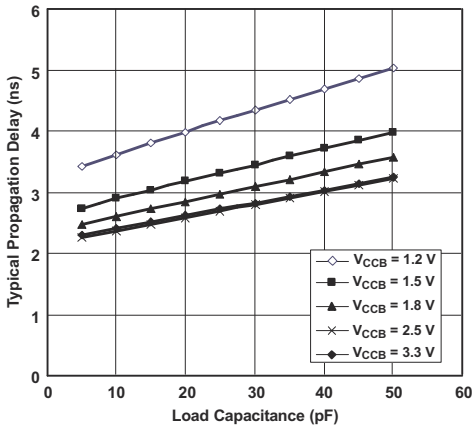
(1) Power dissipation capacitance per transceiver

5.12 Typical Total Static Power Consumption (I_{CCA} + I_{CCB})

V_{CCB}	V_{CCA}						UNIT
	0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	<0.5	<0.5	<0.5	<0.5	<0.5	μA
1.2 V	<0.5	<1	<1	<1	<1	1	
1.5 V	<0.5	<1	<1	<1	<1	1	
1.8 V	<0.5	<1	<1	<1	<1	<1	
2.5 V	<0.5	1	<1	<1	<1	<1	
3.3 V	<0.5	1	<1	<1	<1	<1	

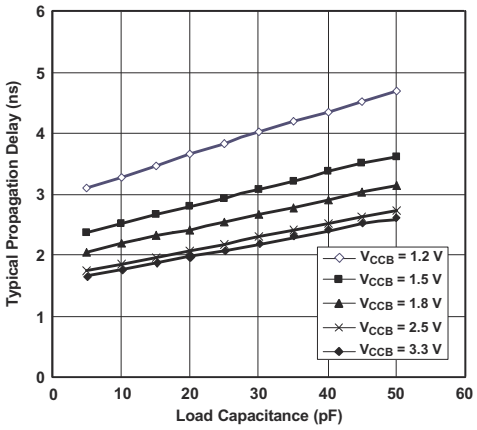
5.13 Typical Characteristics

T_A = 25°C



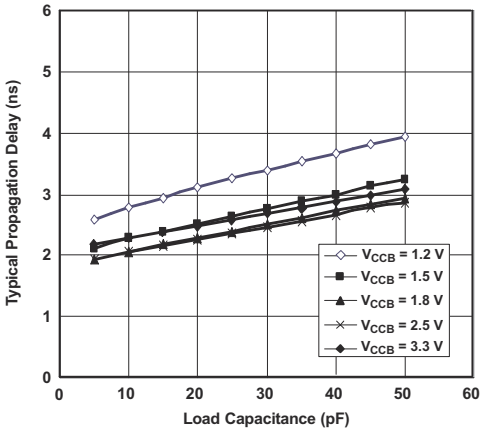
V_{CCA} = 1.2 V

図 5-1. Typical Propagation Delay (A to B) vs Load Capacitance



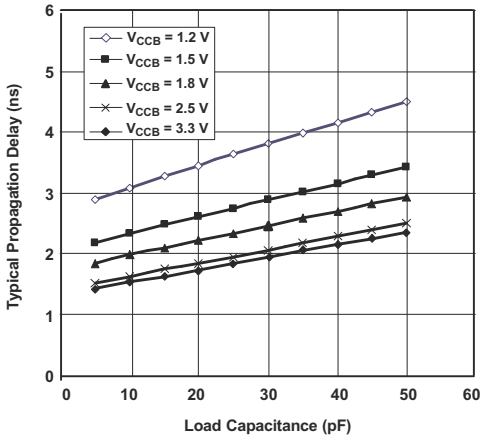
V_{CCA} = 1.5 V

図 5-2. Typical Propagation Delay (A to B) vs Load Capacitance



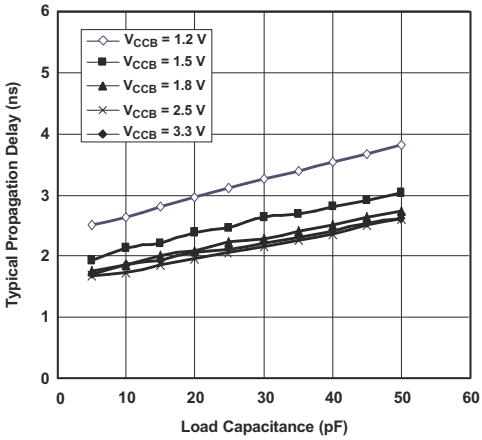
V_{CCA} = 1.5 V

図 5-3. Typical Propagation Delay (A to B) vs Load Capacitance



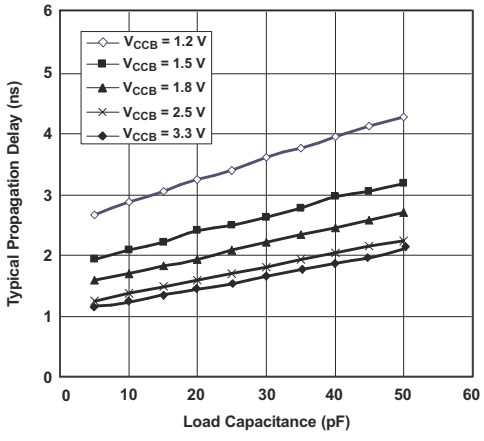
V_{CCA} = 1.8 V

図 5-4. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA} = 1.8 V

図 5-5. Typical Propagation Delay (A to B) vs Load Capacitance

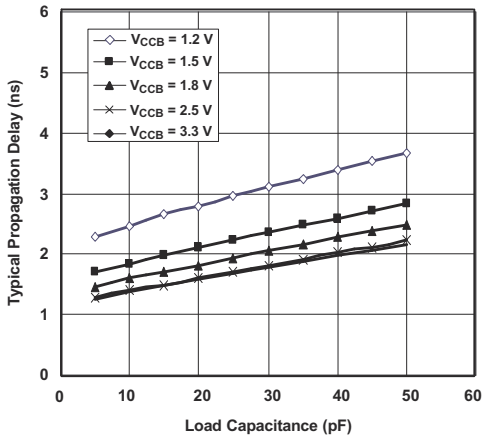


V_{CCA} = 2.5 V

図 5-6. Typical Propagation Delay (A to B) vs Load Capacitance

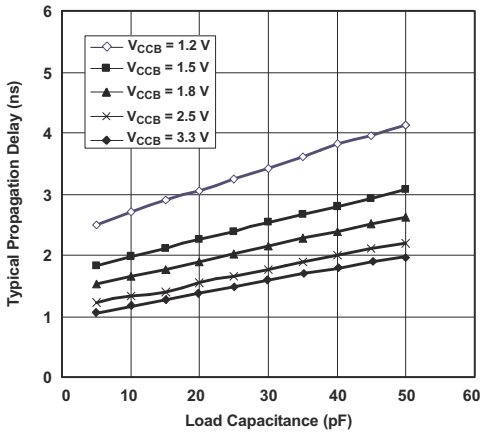
5.13 Typical Characteristics (continued)

T_A = 25°C



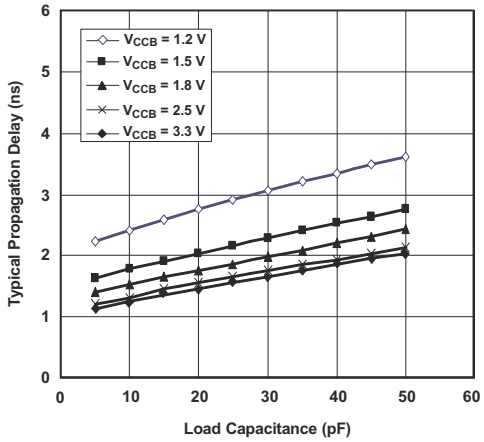
V_{CCA} = 2.5 V

図 5-7. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA} = 3.3 V

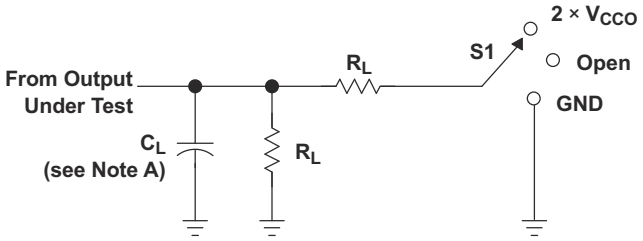
図 5-8. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA} = 3.3 V

図 5-9. Typical Propagation Delay (A to B) vs Load Capacitance

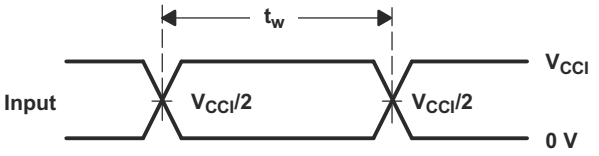
Parameter Measurement Information



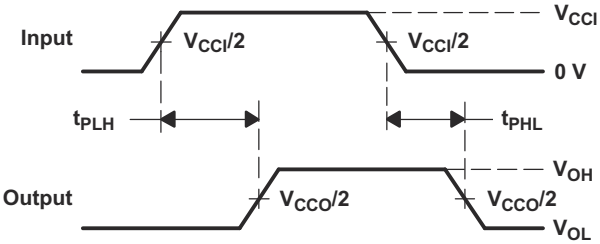
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CCO}
t_{PHZ}/t_{PZH}	GND

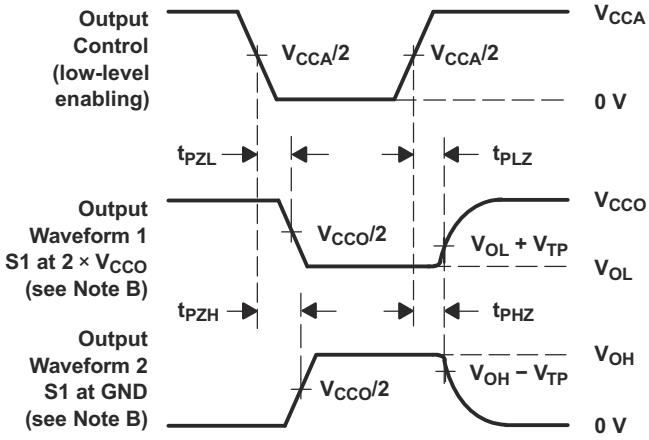
V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kW	0.1 V
1.5 V ± 0.1 V	15 pF	2 kW	0.1 V
1.8 V ± 0.15 V	15 pF	2 kW	0.15 V
2.5 V ± 0.2 V	15 pF	2 kW	0.15 V
3.3 V ± 0.3 V	15 pF	2 kW	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z_O = 50 W, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.

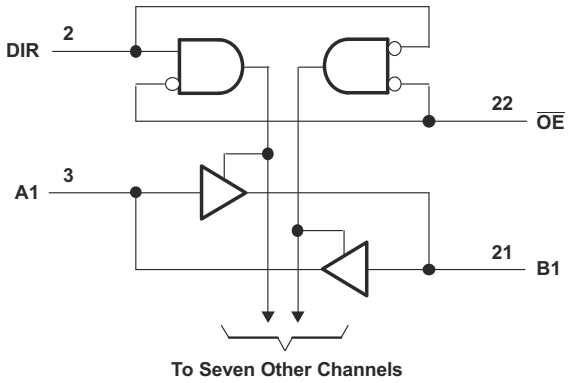
図 6-1. Load Circuit and Voltage Waveforms

6 Detailed Description

6.1 Overview

The SN74AVC8T245 is an 8-bit, dual-supply noninverting transceiver with bidirectional voltage level translation. V_{CCA} supports pins A and the control pins (DIR and $\overline{OE}$), and V_{CCB} supports pins B. The A port is able to accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.2 V to 3.6 V. A high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A when $\overline{OE}$ is set to low. When $\overline{OE}$ is set to high, both A and B are in the high-impedance state.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Fully Configurable Dual-Rail Design

The fully configurable dual-rail design allows each port to operate over the full 1.2-V to 3.6-V power-supply range. Both V_{CCA} and V_{CCB} can be supplied at any voltage between 1.2 V and 3.6 V making the device an excellent choice for translating between any of the low voltage nodes (1.2 V, 1.8 V, 2.5 V, and 3.3 V).

6.3.2 Support High-Speed Translation

SN74AVC8T245 can support high data rate application. The translated signal data rate can be up to 320Mbps when the device power supply is more than 1.8 V.

6.3.3 I_{off} Supports Partial-Power-Down Mode Operation

I_{off} prevents backflow current by disabling I/O output circuits when device is in partial power-down mode. The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

6.3.4 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Two outputs can be connected together for 2X stronger output drive strength. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

6.3.5 Vcc Isolation

The I/Os of both ports will enter a high-impedance state when one of the supplies are at GND, while the other supply is still connected to the device (IOZ shown in *Electrical Characteristics*).

6.4 Device Functional Modes

The SN74AVC8T245 is a voltage level transceiver that can operate from 1.2 V to 3.6 V (V_{CCA}) and 1.2 V to 3.6 V (V_{CCB}). The signal translation between 1.2 V and 3.6 V requires direction control and output enable control. When $\overline{OE}$ is low and DIR is high, data transmission is from A to B. When $\overline{OE}$ is low and DIR is low, data transmission is from B to A. When $\overline{OE}$ is high, both output ports will be high-impedance.

表 6-1. Function Table (Each 8-Bit Section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	All outputs Hi-Z

7 Application and Implementation

注

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7.1 Application Information

The SN74AVC8T245 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AVC8T245 device is an excellent choice for data transmission when direction is different. It is recommended to tie all unused I/Os to GND. The device should not have any floating I/Os when changing translation direction. The maximum data rate can be up to 320Mbps when device voltage power supply is more than 1.8 V.

7.2 Typical Application

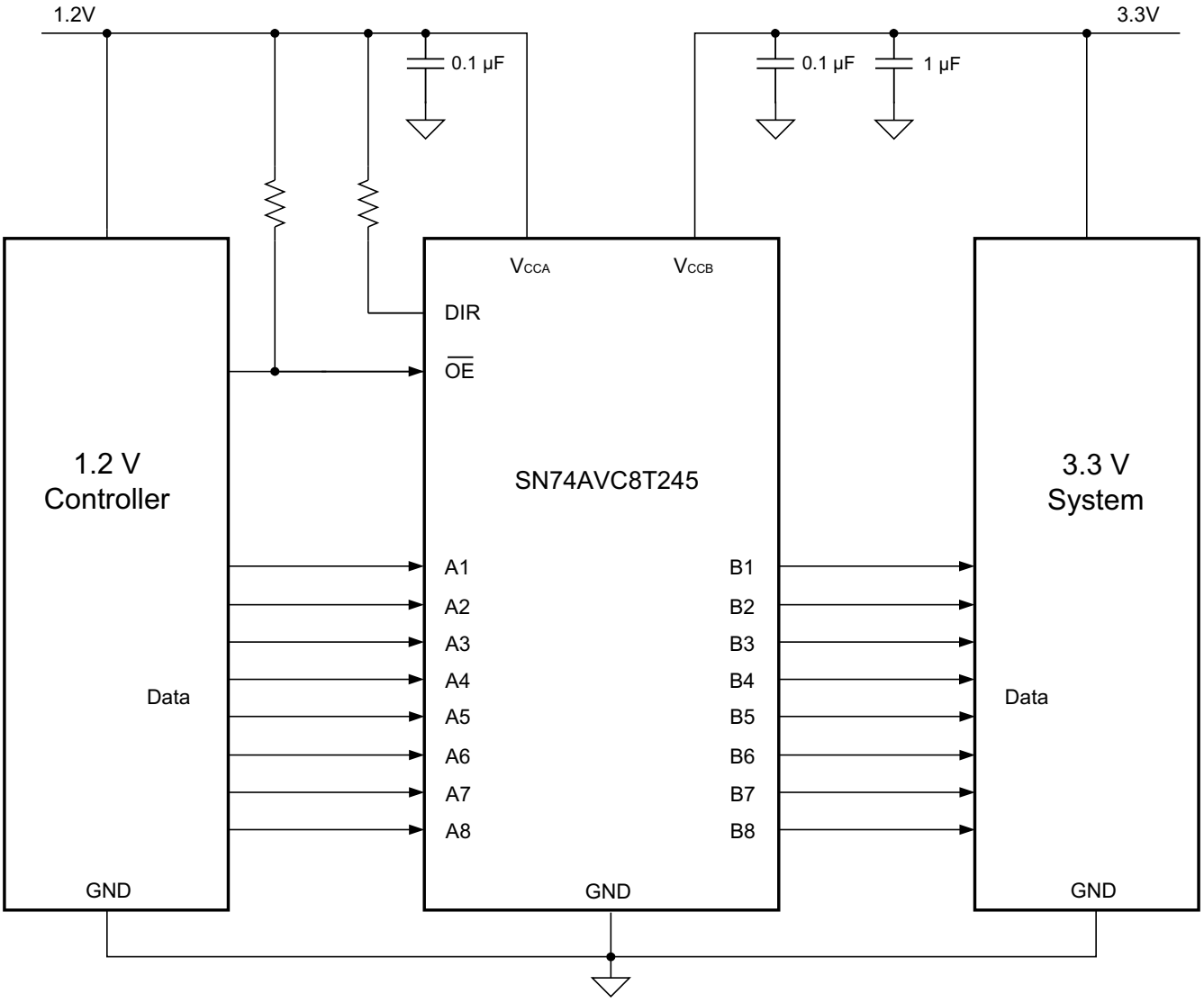

図 7-1. Typical Application Schematic

7.2.1 Design Requirements

For this design example, use the parameters listed in 表 7-1.

表 7-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	1.2 V to 3.6 V
Output voltage range	1.2 V to 3.6 V

7.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AVC8T245 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AVC8T245 device is driving to determine the output voltage range.

7.2.3 Application Curve

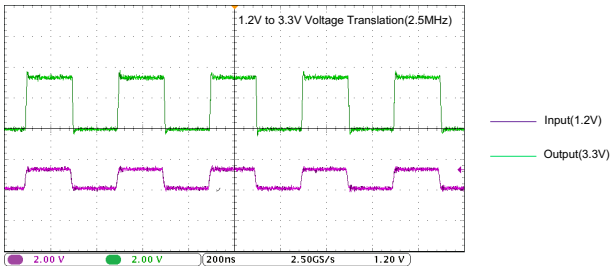

図 7-2. Translation Up (1.2 V to 3.3 V) at 2.5 MHz

7.3 Power Supply Recommendations

The SN74AVC8T245 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V and V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. The A port and B port are designed to track V_{CCA} and V_{CCB}, respectively, allowing for low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V and 3.3-V voltage nodes. The recommendation is to first power-up the input supply rail to help avoid internal floating while the output supply rail ramps up. However, both power-supply rails can be ramped up simultaneously.

The output-enable $\overline{OE}$ input circuit is designed so that it is supplied by V_{CCA} and when the $\overline{OE}$ input is high, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the $\overline{OE}$ input pin must be tied to V_{CCA} through a pullup resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pullup resistor to V_{CCA} is determined by the current-sinking capability of the driver.

7.4 Layout

7.4.1 Layout Guidelines

For device reliability, follow common printed-circuit board layout guidelines such as:

- Use bypass capacitors on power supplies.
- Use short trace lengths to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to adjust the signals rise and fall times, depending on the system requirements.

7.4.2 Layout Example

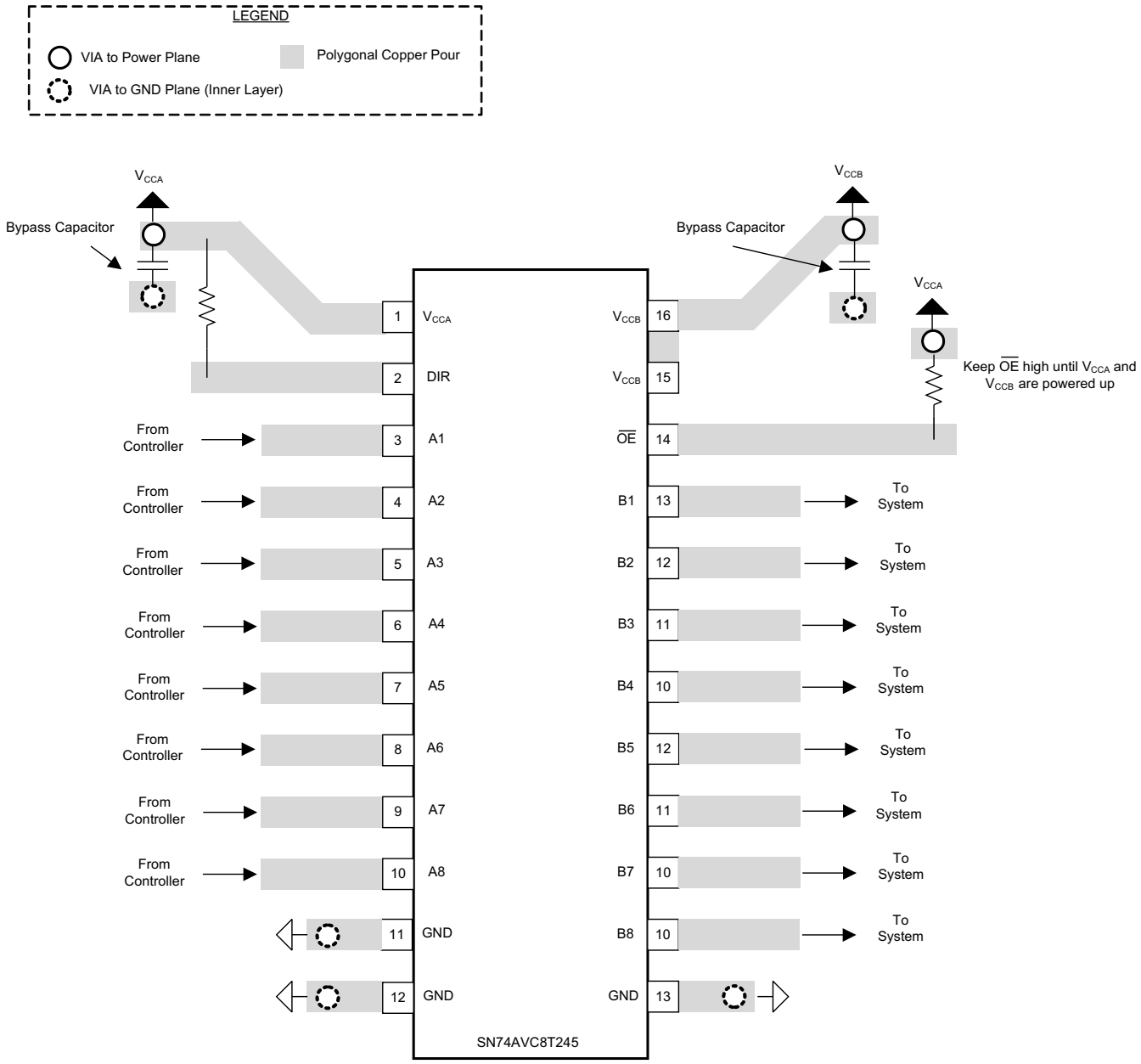

図 7-3. SN74AVC8T245 Layout Example

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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8.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
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8.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision J (March 2017) to Revision K (November 2023)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• パッケージ・リード・サイズを含めるよう「パッケージ情報」表を更新	1
• Updated the *Thermal Information* table for all packages	6

Changes from Revision I (December 2014) to Revision J (March 2017)	Page
• Changed MAX value for Operating free-air temperature, T_A from: 85°C to: 125°C	5
• Added values for T_A = –40°C to +125°C in *Electrical Characteristics* and all *Switching Characteristics* tables	6
• Added *Documentation Support* section, *Receiving Notification of Documentation Updates*, and *Community Resources* section	21

Changes from Revision H (February 2007) to Revision I (December 2014) **Page**

- 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74AVC8T245RHLRG4	Active	Production	VQFN (RHL) | 24	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	WE245
SN74AVC8T245DGVR	Active	Production	TVSOP (DGV) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WE245
SN74AVC8T245DGVR.A	Active	Production	TVSOP (DGV) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WE245
SN74AVC8T245DGVR.B	Active	Production	TVSOP (DGV) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WE245
SN74AVC8T245DGVRG4	Active	Production	TVSOP (DGV) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WE245
SN74AVC8T245DGVRG4.A	Active	Production	TVSOP (DGV) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WE245
SN74AVC8T245DGVRG4.B	Active	Production	TVSOP (DGV) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WE245
SN74AVC8T245PW	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WE245
SN74AVC8T245PW.B	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WE245
SN74AVC8T245PWE4	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WE245
SN74AVC8T245PWG4	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WE245
SN74AVC8T245PWR	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WE245
SN74AVC8T245PWR.A	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WE245
SN74AVC8T245PWR.B	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WE245
SN74AVC8T245PWRE4	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WE245
SN74AVC8T245PWRG4	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WE245
SN74AVC8T245RHLR	Active	Production	VQFN (RHL) | 24	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	WE245
SN74AVC8T245RHLR.A	Active	Production	VQFN (RHL) | 24	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	WE245
SN74AVC8T245RHLR.B	Active	Production	VQFN (RHL) | 24	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	WE245

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AVC8T245 :

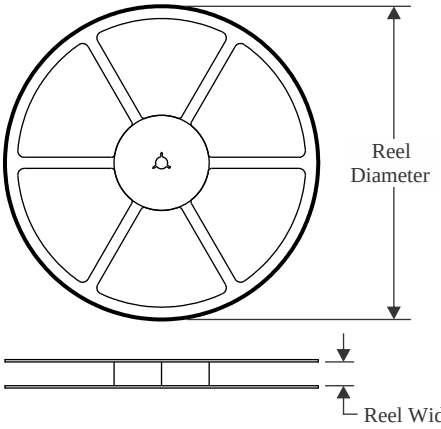
- Automotive : SN74AVC8T245-Q1

NOTE: Qualified Version Definitions:

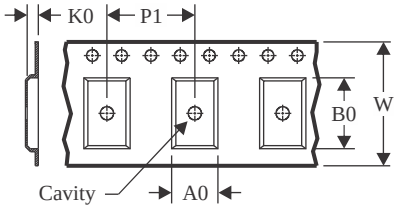
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

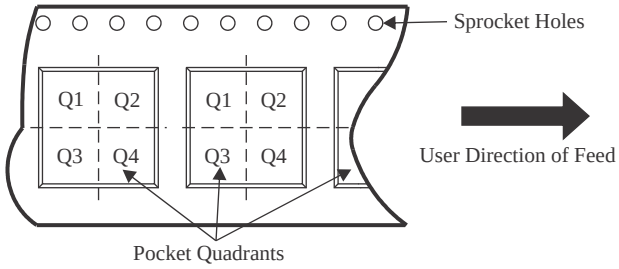


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

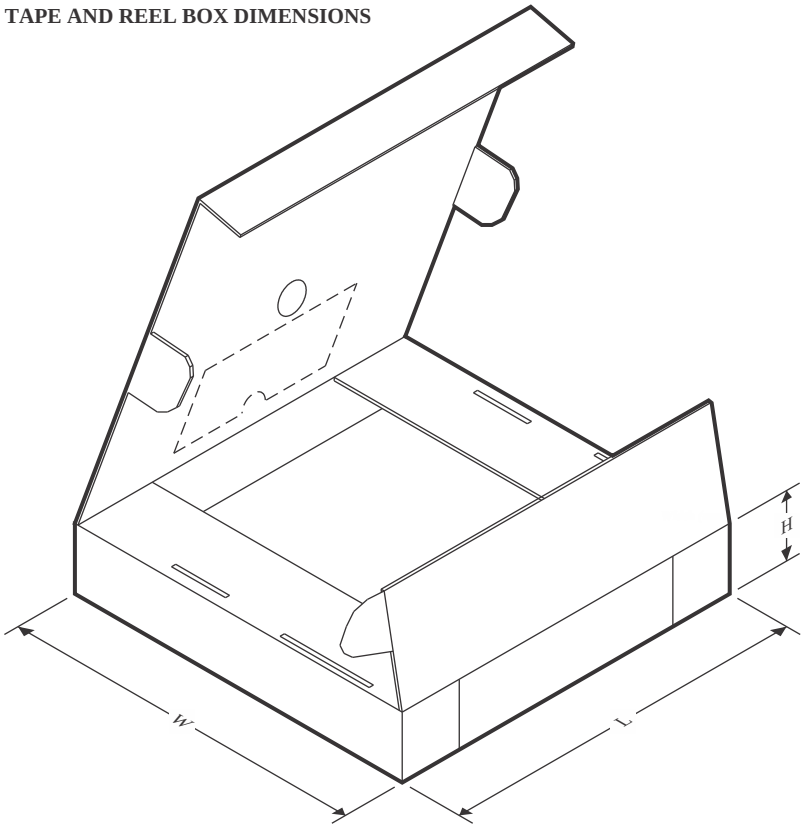
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC8T245DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVC8T245DGVRG4	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVC8T245PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74AVC8T245RHLR	VQFN	RHL	24	1000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
SN74AVC8T245RHLR	VQFN	RHL	24	1000	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
SN74AVC8T245RHLR	VQFN	RHL	24	1000	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

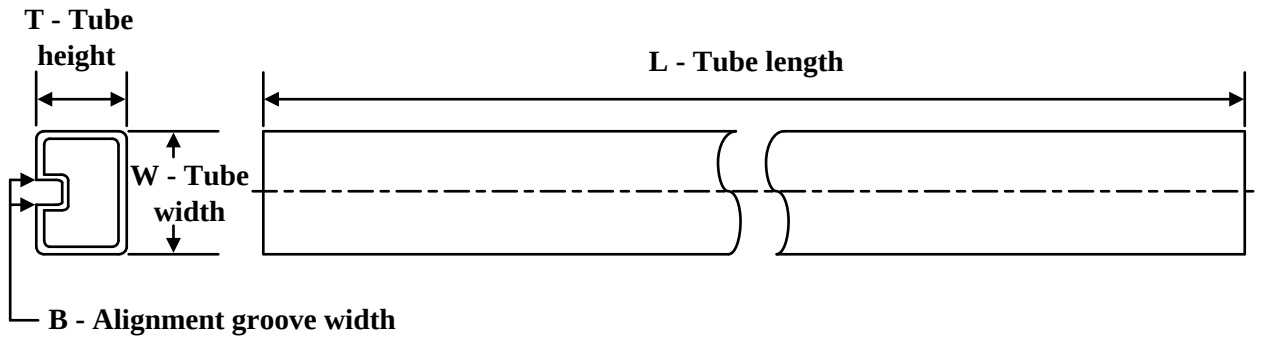
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC8T245DGVR	TVSOP	DGV	24	2000	353.0	353.0	32.0
SN74AVC8T245DGVRG4	TVSOP	DGV	24	2000	353.0	353.0	32.0
SN74AVC8T245PWR	TSSOP	PW	24	2000	353.0	353.0	32.0
SN74AVC8T245RHLR	VQFN	RHL	24	1000	367.0	367.0	35.0
SN74AVC8T245RHLR	VQFN	RHL	24	1000	213.0	191.0	35.0
SN74AVC8T245RHLR	VQFN	RHL	24	1000	210.0	185.0	35.0

TUBE



*All dimensions are nominal

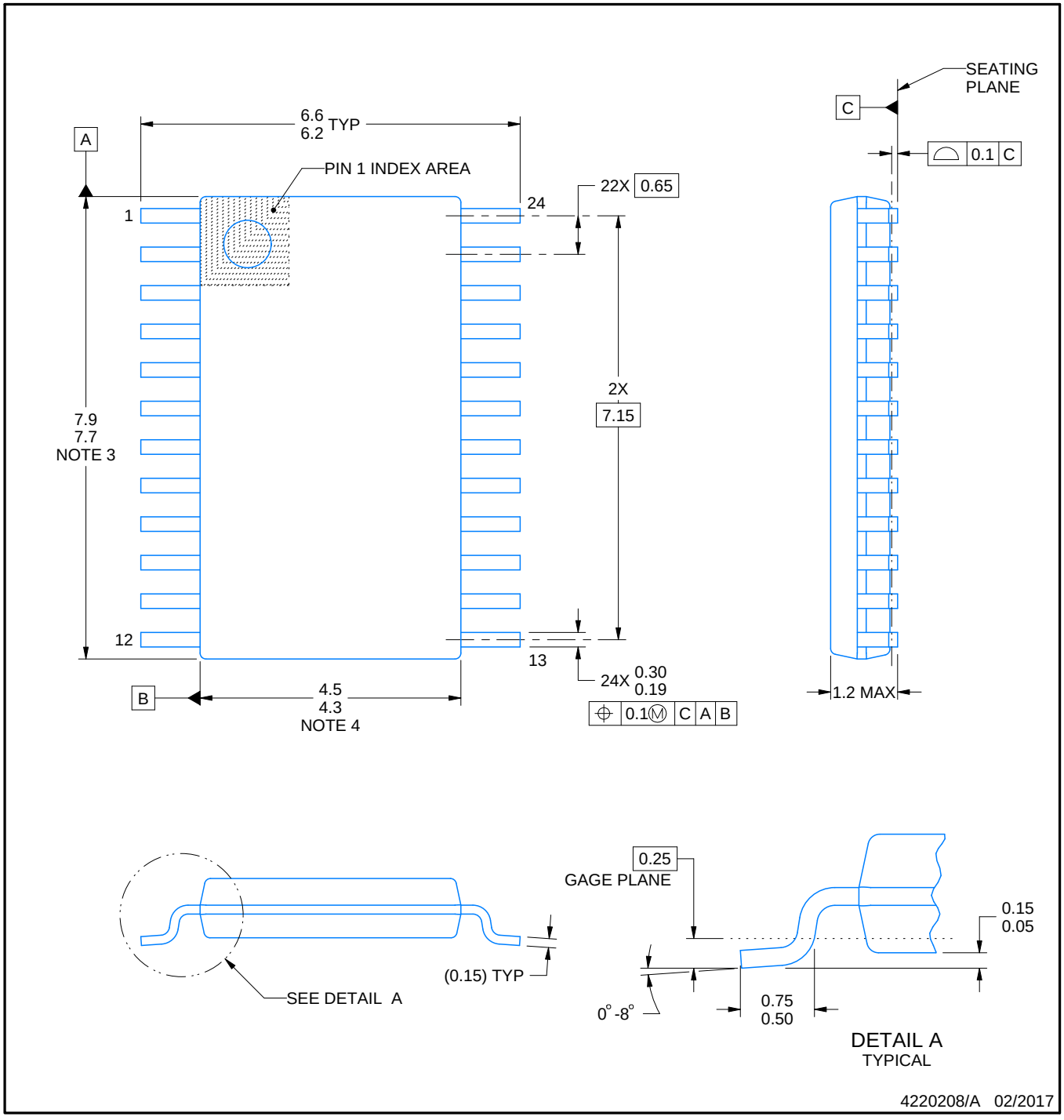
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74AVC8T245PW	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74AVC8T245PW.B	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74AVC8T245PWE4	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74AVC8T245PWG4	PW	TSSOP	24	60	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0024A

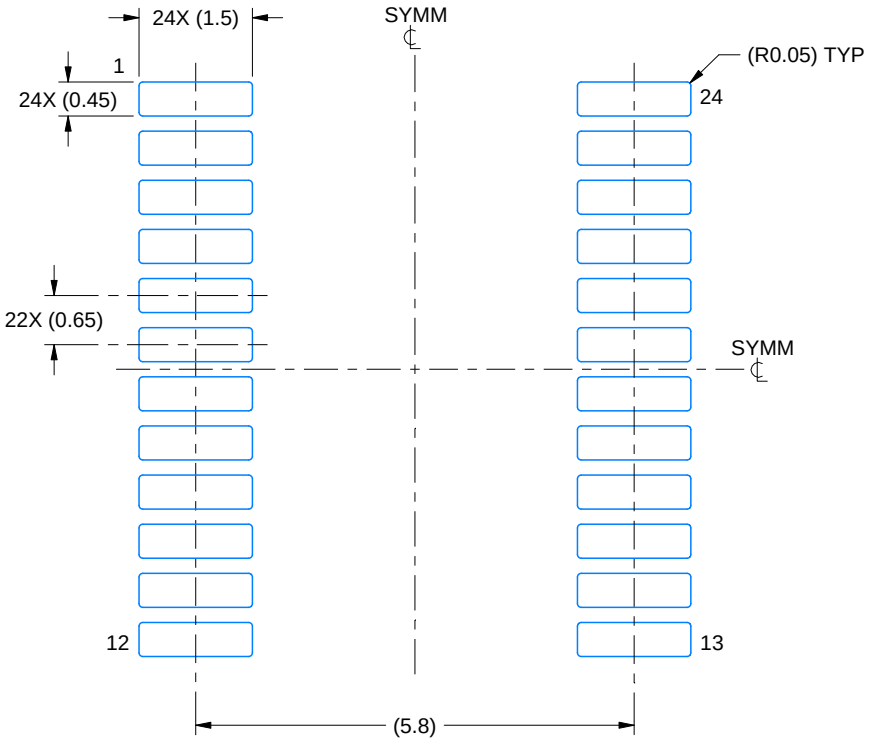
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

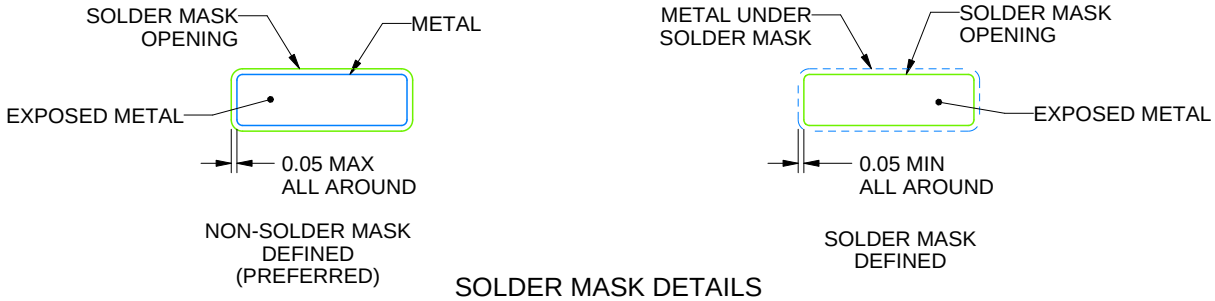


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

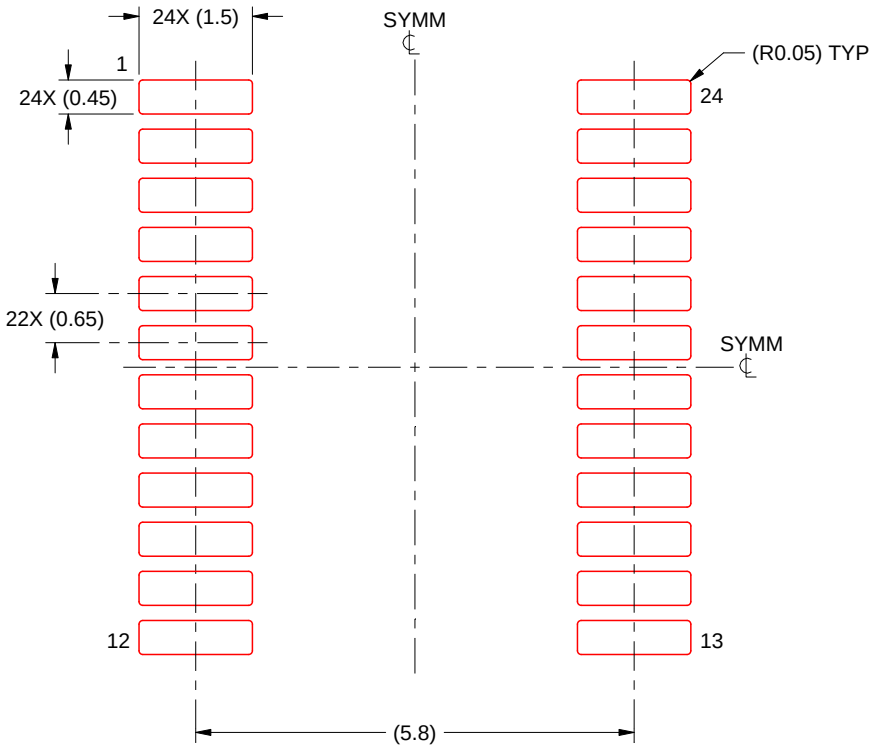


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

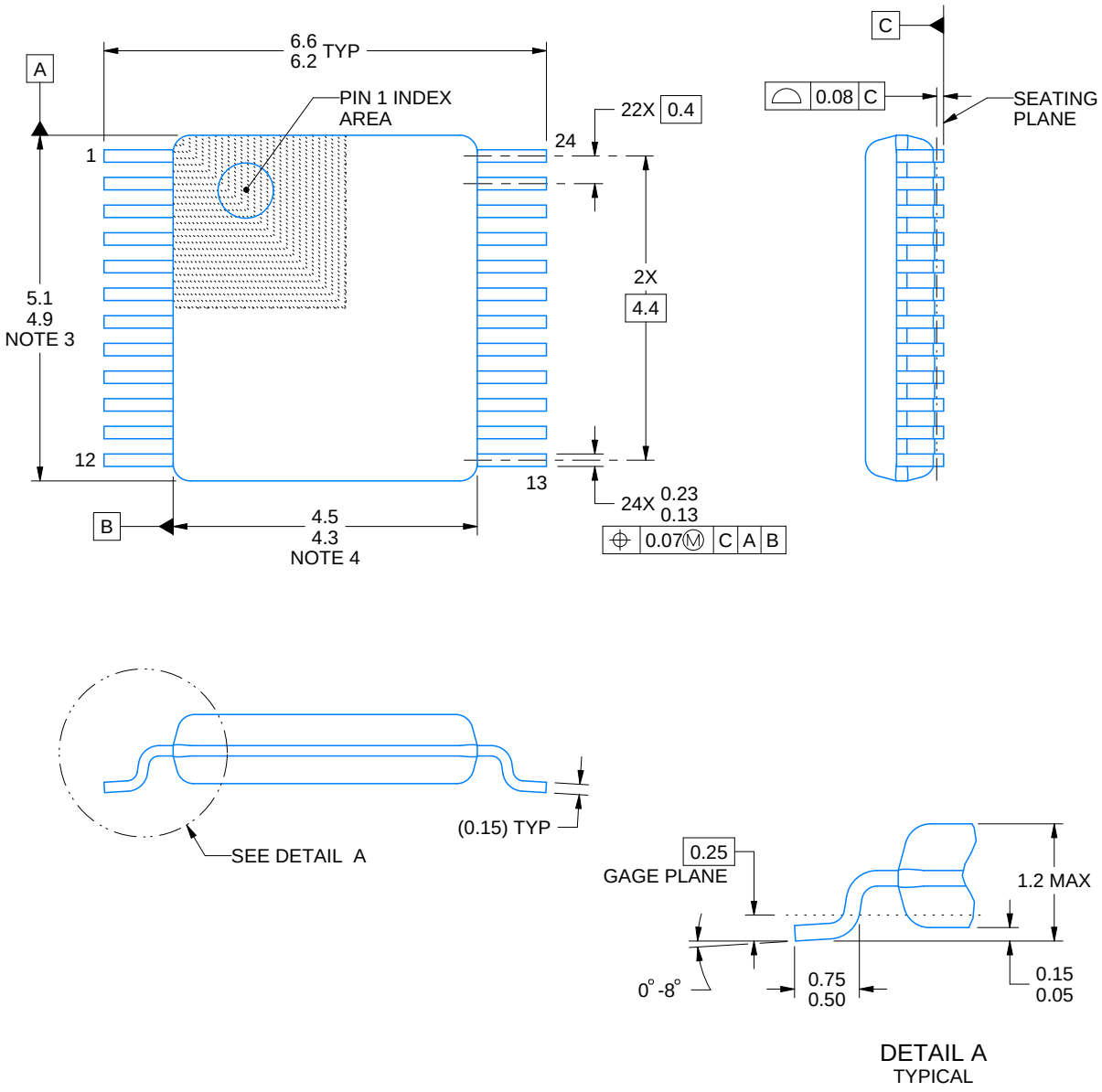
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGV0024A

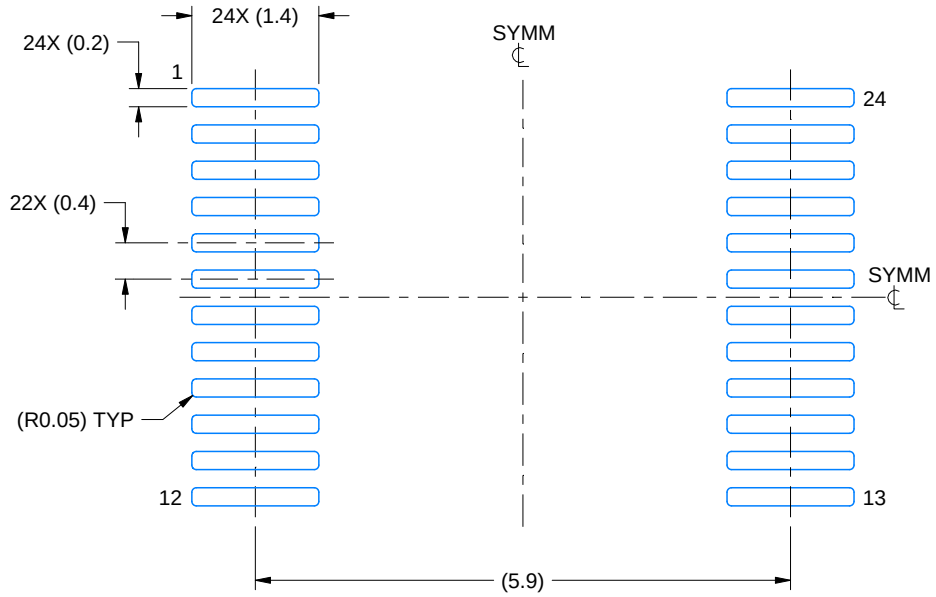
TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

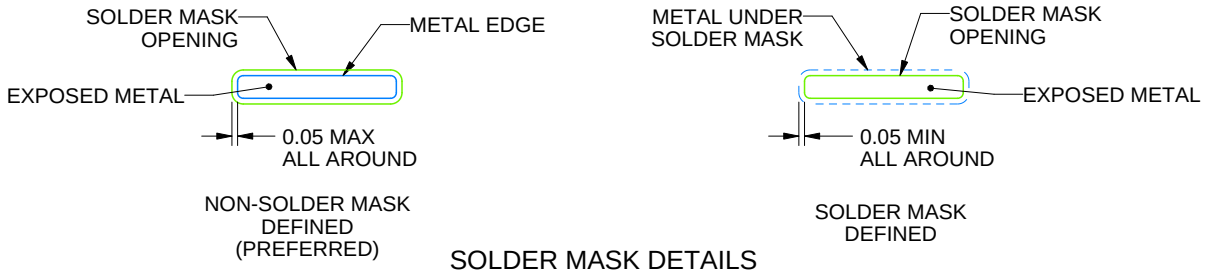


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

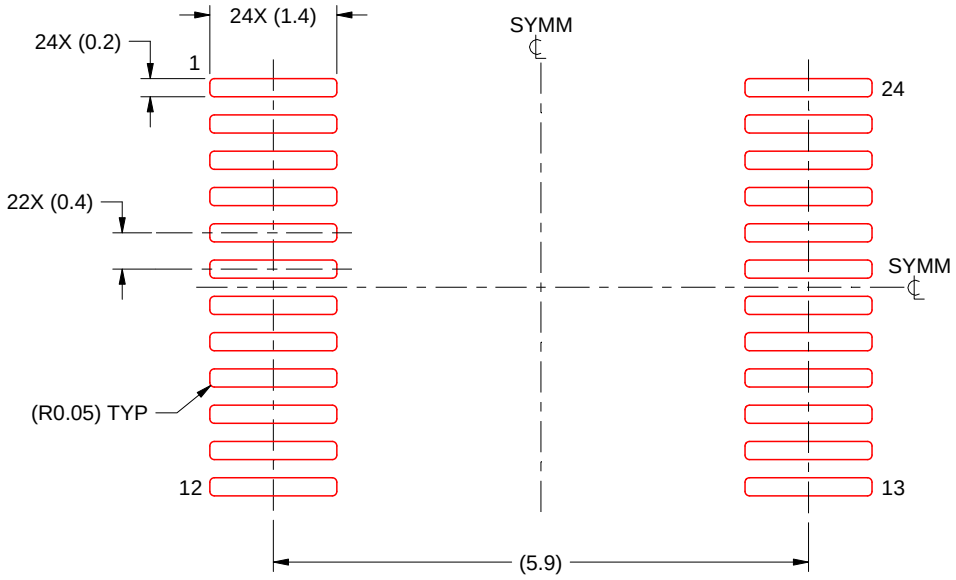


SOLDER MASK DETAILS

4229221/A 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

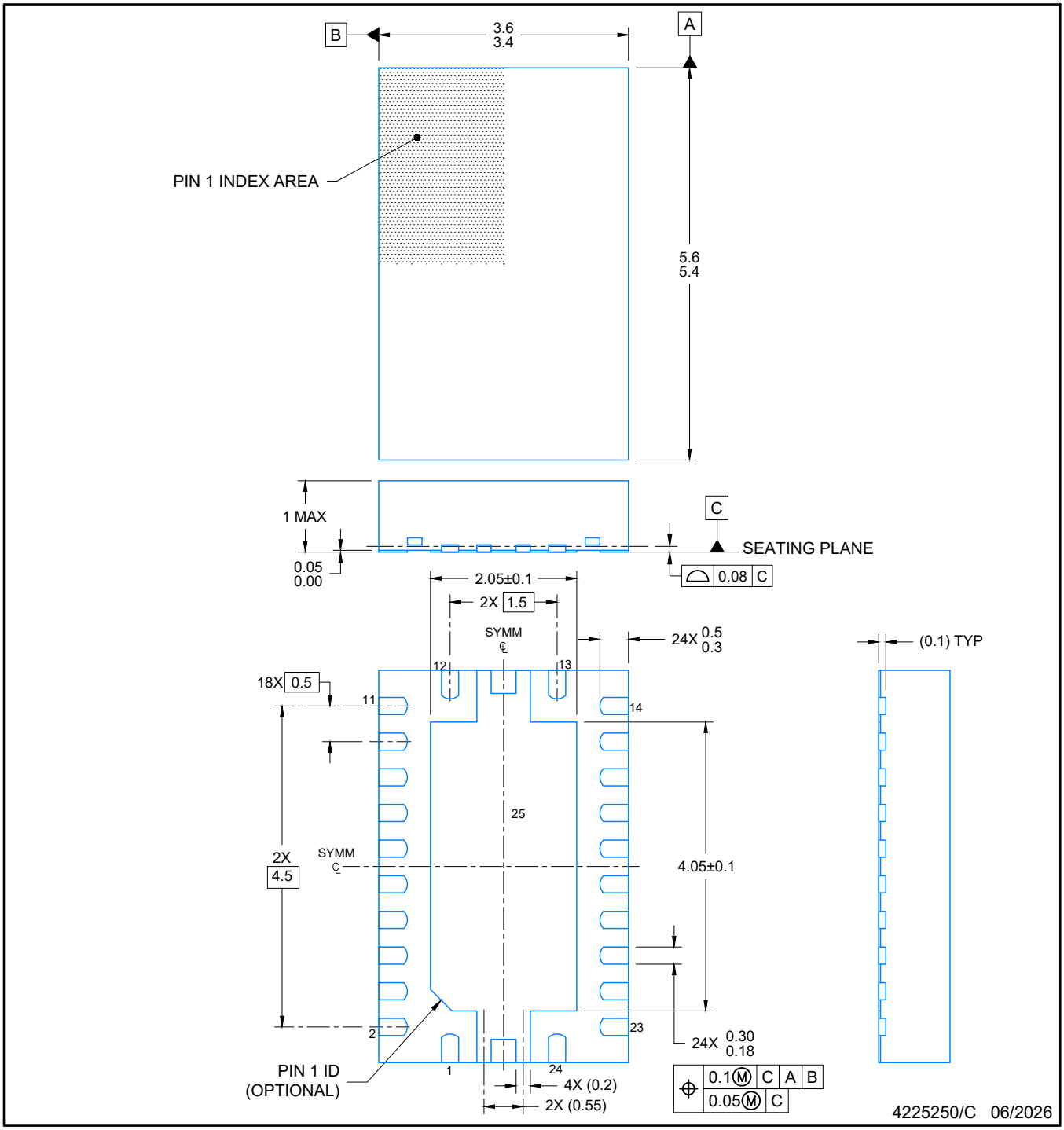


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

4229221/A 12/2022

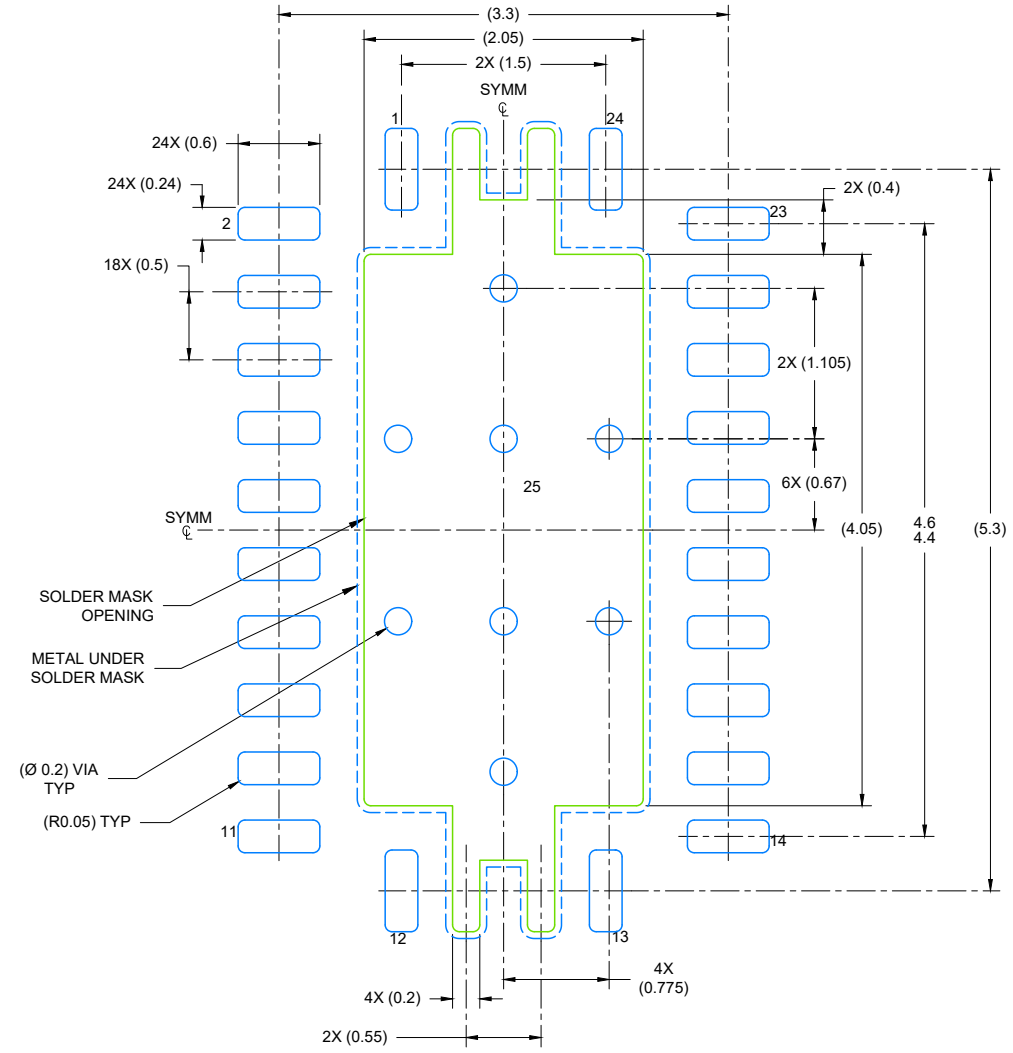
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

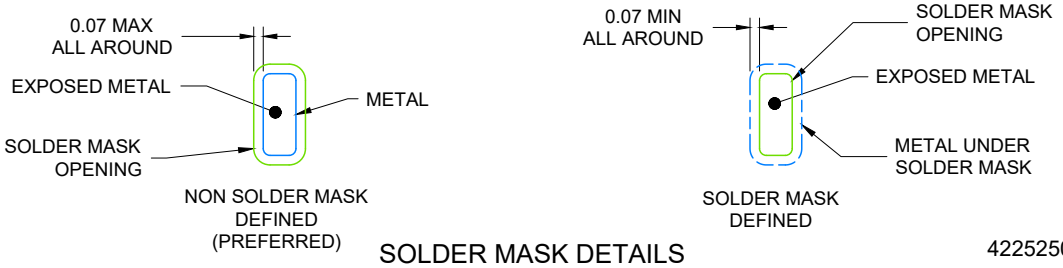


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X



SOLDER MASK DETAILS

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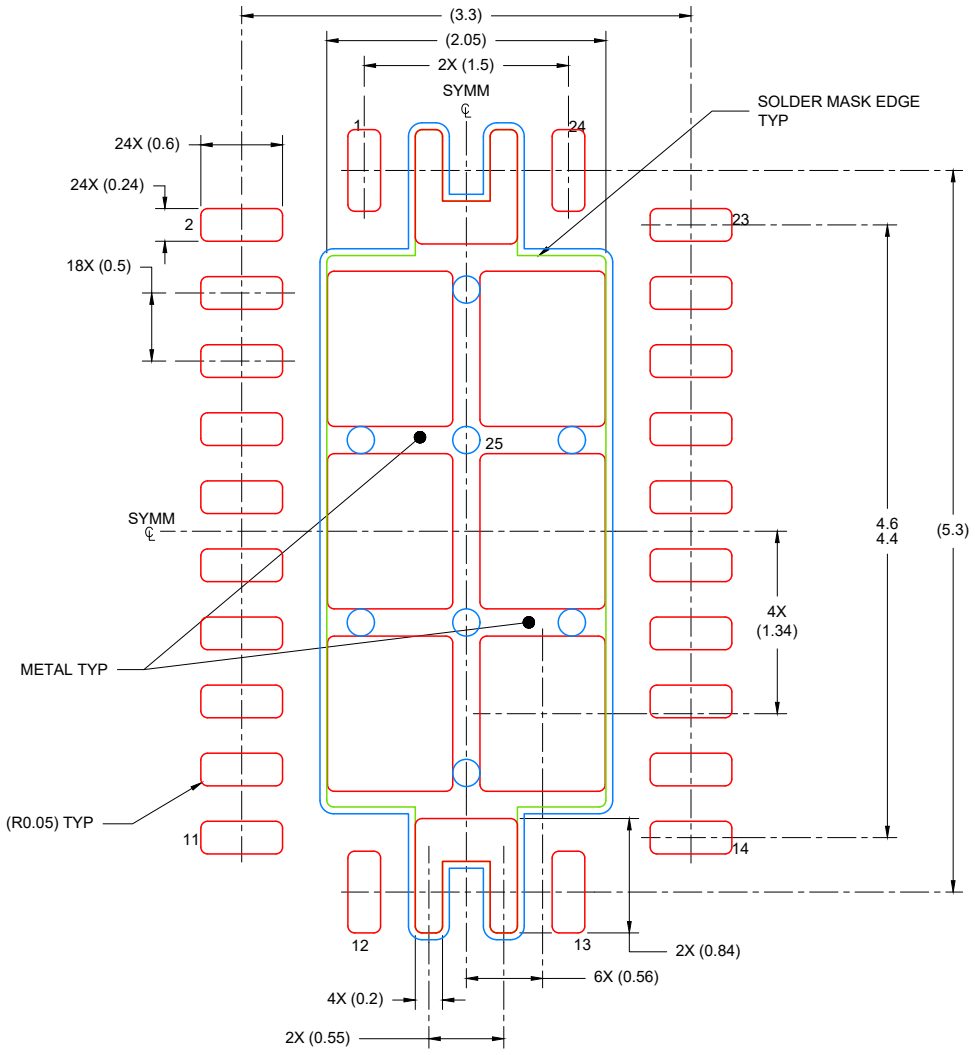
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 18X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月