# SN74AVC8T245-Q1 構成可能な電圧レベル変換および 3 ステート出力搭載、車載用、8 ビット、両電源、バス トランシーバ

## 1 特長

- 車載アプリケーション向けに認定済み
- AEC-Q100 テスト ガイダンスにおいて以下の結果:
  - デバイス温度グレード 1:-40℃～+125℃の動作時周囲温度範囲
  - デバイス HBM ESD 分類レベル H2
  - デバイス CDM ESD 分類レベル C3B
- $V_{CCA}$ 電圧基準の制御入力 $V_{IH}/V_{IL}$ レベル
- $V_{CC}$ 絶縁機能:いずれかの $V_{CC}$ 入力が GND レベルになると、すべての出力がハイ インピーダンス状態に移行
- $I_{off}$ により部分的パワーダウン モードでの動作をサポート
- 完全に構成可能なデュアル レール設計により、1.4V～3.6V の電源電圧の全範囲にわたって各ポートが動作可能
- 4.6V 許容の I/O
- データ レート (最大値):
  - 170Mbps ($V_{CCA}$ < 1.8V または $V_{CCB}$ < 1.8V)
  - 320Mbps ($V_{CCA}$ ≧ 1.8V および $V_{CCB}$ ≧ 1.8V)
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能

## 2 アプリケーション

- テレマティクス
- クラスタ
- ヘッド・ユニット
- ナビゲーション システム

## 3 概要

SN74AVC8T245-Q1 は、設定可能な 2 本の独立した電源レールを採用した 8 ビット非反転バス・トランシーバです。SN74AVC8T245-Q1 の動作は $V_{CCA}$ および $V_{CCB}$ を 1.4V～3.6V に設定して動作させるのが最適です。本デバイスは、$V_{CCA}$ および $V_{CCB}$ がわずか 1.2V で動作します。A ポートは、$V_{CCA}$ をトラッキングするように設計されています。$V_{CCA}$ は 1.2V～3.6V の電源電圧に対応します。B ポートは $V_{CCB}$ に追従する設計で、$V_{CCB}$ には、1.2 V～3.6V 範囲の任意の電源電圧を供給できます。このため、1.2V、1.5V、1.8V、2.5V、3.3V の任意の電圧ノード間で、低電圧の双方向レベル変換を自在に行うことが可能です。

SN74AVC8T245-Q1 の設計により、複数のデータ バス間の非同期通信が可能になります。このデバイスは、方向制御 (DIR) 入力の論理レベルに応じて、A バスから B バス、または B バスから A バスへデータを転送します。出力イネーブル ($\overline{OE}$) 入力を使用して出力をディセーブルにすることにより、バスを実質的に絶縁できます。

SN74AVC8T245-Q1 の設計では、$V_{CCA}$ により制御ピン (DIR および $\overline{OE}$) に電力供給されます。

本デバイス仕様は、$I_{off}$ を使用した部分的パワーダウン アプリケーションを対象としています。$I_{off}$ 回路は、デバイスの電源がオフになったとき、出力をディセーブルにします。これによってデバイスへの電流の逆流を阻止し、デバイスを損傷から保護します。

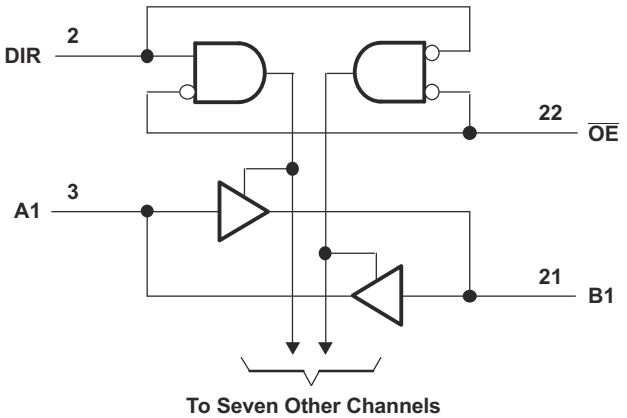
この $V_{CC}$ 絶縁機能により、いずれかの $V_{CC}$ 入力が GND の場合、両方のポートを高インピーダンス状態にすることができます。

電源投入または電源オフの間にデバイスを高インピーダンス状態にするには、$\overline{OE}$ をプルアップ抵抗を介して $V_{CC}$ に接続します。この抵抗の最小値は、ドライバの電流シンク能力によって決まります。

**パッケージ情報**

| 部品番号 | パッケージ(1) | パッケージ サイズ(2) |
|---|---|---|
| SN74AVC8T245-Q1 | RHL (VQFN、24) | 5.5mm × 3.5mm |
| | PW (TSSOP、24) | 7.8mm × 6.4mm |

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。




**論理図 (正論理)**

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# 4 Pin Configuration and Functions

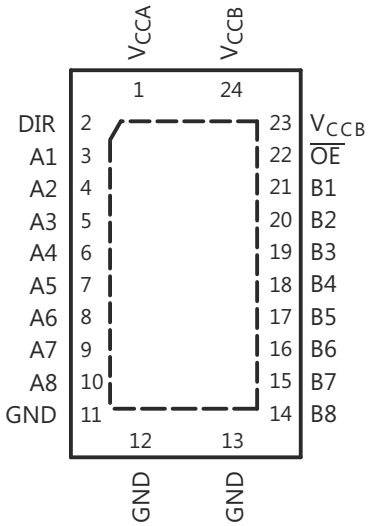



**図 4-1. RHL Package, 24-Pin VQFN (Top View)**

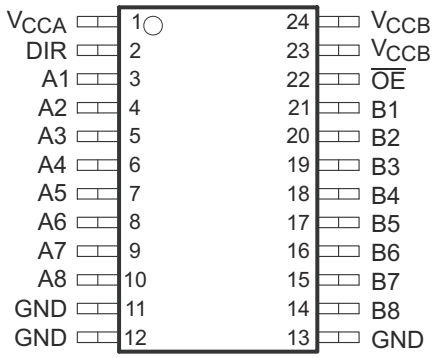



**図 4-2. PW Package, 24-Pin TSSOP (Top View)**

**表 4-1. Pin Functions**

| PIN | | | TYPE(1) | DESCRIPTION |
|---|---|---|---|---|
| NAME | VQFN | TSSOP | | |
| A1 | 3 | 3 | I/O | Input/output A1. Referenced to $V_{CCA}$. |
| A2 | 4 | 4 | I/O | Input/output A2. Referenced to $V_{CCA}$. |
| A3 | 5 | 5 | I/O | Input/output A3. Referenced to $V_{CCA}$. |
| A4 | 6 | 6 | I/O | Input/output A4. Referenced to $V_{CCA}$. |
| A5 | 7 | 7 | I/O | Input/output A5. Referenced to $V_{CCA}$. |
| A6 | 8 | 8 | I/O | Input/output A6. Referenced to $V_{CCA}$. |
| A7 | 9 | 9 | I/O | Input/output A7. Referenced to $V_{CCA}$. |
| A8 | 10 | 10 | I/O | Input/output A8. Referenced to $V_{CCA}$. |
| B1 | 21 | 21 | I/O | Input/output B1. Referenced to $V_{CCB}$. |
| B2 | 20 | 20 | I/O | Input/output B2. Referenced to $V_{CCB}$. |
| B3 | 19 | 19 | I/O | Input/output B3. Referenced to $V_{CCB}$. |
| B4 | 18 | 18 | I/O | Input/output B4. Referenced to $V_{CCB}$. |
| B5 | 17 | 17 | I/O | Input/output B5. Referenced to $V_{CCB}$. |
| B6 | 16 | 16 | I/O | Input/output B6. Referenced to $V_{CCB}$. |
| B7 | 15 | 15 | I/O | Input/output B7. Referenced to $V_{CCB}$. |
| B8 | 14 | 14 | I/O | Input/output B8. Referenced to $V_{CCB}$. |
| DIR | 2 | — | I | Direction-control input for 1 ports |
| GND | 12, 13 | 11, 12, 13 | — | Ground |
| $\overline{OE}$ | 22 | 22 | I | 3-state output-mode enable. Pull $\overline{OE}$ high to place ‘2’ outputs in 3-state mode. Referenced to $V_{CCA}$. |
| $V_{CCA}$ | 1 | 1 | — | A-port power supply voltage. 1.2 V ≤ $V_{CCA}$ ≤ 3.6 V |
| $V_{CCB}$ | 23, 24 | 23, 24 | — | B-port power supply voltage. 1.2 V ≤ $V_{CCB}$ ≤ 3.6 V |
| Thermal pad | | | — | The exposed thermal pad must be connected as a secondary GND or be left electrically open. |

(1) I = input, O = output

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCA}$<br>$V_{CCB}$ | Supply voltage | | –0.5 | 4.6 | V |
| $V_I$ | Input voltage(2) | I/O ports (A port) | –0.5 | 4.6 | V |
| | | I/O ports (B port) | –0.5 | 4.6 | V |
| | | Control inputs | –0.5 | 4.6 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state(2) | A port | –0.5 | 4.6 | V |
| | | B port | –0.5 | 4.6 | V |
| $V_O$ | Voltage range applied to any output in the high or low state(2) (3) | A port | –0.5 | ($V_{CCA}$ + 0.5) | V |
| | | B port | –0.5 | ($V_{CCB}$ + 0.5) | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CCA}$, $V_{CCB}$, or GND | | | ±100 | mA |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The device withstands voltages in excess of input voltage and output negative-voltage ratings while operating within the input and output current ratings.
(3) The device withstands voltages in excess of the output positive-voltage rating up to 4.6 V maximum while operating within the output current rating.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 Classification Level H2(1) | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 Classification Level C3B | ±750 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Recommended Operating Conditions

See (1) (2) (3)

| | | | $V_{CCI}$ | $V_{CCO}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage | | | | 1.2 | 3.6 | V |
| $V_{CCB}$ | Supply voltage | | | | 1.2 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | Data inputs | 1.2 V to 1.95 V | | $V_{CCI}$ × 0.65 | | V |
| | | | 1.95 V to 2.7 V | | 1.6 | | |
| | | | 2.7 V to 3.6 V | | 2 | | |
| $V_{IL}$ | Low-level input voltage | Data inputs | 1.2 V to 1.95 V | | | $V_{CCI}$ × 0.35 | V |
| | | | 1.95 V to 2.7 V | | | 0.7 | |
| | | | 2.7 V to 3.6 V | | | 0.8 | |
| $V_{IH}$ | High-level input voltage | DIR (referenced to $V_{CCA}$) | 1.2 V to 1.95 V | | $V_{CCA}$ × 0.65 | | V |
| | | | 1.95 V to 2.7 V | | 1.6 | | |
| | | | 2.7 V to 3.6 V | | 2 | | |
| $V_{IL}$ | Low-level input voltage | DIR (referenced to $V_{CCA}$) | 1.2 V to 1.95 V | | | $V_{CCA}$ × 0.35 | V |
| | | | 1.95 V to 2.7 V | | | 0.7 | |
| | | | 2.7 V to 3.6 V | | | 0.8 | |
| $V_I$ | Input voltage | | | | 0 | 3.6 | V |
| $V_O$ | Output voltage | Active state | | | 0 | $V_{CCO}$ | V |
| | | 3-state | | | 0 | 3.6 | |
| $I_{OH}$ | High-level output current | | | 1.2 V | | –3 | mA |
| | | | | 1.4 V to 1.6 V | | –6 | |
| | | | | 1.65 V to 1.95 V | | –8 | |
| | | | | 2.3 V to 2.7 V | | –9 | |
| | | | | 3 V to 3.6 V | | –12 | |
| $I_{OL}$ | Low-level output current | | | 1.2 V | | 3 | mA |
| | | | | 1.4 V to 1.6 V | | 6 | |
| | | | | 1.65 V to 1.95 V | | 8 | |
| | | | | 2.3 V to 2.7 V | | 9 | |
| | | | | 3 V to 3.6 V | | 12 | |
| $\Delta t / \Delta v$ | Input transition rise or fall rate | | | | | 5 | ns / V |
| $T_A$ | Operating free-air temperature | | | | –40 | 125 | °C |

(1) $V_{CCI}$ is the $V_{CC}$ associated with the input port.
(2) $V_{CCO}$ is the $V_{CC}$ associated with the output port.
(3) Hold all unused data inputs of the device at $V_{CCI}$ or GND for proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

## 5.4 Thermal Information

| THERMAL METRIC | | SN74AVC8T245-Q1 | | UNIT |
|---|---|---|---|---|
| | | RHL (VQFN) | PW (TSSOP) | |
| | | 24 PINS | 24 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 36.8 | 93.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 32.5 | 36.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 15.7 | 48.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.7 | 93.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 15.6 | 48.0 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 5.6 | N/A | °C/W |

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)(2) (1)

| PARAMETER | | TEST CONDITIONS | | $V_{CCA}$ | $V_{CCB}$ | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OH}$ = –100 µA | $V_I = V_{IH}$ | 1.2 V to 3.6 V | 1.2 V to 3.6 V | $T_A$ = –40°C to +125°C | $V_{CCO}$ – 0.2 | | | V |
| | | $I_{OH}$ = –3 mA | | 1.2 V | 1.2 V | $T_A$ = 25°C | | 0.95 | | |
| | | $I_{OH}$ = –6 mA | | 1.4 V | 1.4 V | $T_A$ = –40°C to +125°C | 1 | | | |
| | | $I_{OH}$ = –8 mA | | 1.65 V | 1.65 V | $T_A$ = –40°C to +125°C | 1.2 | | | |
| | | $I_{OH}$ = –9 mA | | 2.3 V | 2.3 V | $T_A$ = –40°C to +125°C | 1.75 | | | |
| | | $I_{OH}$ = –12 mA | | 3 V | 3 V | $T_A$ = –40°C to +125°C | 2.3 | | | |
| $V_{OL}$ | | $I_{OL}$ = 100 µA | $V_I = V_{IL}$ | 1.2 V to 3.6 V | 1.2 V to 3.6 V | $T_A$ = –40°C to +125°C | | | 0.2 | V |
| | | $I_{OL}$ = 3 mA | | 1.2 V | 1.2 V | $T_A$ = 25°C | | 0.15 | | |
| | | $I_{OL}$ = 6 mA | | 1.4 V | 1.4 V | $T_A$ = –40°C to +125°C | | | 0.35 | |
| | | $I_{OL}$ = 8 mA | | 1.65 V | 1.65 V | $T_A$ = –40°C to +125°C | | | 0.45 | |
| | | $I_{OL}$ = 9 mA | | 2.3 V | 2.3 V | $T_A$ = –40°C to +125°C | | | 0.55 | |
| | | $I_{OL}$ = 12 mA | | 3 V | 3 V | $T_A$ = –40°C to +125°C | | | 0.7 | |
| $I_I$ | Control inputs | $V_I = V_{CCA}$ or GND | | 1.2 V to 3.6 V | 1.2 V to 3.6 V | $T_A$ = 25°C | | ±0.025 | ±0.25 | µA |
| | | | | | | $T_A$ = –40°C to +125°C | | | ±1 | |
| $I_{off}$ | A or B port | $V_I$ or $V_O$ = 0 to 3.6 V | | 0 V | 0 V to 3.6 V | $T_A$ = 25°C | | ±0.1 | ±1 | µA |
| | | | | | | $T_A$ = –40°C to +125°C | | | ±5 | |
| | | | | 0 V to 3.6 V | 0 V | $T_A$ = 25°C | | ±0.1 | ±1 | |
| | | | | | | $T_A$ = –40°C to +125°C | | | ±5 | |
| $I_{OZ}$ (3) | A or B port | $V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$ | | 3.6 V | 3.6 V | $T_A$ = 25°C | | ±0.5 | ±2.5 | µA |
| | | | | | | $T_A$ = –40°C to +125°C | | | ±5 | |

## 5.5 Electrical Characteristics (続き)

over recommended operating free-air temperature range (unless otherwise noted)(2) (1)

| PARAMETER | | TEST CONDITIONS | $V_{CCA}$ | $V_{CCB}$ | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $I_{CCA}$ | | $V_I$ = $V_{CCI}$ or GND(3), $I_O$ = 0 | 1.2 V to 3.6 V | 1.2 V to 3.6 V | $T_A$ = –40°C to +125°C | | | 15 | µA |
| | | | 0 V | 3.6 V | $T_A$ = –40°C to +125°C | | | –2 | |
| | | | 3.6 V | 0 V | $T_A$ = –40°C to +125°C | | | 15 | |
| $I_{CCB}$ | | $V_I$ = $V_{CCI}$ or GND(3), $I_O$ = 0 | 1.2 V to 3.6 V | 1.2 V to 3.6 V | $T_A$ = –40°C to +125°C | | | 15 | µA |
| | | | 0 V | 3.6 V | $T_A$ = –40°C to +125°C | | | 15 | |
| | | | 3.6 V | 0 V | $T_A$ = –40°C to +125°C | | | –2 | |
| $I_{CCA}$ + $I_{CCB}$ | | $V_I$ = $V_{CCI}$ or GND, $I_O$ = 0 | 1.2 V to 3.6 V | 1.2 V to 3.6 V | $T_A$ = –40°C to +125°C | | | 25 | µA |
| $C_i$ | Control inputs | $V_I$ = 3.3 V or GND | 3.3 V | 3.3 V | $T_A$ = 25°C | | 3.5 | | pF |
| $C_{io}$ | A or B port | $V_O$ = 3.3 V or GND | 3.3 V | 3.3 V | $T_A$ = 25°C | | 6 | | pF |

(1) $V_{CCI}$ is the $V_{CC}$ associated with the input port.
(2) $V_{CCO}$ is the $V_{CC}$ associated with the output port.
(3) For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.

## 5.6 Switching Characteristics: $V_{CCA}$ = 1.2 V

over recommended operating free-air temperature range, $V_{CCA}$ = 1.2 V (see 図 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | A | B | $V_{CCB}$ = 1.2 V | 3.1 | ns |
| | | | $V_{CCB}$ = 1.5 V | 2.6 | |
| | | | $V_{CCB}$ = 1.8 V | 2.5 | |
| | | | $V_{CCB}$ = 2.5 V | 3 | |
| | | | $V_{CCB}$ = 3.3 V | 3.5 | |
| $t_{PLH}$, $t_{PHL}$ | B | A | $V_{CCB}$ = 1.2 V | 3.1 | ns |
| | | | $V_{CCB}$ = 1.5 V | 2.7 | |
| | | | $V_{CCB}$ = 1.8 V | 2.5 | |
| | | | $V_{CCB}$ = 2.5 V | 2.4 | |
| | | | $V_{CCB}$ = 3.3 V | 2.3 | |
| $t_{PZH}$, $t_{PZL}$ | $\overline{OE}$ | A | $V_{CCB}$ = 1.2 V | 5.3 | ns |
| | | | $V_{CCB}$ = 1.5 V | | |
| | | | $V_{CCB}$ = 1.8 V | | |
| | | | $V_{CCB}$ = 2.5 V | | |
| | | | $V_{CCB}$ = 3.3 V | | |
| $t_{PZH}$, $t_{PZL}$ | $\overline{OE}$ | B | $V_{CCB}$ = 1.2 V | 5.1 | ns |
| | | | $V_{CCB}$ = 1.5 V | 4 | |
| | | | $V_{CCB}$ = 1.8 V | 3.5 | |
| | | | $V_{CCB}$ = 2.5 V | 3.2 | |
| | | | $V_{CCB}$ = 3.3 V | 3.1 | |

## 5.6 Switching Characteristics: $V_{CCA}$ = 1.2 V (続き)

over recommended operating free-air temperature range, $V_{CCA}$ = 1.2 V (see 図 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $t_{PHZ}$, $t_{PLZ}$ | $\overline{OE}$ | A | $V_{CCB}$ = 1.2 V | 4.8 | ns |
| | | | $V_{CCB}$ = 1.5 V | | |
| | | | $V_{CCB}$ = 1.8 V | | |
| | | | $V_{CCB}$ = 2.5 V | | |
| | | | $V_{CCB}$ = 3.3 V | | |
| $t_{PHZ}$, $t_{PLZ}$ | $\overline{OE}$ | B | $V_{CCB}$ = 1.2 V | 4.7 | ns |
| | | | $V_{CCB}$ = 1.5 V | 4 | |
| | | | $V_{CCB}$ = 1.8 V | 4.1 | |
| | | | $V_{CCB}$ = 2.5 V | 4.3 | |
| | | | $V_{CCB}$ = 3.3 V | 5.1 | |

## 5.7 Switching Characteristics: $V_{CCA}$ = 1.5 V ± 0.1 V

over recommended operating free-air temperature range, $V_{CCA}$ = 1.5 V ± 0.1 V (see 図 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | A | B | $V_{CCB}$ = 1.2 V | | 3.1 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 14.7 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 13.3 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 13.9 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 17.2 | |
| $t_{PLH}$, $t_{PHL}$ | B | A | $V_{CCB}$ = 1.2 V | | 3.1 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 14.7 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 14.2 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 13.5 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 13.2 | |
| $t_{PZH}$, $t_{PZL}$ | $\overline{OE}$ | A | $V_{CCB}$ = 1.2 V | | 5.3 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 20.5 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 20.5 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 20.5 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 20.5 | |
| $t_{PZH}$, $t_{PZL}$ | $\overline{OE}$ | B | $V_{CCB}$ = 1.2 V | | 5.1 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 18.6 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 17.7 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 15.1 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 14.4 | |
| $t_{PHZ}$, $t_{PLZ}$ | $\overline{OE}$ | A | $V_{CCB}$ = 1.2 V | | 4.8 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 20.3 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 20.3 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 20.3 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 20.3 | |

## 5.7 Switching Characteristics: $V_{CCA}$ = 1.5 V ± 0.1 V (続き)

over recommended operating free-air temperature range, $V_{CCA}$ = 1.5 V ± 0.1 V (see 図 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PHZ}$, $t_{PLZ}$ | $\overline{OE}$ | B | $V_{CCB}$ = 1.2 V | | 4.7 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 20.0 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 18.6 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 17.9 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 18.9 | |

## 5.8 Switching Characteristics: $V_{CCA}$ = 1.8 V ± 0.15 V

over recommended operating free-air temperature range, $V_{CCA}$ = 1.8 V ± 0.15 V (see 図 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | A | B | $V_{CCB}$ = 1.2 V | | 2.5 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 14.2 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 13.0 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 12.3 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 12.1 | |
| $t_{PLH}$, $t_{PHL}$ | B | A | $V_{CCB}$ = 1.2 V | | 2.5 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 13.3 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 13.0 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 12.1 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 11.8 | |
| $t_{PZH}$, $t_{PZL}$ | $\overline{OE}$ | A | $V_{CCB}$ = 1.2 V | | 3 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 17.2 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 17.2 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 17.2 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 17.2 | |
| $t_{PZH}$, $t_{PZL}$ | $\overline{OE}$ | B | $V_{CCB}$ = 1.2 V | | 4.6 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 19.6 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 17.0 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 14.2 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 13.2 | |
| $t_{PHZ}$, $t_{PLZ}$ | $\overline{OE}$ | A | $V_{CCB}$ = 1.2 V | | 2.8 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 17.7 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 17.7 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 17.7 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 17.7 | |
| $t_{PHZ}$, $t_{PLZ}$ | $\overline{OE}$ | B | $V_{CCB}$ = 1.2 V | | 3.9 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 18.9 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 17.3 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 15.8 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 15.4 | |

## 5.9 Switching Characteristics: $V_{CCA}$ = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, $V_{CCA}$ = 2.5 V ± 0.2 V (see 図 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | A | B | $V_{CCB}$ = 1.2 V | | 2.4 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 13.5 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 12.1 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 10.7 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 10.2 | |
| $t_{PLH}$, $t_{PHL}$ | B | A | $V_{CCB}$ = 1.2 V | | 3 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 13.9 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 12.3 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 10.7 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 10.4 | |
| $t_{PZH}$, $t_{PZL}$ | $\overline{OE}$ | A | $V_{CCB}$ = 1.2 V | | 2.2 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 13.7 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 13.7 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 13.7 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 13.7 | |
| $t_{PZH}$, $t_{PZL}$ | $\overline{OE}$ | B | $V_{CCB}$ = 1.2 V | | 4.5 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 19.1 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 16.5 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 13.3 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 12.3 | |
| $t_{PHZ}$, $t_{PLZ}$ | $\overline{OE}$ | A | $V_{CCB}$ = 1.2 V | | 1.8 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 14.2 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 14.2 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 14.2 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 14.2 | |
| $t_{PHZ}$, $t_{PLZ}$ | $\overline{OE}$ | B | $V_{CCB}$ = 1.2 V | | 3.6 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 17.7 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 16.3 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 14.2 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 12.1 | |

## 5.10 Switching Characteristics: $V_{CCA}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, $V_{CCA}$ = 3.3 V ± 0.3 V (see 図 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | A | B | $V_{CCB}$ = 1.2 V | | 2.3 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 13.2 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 11.1 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 10.4 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 9.7 | |

## 5.10 Switching Characteristics: $V_{CCA}$ = 3.3 V ± 0.3 V (続き)

over recommended operating free-air temperature range, $V_{CCA}$ = 3.3 V ± 0.3 V (see 図 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | B | A | $V_{CCB}$ = 1.2 V | | 3.5 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 17.2 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 12.1 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 10.2 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 9.7 | |
| $t_{PZH}$, $t_{PZL}$ | $\overline{OE}$ | A | $V_{CCB}$ = 1.2 V | | 2 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 12.3 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 12.3 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 12.3 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 12.3 | |
| $t_{PZH}$, $t_{PZL}$ | $\overline{OE}$ | B | $V_{CCB}$ = 1.2 V | | 4.5 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 18.9 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 16.1 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 13.2 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 12.3 | |
| $t_{PHZ}$, $t_{PLZ}$ | $\overline{OE}$ | A | $V_{CCB}$ = 1.2 V | | 1.7 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 12.3 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 12.3 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 12.3 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 12.3 | |
| $t_{PHZ}$, $t_{PLZ}$ | $\overline{OE}$ | B | $V_{CCB}$ = 1.2 V | | 3.4 | | ns |
| | | | $V_{CCB}$ = 1.5 V ± 0.1 V | 0.5 | | 17.4 | |
| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | 0.5 | | 15.8 | |
| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | 0.5 | | 13.7 | |
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | 0.5 | | 12.6 | |

## 5.11 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | $V_{CCA}$ | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pdA}$ (1) | A to B | Outputs enabled | $C_L$ = 0, f = 10 MHz, $t_r$ = $t_f$ = 1 ns | $V_{CCA}$ = $V_{CCB}$ = 1.2 V | 1 | pF |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 1.5 V | | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 1.8 V | | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 2.5 V | | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 3.3 V | | |
| | | Outputs disabled | $C_L$ = 0, f = 10 MHz, $t_r$ = $t_f$ = 1 ns | $V_{CCA}$ = $V_{CCB}$ = 1.2 V | 1 | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 1.5 V | | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 1.8 V | | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 2.5 V | | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 3.3 V | | |
| | B to A | Outputs enabled | $C_L$ = 0, f = 10 MHz, $t_r$ = $t_f$ = 1 ns | $V_{CCA}$ = $V_{CCB}$ = 1.2 V | 12 | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 1.5 V | 12 | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 1.8 V | 12 | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 2.5 V | 13 | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 3.3 V | 14 | |
| | | Outputs disabled | $C_L$ = 0, f = 10 MHz, $t_r$ = $t_f$ = 1 ns | $V_{CCA}$ = $V_{CCB}$ = 1.2 V | 1 | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 1.5 V | | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 1.8 V | | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 2.5 V | | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 3.3 V | | |
| $C_{pdB}$ (1) | A to B | Outputs enabled | $C_L$ = 0, f = 10 MHz, $t_r$ = $t_f$ = 1 ns | $V_{CCA}$ = $V_{CCB}$ = 1.2 V | 12 | pF |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 1.5 V | 12 | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 1.8 V | 12 | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 2.5 V | 13 | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 3.3 V | 14 | |
| | | Outputs disabled | $C_L$ = 0, f = 10 MHz, $t_r$ = $t_f$ = 1 ns | $V_{CCA}$ = $V_{CCB}$ = 1.2 V | 1 | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 1.5 V | | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 1.8 V | | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 2.5 V | | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 3.3 V | | |
| | B to A | Outputs enabled | $C_L$ = 0, f = 10 MHz, $t_r$ = $t_f$ = 1 ns | $V_{CCA}$ = $V_{CCB}$ = 1.2 V | 1 | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 1.5 V | | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 1.8 V | | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 2.5 V | | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 3.3 V | | |
| | | Outputs disabled | $C_L$ = 0, f = 10 MHz, $t_r$ = $t_f$ = 1 ns | $V_{CCA}$ = $V_{CCB}$ = 1.2 V | 1 | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 1.5 V | | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 1.8 V | | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 2.5 V | | |
| | | | | $V_{CCA}$ = $V_{CCB}$ = 3.3 V | | |

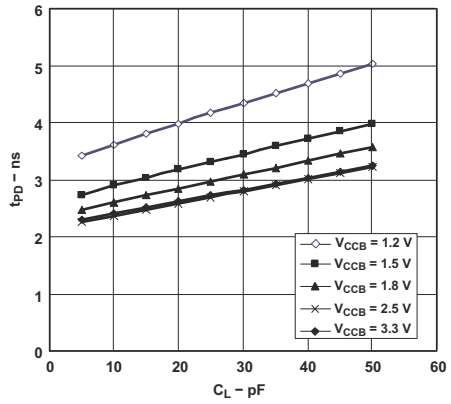
(1) Power dissipation capacitance per transceiver

## 5.12 Typical Total Static Current Consumption ($I_{CCA}$ + $I_{CCB}$)

| $V_{CCB}$ | $V_{CCA}$ | | | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | 0 V | 1.2 V | 1.5 V | 1.8 V | 2.5 V | 3.3 V | |
| **0 V** | 0 | <0.5 | <0.5 | <0.5 | <0.5 | <0.5 | µA |
| **1.2 V** | <0.5 | <1 | <1 | <1 | <1 | 1 | µA |
| **1.5 V** | <0.5 | <1 | <1 | <1 | <1 | 1 | µA |
| **1.8 V** | <0.5 | <1 | <1 | <1 | <1 | <1 | µA |
| **2.5 V** | <0.5 | 1 | <1 | <1 | <1 | <1 | µA |
| **3.3 V** | <0.5 | 1 | <1 | <1 | <1 | <1 | µA |

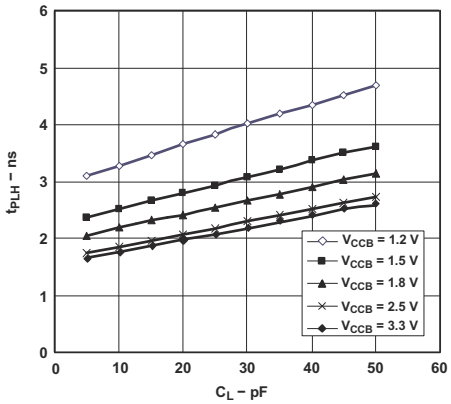
## 5.13 Typical Characteristics

$T_A$ = 25°C



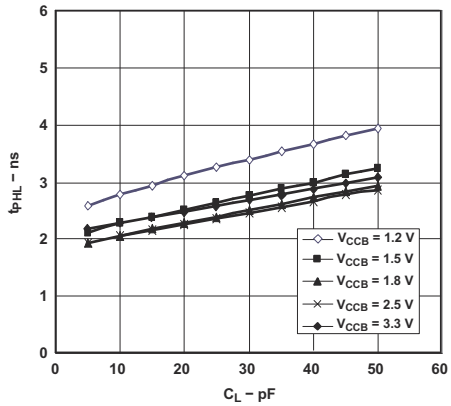

$V_{CCA}$ = 1.2 V

**図 5-1. Typical Propagation Delay (A to B) vs Load Capacitance**



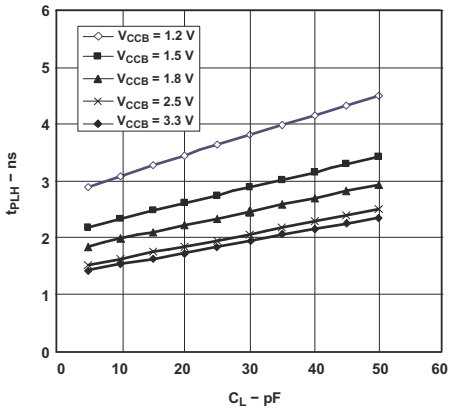

$V_{CCA}$ = 1.5 V

**図 5-2. Typical Propagation Delay (A to B) vs Load Capacitance**



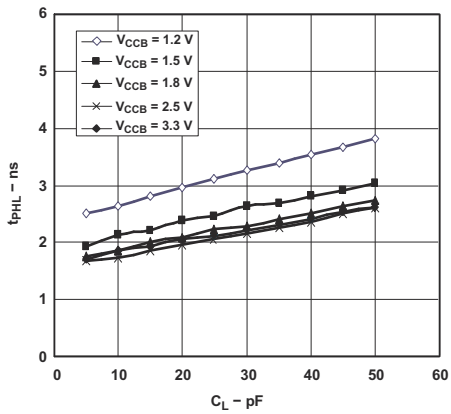

$V_{CCA}$ = 1.5 V

**図 5-3. Typical Propagation Delay (A to B) vs Load Capacitance**



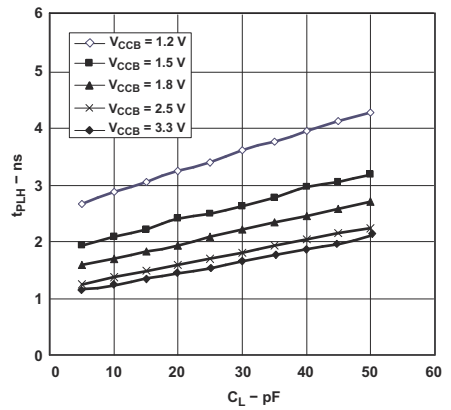

$V_{CCA}$ = 1.8 V

**図 5-4. Typical Propagation Delay (A to B) vs Load Capacitance**




$V_{CCA}$ = 1.8 V

**図 5-5. Typical Propagation Delay (A to B) vs Load Capacitance**

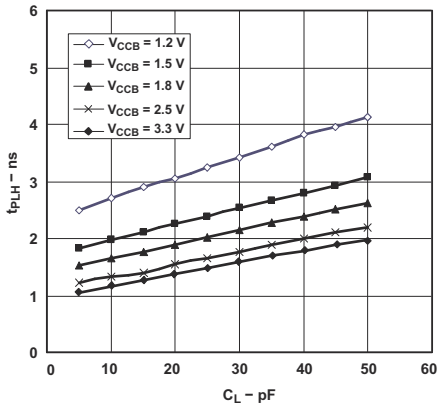



$V_{CCA}$ = 2.5 V

**図 5-6. Typical Propagation Delay (A to B) vs Load Capacitance**

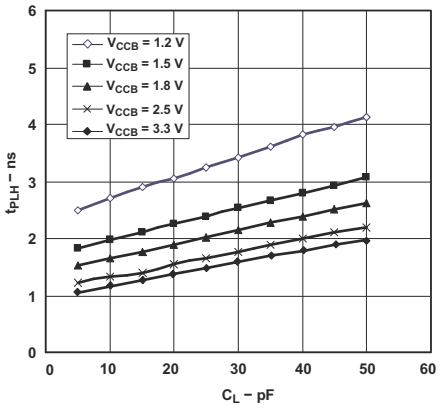
## 5.13 Typical Characteristics (continued)

$T_A$ = 25°C



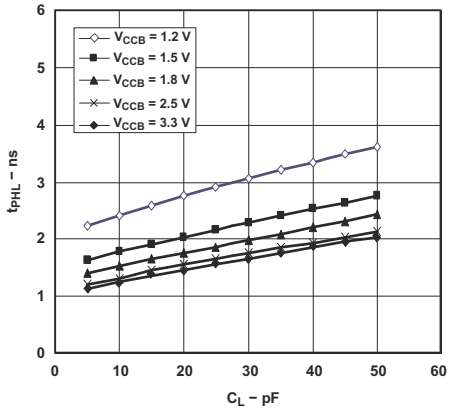

$V_{CCA}$ = 2.5 V

**図 5-7. Typical Propagation Delay (A to B) vs Load Capacitance**




$V_{CCA}$ = 3.3 V

**図 5-8. Typical Propagation Delay (A to B) vs Load Capacitance**




$V_{CCA}$ = 3.3 V

**図 5-9. Typical Propagation Delay (A to B) vs Load Capacitance**

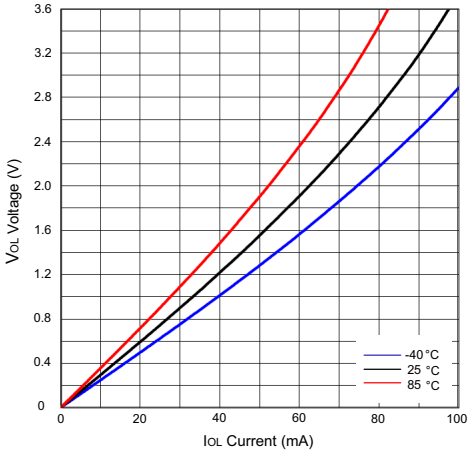



**図 5-10. Low-Level Output Voltage ($V_{OL}$) vs Low-Level Current ($I_{OL}$)**

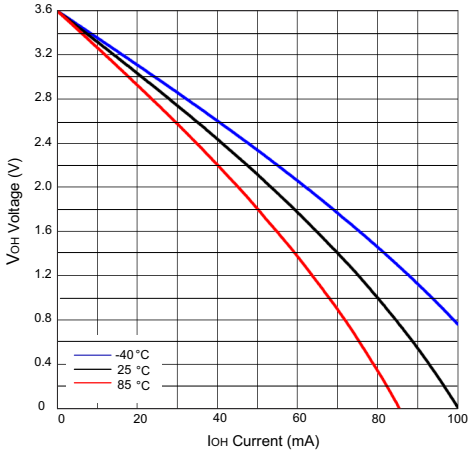
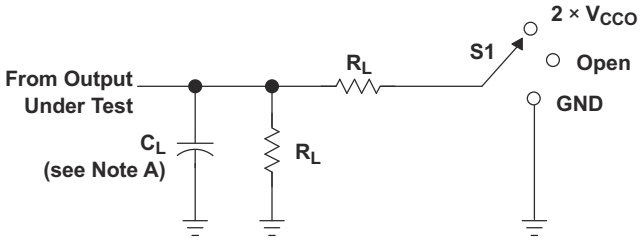



**図 5-11. High-Level Output Voltage ($V_{OH}$) vs High-Level Current ($I_{OH}$)**

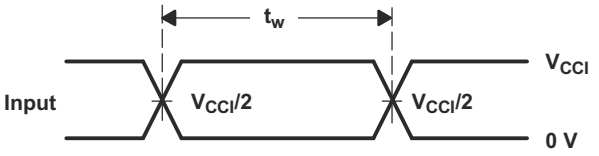
## 6 Parameter Measurement Information



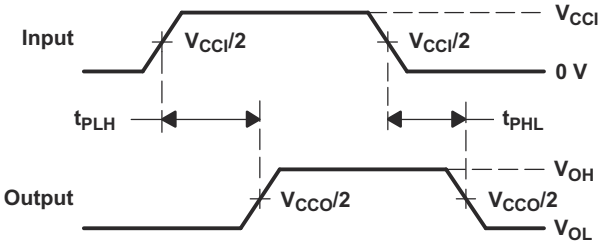

| TEST | S1 |
|---|---|
| $t_{pd}$<br>$t_{PLZ}/t_{PZL}$<br>$t_{PHZ}/t_{PZH}$ | Open<br>2 × $V_{CCO}$<br>GND |

LOAD CIRCUIT

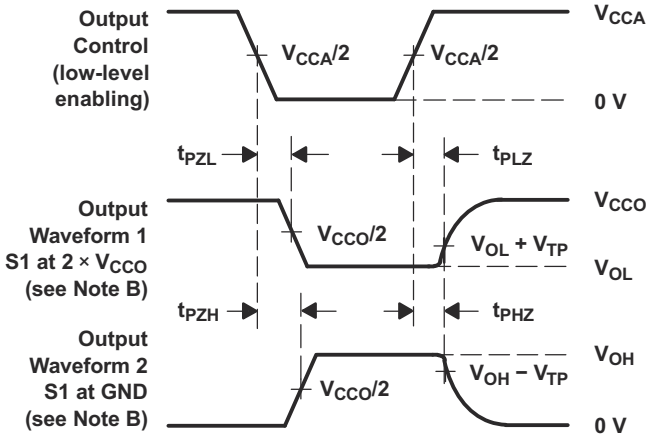
| $V_{CCO}$ | $C_L$ | $R_L$ | $V_{TP}$ |
|---|---|---|---|
| 1.2 V | 15 pF | 2 kΩ | 0.1 V |
| 1.5 V ± 0.1 V | 15 pF | 2 kΩ | 0.1 V |
| 1.8 V ± 0.15 V | 15 pF | 2 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | 15 pF | 2 kΩ | 0.15 V |
| 3.3 V ± 0.3 V | 15 pF | 2 kΩ | 0.3 V |




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. $V_{CCI}$ is the $V_{CC}$ associated with the input port.
I. $V_{CCO}$ is the $V_{CC}$ associated with the output port.

**図 6-1. Load Circuit and Voltage Waveforms**

# 7 Detailed Description

## 7.1 Overview

The SN74AVC8T245-Q1 is an 8-bit, dual-supply noninverting bidirectional voltage level translation device. $V_{CCA}$ supports the Ax pins and control pins (DIR and $\overline{OE}$), and $V_{CCB}$ supports the Bx pins. The A port can accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.2 V to 3.6 V. A high on DIR allows data transmission from Ax to Bx and a low on DIR allows data transmission from Bx to Ax when $\overline{OE}$ is set to low. When $\overline{OE}$ is set to high, both Ax and Bx pins are in the high-impedance state.

## 7.2 Functional Block Diagram

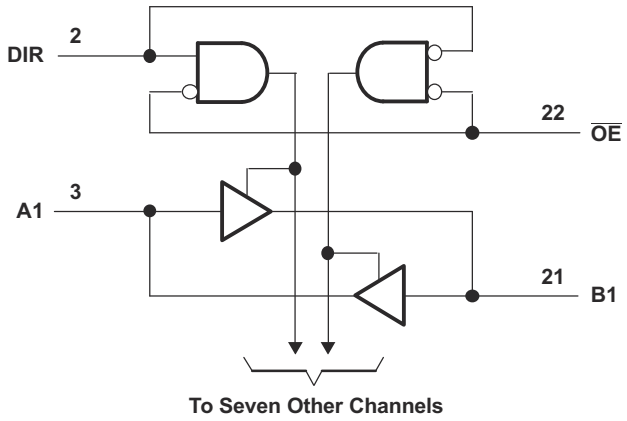



**図 7-1. Logic Diagram (Positive Logic)**

## 7.3 Feature Description

### 7.3.1 Fully Configurable Dual-Rail Design

Both $V_{CCA}$ and $V_{CCB}$ can be supplied at any voltage between 1.2 V and 3.6 V; thus, making the device an excellent choice for translating between any of the low voltage nodes (1.2 V, 1.8 V, 2.5 V, and 3.3 V).

### 7.3.2 Supports High Speed Translation

The SN74AVC8T245-Q1 device can support high data rate applications. The translated signal data rate can be up to 380Mbps when the signal is translated from 1.8 V to 3.3 V.

### 7.3.3 $I_{off}$ Supports Partial-Power-Down Mode Operation

$I_{off}$ prevents backflow current by disabling I/O output circuits when the device is in partial-power-down mode.

## 7.4 Device Functional Modes

表 7-1 lists the functional modes of the device.

**表 7-1. Function Table (Each 8-Bit Section)**

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | All outputs Hi-Z |

# 8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

## 8.1 Application Information

The SN74AVC8T245-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AVC8T245-Q1 device is an excellent choice for applications where a push-pull driver is connected to the data I/Os. The maximum data rate can be up to 320Mbps when the device translates a signal from 1.8 V to 3.3 V.

## 8.2 Typical Application

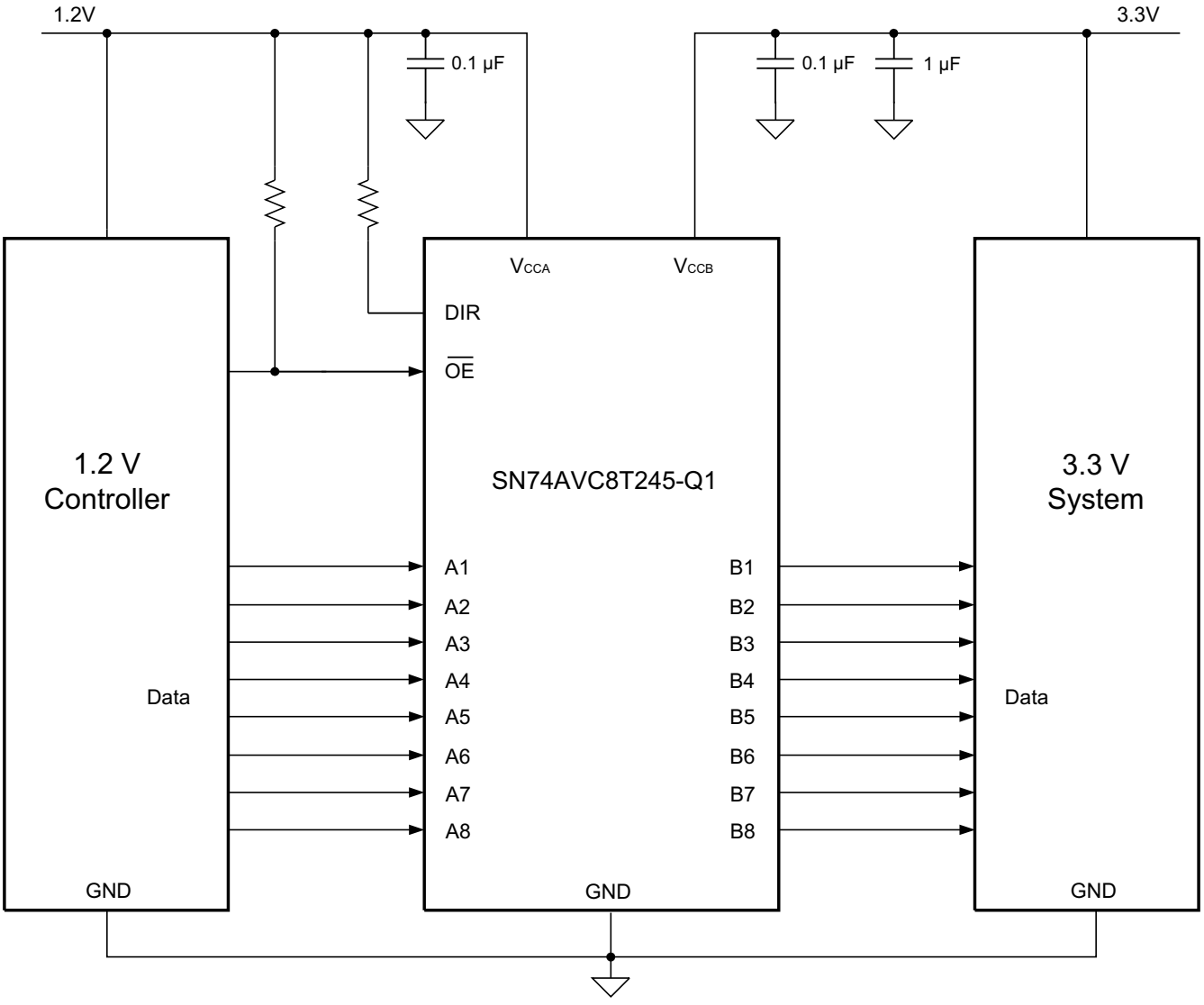



**図 8-1. Typical Application Diagram**

### 8.2.1 Design Requirements

表 8-1 lists the parameters for this design example.

**表 8-1. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage range | 1.2 V |
| Output voltage range | 3.3 V |

### 8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AVC8T245-Q1 device to determine the input voltage range. For a valid logic high, the value must exceed the $V_{IH}$ of the input port. For a valid logic low, the value must be less than the $V_{IL}$ of the input port. For this example, the input voltage is 1.2 V.
- Output voltage range
  - Use the supply voltage of the device that the SN74AVC8T245-Q1 device is driving to determine the output voltage range. For this example, the output voltage is 3.3 V.

### 8.2.3 Application Curve

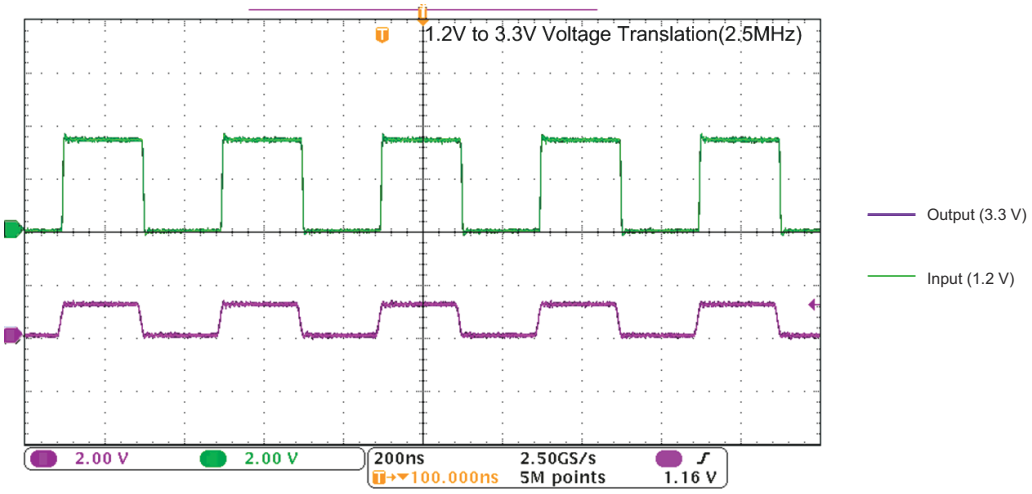



**図 8-2. Translation Up (1.2 V to 3.3 V) at 2.5 MHz**

## 8.3 Power Supply Recommendations

The SN74AVC8T245-Q1 device uses two separate configurable power-supply rails: $V_{CCA}$ and $V_{CCB}$. $V_{CCA}$ accepts any supply voltage from 1.2 V to 3.6 V, and $V_{CCB}$ accepts any supply voltage from 1.2 V to 3.6 V. The A port and B port are designed to track $V_{CCA}$ and $V_{CCB}$ respectively, allowing for low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

$V_{CCA}$ supplies the output-enable ($\overline{OE}$) input circuit in this design; when the $\overline{OE}$ input is high, all outputs are placed in the high-impedance state. To put the outputs in the high-impedance state during power up or power down, the $\overline{OE}$ input pin must be tied to $V_{CCA}$ through a pullup resistor and must not be enabled until $V_{CCA}$ and $V_{CCB}$ are fully ramped and stable. The current-sinking capability of the driver determines the minimum value of the pullup resistor to $V_{CCA}$.

## 8.4 Layout

### 8.4.1 Layout Guidelines

For device reliability, it is recommended to follow common printed-circuit board layout guidelines:

- Use bypass capacitors on power supplies.
- Use short trace lengths to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to adjust signal rise and fall times, depending on the system requirements.

### 8.4.2 Layout Example

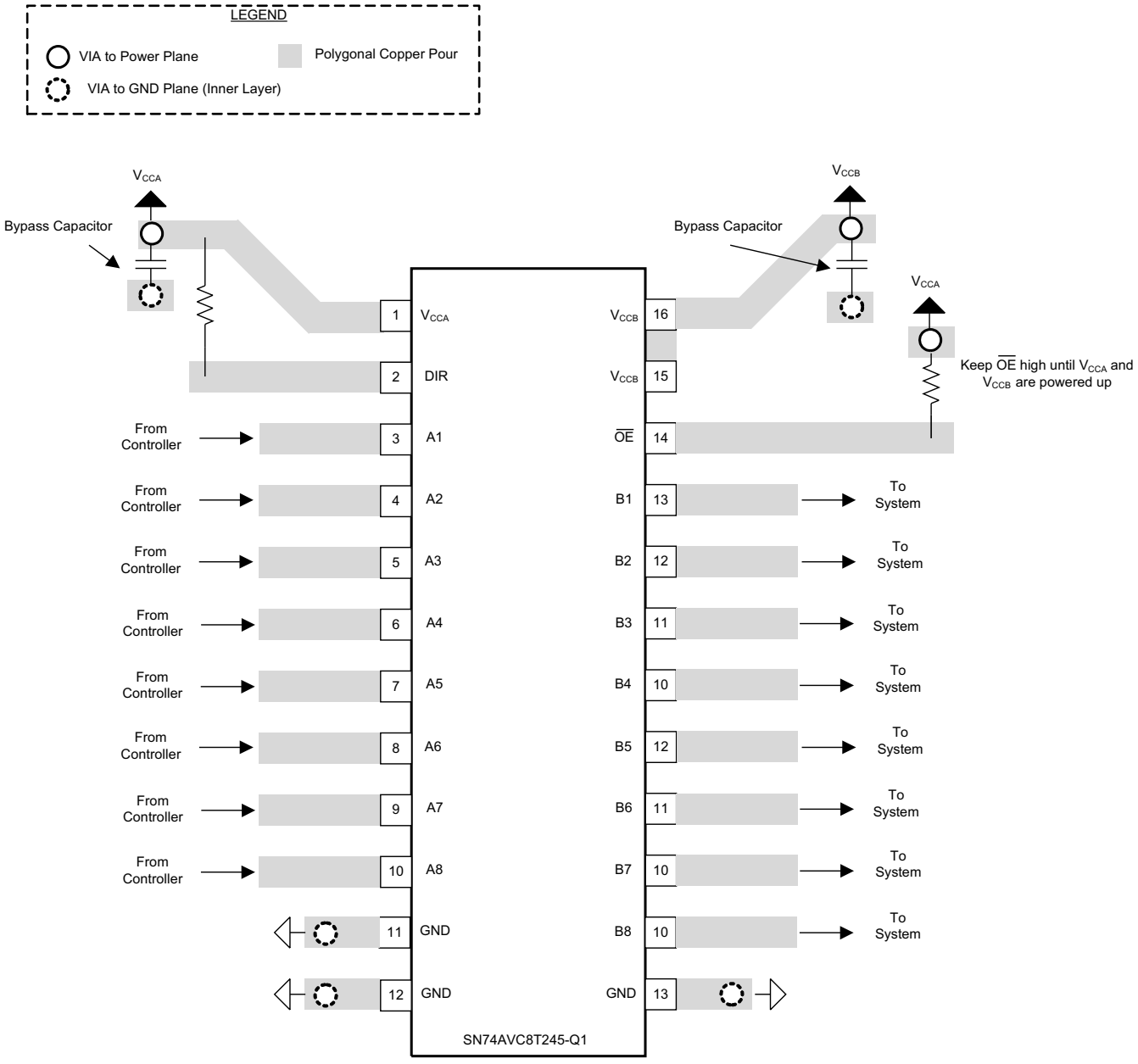



**図 8-3. SN74AVC8T245-Q1 Layout Diagram**

# 9 Device and Documentation Support

## 9.1 Documentation Support

### 9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* Application Note
- Texas Instruments, *Understanding and Interpreting Standard-Logic Data Sheets* Application Note
- Texas Instruments, *Introduction to Logic* Application Note
- Texas Instruments, *Voltage Translation Between 3.3-V, 2.5-V, 1.8-V, and 1.5-V Logic Standards* Application Note
- Texas Instruments, *AVC Advanced Very-Low-Voltage CMOS Logic Data Book* User's Guide

## 9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

## 9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

## 9.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

## 9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

# 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision D (October 2017) to Revision E (November 2023) | Page |
|---|---|
| • 文書全体にわたって表、図、相互参照の採番方法を更新 | 1 |
| • Updated the thermal information for the *RHL* package and updated the information for the *PW* package | 6 |

| Changes from Revision C (March 2016) to Revision D (October 2017) | Page |
|---|---|
| • Added Junction temperature, $T_J$ in *Absolute Maximum Ratings* table | 4 |
| • Deleted 2DIR and 2 $\overline{OE}$ from *Overview* | 17 |

| Changes from Revision B (December 2012) to Revision C (January 2016) | Page |
|---|---|
| • 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。 | 1 |
| • 「注文情報」表を削除 | 1 |

| Changes from Revision A (June 2011) to Revision B (December 2012) | Page |
|---|---|
| • 「特長」リストに複数の箇条書き項目を追加 | 1 |
| • Added *Pin Functions* table to the data sheet | 3 |
| • Deleted $\theta_{JA}$ row from *Absolute Maximum Ratings* table | 4 |
| • Changed ESD ratings | 4 |
| • Added Thermal Information table | 6 |
| • Added Figure 7-10 and Figure 7-11 to the *Typical Characteristics* section | 14 |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| CAVC8T245QRHLRQ1 | Active | Production | VQFN (RHL) \| 24 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | WE245Q |
| CAVC8T245QRHLRQ1.A | Active | Production | VQFN (RHL) \| 24 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | WE245Q |
| CAVC8T245QRHLRQ1.B | Active | Production | VQFN (RHL) \| 24 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | WE245Q |
| SN74AVC8T245QPWRQ1 | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | WE245Q |
| SN74AVC8T245QPWRQ1.A | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | WE245Q |
| SN74AVC8T245QPWRQ1.B | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | WE245Q |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**OTHER QUALIFIED VERSIONS OF SN74AVC8T245-Q1 :**

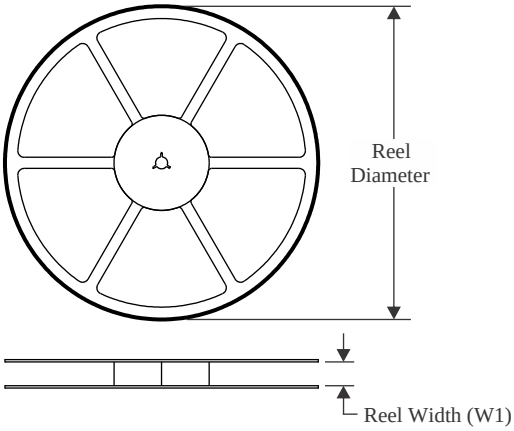
- Catalog : SN74AVC8T245

NOTE: Qualified Version Definitions:

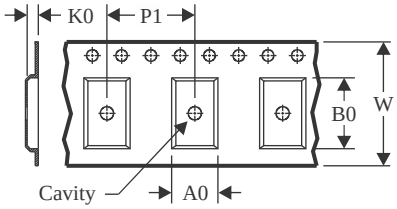
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

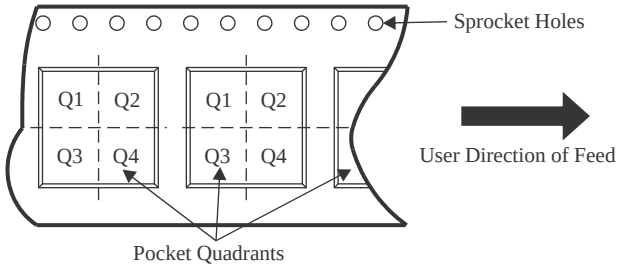



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

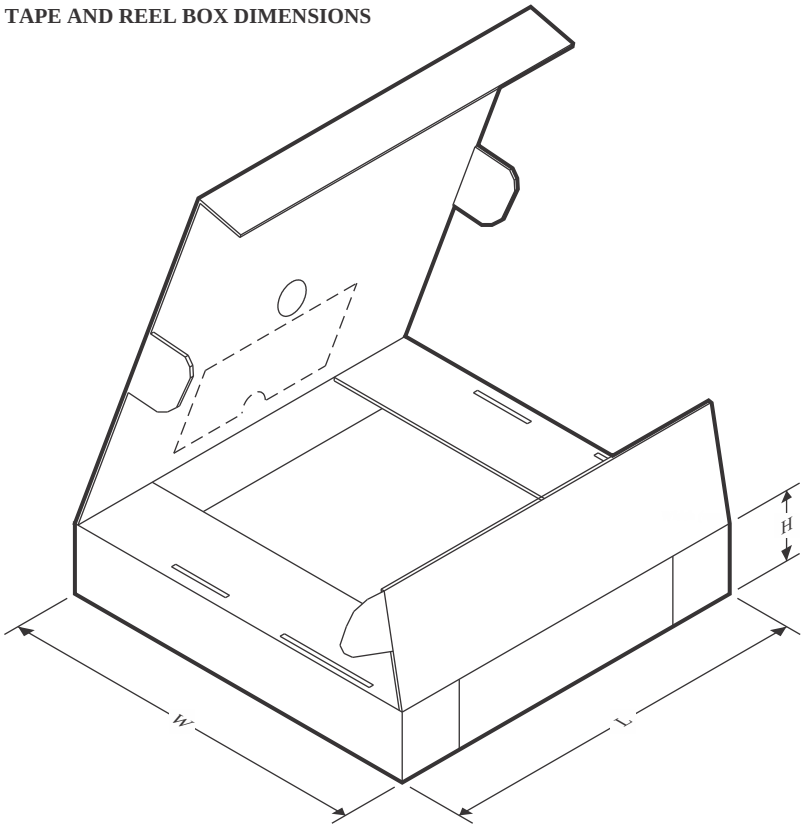
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

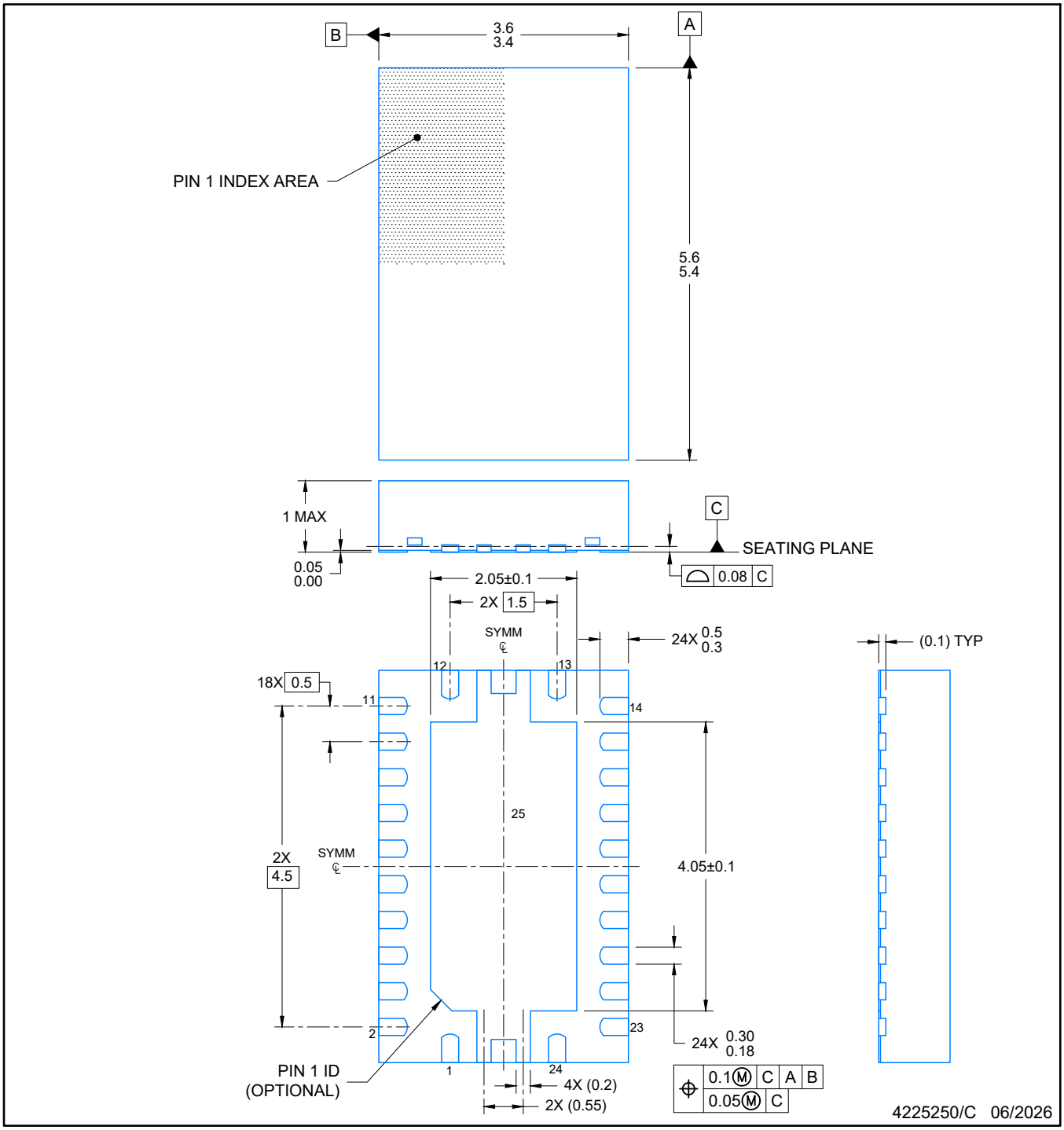
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CAVC8T245QRHLRQ1 | VQFN | RHL | 24 | 1000 | 330.0 | 12.4 | 3.8 | 5.8 | 1.2 | 8.0 | 12.0 | Q1 |
| SN74AVC8T245QPWRQ1 | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



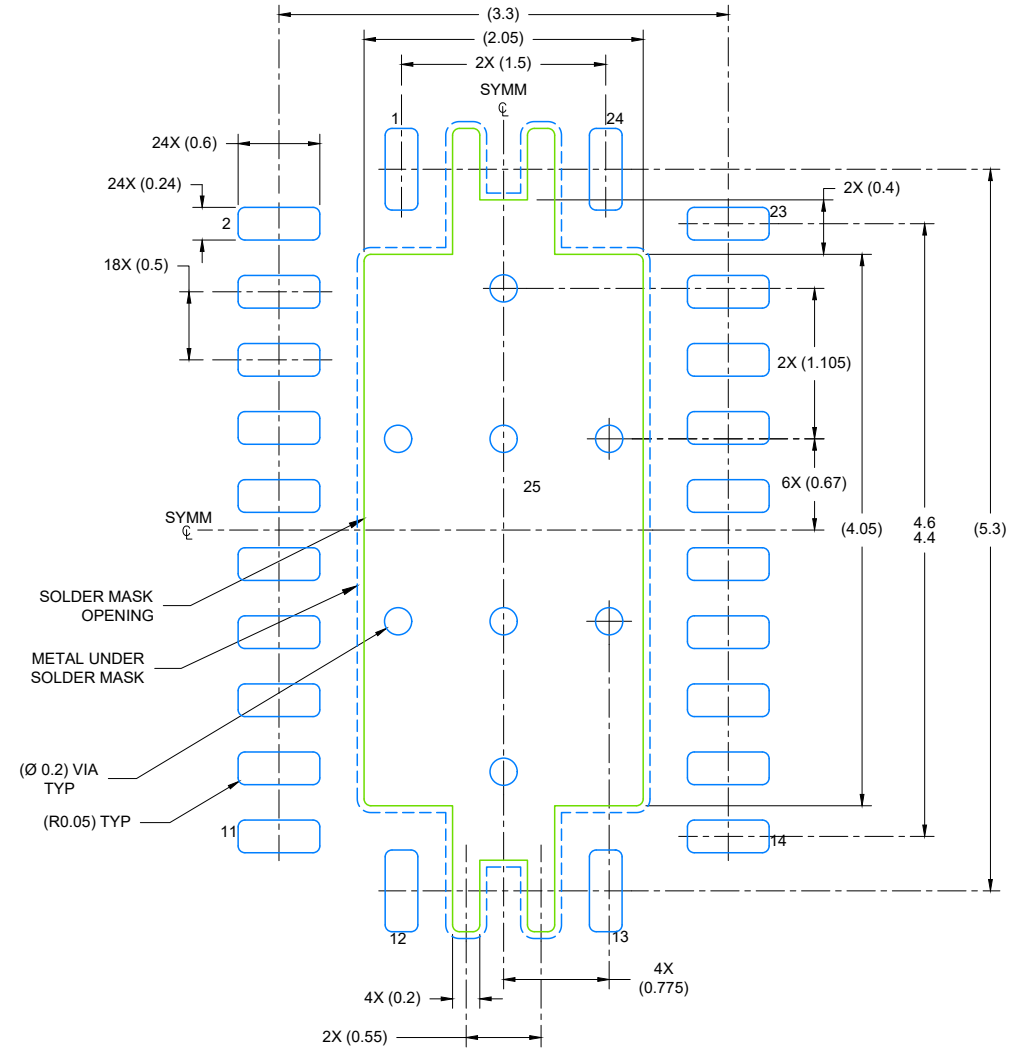

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CAVC8T245QRHLRQ1 | VQFN | RHL | 24 | 1000 | 367.0 | 367.0 | 35.0 |
| SN74AVC8T245QPWRQ1 | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |

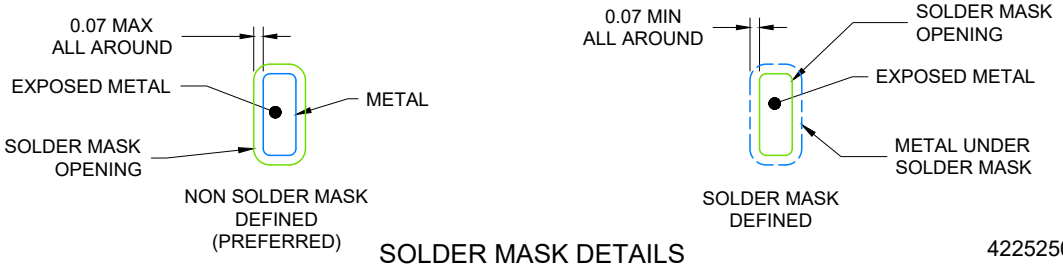



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X

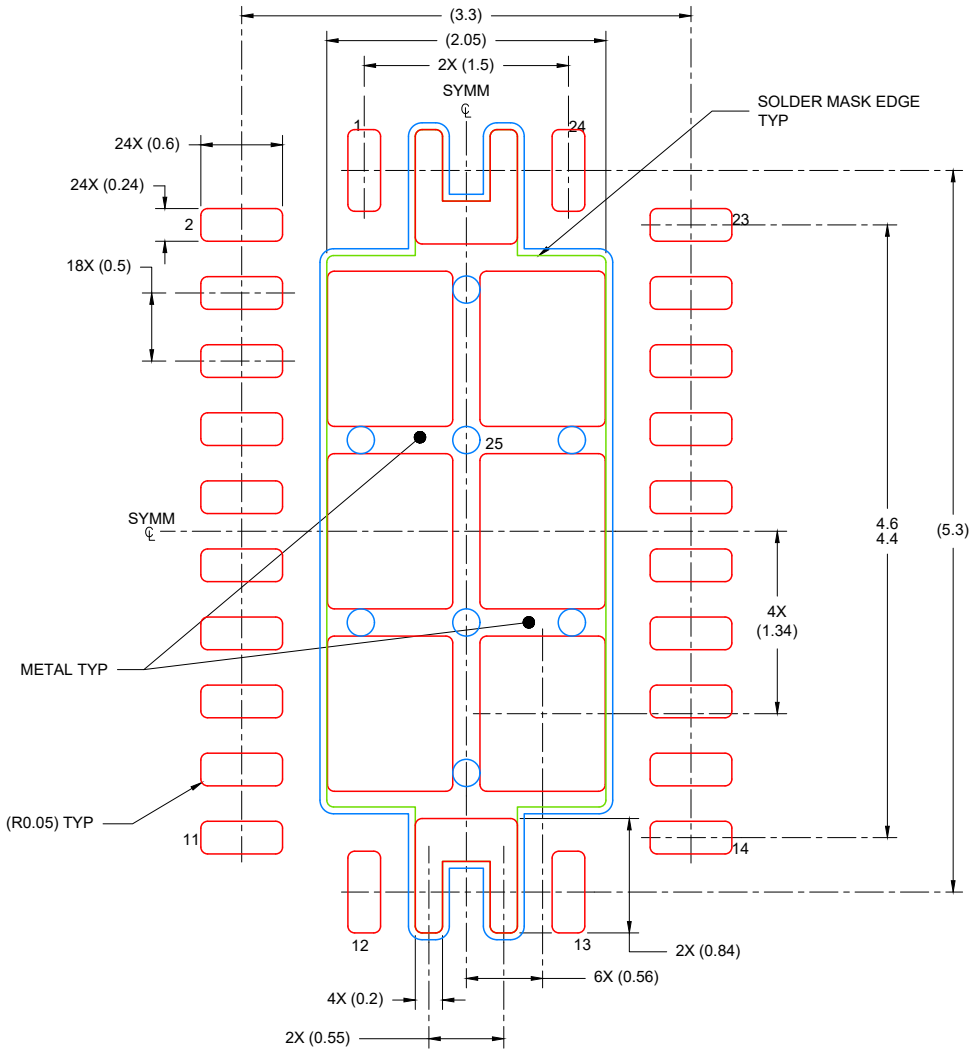



SOLDER MASK DETAILS

4225250/C 06/2026

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 18X

4225250/C 06/2026

NOTES: (continued)

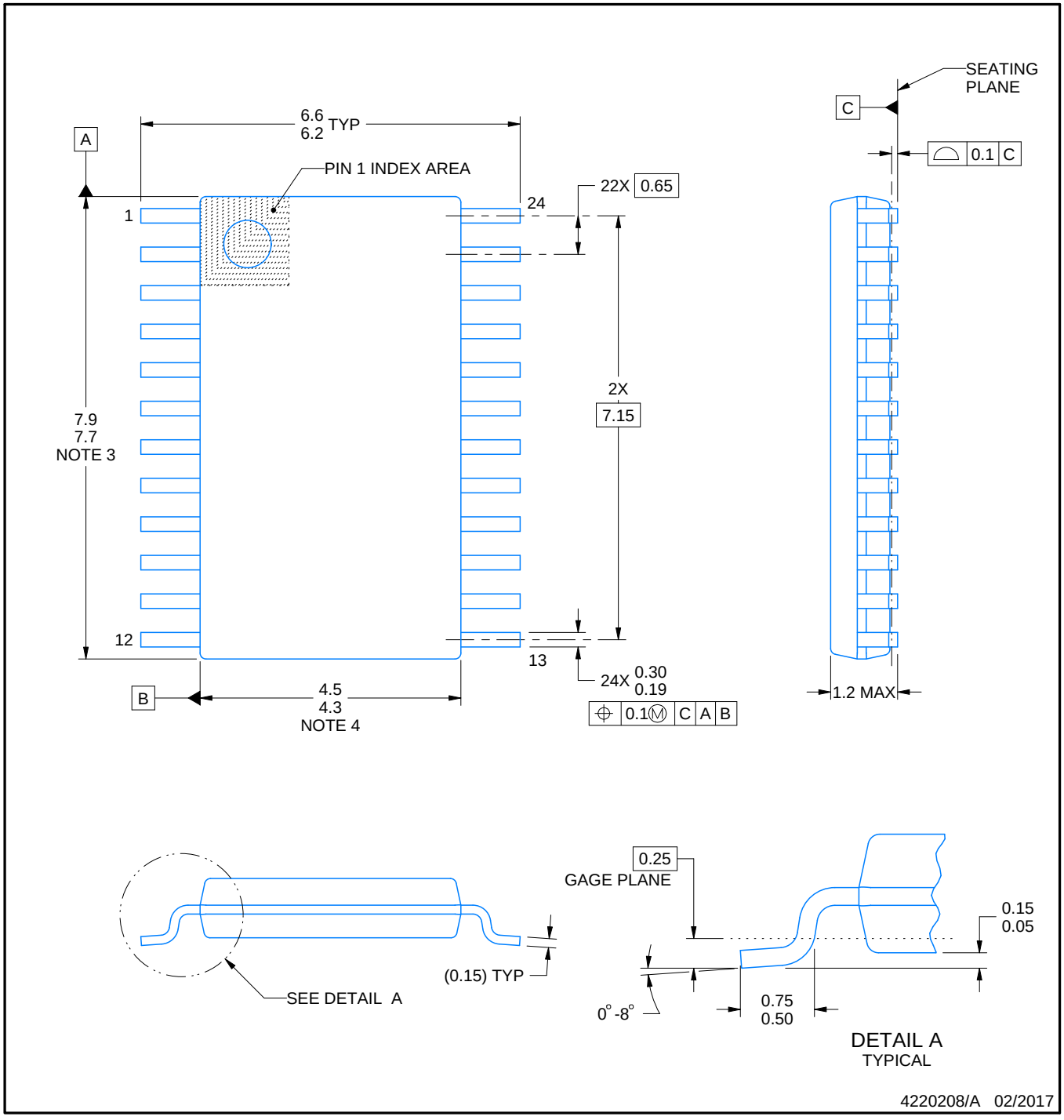
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## PW0024A

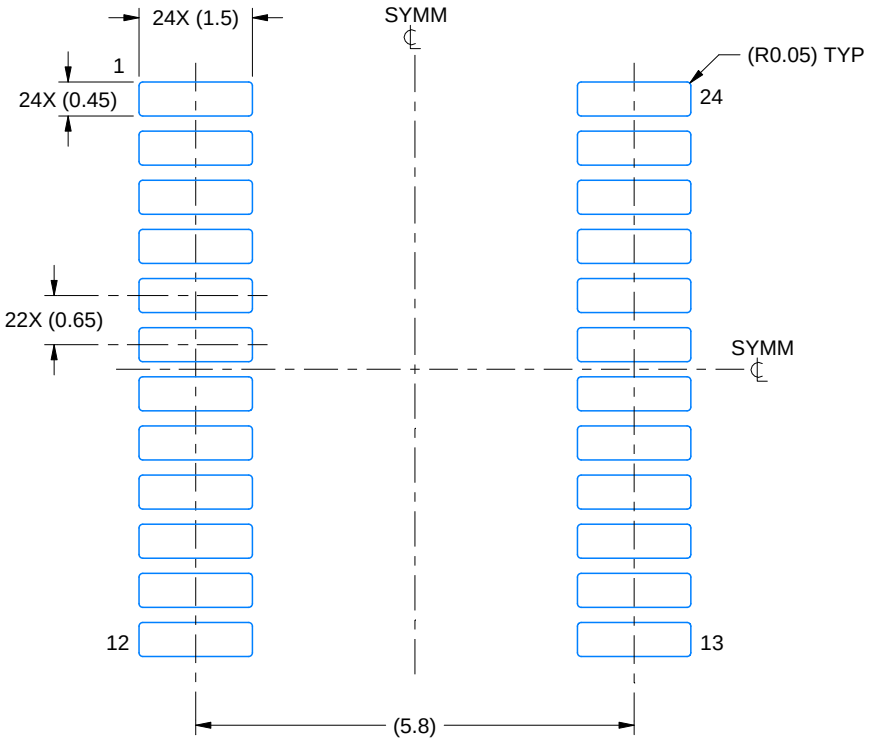
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

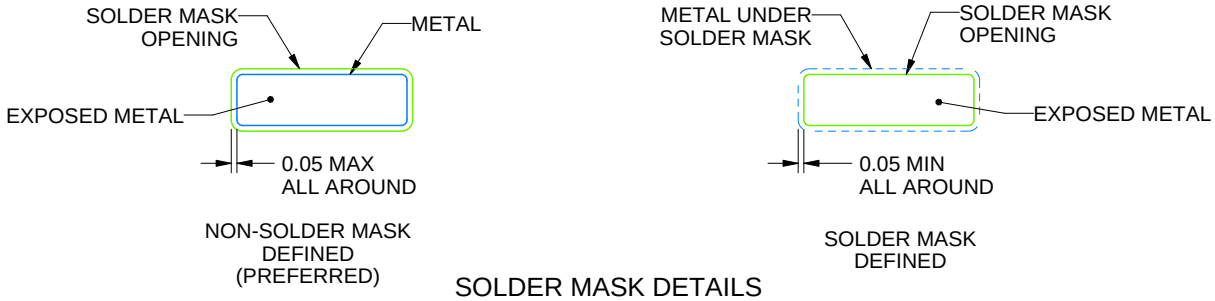



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

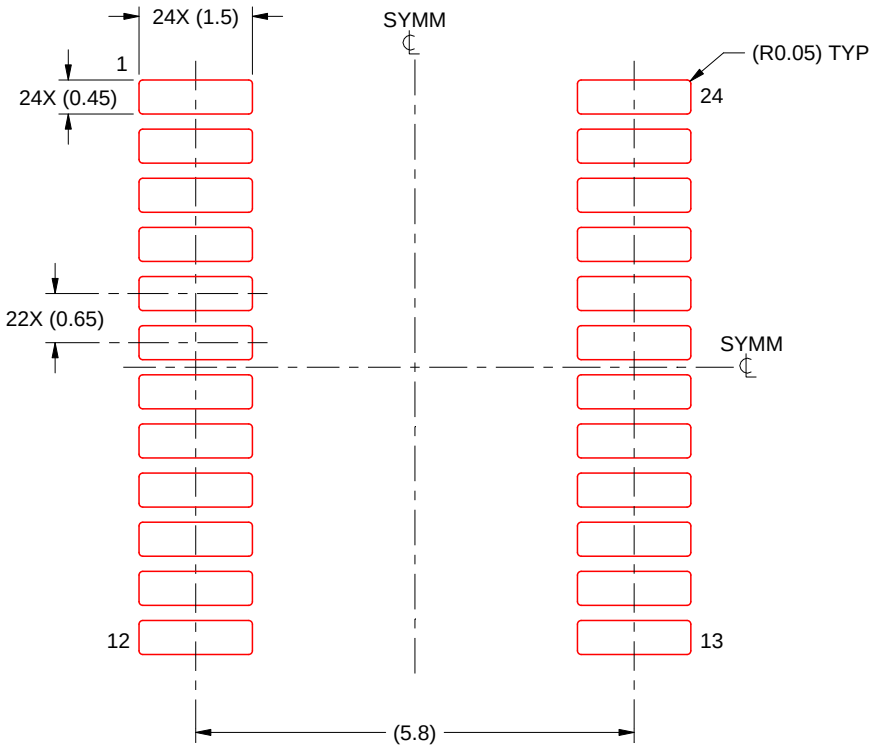



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# 重要なお知らせと免責事項

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