SN74HC165B-EP エンハンスド製品、5V、パラレル・ロード 8 ビット・シフト・レジスタ

1 特長

- 2V～6V の V_{CC} で動作
- JESD 17 準拠で
  250mA 超のラッチアップ性能
- 動作時周囲温度:-55℃～+125℃
- 防衛、航空宇宙、医療アプリケーションをサポート:
  - 管理されたベースライン
  - 単一のアセンブリおよびテスト施設
  - 単一の製造施設
  - 製品ライフ・サイクルの長期化
  - 製品のトレーサビリティ

2 アプリケーション

- マイクロコントローラの入力数拡張

3 概要

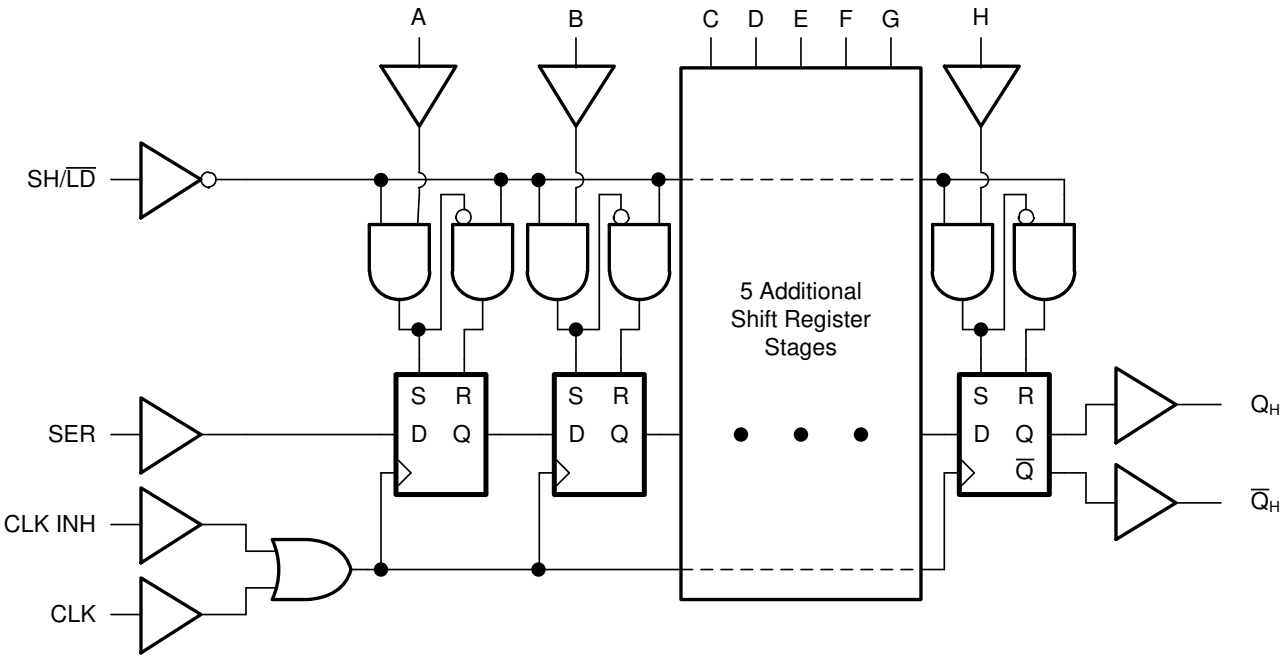
SN74HC165B-EP デバイスは、2V～6V の V_{CC} で動作するように設計された、パラレルロード (並列読み込み) 8 ビット・シフト・レジスタです。

デバイスにクロックが供給されると、データはシリアル出力 Q_H にシフトされます。各段のパラレル入力へのアクセスは、8 つの個別の直接データ入力によって提供されます。これらのデータ入力は、シフト / ロード (SH/$\overline{LD}$) 入力が Low レベルのときイネーブルになります。SN74HC165B-EP デバイスは、クロック禁止機能と、反転したシリアル出力 $\overline{Q}_H$ を備えています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
SN74HC165B-EP	PW (TSSOP、16)	5mm × 6.4mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



論理図 (正論理)

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 6
6.6 Timing Requirements, V_{CC} = 2 V ... 6
6.7 Timing Requirements, V_{CC} = 4.5 V ... 6
6.8 Timing Requirements, V_{CC} = 6 V ... 7
6.9 Switching Characteristics, V_{CC} = 2 V ... 8
6.10 Switching Characteristics, V_{CC} = 4.5 V ... 8
6.11 Switching Characteristics, V_{CC} = 6 V ... 8
6.12 Operating Characteristics ... 8
6.13 Typical Characteristics ... 8
7 Parameter Measurement Information ... 9
8 Detailed Description ... 10
8.1 Overview ... 10
8.2 Functional Block Diagram ... 10
8.3 Feature Description ... 10
8.4 Device Functional Modes ... 11
9 Application and Implementation ... 12
9.1 Application Information ... 12
9.2 Typical Application ... 12
9.3 Power Supply Recommendations ... 14
9.4 Layout ... 15
10 Device and Documentation Support ... 16
10.1 Related Documentation ... 16
10.2 Receiving Notification of Documentation Updates ... 16
10.3 サポート・リソース ... 16
10.4 Trademarks ... 16
10.5 静電気放電に関する注意事項 ... 16
10.6 用語集 ... 16
11 Mechanical, Packaging, and Orderable Information ... 16

4 Revision History

DATE	REVISION	NOTES
August 2023	*	Initial Release

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5 Pin Configuration and Functions

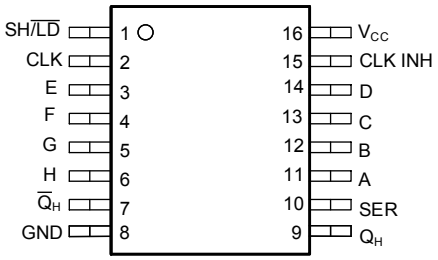


図 5-1. SN74HC165B-EP: PW Package, 16-Pin TSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
A	11	I	Serial input A
B	12	I	Serial input B
C	13	I	Serial input C
CLK	2	I	Storage clock
CLK INH	15	I	Storage clock
D	14	I	Serial input D
E	3	I	Serial input E
F	4	I	Serial input F
G	5	I	Serial input G
GND	8	—	Ground pin
H	6	I	Serial input H
$\overline{Q}_H$	7	O	Output H, inverted
Q_H	9	O	Output H
SH/ $\overline{LD}$	1	I	Load Input
SER	10	I	Serial input
V_{CC}	16	—	Power pin

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
V_O	Output voltage (2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		±20	mA
I_{OK}	Output clamp current	V_O < 0		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 4.5 V	3.15		
		V_{CC} = 6 V	4.2		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 4.5 V		1.35	
		V_{CC} = 6 V		1.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
Δt/Δv	Input transition rise or fall rate	V_{CC} = 2 V		1000	ns/V
		V_{CC} = 4.5 V		500	
		V_{CC} = 6 V		400	
T_A	Operating free-air temperature		–55	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. See *Implications of Slow or Floating CMOS Inputs.*

6.4 Thermal Information

THERMAL METRIC(1)		SN74HC165B-EP PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	131.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	21.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	75.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics.*

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted).

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –20 µA	2 V to 6 V	V_{CC} – 0.1			V
	I_{OH} = –4 mA	4.5 V	3.7	4.3		
	I_{OH} = –5.2 mA	6 V	5.2	5.8		
V_{OL}	I_{OL} = 20 µA	2 V to 6 V			0.1	V
	I_{OL} = 4 mA	4.5 V		0.17	0.4	
	I_{OL} = 5.2 mA	6 V		0.15	0.4	
I_I	V_I = V_{CC} or GND	6 V		±0.1	±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	6 V			160	µA
C_i	V_I = V_{CC} or GND	2 V to 6 V		3	10	pF

6.6 Timing Requirements, V_{CC} = 2 V

over recommended operating free-air temperature range (unless otherwise noted) (see セクション 7)

PARAMETER		TEST CONDITION	25°C		–55°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			6		4.2	MHz
t_w	Pulse duration	CLK high or low	80		120		ns
		SH/ $\overline{LD}$ low	80		120		
t_{su}	Setup time	SH/ $\overline{LD}$ high before CLK ↑	80		120		ns
		SER before CLK ↑	40		60		
		CLK INH before CLK ↑	100		150		
		Data before SH/ $\overline{LD}$ ↑	100		150		
t_h	Hold time	SER data after CLK ↑	5		5		ns
		Parallel data after SH/ $\overline{LD}$ ↑	5		5		
		SH/ $\overline{LD}$ high after CLK ↑	5		5		

6.7 Timing Requirements, V_{CC} = 4.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see セクション 7)

PARAMETER		TEST CONDITION	25°C		–55°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			31		21	MHz
t_w	Pulse duration	CLK high or low	16		24		ns
		SH/ $\overline{LD}$ low	16		24		
t_{su}	Setup time	SH/ $\overline{LD}$ high before CLK ↑	16		24		ns
		SER before CLK ↑	8		12		
		CLK INH before CLK ↑	20		30		
		Data before SH/ $\overline{LD}$ ↑	20		30		
t_h	Hold time	SER data after CLK ↑	5		5		ns
		Parallel data after SH/ $\overline{LD}$ ↑	5		5		
		SH/ $\overline{LD}$ high after CLK ↑	5		5		

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6.8 Timing Requirements, V_{CC} = 6 V

over recommended operating free-air temperature range (unless otherwise noted) (see セクション 7)

PARAMETER		TEST CONDITION	25°C		–55°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			36		25	MHz
t_w	Pulse duration	CLK high or low	14		20		ns
		SH/ $\overline{LD}$ low	14		20		
t_{su}	Setup time	SH/ $\overline{LD}$ high before CLK ↑	14		20		ns
		SER before CLK ↑	7		10		
		CLK INH before CLK ↑	17		25		
		Data before SH/ $\overline{LD}$ ↑	17		26		
t_h	Hold time	SER data after CLK ↑	5		5		ns
		Parallel data after SH/ $\overline{LD}$ ↑	5		5		
		SH/ $\overline{LD}$ high after CLK ↑	5		5		

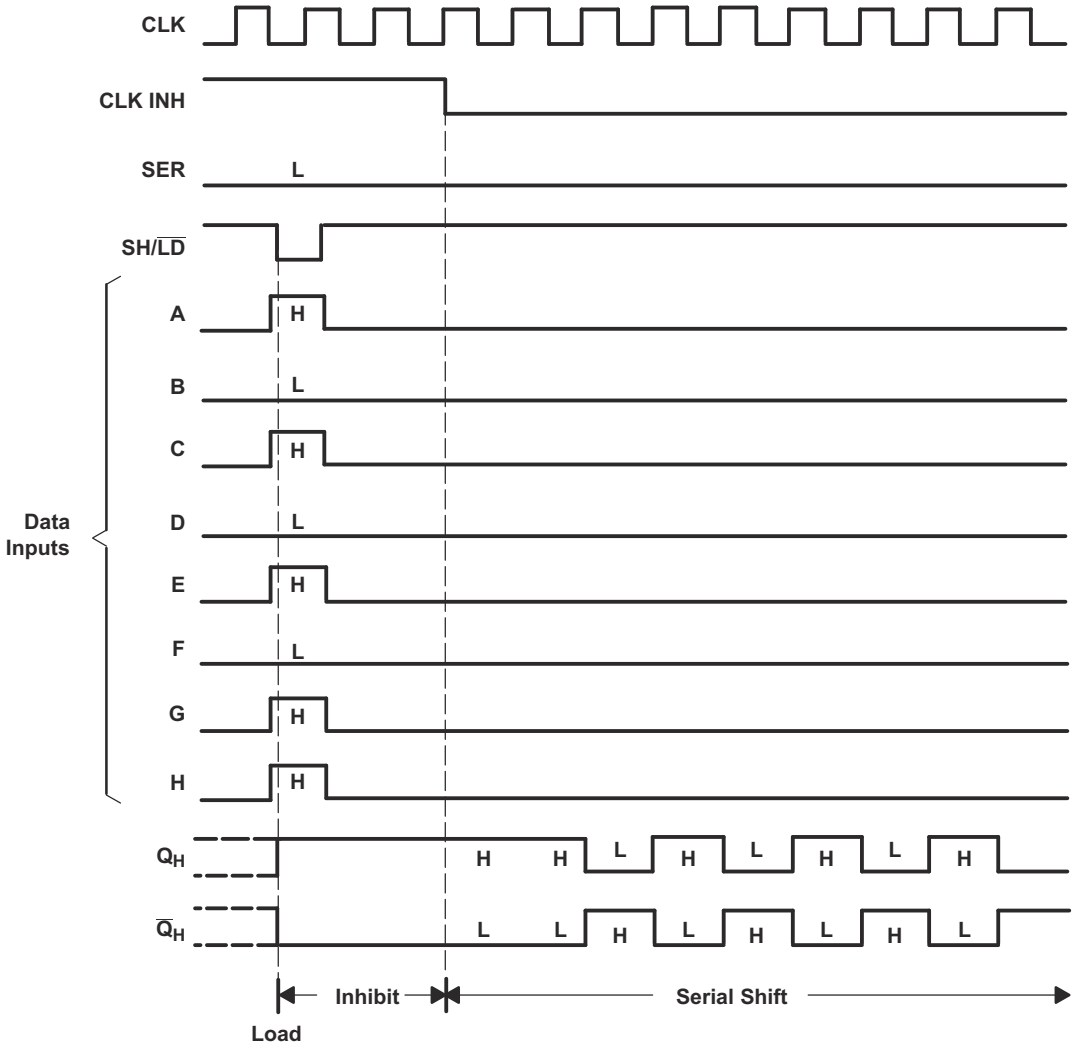


図 6-1. Typical Shift, Load, and Inhibit Sequences

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6.9 Switching Characteristics, V_{CC} = 2 V

over operating free-air temperature range (unless otherwise noted), (see セクション 7)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	25°C			–55°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	CLK	Q_H or $\overline{Q}$	C_L = 50 pF		75	150			225	ns
	SH/ $\overline{LD}$				80	150			225	
	H				75	150			225	

6.10 Switching Characteristics, V_{CC} = 4.5 V

over operating free-air temperature range (unless otherwise noted), (see セクション 7)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	25°C			–55°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	CLK	Q_H or $\overline{Q}$	C_L = 50 pF		15	30			45	ns
	SH/ $\overline{LD}$				20	30			45	
	H				15	30			45	

6.11 Switching Characteristics, V_{CC} = 6 V

over recommended operating free-air temperature range (unless otherwise noted), (see セクション 7)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	25°C			–55°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	CLK	Q_H or $\overline{Q}$	C_L = 50 pF		13	26			38	ns
	SH/ $\overline{LD}$				16	26			38	
	H				13	26			38	

6.12 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	6 V	75	pF

6.13 Typical Characteristics

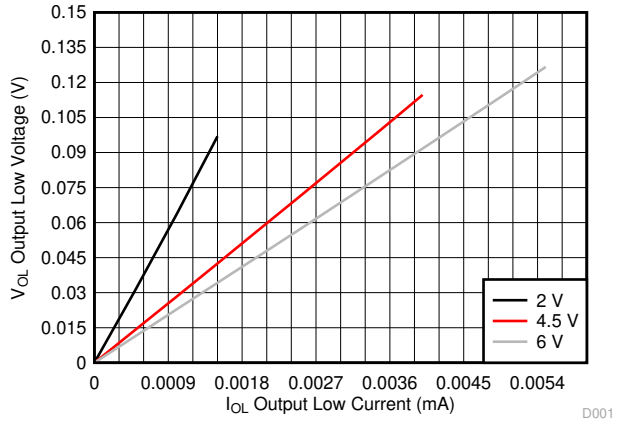


図 6-2. Output Voltage Versus Output Current in Low State

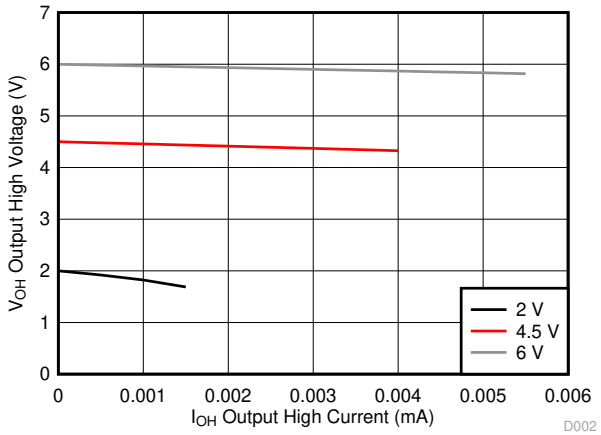
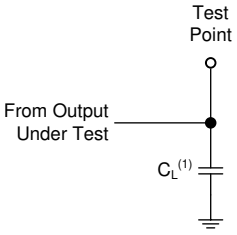


図 6-3. Output Voltage Versus Output Current in High State

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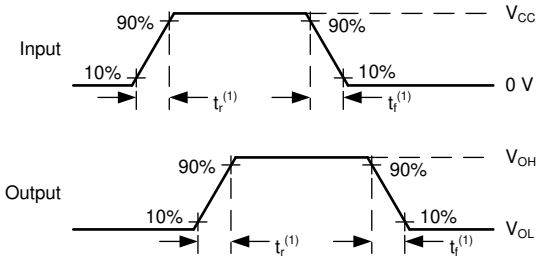
7 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.
- The outputs are measured one at a time, with one input transition per measurement.



A. C_L = 50 pF and includes probe and jig capacitance.

図 7-1. Load Circuit



A. The maximum between t_r and t_f is used for t_t.

図 7-2. Voltage Waveforms Transition Times

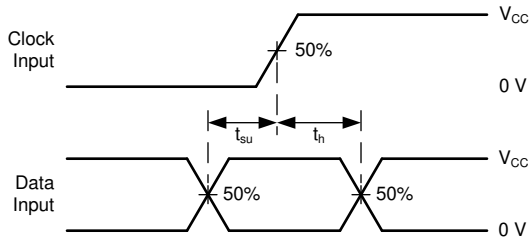


図 7-3. Voltage Waveforms Setup and Hold Times

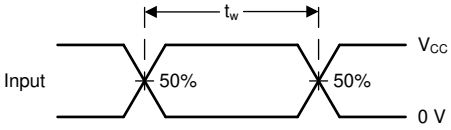
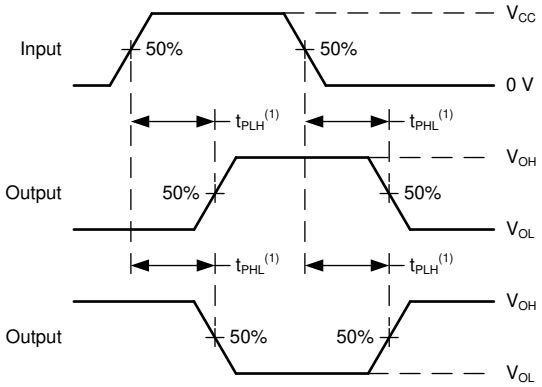


図 7-4. Voltage Waveforms Pulse Width



A. The maximum between t_{PLH} and T_{PHL} is used for t_{pd}.

図 7-5. Voltage Waveforms Propagation Delays

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8 Detailed Description

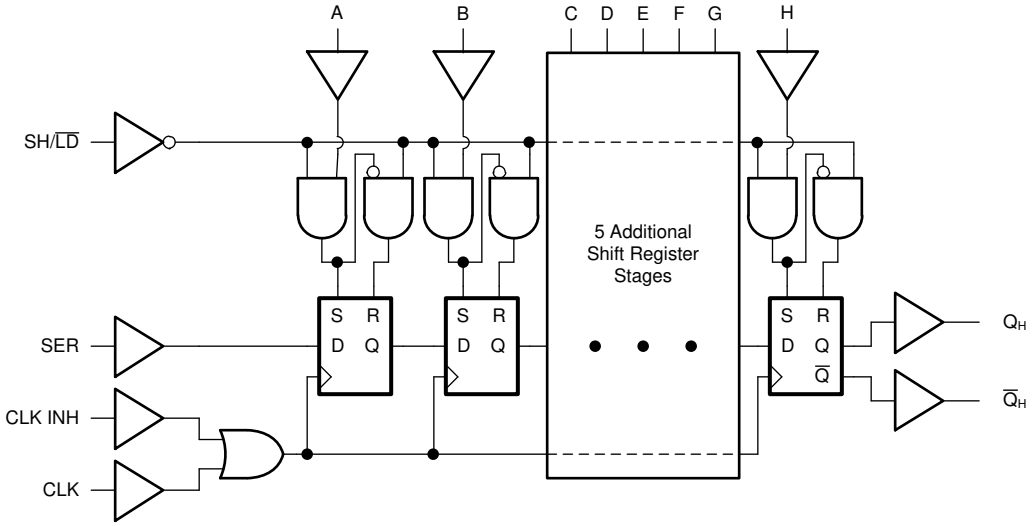
8.1 Overview

The SN74HC165B-EP device is a parallel-load, 8-bit shift registers designed for 2 V to 6 V V_{CC} operation.

When the device is clocked, data is shifted toward the serial output Q_H. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the shift/load (SH/ $\overline{LD}$) input. The SN74HC165B-EP features a clock-inhibit function and a complemented serial output, $\overline{Q}_H$.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/ $\overline{LD}$ is held high and clock inhibit (CLK INH) is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH accomplishes clocking, CLK INH must be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/ $\overline{LD}$ is held high. The parallel inputs to the register are enabled while SH/ $\overline{LD}$ is held low, independently of the levels of CLK, CLK INH, or SER.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

8.3.2 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

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8.3.3 Clamp Diode Structure

図 8-1 shows the inputs and outputs to this device have negative clamping diodes only.

> **注意**
> Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

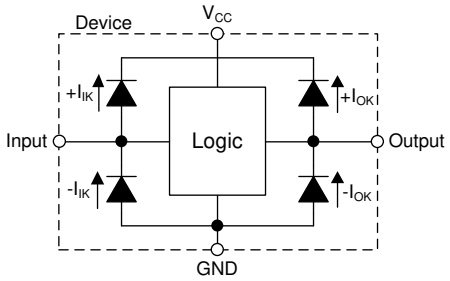


図 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

表 8-1 and 表 8-2 list the functional modes of the SN74HC165B-EP.

表 8-1. Operating Mode Table

INPUTS(1)			FUNCTION
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	No change
H	X	H	No change
H	L	↑	Shift(2)
H	↑	L	Shift(2)

(1) H = High Voltage Level, L = Low Voltage Level, X = Do Not Care, ↑ = Low to High transition
(2) Shift: content of each internal register shifts towards serial output Q_H. Data at SER is shifted into the first register.

表 8-2. Output Function Table

INTERNAL REGISTERS(1) (2)		OUTPUTS(2)	
A — G	H	Q	$\overline{Q}$
X	L	L	H
X	H	H	L

(1) Internal registers refer to the shift registers inside the device. These values are set by either loading data from the parallel inputs, or by clocking data in from the serial input.
(2) H = High Voltage Level, L = Low Voltage Level, X = Do Not Care

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74HC165B-EP is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low-drive and slow-edge rates minimize overshoot and undershoot on the outputs.

9.2 Typical Application

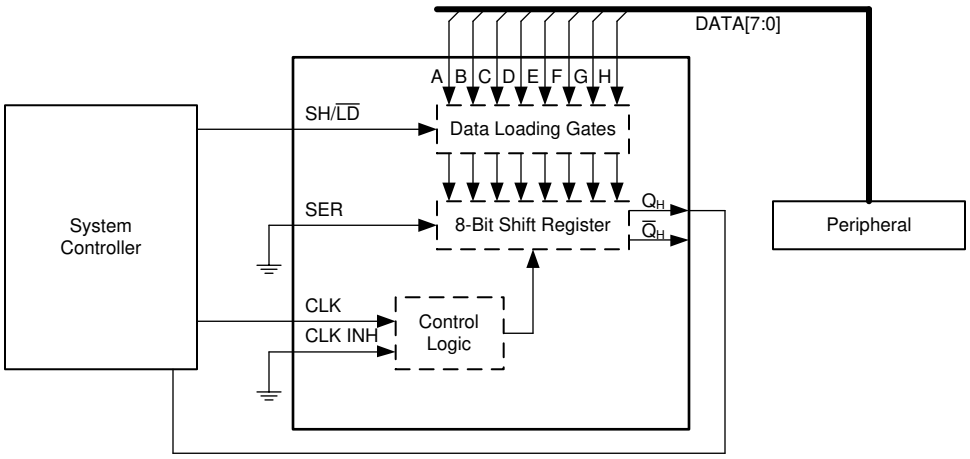


図 9-1. Input Expansion with Shift Registers

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9.2.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HC165B-EP plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HC165B-EP plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74HC165B-EP can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74HC165B-EP can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

> **注意**
> The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74HC165B-EP (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-kΩ resistor value is often used due to these factors.

The SN74HC165B-EP has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

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9.2.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

9.2.4 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74HC165B-EP to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$) Ω, which will not violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

9.2.5 Application Curves

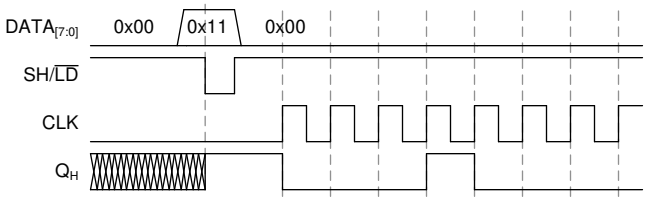


図 9-2. Application Timing Diagram

9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* section. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-μF capacitor; if there are multiple V_{CC} terminals, then TI recommends a 0.01-μF or 0.022-μF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

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9.4 Layout

9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

9.4.2 Layout Example

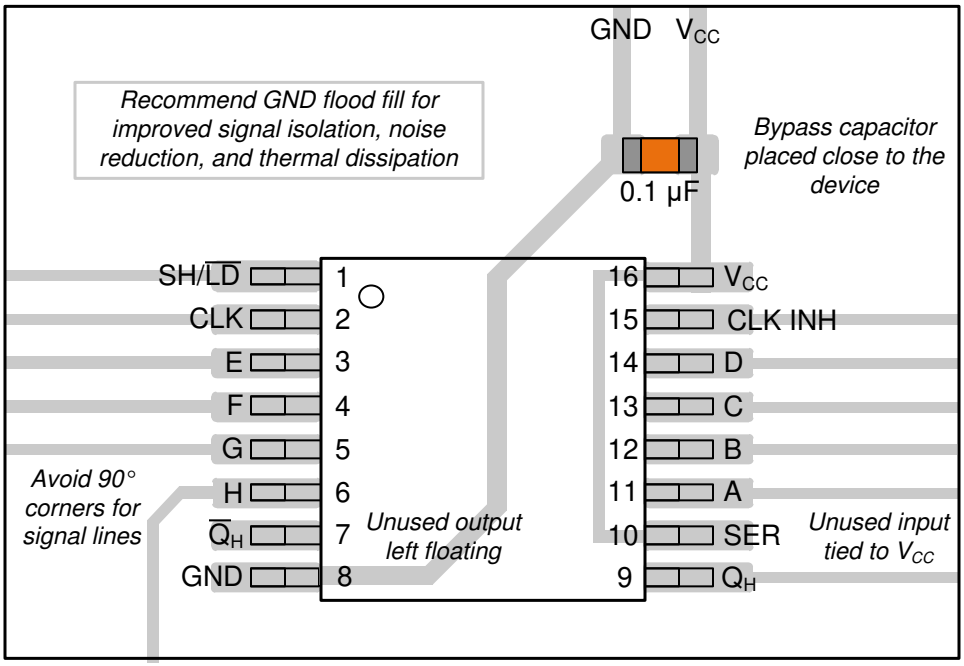


図 9-3. Layout Example for the SN74HC165B-EP in the PW Package

10 Device and Documentation Support

10.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Power-Up Behavior of Clocked Devices*
- Texas Instruments, *Introduction to Logic*

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

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10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HC165BMPWREP	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC165EP
SN74HC165BMPWREP.A	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC165EP
V62/23621-01XE	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See SN74HC165BMPWREP	HC165EP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

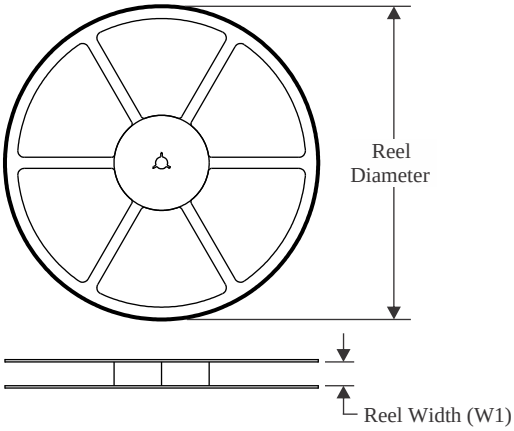
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

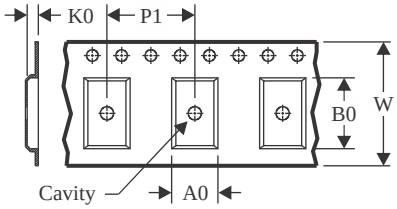
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

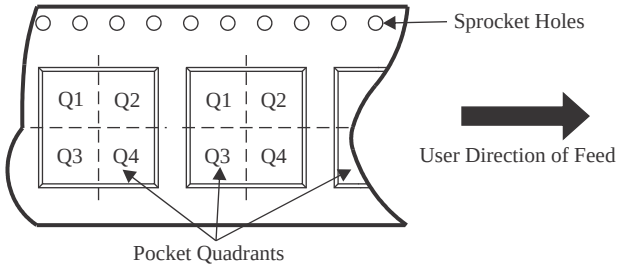


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

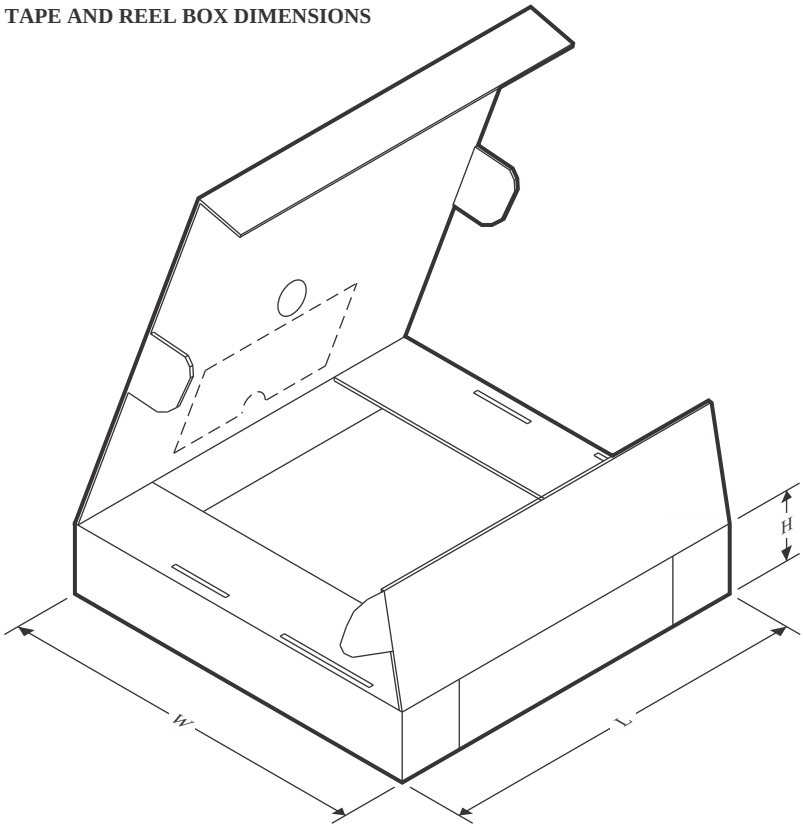
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC165BMPWREP	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

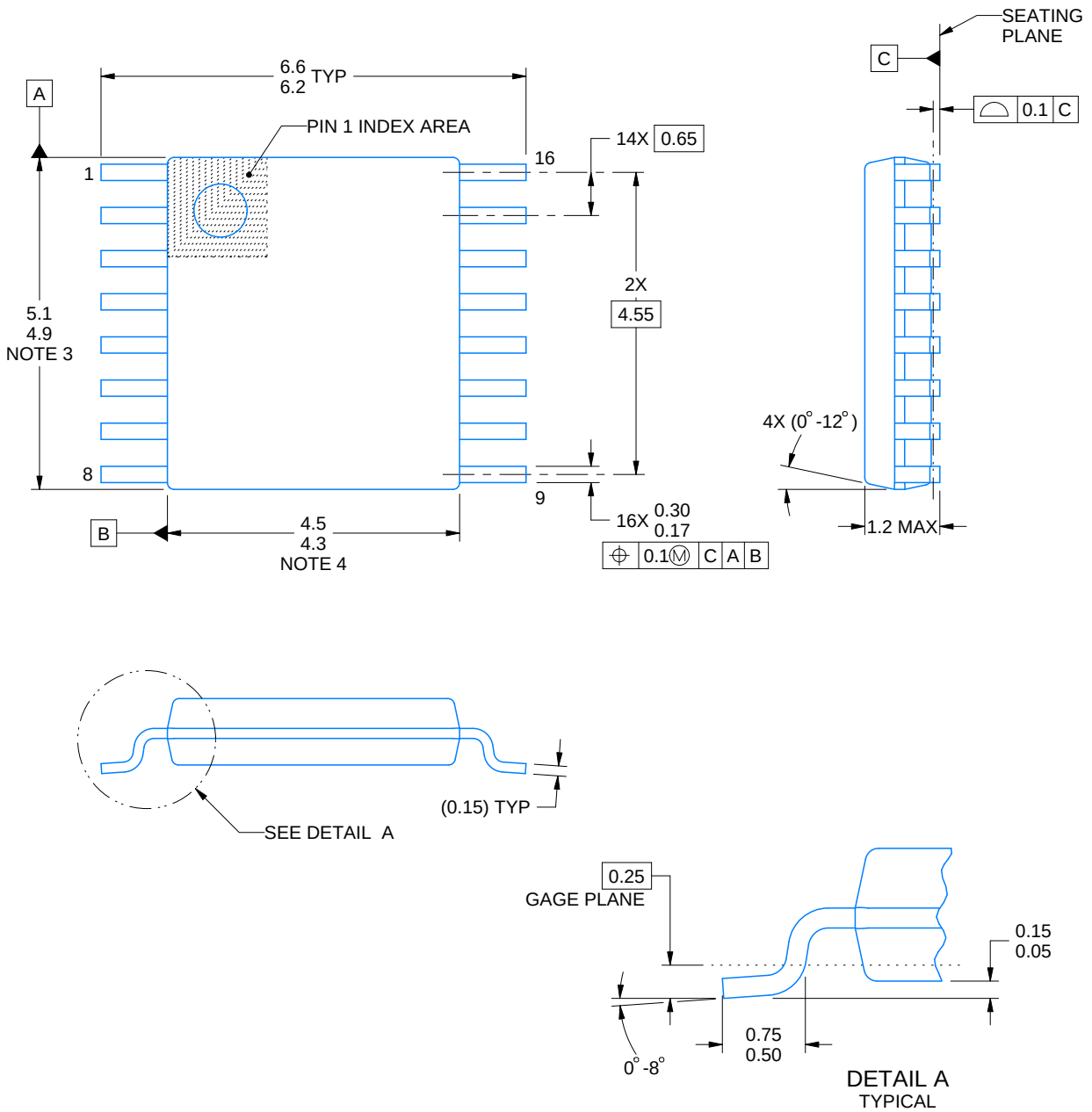
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC165BMPWREP	TSSOP	PW	16	3000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0016A

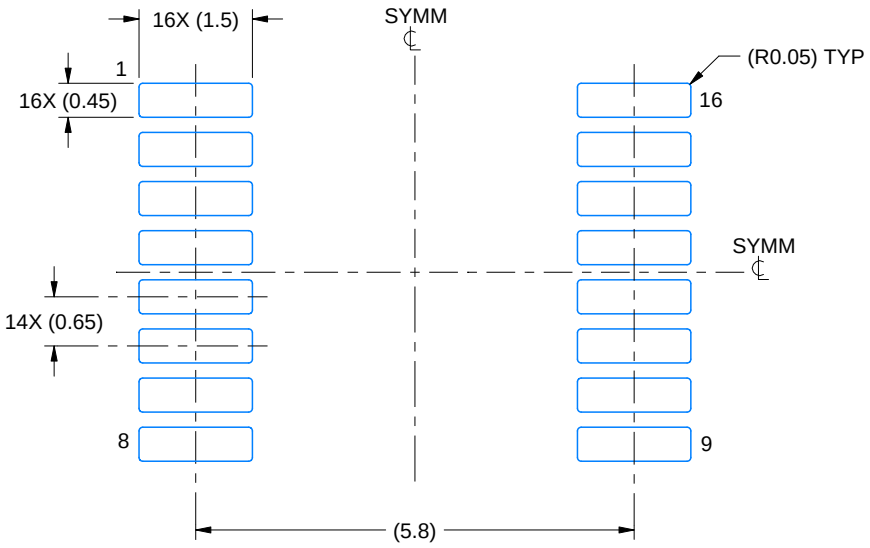
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

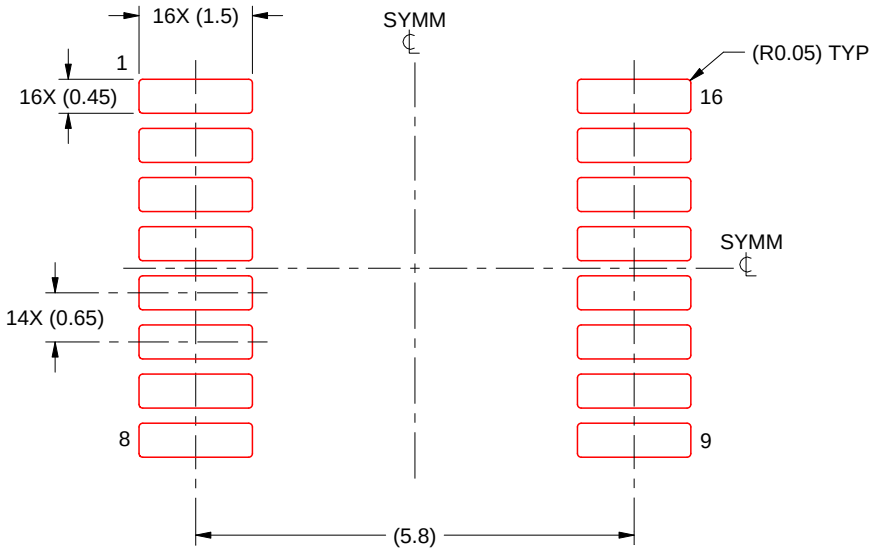


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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