SN54HCT139, SN74HCT139
JAJSP08E – MARCH 1982 – REVISED AUGUST 2022

# デュアル 2 ラインから 4 ラインへのデコーダ / デマルチプレクサ

## 1 特長

- 4.5V～5.5V の動作電源電圧範囲
- 出力は最大 10 個の LSTTL 負荷を駆動可能
- 低い消費電力、最大 $I_{CC}$ 80µA
- $t_{pd}$ = 10ns (標準値)
- 5V で ±4mA の出力駆動能力
- 低い入力電流、最大 1µA
- 入力は TTL 電圧互換
- 高速メモリ・デコーダおよびデータ伝送システム専用に設計
- 2 つのイネーブル入力を備え、カスケード接続やデータ受信を簡素化

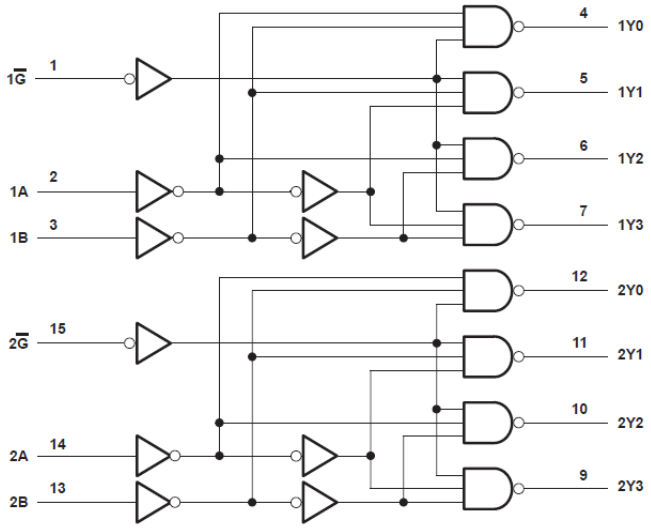
## 2 概要

'HCT139 デバイスは、伝搬遅延時間を極めて短くする必要がある、高性能のメモリ・デコーディングやデータ・ルーティングのアプリケーション用に設計されています。

**製品情報** (1)

| 発注型番 | パッケージ† | 本体サイズ (公称) |
|---|---|---|
| SN74HCT139 | N (PDIP、16) | 19.31mm × 6.35mm |
| | D (SOIC、16) | 9.90mm × 3.90mm |
| | DB (SSOP、16) | 6.2mm × 5.3mm |
| | PW (TSSOP、16) | 5.00mm × 4.40mm |
| SNJ54HCT139 | J (CDIP、16) | 24.38mm × 6.92mm |
| | W (CFP、16) | 10.3mm × 1.65mm |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。




A. ここに示すピン番号は D、DB、J、N、PW、W の各パッケージのものです。

**論理図 (正論理)**

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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## 3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision D (September 2003) to Revision E (August 2022) | Page |
|---|---|
| • 最新のデータシート規格を反映するように、文書全体の採番、書式設定、表、図、相互参照を更新 | 1 |


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## 4 概要 (続き)

'HCT139 デバイスは、2 つの個別の 2 ライン入力、4 ライン出力デコーダを、1 つのパッケージに搭載したものです。アクティブ Low のイネーブル (G) 入力は、デマルチプレクサ・アプリケーションのデータ・ラインとして使用できます。これらのデコーダ / デマルチプレクサの入力は完全にバッファされ、それぞれの入力は、駆動回路に対して 1 つの正規化された負荷のみを表します。

## 5 Pin Configuration and Functions

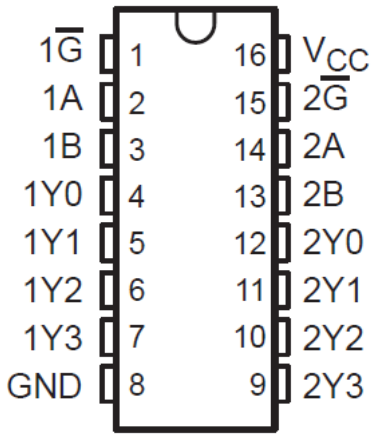
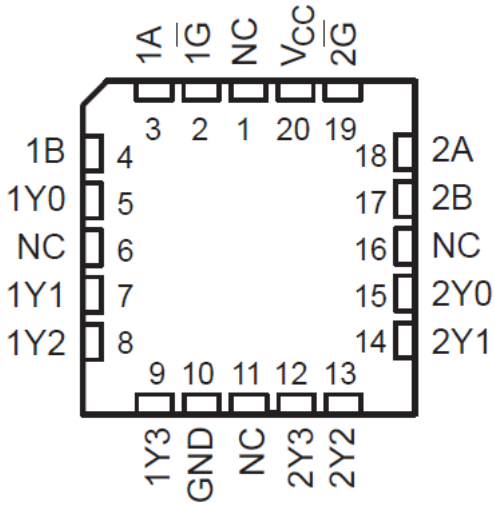



**図 5-1. SN54HCT139 J or W Package**
**SN74HCT139 D, DB, N, or PW Package**
**Top View**




A. NC - No internal connection

**図 5-2. SN54HCT139 FK Package**
**Top View**

# 6 Specifications

## 6.1 Absolute Maximum Rating

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $I_{IK}$ | Input clamp current(2) | $V_I < 0$ or $V_I > V_{CC}$ | | ±20 | mA |
| $I_{OK}$ | Output clamp current(2) | $V_O < 0$ or VO> $V_{CC}$ | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_J$ | Junction Temperature | | | 150 | ℃ |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | ℃ |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 6.2 Recommended Operating Conditions(1)

| | | | SN54HCT139 | | | SN74HCT139 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $t_t$ | Input transition (rise and fall) time | | | | 500 | | | 500 | ns |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | −40 | | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 6.3 Thermal Information

| THERMAL METRIC(1) | | D (SOIC) | DB (SSOP) | N (PDIP) | PW (TSSOP) | UNIT |
|---|---|---|---|---|---|---|
| | | 16 PINS | 16 PINS | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Package thermal impedance | 73 | 82 | 67 | 108 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.


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## 6.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | | SN54HCT139 | | SN74HCT139 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | High level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −20 µA | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | V |
| | | | $I_{OH}$ = −4 mA | | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| $V_{OL}$ | Low level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 µA | 4.V | | 0.001 | 0.1 | | 0.1 | | 0.1 | V |
| | | | $IO_L$ = 4 mA | | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| $I_I$ | Input leakage current V | $V_I$ = $V_{CC}$ or 0 | | 5.5 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or 0 | $I_O$ = 0 | 5.5 V | | | 8 | | 160 | | 80 | µA |
| $\Delta I_{CC}$ (1) | Supply-Current Change | One input at 0.5 V or 2.4 V, Other inputs at 0 or $V_{CC}$ | | 5.5 V | | 1.4 | 2.4 | | 3 | | 2.9 | mA |
| $C_i$ | Input Capacitance | | | 4.5 V to 5.5 V | | 3 | 10 | | 10 | | 10 | pF |

(1) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or $V_{CC}$.

## 6.5 Switching Characteristics

over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see 図 7-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | SN54HCT139 | | SN74HCT139 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A or B | Y | 4.5 V | | 14 | 34 | | 51 | | 43 | ns |
| | | | 5.5 V | | 12 | 30 | | 50 | | 40 | |
| | $\overline{G}$ | Y | 4.5 V | | 11 | 34 | | 51 | | 43 | |
| | | | 5.5 V | | 10 | 30 | | 50 | | 40 | |
| $t_t$ | | Y | 4.5 V | | 8 | 15 | | 22 | | 19 | ns |
| | | | 5.5 V | | 6 | 14 | | 21 | | 17 | |

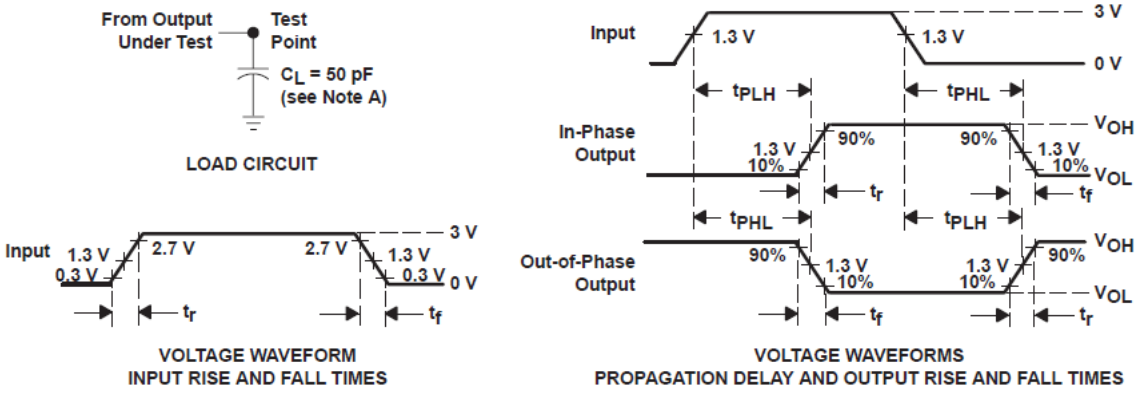
## 6.6 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per decoder | No load | 25 | pF |

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# 7 Parameter Measurement Information




A. $C_L$ includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 6 ns, $t_f$ = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**図 7-1. Load Circuit and Voltage Waveforms**


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# 8 Detailed Description

## 8.1 Overview

The ’HCT139 devices are designed for high performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay time of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

## 8.2 Functional Block Diagram

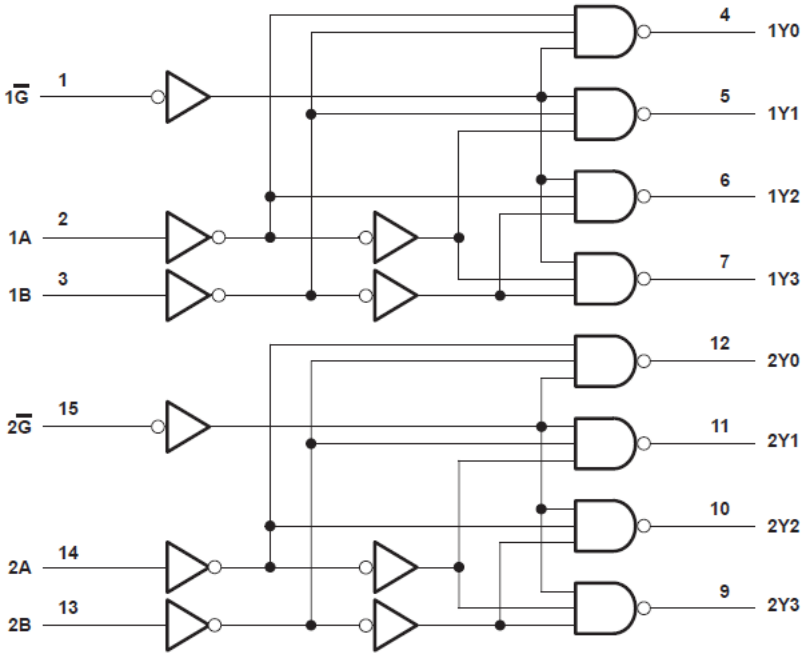



**図 8-1. Function Diagram**

## 8.3 Device Functional Modes

**表 8-1. Function Table**

| INPUTS(1) | | | OUTPUTS(2) | | | |
|---|---|---|---|---|---|---|
| $\overline{G}$ | SELECT | | | | | |
| | B | A | Y0 | Y1 | Y2 | Y3 |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don’t Care
(2) H = Driving High, L = Driving Low, Z = High Impedance State

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# 9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

# 10 Layout

## 10.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.


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# 11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 11.1 Documentation Support

### 11.1.1 Related Documentation

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 サポート・リソース

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## 11.4 Trademarks

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## 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74HCT139D | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -40 to 85 | HCT139 |
| SN74HCT139DBR | Active | Production | SSOP (DB) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT139 |
| SN74HCT139DBR.A | Active | Production | SSOP (DB) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT139 |
| SN74HCT139DR | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | HCT139 |
| SN74HCT139DR.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT139 |
| SN74HCT139DRG4 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT139 |
| SN74HCT139DRG4.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT139 |
| SN74HCT139N | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HCT139N |
| SN74HCT139N.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HCT139N |
| SN74HCT139PWR | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | HT139 |
| SN74HCT139PWR.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT139 |
| SN74HCT139PWRG4 | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT139 |
| SN74HCT139PWT | Obsolete | Production | TSSOP (PW) \| 16 | - | - | Call TI | Call TI | -40 to 85 | HT139 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

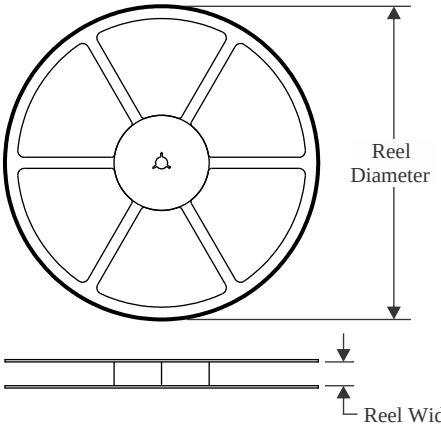
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

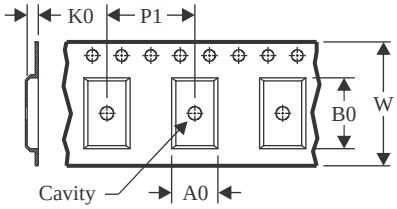
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

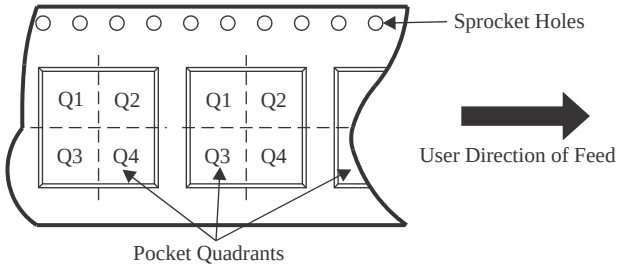



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

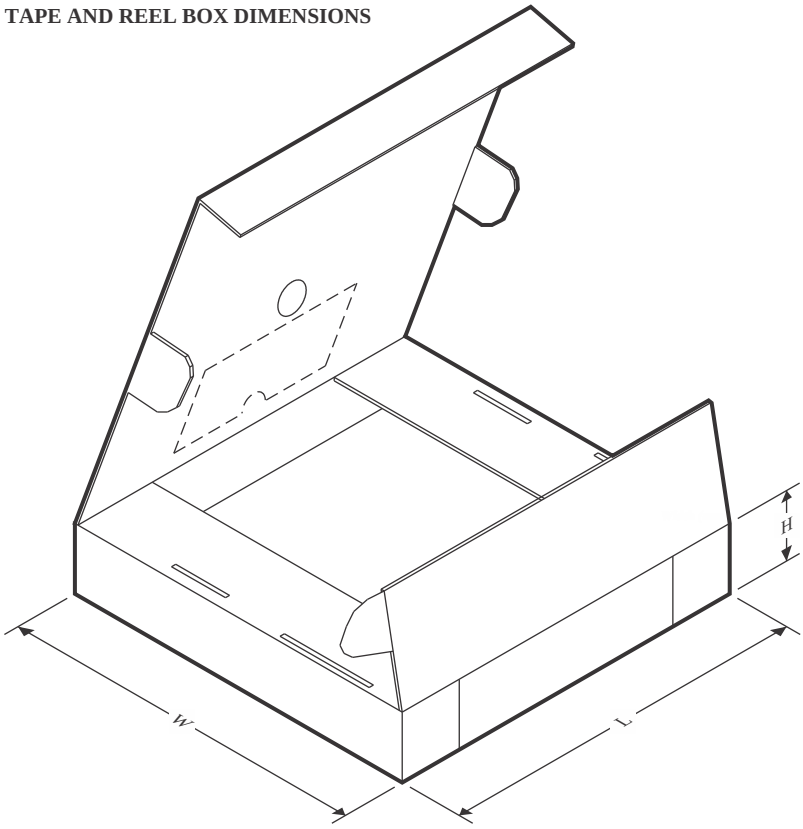
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HCT139DBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74HCT139DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HCT139DRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HCT139PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.3 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HCT139PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HCT139PWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HCT139PWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

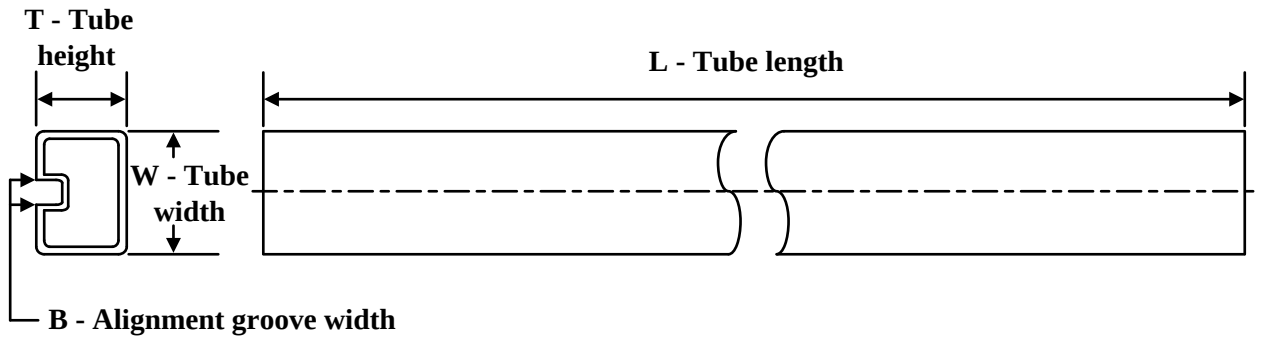
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74HCT139DBR | SSOP | DB | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74HCT139DR | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74HCT139DRG4 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74HCT139PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74HCT139PWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HCT139PWRG4 | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HCT139PWRG4 | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |

## TUBE




*All dimensions are nominal

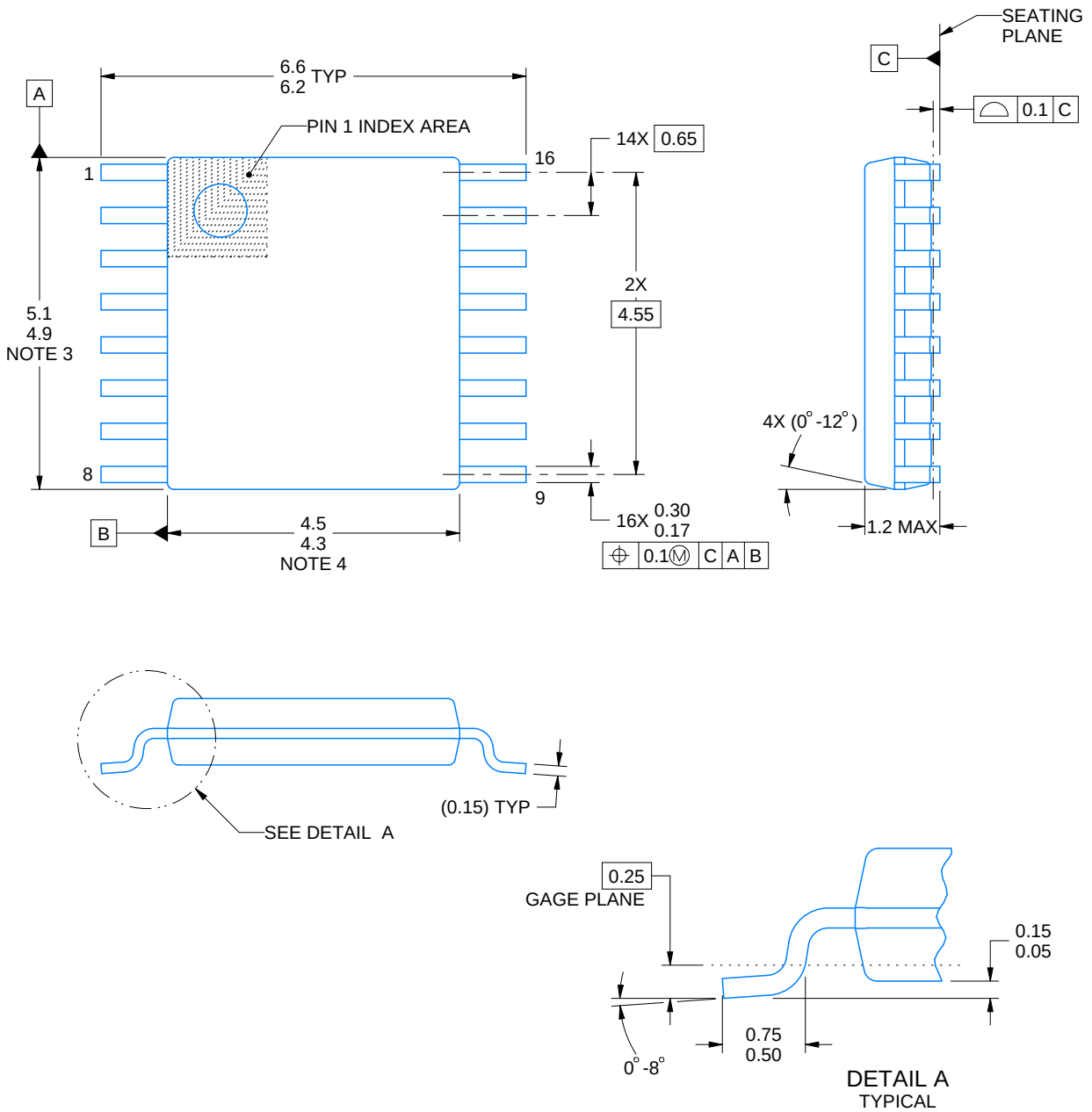
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74HCT139N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HCT139N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HCT139N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HCT139N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

# PACKAGE OUTLINE

## PW0016A

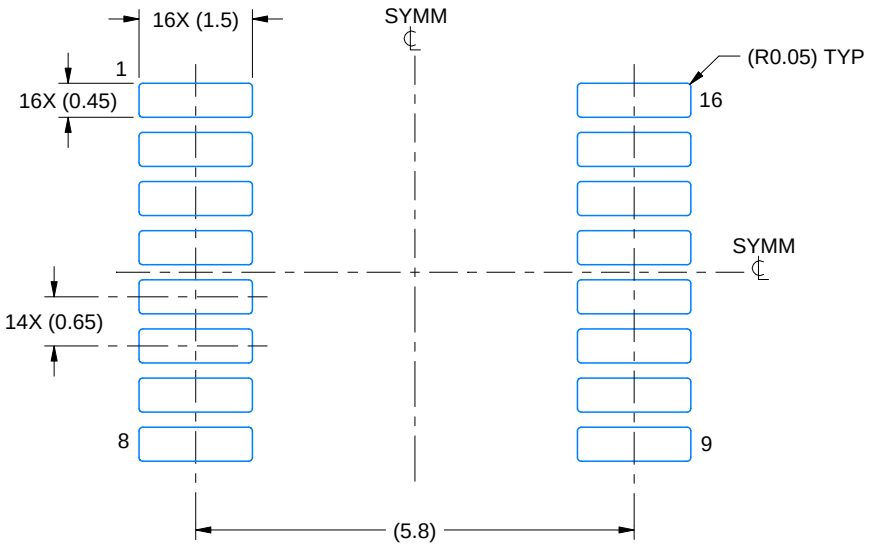
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

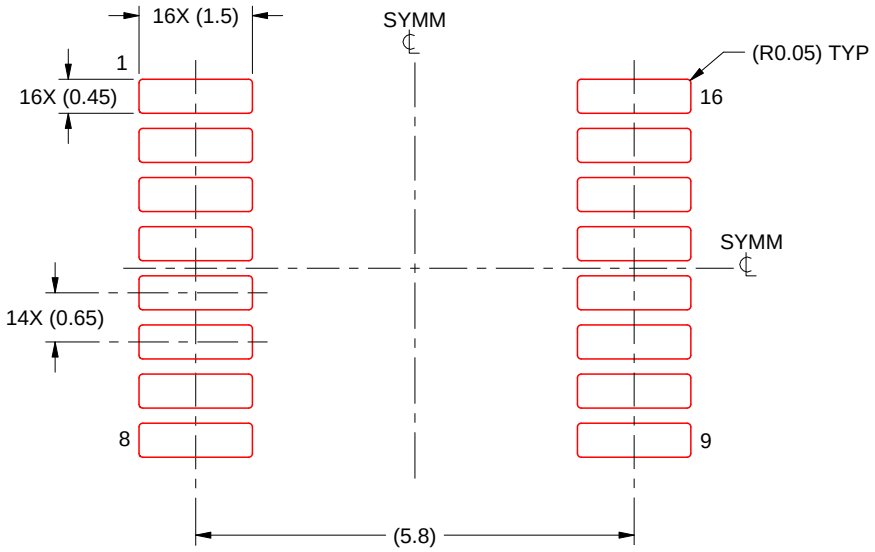



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

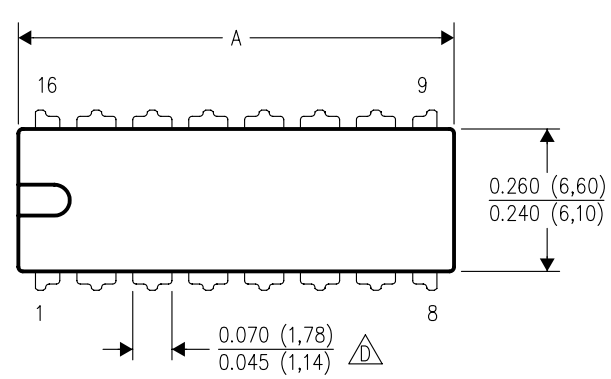
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

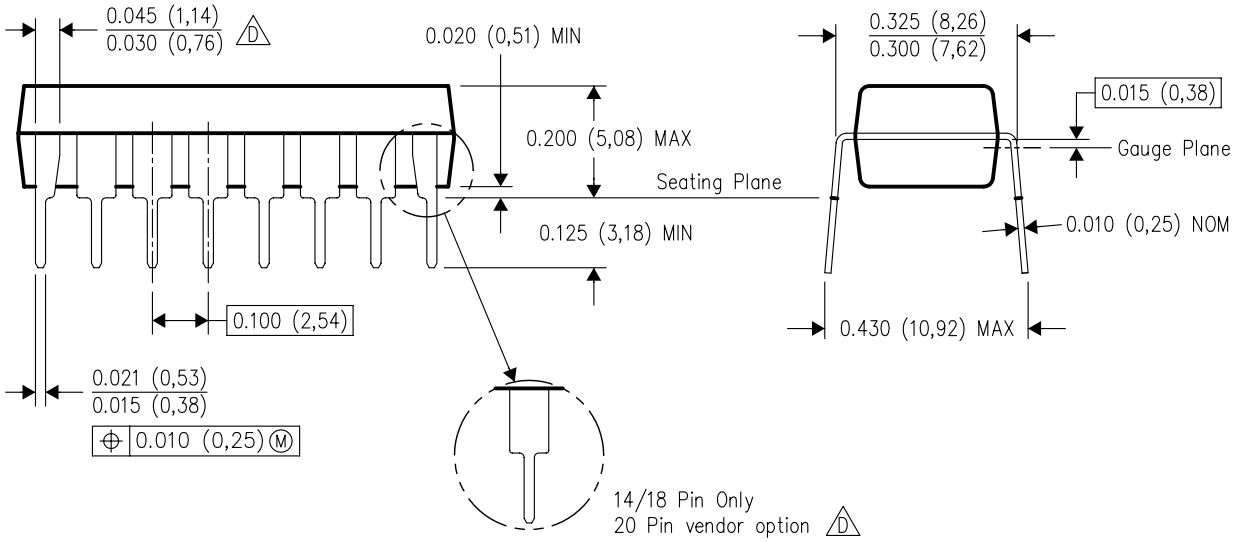
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



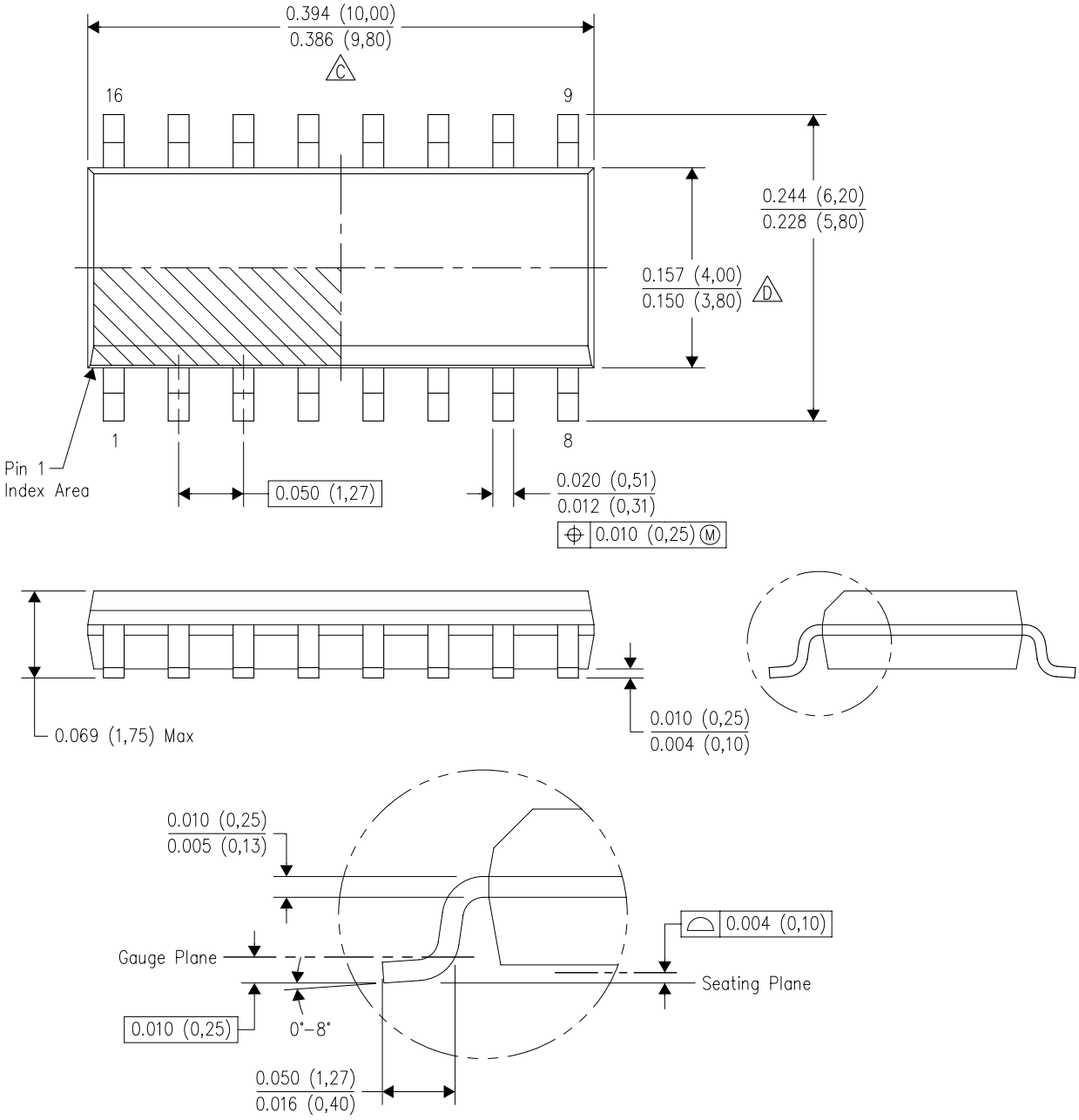

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



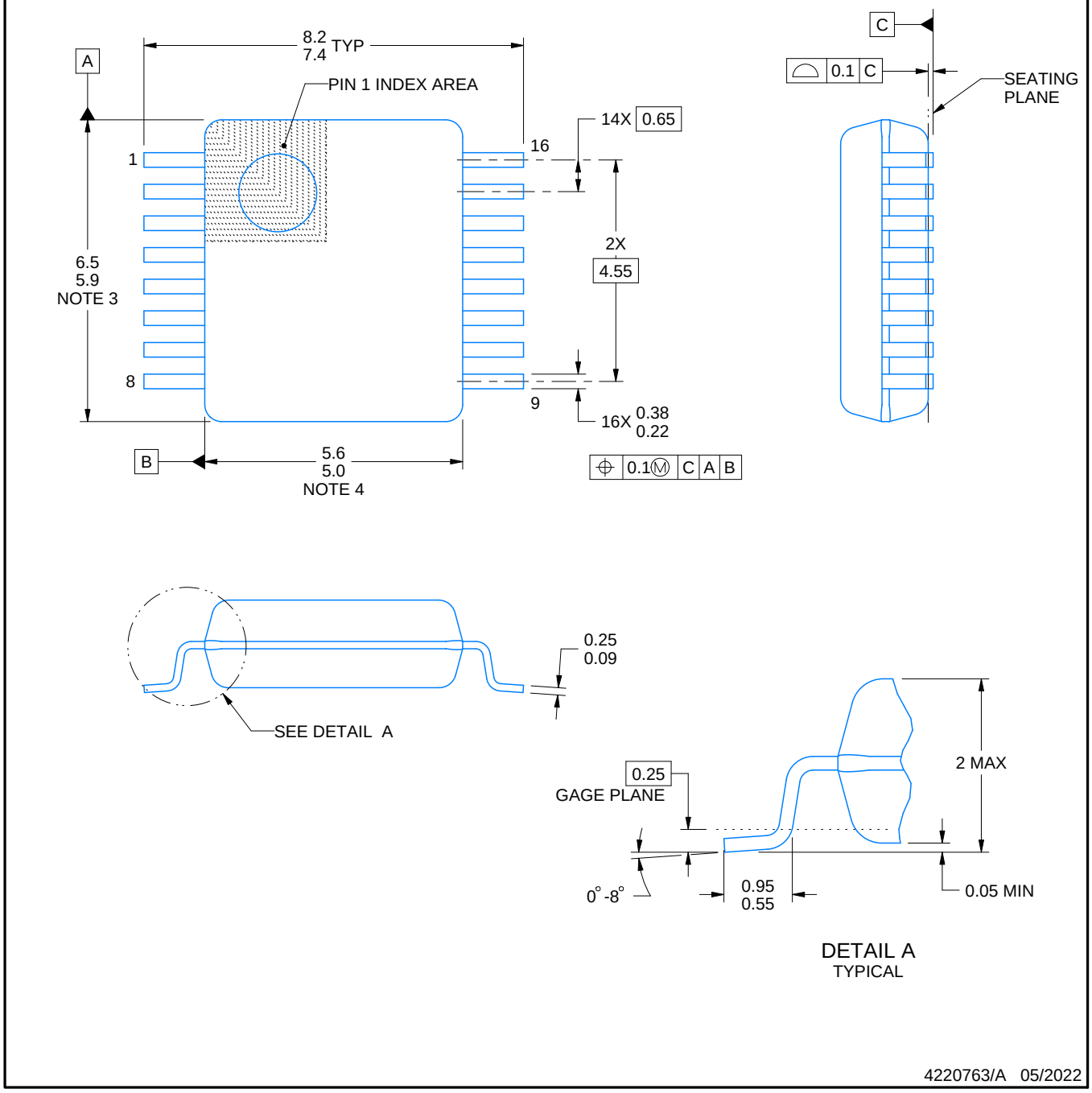

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

# PACKAGE OUTLINE

## DB0016A

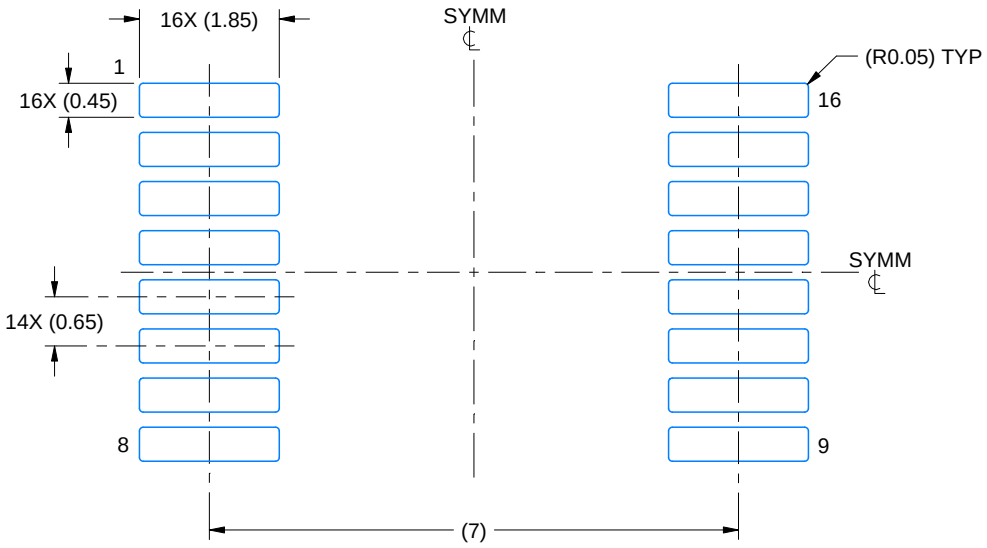
## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

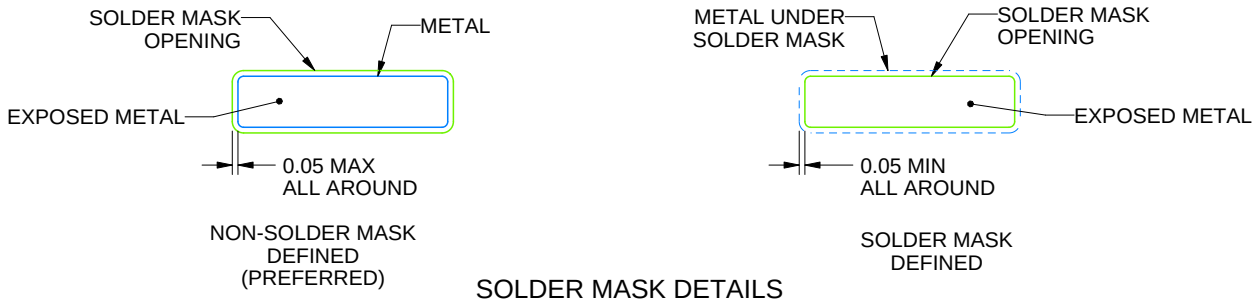



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

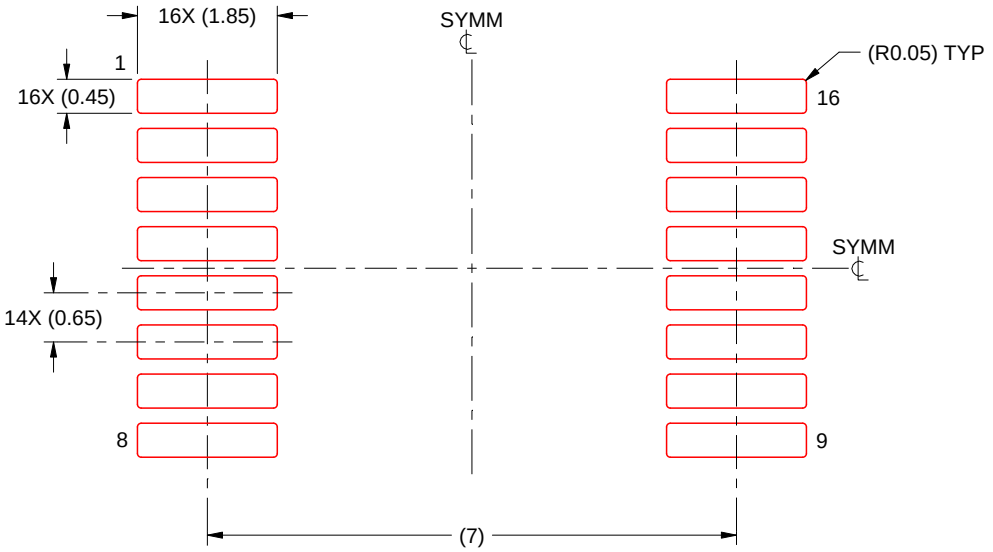



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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