# SN74LV08A-Q1 車載用クワッド 2 入力正論理 AND ゲート

## 1 特長

- 車載アプリケーション向け認定済み
- 標準 $V_{OLP}$ (出力グランド・バウンス) < 0.8V ($V_{CC}$ = 3.3V、$T_A$ = 25℃)
- 標準 $V_{OHV}$ (出力 $V_{OH}$ アンダーシュート) > 2.3V ($V_{CC}$ = 3.3V、$T_A$ = 25℃)
- すべてのポートで混在モード電圧動作をサポート
- $I_{off}$ により部分的パワーダウン・モードでの動作をサポート
- JESD 17 準拠で 250mA 超のラッチアップ性能

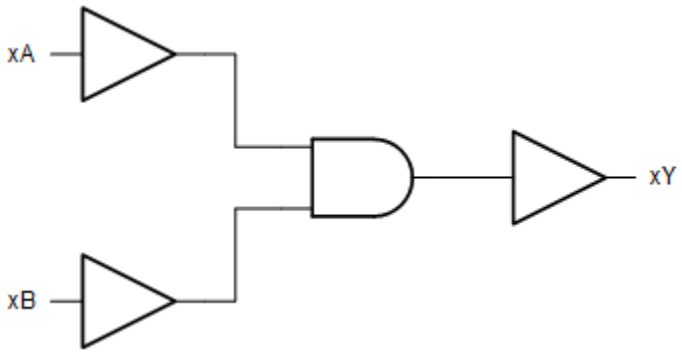
## 2 概要

このクワッド 2 入力の正論理 AND ゲートは、2V～5.5V の $V_{CC}$ で動作するように設計されています。

**パッケージ情報**

| 部品番号 | パッケージ(1) | パッケージ・サイズ(2) |
|---|---|---|
| SN74LV08A-Q1 | PW (TSSOP、14) | 5.00mm × 6.4mm |

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。




**論理図 (正論理)**

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## 3 Revision History

**Changes from Revision C (January 2008) to Revision D (August 2023)** **Page**

- 「パッケージ情報」表、「ピンの機能」表、「ESD 定格」表、「熱に関する情報」表、「デバイスの機能モード」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ... 1


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# 4 Pin Configuration and Functions

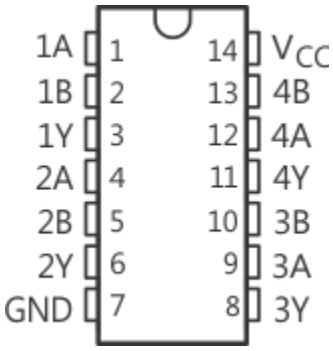



**図 4-1. PW Package**
**14-Pin TSSOP**
**Top View**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | 1A | I | 1A input |
| 2 | 1B | I | 1B |
| 3 | 1Y | O | 1Y |
| 4 | 2A | I | 2A |
| 5 | 2B | I | 2B |
| 6 | 2Y | O | 2Y |
| 7 | GND | — | GND |
| 8 | 3Y | O | 3Y |
| 9 | 3A | I | 3A |
| 10 | 3B | I | 3B |
| 11 | 4Y | O | 4Y |
| 12 | 4A | I | 4A |
| 13 | 4B | I | 4B |
| 14 | $V_{CC}$ | — | $V_{CC}$ |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 7 | V |
| $V_O$ | Voltage applied to any output in the high-impedance or power-off state(2) | | –0.5 | 7 | V |
| $V_O$ | Output voltage range(2) (3) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | –25 | 25 | mA |
| | Continuous current through $V_{CC}$ or GND | | –50 | 50 | mA |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value is limited to 5.5-V maximum.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002(1) | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | ±1000 | |

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | $V_{CC}$ x 0.7 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | $V_{CC}$ x 0.7 | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $V_{CC}$ x 0.7 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | $V_{CC}$ x 0.3 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | $V_{CC}$ x 0.3 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | $V_{CC}$ x 0.3 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | µA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | –2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | –6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | –12 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | µA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | 6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 12 | |


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over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 2.3 V to 2.7 V | | 200 | ns/V |
| | | $V_{CC}$ = 3 V to 3.6 V | | 100 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 20 | |
| $T_A$ | Operating free-air temperature | | –40 | 105 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND for proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

## 5.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

| THERMAL METRIC(1) | | PW | UNIT |
|---|---|---|---|
| | | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 113 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High level output voltage | $I_{OH}$ = –50 µA | 2 to 5.5 V | $V_{CC}$ – 0.1 | | | V |
| | | $I_{OH}$ = –2 mA | 2.3 V | 2 | | | |
| | | $I_{OH}$ = –6 mA | 3 V | 2.48 | | | |
| | | $I_{OH}$ = –12 mA | 4.5 V | 3.8 | | | |
| $V_{OL}$ | Low level output voltage | $I_{OL}$ = 50 µA | 2 to 5.5 V | | | 0.1 | V |
| | | $I_{OL}$ = 2 mA | 2.3 V | | | 0.4 | |
| | | $I_{OL}$ = 6 mA | 3 V | | | 0.44 | |
| | | $I_{OL}$ = 12 mA | 4.5 V | | | 0.55 | |
| $I_I$ | Input leakage current | $V_I$ = 5.5 V or GND | 0 to 5.5 V | | | ±1 | µA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 20 | µA |
| $I_{off}$ | Input/Output Power-Off Leakage Current | $V_I$ or $V_O$ = 0 to 5.5 V | 0 | | | 5 | µA |
| $C_i$ | Input Capacitance | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 3.3 | | pF |
| | | | 5 V | | 3.3 | | |

## 5.6 Switching Characteristics, $V_{CC}$ = 3.3 V ±0.3 V

over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ±0.3 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{pd}$ | A or B | Y | $C_L$ = 50 pF | | 7.5 | 12.3 | 1 | 16 | ns |

## 5.7 Switching Characteristics, $V_{CC}$ = 5 V ±0.5 V

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ±0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $t_{pd}$ | A or B | Y | $C_L$ = 50 pF | | 5.5 | 7.9 | 1 | 12 | ns |

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## 5.8 Noise Characteristics

$V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $T_A$ = 25°C(1)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.2 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.1 | –0.8 | |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 3.1 | | |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.31 | | | |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.99 | |

(1) Characteristics are for surface-mount packages only.

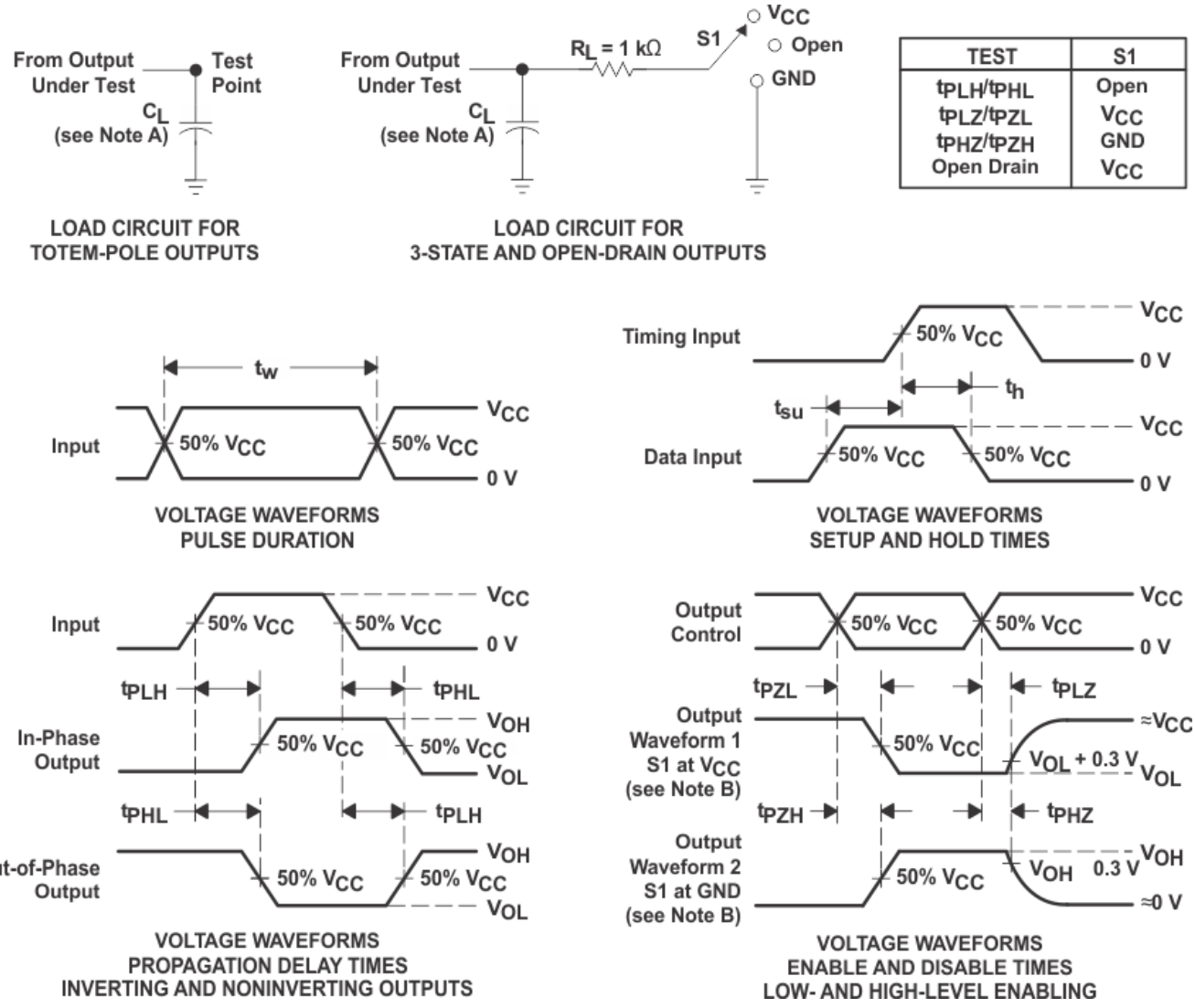
## 5.9 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF, f = 10 MHz | 3.3 V | 8 | pF |
| | | | 5 V | 10 | |


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## 6 Parameter Measurement Information




A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and tPZH are the same as $t_{en}$.
G. $t_{PHL}$ and $t_{PLH}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**図 6-1. Load Circuit and Voltage Waveforms**

# 7 Detailed Description

## 7.1 Overview

This quadruple 2-input positive-AND gate is designed for 2-V to 5.5-V VCC operation.

The SN74LV08A performs the Boolean function Y = A • B or Y = $\overline{A + B}$ in positive logic.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## 7.2 Functional Block Diagram

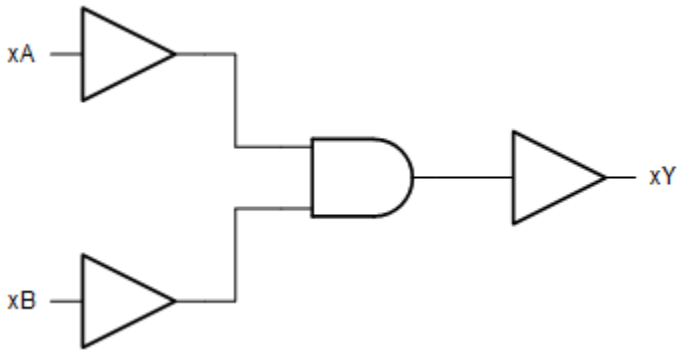



**図 7-1. Logic Diagram, each gate (Positive Logic)**

## 7.3 Device Functional Modes

**表 7-1. Function Table**

| INPUTS(1) | | OUTPUT (2) |
|---|---|---|
| A | B | Y |
| H | H | H |
| L | X | L |
| X | L | L |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State


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# 8 Device and Documentation Support

## 8.1 Documentation Support (Analog)

### 8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**表 8-1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN74LV08A-Q1 | Click here | Click here | Click here | Click here | Click here |

## 8.2 ドキュメントの更新通知を受け取る方法

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## 8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

# 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LV08ATPWRG4Q1 | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | LV08ATQ |
| SN74LV08ATPWRG4Q1.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | LV08ATQ |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN74LV08A-Q1 :**

- Catalog : SN74LV08A

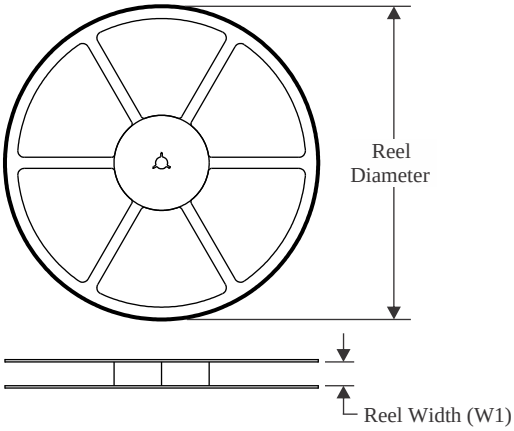
- Enhanced Product : SN74LV08A-EP

NOTE: Qualified Version Definitions:

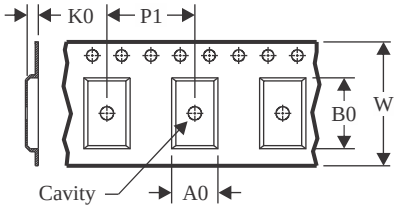
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

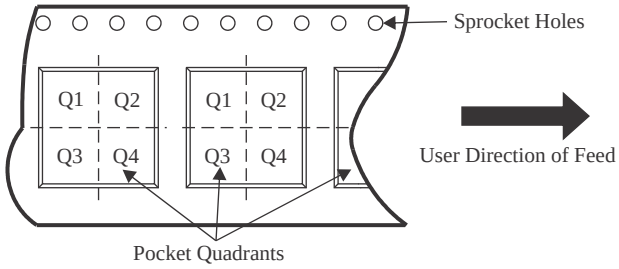



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

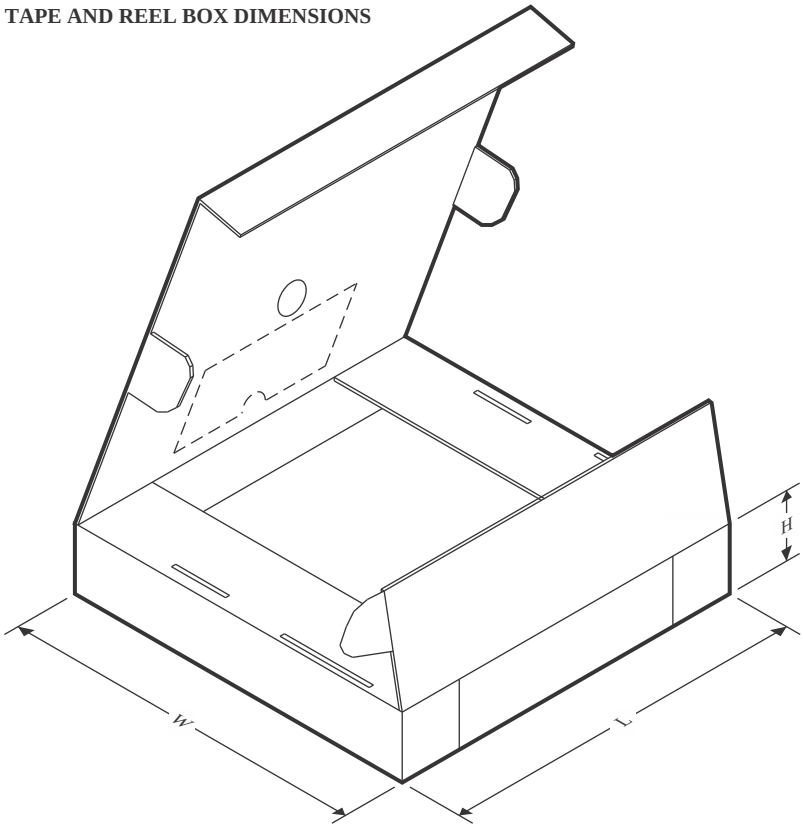
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV08ATPWRG4Q1 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

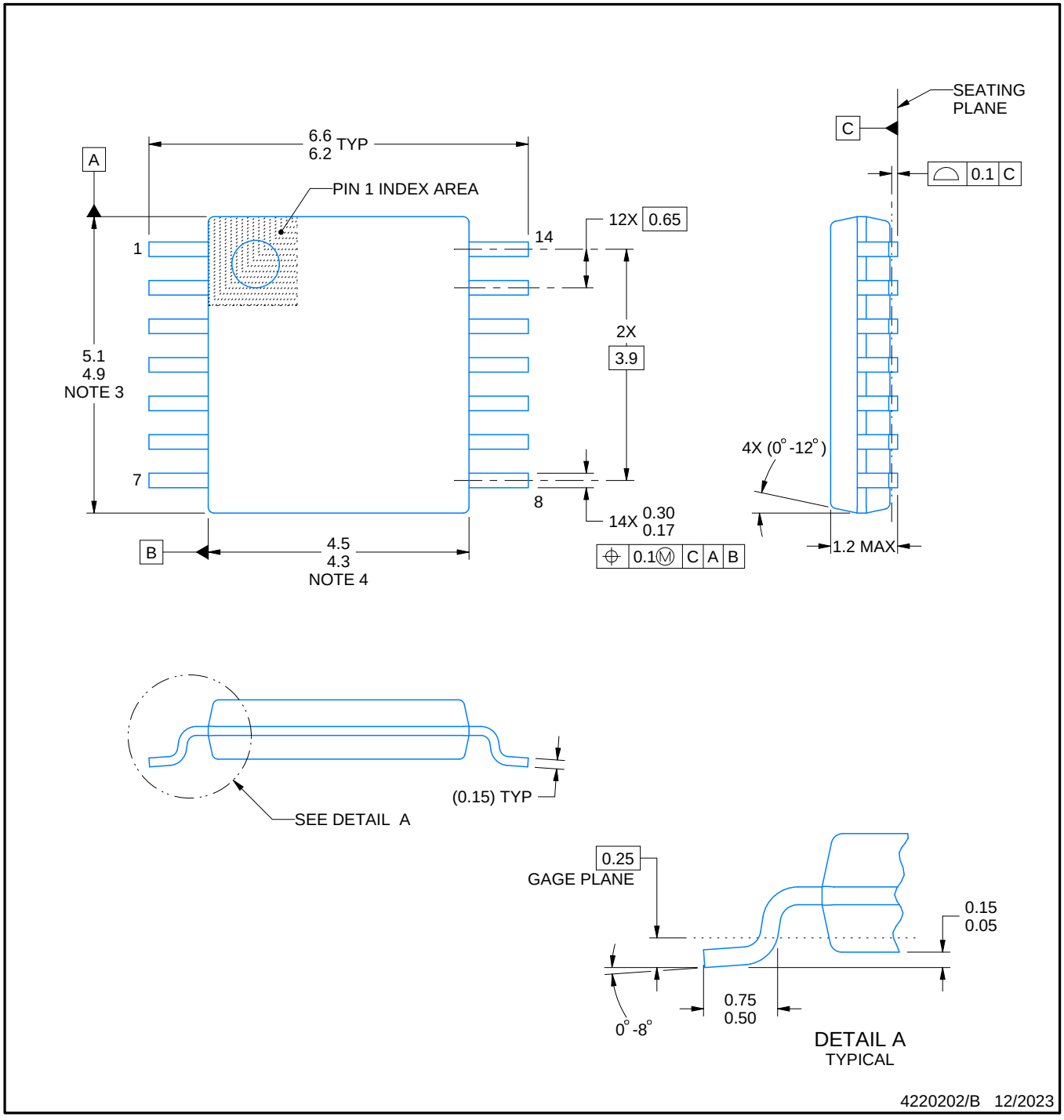
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LV08ATPWRG4Q1 | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |

# PACKAGE OUTLINE

## PW0014A

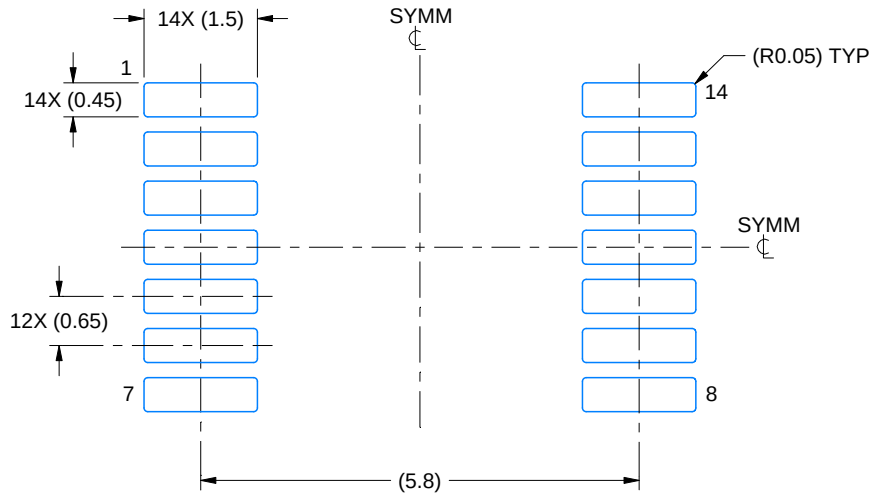
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

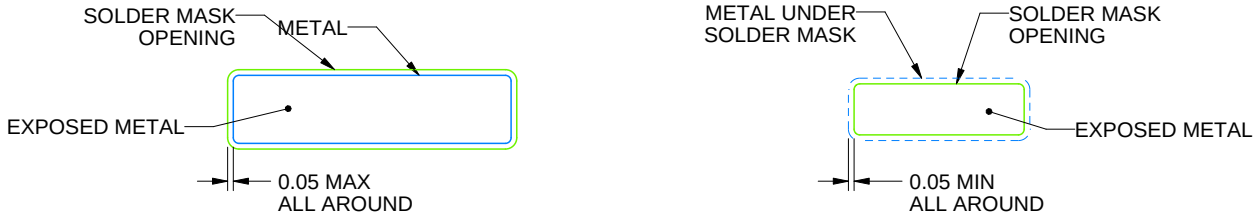



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

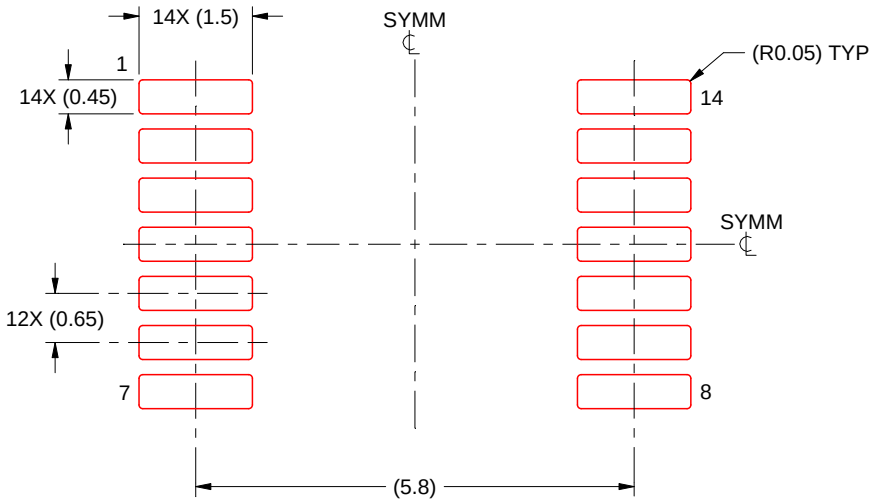



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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