TEXAS INSTRUMENTS
SN74LV125A
JAJSOL6O – DECEMBER 1997 – REVISED MAY 2022

# SN74LV125A 3 ステート出力搭載クワッド・バス・バッファ・ゲート

## 1 特長

- 2V～5.5V の $V_{CC}$ で動作
- 最大 $t_{pd}$:6ns (5V 時)
- 標準 $V_{OLP}$ (出力グランド・バウンス)
  < 0.8V ($V_{CC}$ = 3.3V、$T_A$ = 25℃)
- 標準 $V_{OHV}$ (出力 $V_{OH}$ アンダーシュート)
  > 2.3 V ($V_{CC}$ = 3.3V、$T_A$ = 25℃)
- すべて
  のポートで混在モード電圧動作をサポート
- $I_{off}$ により部分的パワーダウン・モード動作をサポート
- JESD 17 準拠で 250mA 超のラッチアップ性能
- JESD 22 を超える ESD 保護
  - 人体モデルで 4000V
  - マシン・モデルで 200V
  - デバイス帯電モデルで 2000V

## 2 アプリケーション

- 流量計
- ソリッド・ステート・ドライブ (SSD):エンタープライズ
- PoE (Power Over Ethernet)
- プログラマブル・ロジック・コントローラ
- モータ駆動および制御
- 電子 POS

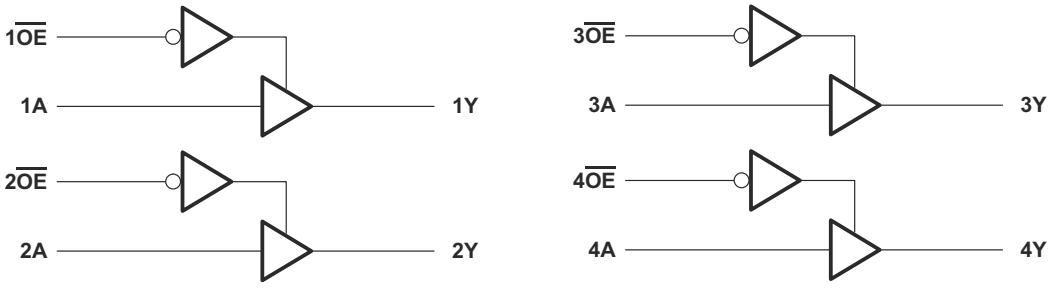
## 3 概要

SN74LV125A クワッド・バス・バッファ・ゲートは、2V～5.5V の $V_{CC}$ で動作するように設計されています。

**製品情報**

| 部品番号(1) | パッケージ | 本体サイズ (公称) |
|---|---|---|
| SN74LV125A | DGV (TVSOP) (14) | 3.60mm × 4.40mm |
| | D (SOIC) (14) | 8.65mm × 3.90mm |
| | NS (SO) (14) | 10.20mm × 5.30mm |
| | DB (SSOP) (14) | 6.20mm × 5.30mm |
| | PW (TSSOP) (14) | 5.00mm × 4.40mm |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。




**Simplified Schematic**

# Table of Contents



## 4 Revision History

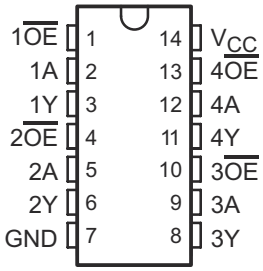
| Changes from Revision N (January 2015) to Revision O (May 2022) | Page |
|---|---|
| • Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards | 4 |

| Changes from Revision M (December 2014) to Revision N (January 2015) | Page |
|---|---|
| • Added $T_j$ spec to *Absolute Maximum Ratings* table | 4 |
| • Added text to *Overview* section | 9 |

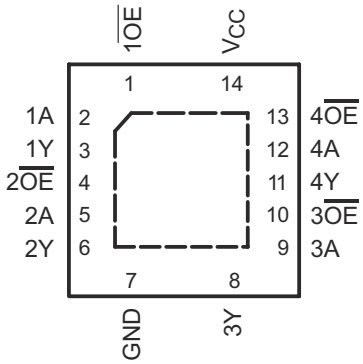
| Changes from Revision L (April 2005) to Revision M (December 2014) | Page |
|---|---|
| • 「アプリケーション」セクション、「製品情報」表、「端子機能」表、「ESD 定格」表、「熱に関する情報」表、「代表的特性」セクション、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 | 1 |
| • 「注文情報」表を削除 | 1 |
| • Changed MAX operating temperature to 125°C in *Recommended Operating Conditions* table. | 5 |

## 5 Pin Configuration and Functions

SN74LV125A . . . D, DB, DGV, N, NS, OR PW PACKAGE (TOP VIEW)




SN74LV125A . . . RGY PACKAGE (TOP VIEW)




### Pin Functions

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | 1$\overline{OE}$ | I | Output Enable 1, Active Low |
| 2 | 1A | I | 1A Input |
| 3 | 1Y | O | 1Y Output |
| 4 | 2$\overline{OE}$ | I | Output Enable 2, Active Low |
| 5 | 2A | I | 2A Input |
| 6 | 2Y | O | 2Y Output |
| 7 | GND | — | Ground Pin |
| 8 | 3Y | O | 3Y Output |
| 9 | 3A | I | 3A Input |
| 10 | 3$\overline{OE}$ | I | Output Enable 3, Active Low |
| 11 | 4Y | O | 4Y Output |
| 12 | 4A | I | 4A Input |
| 13 | 4$\overline{OE}$ | I | Output Enable 4, Active Low |
| 14 | $V_{CC}$ | — | Power Pin |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

| | | | MIN[1] | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 7 | V |
| $V_I$ | Input voltage range[2] | | –0.5 | 7 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state[2] | | –0.5 | 7 | V |
| $V_O$ | Output voltage range[2] [3] | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±35 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±70 | mA |
| $T_j$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *セクション 6.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5-V maximum.

## 6.2 ESD Ratings

| | | | MAX | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1] | ±4000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2] | ±2000 | |
| | | Machine Model (MM) | ±200 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | SN74LV125A | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | $V_{CC}$ × 0.7 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | $V_{CC}$ × 0.7 | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $V_{CC}$ × 0.7 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | $V_{CC}$ × 0.3 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | High or low state | 0 | $V_{CC}$ | V |
| | | 3-state | 0 | 5.5 | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | μA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | –2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | –8 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | –16 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | μA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | 8 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 16 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 2.3 V to 2.7 V | | 200 | ns/V |
| | | $V_{CC}$ = 3 V to 3.6 V | | 100 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 20 | |
| $T_A$ | Operating free-air temperature | | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

## 6.4 Thermal Information

| THERMAL METRIC(1) | | SN74LV125A | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | D | DB | DGV | N | NS | PW | RGY | |
| | | 14 PINS | | | | | | | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 92.7 | 105.0 | 127.6 | 89.2 | 89.6 | 119.8 | 55.0 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 54.1 | 57.5 | 50.7 | 47.0 | 47.2 | 48.6 | 67.4 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 47.0 | 52.3 | 60.5 | 47.9 | 48.4 | 61.5 | 31.0 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 18.9 | 19.1 | 6.1 | 14.1 | 14.0 | 5.7 | 2.6 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 46.7 | 51.8 | 59.8 | 47.5 | 48.1 | 61.0 | 31.1 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | N/A | N/A | 11.6 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | 2 V to 5.5 V | $V_{CC}$ – 0.1 | | | $V_{CC}$ – 0.1 | | $V_{CC}$ – 0.1 | | V |
| | $I_{OH}$ = –2 mA | 2.3 V | 2 | | | 2 | | 2 | | |
| | $I_{OH}$ = –8 mA | 3 V | 2.48 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –16 mA | 4.5 V | 3.8 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 2 V to 5.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 2 mA | 2.3 V | | | 0.4 | | 0.4 | | 0.4 | |
| | $I_{OL}$ = 8 mA | 3 V | | | 0.44 | | 0.44 | | 0.44 | |
| | $I_{OL}$ = 16 mA | 4.5 V | | | 0.55 | | 0.55 | | 0.55 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 0 to 5.5 V | | | ±1 | | ±1 | | ±1 | µA |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±5 | | ±5 | | ±5 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 20 | | 20 | | 20 | µA |
| $I_{off}$ | $V_I$ or $V_O$ = 0 to 5.5 V | 0 | | | 5 | | 5 | | 5 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 1.6 | | | | | | pF |
| | | 5 V | | 1.6 | | | | | | |

## 6.6 Switching Characteristics, $V_{CC}$ = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | $C_L$ = 15 pF | | 6.8(1) | 13(1) | 1 | 15.5 | 1 | 17 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | | | 7(1) | 13(1) | 1 | 15.5 | 1 | 17 | |
| $t_{dis}$ | $\overline{OE}$ | Y | | | 5.1(1) | 14.7(1) | 1 | 17 | 1 | 18 | |
| $t_{pd}$ | A | Y | $C_L$ = 50 pF | | 8.7 | 16.5 | 1 | 18.5 | 1 | 20 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | | | 8.8 | 16.5 | 1 | 18.5 | 1 | 20 | |
| $t_{dis}$ | $\overline{OE}$ | Y | | | 7.3 | 18.2 | 1 | 20.5 | 1 | 21.5 | |
| $t_{sk(o)}$ | | | | | | 2 | | 2 | | 2 | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.7 Switching Characteristics, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range(unless otherwise noted) (see 図 7-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | $C_L$ = 15 pF | | 4.8(1) | 8(1) | 1 | 9.5 | 1 | 11 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | | | 4.8(1) | 8(1) | 1 | 9.5 | 1 | 10.5 | |
| $t_{dis}$ | $\overline{OE}$ | Y | | | 4.1(1) | 9.7(1) | 1 | 11.5 | 1 | 12.5 | |
| $t_{pd}$ | A | Y | $C_L$ = 50 pF | | 6.1 | 11.5 | 1 | 13 | 1 | 14.5 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | | | 6.2 | 11.5 | 1 | 13 | 1 | 14 | |
| $t_{dis}$ | $\overline{OE}$ | Y | | | 5.5 | 13.2 | 1 | 15 | 1 | 16 | |
| $t_{sk(o)}$ | | | | | | 1.5 | | 1.5 | | 1.5 | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.8 Switching Characteristics, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | $C_L$ = 15 pF | | 3.4(1) | 5.5(1) | 1 | 6.5 | 1 | 7.5 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | | | 3.4(1) | 5.1(1) | 1 | 6 | 1 | 7 | |
| $t_{dis}$ | $\overline{OE}$ | Y | | | 3.2(1) | 6.8(1) | 1 | 8 | 1 | 9 | |
| $t_{pd}$ | A | Y | $C_L$ = 50 pF | | 4.3 | 7.5 | 1 | 8.5 | 1 | 9.5 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | | | 4.4 | 7.1 | 1 | 8 | 1 | 9 | |
| $t_{dis}$ | $\overline{OE}$ | Y | | | 4 | 8.8 | 1 | 10 | 1 | 11 | |
| $t_{sk(o)}$ | | | | | | 1 | | 1 | | 1 | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.9 Noise Characteristics

$V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $T_A$ = 25°C

| PARAMETER(1) | | SN74LV125A | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.4 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.3 | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 3 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.31 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.99 | V |

(1) Characteristics are for surface-mount packages only.

## 6.10 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | $C_L$ = 50 pF, | f = 10 MHz | 3.3 V | 15.5 | pF |
| | | | | | 5 V | 17.6 | |

## 6.11 Typical Characteristics

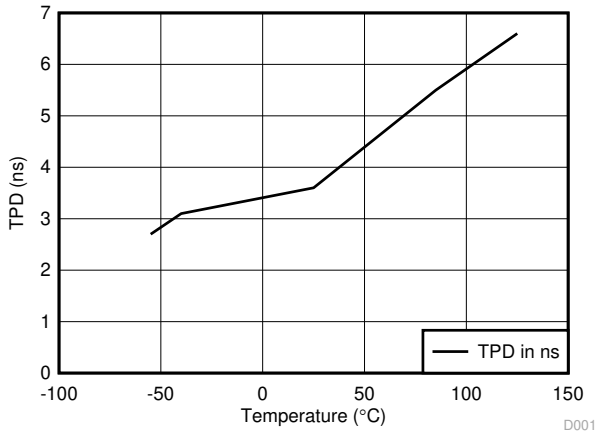



図 6-1. TPD vs Temperature

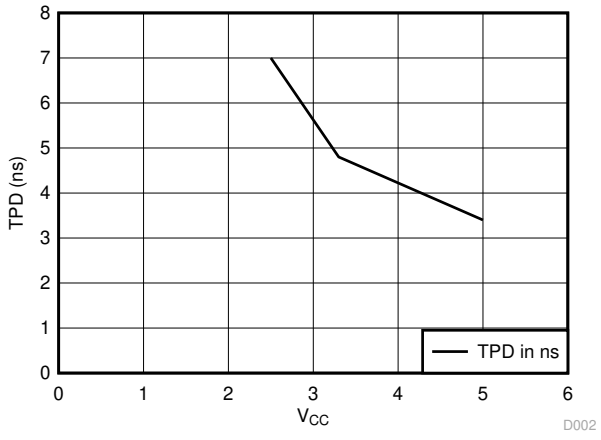
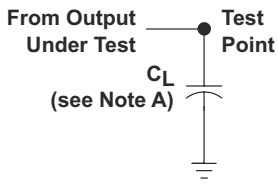


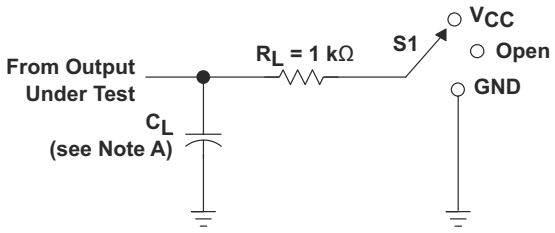

図 6-2. TPD vs $V_{CC}$ at 25°C

# 7 Parameter Measurement Information

## 7.1

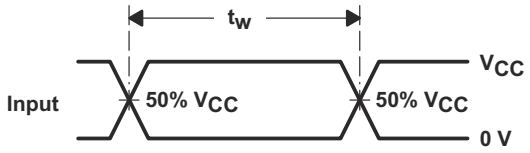



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

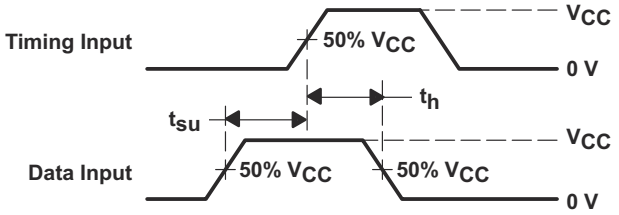



LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

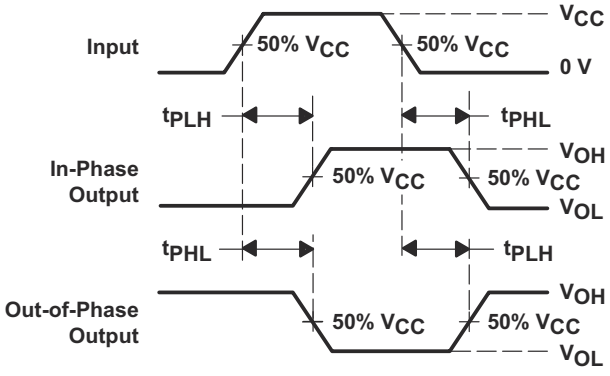
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |



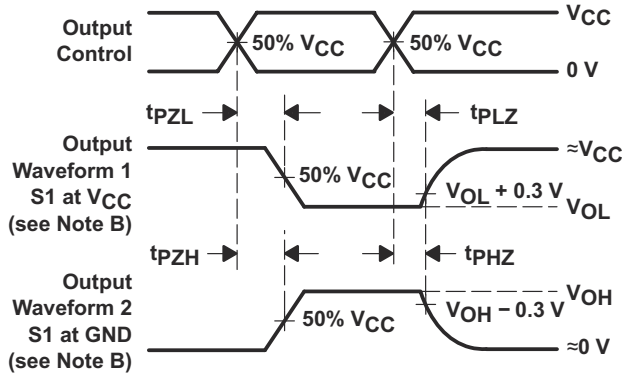

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PHL}$ and $t_{PLH}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**図 7-1. Load Circuit And Voltage Waveforms**

# 8 Detailed Description

## 8.1 Overview

The SN74LV125A quadruple bus buffer gate is designed for 2-V to 5.5-V $V_{CC}$ operation.

These devices feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high.

To ensure the high-impedance state during power up or power down, tie $\overline{OE}$ to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## 8.2 Functional Block Diagram

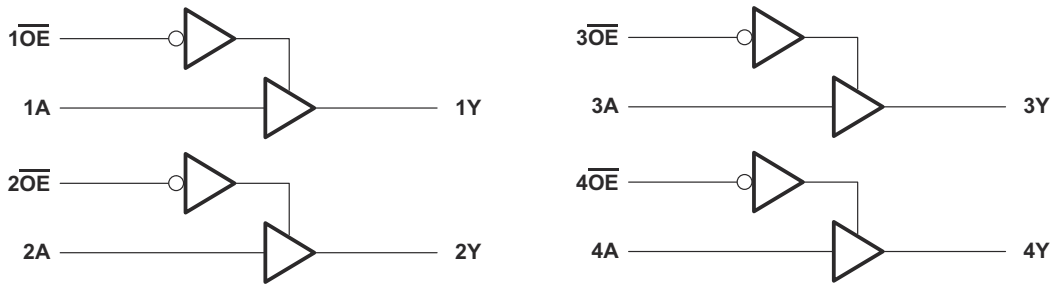



**図 8-1. Logic Diagram (Positive Logic)**

## 8.3 Feature Description

- Wide operating voltage range
  - Operates from 2 V to 5.5 V
- Allows down-voltage translation
  - Inputs accept voltages to 5.5 V
- $I_{off}$ Feature
  - Supports Live Insertion, Partial Power-Down Mode, and Back-Drive Protection

## 8.4 Device Functional Modes

**表 8-1. Function Table (Each Buffer)**

| INPUTS(1) | | OUTPUT(2) |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The SN74LV125A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates minimize overshoot and undershoot on the outputs. The inputs are 5.5-V tolerant at any valid $V_{CC}$, making it ideal for translating down to $V_{CC}$.

## 9.2 Typical Application

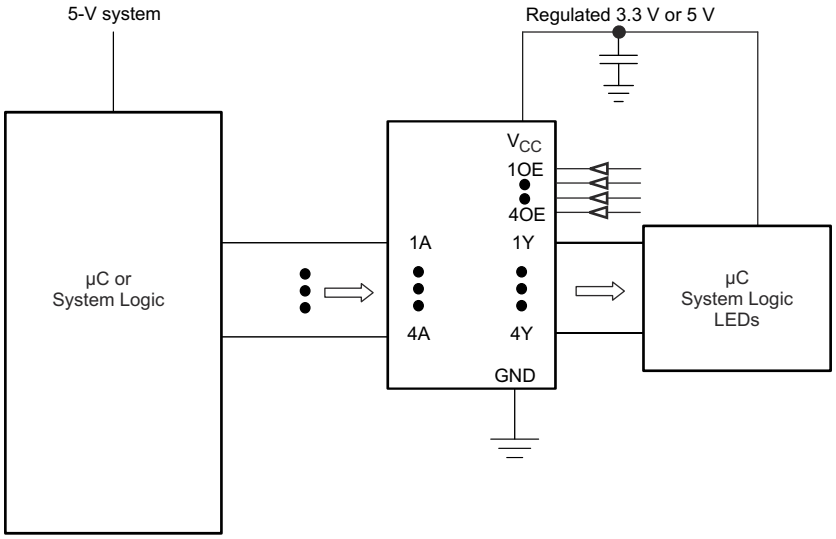



**図 9-1. Typical Application Schematic**

### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For rise time and fall time specifications, see Δt/ΔV in the *セクション 6.3* table.
   - For specified High and low levels, see $V_{IH}$ and $V_{IL}$ in the *セクション 6.3* table.
2. Recommend Output Conditions
   - Load currents should not exceed 35 mA per output and 70 mA total for the part.
   - Outputs should not be pulled above $V_{CC}$.

### 9.2.3 Application Curves

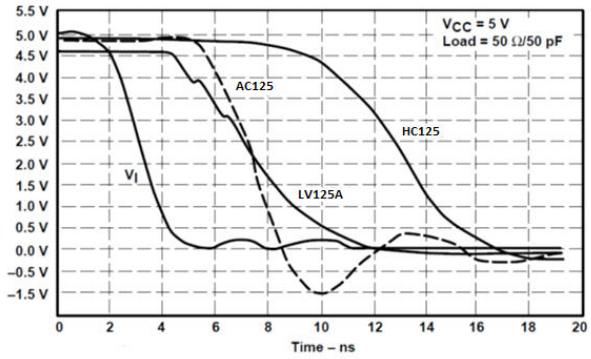



**図 9-2. Switching Characteristics Comparison**

## 10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *セクション 6.3* table.

Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple $V_{CC}$ pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

# 11 Layout

## 11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in 図 11-1 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

## 11.2 Layout Example

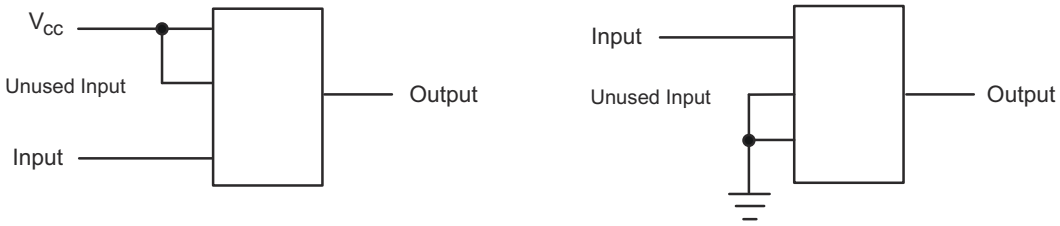



**図 11-1. Layout Diagram**

# 12 Device and Documentation Support

## 12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**表 12-1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN74LV125A | Click here | Click here | Click here | Click here | Click here |

## 12.2 Trademarks

すべての商標は、それぞれの所有者に帰属します。

## 12.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.4 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LV125AD | Obsolete | Production | SOIC (D) \| 14 | - | - | Call TI | Call TI | -40 to 125 | LV125A |
| SN74LV125ADBR | Active | Production | SSOP (DB) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV125A |
| SN74LV125ADBR.A | Active | Production | SSOP (DB) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV125A |
| SN74LV125ADGVR | Active | Production | TVSOP (DGV) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV125A |
| SN74LV125ADGVR.A | Active | Production | TVSOP (DGV) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV125A |
| SN74LV125ADR | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LV125A |
| SN74LV125ADR.A | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV125A |
| SN74LV125AN | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 125 | SN74LV125AN |
| SN74LV125AN.A | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 125 | SN74LV125AN |
| SN74LV125ANSR | NRND | Production | SOP (NS) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 74LV125A |
| SN74LV125ANSR.A | NRND | Production | SOP (NS) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 74LV125A |
| SN74LV125APW | Obsolete | Production | TSSOP (PW) \| 14 | - | - | Call TI | Call TI | -40 to 125 | LV125A |
| SN74LV125APWR | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LV125A |
| SN74LV125APWR.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV125A |
| SN74LV125APWRE4 | Active | Production | TSSOP (PW) \| 14 | 2000 \| null | No | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV125A |
| SN74LV125APWRE4 | Active | Production | TSSOP (PW) \| 14 | 2000 \| null | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV125A |
| SN74LV125APWRE4.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| null | No | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV125A |
| SN74LV125APWRE4.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| null | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV125A |
| SN74LV125APWRG4 | Active | Production | TSSOP (PW) \| 14 | 2000 \| null | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV125A |
| SN74LV125APWRG4 | Active | Production | TSSOP (PW) \| 14 | 2000 \| null | No | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV125A |
| SN74LV125APWRG4.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| null | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV125A |
| SN74LV125APWRG4.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| null | No | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV125A |
| SN74LV125APWT | Obsolete | Production | TSSOP (PW) \| 14 | - | - | Call TI | Call TI | -40 to 125 | LV125A |
| SN74LV125ARGYR | Active | Production | VQFN (RGY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LV125A |
| SN74LV125ARGYR.A | Active | Production | VQFN (RGY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LV125A |
| SN74LV125ARGYRG4 | Active | Production | VQFN (RGY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LV125A |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LV125A :**

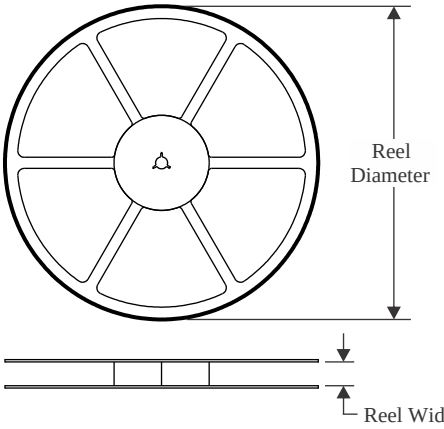
- Automotive : SN74LV125A-Q1

NOTE: Qualified Version Definitions:

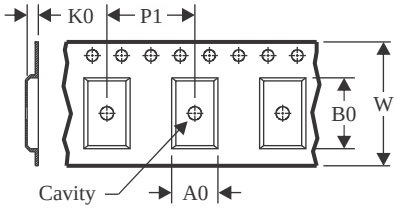
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

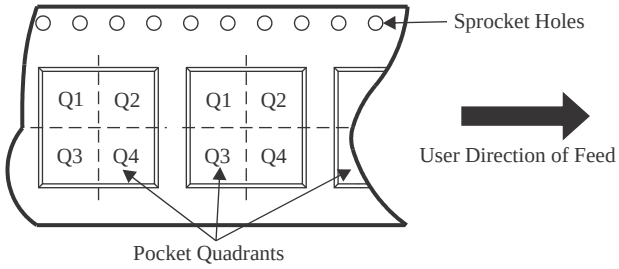



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

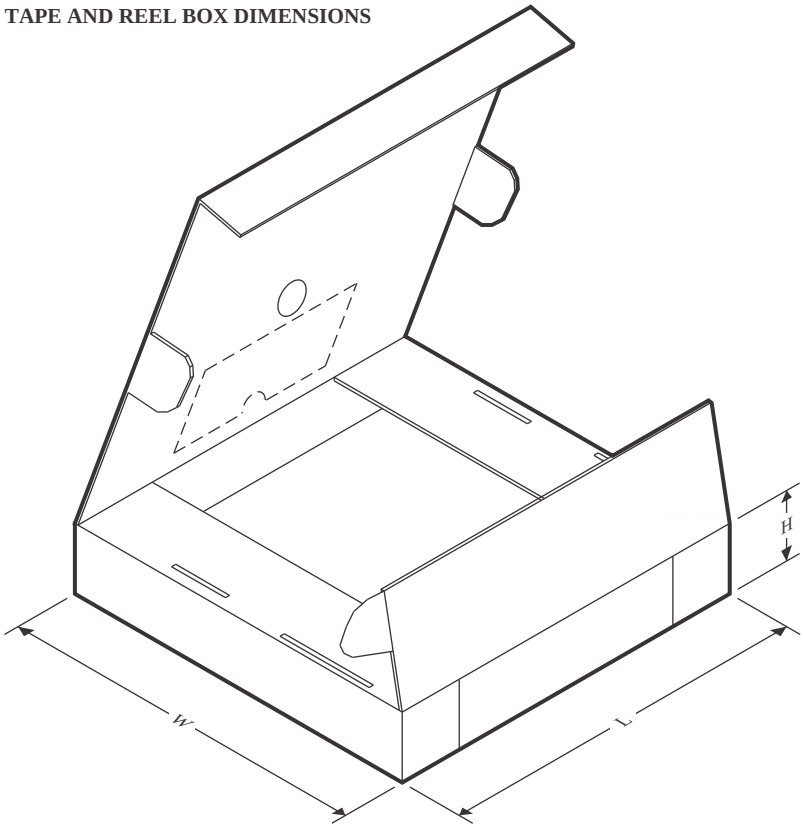
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV125ADBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74LV125ADGVR | TVSOP | DGV | 14 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV125ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV125ANSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV125APWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV125ARGYR | VQFN | RGY | 14 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |

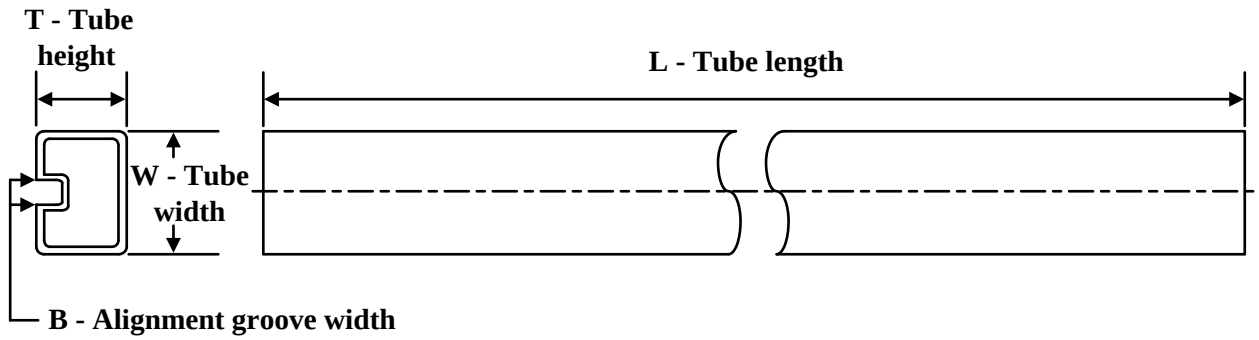
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LV125ADBR | SSOP | DB | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LV125ADGVR | TVSOP | DGV | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LV125ADR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74LV125ANSR | SOP | NS | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LV125APWR | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LV125ARGYR | VQFN | RGY | 14 | 3000 | 353.0 | 353.0 | 32.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74LV125AN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LV125AN.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |

# GENERIC PACKAGE VIEW

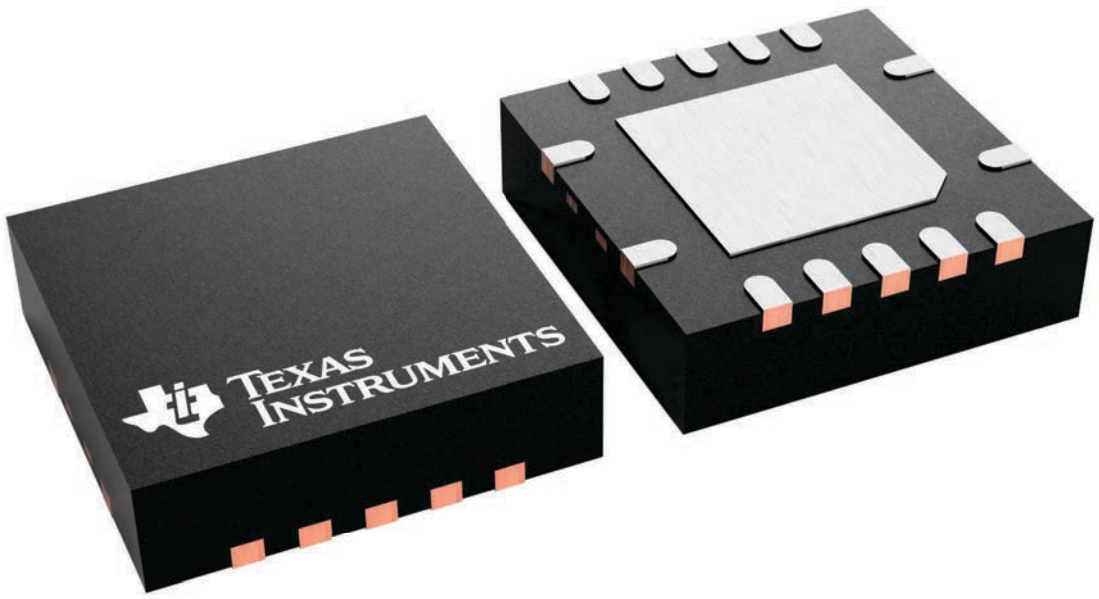
## RGY 14

## VQFN - 1 mm max height

**3.5 x 3.5, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



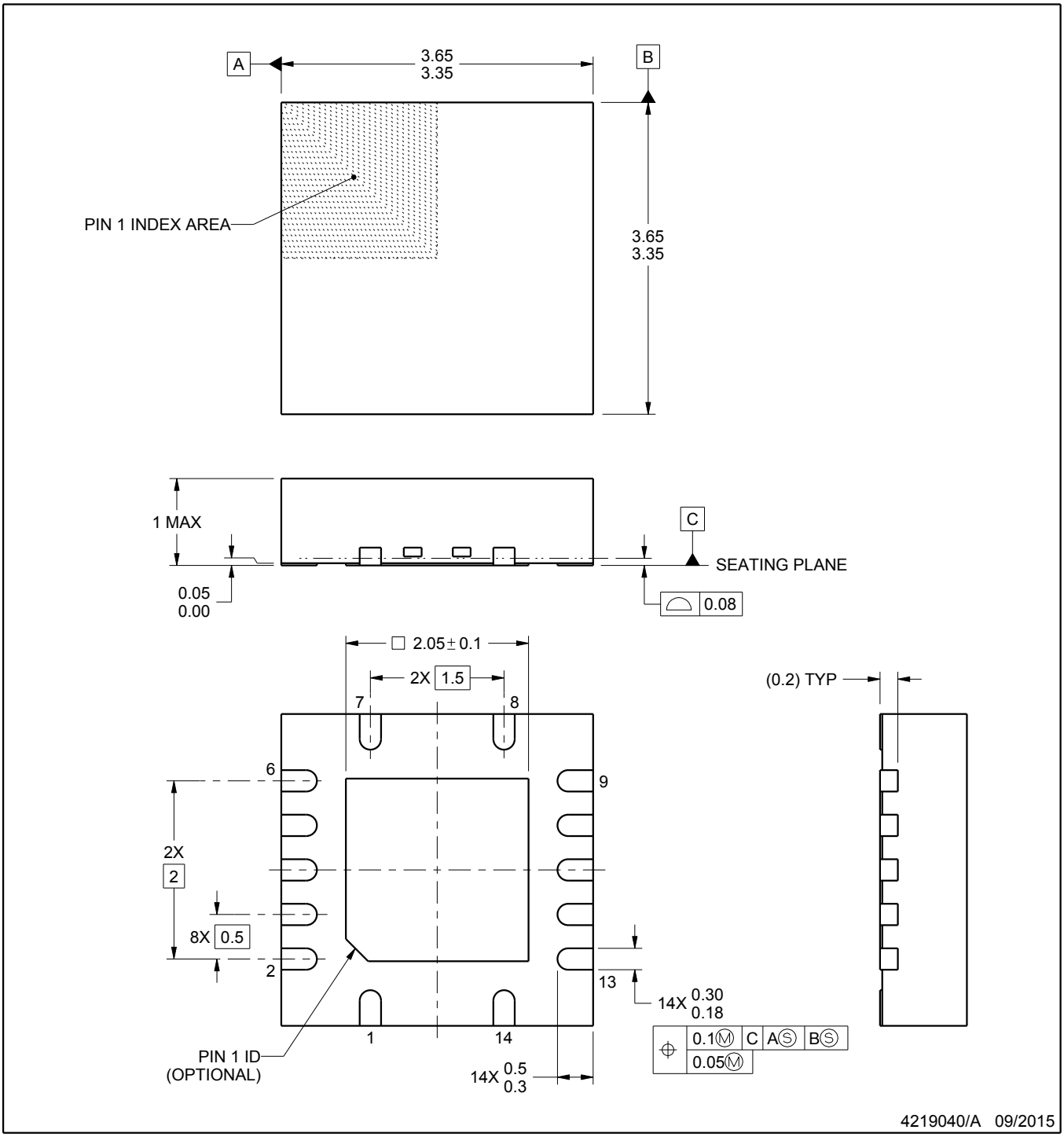

4231541/A

# PACKAGE OUTLINE

## RGY0014A

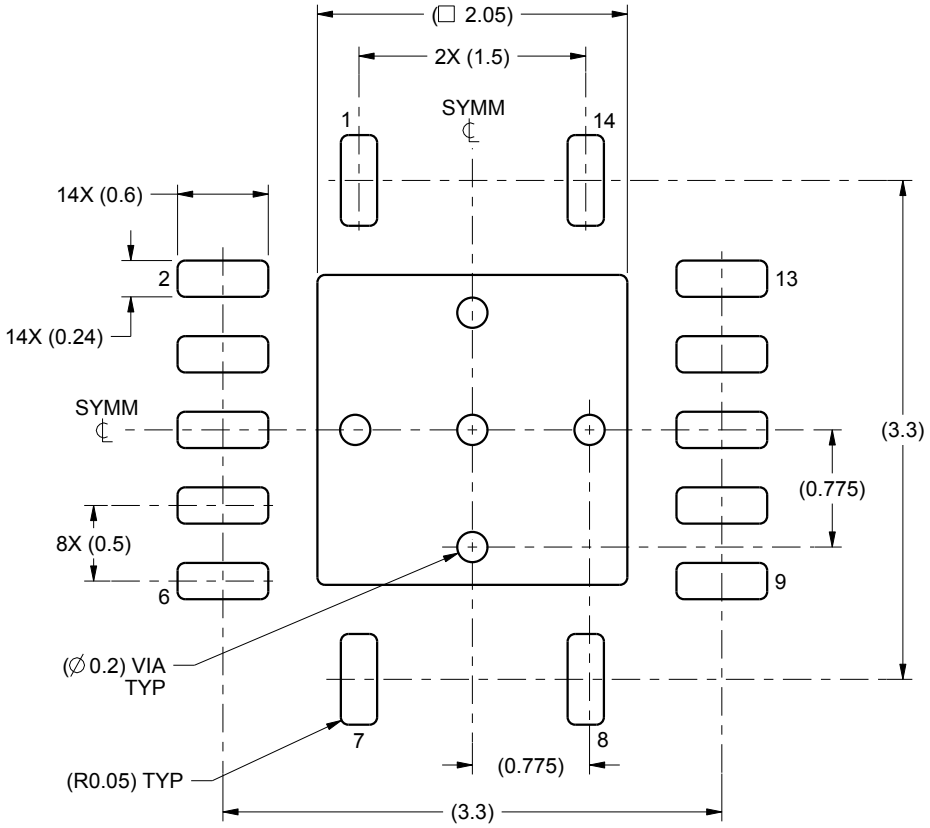
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

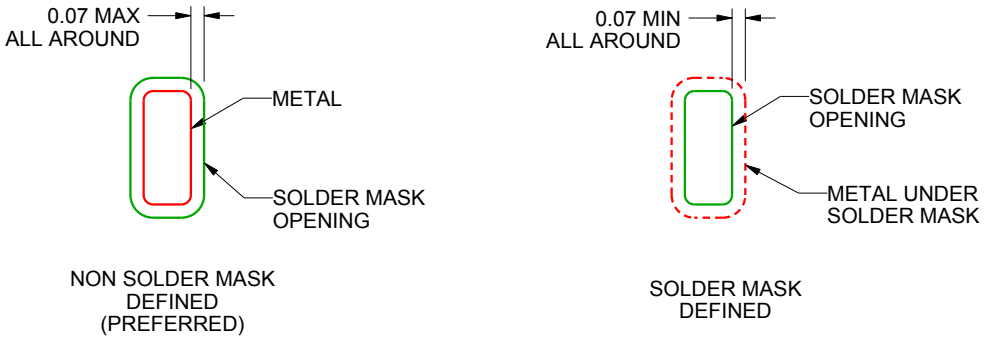



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:20X

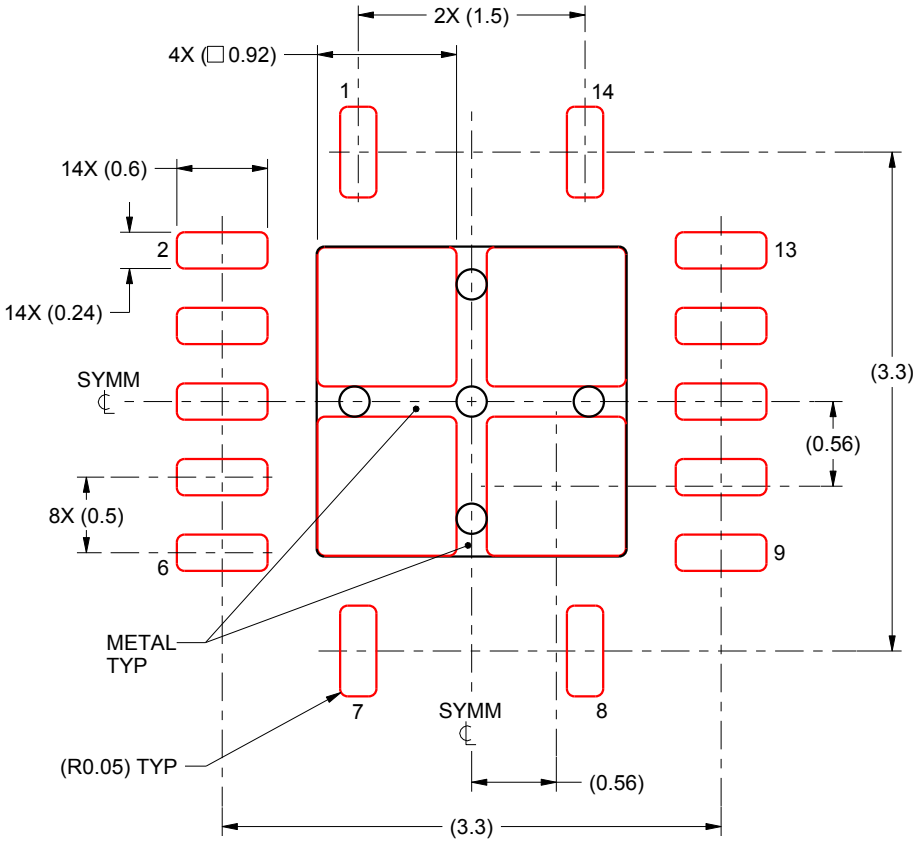



SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



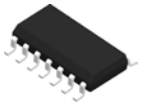

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

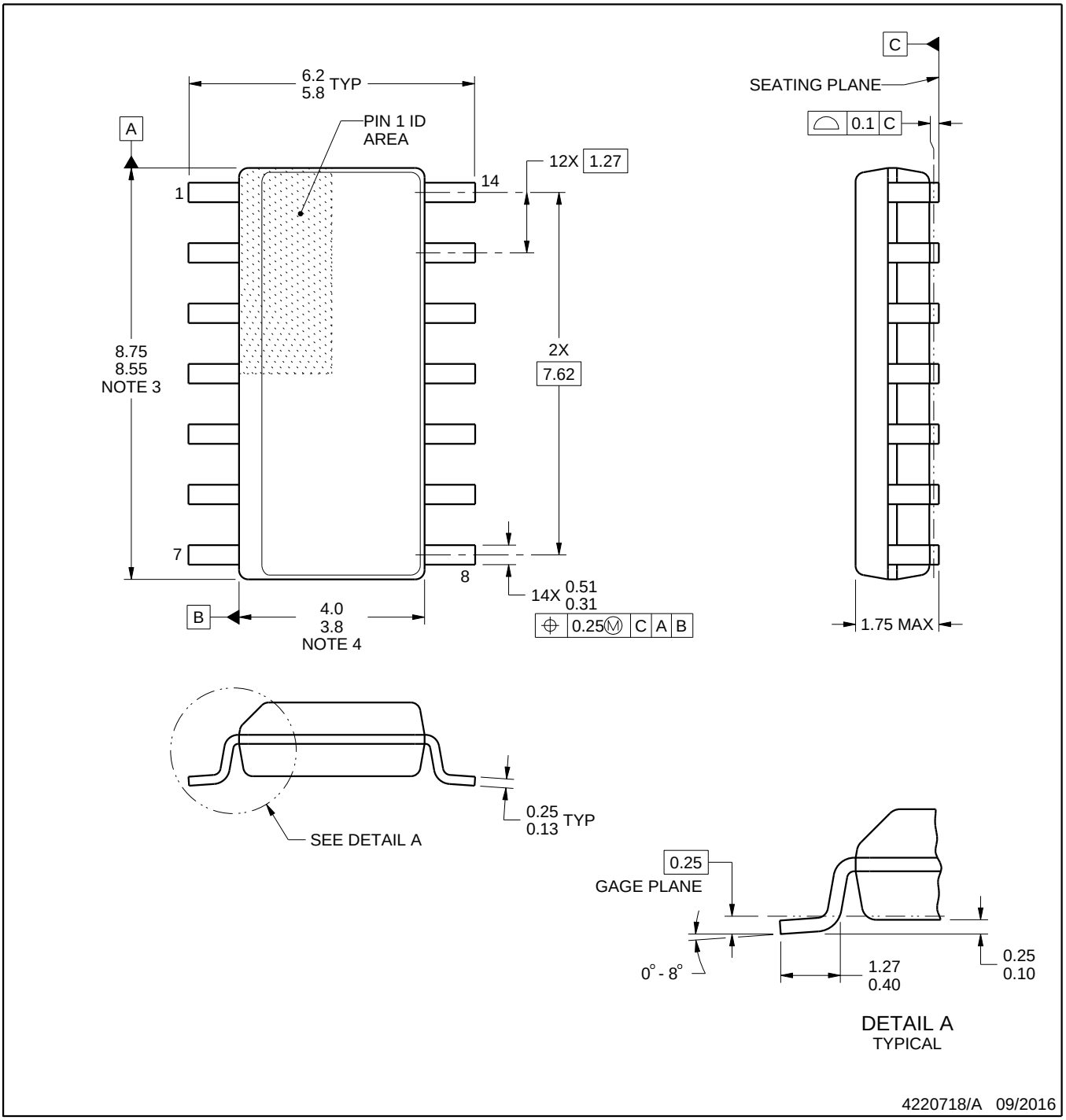


# PACKAGE OUTLINE

## D0014A

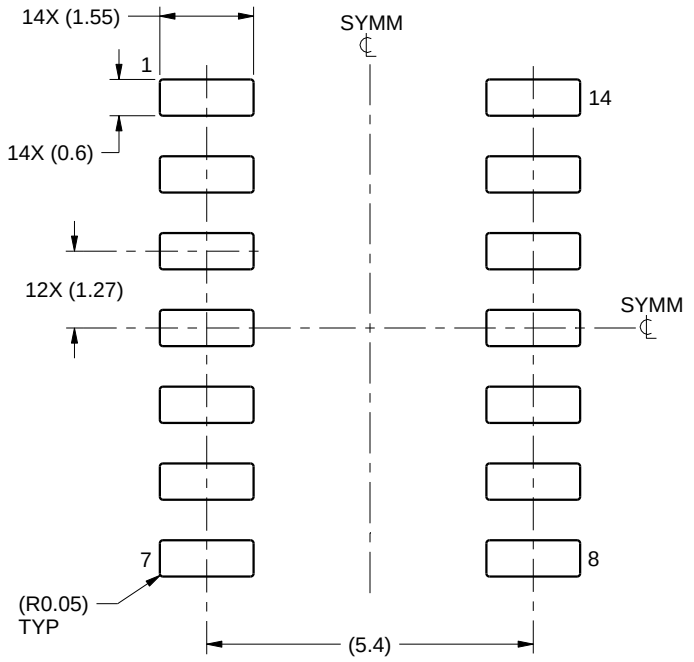
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

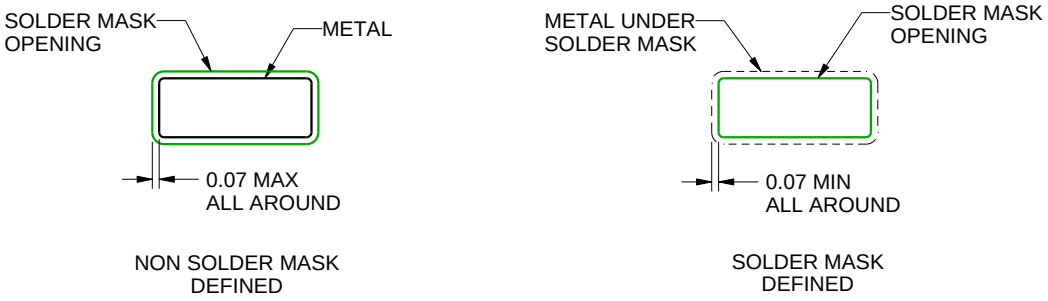



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

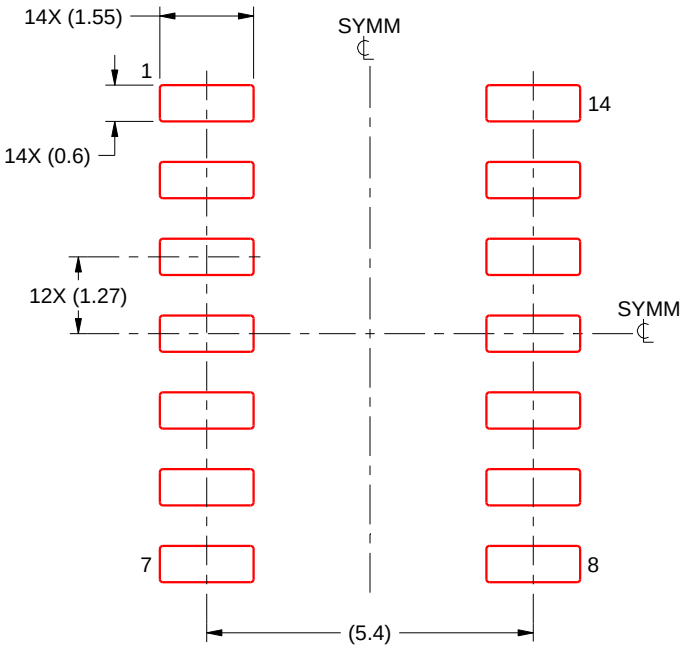
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

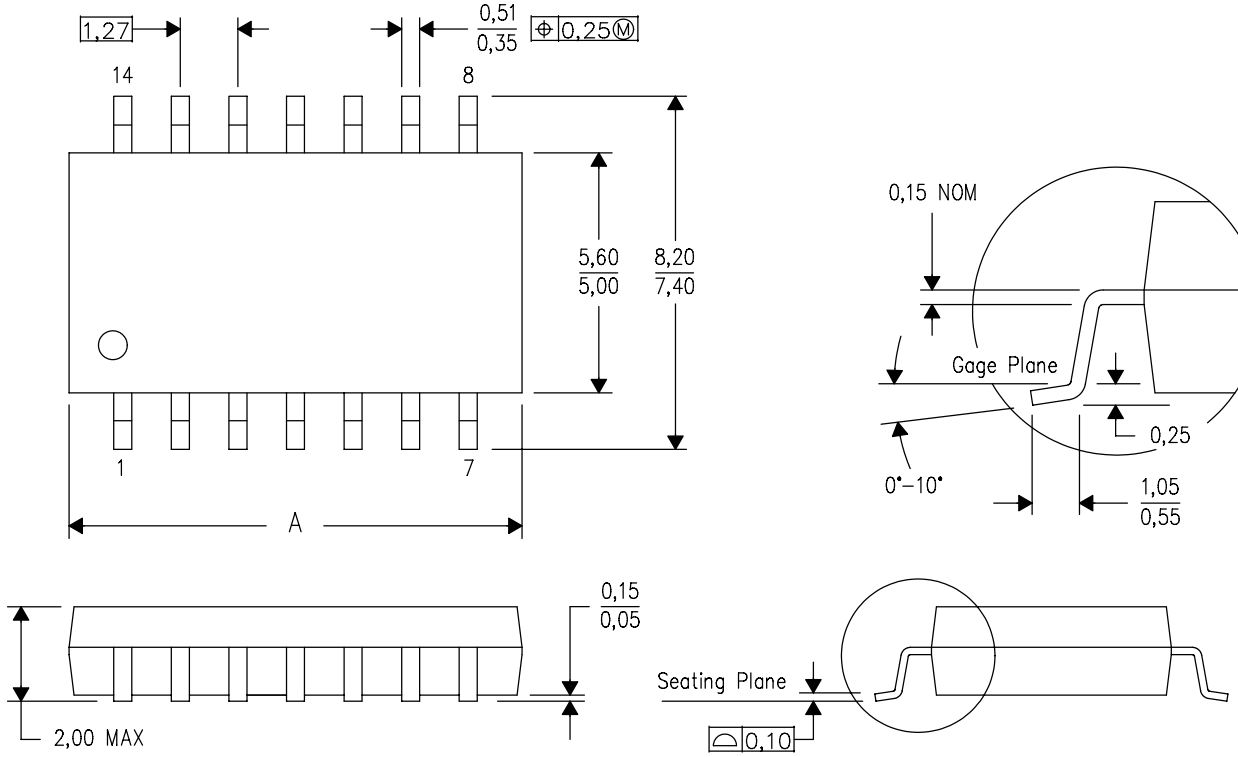
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



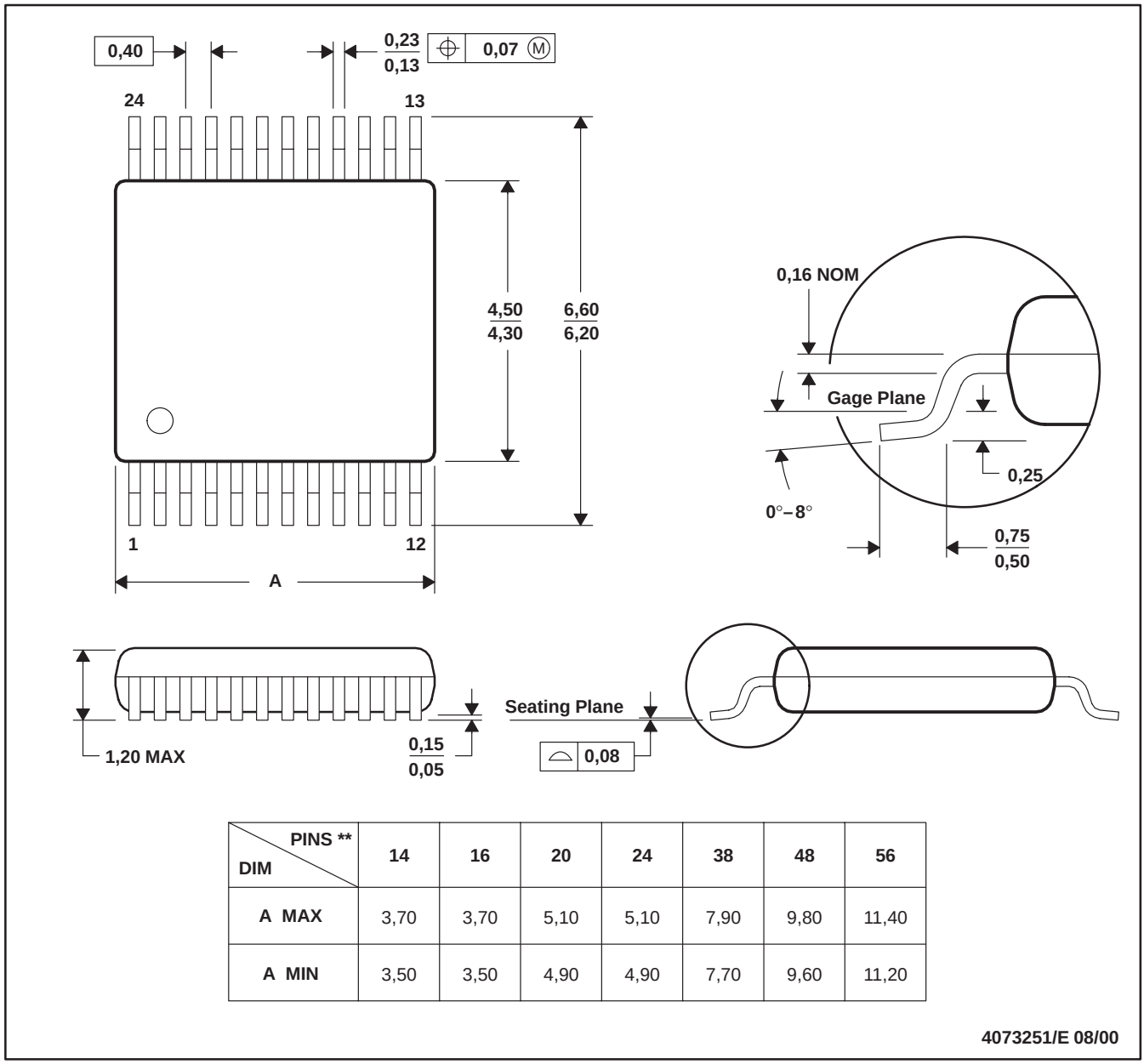

| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

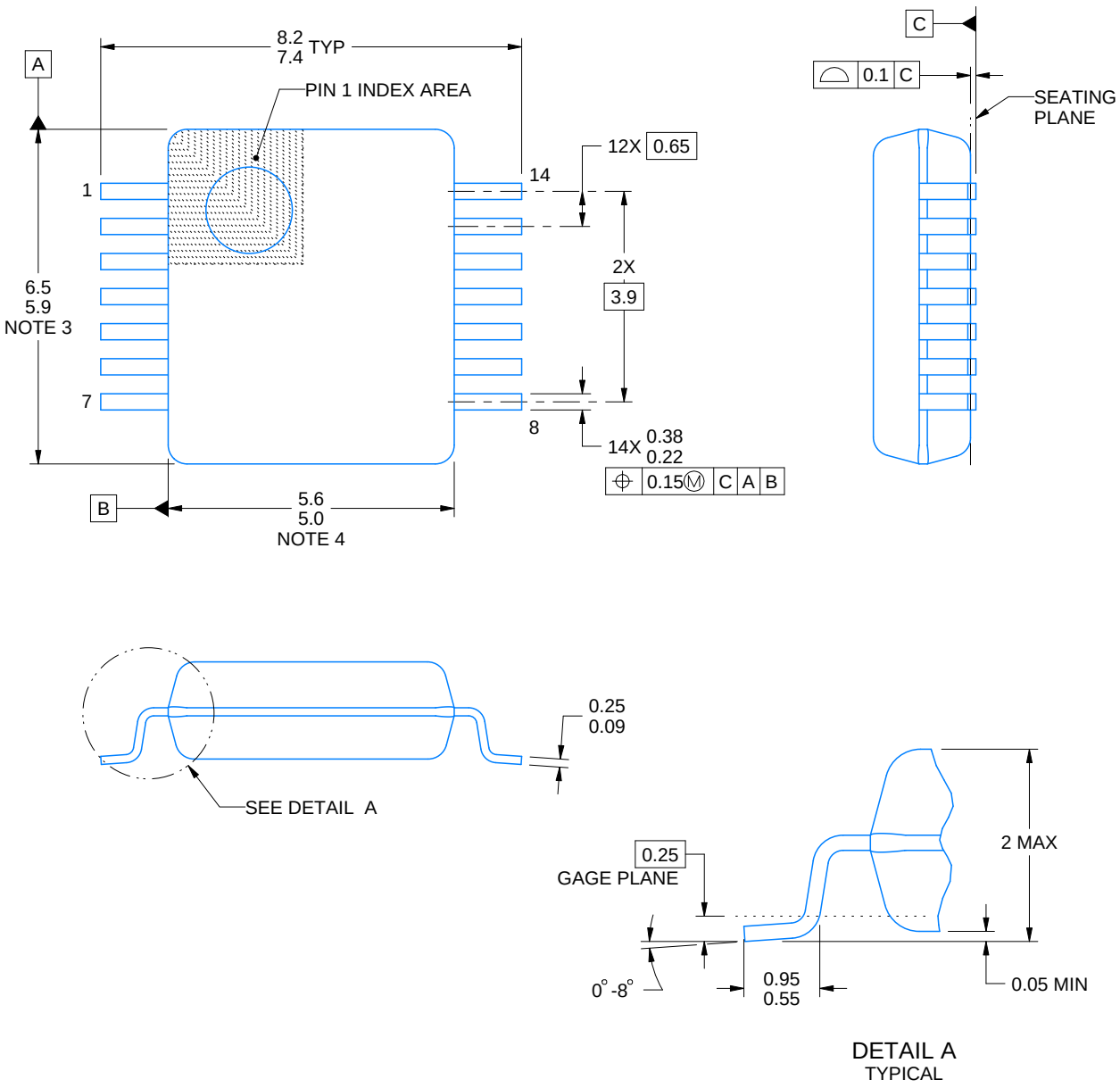
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

# PACKAGE OUTLINE

## DB0014A

## SSOP - 2 mm max height

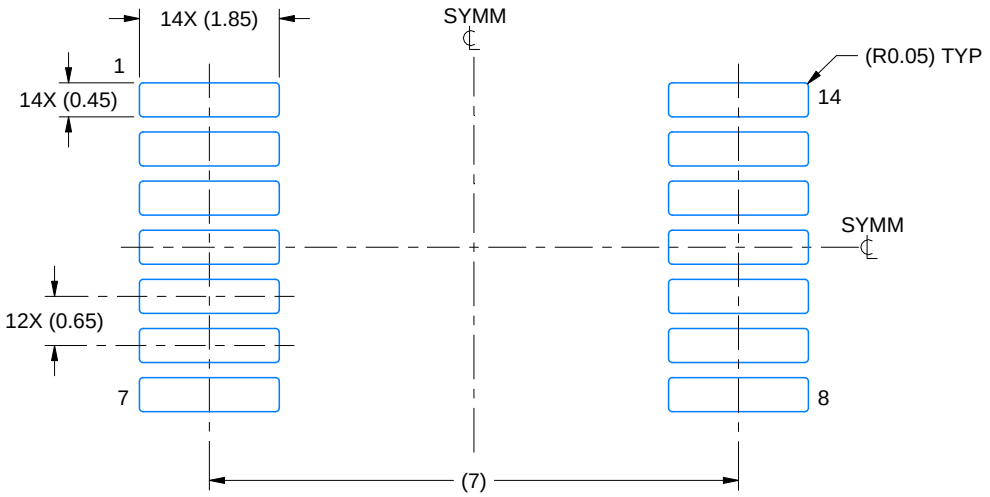
SMALL OUTLINE PACKAGE



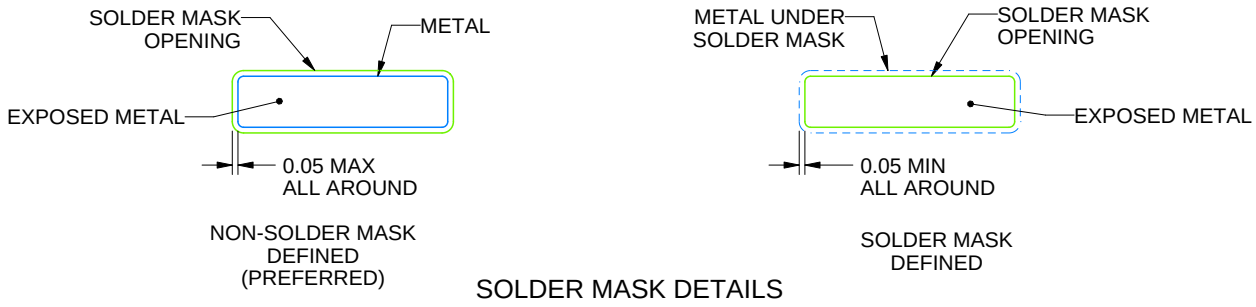

4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

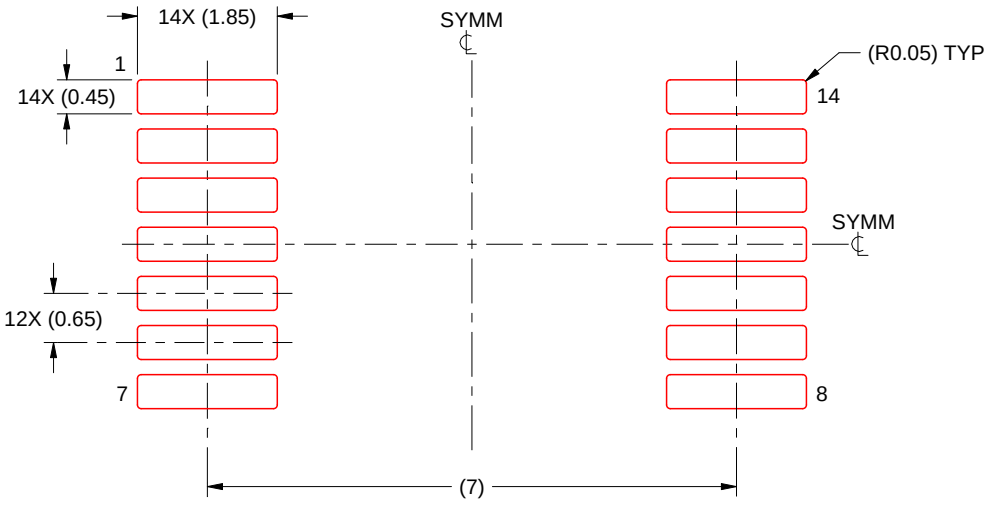



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

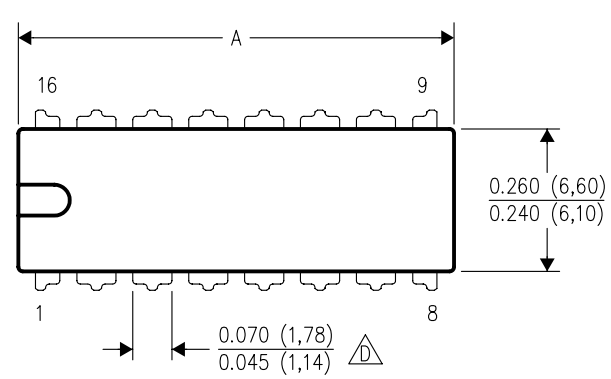
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

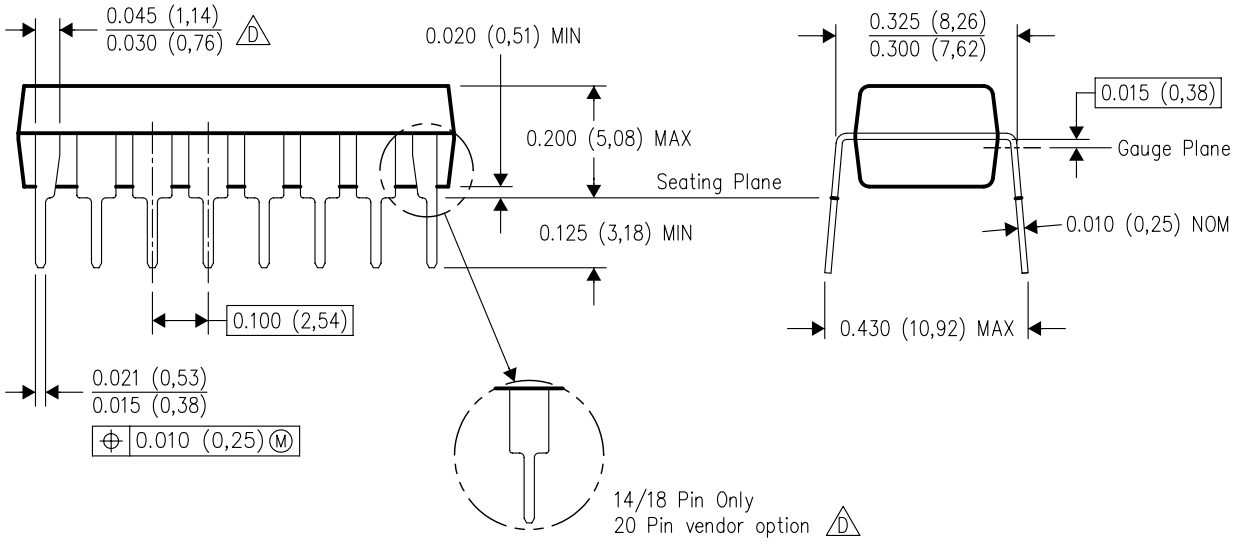
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

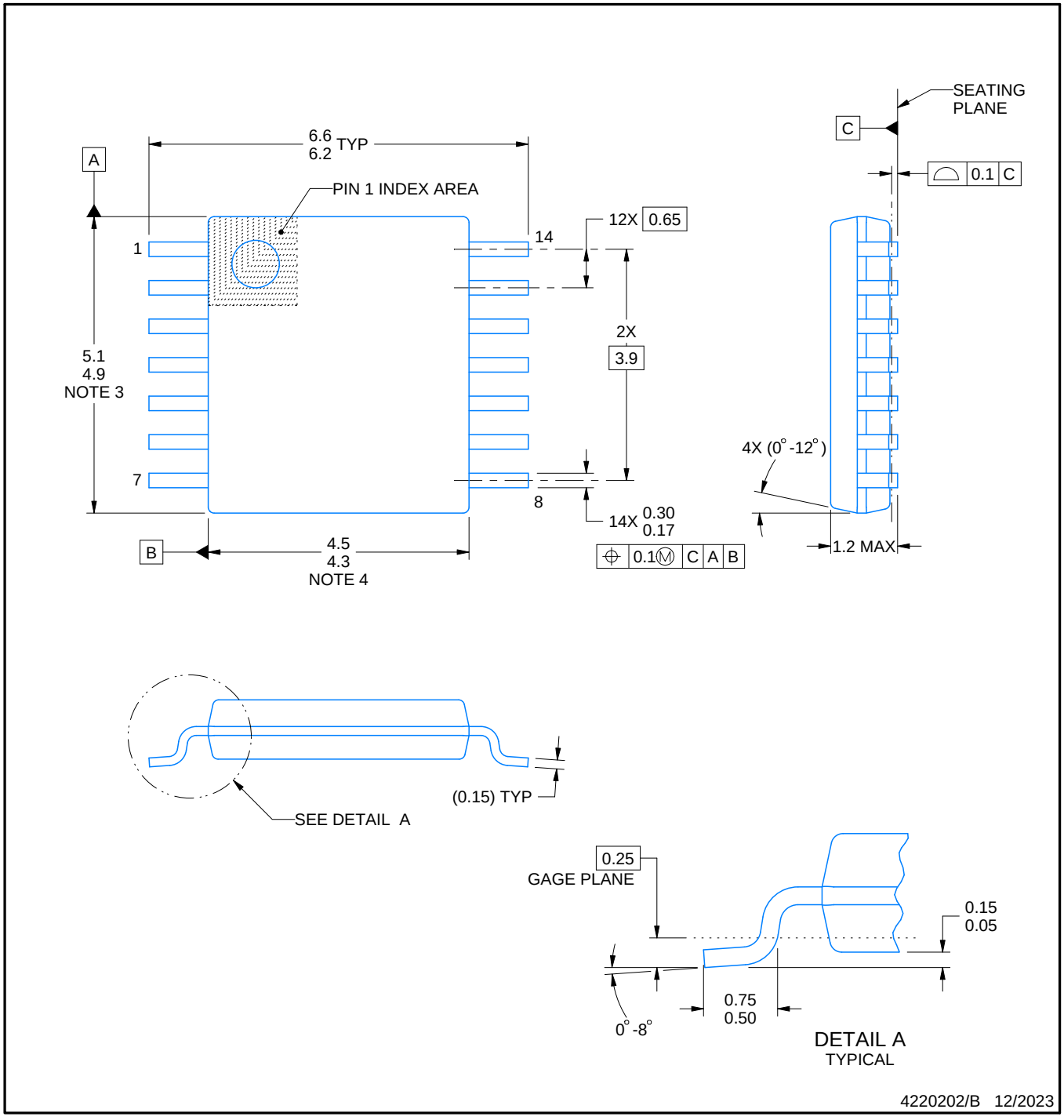
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

# PACKAGE OUTLINE

## PW0014A

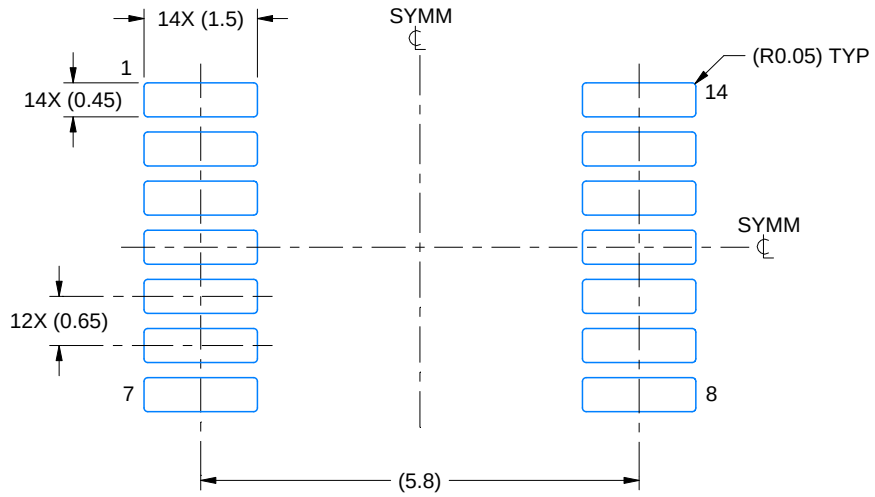
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

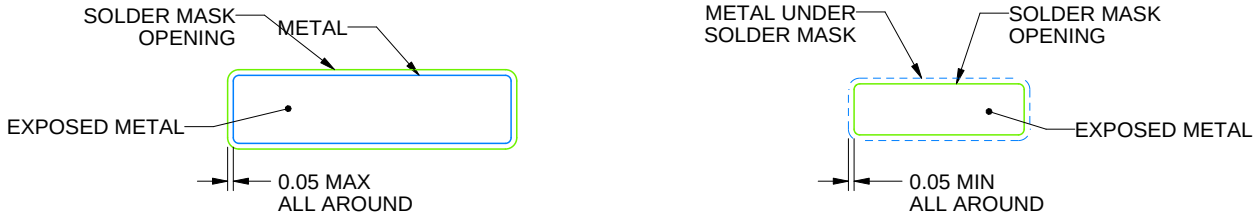



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

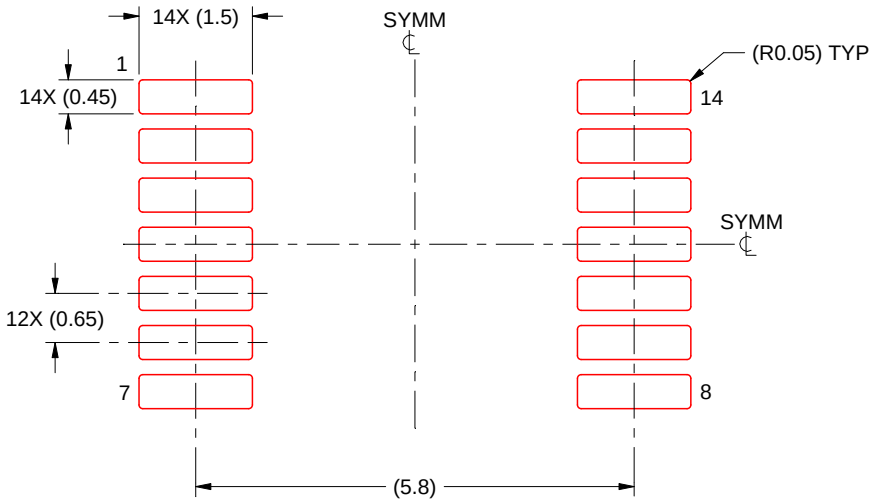



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。



最終更新日：2025 年 10 月