SN74LV14A ヘキサ・シュミット・トリガ・インバータ

1 特長

- V_{CC} 範囲:2 V ～ 5.5 V
- 最大 t_{pd}:10ns (5V 時)
- 標準 V_{OLP} (出力グランド・バウンス)
  < 0.8V (V_{CC} = 3.3V、T_A = 25℃)
- 標準 V_{OHV} (出力 V_{OH} アンダーシュート)
  > 2.3V (V_{CC} = 3.3V、T_A = 25℃)
- すべて
  のポートで混在モード電圧動作をサポート
- I_{off} により部分的パワーダウン・モード動作をサポート
- JESD 17 準拠で 250mA 超のラッチアップ性能

2 アプリケーション

- ネットワーク・スイッチ
- ウェアラブルなヘルスケア / フィットネス機器
- PDA
- LCD TV
- 電力インフラストラクチャ

3 説明

これらのヘキサ・シュミット・トリガ・インバータは、2V～5.5V V_{CC} 動作用に設計されています。

SN74LV14A デバイスには、6 つの独立したインバータがあります。これらのデバイスはブール関数 $Y = \overline{A}$ を実行します。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
SN74LV14A	TVSOP (14)	3.60mm × 4.40mm
	SOIC (14)	8.65mm × 3.91mm
	SSOP (14)	6.20mm × 5.30mm
	TSSOP (14)	5.00mm × 4.40mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



図 3-1. 概略回路図

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4 Revision History

Changes from Revision K (September 2014) to Revision L (December 2022) — **Page**

- 文書全体にわたって表、図、相互参照の形式を更新 ... 1

Changes from Revision J (September 1997) to Revision K (September 2014) — **Page**

- ドキュメントを新しいテキサス・インスツルメンツのデータシートのフォーマットに更新 ... 1
- 「注文情報」表を削除 ... 1
- 「アプリケーション」を追加 ... 1
- 「製品情報」表を追加 ... 1
- Added Pin Functions table ... 3
- Changed MAX operating temperature to 125°C in Recommended Operating Conditions table. ... 4
- Added Thermal Information table ... 5
- Added Typical Characteristics ... 7
- Added Application and Implementation section ... 10
- Added Power Supply Recommendations and Layout sections ... 12

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5 Pin Configuration and Functions

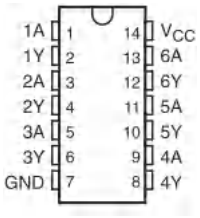


図 5-1. SN74LV14A D, DB, DGV, NS OR PW Package Top View

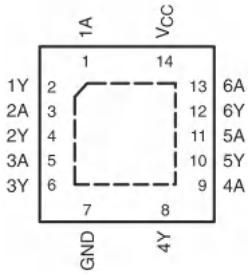


図 5-2. SN74LV14A RGY Package Top View

Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	SN74LV14A			
	D, DB, DGV, NS, PW	RGY		
1A	1	1	I	Input 1A
1Y	2	2	O	Output 1Y
2A	3	3	I	Input 2A
2Y	4	4	O	Output 2Y
3A	5	5	I	Input 3A
3Y	6	6	O	Output 3Y
4Y	8	8	O	Output 4Y
4A	9	9	I	Input 4A
5Y	10	10	O	Output 5Y
5A	11	11	I	Input 5A
6Y	12	12	O	Output 6Y
6A	13	13	I	Input 6A
GND	7	7	—	Ground Pin
NC	—	—	—	No Connection
V_{CC}	14	14	—	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
V_O	Output voltage range(2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *セクション 6.1* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *セクション 6.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5-V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	
		Machine Model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN74LV14A		UNIT
			MIN	MAX	
V_{CC}	Supply voltage		2	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	μA
		V_{CC} = 2.3 V to 2.7 V		–2	mA
		V_{CC} = 3 V to 3.6 V		–6	
		V_{CC} = 4.5 V to 5.5 V		–12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		6	
		V_{CC} = 4.5 V to 5.5 V		12	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

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6.4 Thermal Information

THERMAL METRIC[1]		SN74LV14A						UNIT
		D	DB	DGV	NS	PW	RGY	
		14 PINS						
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.9	107.4	130.4	91.4	122.6	57.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	59.9	53.4	49.0	51.3	70.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	49.2	54.7	63.5	50.2	64.4	33.6	
ψ_{JT}	Junction-to-top characterization parameter	20.7	21.0	7.3	15.3	6.8	3.5	
ψ_{JB}	Junction-to-board characterization parameter	48.9	51.2	62.8	49.8	63.8	33.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	–	–	–	14.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	SN74LV14A –40°C to 85°C			SN74LV14A –40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{T+}	Positive-going threshold		2.5 V			1.75			1.75	V
			3.3 V			2.31			2.31	
			5 V			3.5			3.5	
V_{T-}	Negative-going threshold		2.5 V	0.75			0.75			V
			3.3 V	0.99			0.99			
			5 V	1.5			1.5			
ΔV_T ($V_{T+} - V_{T-}$)	Hysteresis		2.5 V	0.25			0.25			V
			3.3 V	0.33			0.33			
			5 V	0.5			0.5			
V_{OH}	High-level output voltage	I_{OH} = –50 µA	2 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1			V
		I_{OH} = –2 mA	2.3 V	2			2			
		I_{OH} = –6 mA	3 V	2.48			2.48			
		I_{OH} = –12 mA	4.5 V	3.8			3.8			
V_{OL}	Low-level output voltage	I_{OL} = 50 µA	2 V to 5.5 V			0.1			0.1	V
		I_{OL} = 2 mA	2.3 V			0.4			0.4	
		I_{OL} = 6 mA	3 V			0.44			0.44	
		I_{OL} = 12 mA	4.5 V			0.55			0.55	
I_I	Input leakage current	V_I = V_{CC} or GND	0 to 5.5 V			±1			±1	µA
I_{CC}	Static supply current	V_I = V_{CC} or GND, I_O = 0	5.5 V			20			20	µA
I_{off}	Input/Output Power-Off Leakage Current	V_I or V_O = 0 to 5.5 V	0			5			5	µA
C_i	Input capacitance	V_I = V_{CC} or GND	3.3 V		2.3			2.3		pF
			5 V		2.3			2.3		

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6.6 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74LV14A –40°C to 85°C		SN74LV14A –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	C_L = 15 pF		10.2(1)	19.7(1)	1	22	1	23	ns
			C_L = 50 pF		13.3	24	1	27	1	28	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.7 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74LV14A –40°C to 85°C		SN74LV14A –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	C_L = 15 pF		7.3(1)	12.8(1)	1	15	1	16	ns
			C_L = 50 pF		9.6	16.3	1	18.5	1	19.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.8 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74LV14A –40°C to 85°C		SN74LV14A –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	C_L = 15 pF		5.1(1)	8.6(1)	1	10	1	11	ns
			C_L = 50 pF		6.7	10.6	1	12	1	13	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.9 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C(1)

		SN74LV14A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic		0.2	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic		–0.1	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic		3.1		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

6.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF f = 10 MHz	3.3 V	8.8	pF
			5 V	9.6	

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6.11 Typical Characteristics

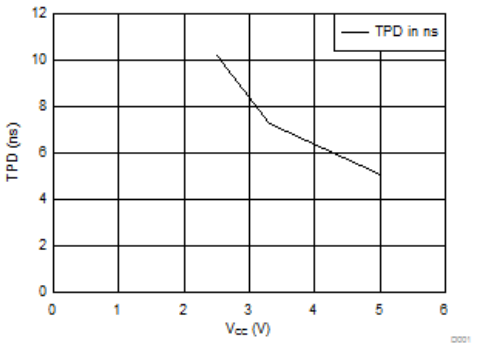


図 6-1. TPD vs V_{CC}

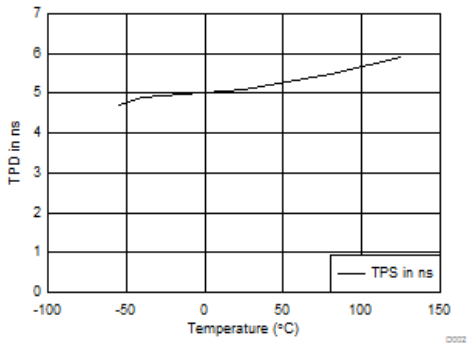
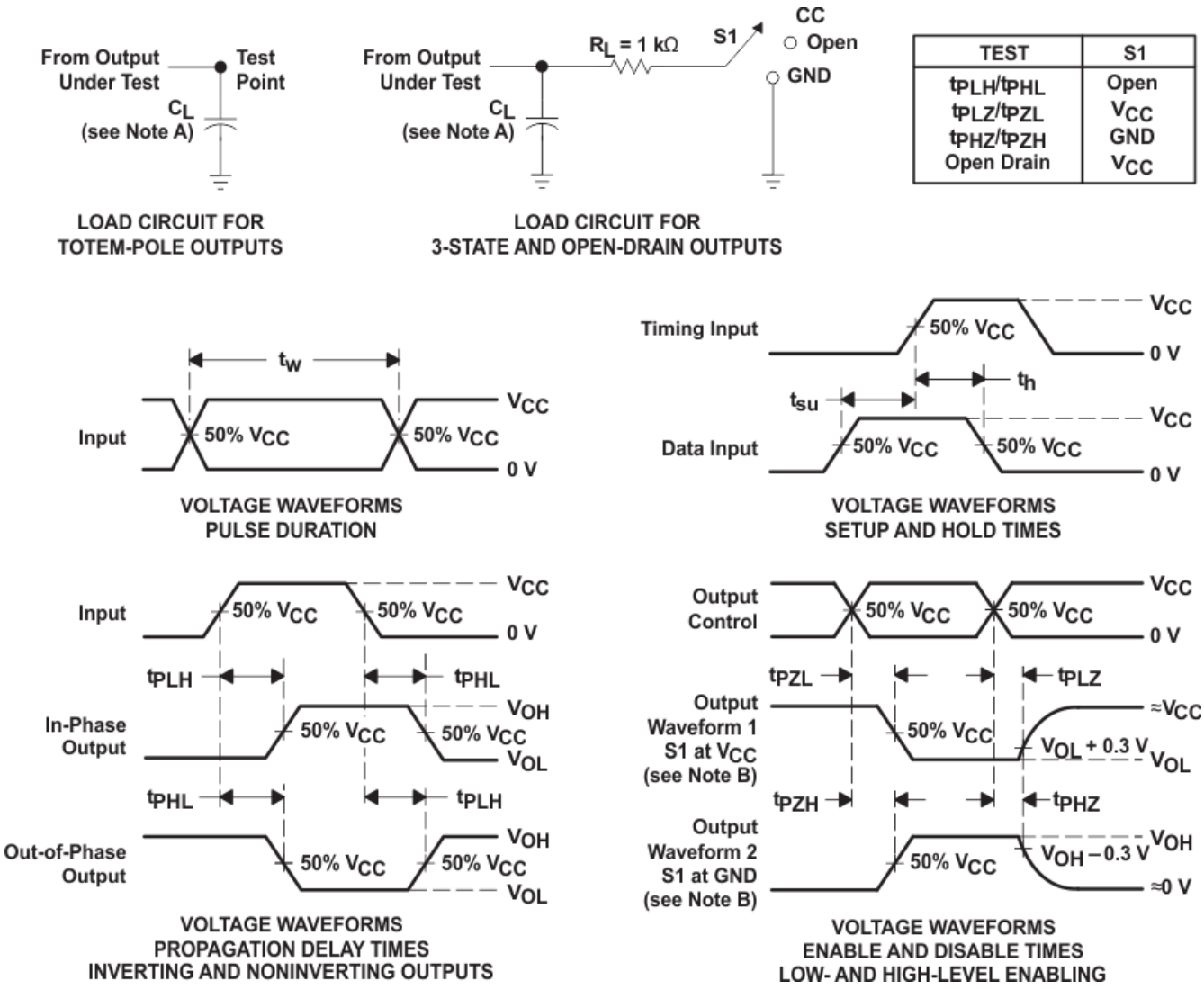


図 6-2. TPD vs Temperature

7 Parameter Measurement Information

7.1



A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

図 7-1. Load Circuit and Voltage Waveforms

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8 Detailed Description

8.1 Overview

These hex Schmitt-trigger inverters are designed for 2 V to 5.5 V V_{CC} operation.

The SN74LV14A devices contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$.

These devices are fully specified for partial-power-down application using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

8.2 Functional Block Diagram



図 8-1. Logic Diagram, Each Inverter (Positive Logic)

8.3 Feature Description

- Wide operating voltage range
  - Operates From 2 V to 5.5 V
- Allows up or down voltage translation
  - Inputs and outputs accept voltages to 5.5 V
- I_{off} feature
  - Allows voltages on the inputs and outputs when V_{CC} is 0 V
- Schmitt-trigger inputs allow for slow or noisy inputs

8.4 Device Functional Modes

表 8-1. Function Table (Each Inverter)

INPUT(1) A	OUTPUT(2) Y
H	L
L	H

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

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9 Application and Implementation

注

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9.1 Application Information

Schmitt triggers should be used anytime you need to translate a sign wave into a square wave as shown in 図 9-1. They may also be used where a slow or noisy input needs to be sped up or cleaned up as shown in 図 9-2.

9.2 Typical Application

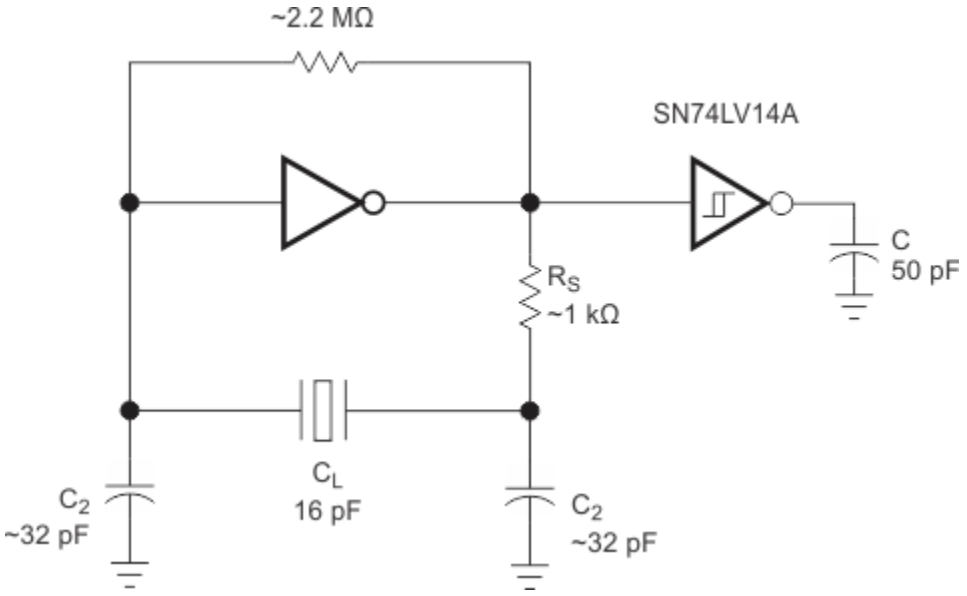


図 9-1. Oscillator Application Schematic

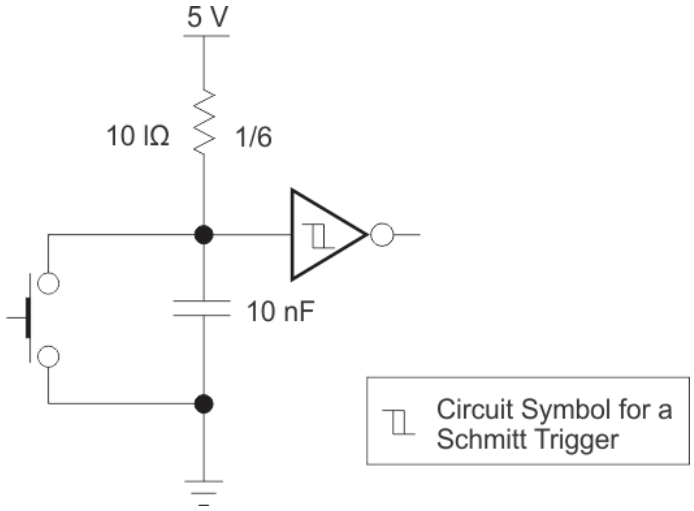


図 9-2. Switch De-bouncer Schematic

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9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specifcations, see Δt/ΔV in *セクション 6.3* table.
   - For specified high and low levels, see V_{IH} and V_{IL} in *セクション 6.3* table.
   - Inputs and outputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommend Output Conditions:
   - Load currents should not exceed 35 mA per output and 50 mA total for the part.

9.2.3 Application Curves

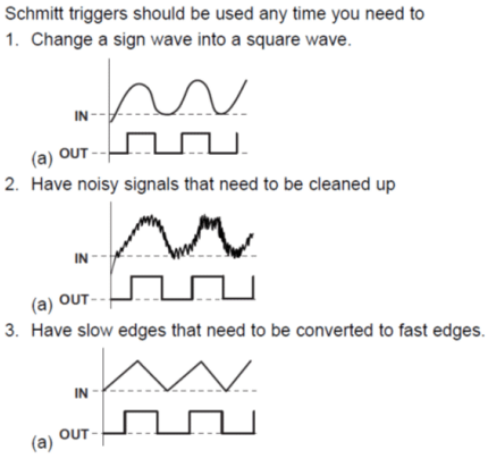


図 9-3. Schmitt Trigger Curves

10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *セクション 6.3* table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 µF capacitor is recommended. If there are multiple V_{CC} terminals then 0.01 µF or 0.022 µF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 µF and 1.0 µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in the 図 11-1 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver.

11.2 Layout Example

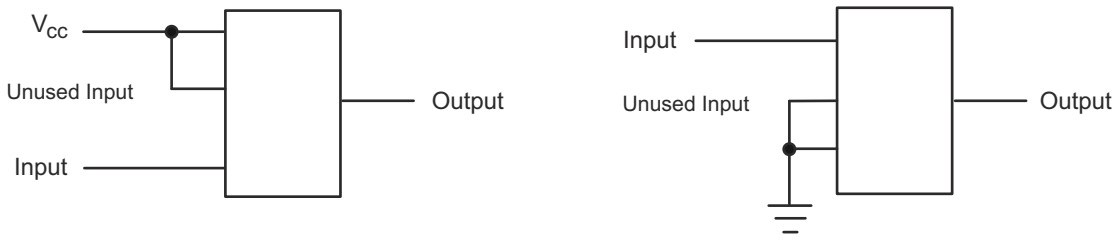


図 11-1. Layout Diagram

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12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LV14A	Click here	Click here	Click here	Click here	Click here
SN74LV14A	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV14AD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 125	LV14A
SN74LV14ADBR	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14ADBR.A	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14ADGVR	Active	Production	TVSOP (DGV) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14ADGVR.A	Active	Production	TVSOP (DGV) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14ADR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14ADR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14ADRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14ADRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14ANSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV14A
SN74LV14ANSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV14A
SN74LV14APW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 125	LV14A
SN74LV14APWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14APWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14APWRG3	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14APWRG3.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14APWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14APWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14ARGYR	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV14A
SN74LV14ARGYR.A	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV14A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV14A :

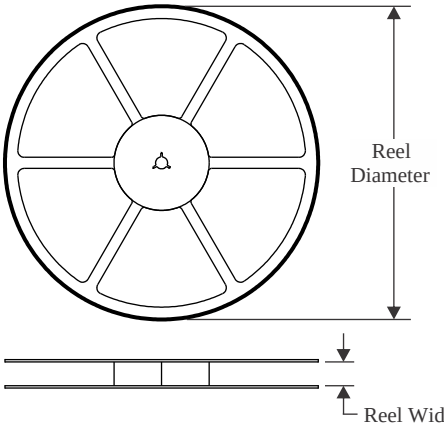
- Automotive : SN74LV14A-Q1
- Enhanced Product : SN74LV14A-EP

NOTE: Qualified Version Definitions:

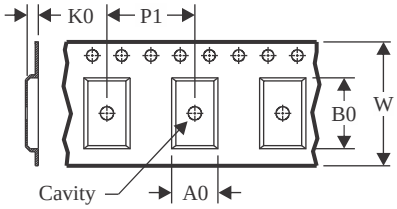
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

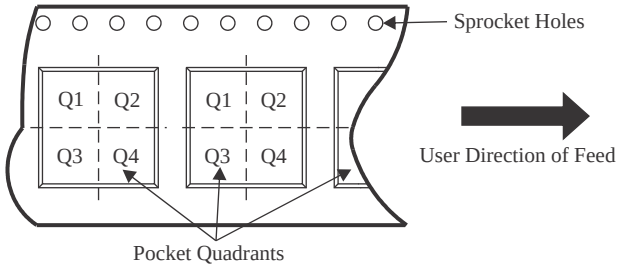


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

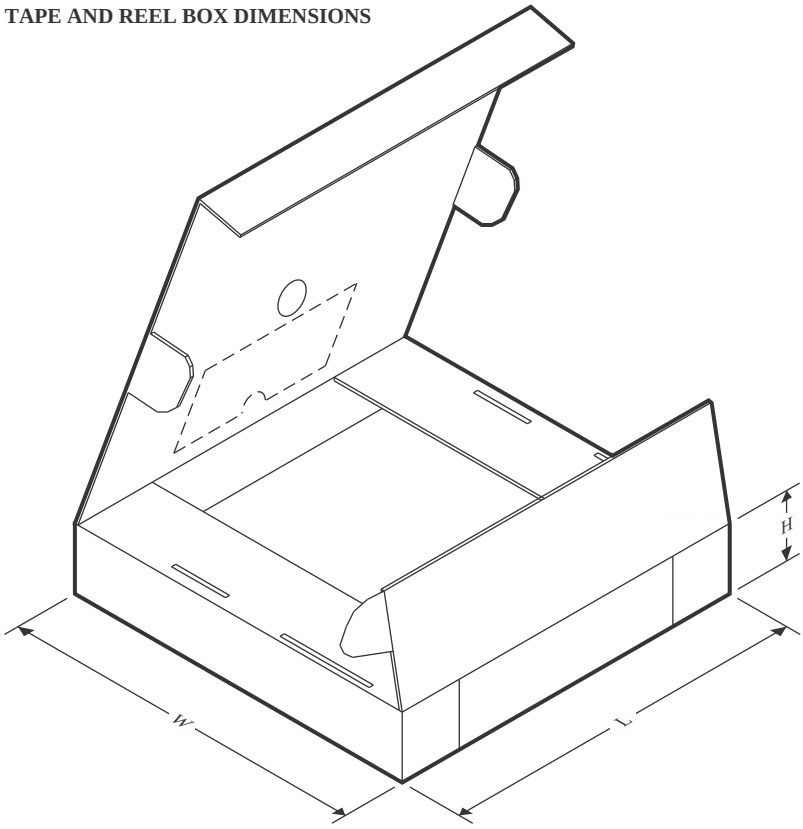
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

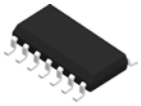
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV14ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV14ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV14ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV14ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV14ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV14ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV14ANSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74LV14APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV14APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.3	1.6	8.0	12.0	Q1
SN74LV14APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV14APWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV14APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV14APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.3	1.6	8.0	12.0	Q1
SN74LV14ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV14ADBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74LV14ADGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74LV14ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LV14ADR	SOIC	D	14	2500	340.5	336.1	32.0
SN74LV14ADRG4	SOIC	D	14	2500	353.0	353.0	32.0
SN74LV14ADRG4	SOIC	D	14	2500	340.5	336.1	32.0
SN74LV14ANSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74LV14APWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LV14APWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74LV14APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV14APWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LV14APWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LV14APWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74LV14ARGYR	VQFN	RGY	14	3000	360.0	360.0	36.0

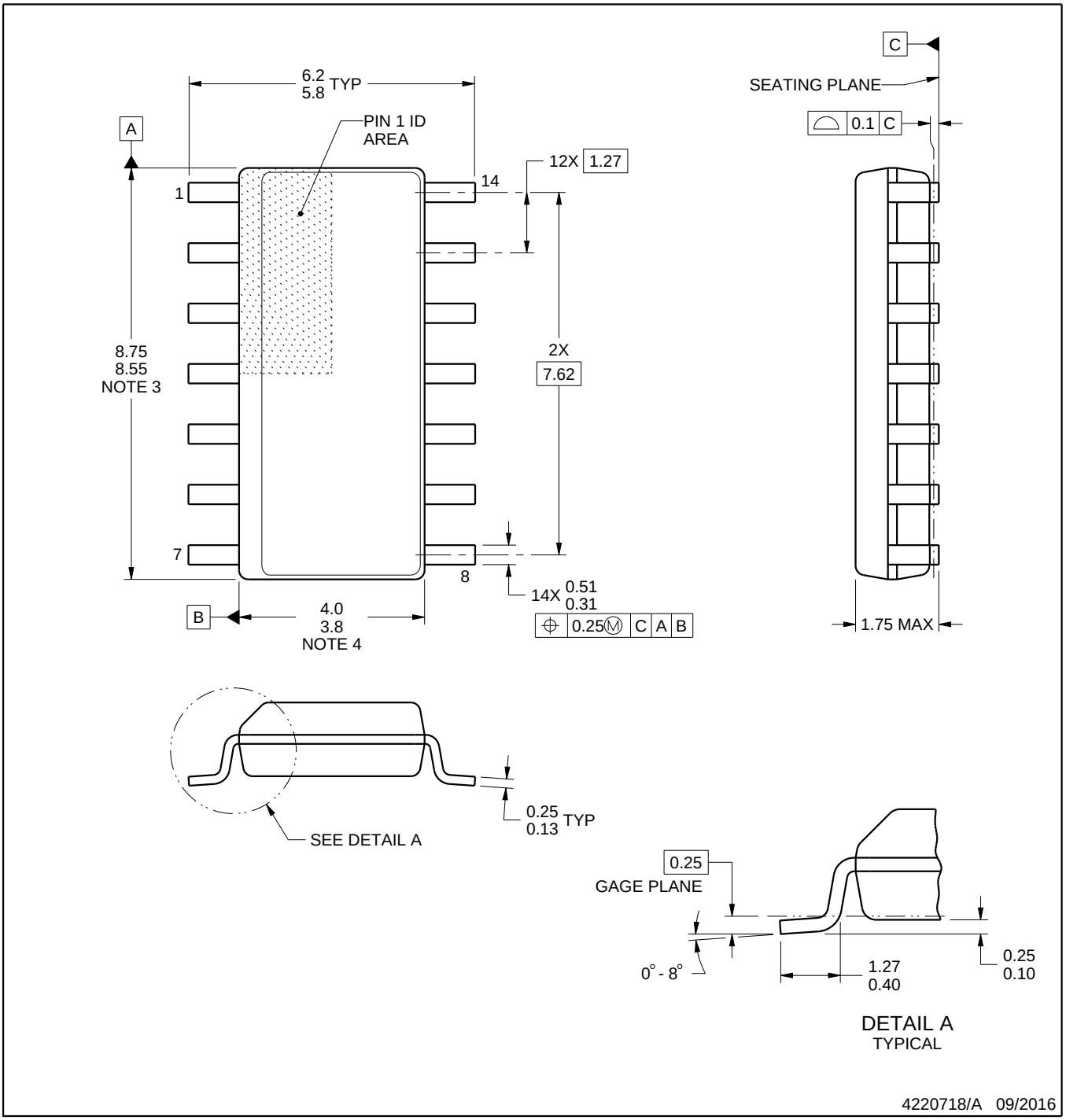


PACKAGE OUTLINE

D0014A

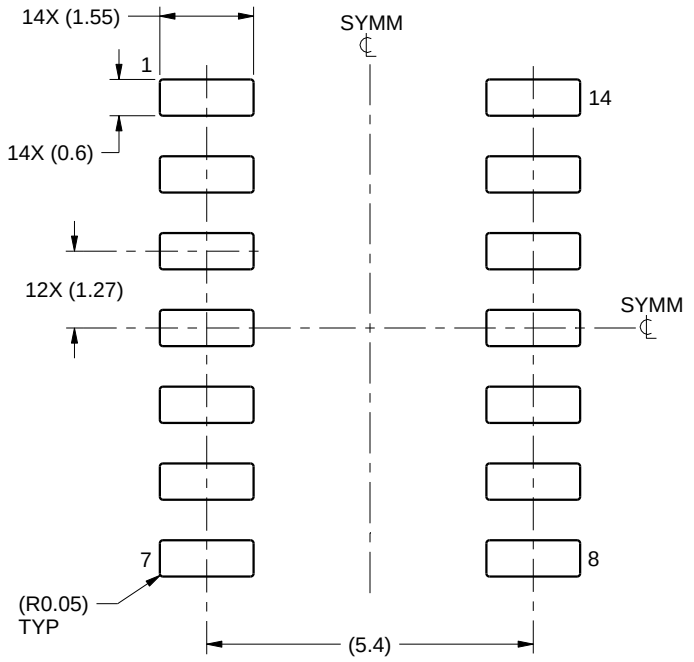
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

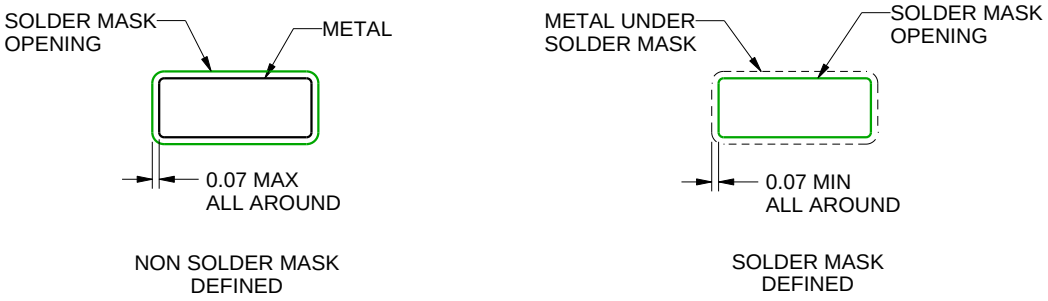


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

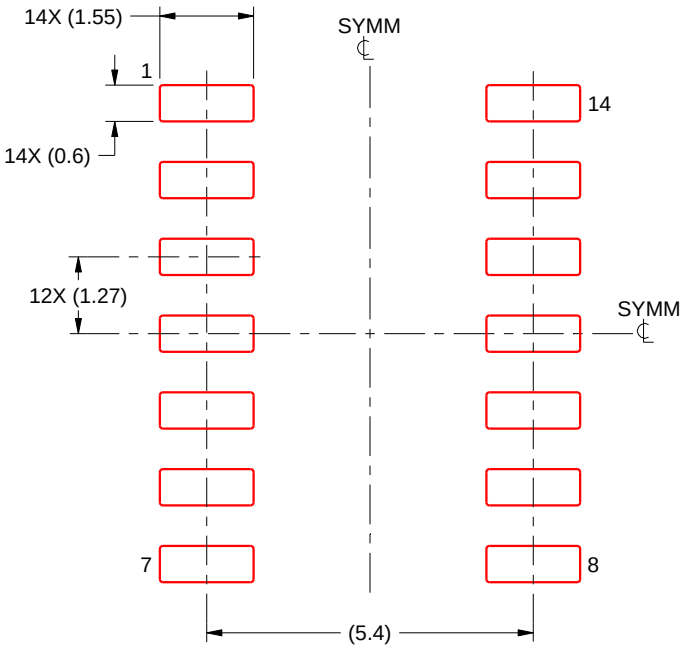
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

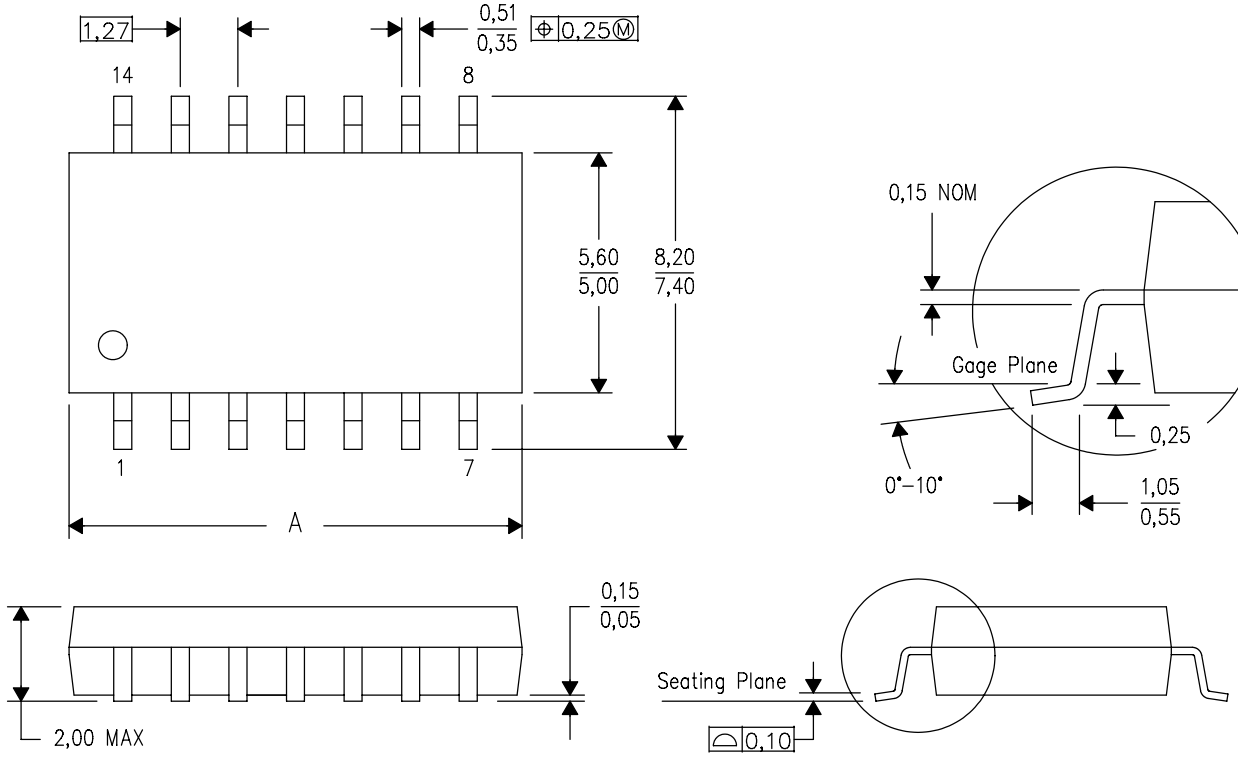
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



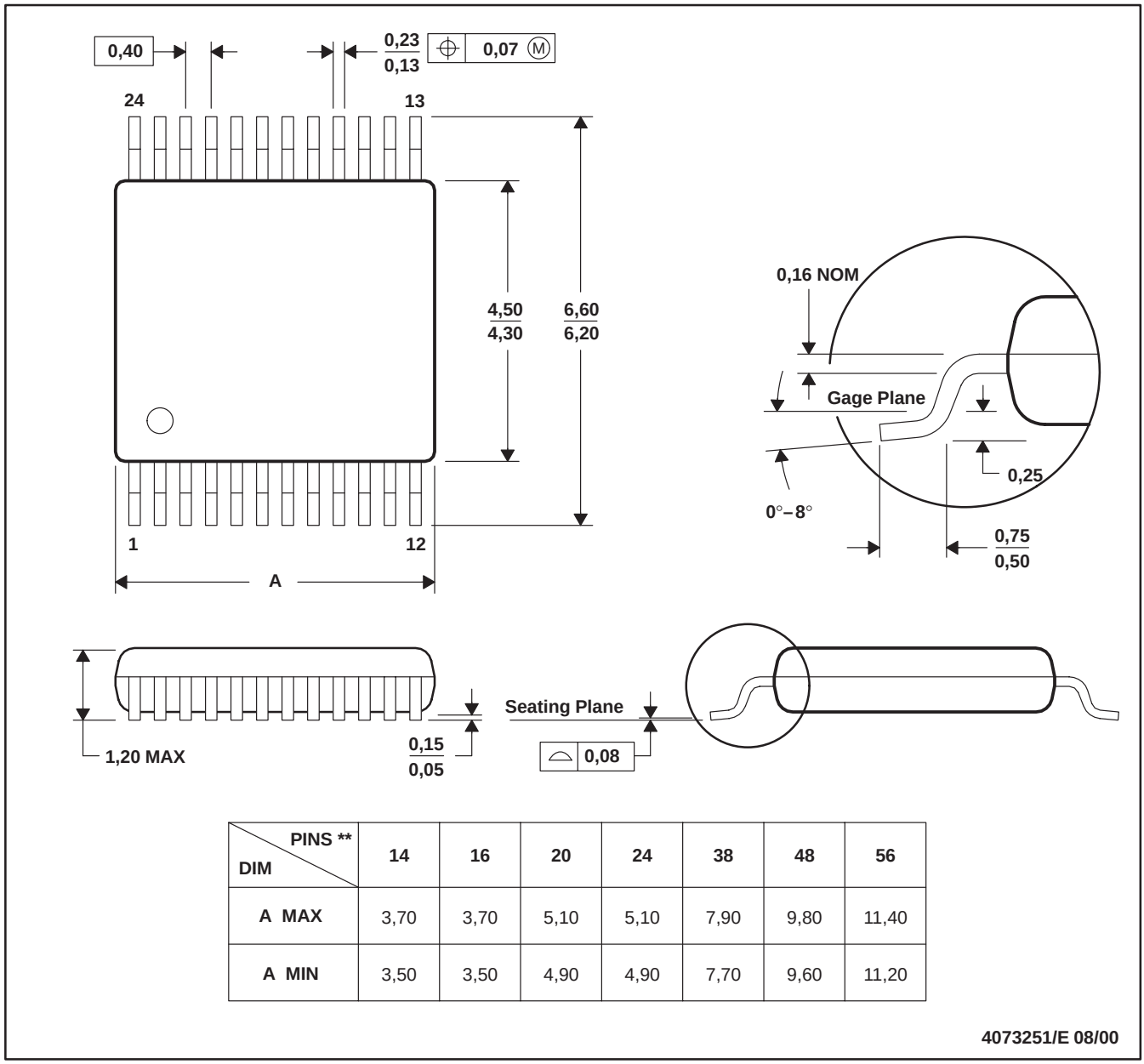
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

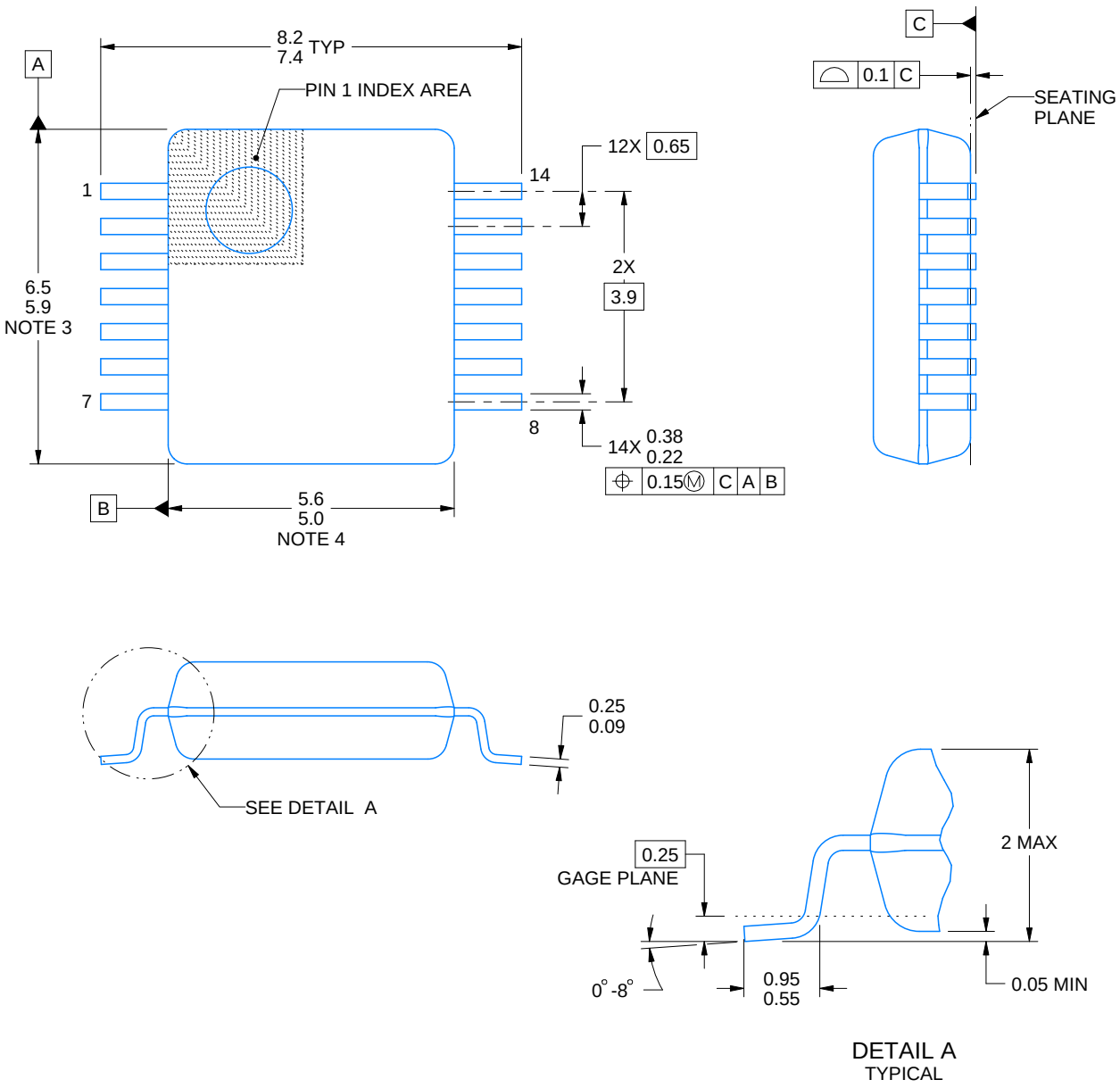
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

PACKAGE OUTLINE

DB0014A

SSOP - 2 mm max height

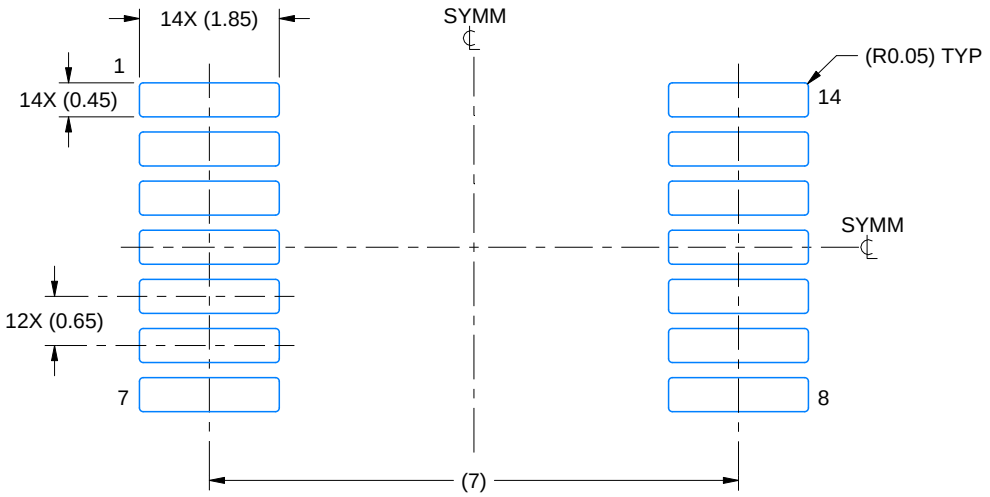
SMALL OUTLINE PACKAGE



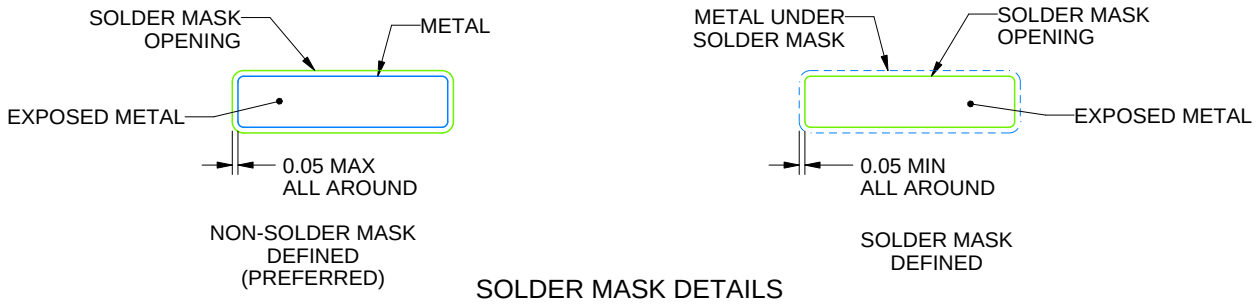
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

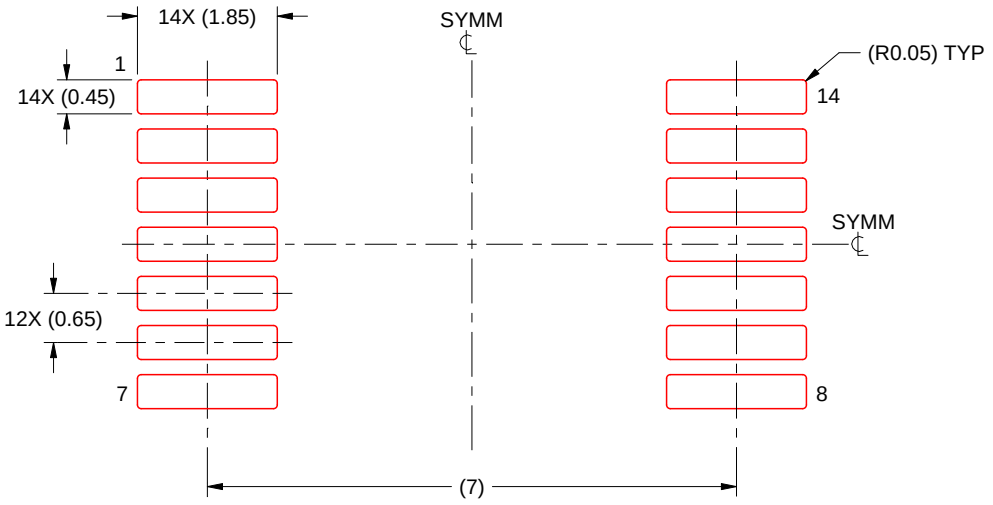


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

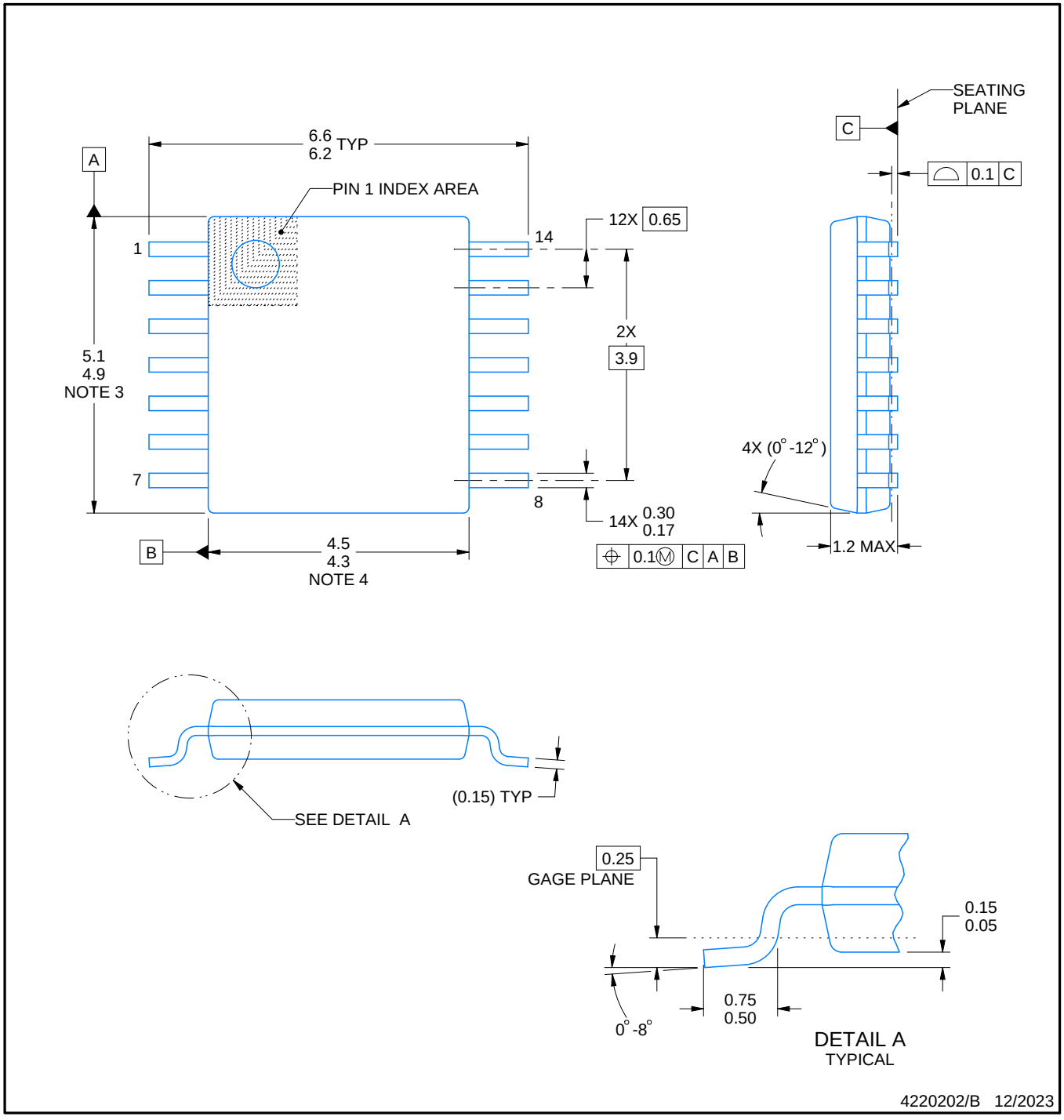
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

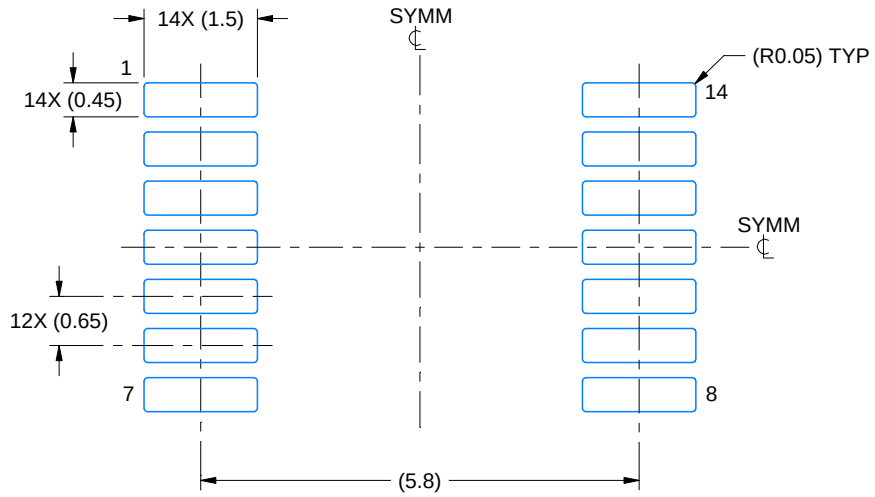
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

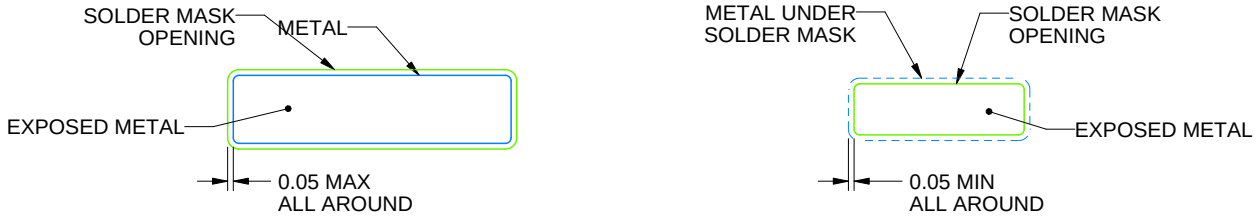


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

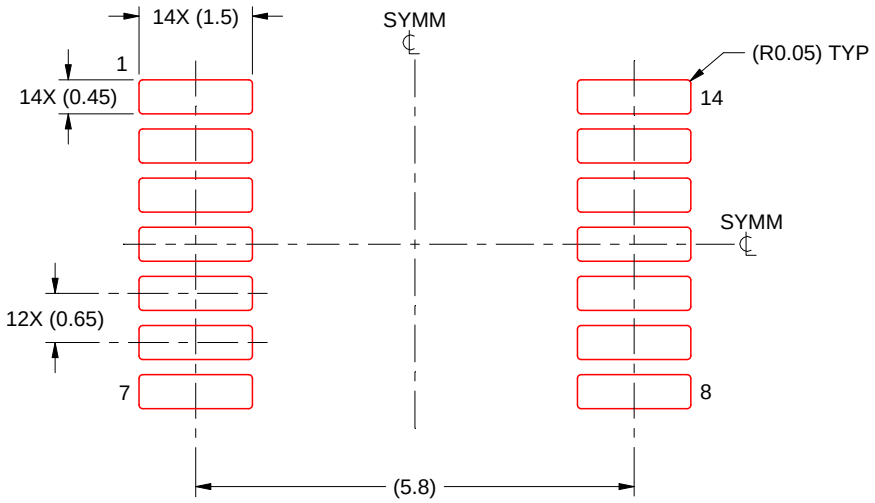


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

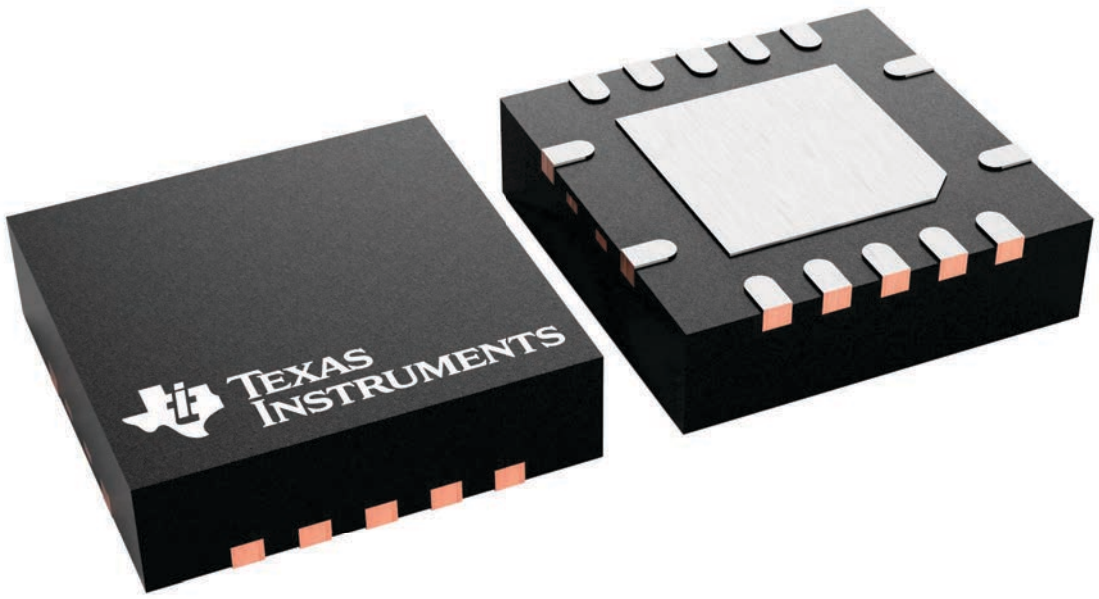
RGY 14

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231541/A

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