

SN74LV157A クワッド、2 ライン入力 1 ライン出力、データ・セクタ / マルチプレクサ

1 特長

- 2V~5.5V の V_{CC} で動作
- 5.5V までの入力電圧に対応
- 最大 t_{pd} 7.5ns (5V 時)
- 標準 V_{OLP} (出力グランド・バウンス) $< 0.8V$ ($V_{CC} = 3.3V$, $T_A = 25^\circ C$)
- 標準 V_{OHV} (出力 V_{OH} アンダーシュート) $> 2V$ (V_{CC} , $T_A = 25^\circ C$)
- JESD 78, Class II 準拠で 100mA 超のラッチアップ性能

2 アプリケーション

- サーバー
- LED ディスプレイ
- ネットワーク・スイッチ
- 通信インフラ
- モーター・ドライバ
- I/O エクスパンダ

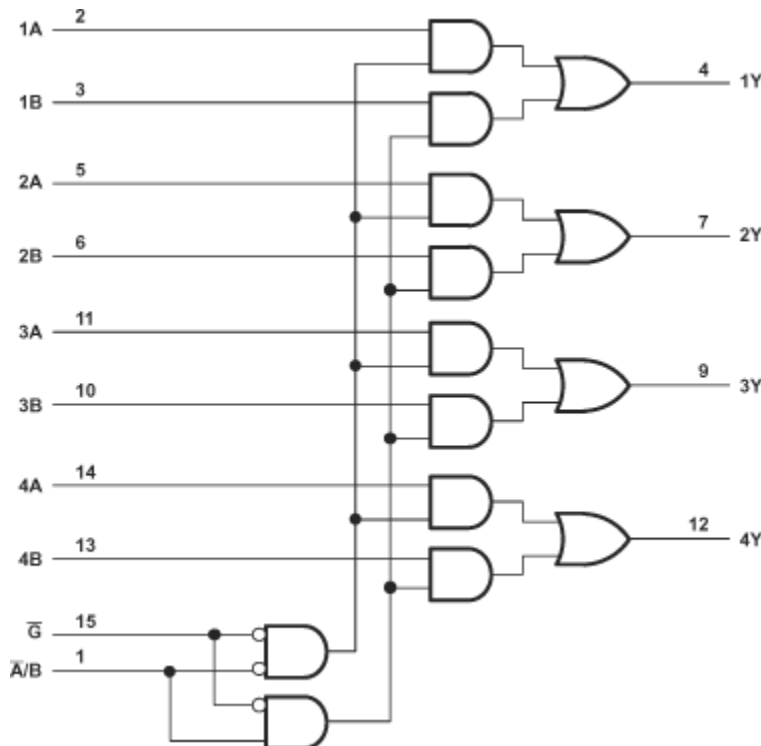
3 説明

LV157A デバイスは、2V~5.5V の V_{CC} で動作するように設計されたクワッド、2 ライン入力 1 ライン出力、データ・セクタ / マルチプレクサです。

パッケージ情報⁽¹⁾

部品番号	パッケージ	本体サイズ (公称)
SN74LV157A	DB (SSOP, 16)	6.2mm × 5.3mm
	DGV (TVSOP, 16)	3.6mm × 4.4mm
	DW (SOIC, 16)	10.3mm × 7.5mm
	NS (SOP, 16)	10.3mm × 5.3mm
	PW (TSSOP, 16)	5mm × 4.4mm

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



論理図 (正論理)



Table of Contents

1 特長	1	7 Parameter Measurement Information	8
2 アプリケーション	1	8 Detailed Description	9
3 説明	1	8.1 Overview.....	9
4 Revision History	2	8.2 Functional Block Diagram.....	9
5 Pin Configuration and Functions	3	8.3 Device Functional Modes.....	9
6 Specifications	4	9 Application and Implementation	10
6.1 Absolute Maximum Ratings.....	4	9.1 Power Supply Recommendations.....	10
6.2 ESD Ratings.....	4	9.2 Layout.....	10
6.3 Recommended Operating Conditions	5	10 Device and Documentation Support	11
6.4 Thermal Information.....	5	10.1 Documentation Support.....	11
6.5 Electrical Characteristics.....	5	10.2 ドキュメントの更新通知を受け取る方法.....	11
6.6 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	6	10.3 サポート・リソース.....	11
6.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	6	10.4 静電気放電に関する注意事項.....	11
6.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	6	10.5 用語集.....	11
6.9 Noise Characteristics.....	7	11 Mechanical, Packaging, and Orderable Information	12
6.10 Operating Characteristics.....	7		

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision F (April 1998) to Revision G (March 2023)	Page
「アプリケーション」、「パッケージ情報」表、「ピンの機能」表、「ESD 定格」表、「熱に関する情報」表、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、および「メカニカル、パッケージ、および注文情報」セクションを追加	1

5 Pin Configuration and Functions

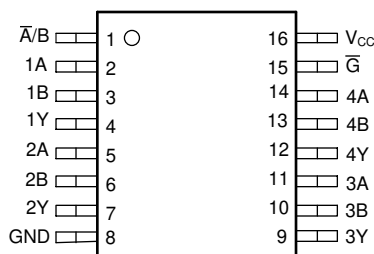


图 5-1. D, DB, DGV, NS, or PW Package (Top View)

表 5-1. Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	A/B	I	Address select
2	1A	I	Channel 1, data input A
3	1B	I	Channel 1, data input B
4	1Y	I	Channel 1, data output
5	2A	O	Channel 2, data input A
6	2B	O	Channel 2, data input B
7	2Y	I	Channel 2, data output
8	GND	—	Ground
9	3Y	I	Channel 3, data output
10	3B	I	Channel 3, data input B
11	3A	I	Channel 3, data input A
12	4Y	I	Channel 4, data output
13	4B	I	Channel 4, data input B
14	4A	I	Channel 4, data input A
15	G	I	Output strobe, active low
16	V _{CC}	—	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	7	V
V_I	Input voltage ¹	–0.5	7	V
V_O	Output voltage range applied in high or low state ¹ (2)	–0.5	$V_{CC} + 0.5$	V
V_O	Output voltage range applied in power-off state ¹	–0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$	–20	mA
I_{OK}	Output clamp current	$V_O < 0$	–50	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}	±25	mA
	Continuous current through V_{CC} or GND		±50	mA
T_{stg}	Storage temperature	–65	150	°C

(1) This value is limited to 5.5 V maximum.

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge		
	Human-Body Model (A114-A) ⁽¹⁾	±2000	V
	Machine Model (A115-A)	±200	
	Charged-Device Model (C101) ⁽²⁾	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		V
		V _{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		
		V _{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		
		V _{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5	V
		V _{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$	
		V _{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$	
		V _{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$	
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		– 50	μA
		V _{CC} = 2.3 V to 2.7 V		– 2	
		V _{CC} = 3 V to 3.6 V		6	
		V _{CC} = 4.5 V to 5.5 V		– 12	
I _{OL}	Low-level output current	V _{CC} = 2 V		50	μA
		V _{CC} = 2.3 V to 2.7 V		2	
		V _{CC} = 3 V to 3.6 V		6	
		V _{CC} = 4.5 V to 5.5 V		12	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	
T _A	Operating free-air temperature		–40	85	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LV157A					UNIT
		D	DB	DGV	NS	PW	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	73	82	120	64	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			
	I _{OH} = –6 mA	3 V	2.48			
	I _{OH} = –12 mA	4.5 V	3.8			

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OL}	$I_{OL} = 50 \mu A$	2 V to 5.5 V			0.1	V
	$I_{OL} = 2 \text{ mA}$	2.3 V			0.4	
	$I_{OL} = 6 \text{ mA}$	3 V			0.44	
	$I_{OL} = 12 \text{ mA}$	4.5 V			0.55	
I_I	$V_I = 5.5 \text{ V}$ or GND	0 to 5.5 V			± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			20	μA
I_{off}	V_I or $V_O = 0$ to 5.5 V	0			5	μA
C_i	$V_I = V_{CC}$ or GND	3.3 V		1.7		pF

6.6 Switching Characteristics, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TA = 25°C			SN74LV157A		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	$C_L = 15 \text{ pF}$		7.4 ¹	15.9 ¹	1	19.5	ns
	$\bar{A}/B$	Y			7.9 ¹	19.4 ¹	1	23.5	
	$\bar{C}$	Y			7.8 ¹	19.8 ¹	1	24	
t_{pd}	A or B	Y	$C_L = 50 \text{ pF}$		9.4	18.8	1	22	ns
	$\bar{A}$	Y			10.8	22.3	1	26	
	$\bar{C}$	Y			9.6	22.7	1	26.5	

- On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.7 Switching Characteristics, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TA = 25°C			SN74LV157A		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	$C_L = 15 \text{ pF}$		5.2 ¹	9.7 ¹	1	11.5	ns
	$\bar{A}/B$	Y			5.8 ¹	13.2 ¹	1	15.5	
	$\bar{C}$	Y			5.5 ¹	13.6 ¹	1	16	
t_{pd}	A or B	Y	$C_L = 50 \text{ pF}$		6.7	13.2	1	15	ns
	$\bar{A}$	Y			7.6	16.7	1	19	
	$\bar{C}$	Y			7	17.1	1	19.5	

- On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.8 Switching Characteristics, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TA = 25°C			SN74LV157A		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	$C_L = 15 \text{ pF}$		3.6 ¹	6.4 ¹	1	7.5	ns
	$\bar{A}/B$	Y			4.1 ¹	8.1 ¹	1	9.5	
	$\bar{C}$	Y			3.8 ¹	8.6 ¹	1	10	

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TA = 25°C			SN74LV157A		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	A or B	Y	C _L = 50 pF		4.8	8.4	1	9.5	ns
	$\bar{A}$	Y			5.4	10.1	1	11.5	
	$\bar{B}$	Y			5	10.6	1	12	

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.9 Noise Characteristics

$V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER		MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.3	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		– 0.1	–0.8	V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		3.2		V
V _{IH(D)}	High-level dynamic input voltage	2.31			V
V _{IL(D)}	Low-level dynamic input voltage			0.99	V

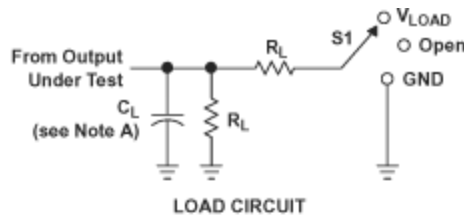
(1) Characteristics are for surface-mount packages only.

6.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

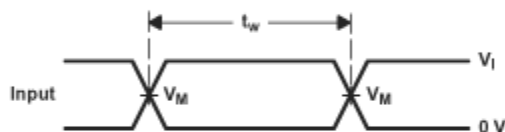
PARAMETER		TEST CONDITIONS		V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance	C _L = 50 pF	f = 10 MHz	3.3 V 5 V	12.1 13.1	pF

7 Parameter Measurement Information

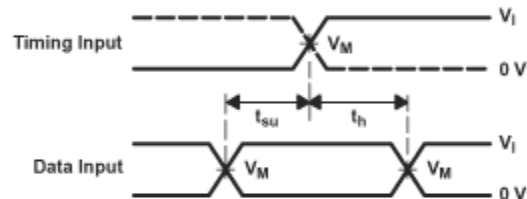


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

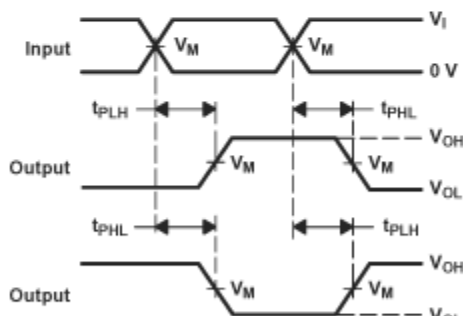
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
2.7 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V $\pm$ 0.3 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



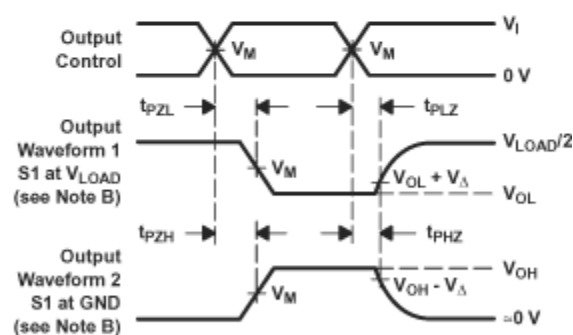
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, $Z_O = 50 \Omega$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dL} .
- F. t_{PZL} and t_{PZH} are the same as t_{dH} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

8 Detailed Description

8.1 Overview

The 'LV157A devices contain inverters and drivers to supply full data selection to the four output gates. A separate strobe ($\overline{G}$) input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The 'LV157A devices present true data.

8.2 Functional Block Diagram

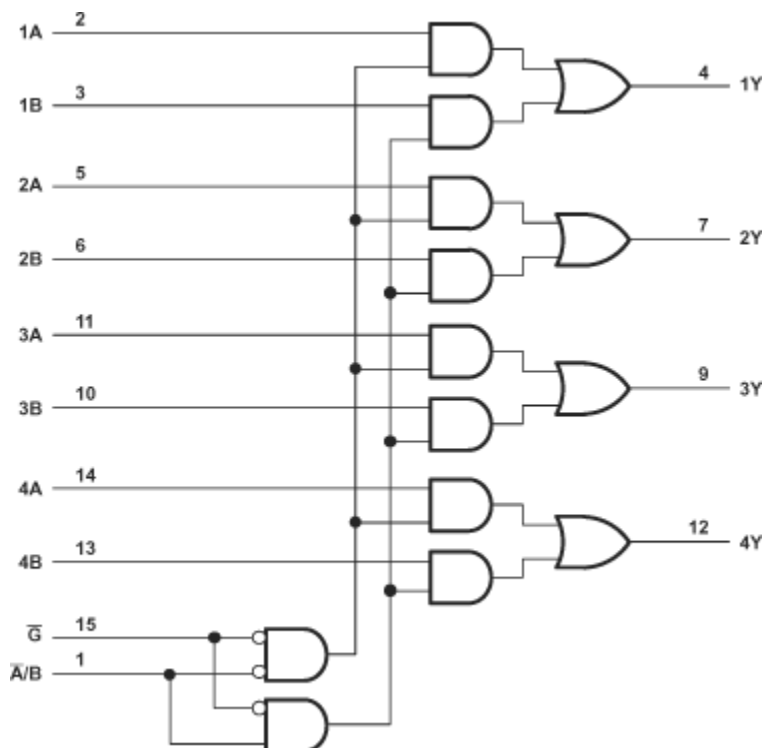


图 8-1. Logic Diagram (Positive Logic)

8.3 Device Functional Modes

表 8-1. Function Table

INPUTS ⁽¹⁾		DATA		OUTPUT Y
$\overline{G}$	SELECT A/B	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

(1) H = High Voltage Level, L = Low Voltage Level, X = Do not Care, Z = High Impedance

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in [セクション 6.3](#).

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μF capacitor is recommended. If there are multiple V_{CC} terminals then 0.01 μF or 0.022 μF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 μF and 1.0 μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

9.2 Layout

9.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

9.2.1.1 Layout Example

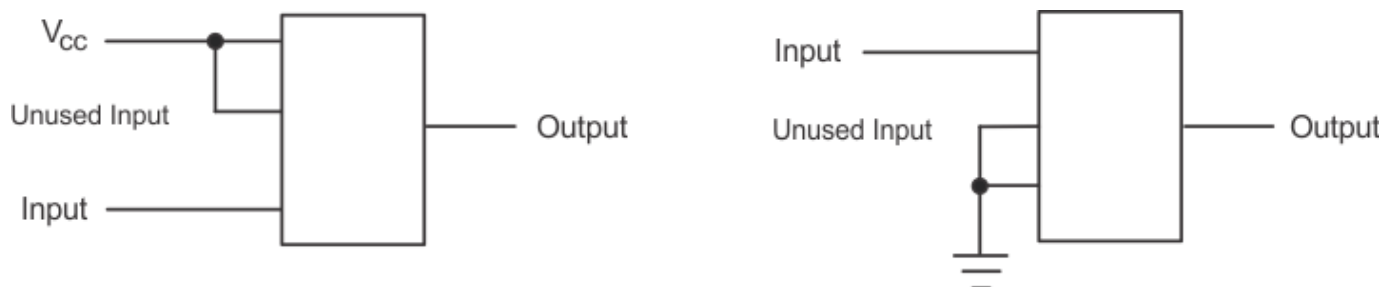


図 9-1. Layout Diagram

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV157A	Click here	Click here	Click here	Click here	Click here

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.5 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV157AD	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 85	LV157A
SN74LV157ADBR	Last Time Buy	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV157A
SN74LV157ADBR.A	Last Time Buy	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV157A
SN74LV157ADGVR	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV157A
SN74LV157ADGVR.A	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV157A
SN74LV157ADR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV157A
SN74LV157ADR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV157A
SN74LV157ANSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV157A
SN74LV157ANSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV157A
SN74LV157APW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	LV157A
SN74LV157APWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	LV157A
SN74LV157APWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV157A
SN74LV157APWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV157A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

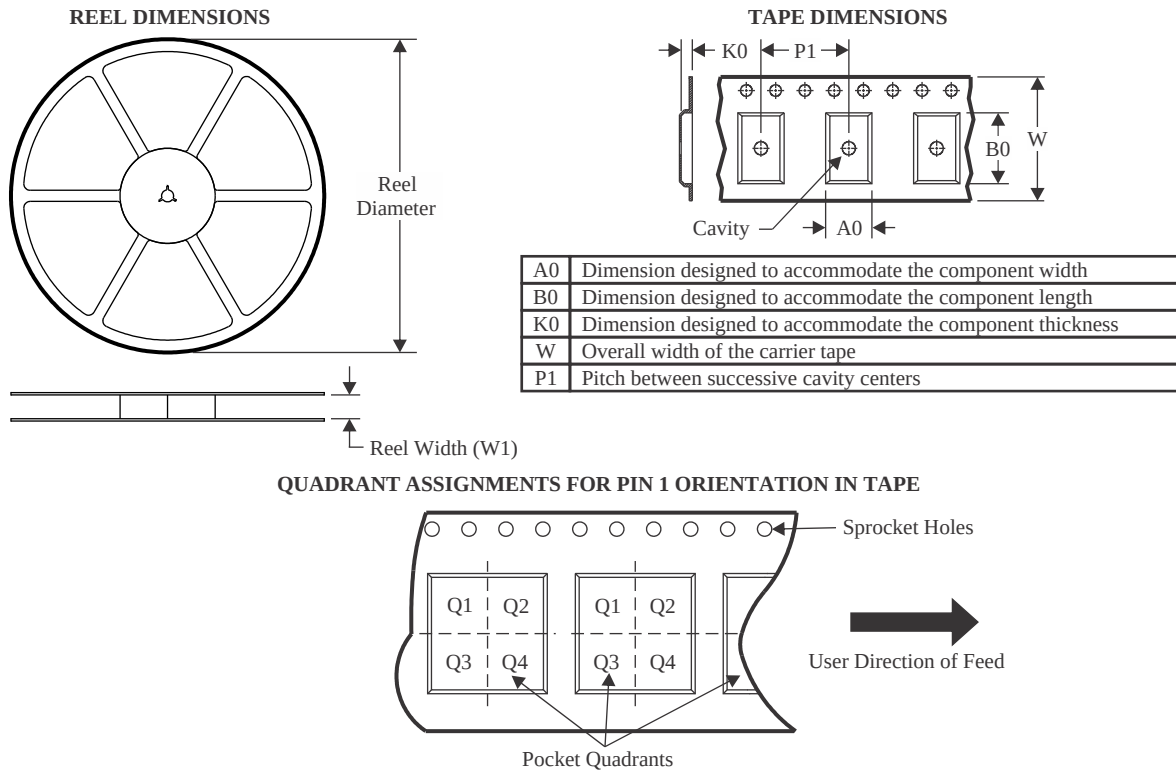
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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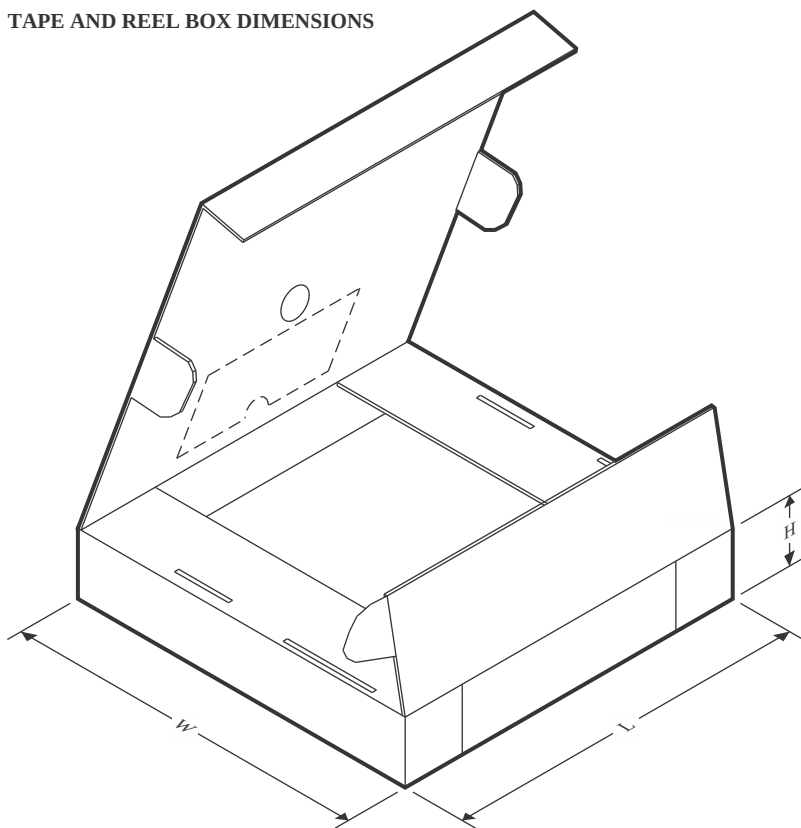
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

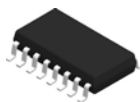
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV157ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV157ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV157ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV157ADR	SOIC	D	16	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74LV157ANSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LV157APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV157APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV157ADBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74LV157ADGVR	TVSOP	DGV	16	2000	353.0	353.0	32.0
SN74LV157ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LV157ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LV157ANSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74LV157APWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74LV157APWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0

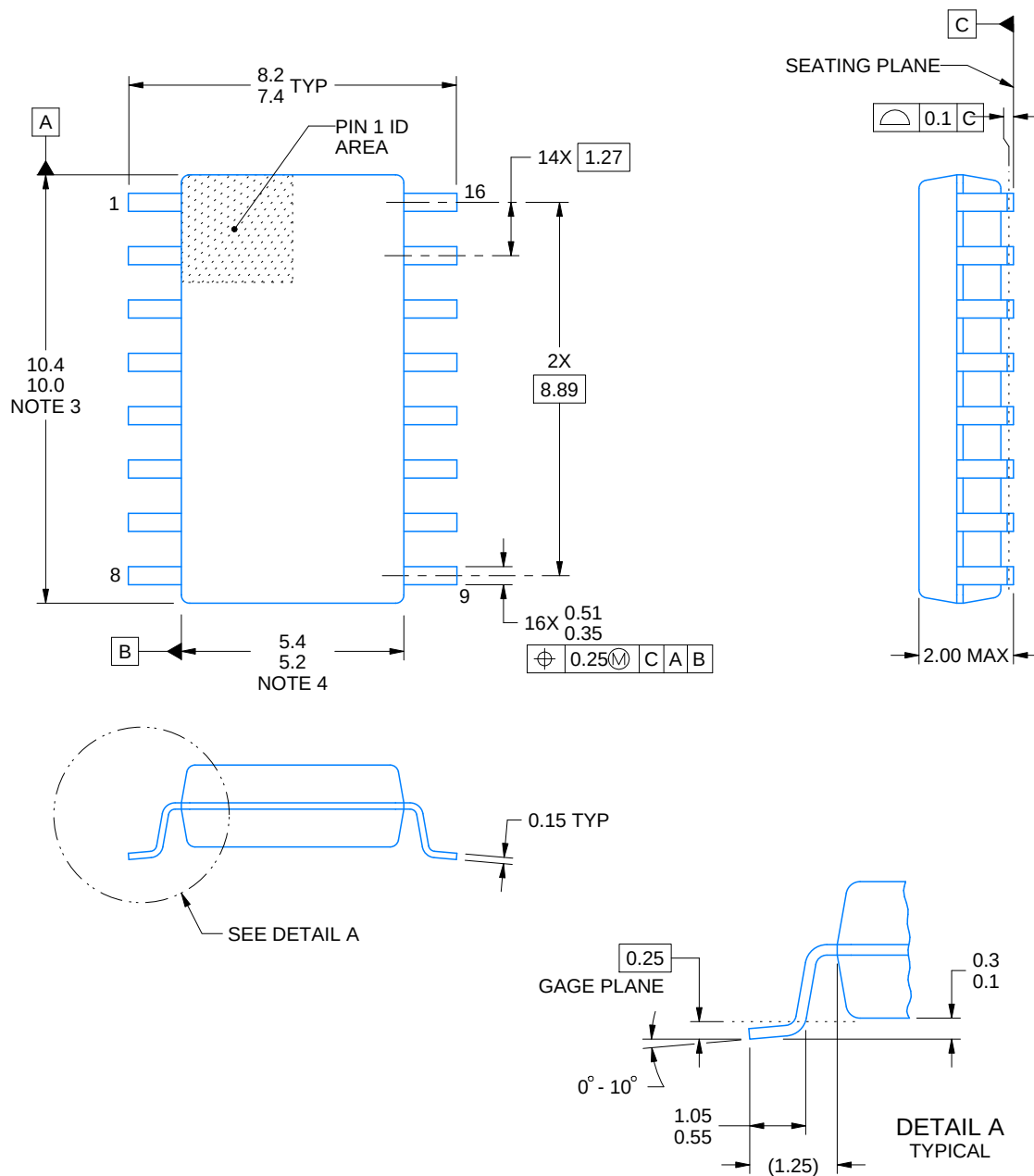


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

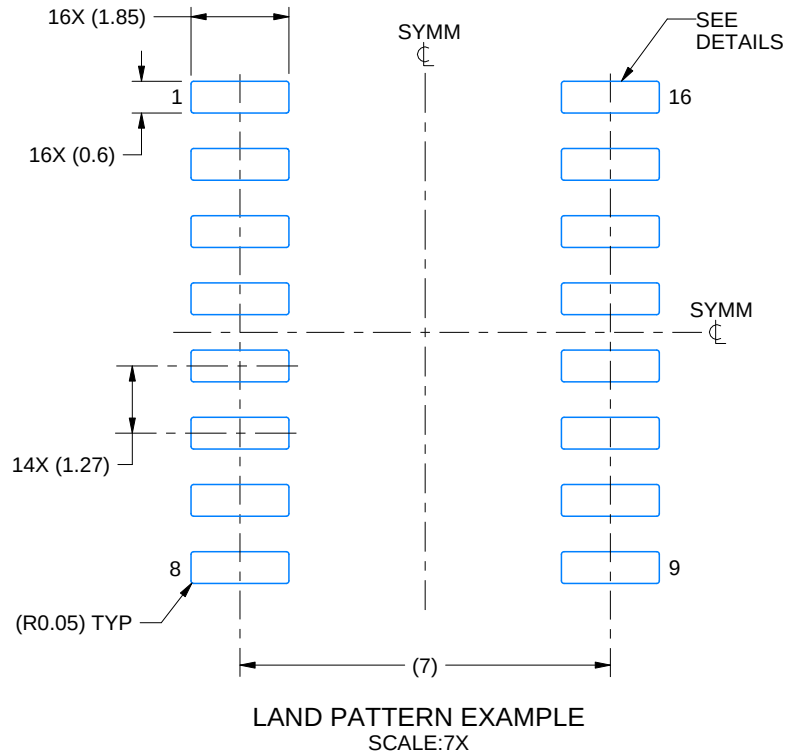
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP

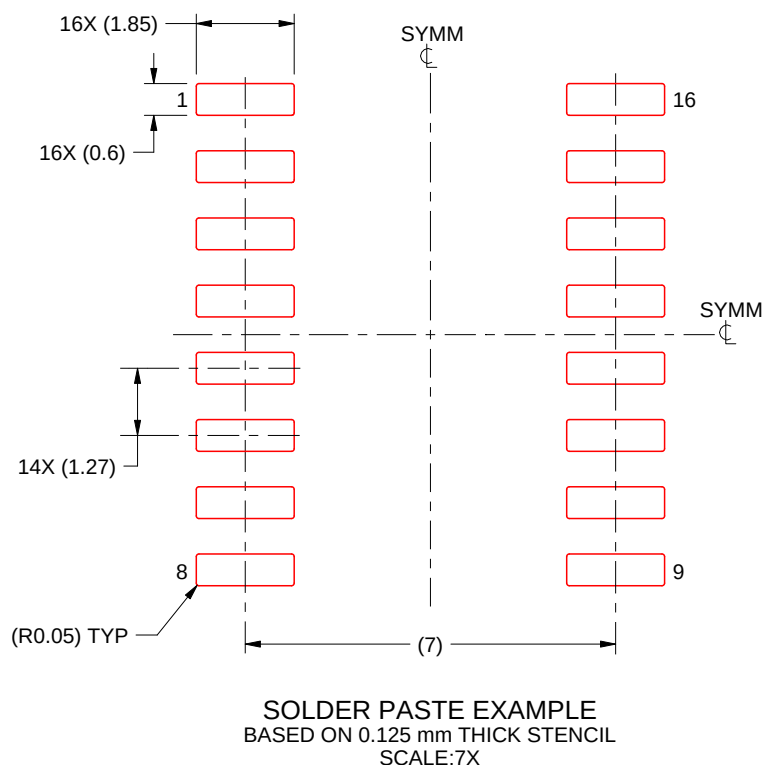


4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



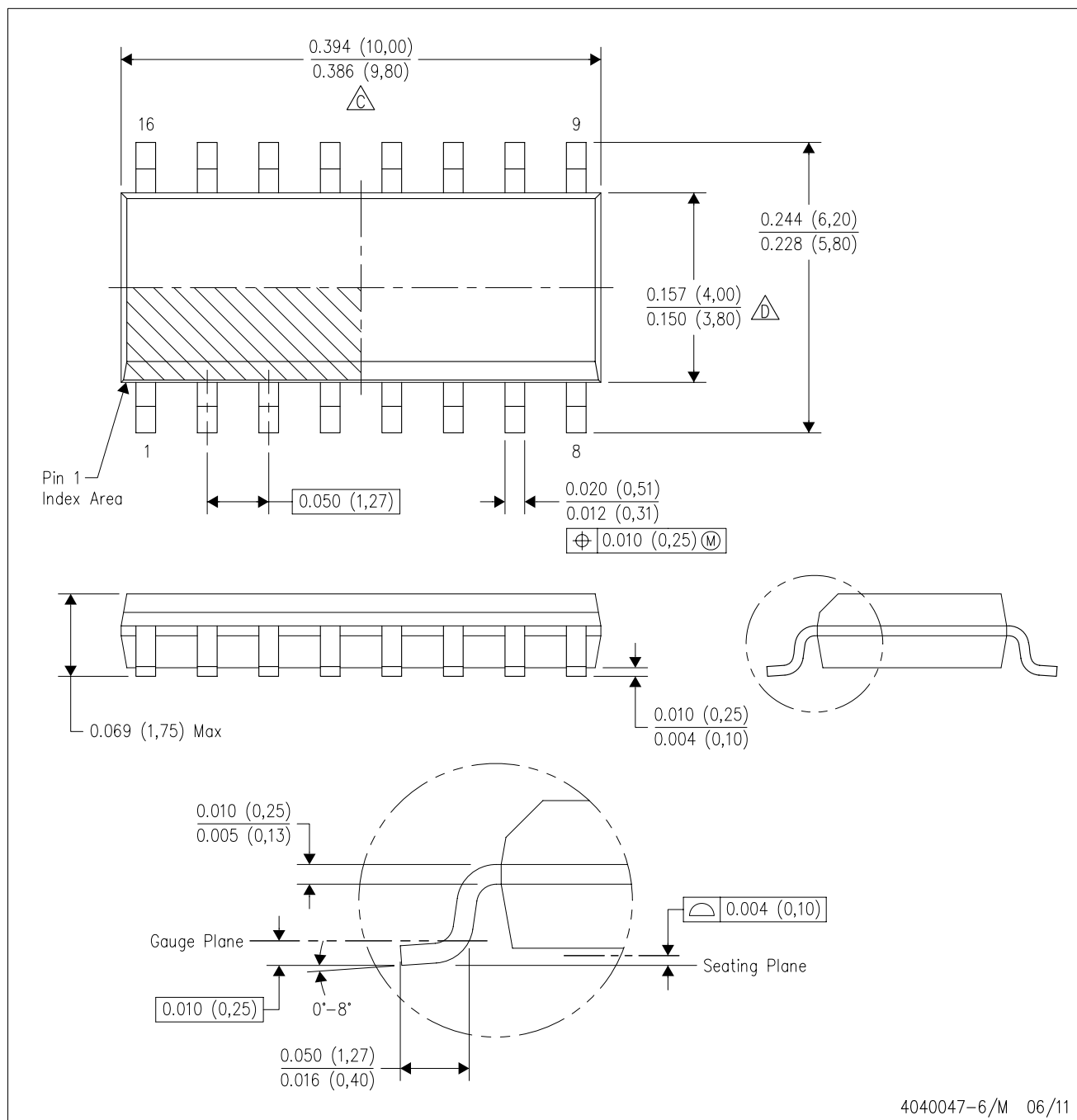
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

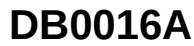
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



SSOP - 2 mm max height

[illegible]

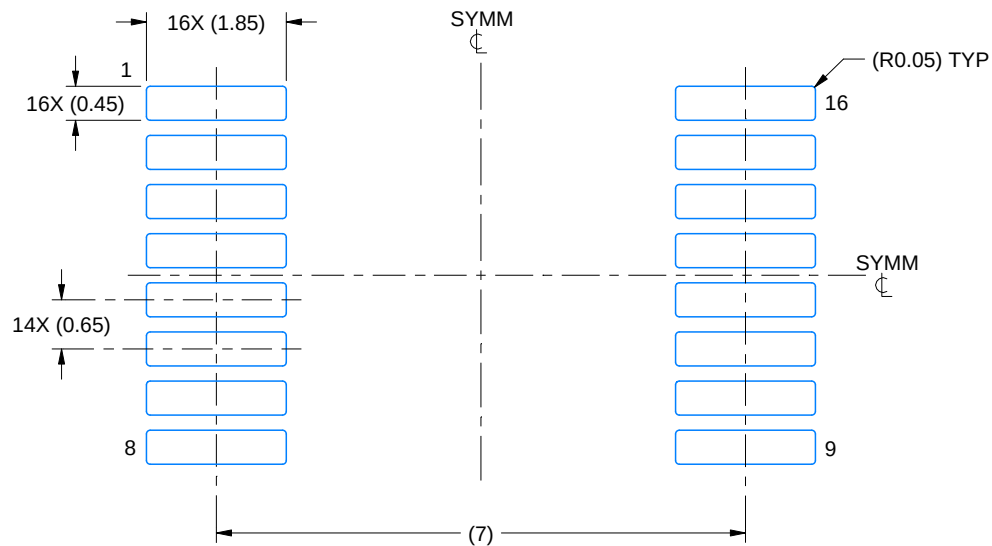
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

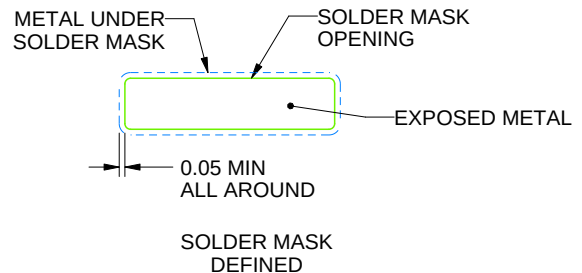
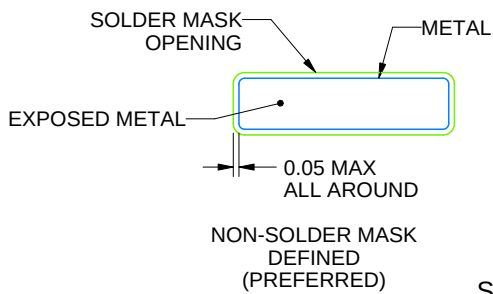
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

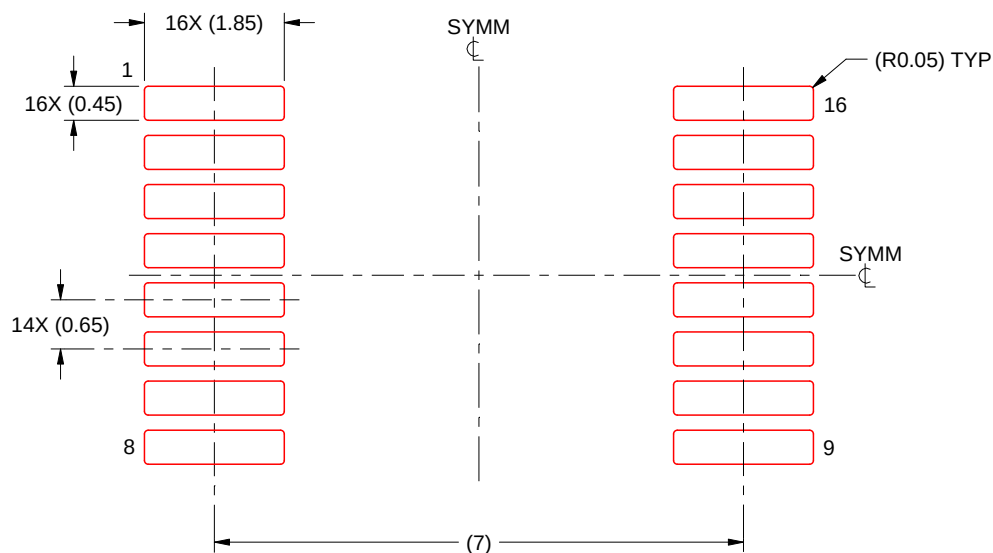
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

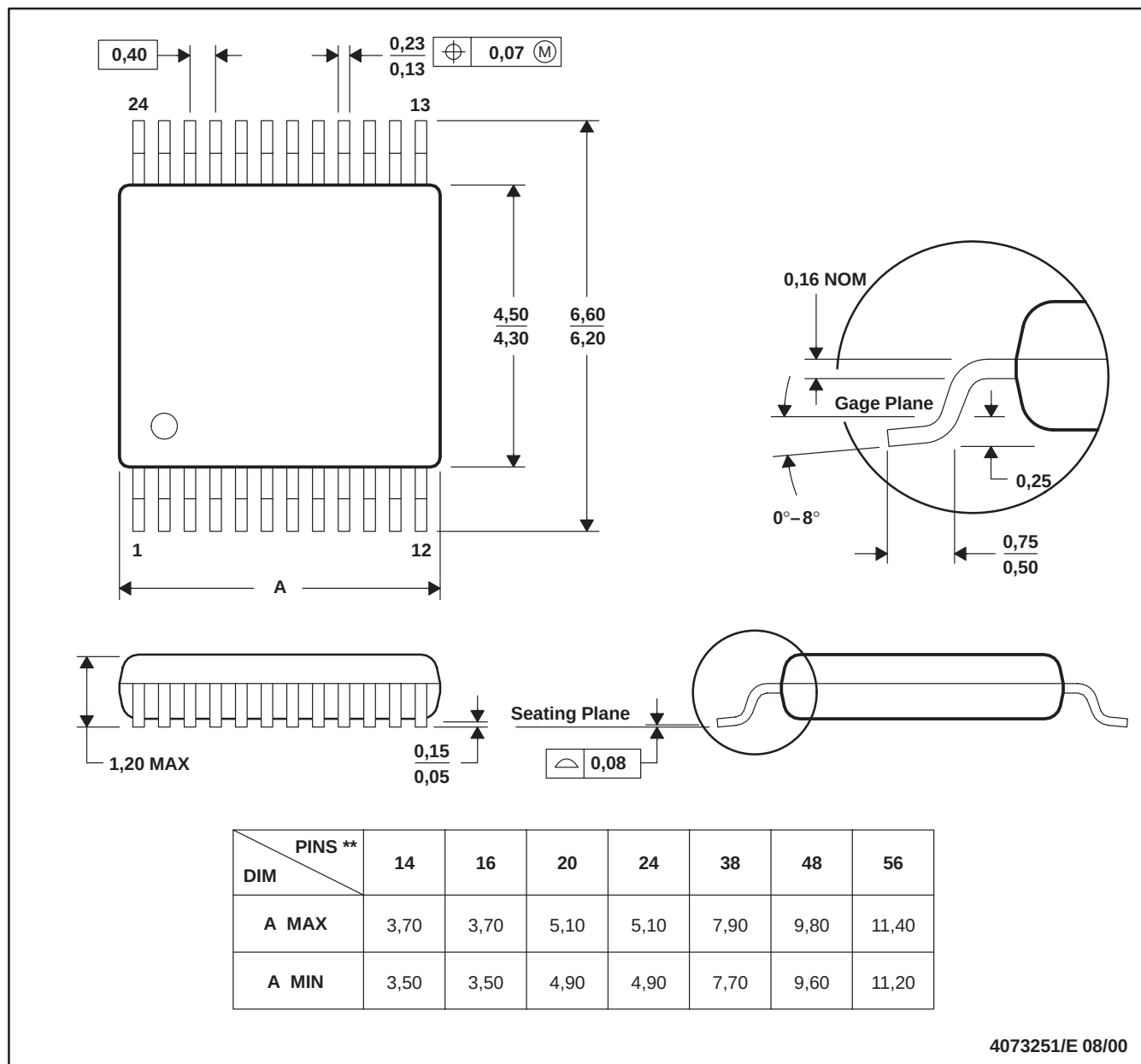
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

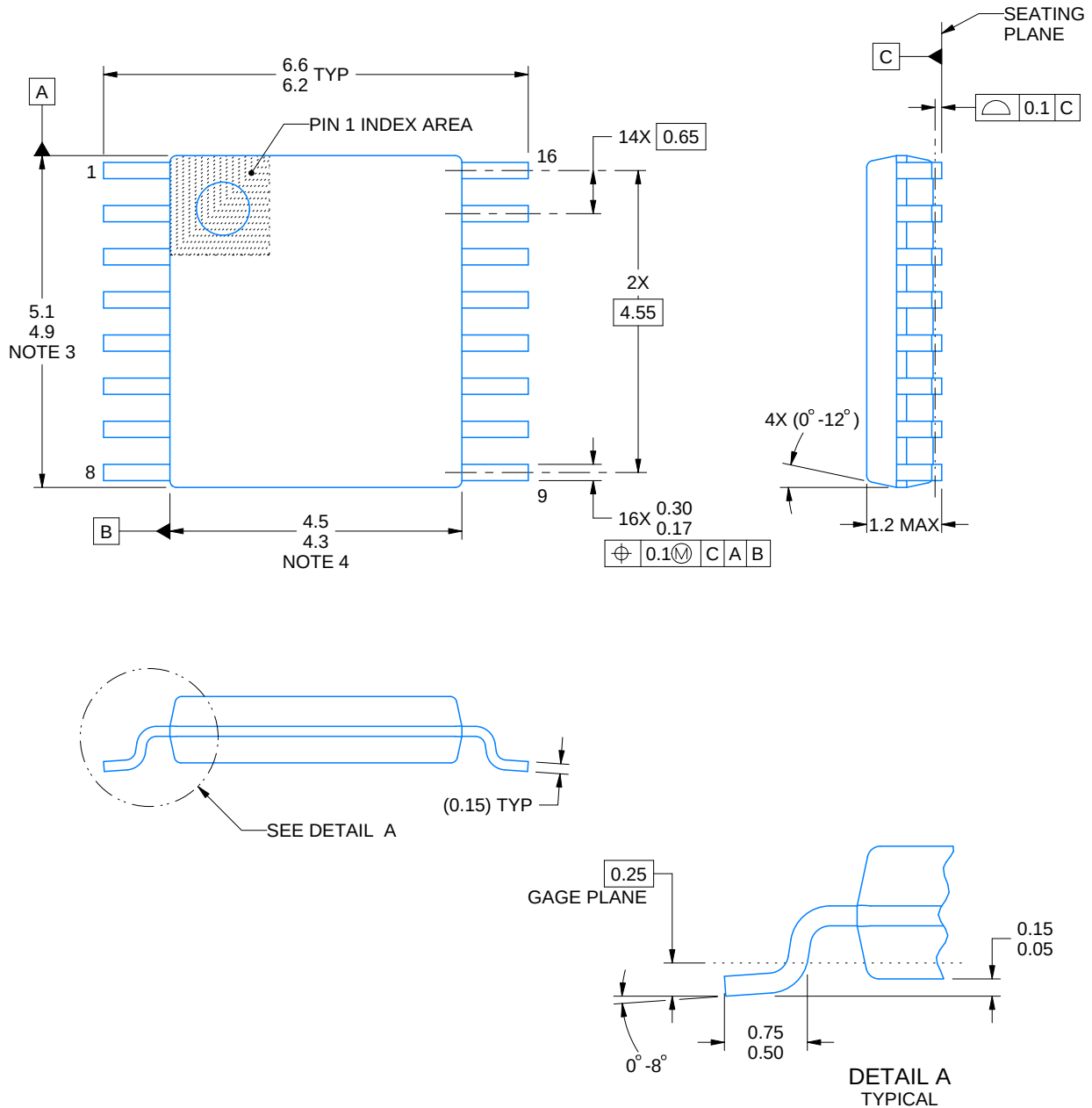
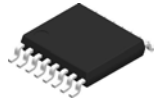
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



4220204/B 12/2023

NOTES:

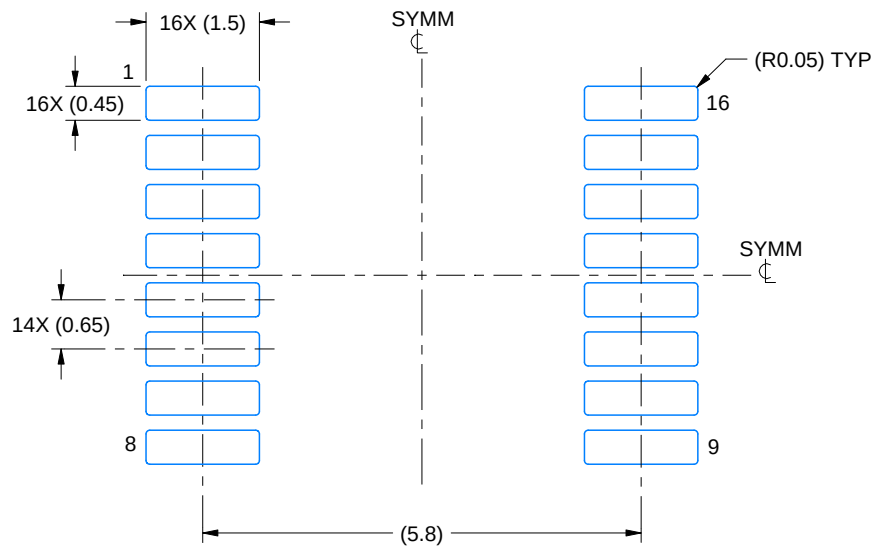
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

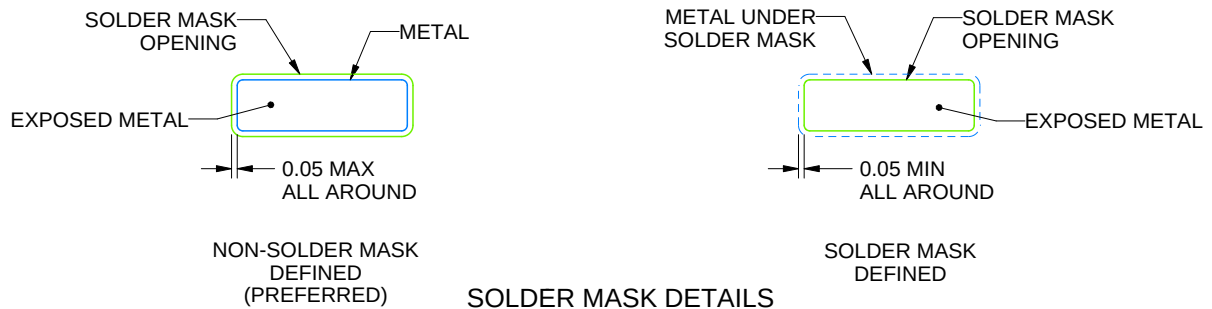
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

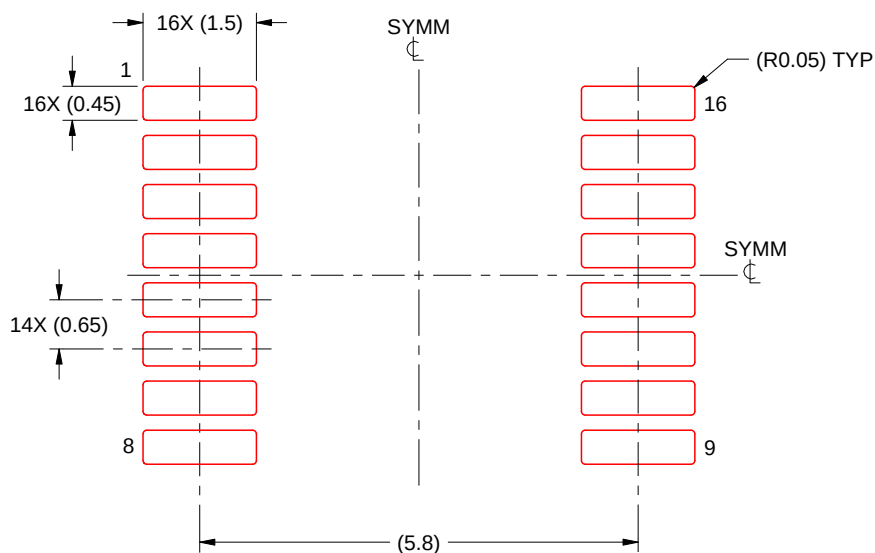
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月