SN74LV21A デュアル 4 入力正論理 AND ゲート

1 特長

- 2V～5.5V の V_{CC} で動作
- 最大 t_{pd}:6ns (5V 時)
- 標準 V_{OLP} (出力グランド・バウンス) < 0.8V (V_{CC} = 3.3V、T_A = 25℃)
- 標準 V_{OHV} (出力 V_{OH} アンダーシュート) > 2.3V (V_{CC} = 3.3V、TA = 25℃)
- I_{off} により部分的パワーダウン・モード動作をサポート
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能

2 概要

これらのデュアル 4 入力正論理 AND ゲートは、2V～5.5V V_{CC} 動作用に設計されています。

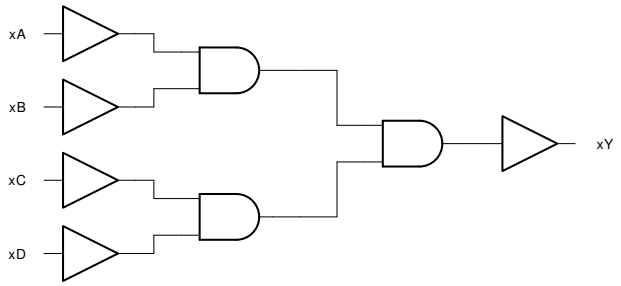
SN74LV21A デバイスはブール関数 Y = A • B • C • D を正論理で実行します。

これらのデバイスは、I_{off} を使用する部分的パワーダウン・アプリケーション用の動作が完全に規定されています。I_{off} 回路が出力をディセーブルにするので、電源切断時にデバイスに電流が逆流して損傷に至ることを回避できます。

パッケージ情報

部品番号	パッケージ [1]	パッケージ・サイズ [2]
SN74LV21A	DGV (TVSOP、14)	3.60mm × 6.4mm
	D (SOIC、14)	8.65mm × 6mm
	NS (SO、14)	10.20mm × 7.8mm
	DB (SSOP、14)	6.20mm × 7.8mm
	PW (TSSOP、14)	5.00mm × 6.4mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



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Table of Contents

1 特長 ... 1
2 概要 ... 1
3 Revision History ... 2
4 Pin Configuration and Functions ... 3
5 Specifications ... 4
5.1 Absolute Maximum Ratings ... 4
5.2 ESD Ratings ... 4
5.3 Recommended Operating Conditions ... 4
5.4 Thermal Information ... 5
5.5 Electrical Characteristics ... 5
5.6 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V ... 5
5.7 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V ... 6
5.8 Switching Characteristics, V_{CC} = 5 V ± 0.5 V ... 6
5.9 Noise Characteristics ... 6
5.10 Operating Characteristics ... 6
6 Parameter Measurement Information ... 7
7 Detailed Description ... 8
7.1 Overview ... 8
7.2 Functional Block Diagram ... 8
7.3 Device Functional Modes ... 8
8 Device and Documentation Support ... 9
8.1 Documentation Support (Analog) ... 9
8.2 ドキュメントの更新通知を受け取る方法 ... 9
8.3 サポート・リソース ... 9
8.4 Trademarks ... 9
8.5 静電気放電に関する注意事項 ... 9
8.6 用語集 ... 9
9 Mechanical, Packaging, and Orderable Information ... 9

3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (April 2005) to Revision F (July 2023)	Page
• 最新のデータシート規格を反映するように、文書全体にわたって採番方式、書式、表、図、相互参照を更新	1

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4 Pin Configuration and Functions

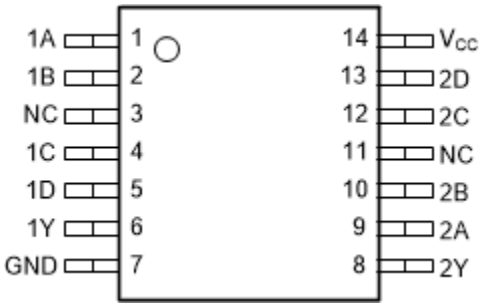


図 4-1. SN74LV21A D, DB, DGV, NS, or PW Package (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1A	1	I	1A Input
1B	2	I	1B Input
NC	3	—	Not internally connected
1C	4	I	1C Input
1D	5	I	1D Input
1Y	6	O	1Y Output
2Y	8	O	2Y Output
2A	9	I	2A Input
2B	10	I	2B Input
NC	11	—	Not internally connected
2C	12	I	2C Input
2D	13	I	2D Input
GND	7	—	Ground Pin
V_{CC}	14	—	Power Pin

(1) Signal Types: I = Input, O = Output.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Output voltage range applied in high or low state(2) (3)		–0.5	V_{CC} + 0.5	V
V_O	Output voltage range applied in power-off state(2)		–0.5	7	V
I_{IK}	Input clamp current	(V_I < 0)		–20	mA
I_{OK}	Output clamp current	(V_O < 0)		–50	mA
I_O	Continuous output current	(V_O = 0 to V_{CC})		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	± 2000	V
		Charged device model (CDM), per JESD22-C101(2)	± 1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High level output current	V_{CC} = 2 V		–50	μA
		V_{CC} = 2.3 V to 2.7 V		–2	mA
		V_{CC} = 3 V to 3.6 V		–6	
		V_{CC} = 4.5 V to 5.5 V		–12	

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5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
I_{OL}	Low level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		6	
		V_{CC} = 4.5 V to 5.5 V		12	
Δt/Δv	Input transition rise and fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs,* literature number SCBA004

5.4 Thermal Information

THERMAL METRIC[1]		SN74LV21A					UNIT
		D	DB	DGV	NS	PW	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86	96	127	76	113	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –50 µA	2 V to 5.5 V	V_{CC} - 0.1			V
		I_{OH} = –2 mA	2.3 V	2			
		I_{OH} = –6 mA	3 V	2.48			
		I_{OH} = –12 mA	4.5 V	3.8			
V_{OL}	Low-level output voltage	I_{OL} = 50 µA	2 V to 5.5 V			0.1	V
		I_{OL} = 2 mA	2.3 V			0.4	
		I_{OL} = 6 mA	3 V			0.44	
		I_{OL} = 12 mA	4.5 V			0.55	
I_I	Input leakage current	V_I = 5.5 V or GND	0 to 5.5 V			±1	µA
I_{CC}	Supply current	V_I = V_{CC} or GND, I_O = 0	5.5 V			20	µA
I_{off}	Off-state leakage current	V_I or V_O = 0 to 5.5 V	0 V			5	µA
C_i	Input capacitance	V_I = V_{CC} or GND	3.3 V		1.9		pF

5.6 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74LV21A		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, C or D	Y	C_L = 15 pF		7	12	1	14	ns
t_{pd}	A, B, C or D	Y	C_L = 50 pF		9.2	15.7	1	19	

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5.7 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74LV21A		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, C, or D	Y	C_L = 15 pF		5.1	7	1	8.5	ns
t_{pd}	A, B, C, or D	Y	C_L = 50 pF		6.6	10.5	1	12	

5.8 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74LV21A		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, C, or D	Y	C_L = 15 pF		3.8	5	1	6	ns
t_{pd}	A, B, C, or D	Y	C_L = 50 pF		4.9	7	1	8	

5.9 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

PARAMETER[1]		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.2	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		0	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.2		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

5.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 10 MHz	3.3 V	17.4	pF
				5 V	20.2	

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6 Parameter Measurement Information

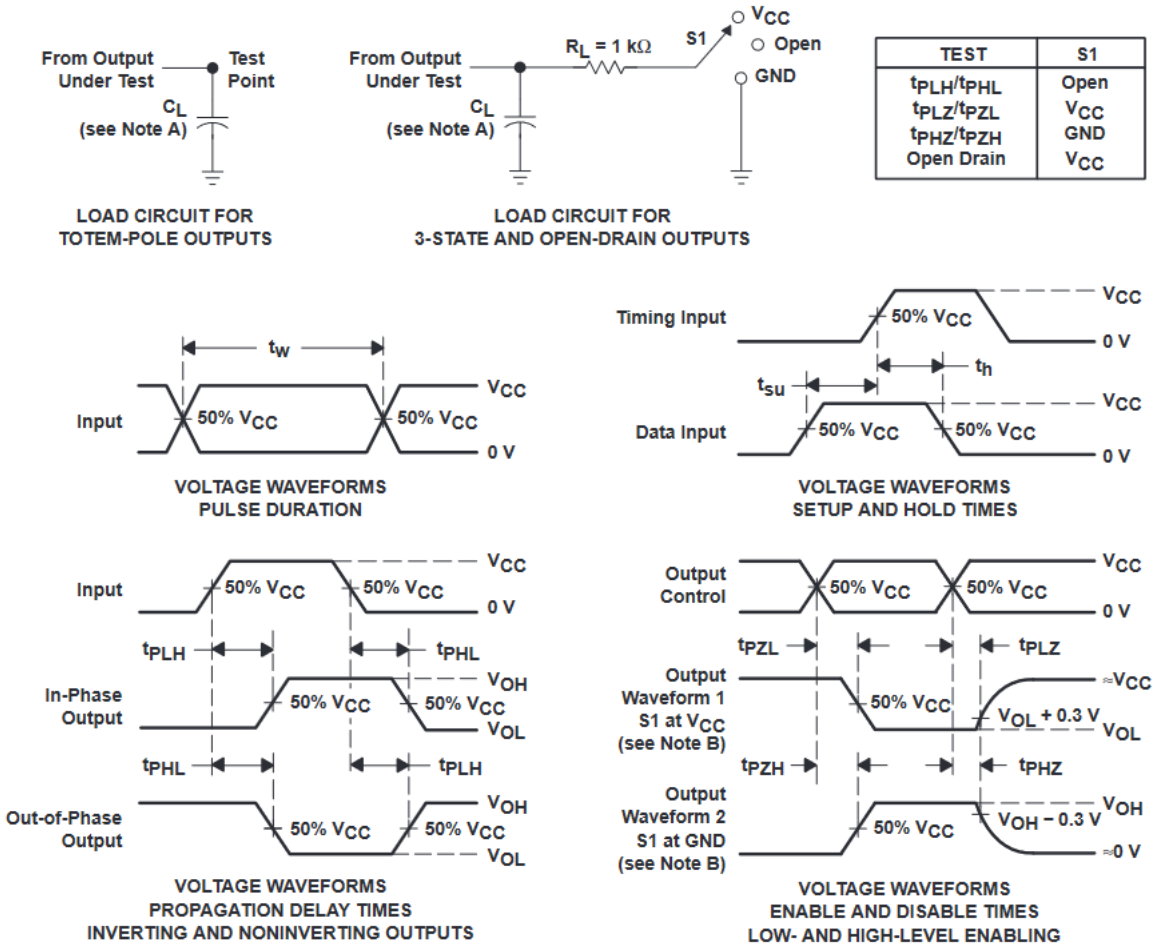


図 6-1. Load Circuit and Voltage Waveforms

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

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7 Detailed Description

7.1 Overview

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The SN74LV21A devices perform the Boolean function Y = A • B • C • D in positive logic. These dual 4-input positive-AND gates are designed for 2-V to 5.5-V V_{CC} operation.

7.2 Functional Block Diagram

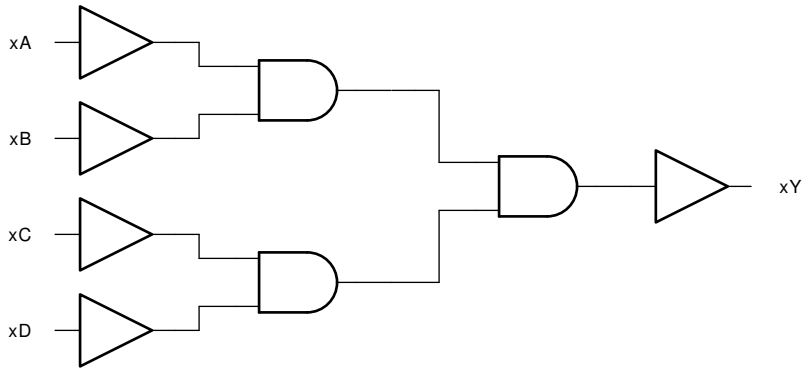


図 7-1. logic diagram (positive logic)

7.3 Device Functional Modes

Function Table
(each gate)

INPUTS(1)				OUTPUT(2)
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

(1) H = High Voltage Level, L = Low Voltage Level, X = Do not Care, Z = High Impedance
(2) H = Driving High, L = Driving Low, Z = High Impedance State

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8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV21A	Click here	Click here	Click here	Click here	Click here

8.2 ドキュメントの更新通知を受け取る方法

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV21AD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	LV21A
SN74LV21ADBR	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV21A
SN74LV21ADBR.A	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV21A
SN74LV21ADGVR	NRND	Production	TVSOP (DGV) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV21A
SN74LV21ADGVR.A	NRND	Production	TVSOP (DGV) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV21A
SN74LV21ADR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LV21A
SN74LV21ADR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV21A
SN74LV21ANSR	Last Time Buy	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV21A
SN74LV21ANSR.A	Last Time Buy	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV21A
SN74LV21APW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 85	LV21A
SN74LV21APWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LV21A
SN74LV21APWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV21A
SN74LV21APWRG4	Active	Production	TSSOP (PW) | 14	2000 | null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV21A
SN74LV21APWRG4	Active	Production	TSSOP (PW) | 14	2000 | null	No	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV21A
SN74LV21APWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV21A
SN74LV21APWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | null	No	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV21A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

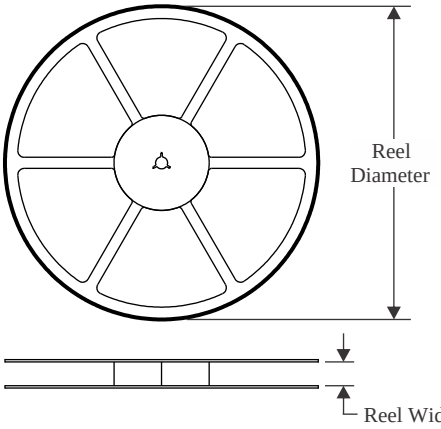
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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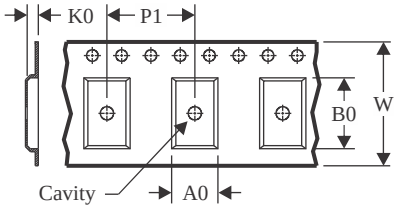
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

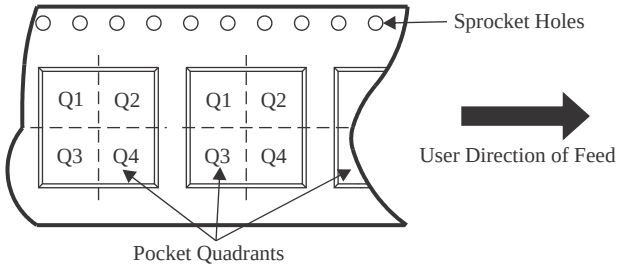


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

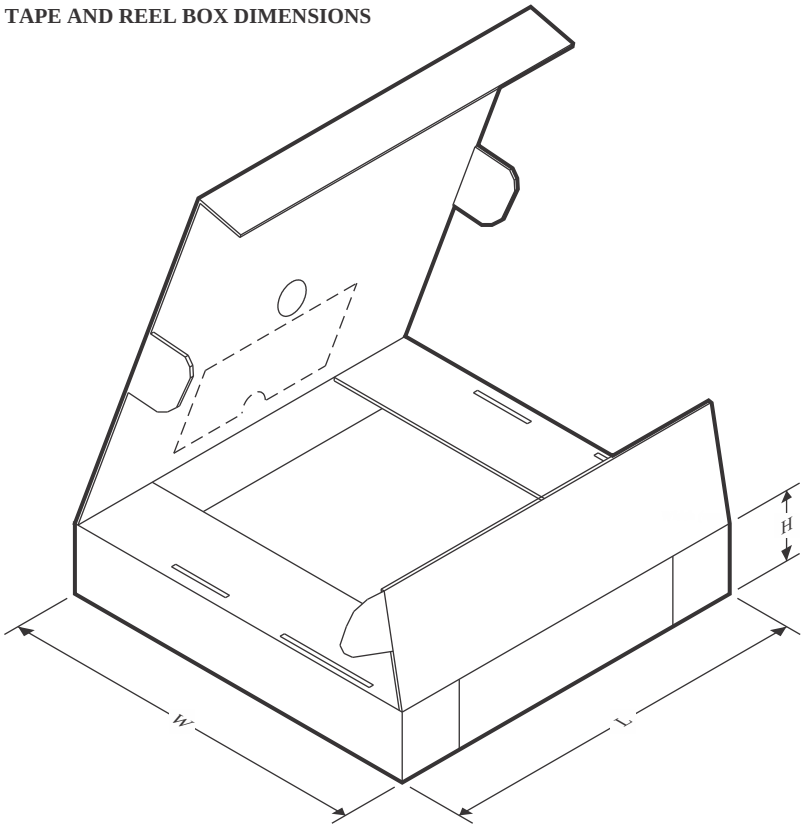
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

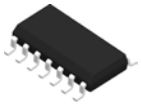
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV21ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV21ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV21ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV21ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LV21APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV21ADBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74LV21ADGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74LV21ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LV21ANSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74LV21APWR	TSSOP	PW	14	2000	353.0	353.0	32.0

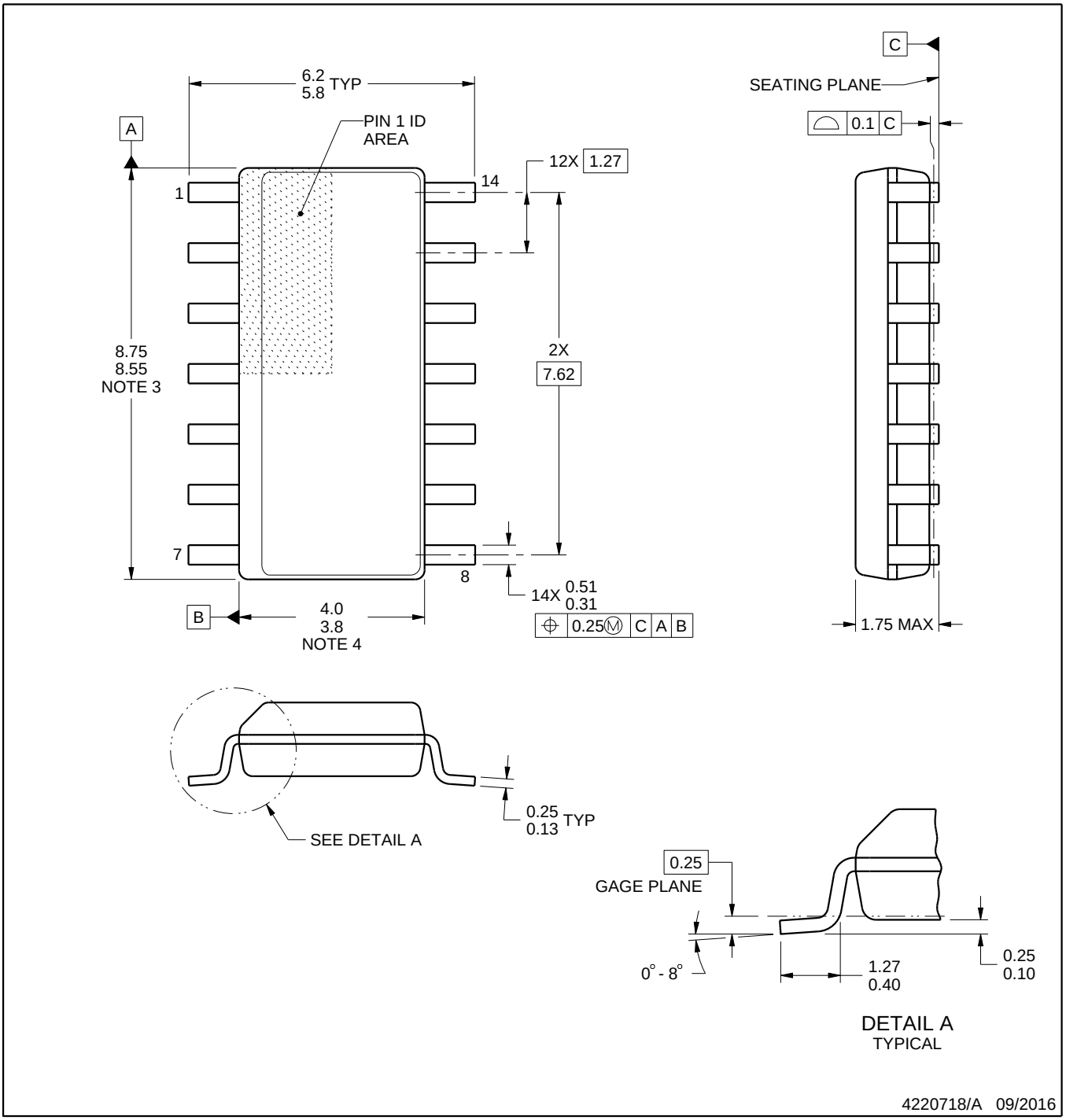


PACKAGE OUTLINE

D0014A

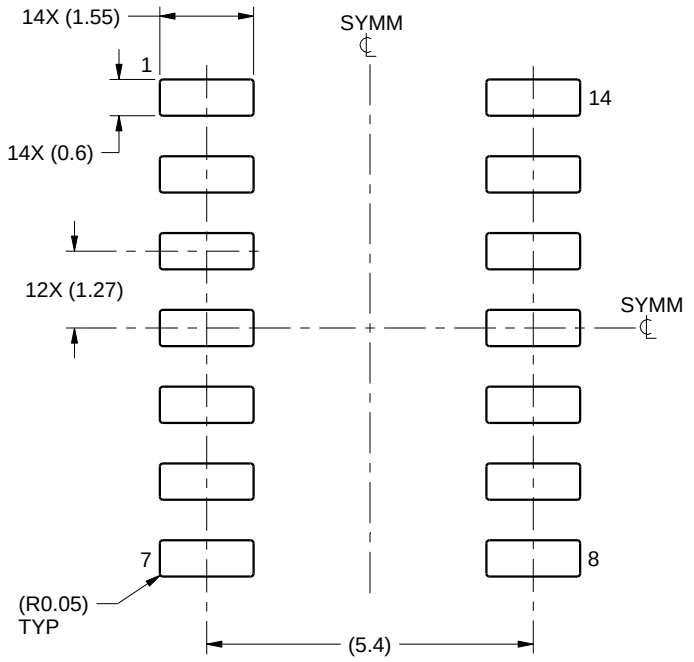
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

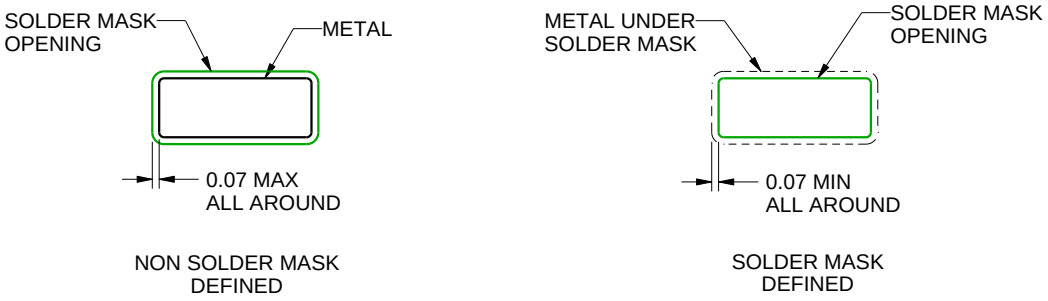


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

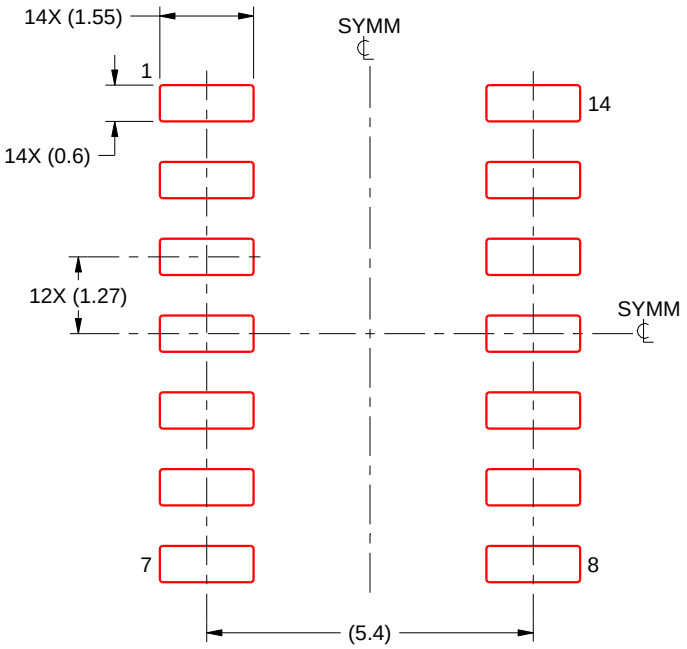
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

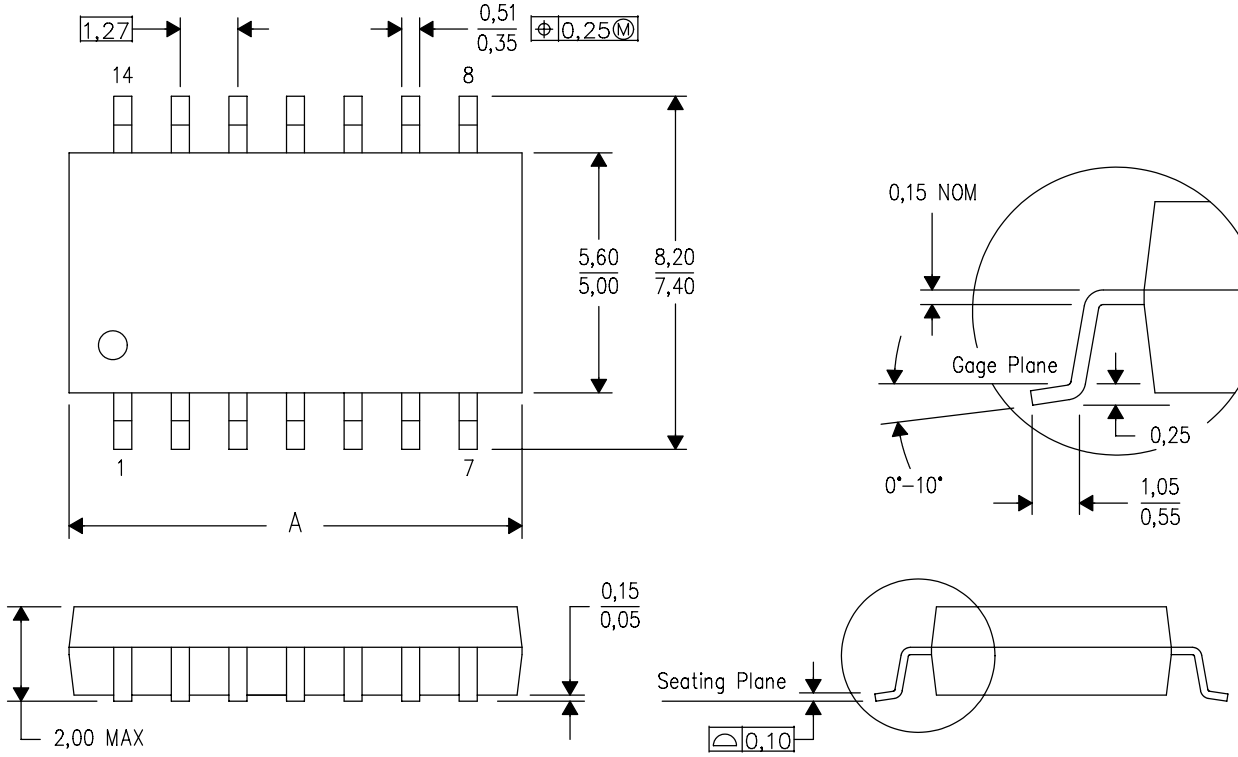
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



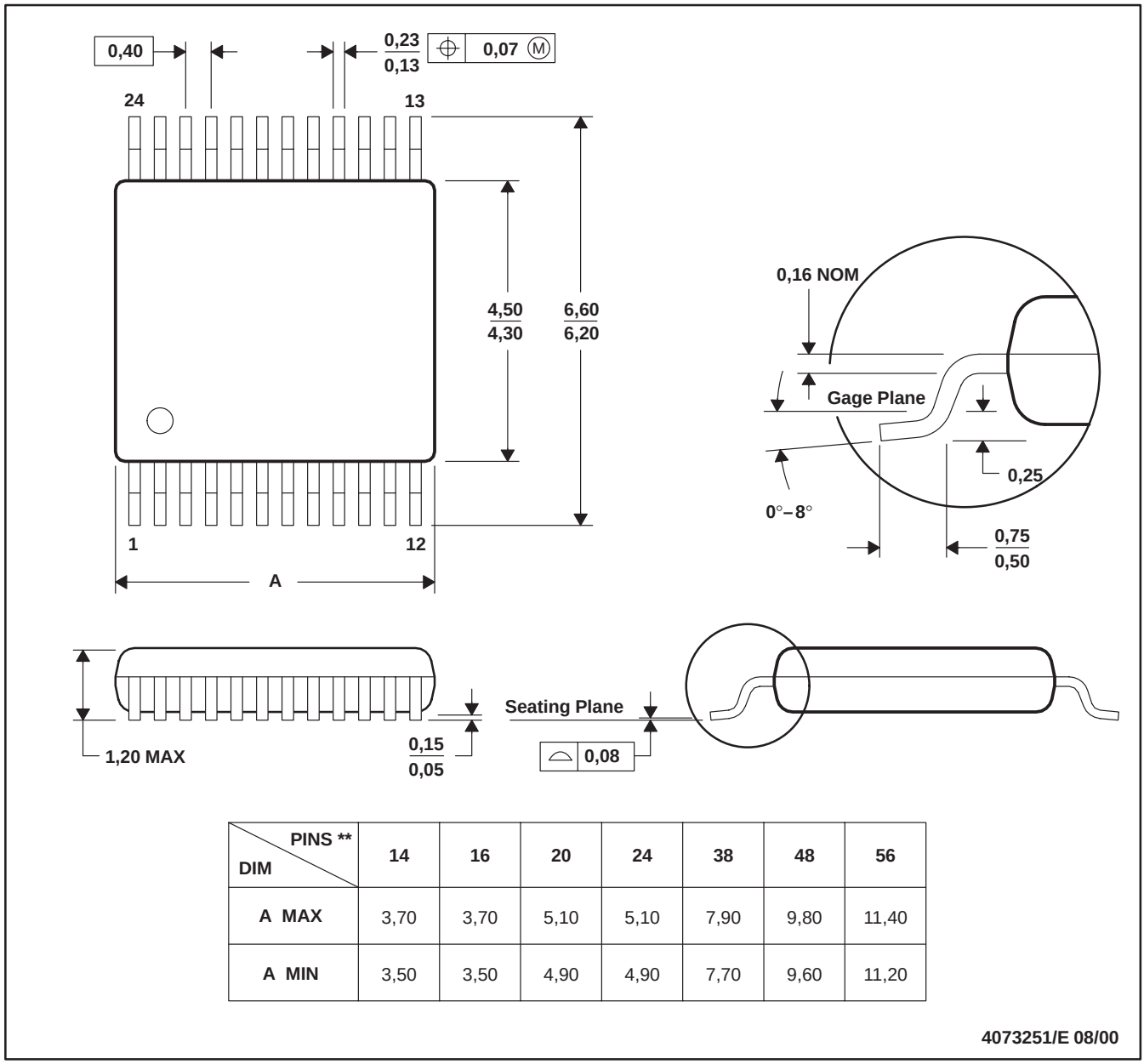
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

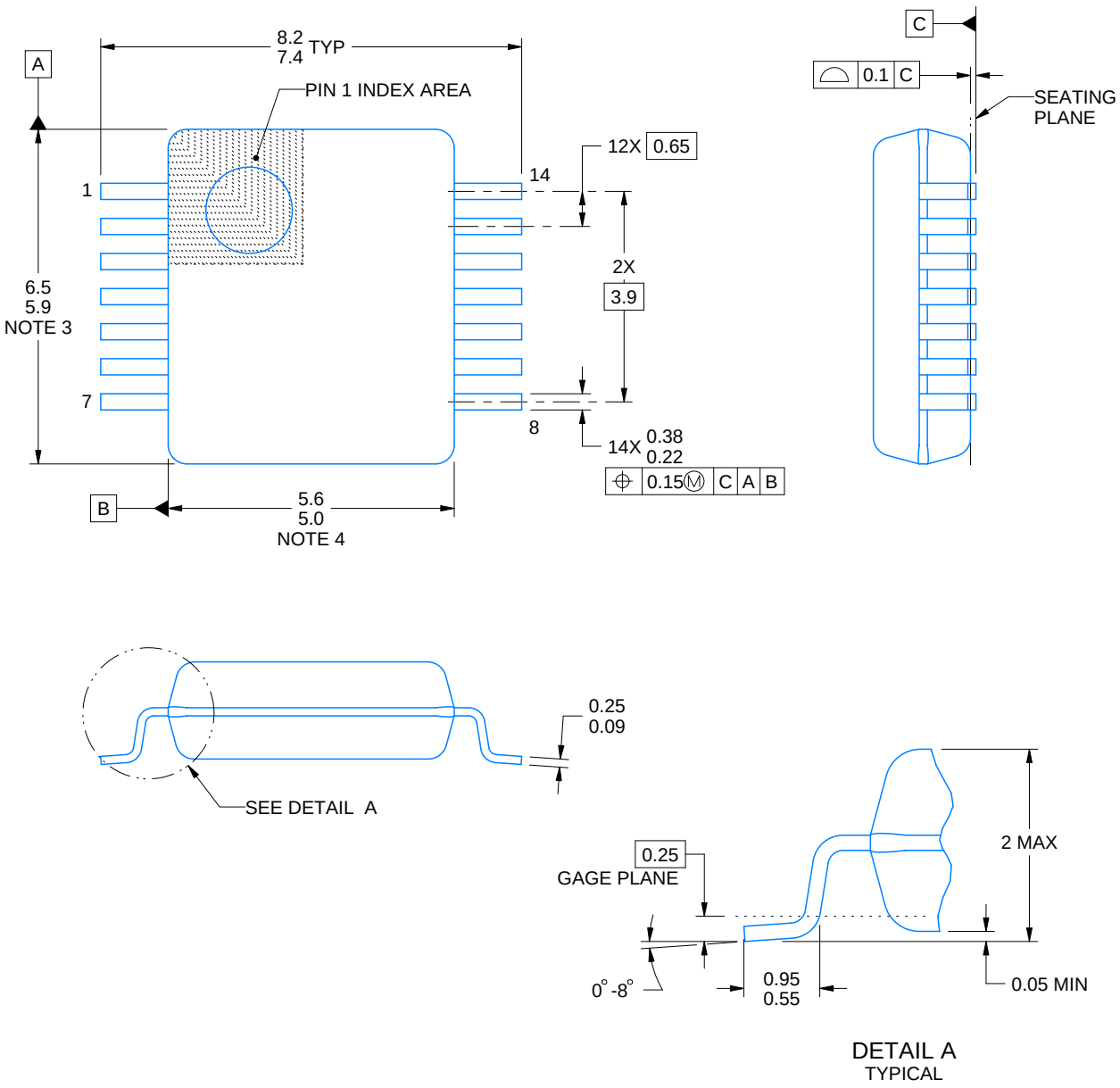
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

PACKAGE OUTLINE

DB0014A

SSOP - 2 mm max height

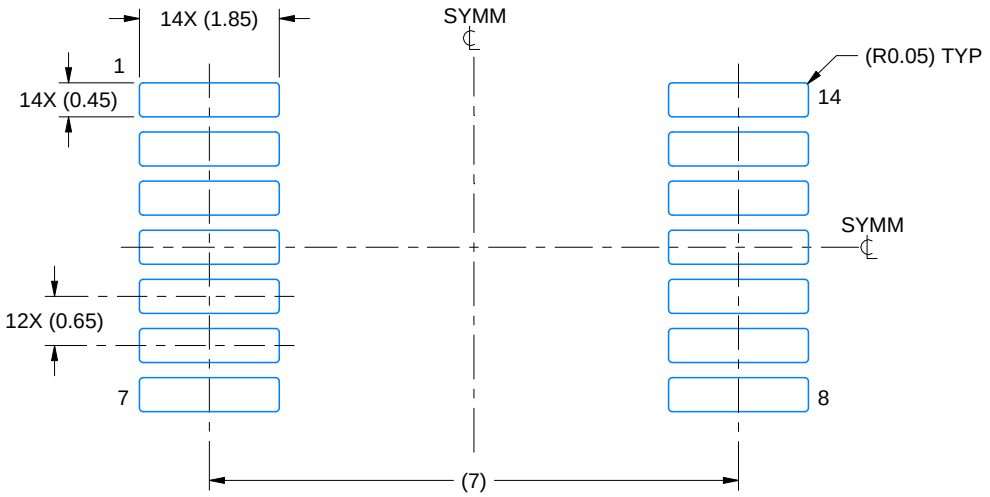
SMALL OUTLINE PACKAGE



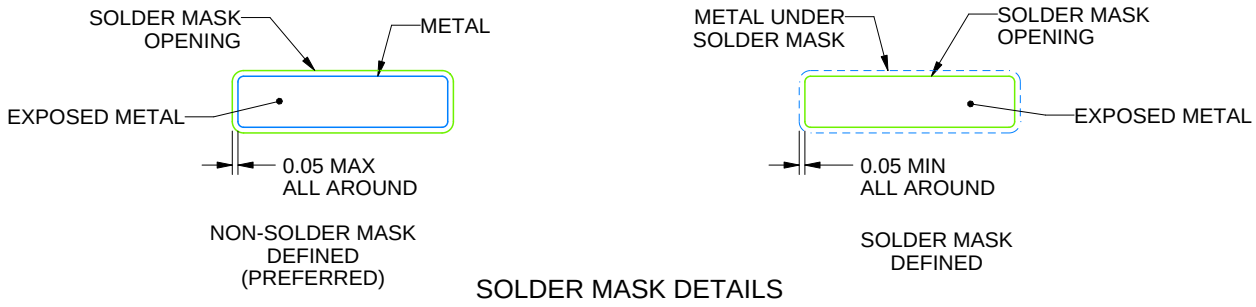
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

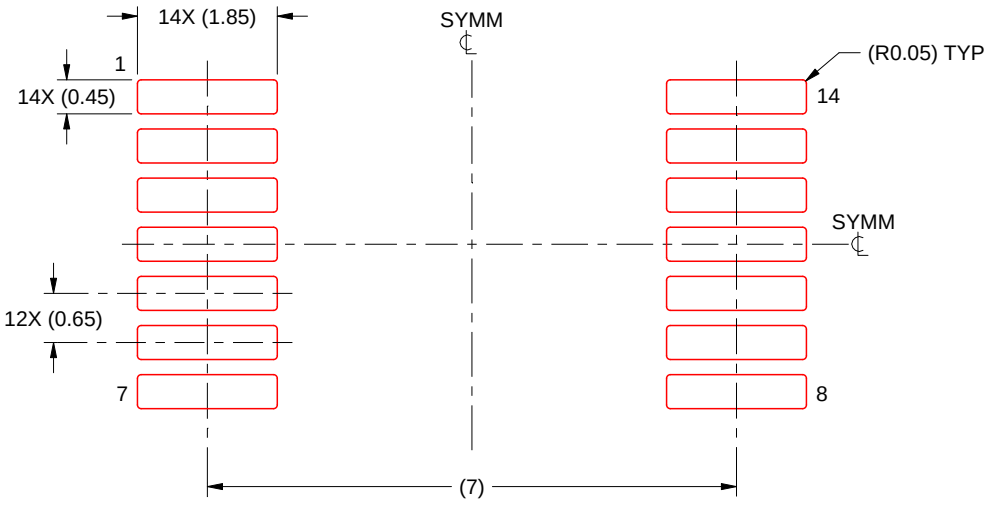


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

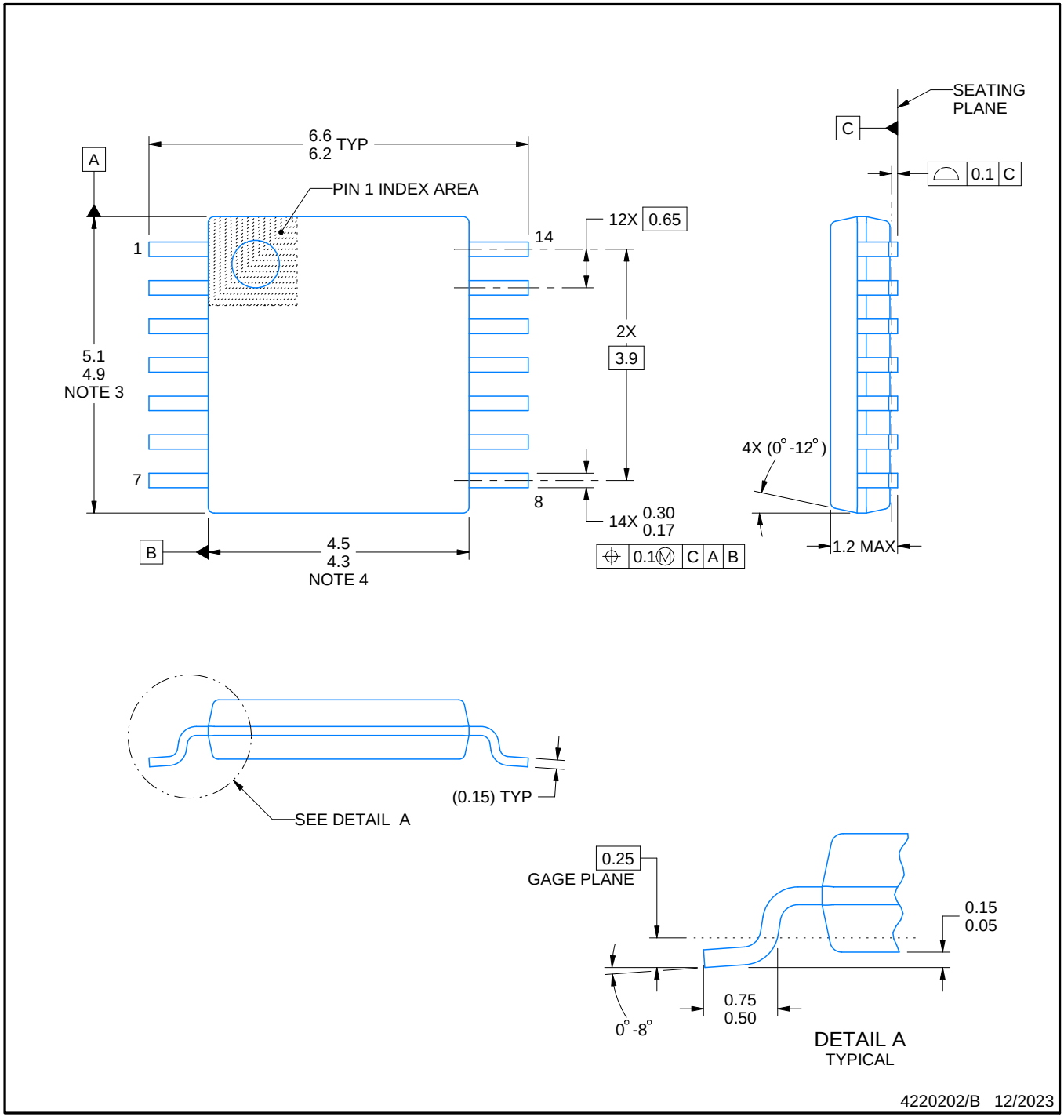
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

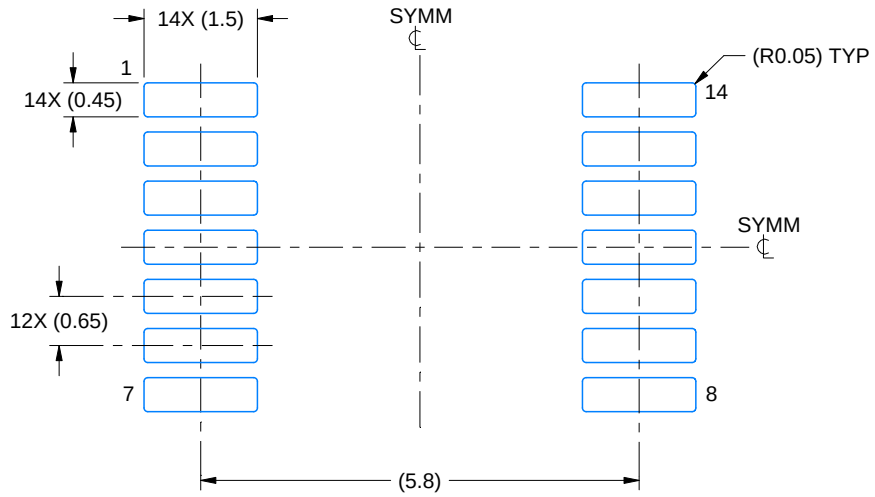
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

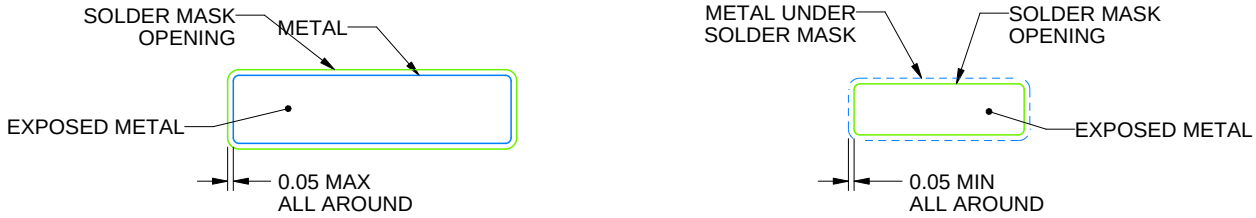


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

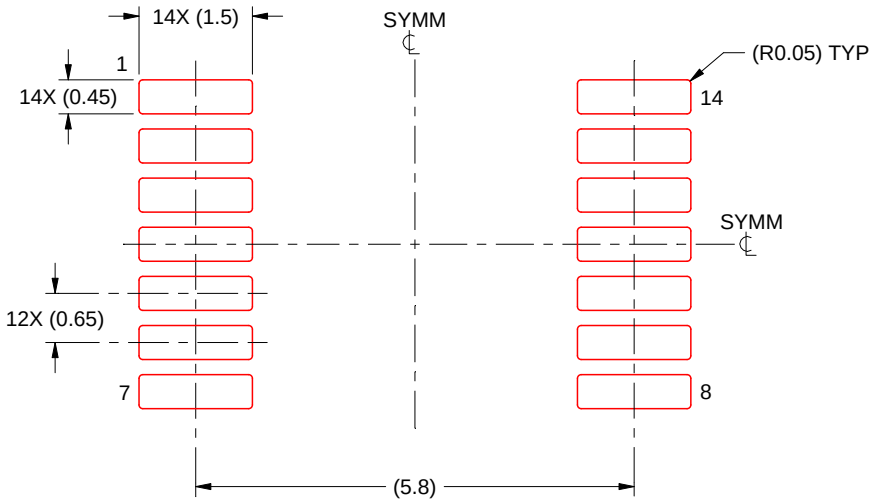


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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