SN74LV373A 3 ステート出力、オクタル・トランスペアレント D タイプ・ラッチ

1 特長

- V_{CC} 範囲:2V ～ 5.5V
- 最大 t_{pd} 8.5ns (5V 時)
- 標準 V_{OLP} (出力グランド・バウンス)
  < 0.8V (V_{CC} = 3.3V、T_A = 25℃)
- 標準 V_{OHV} (出力 V_{OH} アンダーシュート)
  > 2.3 V (V_{CC} = 3.3V、T_A = 25℃)
- すべて
  のポートで混在モード電圧動作をサポート
- I_{off} により部分的パワーダウン・モード動作をサポート
- JESD 17 準拠で 250mA 超のラッチアップ性能

2 アプリケーション

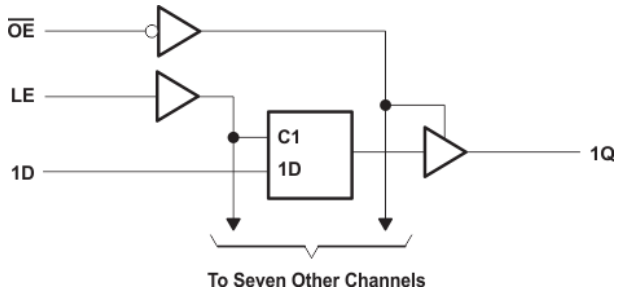
- プリンタ
- ネットワーク・スイッチ
- 試験および測定機器
- ワイヤレス・インフラ
- モータ制御
- サーバー・マザーボード

3 概要

SN74LV373A デバイスは、2V～5.5V の V_{CC} で動作するように設計されたオクタル・トランスペアレント D タイプ・ラッチです。

パッケージ情報

部品番号	パッケージ	本体サイズ (公称)
SN74LV373A	VQFN (20)	4.50 × 3.50mm
	SSOP (20)	7.50 × 5.30mm
	TSSOP (20)	6.50 × 4.40mm
	TVSOP (20)	5.00 × 4.40mm
	SOIC (20)	12.80 × 7.50mm
	SO (20)	12.60mm × 5.30mm



概略回路図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Pin Configuration and Functions ... 3
5 Specifications ... 4
5.1 Absolute Maximum Ratings ... 4
5.2 ESD Ratings ... 4
5.3 Recommended Operating Conditions ... 5
5.4 Thermal Information ... 5
5.5 Electrical Characteristics ... 6
5.6 Timing Requirements, V_{CC} = 2.5 V ± 0.2 V ... 6
5.7 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V ... 6
5.8 Timing Requirements, V_{CC} = 5 V ± 0.5 V ... 6
5.9 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V ... 7
5.10 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V ... 7
5.11 Switching Characteristics, V_{CC} = 5 V ± 0.5 V ... 7
5.12 Noise Characteristics ... 8
5.13 Operating Characteristics ... 8
5.14 Typical Characteristics ... 8
6 Parameter Measurement Information ... 9
7 Detailed Description ... 10
7.1 Overview ... 10
7.2 Functional Block Diagram ... 10
7.3 Feature Description ... 10
7.4 Device Functional Modes ... 10
8 Application and Implementation ... 11
8.1 Application Information ... 11
8.2 Typical Application ... 11
8.3 Layout ... 12
9 Device and Documentation Support ... 13
9.1 Receiving Notification of Documentation Updates ... 13
9.2 Community Resources ... 13
9.3 Trademarks ... 13
10 Revision History ... 13
11 Mechanical, Packaging, and Orderable Information ... 13

Copyright © 2023 Texas Instruments Incorporated

4 Pin Configuration and Functions

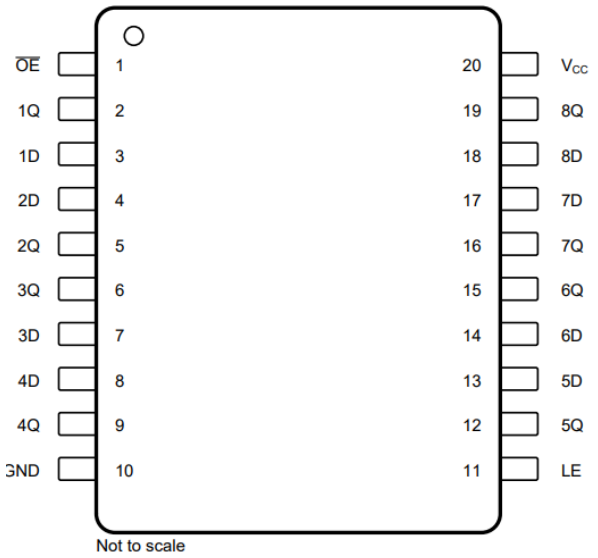


図 4-1. DB, DGV, DW, NS, or PW 20-Pin SSOP, TVSOP, SOIC, SO, or TSSOP Top View

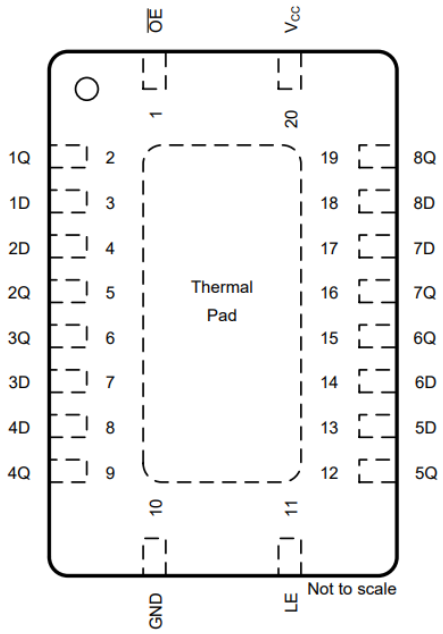


図 4-2. RGY Package 20-Pin VQFN Top View

表 4-1. Pin Functions

PIN			TYPE	DESCRIPTION
NO.	SSOP, TVSOP, SOIC, SO, or TSSOP	VQFN		
1	$\overline{OE}$	$\overline{OE}$	I	Output Enable
2	1Q	1Q	O	1Q Output
3	1D	1D	I	1D Input
4	2D	2D	I	2D Input
5	2Q	2Q	O	2Q Output
6	3Q	3Q	O	3Q Output
7	3D	3D	I	3D Input
8	4D	4D	I	4D Input
9	4Q	4Q	O	4Q Output
10	GND	GND	—	Ground Pin
11	LE	LE	I	Latch Enable
12	5Q	5Q	O	5Q Output
13	5D	5D	I	5D Input
14	6D	6D	I	6D Input
15	6Q	6Q	O	6Q Output
16	7Q	7Q	O	7Q Output
17	7D	7D	I	7D Input
18	8D	8D	I	8D Input
19	8Q	8Q	O	8Q Output
20	V_{CC}	V_{CC}	—	Power Pin
—	—	Thermal Pad	—	Thermal Pad, normally tied to GND

Copyright © 2023 Texas Instruments Incorporated

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
V_O	Output voltage(2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±35	mA
	Continuous channel current through V_{CC} or GND			±70	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under セクション 5.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5-V maximum.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±2000	
		Machine Model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Copyright © 2023 Texas Instruments Incorporated

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V ± 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V ± 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V ± 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V ± 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V ± 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V ± 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2 V		–50	µA
		V_{CC} = 2.3 V ± 2.7 V		–2	mA
		V_{CC} = 3 V ± 3.6 V		–8	
		V_{CC} = 4.5 V ± 5.5 V		–16	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 2.3 V ± 2.7 V		2	mA
		V_{CC} = 3 V ± 3.6 V		8	
		V_{CC} = 4.5 V ± 5.5 V		16	
Δt/Δv	Input transition rise or fall	V_{CC} = 2.3 V ± 2.7 V		200	ns/V
		V_{CC} = 3 V ± 3.6 V		100	
		V_{CC} = 4.5 V ± 5.5 V		20	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

5.4 Thermal Information

THERMAL METRIC(1)		SN74LV373A						UNIT
		DB (SSOP)	DGV (TVSOP)	DW (SOIC)	NS (SO)	PW (TSSOP)	RGY (VQFN)	
		20 PINS						
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.5	116.2	79.2	76.7	128.2	34.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.4	31.2	43.7	43.2	70.5	42.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	57.7	47.0	44.2	79.3	12.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.5	0.9	18.6	16.8	23.4	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.3	57.0	46.5	43.8	78.9	12.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	7.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Copyright © 2023 Texas Instruments Incorporated

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			–40°C to +85°C		–40°C to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 µA	2 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1		V_{CC} – 0.1		V
	I_{OH} = –2 mA	2.3 V	2			2		2		
	I_{OH} = –8 mA	3 V	2.48			2.48		2.48		
	I_{OH} = –16 mA	4.5 V	3.8			3.8		3.8		
V_{OL}	I_{OL} = 50 µA	2 V to 5.5 V			0.1		0.1		0.1	V
	I_{OL} = 2 mA	2.3 V			0.4		0.4		0.4	
	I_{OL} = 8 mA	3 V			0.44		0.44		0.44	
	I_{OL} = 16 mA	4.5 V			0.55		0.55		0.55	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±1		±1		±1	µA
I_{OZ}	V_I = V_{CC} or GND	5.5 V			±5		±5		±5	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20		20		20	µA
I_{off}	V_I or V_O = 0 to V_{CC}	0			5		5		5	µA
C_i	V_I = V_{CC} or GND	3.3 V		2.9						pF

5.6 Timing Requirements, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see 図 6-1)

			T_A = 25°C		–40°C to +85°C		–40°C to +125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		6		6.5		6.5		ns
t_{su}	Setup time, data before LE ↓	High or low	4.5		5		5.5		ns
t_h	Hold time, data after LE ↓	High or low	1.5		1.5		2		ns

5.7 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see 図 6-1)

			T_A = 25°C		–40°C to +85°C		–40°C to +125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		5		5		5		ns
t_{su}	Setup time, data before LE ↓	High or low	4		4		4.5		ns
t_h	Hold time, data after LE ↓	High or low	1		1		1.5		ns

5.8 Timing Requirements, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see 図 6-1)

			T_A = 25°C		–40°C to +85°C		–40°C to +125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		5		5		5		ns
t_{su}	Setup time, data before LE ↓	High or low	4		4		4.5		ns
t_h	Hold time, data after LE ↓	High or low	1		1		1.5		ns

Copyright © 2023 Texas Instruments Incorporated

5.9 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40°C to +85°C		–40°C to +125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	C_L = 15 pF		8.3(1)	15.2(1)	1	17	1	18.5	ns
	LE	Q			9.1(1)	15.7(1)	1	19	1	20.5	
t_{en}	$\overline{OE}$	Q			8.9(1)	15.8(1)	1	19	1	20	
t_{dis}	$\overline{OE}$	Q			6.2(1)	12.6(1)	1	15	1	16.5	
t_{pd}	D	Q	C_L = 50 pF		10.4	18	1	21	1	22.5	ns
	LE	Q			11.1	18.6	1	22	1	23.5	
t_{en}	$\overline{OE}$	Q			10.9	18.8	1	22	1	23.5	
t_{dis}	$\overline{OE}$	Q			8.3	17.4	1	19	1	20.5	
$t_{sk(o)}$						2		2		2	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.10 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40°C to +85°C		–40°C to +125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	C_L = 15 pF		5.8(1)	11.4(1)	1	13.5	1	14.5	ns
	LE	Q			6.4(1)	11(1)	1	13	1	14	
t_{en}	$\overline{OE}$	Q			6.3(1)	11.4(1)	1	13.5	1	14.5	
t_{dis}	$\overline{OE}$	Q			4.7(1)	10(1)	1	12	1	12.5	
t_{pd}	D	Q	C_L = 50 pF		7.3	14.9	1	17	1	18	ns
	LE	Q			7.8	14.5	1	16.5	1	17.5	
t_{en}	$\overline{OE}$	Q			7.7	14.9	1	17	1	18	
t_{dis}	$\overline{OE}$	Q			6	13.2	1	15	1	15.5	
$t_{sk(o)}$						1.5		1.5		1.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.11 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40°C to +85°C		–40°C to +125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	C_L = 15 pF		4.1(1)	7.2(1)	1	8.5	1	9.5	ns
	LE	Q			4.5(1)	7.2(1)	1	8.5	1	9.5	
t_{en}	$\overline{OE}$	Q			4.5(1)	8.1(1)	1	9.5	1	10.5	
t_{dis}	$\overline{OE}$	Q			3.3(1)	7.2(1)	1	8.5	1	9	
t_{pd}	D	Q	C_L = 50 pF		5.1	9.2	1	10.5	1	11.5	ns
	LE	Q			5.5	9.2	1	10.5	1	11.5	
t_{en}	$\overline{OE}$	Q			5.5	10.1	1	11.5	1	12.5	
t_{dis}	$\overline{OE}$	Q			4	9.2	1	10.5	1	11	
$t_{sk(o)}$						1		1		1	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

Copyright © 2023 Texas Instruments Incorporated

5.12 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C(1)

PARAMETER		SN74LV373A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.6	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

5.13 Operating Characteristics

T_A = 25°C

PARAMETER			TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF	f = 10 MHz	3.3 V	17.4	pF
					5 V	19.5	

5.14 Typical Characteristics

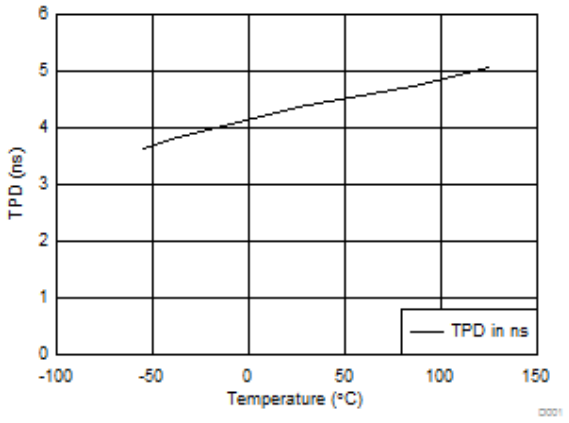


図 5-1. TPD vs Temperature at 5 V

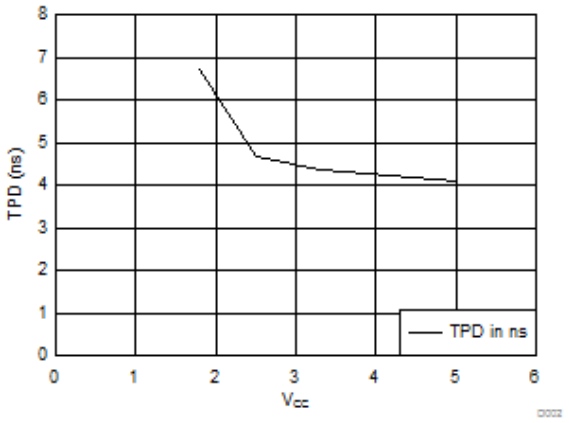
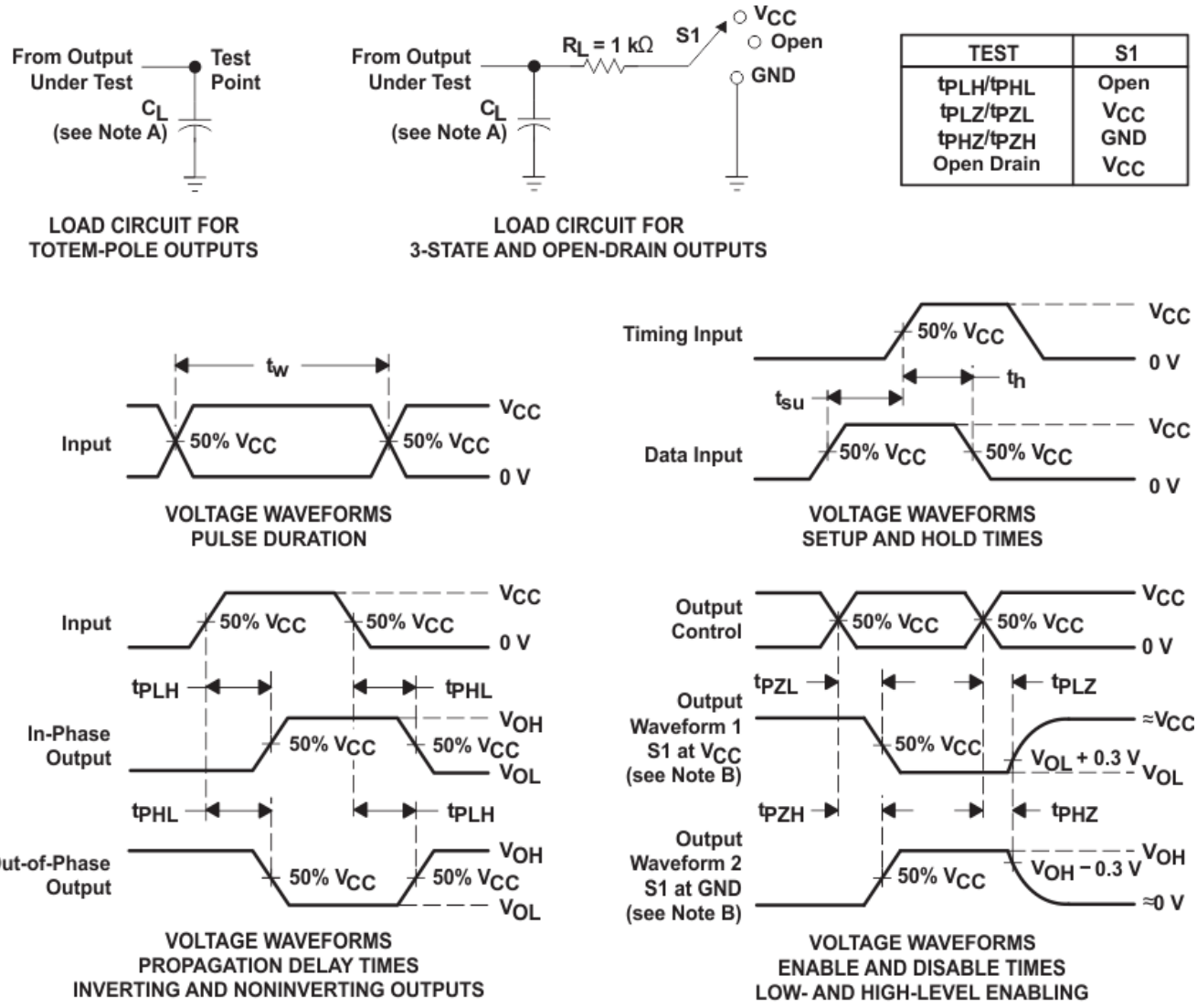


図 5-2. TPD vs V_{CC} at 25°C

Copyright © 2023 Texas Instruments Incorporated

6 Parameter Measurement Information

6.1



NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

図 6-1. Load Circuit and Voltage Waveforms

Copyright © 2023 Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

The SN74LV373A device is an octal transparent D-type latch designed for 2 V to 5.5 V V_{CC} operation.

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

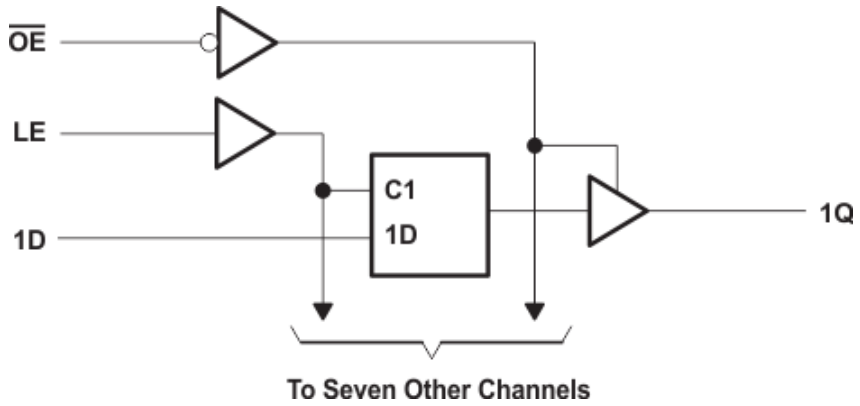
At power-up, the state of the Q outputs are not predictable until the first valid clock.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pull-up components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram



7.3 Feature Description

- Wide operating voltage range
  - Operates from 2 V to 5.5 V
- Allows down-voltage translation
  - Inputs accept voltages to 5.5 V
- Slow edges reduce output ringing

7.4 Device Functional Modes

表 7-1 shows the functional modes of SN74LV373A.

表 7-1. Function Table
(Each Latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Copyright © 2023 Texas Instruments Incorporated

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The SN74LV540A device is a low-drive CMOS device that can be used for a multitude of bus interface type applications where putput ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are tolerant to 5.5 V at any valid V_{CC}. This feature makes it Ideal for translating down to the V_{CC} level. 図 8-2 shows the reduction in ringing compared to higher drive parts such as AC.

8.2 Typical Application

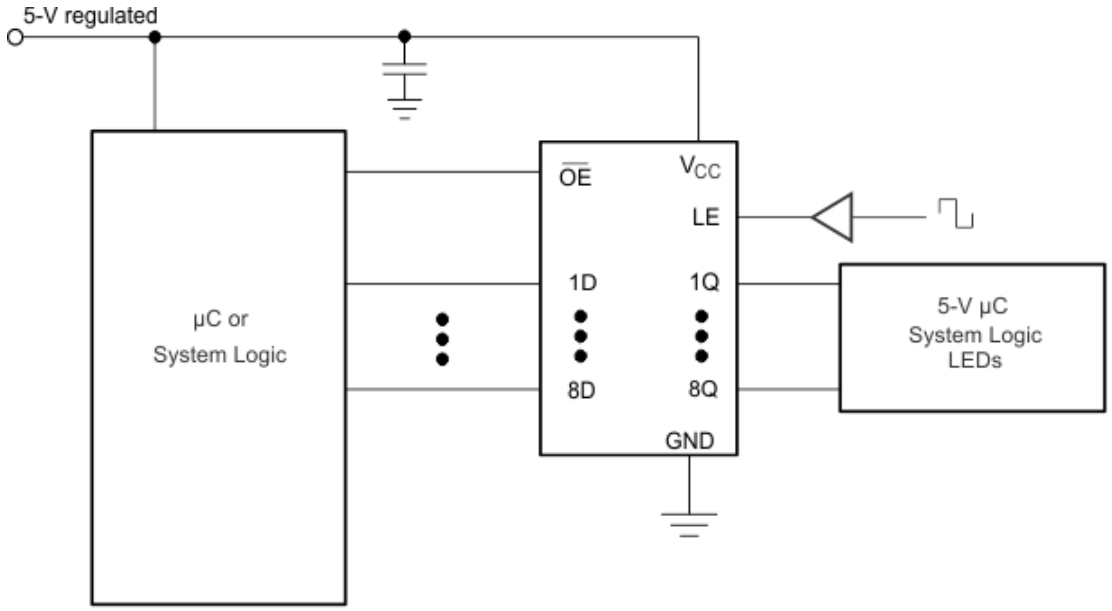


図 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For rise time and fall time specifications, see Δt/ΔV in the *セクション 5.3* table.
   - For specified High and low levels, see V_{IH} and V_{IL} in the *セクション 5.3* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommend Output Conditions
   - Load currents should not exceed 35 mA per output and 70 mA total for the part.
   - Outputs should not be pulled above V_{CC}.

Copyright © 2023 Texas Instruments Incorporated

8.2.3 Application Curves

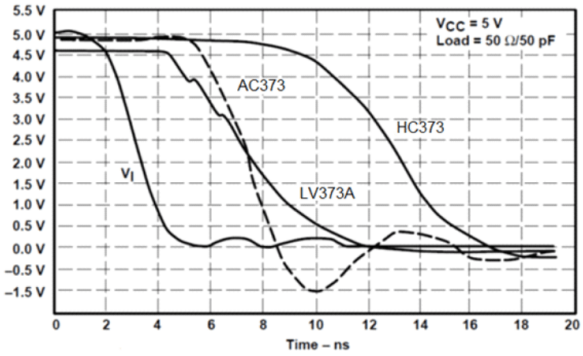


図 8-2. Switching Characteristics Comparison

Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *セクション 5.3* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple V_{CC} pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.3 Layout

8.3.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in 図 8-3 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

8.3.2 Layout Example

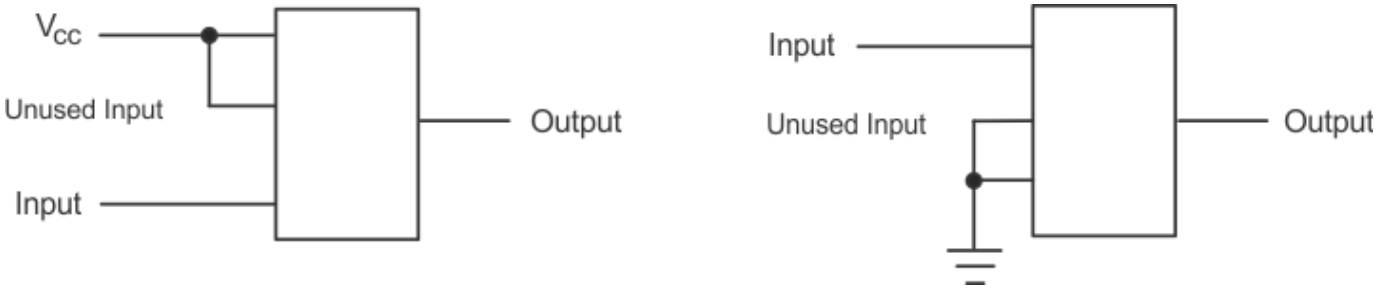


図 8-3. Layout Diagram

Copyright © 2023 Texas Instruments Incorporated

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Community Resources

9.3 Trademarks

すべての商標は、それぞれの所有者に帰属します。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision M (December 2022) to Revision N (December 2023)	Page
• Updated thermal values for PW package from RθJA = 102.4 to 128.2, RθJC(top) = 36.5 to 70.5, RθJB = 53.6 to 79.3, ΨJT = 2.4 to 23.4, ΨJB = 52.9 to 78.9, all values in °C/W	5

Changes from Revision L (August 2016) to Revision M (December 2022)	Page
• 文書全体にわたって表、図、相互参照の形式を更新	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2023 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV373ADBR	NRND	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV373A
SN74LV373ADBR.A	NRND	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV373A
SN74LV373ADGSR	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L373A
SN74LV373ADGSR.A	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L373A
SN74LV373ADGVR	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV373A
SN74LV373ADGVR.A	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV373A
SN74LV373ADW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-40 to 125	LV373A
SN74LV373ADWR	Last Time Buy	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV373A
SN74LV373ADWR.A	Last Time Buy	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV373A
SN74LV373ANSR	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV373A
SN74LV373ANSR.A	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV373A
SN74LV373APW	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 125	LV373A
SN74LV373APWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV373A
SN74LV373APWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV373A
SN74LV373APWRG4	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV373A
SN74LV373APWRG4.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV373A
SN74LV373APWT	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 125	LV373A
SN74LV373ARGYR	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV373A
SN74LV373ARGYR.A	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV373A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV373A :

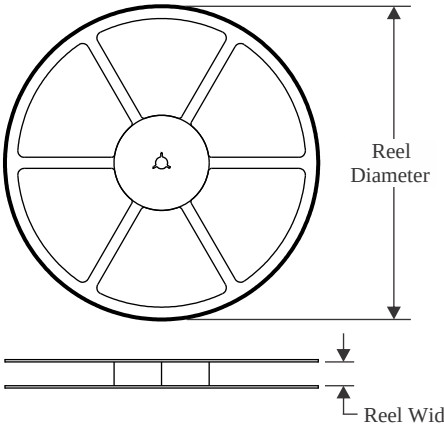
- Automotive : SN74LV373A-Q1

NOTE: Qualified Version Definitions:

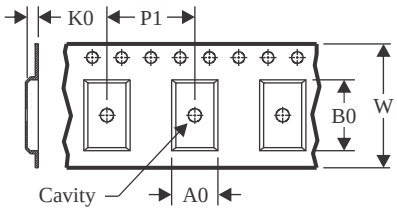
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

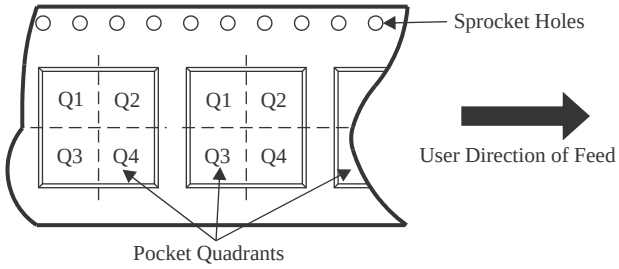


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

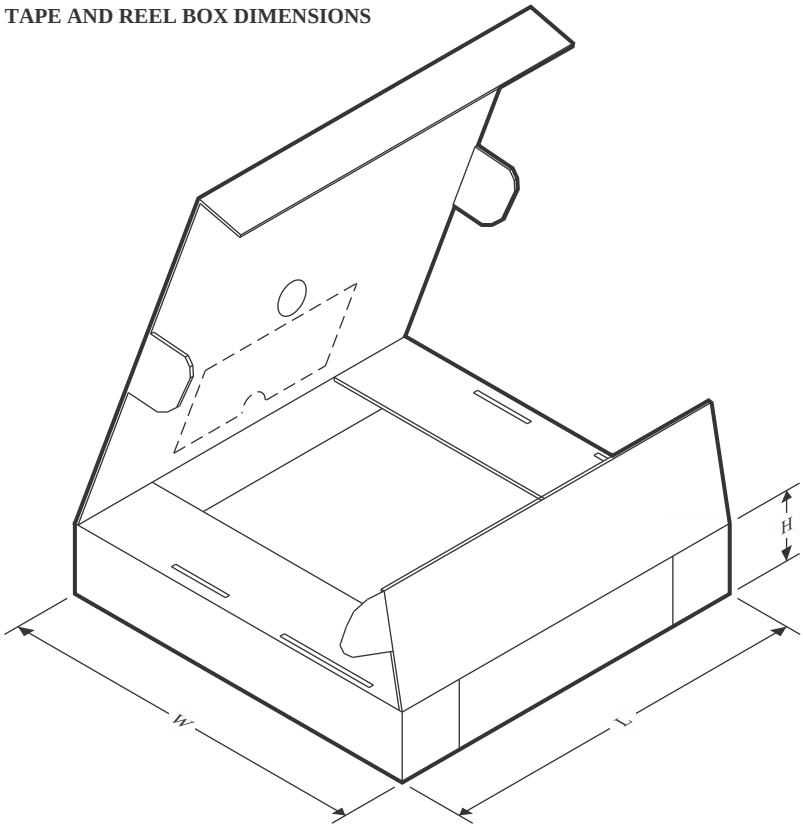
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV373ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV373ADGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74LV373ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV373ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV373ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV373APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV373APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV373ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

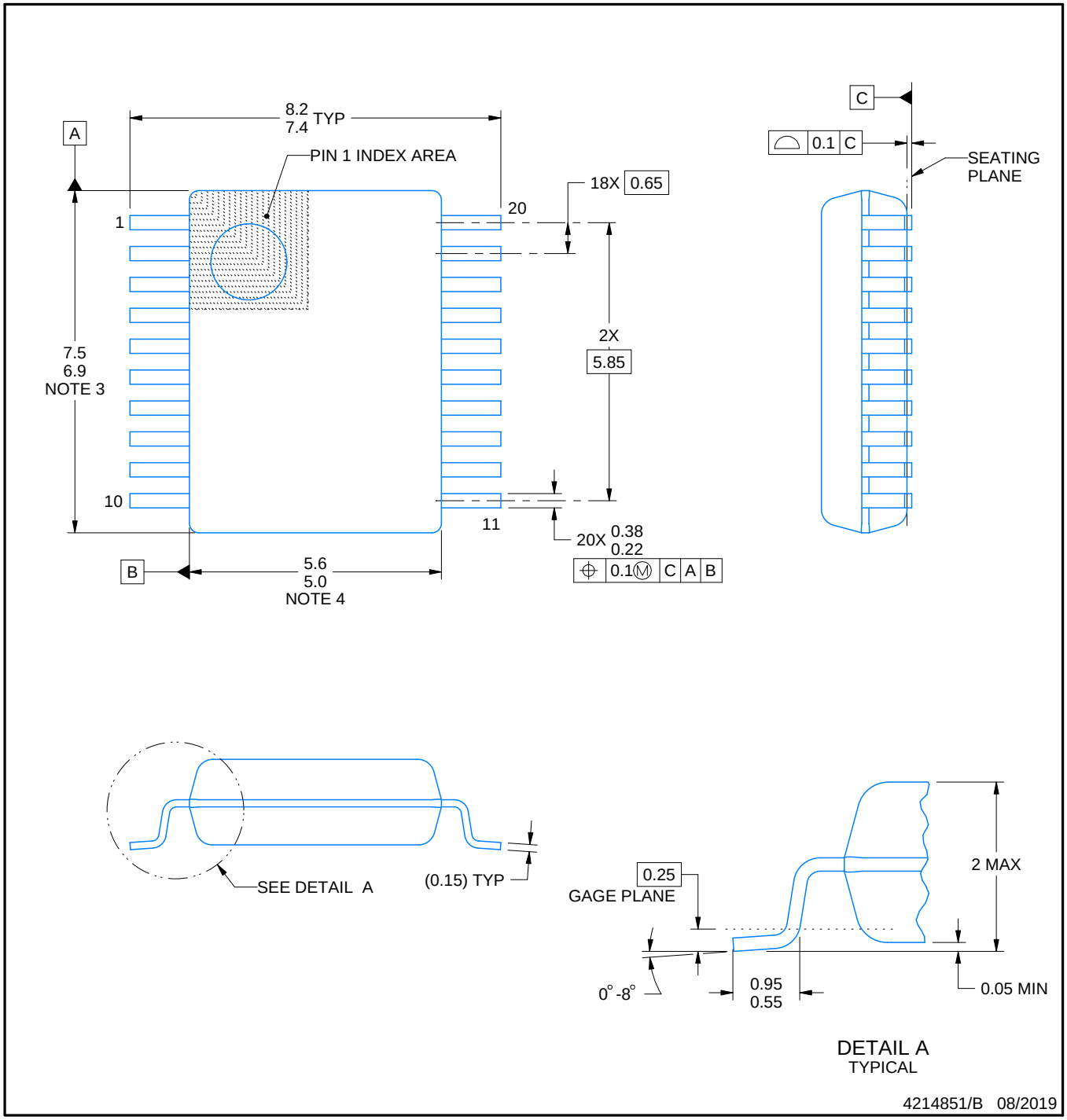
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV373ADBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74LV373ADGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74LV373ADGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74LV373ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LV373ANSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LV373APWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LV373APWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LV373ARGYR	VQFN	RGY	20	3000	353.0	353.0	32.0

PACKAGE OUTLINE

DB0020A

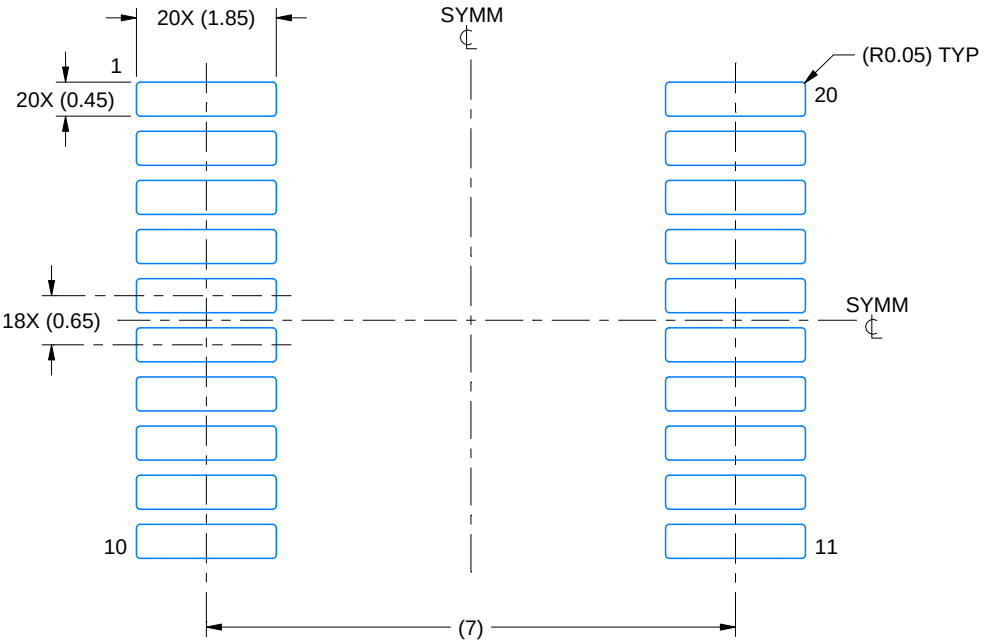
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

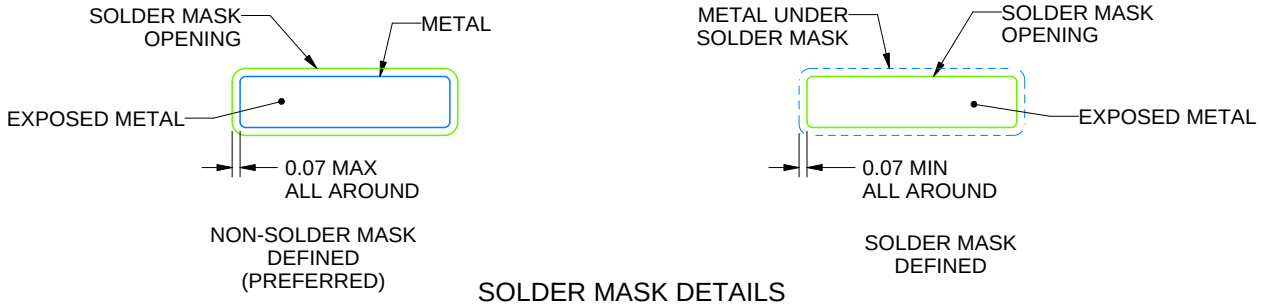


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

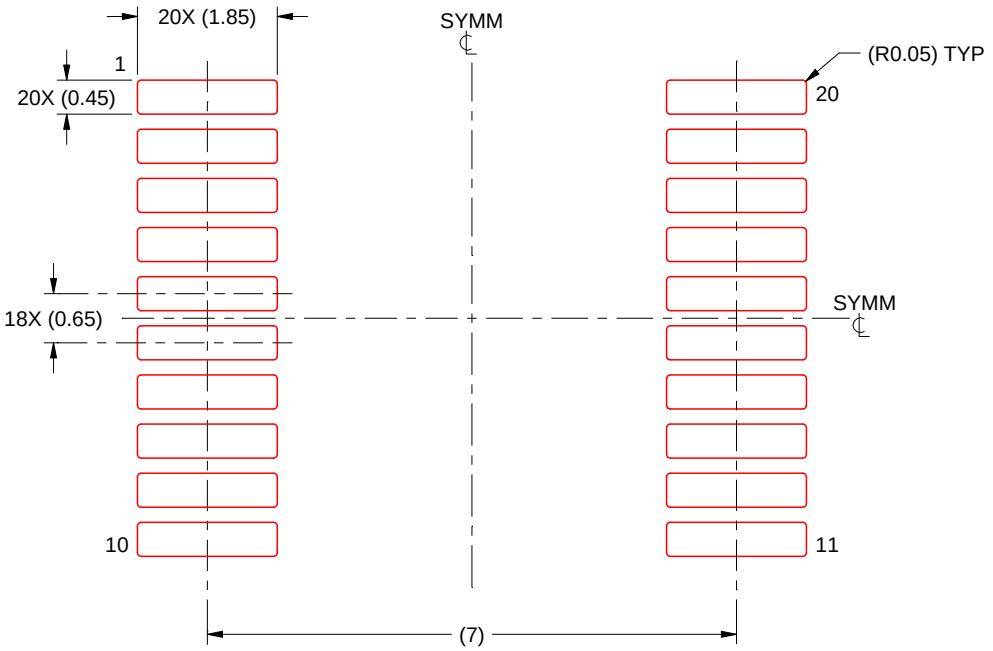
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

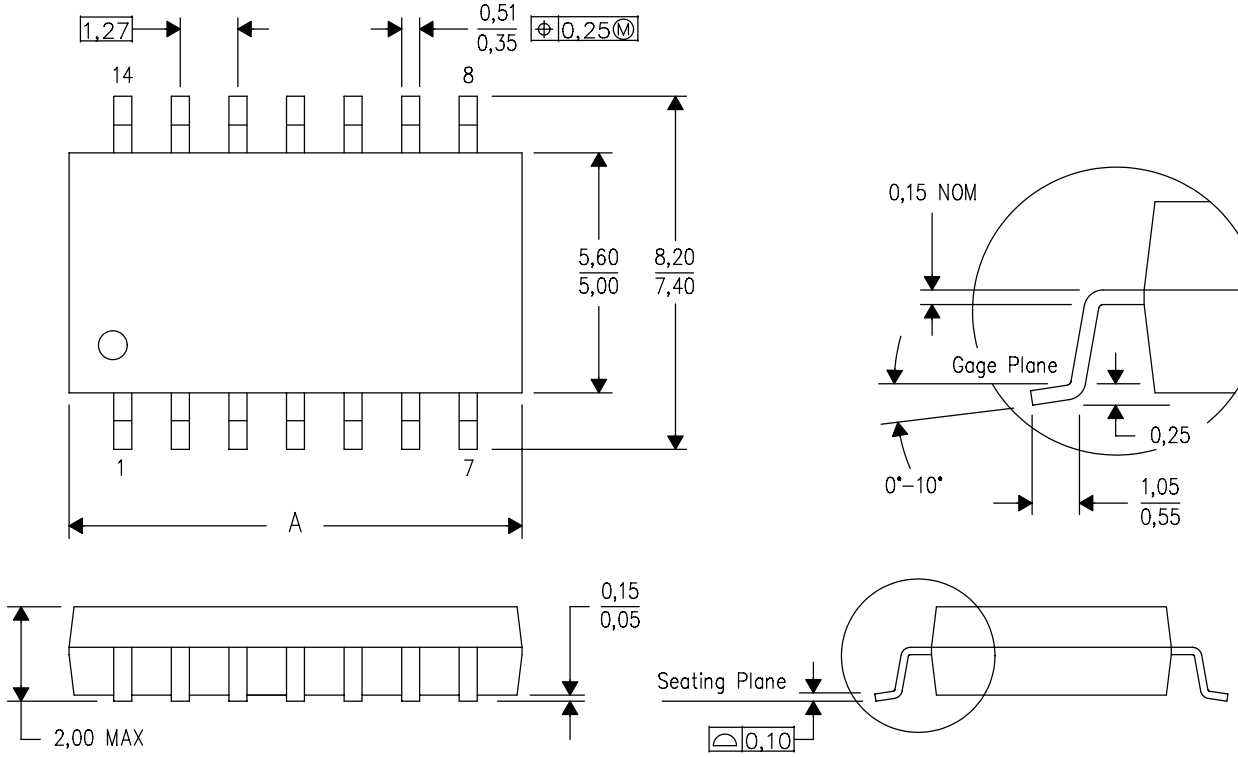
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



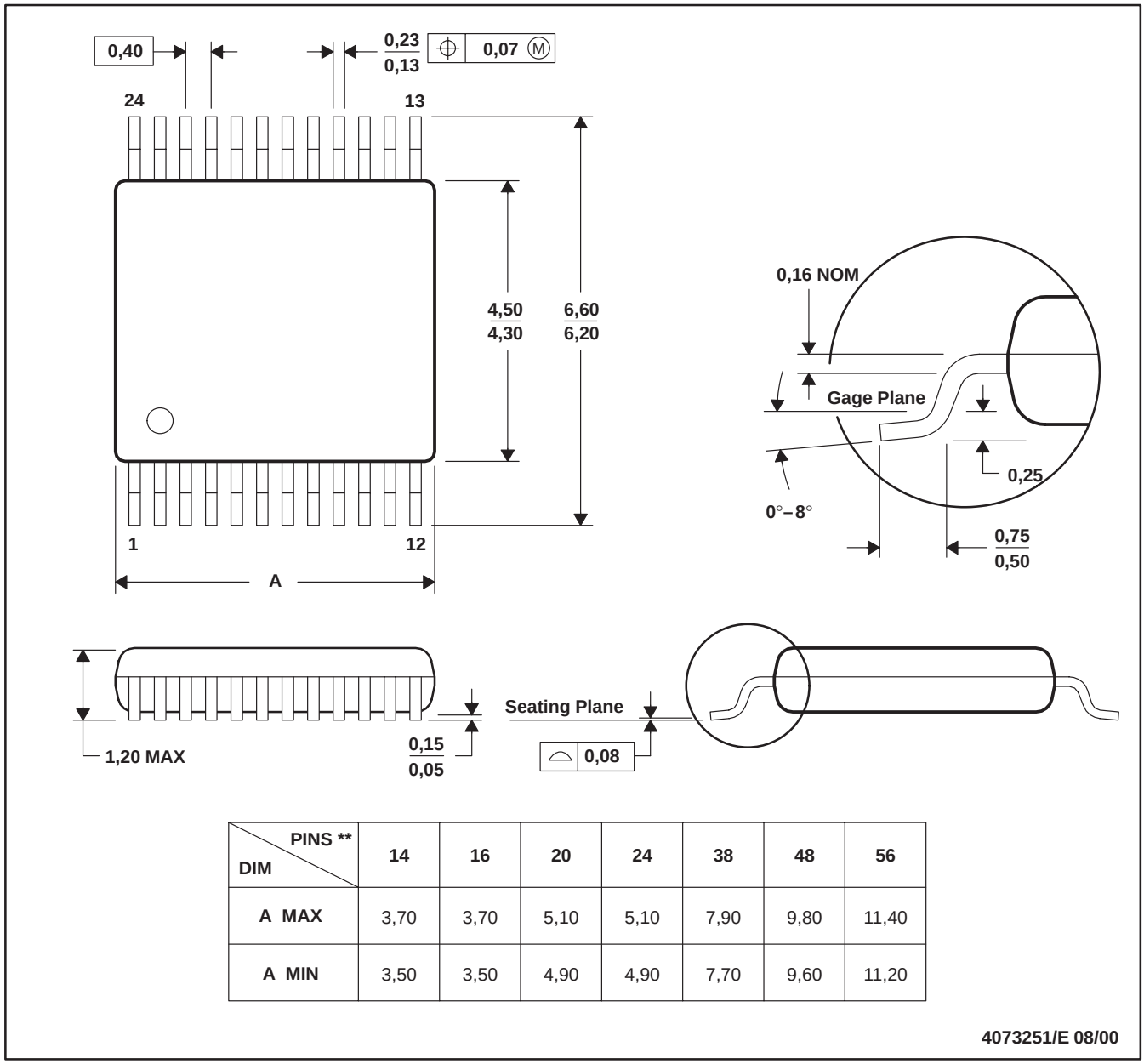
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

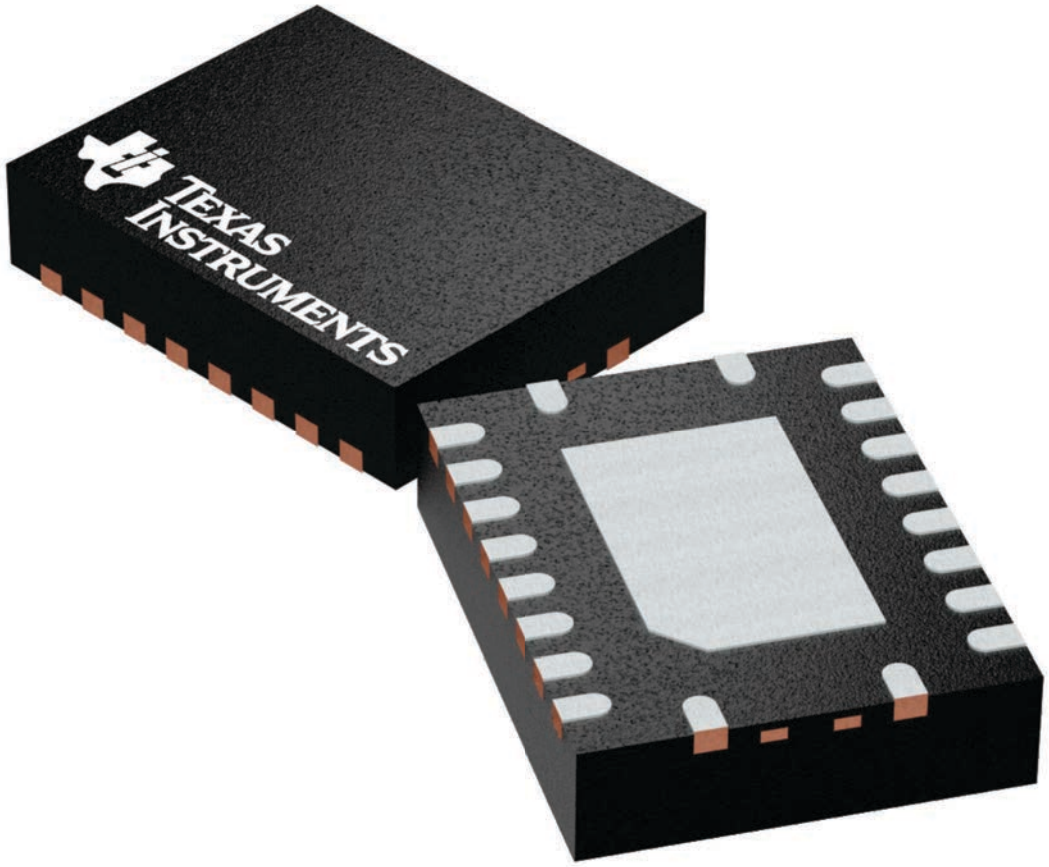
RGY 20

VQFN - 1 mm max height

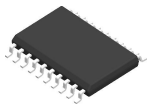
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225264/A

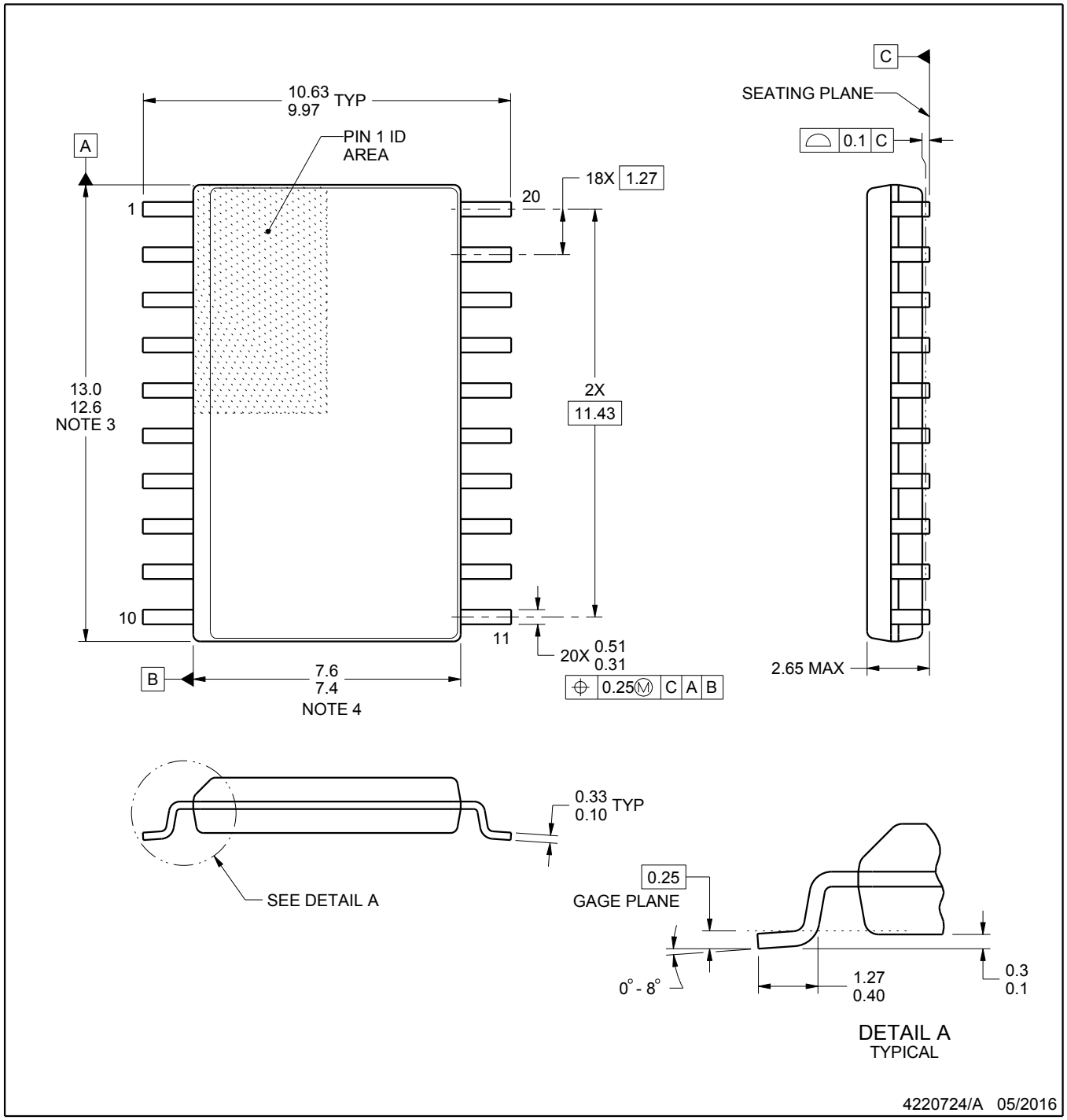


PACKAGE OUTLINE

DW0020A

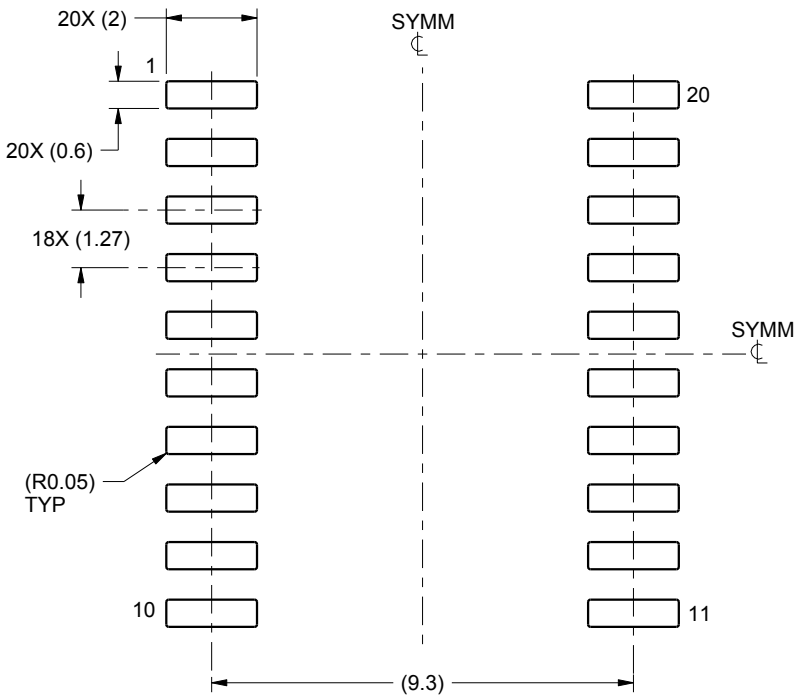
SOIC - 2.65 mm max height

SOIC

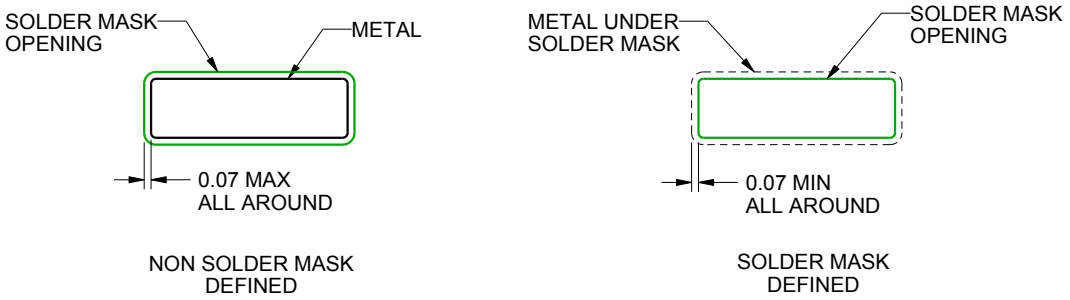


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

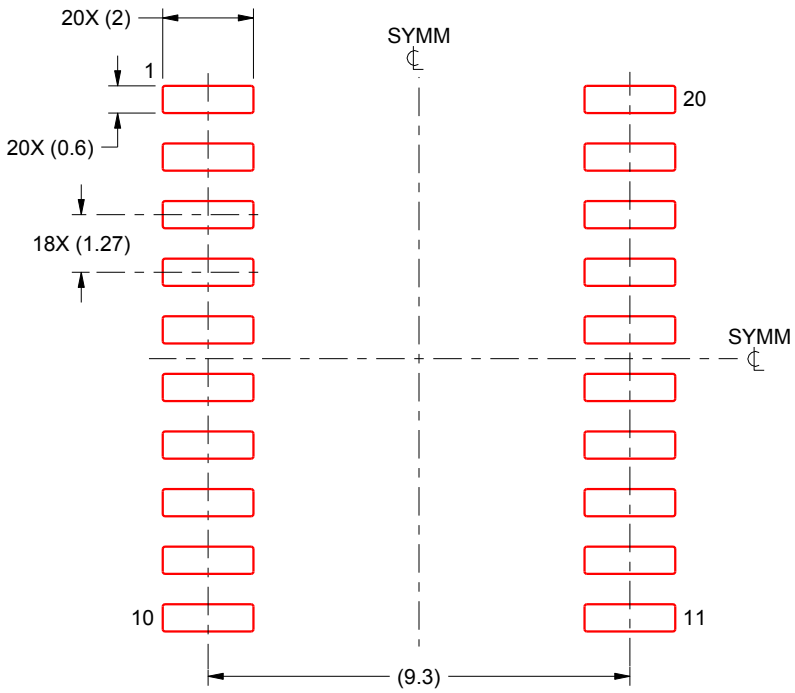


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

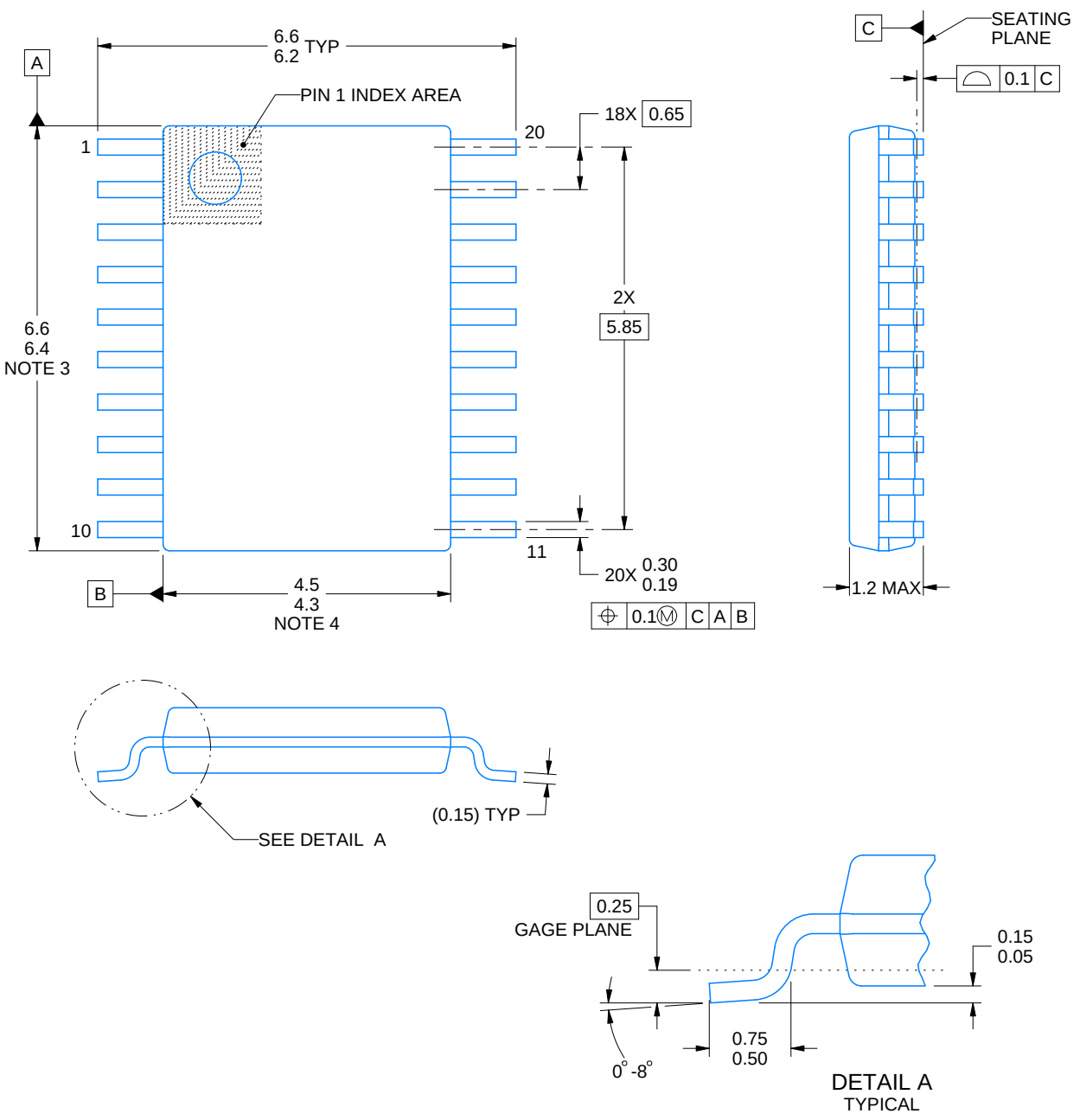
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0020A

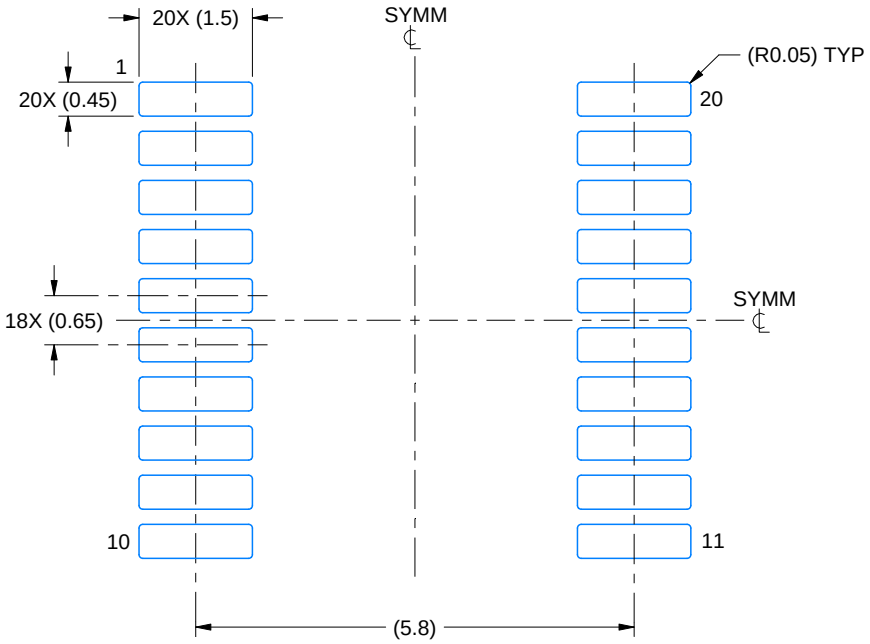
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

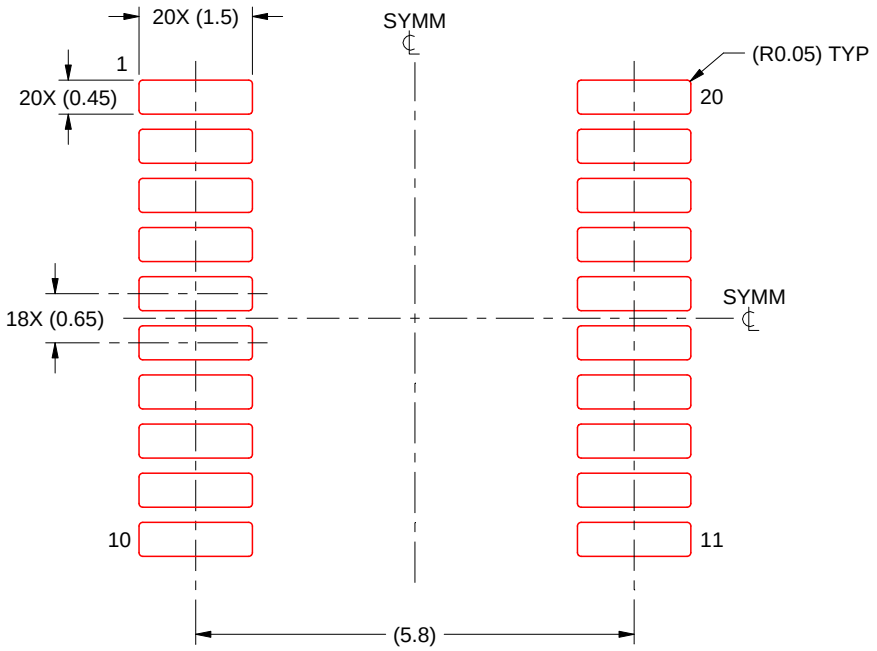


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

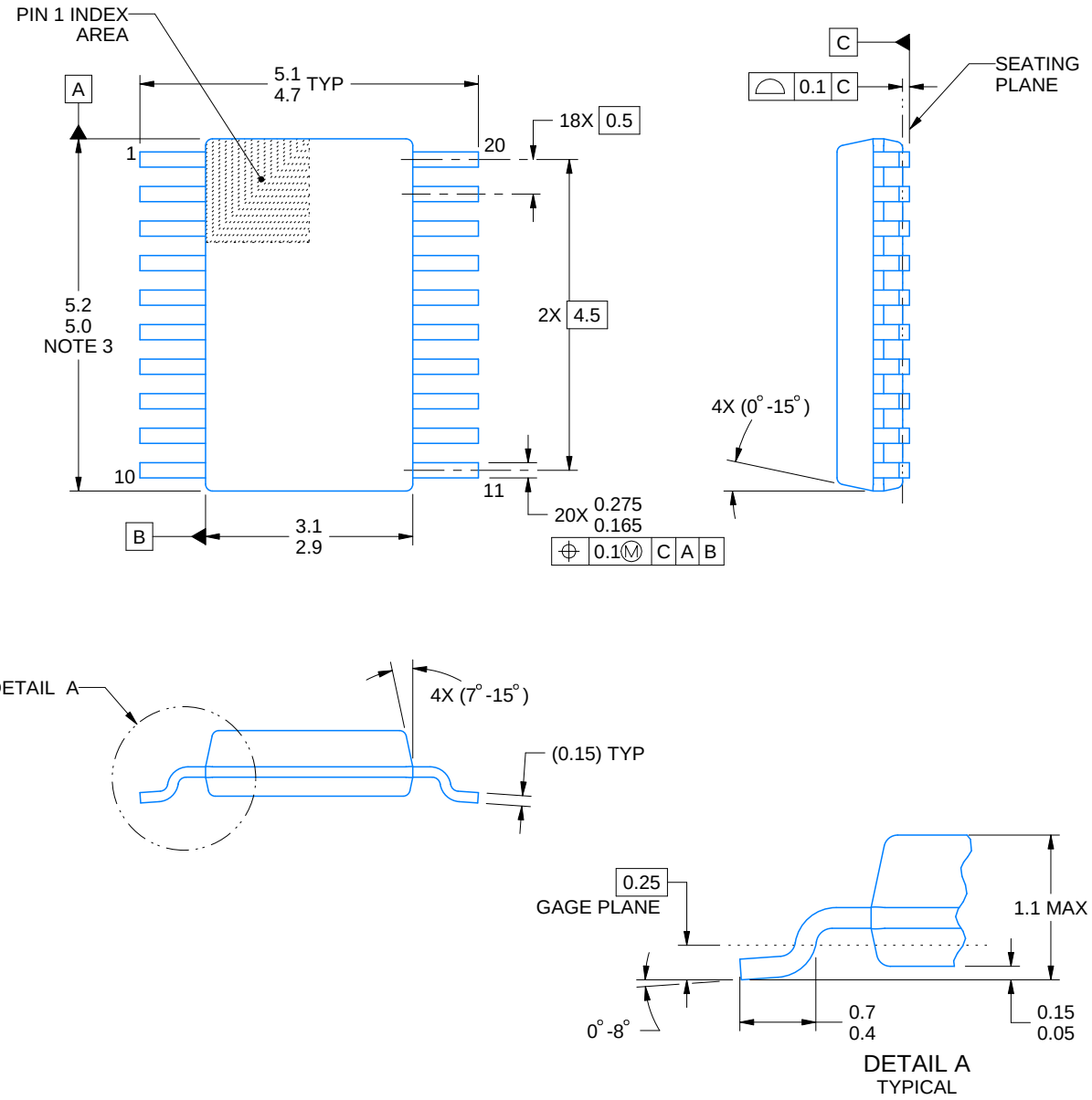
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0020A

VSSOP - 1.1 mm max height

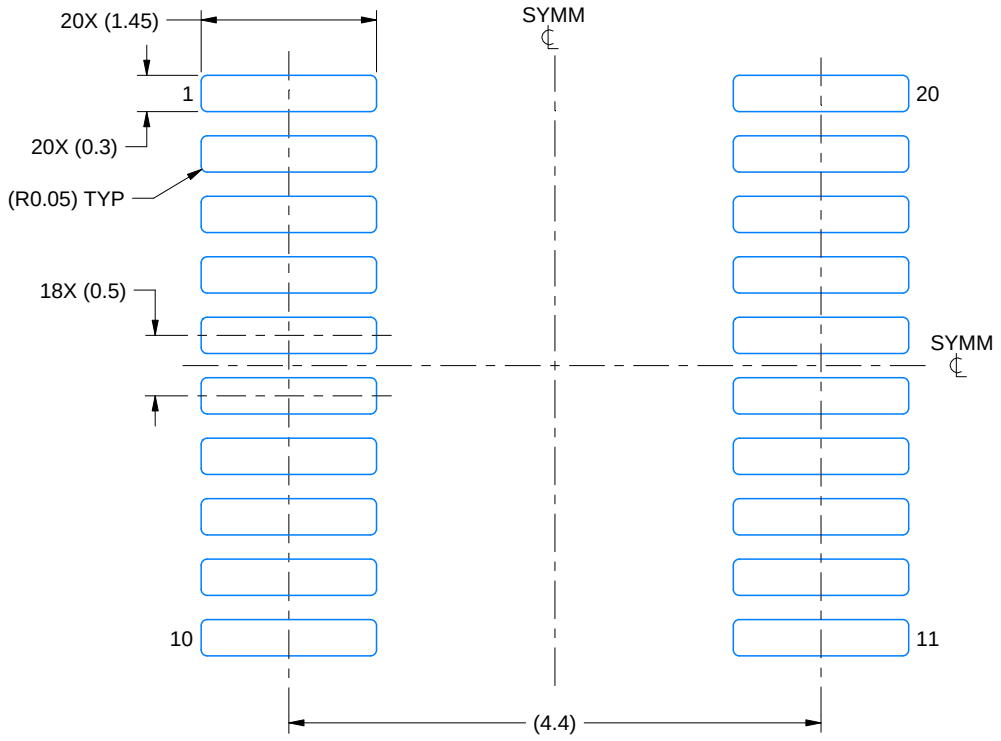
SMALL OUTLINE PACKAGE



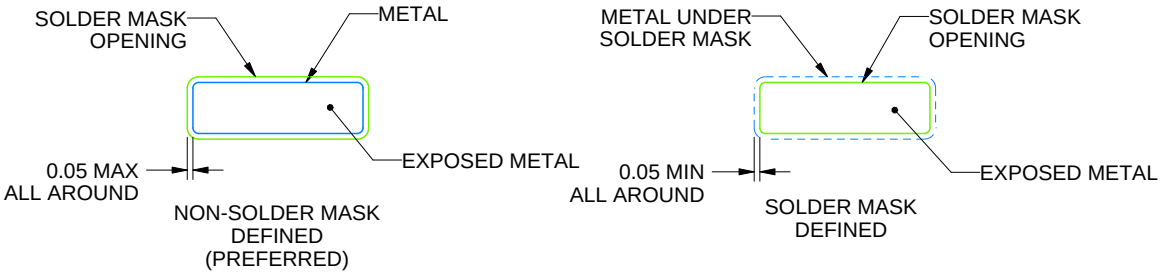
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X

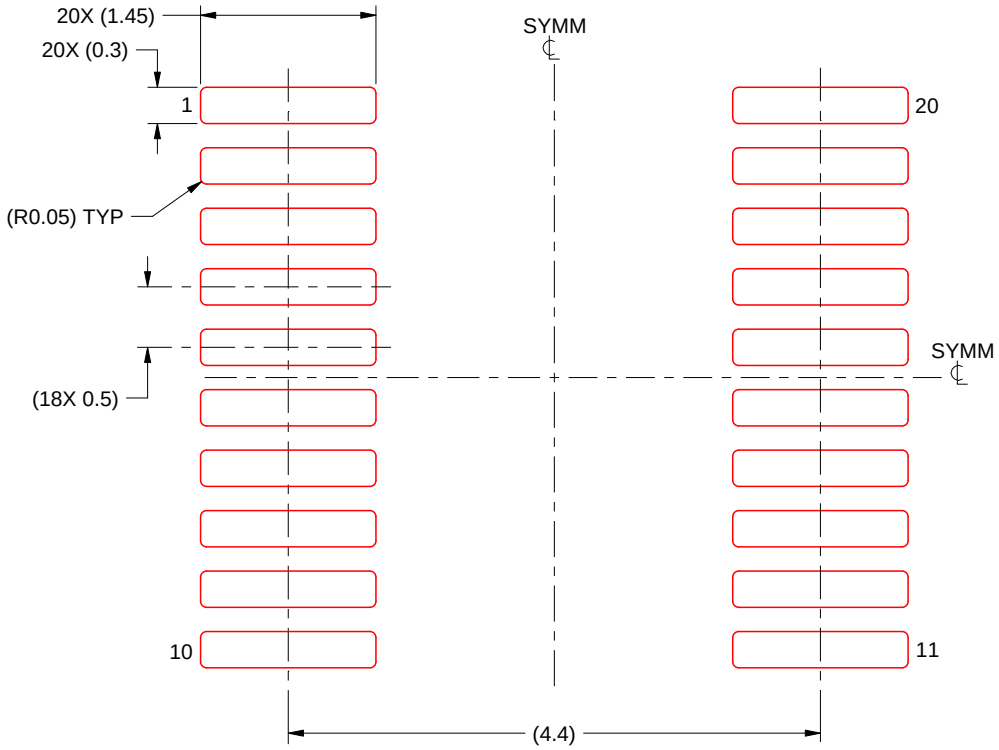


SOLDER MASK DETAILS

4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月