SN74LV393A-Q1 デュアル 4 ビット・バイナリ・カウンタ

1 特長

- 2V～5.5V の V_{CC} で動作
- 最大 t_{pd} 9.5ns (5V 時)
- 標準 V_{OLP} (出力グランド・バウンス) < 0.8V (V_{CC} = 3.3V、T_A = 25℃)
- 標準 V_{OHV} (出力 V_{OH} アンダーシュート) > 2.3V (V_{CC} = 3.3V、T_A = 25℃)
- すべてのポートで混在モード電圧動作をサポート
- I_{off} により部分的パワーダウン・モード動作をサポート
- JESD 17 準拠で 250mA 超のラッチアップ性能

2 アプリケーション

- 反転クロック入力の同期
- スイッチのデバウンス
- デジタル信号の反転

3 説明

LV393A デバイスには 8 つのフリップ・フロップと追加のゲート処理機能が搭載されており、2 つの独立した 4 ビット・カウンタを 1 つのパッケージに実装しています。これらのデバイスは、2V～5.5V の V_{CC} 動作用に設計されています。

パッケージ情報

部品番号	パッケージ(1)	本体サイズ (公称)
SN74LV393A-Q1	PW (TSSOP、14)	5mm × 4.4mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

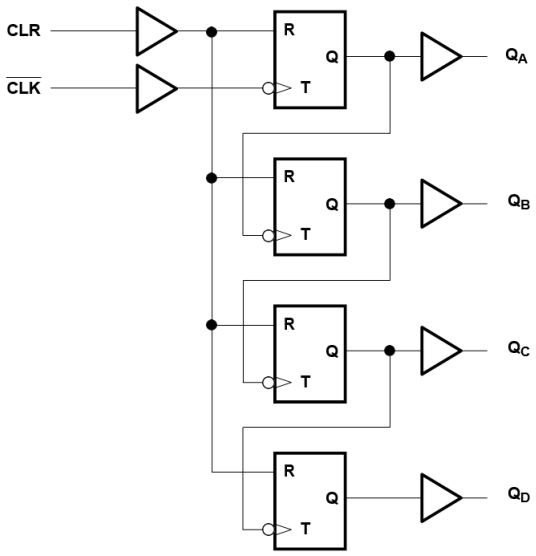


図 3-1. 各カウンタの論理図 (正論理)

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (February 2008) to Revision D (March 2023)	Page
• 「アプリケーション」セクション、「製品情報」表、「ピン機能」表、「ESD 定格」表、「熱に関する情報」表、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加.	1

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5 Pin Configuration and Functions

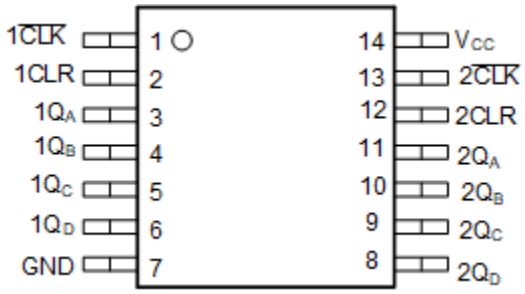


図 5-1. PW Package, 14-Pin TSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1$\overline{CLK}$	1	I	Counter 1 Clock Input
1CLR	2	I	Counter 1 Clear Input
$1Q_A$	3	O	Counter 1 A Output
$1Q_B$	4	O	Counter 1 B Output
$1Q_C$	5	O	Counter 1 B Output
$1Q_D$	6	O	Counter 1 B Output
GND	7	G	Ground
$2Q_D$	8	O	Counter 2 D Output
$2Q_C$	9	O	Counter 2 C Output
$2Q_B$	10	O	Counter 2 B Output
$2Q_A$	11	O	Counter 2 A Output
2CLR	12	I	Counter 2 Clear Input
2$\overline{CLK}$	13	I	Counter 2 Clock Input
V_{CC}	14	P	V_{CC}

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage(1)		–0.5	7	V
V_O	Output voltage range applied in high or low state(1) (2)		–0.5	V_{CC} + 0.5	V
V_O	Output voltage range applied in power-off state (1)		–0.5	7	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- This value is limited to 7 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (MIL-STD-883, Method 3015)(1)	±2000	V
		Machine Model (C = 200 pF, R = 0)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	µA
		V_{CC} = 2.3 V to 2.7 V		–2	mA
		V_{CC} = 3 V to 3.6 V		–6	
		V_{CC} = 4.5 V to 5.5 V		–12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		6	
		V_{CC} = 4.5 V to 5.5 V		12	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs.*

6.4 Thermal Information

THERMAL METRIC(1)		PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics.*

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –50 µA	2 V to 5.5 V	V_{CC} – 0.1			V
	I_{OH} = –2 mA	2.3 V	2			
	I_{OH} = –6 mA	3 V	2.48			
	I_{OH} = –12 mA	4.5 V	3.8			
V_{OL}	I_{OL} = 50 µA	2 V to 5.5 V			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4	
	I_{OL} = 6 mA	3 V			0.44	
	I_{OL} = 12 mA	4.5 V			0.55	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±1	µA
I_{cc}	V_I = V_{CC} or GND, I_O =0	5.5 V			20	µA
I_{off}	V_I or V_O = 0 to 5.5 V	0 V			5	µA
C_i	V_I = V_{CC} or GND	3.3 V		1.8		pF

6.6 Timing Requirements, V_{CC} = 2.5 V ± 0.2 V

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

			T_A = 25°C		SN74LV393A-Q1		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLK}$ high or low	5		5		ns
		CLR high	5		5		
t_{su}	Setup time	CLR inactive before CLK ↓	6		6		ns

6.7 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

			T_A = 25°C		SN74LV393A-Q1		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLK}$ high or low	5		5		ns
		CLR high	5		5		
t_{su}	Setup time	CLR inactive before CLK ↓	5		5		ns

6.8 Timing Requirements, V_{CC} = 5 V ± 0.5 V

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

			T_A = 25°C		SN74LV393A-Q1		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLK}$ high or low	5		5		ns
		CLR high	5		5		
t_{su}	Setup time	CLR inactive before CLK ↓	4		4		ns

6.9 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TA = 25°C			SN74LV393A-Q1		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			C_L = 50 pF	30	70		25		MHz

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6.9 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V (continued)

over operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TA = 25°C			SN74LV393A-Q1		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	$\overline{CLK}$	Q_A	C_L = 50 pF		9.3[1]	21.3[1]	1	24.5	ns
		Q_B			10.9[1]	23.9[1]	1	27.5	
		Q_C			12.3[1]	26.1[1]	1	30	
		Q_D			13.4[1]	27.8[1]	1	32	
t_{PHL}	CLR	Q_n			9.1[1]	17.4[1]	1	20	

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.10 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TA = 25°C			SN74LV393A-Q1		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			C_L = 50 pF	45	105		35		MHz
t_{pd}	$\overline{CLK}$	Q_A	C_L = 50 pF		6.7[1]	16.7[1]	1	19	ns
		Q_B			7.8[1]	19.3[1]	1	22	
		Q_C			8.7[1]	21.5[1]	1	24.5	
		Q_D			9.5[1]	23.2[1]	1	26.5	
t_{PHL}	CLR	Q_n			6.8[1]	15.8[1]	1	18	

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.11 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TA = 25°C			SN74LV393A-Q1		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			C_L = 50 pF	85	150		75		MHz
t_{pd}	$\overline{CLK}$	Q_A	C_L = 50 pF		4.9[1]	10.5[1]	1	12	ns
		Q_B			5.6[1]	11.8[1]	1	13.5	
		Q_C			6.2[1]	13.2[1]	1	15	
		Q_D			6.6[1]	14.5[1]	1	16.5	
t_{PHL}	CLR	Q_n			5.2[1]	10.1[1]	1	11.5	

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.12 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

PARAMETER[(1)]		SN74LV393A-Q1			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		− 0.2	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.8		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics for surface-mount packages only.

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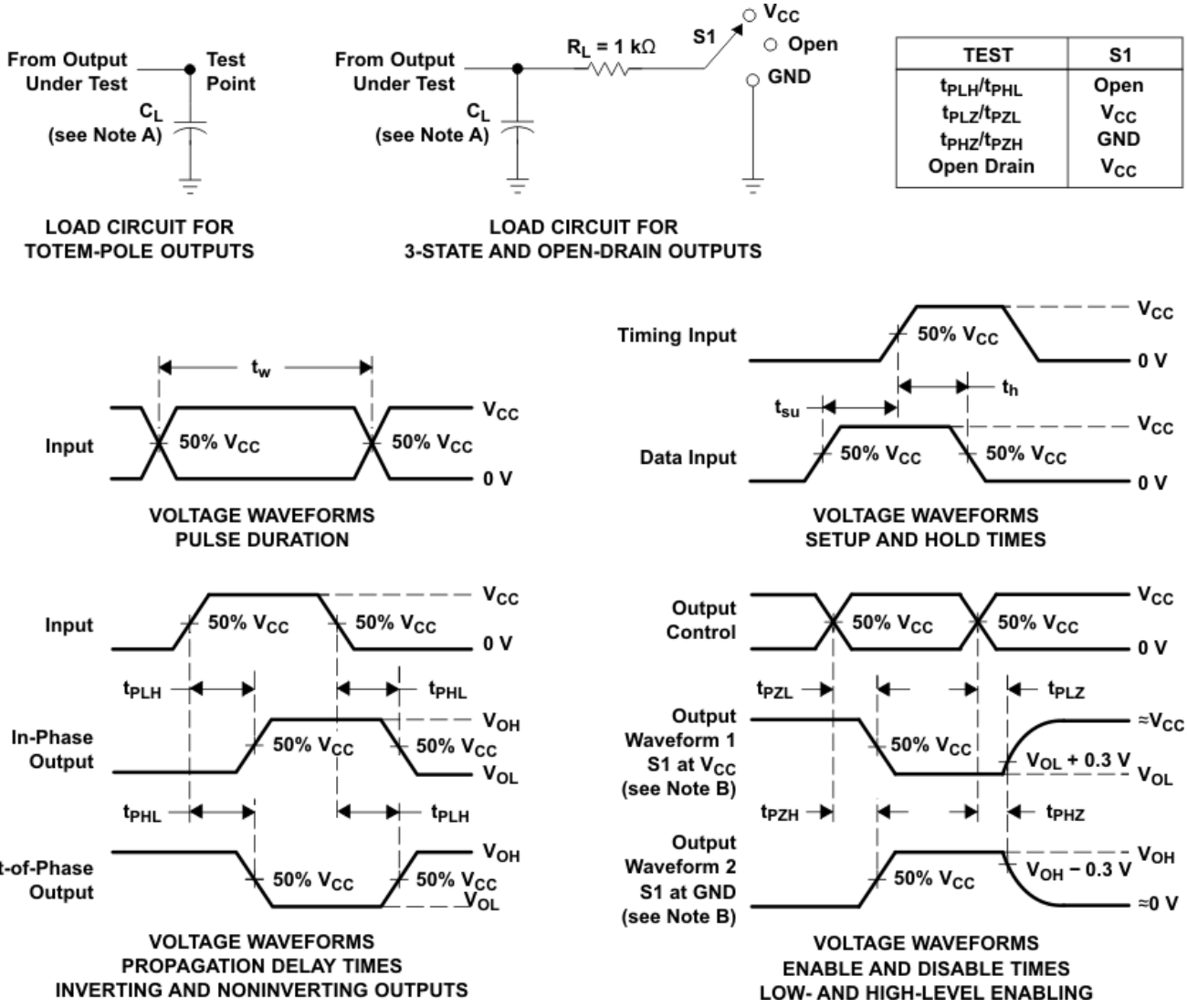
6.13 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V	15.2	pF
			5 V	17.3	

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7 Parameter Measurement Information



A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, and t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

図 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

These devices comprise two independent 4-bit binary counters, each having a clear (CLR) and a clock ($\overline{CLK}$) input. These devices change state on the negative-going transition of the $\overline{CLK}$ pulse. N-bit binary counters can be implemented with each package, providing the capability of divide by 256. The ’LV393A devices have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system timing signals.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

8.2 Functional Block Diagram

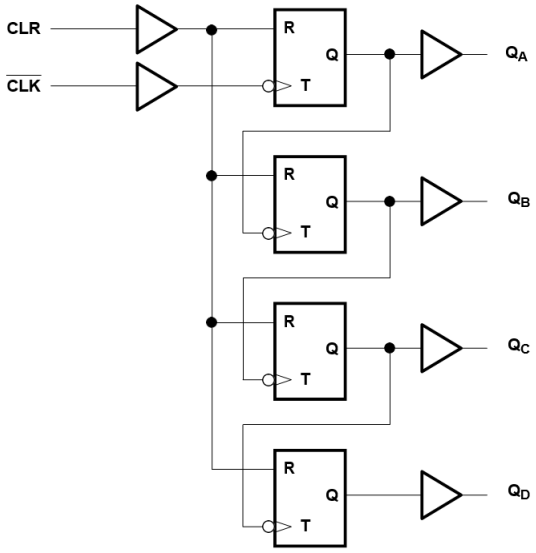


図 8-1. Logic Diagram, Each Counter (Positive Logic)

8.3 Device Functional Modes

表 8-1. Function Table

INPUTS		FUNCTION
$\overline{CLK}$	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

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9 Application and Implementation

注

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9.1 Power Supply Recommendations

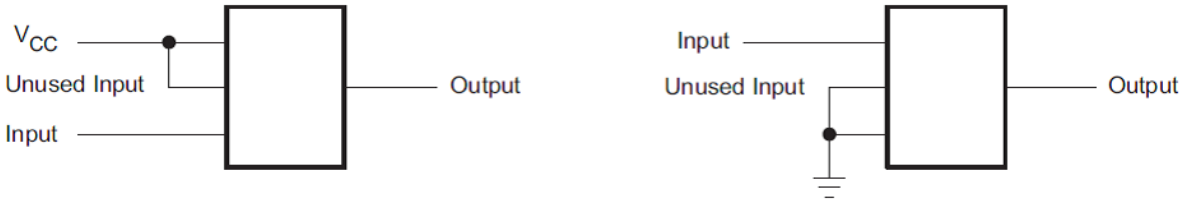
The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* section. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor; if there are multiple V_{CC} terminals, then TI recommends a 0.01-µF or 0.022-µF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

9.2 Layout

9.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

9.2.1.1 Layout Example



10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Device Support

10.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV393A-Q1	Click here	Click here	Click here	Click here	Click here

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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10.4 Trademarks

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10.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV393ATPWRG4Q1	NRND	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LV393AT
SN74LV393ATPWRG4Q1.A	NRND	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LV393AT
SN74LV393ATPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 105	LV393AT
SN74LV393ATPWRQ1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LV393AT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV393A-Q1 :

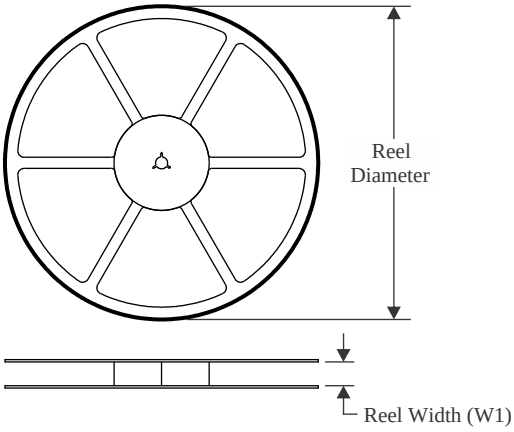
- Catalog : SN74LV393A
- Enhanced Product : SN74LV393A-EP

NOTE: Qualified Version Definitions:

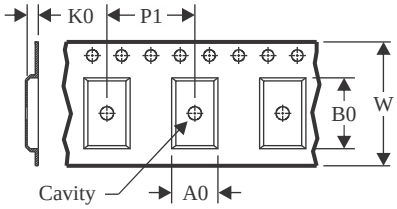
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

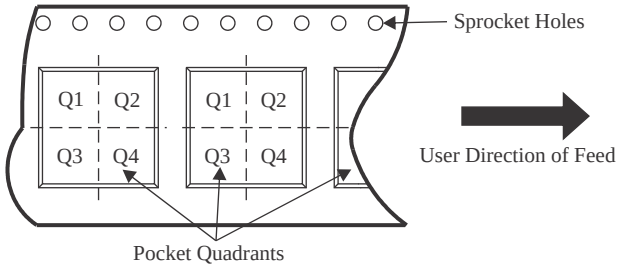


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

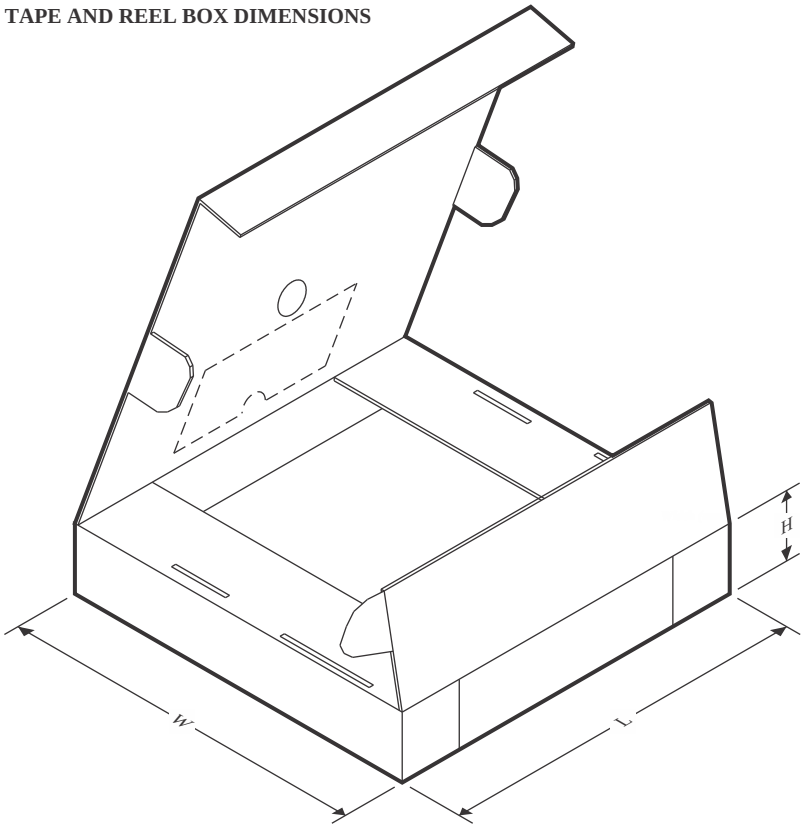
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV393ATPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV393ATPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV393ATPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV393ATPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

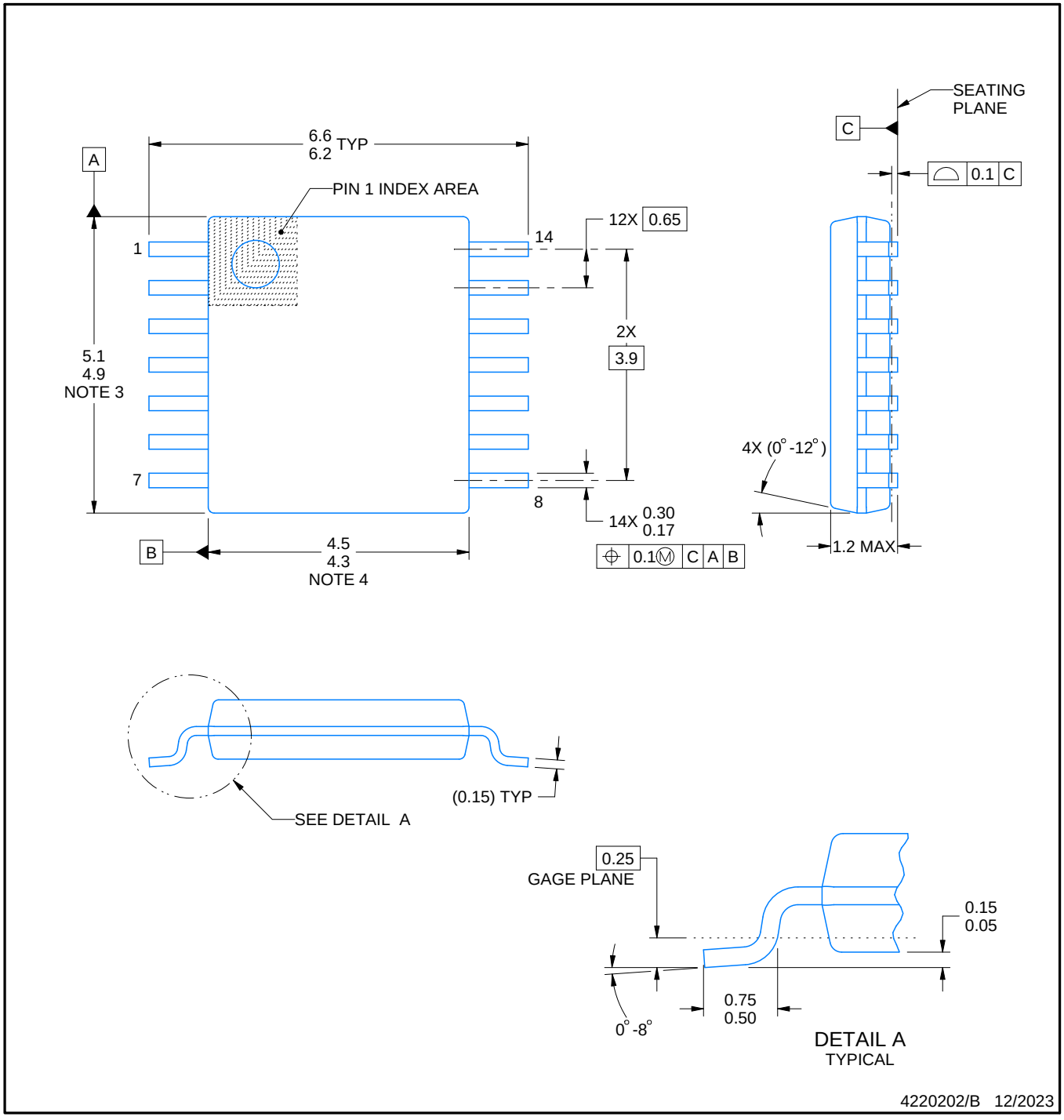
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV393ATPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LV393ATPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV393ATPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LV393ATPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0014A

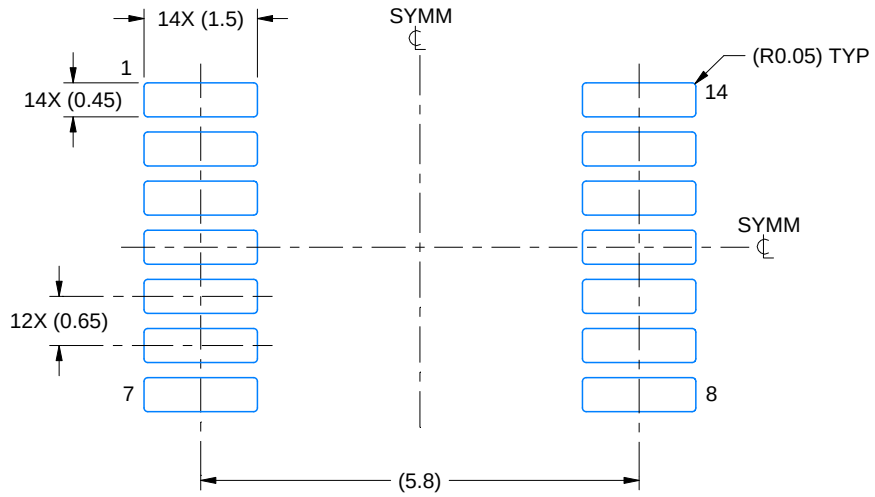
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

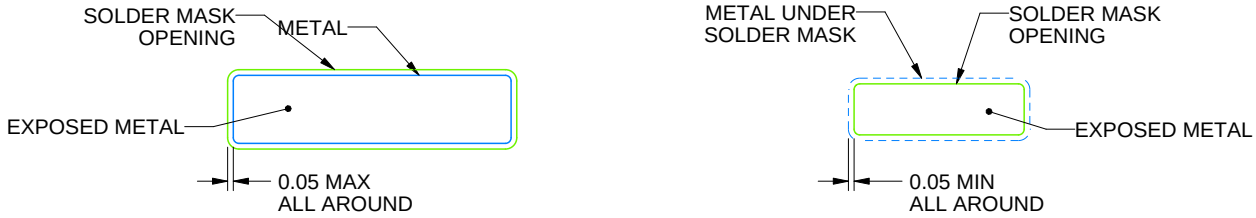


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

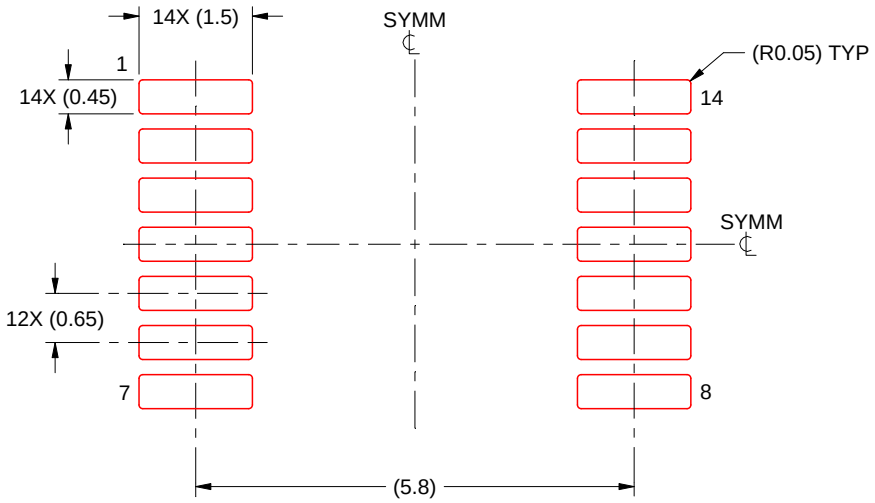


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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