

# SNx4LV4053A トリプル 2 チャネル アナログ マルチプレクサ / デマルチプレクサ

## 1 特長

- 1.65V～5.5V の  $V_{CC}$  で動作
- すべてのポートで混在モード電圧動作をサポート
- 高いオン / オフ出力電圧比
- スイッチ間の低いクロストーク
- スイッチの個別制御
- 非常に低い入力電流
- JESD 17 準拠  
250mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護
  - 2000V、人体モデル (A114-A)
  - 1000V、デバイス帯電モデル (C101)

## 2 アプリケーション

- [テレコミュニケーション](#)
- [インフォテインメント](#)
- 信号のゲーティングと絶縁
- [家電製品](#)
- プログラマブル ロジック回路
- 変調および復調

## 3 概要

これらのトリプル 2 チャネル CMOS アナログ マルチプレクサ / デマルチプレクサは、1.65V ～ 5.5V の  $V_{CC}$  で動作するように設計されています。

SNx4LV4053A は、アナログとデジタルの両方の信号を扱います。各チャネルは、最大 5.5V (ピーク) までの振幅の信号をどちらの方向にも伝送できます。

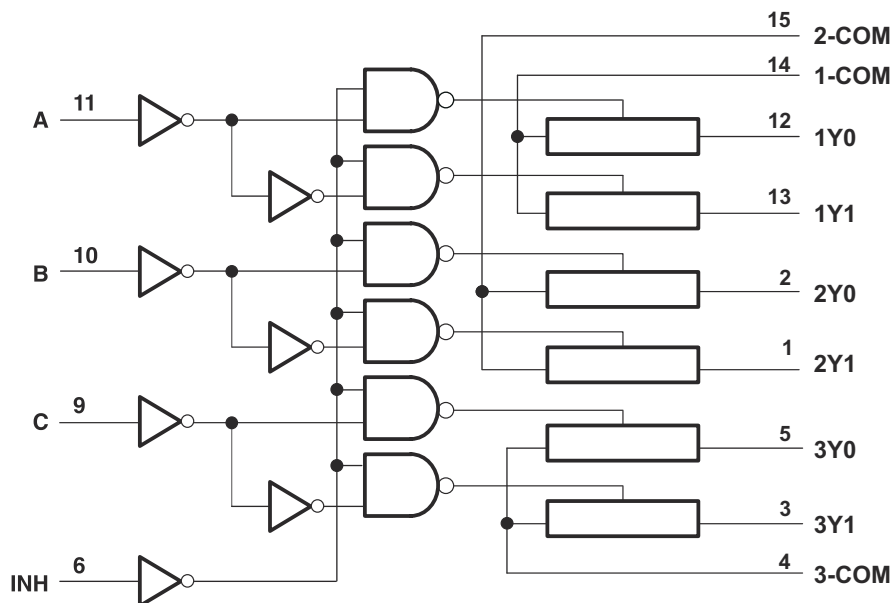
信号ゲーティング、チョッピング、変調または復調 (モデム)、およびアナログ / デジタルやデジタル / アナログ変換システム用の信号多重化などのアプリケーションに使用できます。

### パッケージ情報

| 部品番号        | パッケージ <sup>(1)</sup>  | パッケージサイズ <sup>(2)</sup> |
|-------------|-----------------------|-------------------------|
| SNx4LV4053A | D (SOIC, 16)          | 9.9mm × 6 mm            |
|             | PW (TSSOP, 16)        | 5mm × 6.4 mm            |
|             | RGY (VQFN, 16)        | 4mm × 3.5 mm            |
|             | DYY (SOT-23-THIN, 16) | 4.2 mm × 3.26mm         |

(1) 詳細については、[セクション 11](#) を参照してください。

(2) パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



機能ブロック図



## Table of Contents

|                                                                           |           |                                                                  |           |
|---------------------------------------------------------------------------|-----------|------------------------------------------------------------------|-----------|
| <b>1 特長</b> .....                                                         | <b>1</b>  | 7.1 Functional Block Diagram.....                                | <b>14</b> |
| <b>2 アプリケーション</b> .....                                                   | <b>1</b>  | 7.2 Device Functional Modes.....                                 | <b>14</b> |
| <b>3 概要</b> .....                                                         | <b>1</b>  | <b>8 Application and Implementation</b> .....                    | <b>15</b> |
| <b>4 Pin Configuration and Functions</b> .....                            | <b>3</b>  | 8.1 Application Information.....                                 | <b>15</b> |
| <b>5 Specifications</b> .....                                             | <b>4</b>  | 8.2 Typical Application.....                                     | <b>15</b> |
| 5.1 Absolute Maximum Ratings.....                                         | <b>4</b>  | 8.3 Power Supply Recommendations.....                            | <b>15</b> |
| 5.2 ESD Ratings.....                                                      | <b>4</b>  | 8.4 Layout.....                                                  | <b>15</b> |
| 5.3 Thermal Information: SN74LV4053A.....                                 | <b>4</b>  | <b>9 Device and Documentation Support</b> .....                  | <b>17</b> |
| 5.4 Recommended Operating Conditions.....                                 | <b>5</b>  | 9.1 ドキュメントの更新通知を受け取る方法.....                                      | <b>17</b> |
| 5.5 Electrical Characteristics.....                                       | <b>5</b>  | 9.2 サポート・リソース.....                                               | <b>17</b> |
| 5.6 Timing Characteristics $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ ..... | <b>7</b>  | 9.3 Trademarks.....                                              | <b>17</b> |
| 5.7 Timing Characteristics $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ..... | <b>7</b>  | 9.4 静電気放電に関する注意事項.....                                           | <b>17</b> |
| 5.8 Timing Characteristics $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .....   | <b>8</b>  | 9.5 用語集.....                                                     | <b>17</b> |
| 5.9 AC Characteristics.....                                               | <b>8</b>  | <b>10 Revision History</b> .....                                 | <b>17</b> |
| <b>6 Parameter Measurement Information</b> .....                          | <b>10</b> | <b>11 Mechanical, Packaging, and Orderable Information</b> ..... | <b>18</b> |
| <b>7 Detailed Description</b> .....                                       | <b>14</b> |                                                                  |           |

## 4 Pin Configuration and Functions

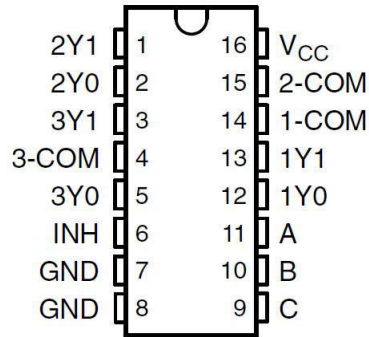


図 4-1. SN74LV4053A D, PW or DYY Packages, 16-Pin SOIC, TSSOP or SOT-23-THIN (Top View)

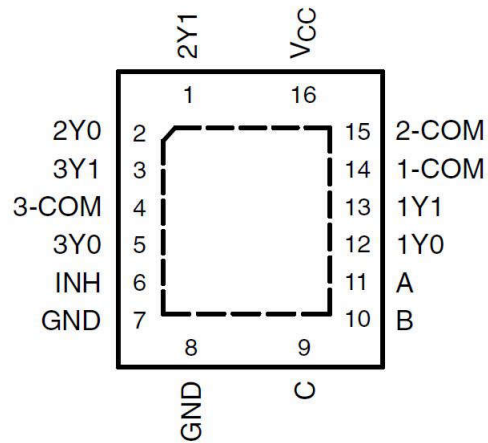


図 4-2. SN74LV4053A RGY, 16-Pin VQFN (Top View)

表 4-1. Pin Functions

| PIN             |     | TYPE <sup>(2)</sup> | DESCRIPTION                                                                                                 |
|-----------------|-----|---------------------|-------------------------------------------------------------------------------------------------------------|
| NAME            | NO. |                     |                                                                                                             |
| 2Y1             | 1   | I <sup>(1)</sup>    | Input to mux 2                                                                                              |
| 2Y0             | 2   | I <sup>(1)</sup>    | Input to mux 2                                                                                              |
| 3Y1             | 3   | I <sup>(1)</sup>    | Input to mux 3                                                                                              |
| 3-COM           | 4   | O <sup>(1)</sup>    | Output of mux 3                                                                                             |
| 3Y0             | 5   | I <sup>(1)</sup>    | Input to mux 3                                                                                              |
| INH             | 6   | I                   | Enables the outputs of the device. Logic low level with turn the outputs on, high level will turn them off. |
| GND             | 7   | -                   | Ground                                                                                                      |
| GND             | 8   | -                   | Ground                                                                                                      |
| C               | 9   | I                   | Selector line for outputs (see セクション 7.2 for specific information)                                          |
| B               | 10  | I                   | Selector line for outputs (see セクション 7.2 for specific information)                                          |
| A               | 11  | I                   | Selector line for outputs (see セクション 7.2 for specific information)                                          |
| 1Y0             | 12  | I <sup>(1)</sup>    | Input to mux 1                                                                                              |
| 1Y1             | 13  | I <sup>(1)</sup>    | Input to mux 1                                                                                              |
| 1-COM           | 14  | O <sup>(1)</sup>    | Output of mux 1                                                                                             |
| 2-COM           | 15  | O <sup>(1)</sup>    | Output of mux 2                                                                                             |
| V <sub>CC</sub> | 16  | I                   | Device power input                                                                                          |

- (1) These I/O descriptions represent the device when used as a multiplexer, when this device is operated as a demultiplexer pins 1Y0, 1Y1, 2Y0, 2Y1, 3Y0, 3Y1 may be considered outputs (O) and pins 1-COM, 2-COM, and 3-COM may be considered inputs (I).
- (2) I = input, O = output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (3)</sup>

|           |                                             |                                   | MIN  | MAX            | UNIT |
|-----------|---------------------------------------------|-----------------------------------|------|----------------|------|
| $V_{CC}$  | Supply voltage                              |                                   | –0.5 | 7.0            | V    |
| $V_I$     | Logic input voltage range                   |                                   | –0.5 | 7.0            | V    |
| $V_{IO}$  | Switch I/O voltage range <sup>(2) (3)</sup> |                                   | –0.5 | $V_{CC} + 0.5$ | V    |
| $I_{IK}$  | Input clamp current                         | $V_I < 0$                         | –20  |                | mA   |
| $I_{IOK}$ | Switch IO diode clamp current               | $V_{IO} < 0$ or $V_{IO} > V_{CC}$ | –50  | 50             | mA   |
| $I_T$     | Switch continuous current                   | $V_{IO} = 0$ to $V_{CC}$          |      | ±25            | mA   |
|           | Continuous current through $V_{CC}$ or GND  |                                   |      | ±50            | mA   |
| $T_J$     | Junction temperature                        |                                   |      | 150            | °C   |
| $T_{stg}$ | Storage temperature                         |                                   | –65  | 150            | °C   |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
- (3) This value is limited to 5.5 V maximum

### 5.2 ESD Ratings

|             |                         |                                                                                          | VALUE | UNIT |
|-------------|-------------------------|------------------------------------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins <sup>(1)</sup>             | ±2000 | V    |
|             |                         | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | ±1000 |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Thermal Information: SN74LV4053A

| THERMAL METRIC <sup>(1)</sup> |                                              | SN74LV4053A |            |            |           | UNIT |
|-------------------------------|----------------------------------------------|-------------|------------|------------|-----------|------|
|                               |                                              | D (SOIC)    | PW (TSSOP) | RGY (VQFN) | DYY (SOT) |      |
|                               |                                              | 16 PINS     | 16 PINS    | 16 PINS    | 16 PINS   |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 115.2       | 140.2      | 89.4       | 199.7     | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 75.0        | 72.6       | 89.7       | 121.2     | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 76.6        | 98.7       | 65.4       | 129.0     | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 31.3        | 13.4       | 25.0       | 24.6      | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 75.7        | 97.3       | 65.2       | 126.7     | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | N/A         | N/A        | 48.9       | N/A       | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                                   |                                  | MIN                   | NOM                   | MAX             | UNIT |
|-----------------|---------------------------------------------------|----------------------------------|-----------------------|-----------------------|-----------------|------|
| V <sub>CC</sub> | Supply voltage                                    |                                  | 1 <sup>(2)</sup>      |                       | 5.5             | V    |
| V <sub>IH</sub> | High-level input voltage,<br>logic control inputs | V <sub>CC</sub> = 1.65           | 1.2                   |                       | 5.5             | V    |
|                 |                                                   | V <sub>CC</sub> = 2 V            | 1.5                   |                       | 5.5             |      |
|                 |                                                   | V <sub>CC</sub> = 2.3 V to 2.7 V | V <sub>CC</sub> × 0.7 |                       | 5.5             |      |
|                 |                                                   | V <sub>CC</sub> = 3 V to 3.6 V   | V <sub>CC</sub> × 0.7 |                       | 5.5             |      |
|                 |                                                   | V <sub>CC</sub> = 4.5 V to 5.5 V | V <sub>CC</sub> × 0.7 |                       | 5.5             |      |
| V <sub>IL</sub> | Low-level input voltage,<br>logic control inputs  | V <sub>CC</sub> = 1.65           | 0                     |                       | 0.4             | V    |
|                 |                                                   | V <sub>CC</sub> = 2 V            | 0                     |                       | 0.5             |      |
|                 |                                                   | V <sub>CC</sub> = 2.3 V to 2.7 V | 0                     | V <sub>CC</sub> × 0.3 |                 |      |
|                 |                                                   | V <sub>CC</sub> = 3 V to 3.6 V   | 0                     | V <sub>CC</sub> × 0.3 |                 |      |
|                 |                                                   | V <sub>CC</sub> = 4.5 V to 5.5 V | 0                     | V <sub>CC</sub> × 0.3 |                 |      |
| V <sub>I</sub>  | Logic control input voltage                       |                                  | 0                     |                       | 5.5             | V    |
| V <sub>IO</sub> | Switch input or output voltage                    |                                  | 0                     |                       | V <sub>CC</sub> | V    |
| Δt/ΔV           | Logic input transition rise or fall rate          | V <sub>CC</sub> = 2.3 V to 2.7 V |                       |                       | 200             | ns/V |
|                 |                                                   | V <sub>CC</sub> = 3 V to 3.6 V   |                       |                       | 100             |      |
|                 |                                                   | V <sub>CC</sub> = 4.5 V to 5.5 V |                       |                       | 20              |      |
| T <sub>A</sub>  | Ambient temperature                               |                                  | –40                   |                       | 125             | °C   |

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, SCBA004.
- (2) When using a V<sub>CC</sub> of ≤1.2 V, it is recommended to use these devices only for transmitting digital signals. When supply voltage is near 1.2 V the analog switch ON resistance becomes very non-linear

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER          | Condition                                                                                                                              | T <sub>A</sub> | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|--------------------|----------------------------------------------------------------------------------------------------------------------------------------|----------------|-----------------|-----|-----|-----|------|
| r <sub>ON</sub>    | ON-state switch resistance<br>I <sub>T</sub> = 2 mA,<br>V <sub>I</sub> = V <sub>CC</sub> or GND,<br>V <sub>INH</sub> = V <sub>IL</sub> | 25°C           | 1.65 V          |     | 60  | 150 | Ω    |
| r <sub>ON</sub>    | ON-state switch resistance<br>I <sub>T</sub> = 2 mA,<br>V <sub>I</sub> = V <sub>CC</sub> or GND,<br>V <sub>INH</sub> = V <sub>IL</sub> | –40°C to 85°C  | 1.65 V          |     |     | 225 | Ω    |
| r <sub>ON</sub>    | ON-state switch resistance<br>I <sub>T</sub> = 2 mA,<br>V <sub>I</sub> = V <sub>CC</sub> or GND,<br>V <sub>INH</sub> = V <sub>IL</sub> | –40°C to 125°C | 1.65 V          |     |     | 225 | Ω    |
| r <sub>ON</sub>    | ON-state switch resistance<br>I <sub>T</sub> = 2 mA,<br>V <sub>I</sub> = V <sub>CC</sub> or GND,<br>V <sub>INH</sub> = V <sub>IL</sub> | 25°C           | 2.3 V           |     | 38  | 180 | Ω    |
|                    |                                                                                                                                        | –40°C to 85°C  |                 |     |     | 225 |      |
|                    |                                                                                                                                        | –40°C to 125°C |                 |     |     | 225 |      |
|                    |                                                                                                                                        | 25°C           | 3 V             |     | 30  | 150 | Ω    |
|                    |                                                                                                                                        | –40°C to 85°C  |                 |     |     | 190 |      |
|                    |                                                                                                                                        | –40°C to 125°C |                 |     |     | 190 |      |
|                    |                                                                                                                                        | 25°C           | 4.5 V           |     | 22  | 75  | Ω    |
|                    |                                                                                                                                        | –40°C to 85°C  |                 |     |     | 100 |      |
|                    |                                                                                                                                        | –40°C to 125°C |                 |     |     | 100 |      |
| r <sub>ON(p)</sub> | Peak ON-state resistance<br>I <sub>T</sub> = 2 mA,<br>V <sub>I</sub> = GND to V <sub>CC</sub> ,<br>V <sub>INH</sub> = V <sub>IL</sub>  | 25°C           | 1.65 V          |     | 220 | 600 | Ω    |

## 5.5 Electrical Characteristics (続き)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                          |                                                    | Condition                                                                                                                                                          | T <sub>A</sub> | V <sub>CC</sub> | MIN | TYP  | MAX | UNIT |
|------------------------------------|----------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|-----------------|-----|------|-----|------|
| r <sub>ON(p)</sub>                 | Peak ON-state resistance                           | I <sub>T</sub> = 2 mA,<br>V <sub>I</sub> = GND to V <sub>CC</sub> ,<br>V <sub>INH</sub> = V <sub>IL</sub>                                                          | –40°C to 85°C  | 1.65 V          |     |      | 700 | Ω    |
| r <sub>ON(p)</sub>                 | Peak ON-state resistance                           | I <sub>T</sub> = 2 mA,<br>V <sub>I</sub> = GND to V <sub>CC</sub> ,<br>V <sub>INH</sub> = V <sub>IL</sub>                                                          | –40°C to 125°C | 1.65 V          |     |      | 700 | Ω    |
| r <sub>ON(p)</sub>                 | Peak ON-state resistance                           | I <sub>T</sub> = 2 mA,<br>V <sub>I</sub> = GND to V <sub>CC</sub> ,<br>V <sub>INH</sub> = V <sub>IL</sub>                                                          | 25°C           | 2.3 V           |     | 113  | 500 | Ω    |
|                                    |                                                    |                                                                                                                                                                    | –40°C to 85°C  |                 |     |      | 600 |      |
|                                    |                                                    |                                                                                                                                                                    | –40°C to 125°C |                 |     |      | 600 |      |
|                                    |                                                    |                                                                                                                                                                    | 25°C           | 3 V             |     | 54   | 180 | Ω    |
|                                    |                                                    |                                                                                                                                                                    | –40°C to 85°C  |                 |     |      | 225 |      |
|                                    |                                                    |                                                                                                                                                                    | –40°C to 125°C |                 |     |      | 225 |      |
|                                    |                                                    |                                                                                                                                                                    | 25°C           | 4.5 V           |     | 31   | 100 | Ω    |
|                                    |                                                    |                                                                                                                                                                    | –40°C to 85°C  |                 |     |      | 125 |      |
|                                    |                                                    |                                                                                                                                                                    | –40°C to 125°C |                 |     |      | 125 |      |
| Δr <sub>ON</sub>                   | Difference in ON-state resistance between switches | I <sub>T</sub> = 2 mA,<br>V <sub>I</sub> = GND to V <sub>CC</sub> ,<br>V <sub>INH</sub> = V <sub>IL</sub>                                                          | 25°C           | 1.65 V          |     | 3    | 40  | Ω    |
| Δr <sub>ON</sub>                   | Difference in ON-state resistance between switches | I <sub>T</sub> = 2 mA,<br>V <sub>I</sub> = GND to V <sub>CC</sub> ,<br>V <sub>INH</sub> = V <sub>IL</sub>                                                          | –40°C to 85°C  | 1.65 V          |     |      | 50  | Ω    |
| Δr <sub>ON</sub>                   | Difference in ON-state resistance between switches | I <sub>T</sub> = 2 mA,<br>V <sub>I</sub> = GND to V <sub>CC</sub> ,<br>V <sub>INH</sub> = V <sub>IL</sub>                                                          | –40°C to 85°C  | 1.65 V          |     |      | 50  | Ω    |
| Δr <sub>ON</sub>                   | Difference in ON-state resistance between switches | I <sub>T</sub> = 2 mA,<br>V <sub>I</sub> = GND to V <sub>CC</sub> ,<br>V <sub>INH</sub> = V <sub>IL</sub>                                                          | 25°C           | 2.3 V           |     | 2.1  | 30  | Ω    |
|                                    |                                                    |                                                                                                                                                                    | –40°C to 85°C  |                 |     |      | 40  |      |
|                                    |                                                    |                                                                                                                                                                    | –40°C to 125°C |                 |     |      | 40  |      |
|                                    |                                                    |                                                                                                                                                                    | 25°C           | 3 V             |     | 1.4  | 20  | Ω    |
|                                    |                                                    |                                                                                                                                                                    | –40°C to 85°C  |                 |     |      | 30  |      |
|                                    |                                                    |                                                                                                                                                                    | –40°C to 125°C |                 |     |      | 30  |      |
|                                    |                                                    |                                                                                                                                                                    | 25°C           | 4.5 V           |     | 1.3  | 15  | Ω    |
|                                    |                                                    |                                                                                                                                                                    | –40°C to 85°C  |                 |     |      | 20  |      |
|                                    |                                                    |                                                                                                                                                                    | –40°C to 125°C |                 |     |      | 20  |      |
| I <sub>IH</sub><br>I <sub>IL</sub> | Control input current                              | V <sub>I</sub> = 5.5 V or GND                                                                                                                                      | 25°C           | 0 to 5.5 V      |     |      | 0.1 | μA   |
|                                    |                                                    |                                                                                                                                                                    | –40°C to 85°C  |                 |     |      | 1   |      |
|                                    |                                                    |                                                                                                                                                                    | –40°C to 125°C |                 |     |      | 2   |      |
| I <sub>S(off)</sub>                | OFF-state switch leakage current                   | V <sub>I</sub> = V <sub>CC</sub> and V <sub>O</sub> = GND,<br>or V <sub>I</sub> = GND and V <sub>O</sub> = V <sub>CC</sub> ,<br>V <sub>INH</sub> = V <sub>IH</sub> | 25°C           | 5.5 V           |     |      | 0.1 | μA   |
|                                    |                                                    |                                                                                                                                                                    | –40°C to 85°C  |                 |     |      | 1   |      |
|                                    |                                                    |                                                                                                                                                                    | –40°C to 125°C |                 |     |      | 2   |      |
| I <sub>S(on)</sub>                 | ON-state switch leakage current                    | V <sub>I</sub> = V <sub>CC</sub> or GND,<br>V <sub>INH</sub> = V <sub>IL</sub><br>(see Figure4)                                                                    | 25°C           | 5.5 V           |     |      | 0.1 | μA   |
|                                    |                                                    |                                                                                                                                                                    | –40°C to 85°C  |                 |     |      | 1   |      |
|                                    |                                                    |                                                                                                                                                                    | –40°C to 125°C |                 |     |      | 2   |      |
| I <sub>CC</sub>                    | Supply current                                     | V <sub>I</sub> = V <sub>CC</sub> or GND<br>V <sub>INH</sub> = 0 V                                                                                                  | 25°C           | 5.5 V           |     | 0.01 |     | μA   |
|                                    |                                                    |                                                                                                                                                                    | –40°C to 85°C  |                 |     |      | 20  |      |
|                                    |                                                    |                                                                                                                                                                    | –40°C to 125°C |                 |     |      | 40  |      |

## 5.5 Electrical Characteristics (続き)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER           |                                | Condition                          | T <sub>A</sub> | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|---------------------|--------------------------------|------------------------------------|----------------|-----------------|-----|-----|-----|------|
| C <sub>IC</sub>     | Control input capacitance      | f = 10 MHz                         | 25°C           | 3.3 V           |     | 2   |     | pF   |
| C <sub>OS</sub>     | Switch terminal capacitance    | f = 10 MHz                         | 25°C           | 3.3 V           |     | 5   |     | pF   |
| C <sub>IS</sub>     | Common terminal capacitance    | f = 10 MHz                         | 25°C           | 3.3 V           |     | 23  |     | pF   |
| C <sub>OS(on)</sub> | Common terminal ON-capacitance | f = 10 MHz                         | 25°C           | 3.3 V           |     | 23  |     | pF   |
| C <sub>F</sub>      | Feedthrough capacitance        | f = 10 MHz                         | 25°C           | 3.3 V           |     | 0.5 |     | pF   |
| C <sub>PD</sub>     | Power dissipation capacitance  | C <sub>L</sub> = 50 pF, f = 10 MHz | 25°C           | 3.3 V           |     | 6   |     | pF   |

## 5.6 Timing Characteristics V<sub>CC</sub> = 2.5 V ± 0.2 V

| PARAMETER                            |                        | FROM (INPUT) | TO (OUTPUT) | CONDITIONS             | T <sub>A</sub> | MIN | TYP  | MAX | UNIT |
|--------------------------------------|------------------------|--------------|-------------|------------------------|----------------|-----|------|-----|------|
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay time | COM or Yn    | Yn or COM   | C <sub>L</sub> = 15 pF | 25°C           |     | 1.9  | 10  | ns   |
|                                      |                        |              |             |                        | –40°C to 85°C  |     |      | 16  |      |
|                                      |                        |              |             |                        | –40°C to 125°C |     |      | 18  |      |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Enable delay time      | INH          | COM or Yn   | C <sub>L</sub> = 15 pF | 25°C           |     | 6.6  | 18  | ns   |
|                                      |                        |              |             |                        | –40°C to 85°C  |     |      | 23  |      |
|                                      |                        |              |             |                        | –40°C to 125°C |     |      | 25  |      |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Disable delay time     | INH          | COM or Yn   | C <sub>L</sub> = 15 pF | 25°C           |     | 7.4  | 18  | ns   |
|                                      |                        |              |             |                        | –40°C to 85°C  |     |      | 23  |      |
|                                      |                        |              |             |                        | –40°C to 125°C |     |      | 25  |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay time | COM or Yn    | Yn or COM   | C <sub>L</sub> = 50 pF | 25°C           |     | 3.8  | 12  | ns   |
|                                      |                        |              |             |                        | –40°C to 85°C  |     |      | 18  |      |
|                                      |                        |              |             |                        | –40°C to 125°C |     |      | 20  |      |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Enable delay time      | INH          | COM or Yn   | C <sub>L</sub> = 50 pF | 25°C           |     | 7.8  | 28  | ns   |
|                                      |                        |              |             |                        | –40°C to 85°C  |     |      | 35  |      |
|                                      |                        |              |             |                        | –40°C to 125°C |     |      | 35  |      |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Disable delay time     | INH          | COM or Yn   | C <sub>L</sub> = 50 pF | 25°C           |     | 11.5 | 28  | ns   |
|                                      |                        |              |             |                        | –40°C to 85°C  |     |      | 35  |      |
|                                      |                        |              |             |                        | –40°C to 125°C |     |      | 35  |      |

## 5.7 Timing Characteristics V<sub>CC</sub> = 3.3 V ± 0.3 V

| PARAMETER                            |                        | FROM (INPUT) | TO (OUTPUT) | CONDITIONS             | T <sub>A</sub> | MIN | TYP | MAX | UNIT |
|--------------------------------------|------------------------|--------------|-------------|------------------------|----------------|-----|-----|-----|------|
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay time | COM or Yn    | Yn or COM   | C <sub>L</sub> = 15 pF | 25°C           |     | 1.2 | 6   | ns   |
|                                      |                        |              |             |                        | –40°C to 85°C  |     |     | 10  |      |
|                                      |                        |              |             |                        | –40°C to 125°C |     |     | 12  |      |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Enable delay time      | INH          | COM or Yn   | C <sub>L</sub> = 15 pF | 25°C           |     | 4.7 | 12  | ns   |
|                                      |                        |              |             |                        | –40°C to 85°C  |     |     | 15  |      |
|                                      |                        |              |             |                        | –40°C to 125°C |     |     | 18  |      |

## 5.7 Timing Characteristics $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (続き)

| PARAMETER              |                        | FROM (INPUT) | TO (OUTPUT) | CONDITIONS           | $T_A$          | MIN | TYP | MAX | UNIT |
|------------------------|------------------------|--------------|-------------|----------------------|----------------|-----|-----|-----|------|
| $t_{PHZ}$<br>$t_{PLZ}$ | Disable delay time     | INH          | COM or Yn   | $C_L = 15\text{ pF}$ | 25°C           |     | 5.7 | 12  | ns   |
|                        |                        |              |             |                      | –40°C to 85°C  |     |     | 15  |      |
|                        |                        |              |             |                      | –40°C to 125°C |     |     | 18  |      |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay time | COM or Yn    | Yn or COM   | $C_L = 50\text{ pF}$ | 25°C           |     | 2.5 | 9   | ns   |
|                        |                        |              |             |                      | –40°C to 85°C  |     |     | 12  |      |
|                        |                        |              |             |                      | –40°C to 125°C |     |     | 14  |      |
| $t_{PZH}$<br>$t_{PZL}$ | Enable delay time      | INH          | COM or Yn   | $C_L = 50\text{ pF}$ | 25°C           |     | 5.5 | 20  | ns   |
|                        |                        |              |             |                      | –40°C to 85°C  |     |     | 25  |      |
|                        |                        |              |             |                      | –40°C to 125°C |     |     | 25  |      |
| $t_{PHZ}$<br>$t_{PLZ}$ | Disable delay time     | INH          | COM or Yn   | $C_L = 50\text{ pF}$ | 25°C           |     | 8.8 | 20  | ns   |
|                        |                        |              |             |                      | –40°C to 85°C  |     |     | 25  |      |
|                        |                        |              |             |                      | –40°C to 125°C |     |     | 25  |      |

## 5.8 Timing Characteristics $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

| PARAMETER              |                        | FROM (INPUT) | TO (OUTPUT) | CONDITIONS           | $T_A$          | MIN | TYP | MAX | UNIT |
|------------------------|------------------------|--------------|-------------|----------------------|----------------|-----|-----|-----|------|
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay time | COM or Yn    | Yn or COM   | $C_L = 15\text{ pF}$ | 25°C           |     | 0.6 | 4   | ns   |
|                        |                        |              |             |                      | –40°C to 85°C  |     |     | 7   |      |
|                        |                        |              |             |                      | –40°C to 125°C |     |     | 10  |      |
| $t_{PZH}$<br>$t_{PZL}$ | Enable delay time      | INH          | COM or Yn   | $C_L = 15\text{ pF}$ | 25°C           |     | 3.5 | 8   | ns   |
|                        |                        |              |             |                      | –40°C to 85°C  |     |     | 10  |      |
|                        |                        |              |             |                      | –40°C to 125°C |     |     | 12  |      |
| $t_{PHZ}$<br>$t_{PLZ}$ | Disable delay time     | INH          | COM or Yn   | $C_L = 15\text{ pF}$ | 25°C           |     | 4.4 | 10  | ns   |
|                        |                        |              |             |                      | –40°C to 85°C  |     |     | 11  |      |
|                        |                        |              |             |                      | –40°C to 125°C |     |     | 12  |      |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay time | COM or Yn    | Yn or COM   | $C_L = 50\text{ pF}$ | 25°C           |     | 1.5 | 6   | ns   |
|                        |                        |              |             |                      | –40°C to 85°C  |     |     | 8   |      |
|                        |                        |              |             |                      | –40°C to 125°C |     |     | 10  |      |
| $t_{PZH}$<br>$t_{PZL}$ | Enable delay time      | INH          | COM or Yn   | $C_L = 50\text{ pF}$ | 25°C           |     | 4   | 14  | ns   |
|                        |                        |              |             |                      | –40°C to 85°C  |     |     | 18  |      |
|                        |                        |              |             |                      | –40°C to 125°C |     |     | 18  |      |
| $t_{PHZ}$<br>$t_{PLZ}$ | Disable delay time     | INH          | COM or Yn   | $C_L = 50\text{ pF}$ | 25°C           |     | 6.2 | 14  | ns   |
|                        |                        |              |             |                      | –40°C to 85°C  |     |     | 18  |      |
|                        |                        |              |             |                      | –40°C to 125°C |     |     | 18  |      |

## 5.9 AC Characteristics

| PARAMETER                                         | FROM (INPUT) | TO (OUTPUT) | Device     | CONDITIONS                                                                                                |                         | MIN | TYP | MAX | UNIT |
|---------------------------------------------------|--------------|-------------|------------|-----------------------------------------------------------------------------------------------------------|-------------------------|-----|-----|-----|------|
| Frequency response (switch on)                    | COM or Yn    | Yn or COM   | SN74LV4053 | $C_L = 50\text{ pF}$ , $R_L = 600\ \Omega$ ,<br>$F_{in} = 1\text{ MHz}$ (sine wave),<br>(see Figure 7)(1) | $V_{CC} = 2.3\text{ V}$ |     | 40  |     | MHz  |
|                                                   |              |             |            |                                                                                                           | $V_{CC} = 3\text{ V}$   |     | 45  |     |      |
|                                                   |              |             |            |                                                                                                           | $V_{CC} = 4.5\text{ V}$ |     | 60  |     |      |
| Charge Injection (control input to signal output) | INH          | COM or Yn   |            | $C_L = 50\text{ pF}$ , $R_L = 600\ \Omega$ ,<br>$F_{in} = 1\text{ MHz}$ (sine wave)<br>(see Figure 9)     | $V_{CC} = 2.3\text{ V}$ |     | 20  |     | mV   |
|                                                   |              |             |            |                                                                                                           | $V_{CC} = 3\text{ V}$   |     | 35  |     |      |
|                                                   |              |             |            |                                                                                                           | $V_{CC} = 4.5\text{ V}$ |     | 60  |     |      |



## 5.9 AC Characteristics (続き)

| PARAMETER                            | FROM (INPUT) | TO (OUTPUT) | Device | CONDITIONS                                                                                                      | MIN                                           | TYP | MAX | UNIT |
|--------------------------------------|--------------|-------------|--------|-----------------------------------------------------------------------------------------------------------------|-----------------------------------------------|-----|-----|------|
| Feedthrough attenuation (switch off) | COM or Yn    | Yn or COM   |        | $C_L = 50 \text{ pF}$ , $R_L = 600 \Omega$ ,<br>$F_{in} = 1 \text{ MHz}$ (sine wave)<br>(see Figure 10) (2)     | $V_{CC} = 2.3 \text{ V}$                      | –45 |     | dB   |
|                                      |              |             |        |                                                                                                                 | $V_{CC} = 3 \text{ V}$                        | –45 |     |      |
|                                      |              |             |        |                                                                                                                 | $V_{CC} = 4.5 \text{ V}$                      | –45 |     |      |
| Crosstalk (between any switches)     | COM or Yn    | Yn or COM   |        | $C_L = 50 \text{ pF}$ , $R_L = 600 \Omega$ ,<br>$F_{in} = 1 \text{ MHz}$ (sine wave)<br>(see Figure 8)(2)       | $V_{CC} = 2.3 \text{ V}$                      | –45 |     | dB   |
|                                      |              |             |        |                                                                                                                 | $V_{CC} = 3 \text{ V}$                        | –45 |     |      |
|                                      |              |             |        |                                                                                                                 | $V_{CC} = 4.5 \text{ V}$                      | –45 |     |      |
| Sine-wave distortion                 | COM or Yn    | Yn or COM   |        | $C_L = 50 \text{ pF}$ , $R_L = 10 \text{ k}\Omega$ ,<br>$F_{in} = 1 \text{ kHz}$ (sine wave)<br>(see Figure 11) | $V_I = 2 V_{p-p}$<br>$V_{CC} = 2.3 \text{ V}$ | 0.1 |     | %    |
|                                      |              |             |        |                                                                                                                 | $V_I = 2.5 V_{p-p}$<br>$V_{CC} = 3 \text{ V}$ | 0.1 |     |      |
|                                      |              |             |        |                                                                                                                 | $V_I = 4 V_{p-p}$<br>$V_{CC} = 4.5 \text{ V}$ | 0.1 |     |      |

## 6 Parameter Measurement Information

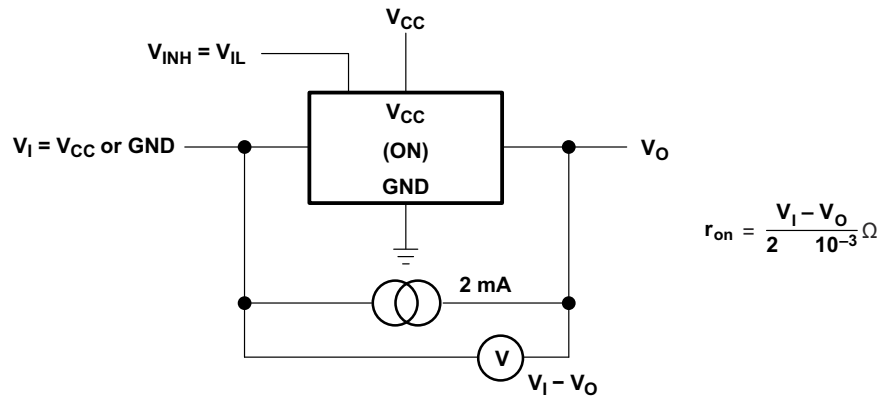


図 6-1. On-State Resistance Test Circuit

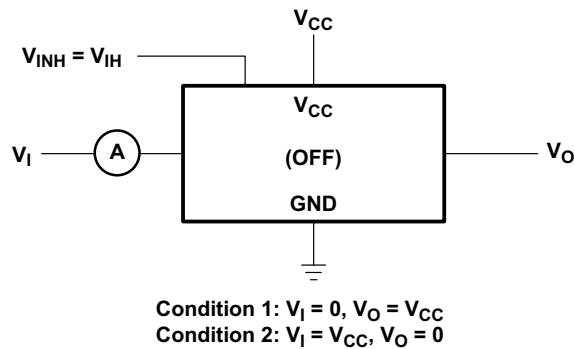


図 6-2. Off-State Switch Leakage-Current Test Circuit

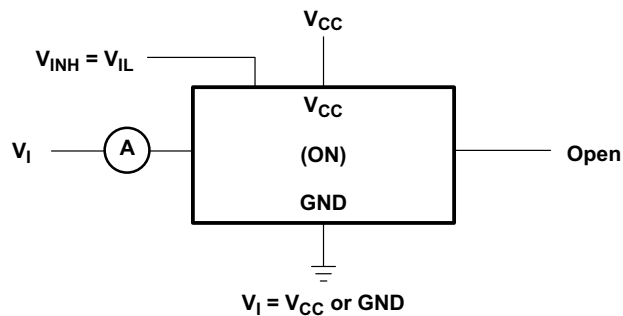


図 6-3. On-State Switch Leakage-Current Test Circuit

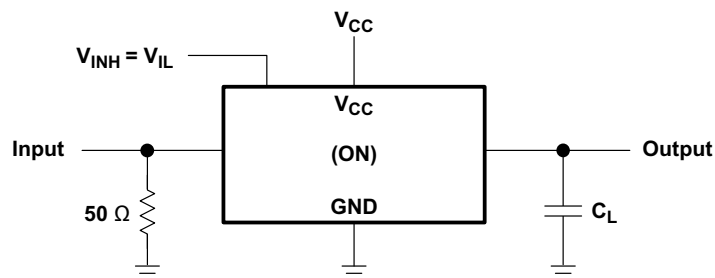
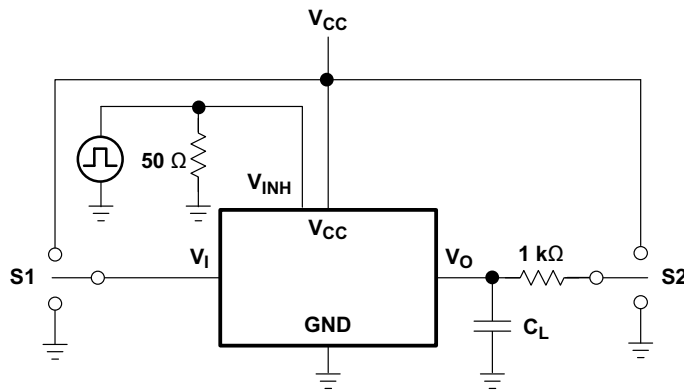
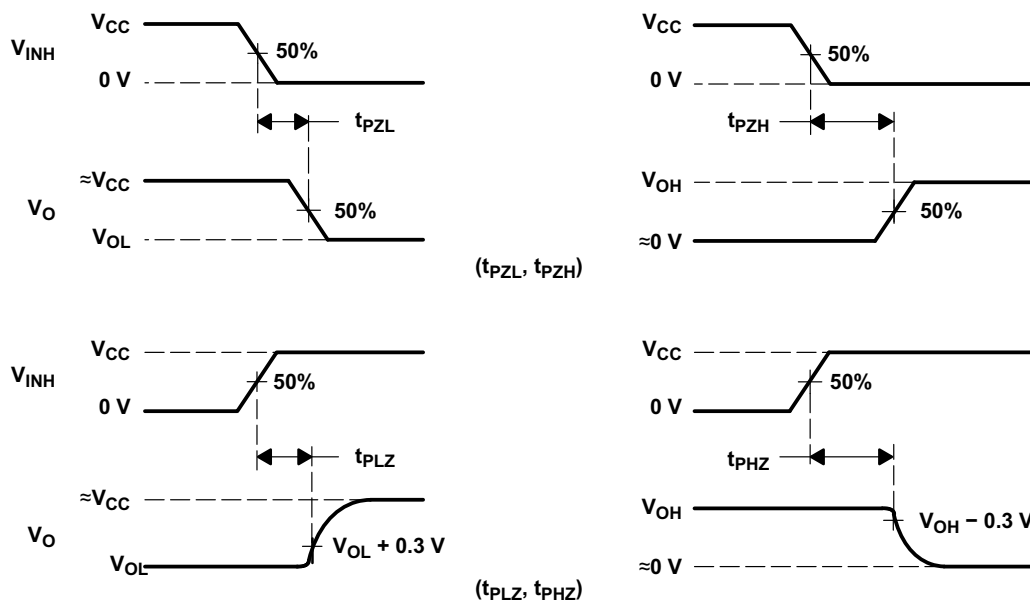


図 6-4. Propagation Delay Time, Signal Input to Signal Output



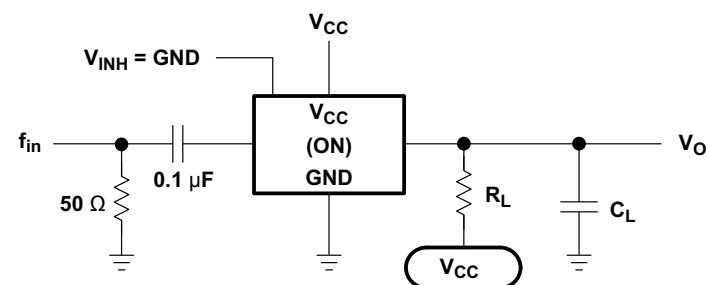
TEST CIRCUIT

| TEST              | S1       | S2       |
|-------------------|----------|----------|
| $t_{PLZ}/t_{PZL}$ | GND      | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | $V_{CC}$ | GND      |



VOLTAGE WAVEFORMS

FIG 6-5. Switching Time ( $t_{PZL}$ ,  $t_{PLZ}$ ,  $t_{PZH}$ ,  $t_{PHZ}$ ), Control to Signal Output



NOTE A:  $f_{in}$  is a sine wave.

FIG 6-6. Frequency Response (Switch On)

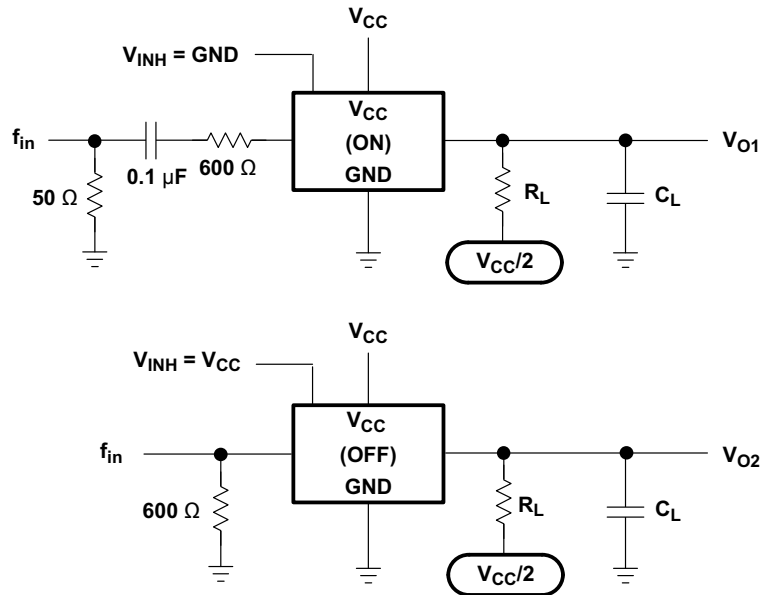


図 6-7. Crosstalk Between Any Two Switches

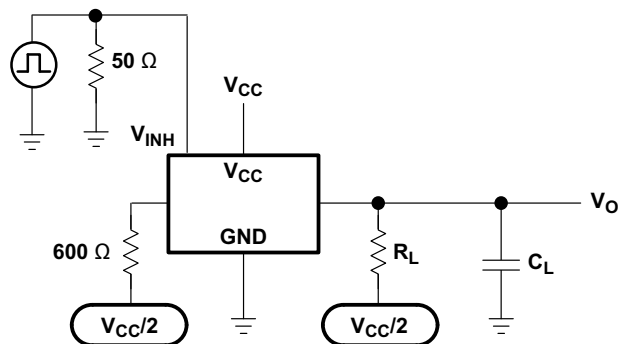


図 6-8. Crosstalk Between Control Input and Switch Output

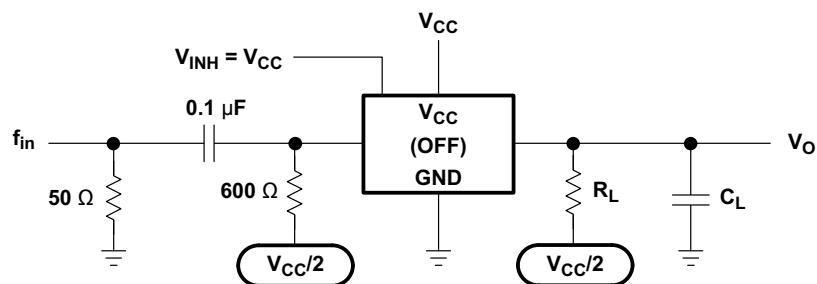
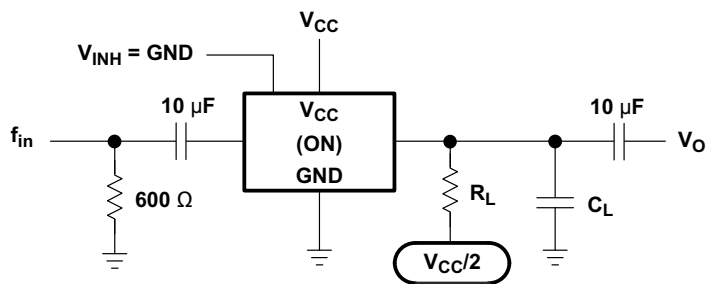


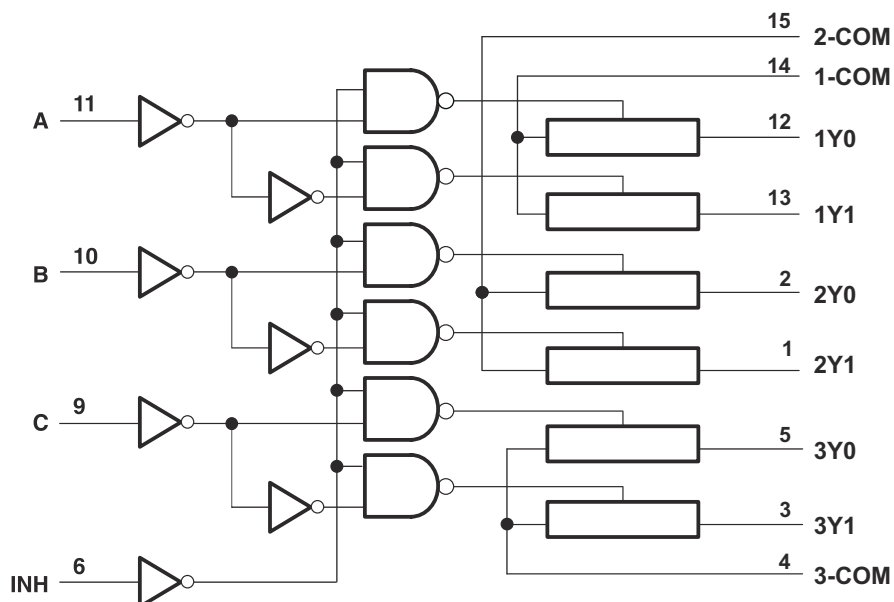
図 6-9. Feedthrough Attenuation (Switch Off)




**6-10. Sine-Wave Distortion**

## 7 Detailed Description

### 7.1 Functional Block Diagram



### 7.2 Device Functional Modes

Function Table

| INPUTS |   |   |   | ON CHANNEL    |
|--------|---|---|---|---------------|
| INH    | C | B | A |               |
| L      | L | L | L | 1Y0, 2Y0, 3Y0 |
| L      | L | L | H | 1Y1, 2Y0, 3Y0 |
| L      | L | H | L | 1Y0, 2Y1, 3Y0 |
| L      | L | H | H | 1Y1, 2Y1, 3Y0 |
| L      | H | L | L | 1Y0, 2Y0, 3Y1 |
| L      | H | L | H | 1Y1, 2Y0, 3Y1 |
| L      | H | H | L | 1Y0, 2Y1, 3Y1 |
| L      | H | H | H | 1Y1, 2Y1, 3Y1 |
| H      | X | X | X | None          |

## 8 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 8.1 Application Information

A multiplexer is used in applications where multiple signals share a resource. In the following example, several different sensors are connected to the analog-to-digital converter (ADC) of a microcontroller (MCU).

### 8.2 Typical Application

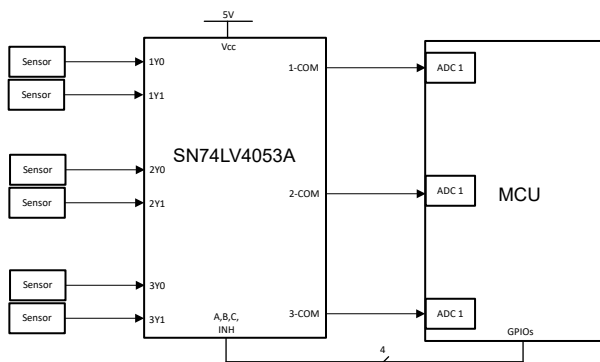


図 8-1. Typical Application Schematic

#### 8.2.1 Design Requirements

Processing 8 different analog signals would normally require 8 separate ADCs, but the previous figure shows how to achieve this using only 2 ADCs and 3 GPIOs (general purpose input/outputs).

#### 8.2.2 Detailed Design Procedure

To design with the SNx4LV4053A, a stable input voltage between 2V (see *Recommended Operating Conditions* for details) and 5.5V must be available. The characteristics of the signal that is being multiplexed so that no important information is lost due to timing or voltage level incompatibility with this device is another important design consideration.

### 8.3 Power Supply Recommendations

Most systems have a common 3.3V or 5V rail that may be used to supply the  $V_{CC}$  pin of this device. If this is not available, then a Switch-Mode-Power-Supply (SMPS) or a Linear Dropout Regulator (LDO) may be used to supply this device from a higher voltage rail.

### 8.4 Layout

#### 8.4.1 Layout Guidelines

In general, it is best to keep signal lines as short and as straight as possible. Incorporation of microstrip or stripline techniques is also recommended when signal lines are greater than 1 inch in length. These traces must be designed with a characteristic impedance of either 50Ω or 75Ω, as required by the application. Be careful when placing this device too close to high voltage switching components, as they may cause interference.

## 8.4.2 Layout Example

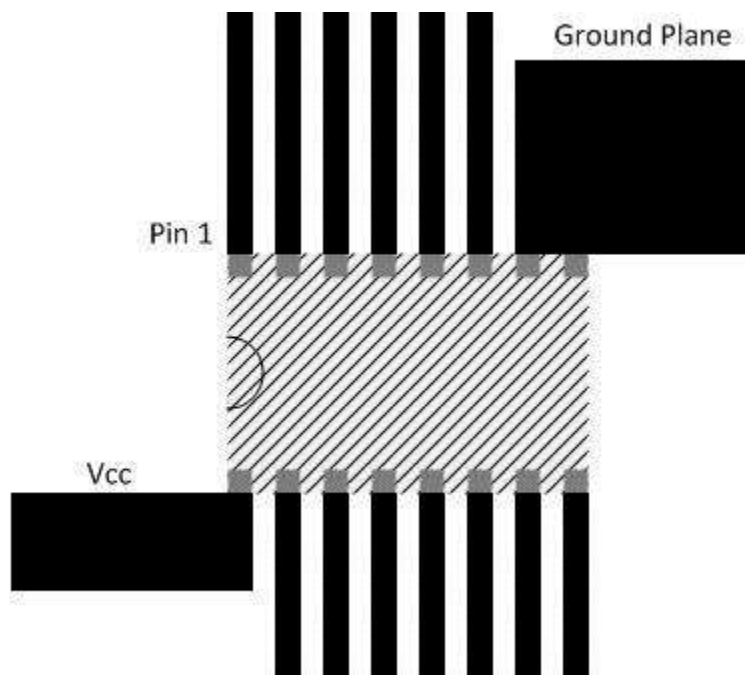


図 8-2. Layout Example Schematic



## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

### 9.2 サポート・リソース

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### 9.3 Trademarks

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### 9.4 静電気放電に関する注意事項



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### 9.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### Changes from Revision L (June 2024) to Revision M (September 2024)

|                          | Page |
|--------------------------|------|
| • DYY パッケージとサイズを追加.....  | 1    |
| • Added DYY package..... | 3    |
| • Added DYY package..... | 4    |

### Changes from Revision K (April 2005) to Revision L (June 2024)

|                                                                       | Page |
|-----------------------------------------------------------------------|------|
| • ドキュメント全体にわたって表、図、相互参照の採番方法を変更.....                                  | 1    |
| • Added new VIH and VIL Specifications at 1.65V Vcc.....              | 5    |
| • Increased max ambient temperature max to 125C.....                  | 5    |
| • Added Ron, Ron Peak, and Delta Ron Specifications at 1.65V Vcc..... | 5    |
| • Added Ron, Ron Peak, and Delta Ron Specifications at 125C.....      | 5    |
| • Added Timing Specifications at 125C.....                            | 7    |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins            | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------------|---------------|----------------------|---------------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74LV4053AD</a>     | Obsolete      | Production           | SOIC (D)   16             | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | LV4053A             |
| <a href="#">SN74LV4053ADBR</a>   | NRND          | Production           | SSOP (DB)   16            | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LW053A              |
| SN74LV4053ADBR.A                 | NRND          | Production           | SSOP (DB)   16            | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LW053A              |
| <a href="#">SN74LV4053ADGVR</a>  | NRND          | Production           | TVSOP (DGV)   16          | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LW053A              |
| SN74LV4053ADGVR.A                | NRND          | Production           | TVSOP (DGV)   16          | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LW053A              |
| <a href="#">SN74LV4053ADR</a>    | Active        | Production           | SOIC (D)   16             | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV4053A             |
| SN74LV4053ADR.A                  | Active        | Production           | SOIC (D)   16             | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV4053A             |
| <a href="#">SN74LV4053ADYYR</a>  | Active        | Production           | SOT-23-THIN<br>(DYY)   16 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV4053              |
| SN74LV4053ADYYR.A                | Active        | Production           | SOT-23-THIN<br>(DYY)   16 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV4053              |
| <a href="#">SN74LV4053AN</a>     | NRND          | Production           | PDIP (N)   16             | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74LV4053AN        |
| SN74LV4053AN.A                   | NRND          | Production           | PDIP (N)   16             | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74LV4053AN        |
| <a href="#">SN74LV4053ANSR</a>   | NRND          | Production           | SOP (NS)   16             | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 74LV4053A           |
| SN74LV4053ANSR.A                 | NRND          | Production           | SOP (NS)   16             | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 74LV4053A           |
| <a href="#">SN74LV4053APW</a>    | Obsolete      | Production           | TSSOP (PW)   16           | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | LW053A              |
| <a href="#">SN74LV4053APWR</a>   | Active        | Production           | TSSOP (PW)   16           | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LW053A              |
| SN74LV4053APWR.A                 | Active        | Production           | TSSOP (PW)   16           | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LW053A              |
| <a href="#">SN74LV4053APWRG4</a> | Obsolete      | Production           | TSSOP (PW)   16           | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | LW053A              |
| <a href="#">SN74LV4053APWT</a>   | Obsolete      | Production           | TSSOP (PW)   16           | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | LW053A              |
| <a href="#">SN74LV4053ARGYR</a>  | Active        | Production           | VQFN (RGY)   16           | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LW053A              |
| SN74LV4053ARGYR.A                | Active        | Production           | VQFN (RGY)   16           | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LW053A              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LV4053A :**

- Automotive : [SN74LV4053A-Q1](#)
- Enhanced Product : [SN74LV4053A-EP](#)

NOTE: Qualified Version Definitions:

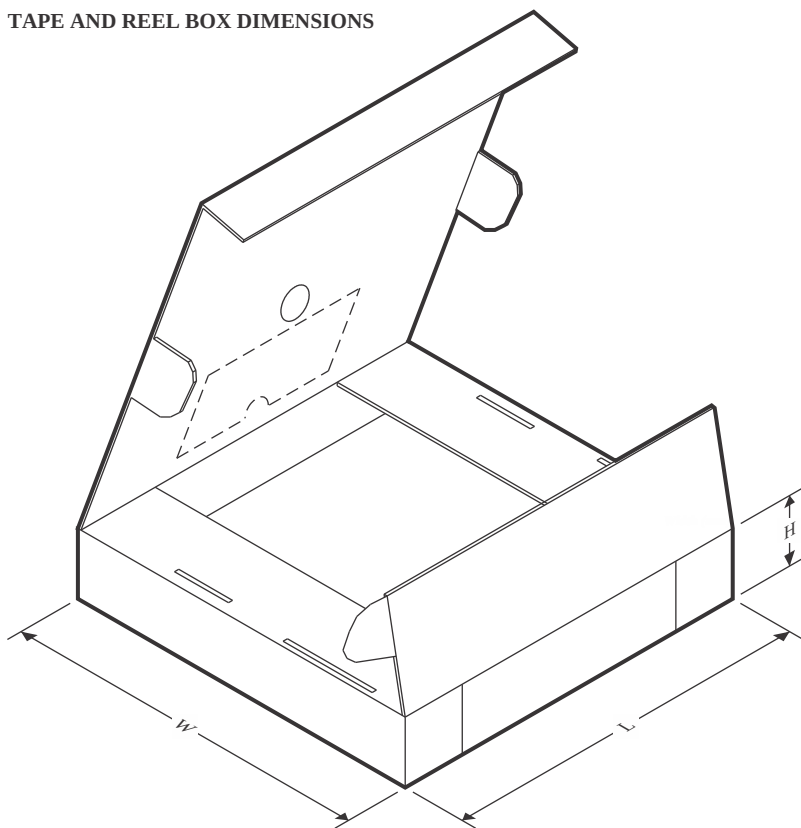
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

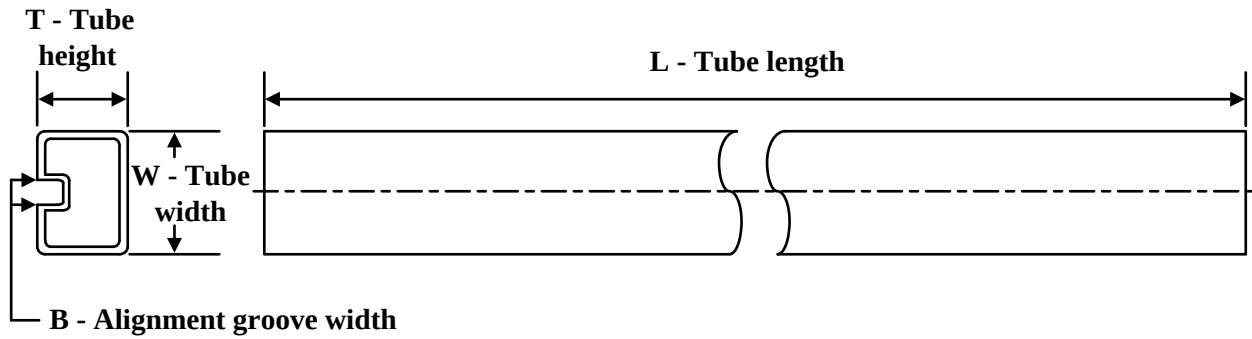
| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV4053ADBR  | SSOP         | DB              | 16   | 2000 | 330.0              | 16.4               | 8.35    | 6.6     | 2.4     | 12.0    | 16.0   | Q1            |
| SN74LV4053ADGVR | TVSOP        | DGV             | 16   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LV4053ADR   | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LV4053ADYYR | SOT-23-THIN  | DYY             | 16   | 3000 | 330.0              | 12.4               | 4.8     | 3.6     | 1.6     | 8.0     | 12.0   | Q3            |
| SN74LV4053ANSR  | SOP          | NS              | 16   | 2000 | 330.0              | 16.4               | 8.1     | 10.4    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LV4053APWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LV4053ARGYR | VQFN         | RGY             | 16   | 3000 | 330.0              | 12.4               | 3.8     | 4.3     | 1.5     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV4053ADBR  | SSOP         | DB              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LV4053ADGVR | TVSOP        | DGV             | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LV4053ADR   | SOIC         | D               | 16   | 2500 | 353.0       | 353.0      | 32.0        |
| SN74LV4053ADYYR | SOT-23-THIN  | DYY             | 16   | 3000 | 336.6       | 336.6      | 31.8        |
| SN74LV4053ANSR  | SOP          | NS              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LV4053APWR  | TSSOP        | PW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LV4053ARGYR | VQFN         | RGY             | 16   | 3000 | 360.0       | 360.0      | 36.0        |

**TUBE**


\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LV4053AN   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74LV4053AN   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74LV4053AN.A | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74LV4053AN.A | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |





**NS0016A**

**SOP - 2.00 mm max height**

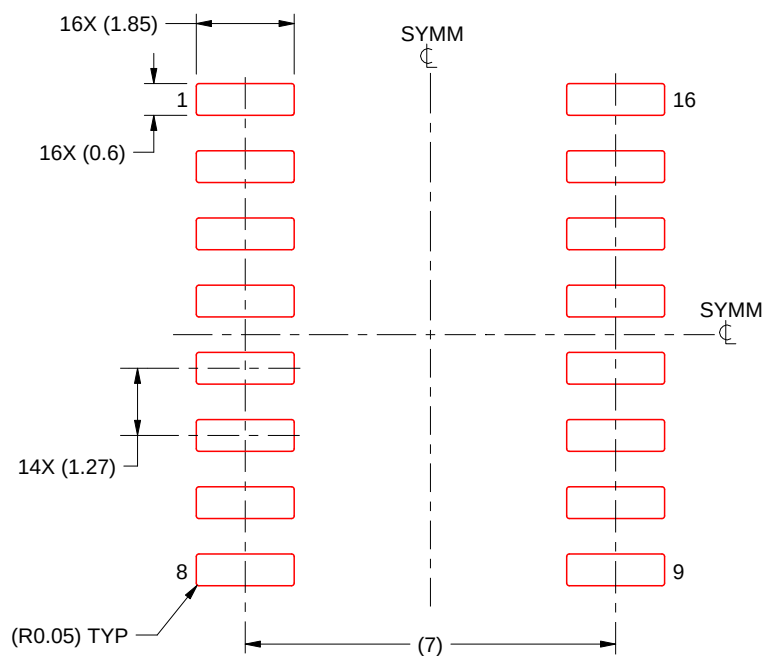
SOP



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.





SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:7X

4220735/A 12/2021

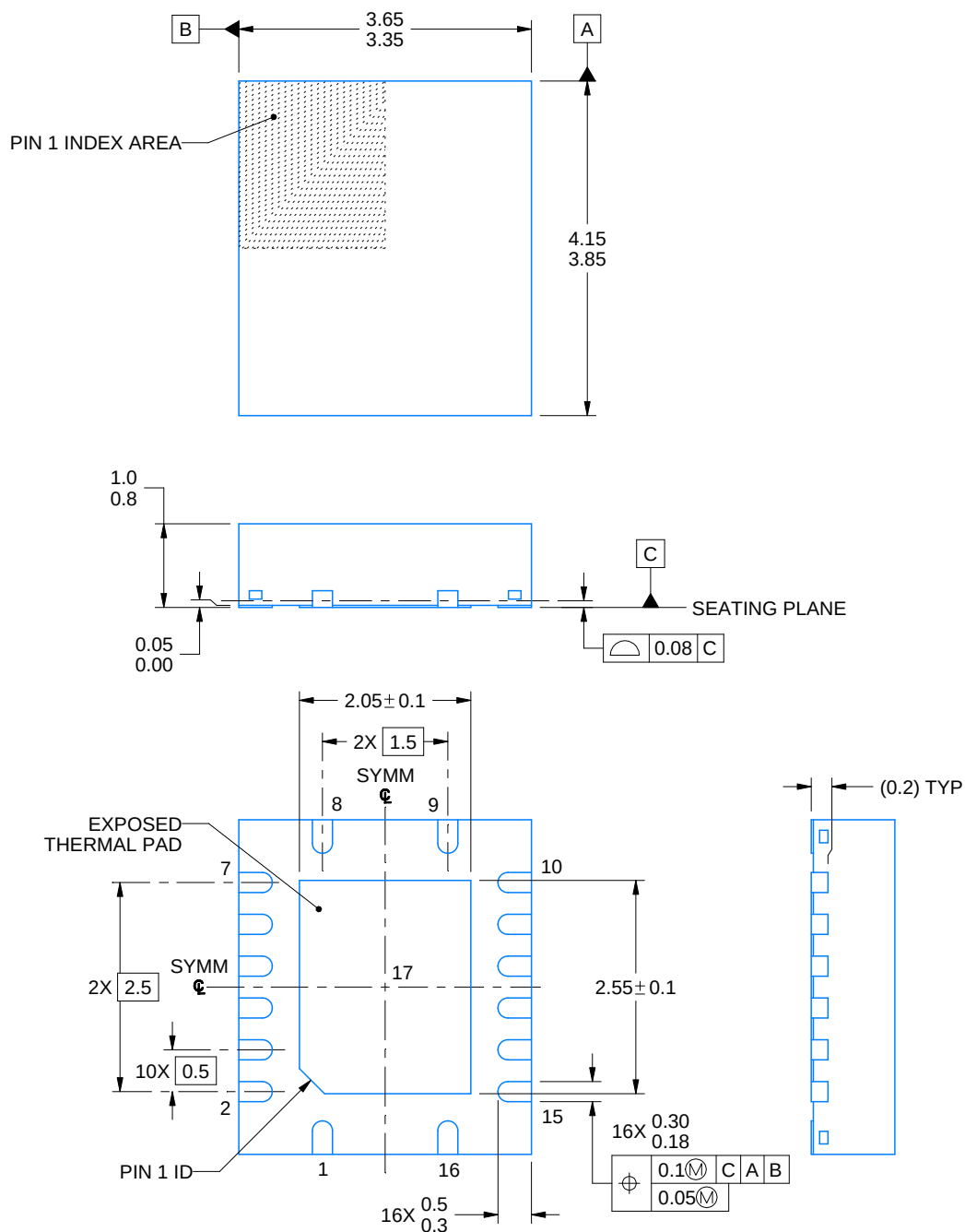
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4225140/A 07/2019

NOTES:

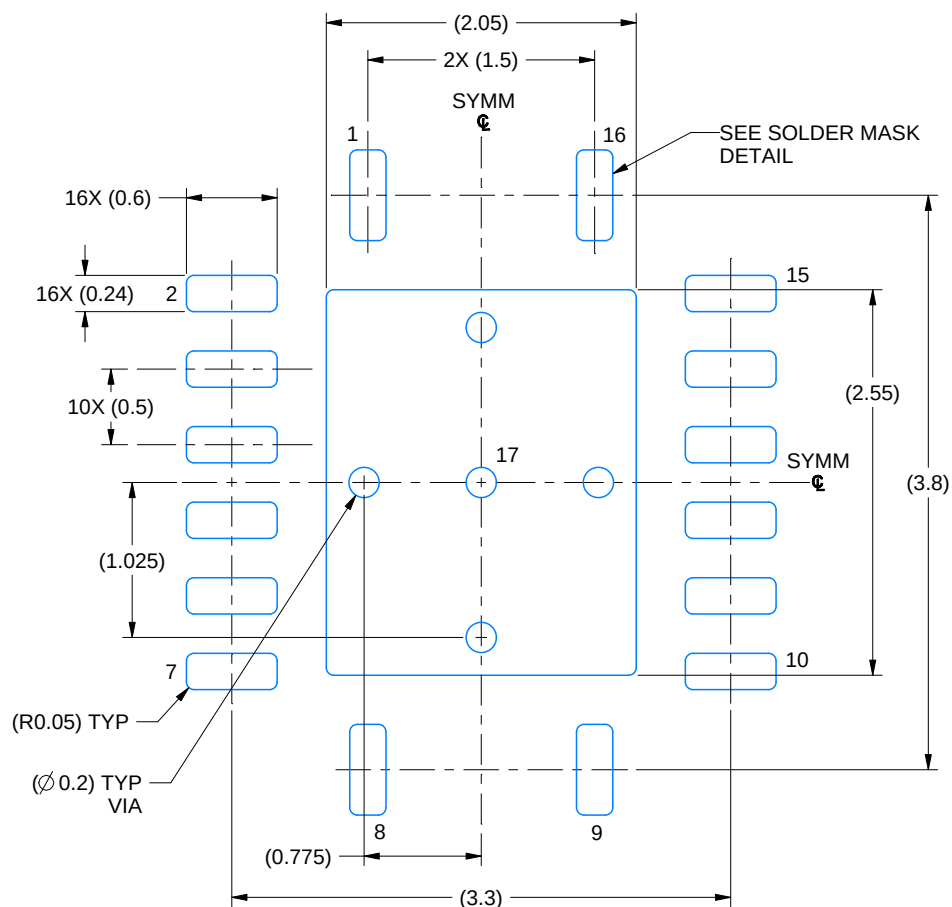
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

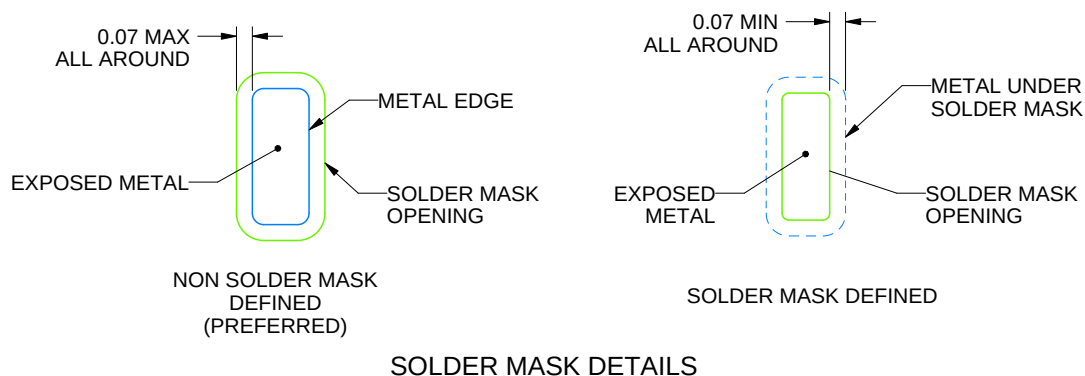
RGY0016A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4225140/A 07/2019

NOTES: (continued)

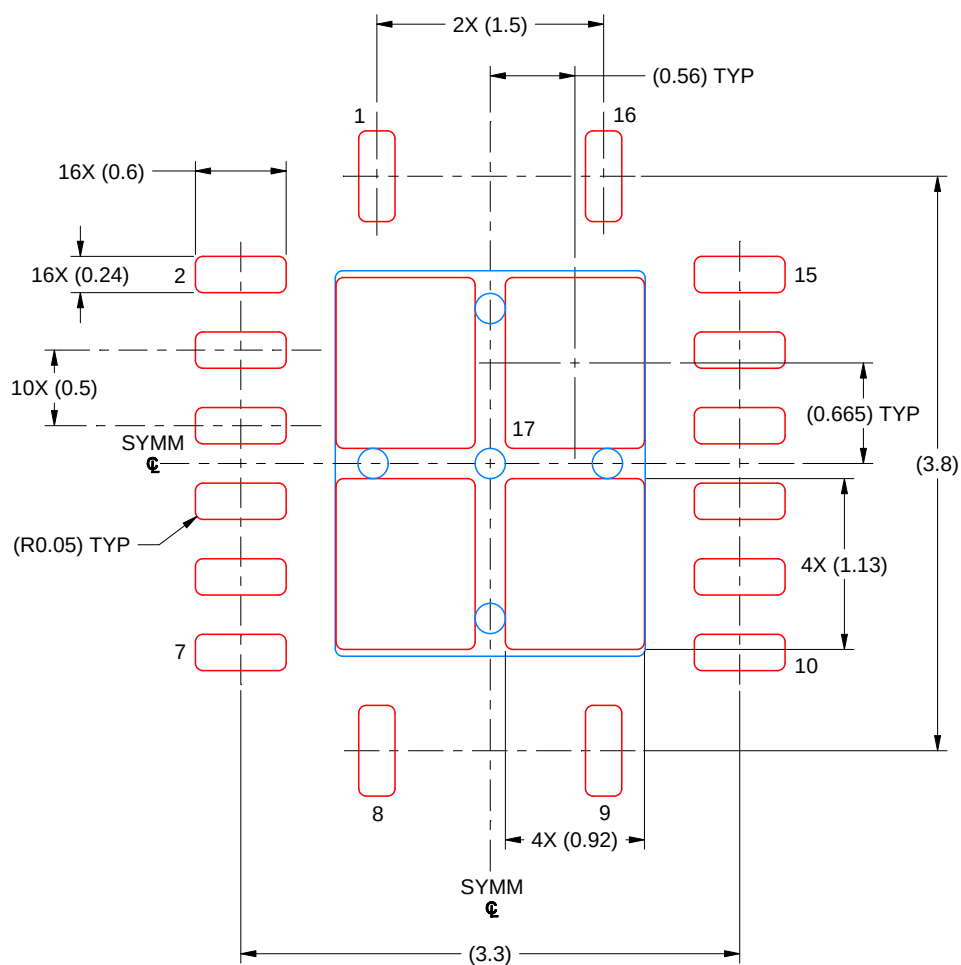
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGY0016A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 20X

EXPOSED PAD 17  
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

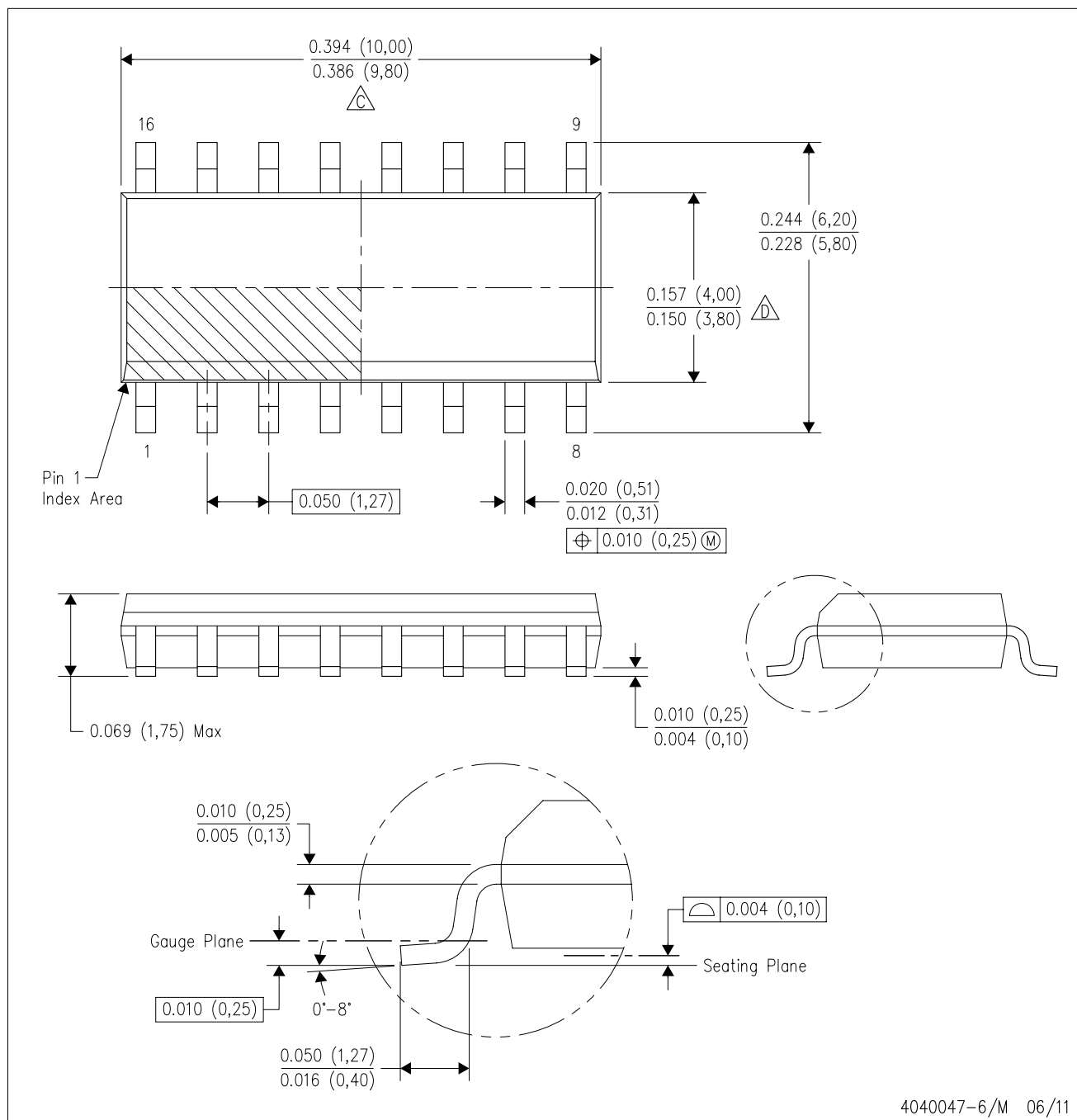
4225140/A 07/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



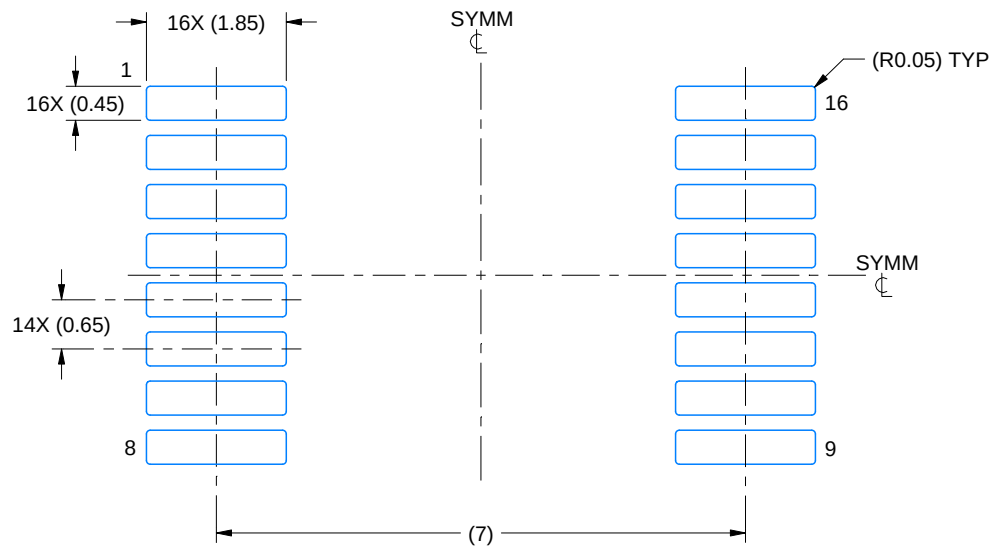


# EXAMPLE BOARD LAYOUT

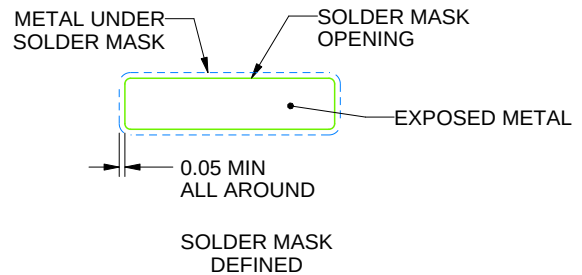
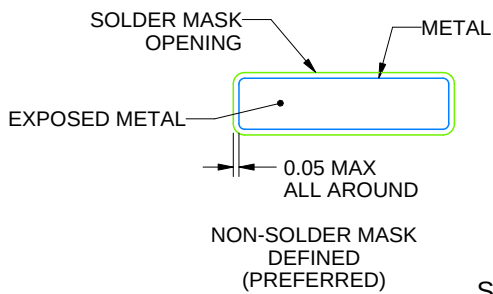
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

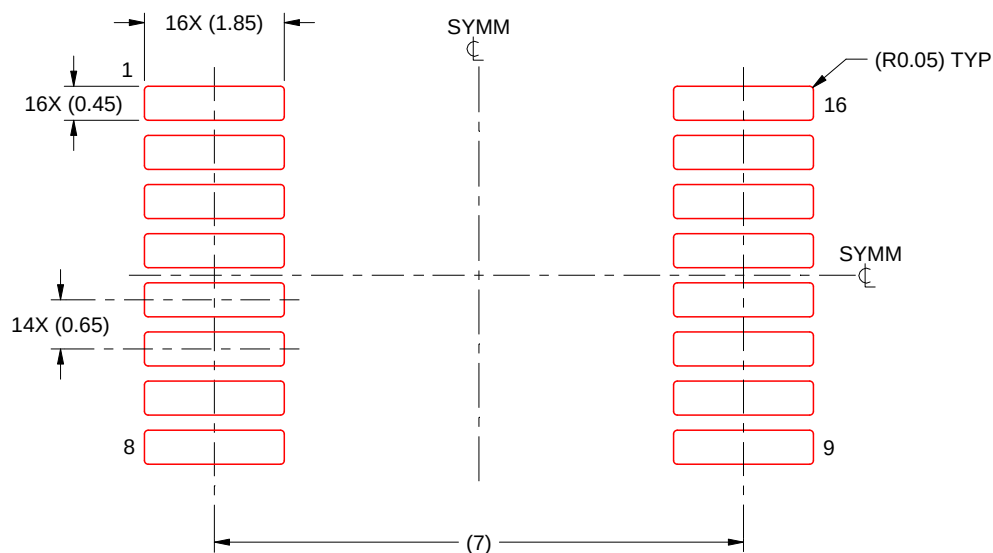
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220763/A 05/2022

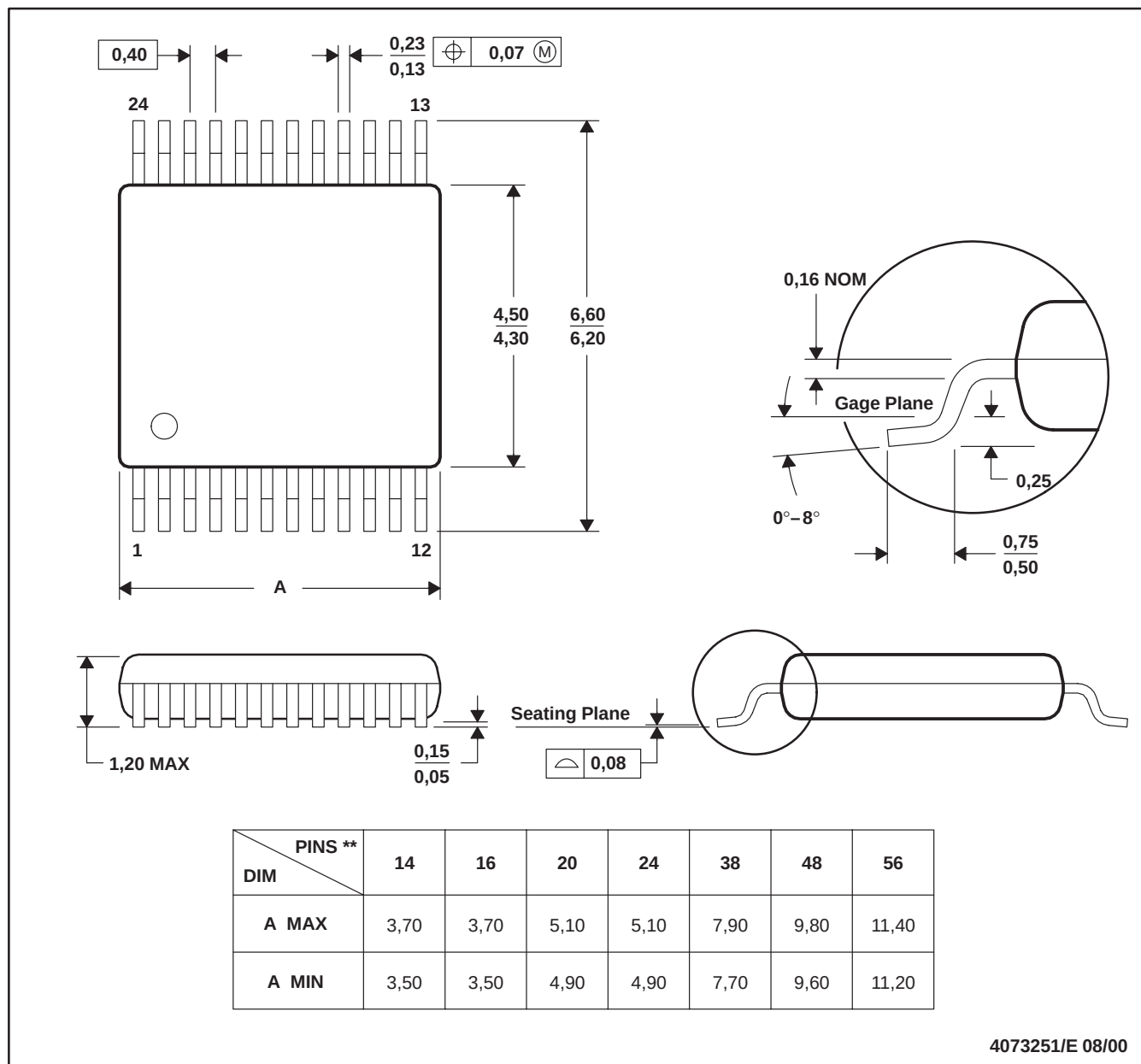
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

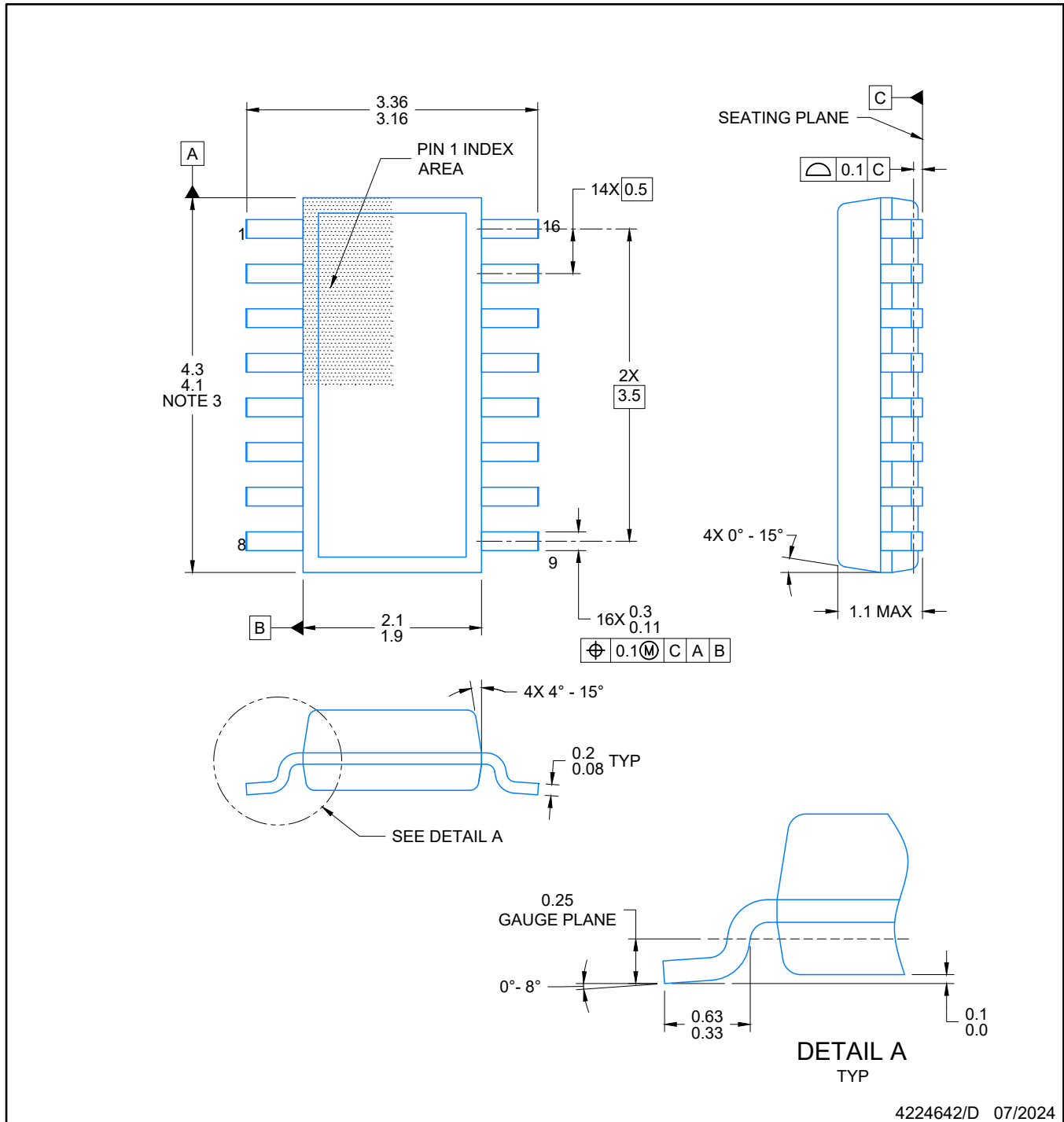
## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



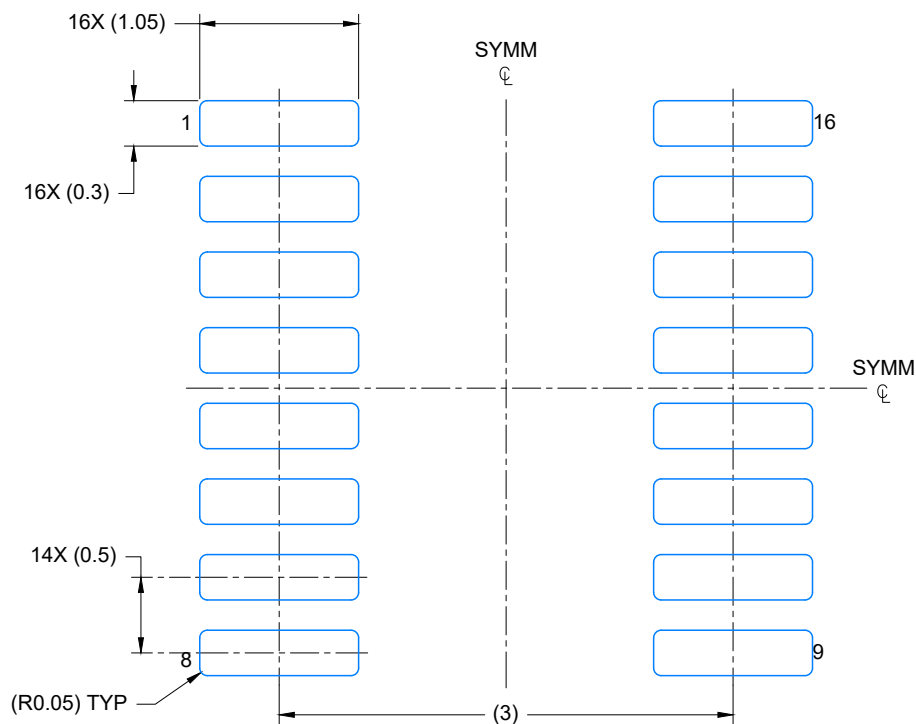
- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



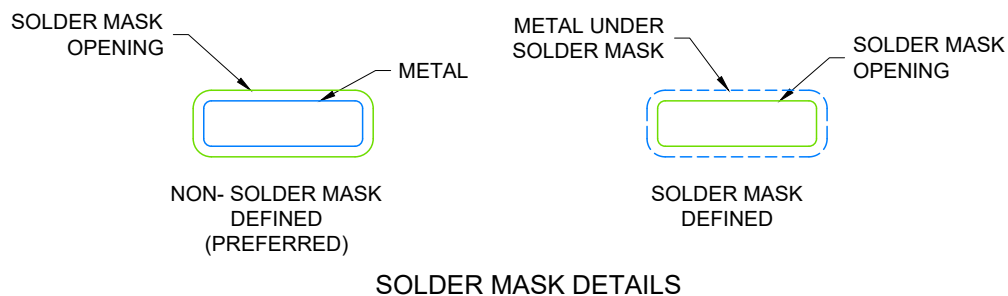
4224642/D 07/2024

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



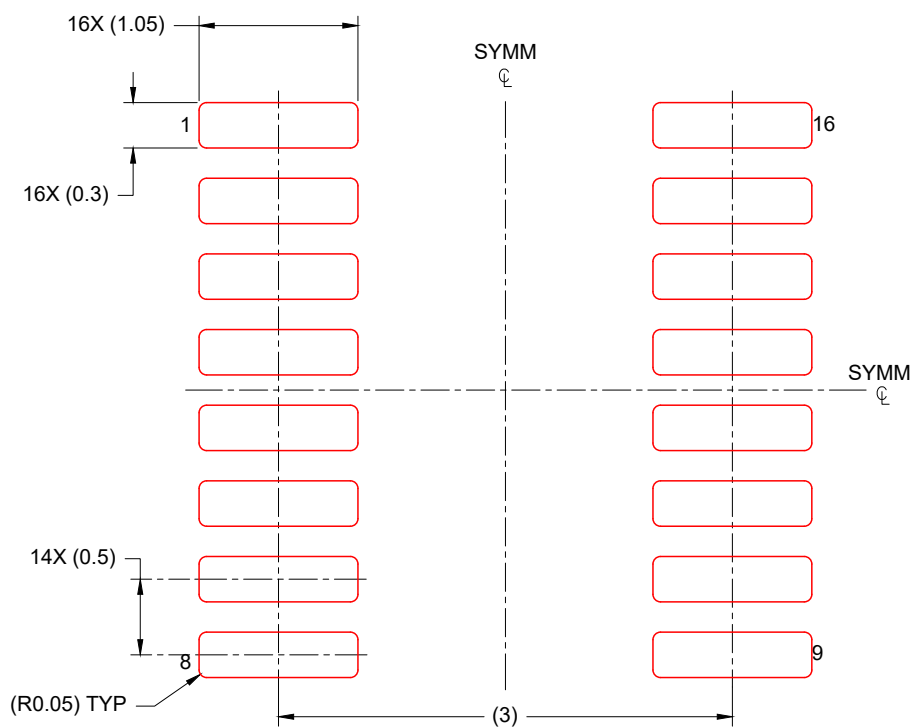
LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224642/D 07/2024

## NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

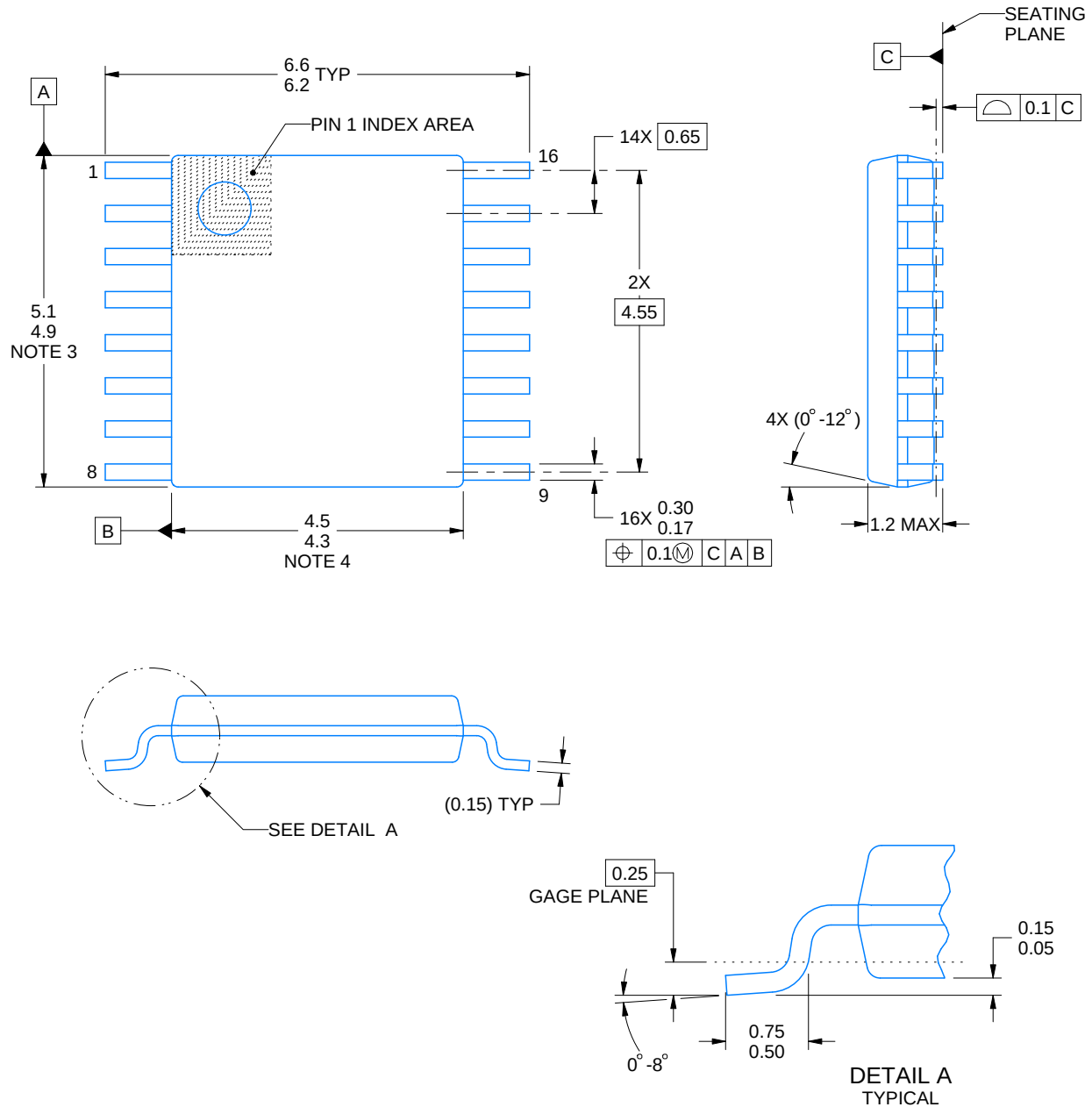
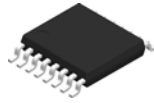


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 20X

4224642/D 07/2024

## NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220204/B 12/2023

## NOTES:

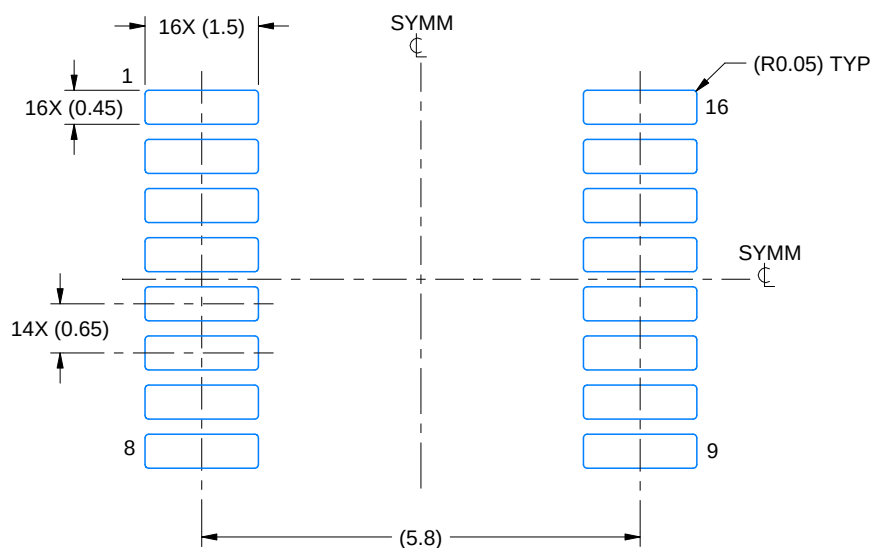
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

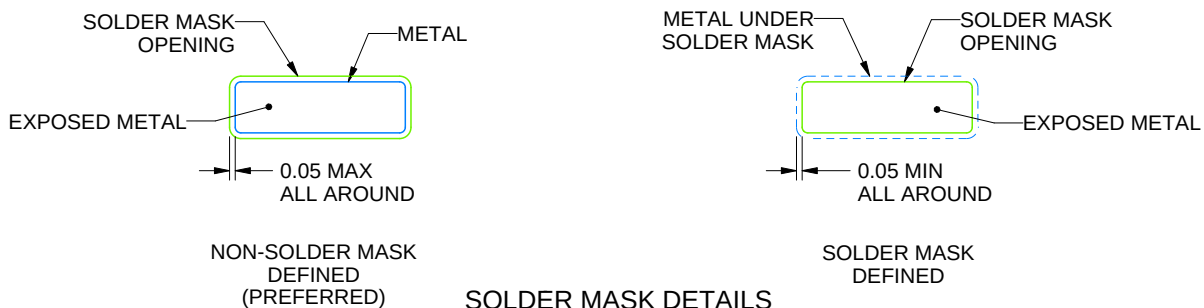
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

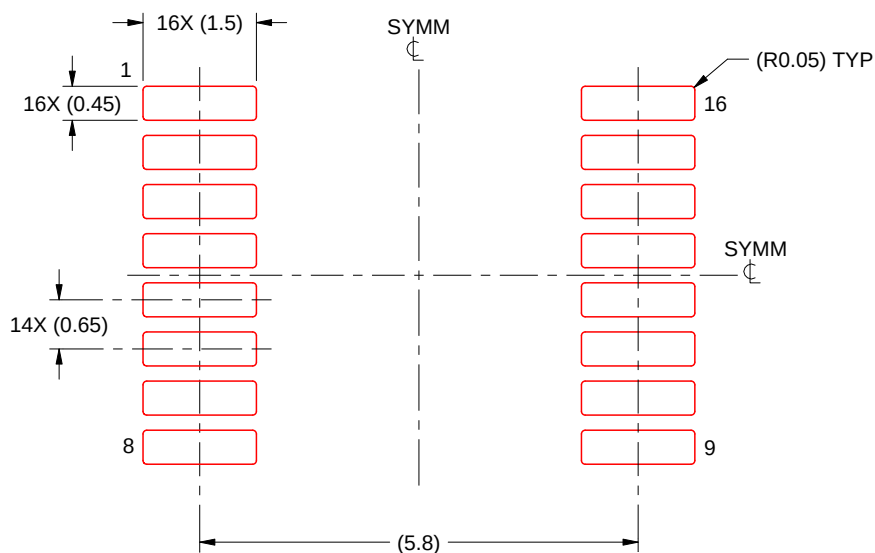


# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220204/B 12/2023

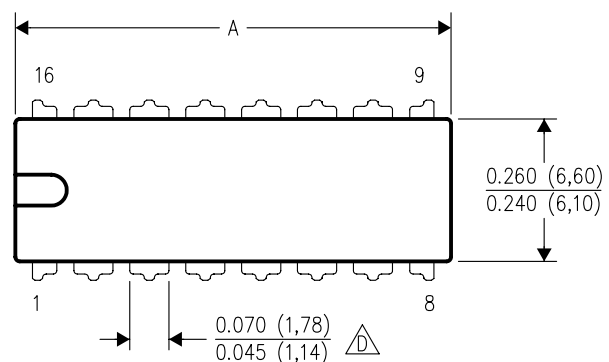
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

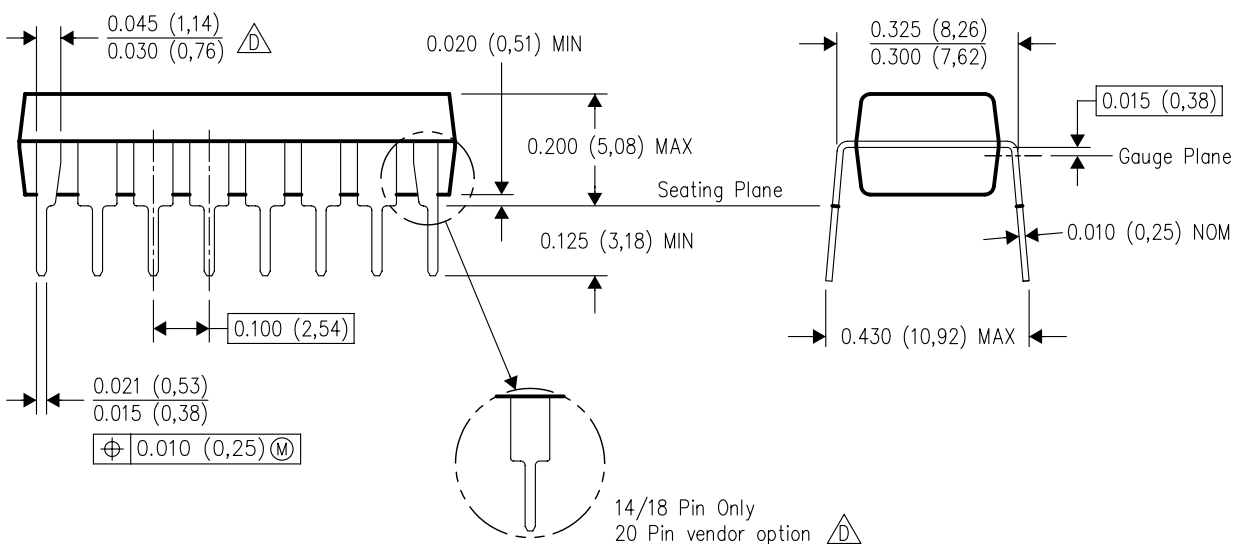
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

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