SN74LVC1G66 シングル双方向アナログ スイッチ

1 特長

- テキサス・インスツルメンツの NanoFree™ パッケージで提供
- 1.65V～5.5V の V_{CC} で動作
- 5.5V までの入力許容電圧
- 最大 t_{pd} 0.8ns (3.3V 時)
- 高いオン / オフ出力電圧比
- 高度な線形性
- 高速、標準値 0.5ns (V_{CC} = 3V、C_L = 50pF)
- 低オン状態抵抗、標準値約 5.5Ω (V_{CC} = 4.5V)
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を超える ESD 保護
  - 2000V、人体モデル (A114-A)
  - 200V、マシン モデル(A115-A)
  - 1000V、デバイス帯電モデル (C101)

2 アプリケーション

- ワイヤレス デバイス
- オーディオおよびビデオ信号のルーティング
- ポータブル コンピュータ
- ウェアラブル デバイス
- 信号ゲーティング、チョッピング、変調または復調 (モデム)
- アナログ / デジタル (A/D) およびデジタル / アナログ (D/A) 変換システム用の信号多重化

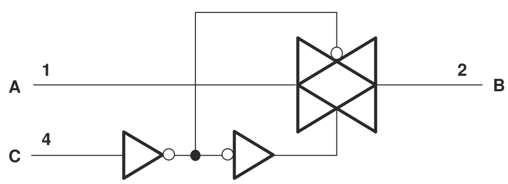
3 説明

SN74LVC1G66 はシングル双方向アナログ スイッチで、1.65V ～ 5.5V の V_{CC} で動作するよう設計され、アナログ信号とデジタル信号の両方をサポートします。SN74LVC1G66 は、最大 5.5V (ピーク) の振幅で信号を双方向伝送できます。ダイをパッケージとして使用し、IC パッケージの概念の大幅な進歩を象徴する NanoFree パッケージ技術を採用しています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
SN74LVC1G66DBV	DBV (SOT-23、5)	2.90mm × 2.80mm
SN74LVC1G66DCK	DCK (SC70、5)	2.00mm × 2.10mm
SN74LVC1G66DRL	DRL (SOT、5)	1.60mm × 1.60mm
SN74LVC1G66DRY	DRY (SON、6)	1.45mm × 1.00mm
SN74LVC1G66YZP	YZP (DSBGA、5)	1.39mm × 0.89mm
SN74LVC1G66DSF	DSF (SON、6)	1.00mm × 1.00 mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンを含みます。



論理図 (正論理)

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4 Pin Configuration and Functions

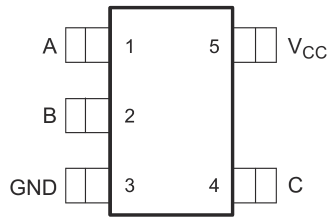


図 4-1. DBV Package 5-Pin SOT-23 (Top View)

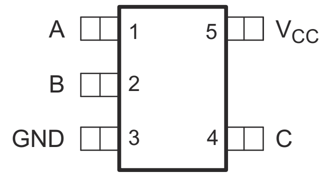


図 4-2. DCK Package 5-Pin SC70 (Top View)

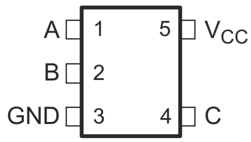


図 4-3. DRL Package 5-Pin SOT (Top View)

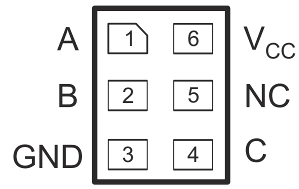


図 4-4. DSF Package 6-Pin X2SON (Top View)

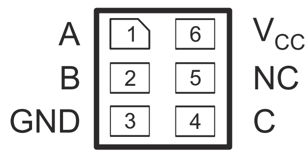


図 4-5. DRY Package 6-Pin USON (Top View)

Pin Functions

PIN			Type(1)	DESCRIPTION
NAME	SOT NO.	USON, X2SON NO.		
A	1	1	I/O	Bidirectional signal to be switched
B	2	2	I/O	Bidirectional signal to be switched
C	4	4	I	Controls the switch (L = OFF, H = ON)
GND	3	3	—	Ground pin
NC	—	5	—	Do not connect
V_{CC}	5	6	—	Power pin

(1) I = input; O = output; I/O = input or output

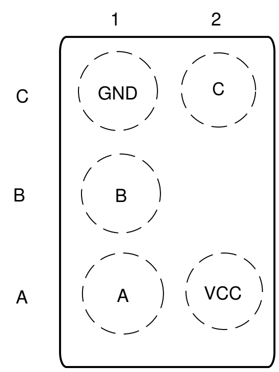


図 4-6. YZP Package 5-Pin DSBGA (BottomView)

Pin Functions

PIN		Type(1)	DESCRIPTION
NAME	DSBGA NO.		
A	A1	I/O	Bidirectional signal to be switched
B	B1	I/O	Bidirectional signal to be switched
C	C2	I	Controls the switch (L = OFF, H = ON)
GND	C1	—	Ground pin
V_{CC}	A2	—	Power pin

(1) I = input; O = output; I/O = input or output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage[(2)]		–0.5	6	V
V_I	Input voltage[(2) (3)]		–0.5	6	V
$V_{I/O}$	Switch I/O voltage[(2) (3) (4)]		–0.5	V_{CC} + 0.5	V
I_{IK}	Control input clamp current	$V_I < 0$		–50	mA
I_{IOK}	I/O port diode current	$V_{I/O} < 0$ or $V_{I/O} > V_{CC}$		±50	mA
I_T	ON-state switch current	$V_{I/O} < 0$ to V_{CC}		±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage Temperature		–65	150	°C
T_j	Junction Temperature			150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5V maximum.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	+2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	+1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
$V_{I/O}$	I/O port voltage.		0	V_{CC}	V
V_{IH}	High-level input voltage, control input	V_{CC} = 1.65V to 1.95V	V_{CC} × 0.65		V
		V_{CC} = 2.3V to 2.7V	V_{CC} × 0.7		
		V_{CC} = 3V to 3.6V	V_{CC} × 0.7		
		V_{CC} = 4.5V to 5.5V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage, control input	V_{CC} = 1.65V to 1.95V		V_{CC} × 0.35	V
		V_{CC} = 2.3V to 2.7V		V_{CC} × 0.3	
		V_{CC} = 3V to 3.6V		V_{CC} × 0.3	
		V_{CC} = 4.5V to 5.5V		V_{CC} × 0.3	
V_I	Control input voltage		0	5.5	V
Δt/Δv	Control input transition rise and fall time	V_{CC} = 1.65V to 1.95V		20	ns/V
		V_{CC} = 2.3V to 2.7V		20	
		V_{CC} = 3V to 3.6V		10	
		V_{CC} = 4.5V to 5.5V		10	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to provide proper device operation. See also, the *Implications of Slow or Floating CMOS Inputs* application note.

5.4 Thermal Information

THERMAL METRIC[1]		SN74LVC1G66						UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT)	DRY (USON)	DSF (X2SON)	YZP (DSBGA)	
		5 PINS	5 PINS	5 PINS	6 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	262	313	142	355	348	132	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	198	203	—	250	215	—	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	142	195	—	222	211	—	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	123	120	—	78	35	—	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	142	194	—	221	210	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
r_{on}	ON-state switch resistance	$V_I = V_{CC}$ or GND, $V_C = V_{IH}$ (see 図 6-1 and 図 5-1)	I_S = 4mA	1.65V		12	30	Ω
			I_S = 8mA	2.3V		9	20	
			I_S = 24mA	3V		7.5	15	
			I_S = 32mA	4.5V		5.5	10	
$r_{on(p)}$	Peak on resistance	$V_I = V_{CC}$ to GND, $V_C = V_{IH}$ (see 図 6-1 and 図 5-1)	I_S = 4mA	1.65V		125	200	Ω
			I_S = 8mA	2.3V		35	60	
			I_S = 24mA	3V		11.5	25	
			I_S = 32mA	4.5V		7.5	15	
$I_{S(off)}$	OFF-state switch leakage current	$V_I = V_{CC}$ and V_O = GND or V_I = GND and $V_O = V_{CC}$, $V_C = V_{IL}$ (see 図 6-2)		5.5V			±1	μA
			T_A = 25°C				±0.1	
$I_{S(on)}$	ON-state switch leakage current	$V_I = V_{CC}$ or GND, $V_C = V_{IH}$, V_O = Open (see 図 6-3)		5.5V			±1	μA
			T_A = 25°C				±0.1	
I_I	Control input current	$V_C = V_{CC}$ or GND		5.5V			±1	μA
			T_A = 25°C				±0.1	
I_{CC}	Supply current	$V_C = V_{CC}$ or GND		5.5V			10	μA
			T_A = 25°C				1	
ΔI_{CC}	Supply current change	$V_C = V_{CC}$ – 0.6V		5.5V			500	μA
C_{ic}	Control input capacitance			5V		2		pF
$C_{io(off)}$	Switch input and output capacitance			5V		6		pF
$C_{io(on)}$	Switch input and output capacitance			5V		15		pF

(1) T_A = 25°C

5.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see 図 6-4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		V_{CC} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd} (1)	A or B	B or A		2.2		1.2		0.8		0.6	ns
t_{en} (2)	C	A or B	2.5	12	1.9	6.5	1.8	5	1.5	4.2	ns
t_{dis} (3)	C	A or B	2.2	11.5	1.4	6.9	2	6.5	1.4	6	ns

(1) t_{PLH} and t_{PHL} are the same as t_{pd}. The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
(2) t_{PZL} and t_{PZH} are the same as t_{en}.
(3) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

5.7 Analog Switch Characteristics

T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response[(1)] (switch ON)	A or B	B or A	C_L = 50pF, R_L = 600Ω, f_{in} = sine wave (see 図 6-5)	1.65V	35	MHz
				2.3V	120	
				3V	175	
				4.5V	195	
			C_L = 5pF, R_L = 50Ω, f_{in} = sine wave (see 図 6-5)	1.65V	>300	
				2.3V	>300	
				3V	>300	
				4.5V	>300	
Crosstalk (control input to signal output)	C	A or B	C_L = 50pF, R_L = 600Ω, f_{in} = 1MHz (square wave) (see 図 6-6)	1.65V	35	mV
				2.3V	50	
				3V	70	
				4.5V	100	
Feedthrough attenuation[(2)] (switch OFF)	A or B	B or A	C_L = 50pF, R_L = 600Ω, f_{in} = 1MHz (sine wave) (see 図 6-7)	1.65V	–58	dB
				2.3V	–58	
				3V	–58	
				4.5V	–58	
			C_L = 5pF, R_L = 50Ω, f_{in} = 1MHz (sine wave) (see 図 6-7)	1.65V	–42	
				2.3V	–42	
				3V	–42	
				4.5V	–42	
Sine-wave distortion	A or B	B or A	C_L = 50pF, R_L = 10kΩ, f_{in} = 1kHz (sine wave) (see 図 6-8)	1.65V	0.5%	
				2.3V	0.025%	
				3V	0.015%	
				4.5V	0.01%	
			C_L = 50pF, R_L = 10kΩ, f_{in} = 10kHz (sine wave) (see 図 6-8)	1.65V	0.15%	
				2.3V	0.025%	
				3V	0.015%	
				4.5V	0.01%	

(1) Adjust f_{in} voltage to obtain 0dBm at output. Increase f_{in} frequency untildB meter reads –3dB.
(2) Adjust f_{in} voltage to obtain 0dBm at input.

5.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8V	V_{CC} = 2.5V	V_{CC} = 3.3V	V_{CC} = 5V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10MHz	8	9	9	11	pF

5.9 Typical Characteristics

T_A = 25°C

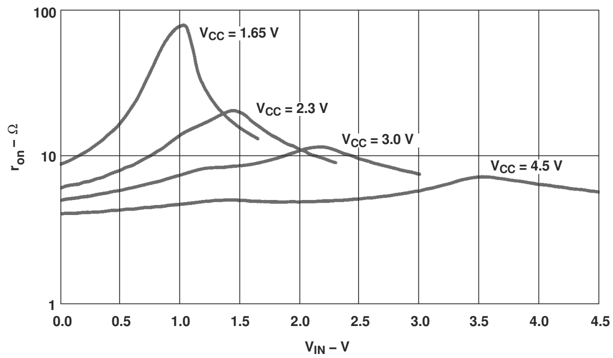


図 5-1. Typical r_{on} as a Function of Input Voltage (V_I) for V_I = 0 to V_{CC}

6 Parameter Measurement Information

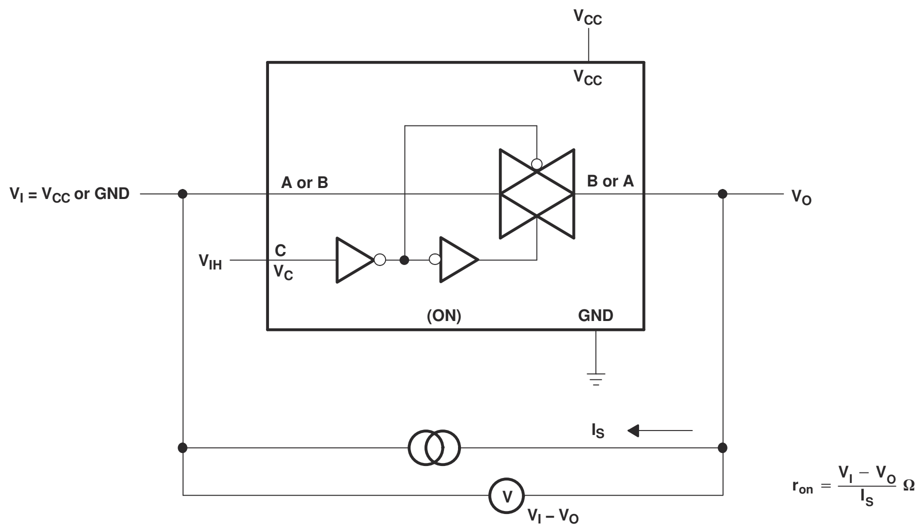


図 6-1. ON-State Resistance Test Circuit

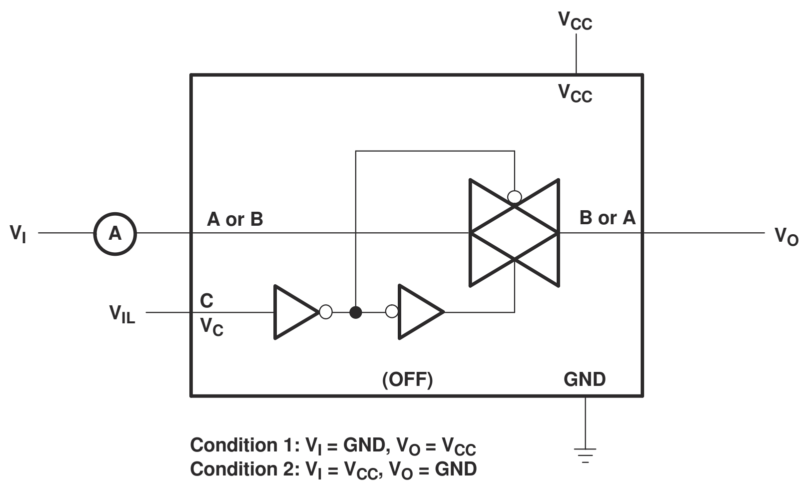


図 6-2. OFF-State Switch Leakage-Current Test Circuit

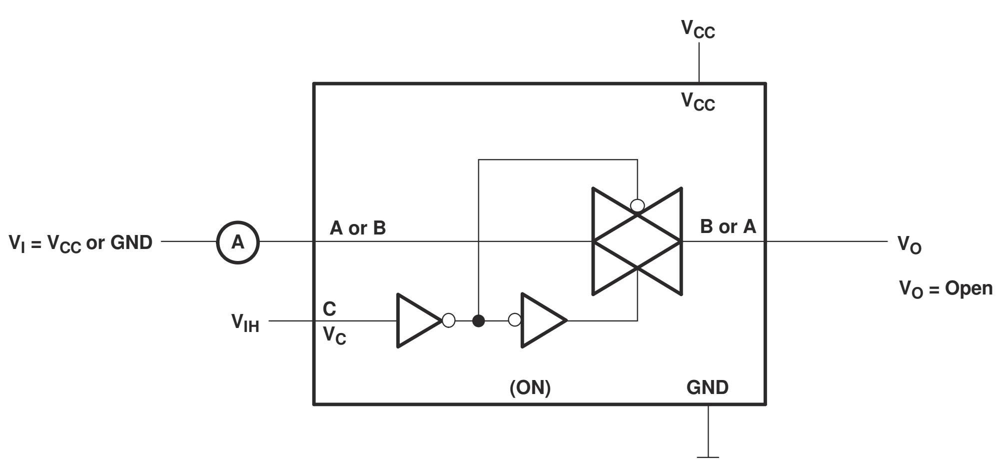
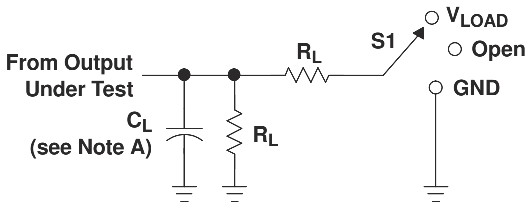


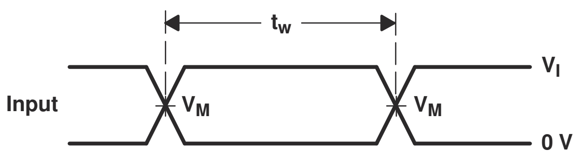
図 6-3. ON-State Switch Leakage-Current Test Circuit



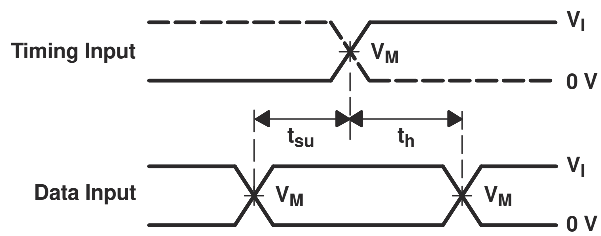
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

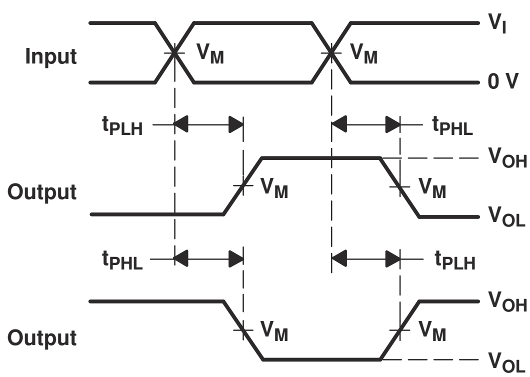
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



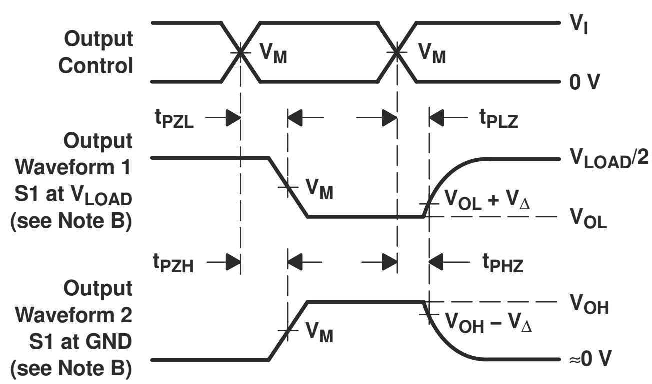
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

図 6-4. Load Circuit and Voltage Waveforms

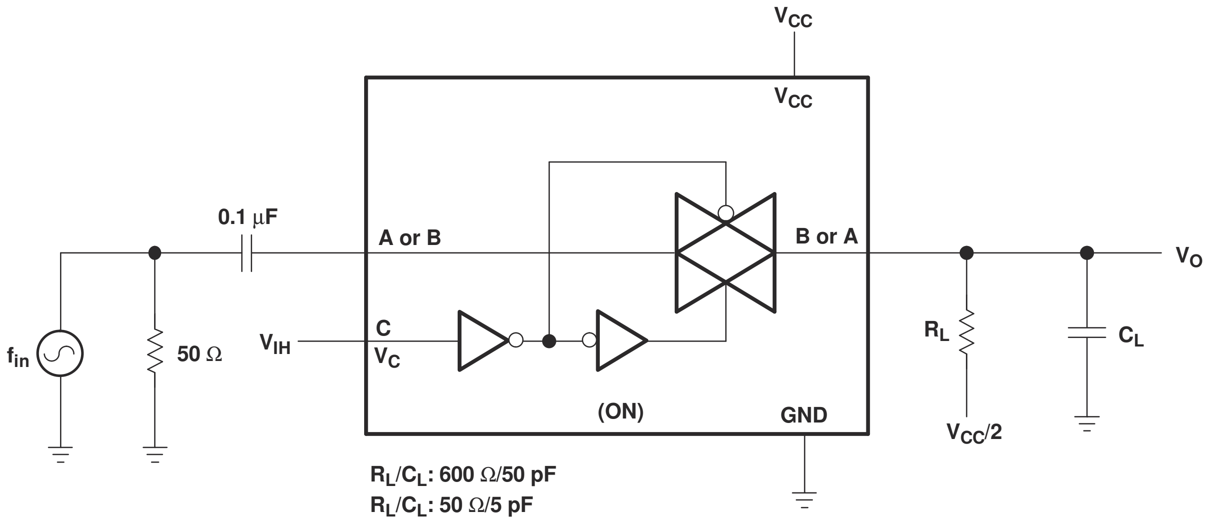


図 6-5. Frequency Response (Switch ON)

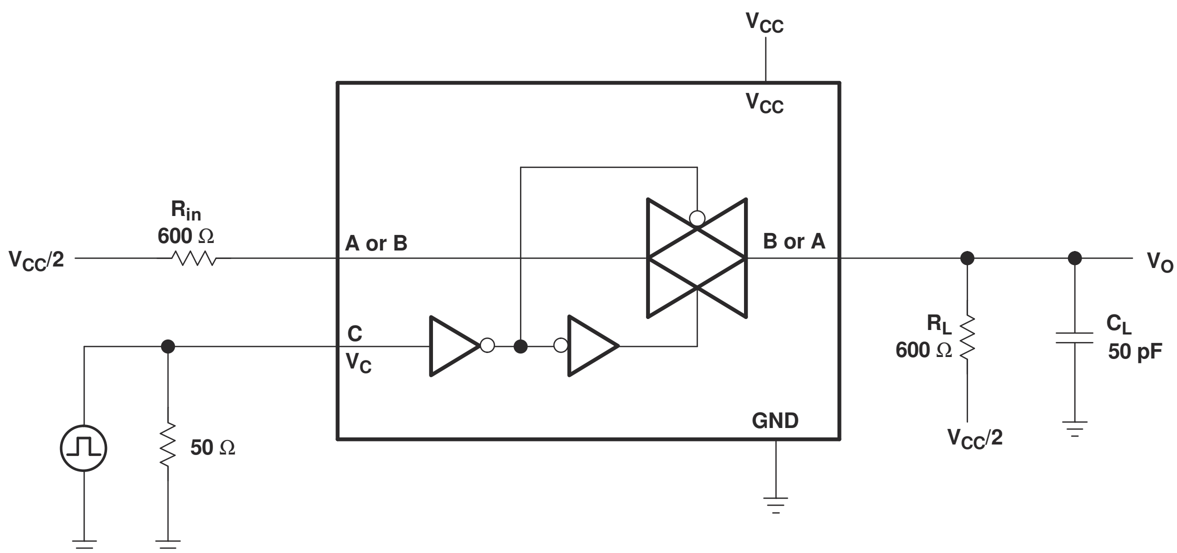


図 6-6. Crosstalk (Control Input – Switch Output)

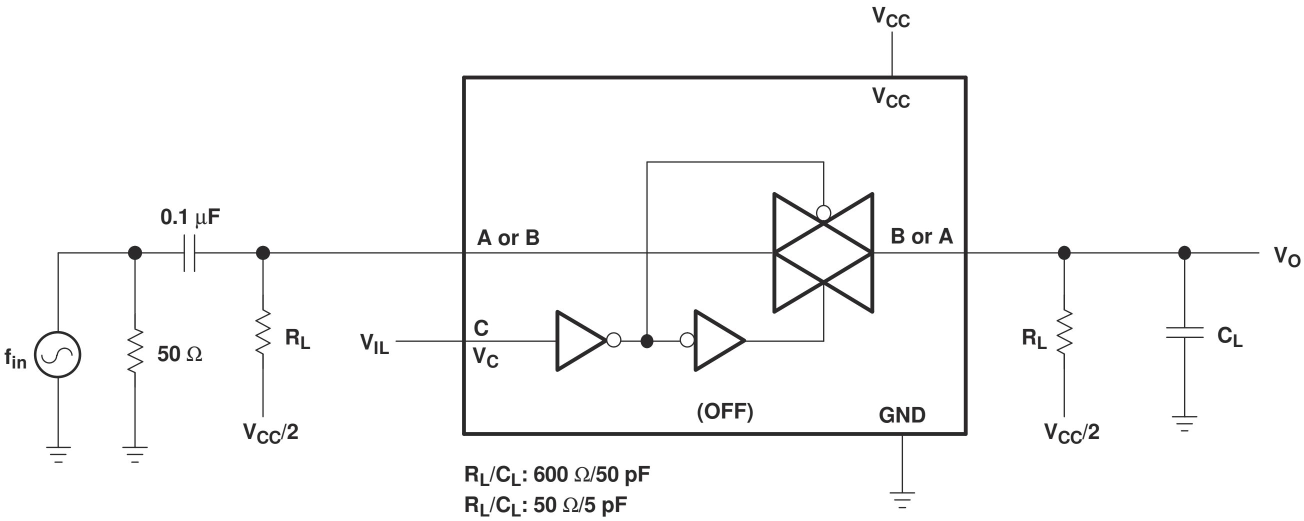


図 6-7. Feedthrough (Switch OFF)

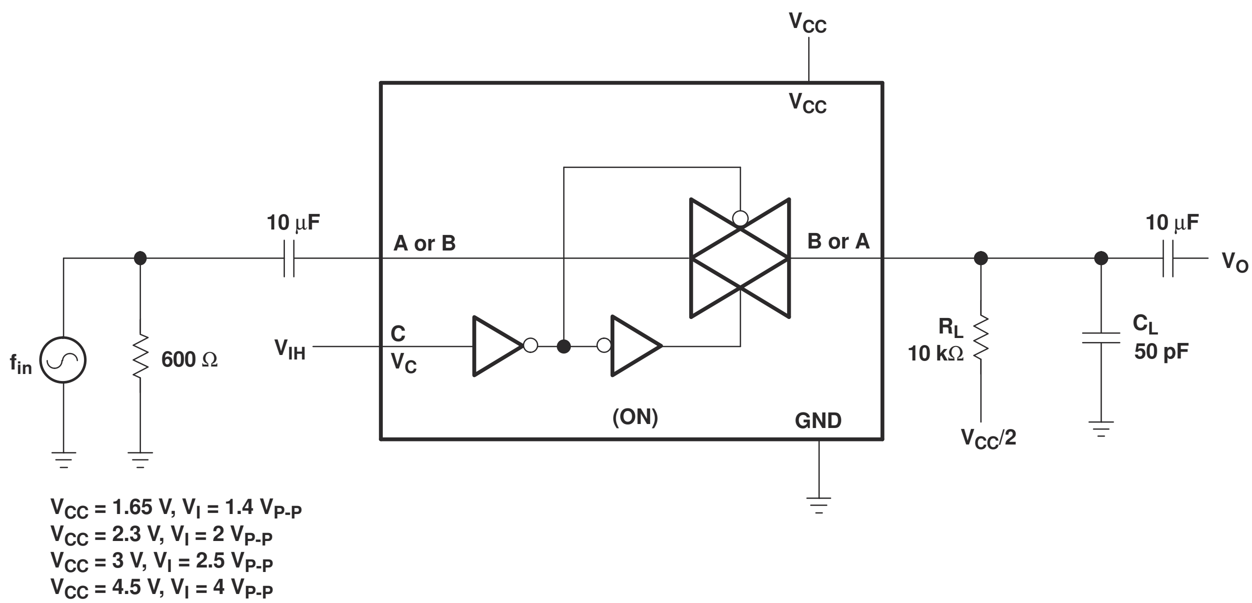


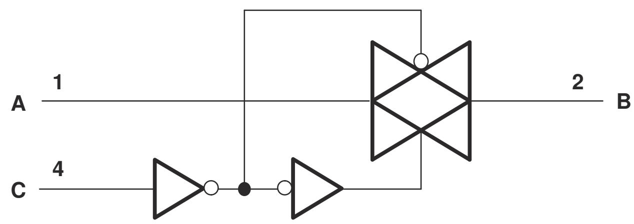
図 6-8. Sine-Wave Distortion

7 Detailed Description

7.1 Overview

The SN74LVC1G66 single, bilateral analog switch is designed for 1.65V to 5.5V V_{CC} operation, and supports both analog and digital signals. SN74LVC1G66 permits bidirectional transmission of signals with amplitudes of up to 5.5V (peak). By using the die as the package, NanoFree package technology represents a significant advancement in IC packaging concepts.

7.2 Functional Block Diagram



Logic Diagram (Positive Logic)

7.3 Feature Description

The TI NanoFree package is one of TI's smallest packages, which enables customers to save board space. The solder bumps enable easy testing. The SN74LVC1G66 has a wide V_{CC} range, enabling rail-to-rail operation of signals anywhere from a 1.8V to a 5V system. In addition, the control input (C Pin) tolerates up to 5.5V, enabling higher-voltage logic to interface to the switch control system.

7.4 Device Functional Modes

表 7-1. Function Table

CONTROL INPUT (C)	SWITCH
L	OFF
H	ON

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SN74LVC1G66 can be used in any application where an SPST switch is used and a solid-state, voltage-controlled version is preferred.

8.2 Typical Application

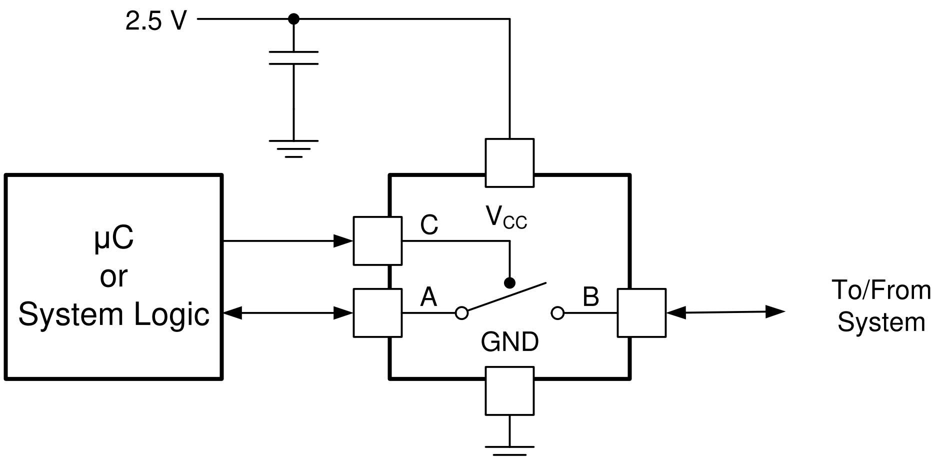


図 8-1. Typical Application Schematic

8.2.1 Design Requirements

The SN74LVC1G66 enables on and off control of analog and digital signals with a digital control signal. All input signals must remain between 0V and V_{CC} for optimal operation.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specifications, see Δt/Δv in *セクション 5.3*.
   - For specified high and low levels, see V_{IH} and V_{IL} in *セクション 5.3*.
   - Inputs and outputs are overvoltage tolerant allowing them to go as high as 5.5V at any valid V_{CC}.
2. Recommended Output Conditions:
   - Load currents must not exceed ±50mA.
3. Frequency Selection Criterion:
   - Maximum frequency tested is 150MHz.
   - Added trace resistance/capacitance can reduce maximum frequency capability; use layout practices as directed in *セクション 8.4*.

8.2.3 Application Curve

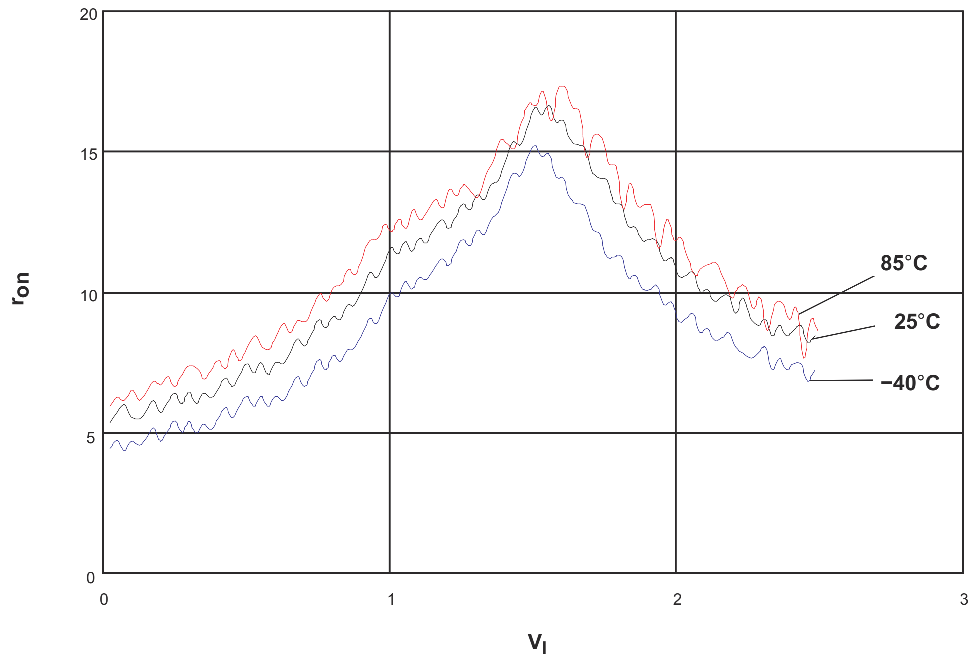


図 8-2. r_{on} vsV_I,V_{CC} = 2.5V (SN74LVC1G66)

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *セクション 5.3*.

Each V_{CC} terminal must have a bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1µF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01µF or 0.022µF capacitor is recommended for each V_{CC} because the V_{CC} pins are connected internally. For devices with dual supply pins operating at different voltages (for example V_{CC} and V_{DD}), a 0.1µF bypass capacitor is recommended for each supply pin. Having parallel multiple bypass capacitors is acceptable to reject different frequencies of noise. 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant a separate discussion. When a PCB trace turns a corner at a 90 degree angle, a reflection can occur. This occurs primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times the width. This upsets the transmission line characteristics — especially the distributed capacitance and self–inductance of the trace — resulting in the reflection.

注

Not all PCB traces can be straight, and so can require turning corners. 図 8-3 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

8.4.2 Layout Example

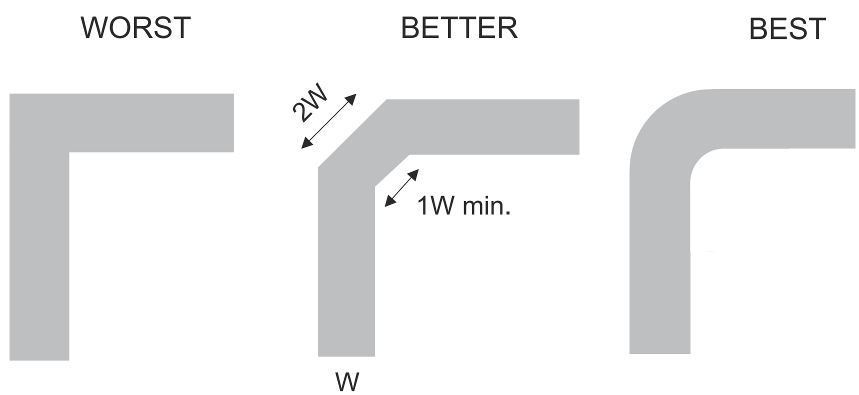


図 8-3. Trace Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

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9.6 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision Q (March 2017) to Revision R (June 2025) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 ... 1
- Updated Thermal Information ... 6
- Updated resistance range in セクション 5.5 ... 7
- Updated switching timing in セクション 5.6 ... 7
- Updated Sine-wave distortion in セクション 5.7 ... 8
- Added *Receiving Notifications of Documentation Updates*, *Support Resources*, *Electrostatic Discharge Caution*, and *Glossary* the sections ... 18

Changes from Revision P (March 2016) to Revision Q (March 2017) **Page**

- Changed the YZP package pin out graphic ... 4

Changes from Revision O (March 2015) to Revision P (March 2016) **Page**

- Added Junction temperature specification to *Absolute Maximum Ratings* table ... 5
- Added "Control" to "Input transition rise and fall time" in *Recommended Operating Conditions* table ... 6

Changes from Revision N (December 2012) to Revision O (March 2015) **Page**

- 「*ピン構成および機能*」セクション、「*ESD 定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1
- 「注文情報」表を削除 ... 1
- 「*デバイス情報*」表を追加 ... 1

Changes from Revision M (January 2012) to Revision N (December 2012) **Page**

- 「*注文情報*」表にジャンボ リールを追加 ... 1

Changes from Revision L (January 2007) to Revision M (January 2012) **Page**

- Added DSF and DRY package to pin out graphic ... 3

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G66DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(C665, C66J, C66R, C66T)
SN74LVC1G66DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(C665, C66J, C66R, C66T)
SN74LVC1G66DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(C665, C66J, C66R, C66T)
SN74LVC1G66DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(C65, C6F, C6J, C6 K, C6O, C6R, C 6T)
SN74LVC1G66DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C65, C6F, C6J, C6 K, C6O, C6R, C 6T)
SN74LVC1G66DCKR.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C65, C6F, C6J, C6 K, C6O, C6R, C 6T)
SN74LVC1G66DRLR	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(C67, C6R)
SN74LVC1G66DRLR.A	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(C67, C6R)
SN74LVC1G66DRLR.B	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(C67, C6R)
SN74LVC1G66DRYR	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C6
SN74LVC1G66DRYR.A	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C6
SN74LVC1G66DRYR.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C6
SN74LVC1G66DSFR	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C6
SN74LVC1G66DSFR.A	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C6
SN74LVC1G66DSFR.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C6
SN74LVC1G66YZPR	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C6N
SN74LVC1G66YZPR.B	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C6N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G66 :

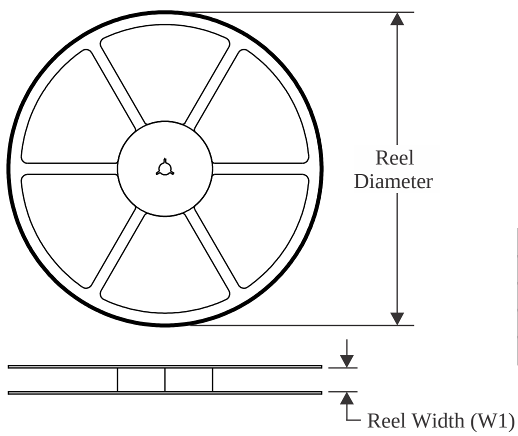
- Automotive : SN74LVC1G66-Q1

NOTE: Qualified Version Definitions:

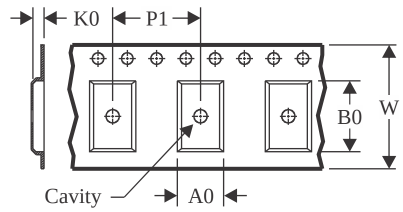
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

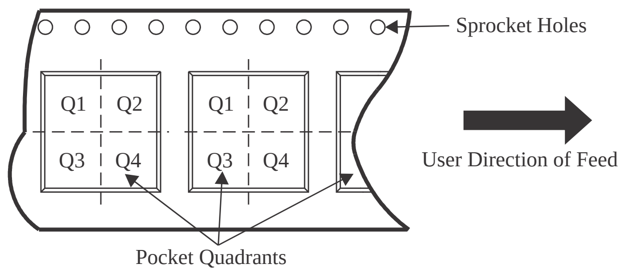


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

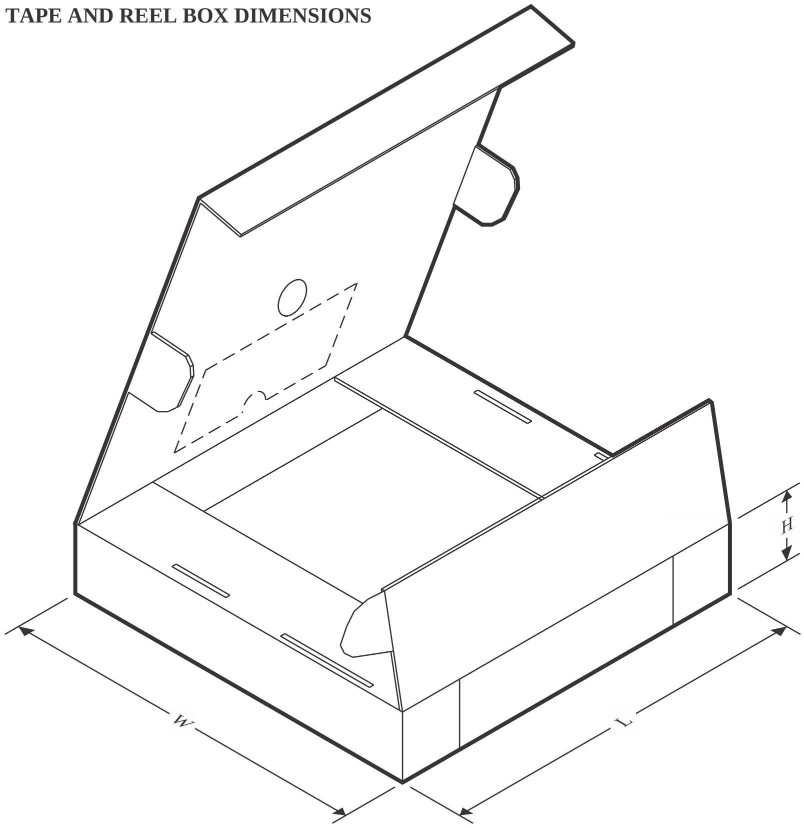
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G66DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G66DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G66DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G66DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G66DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G66DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G66DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G66DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G66YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



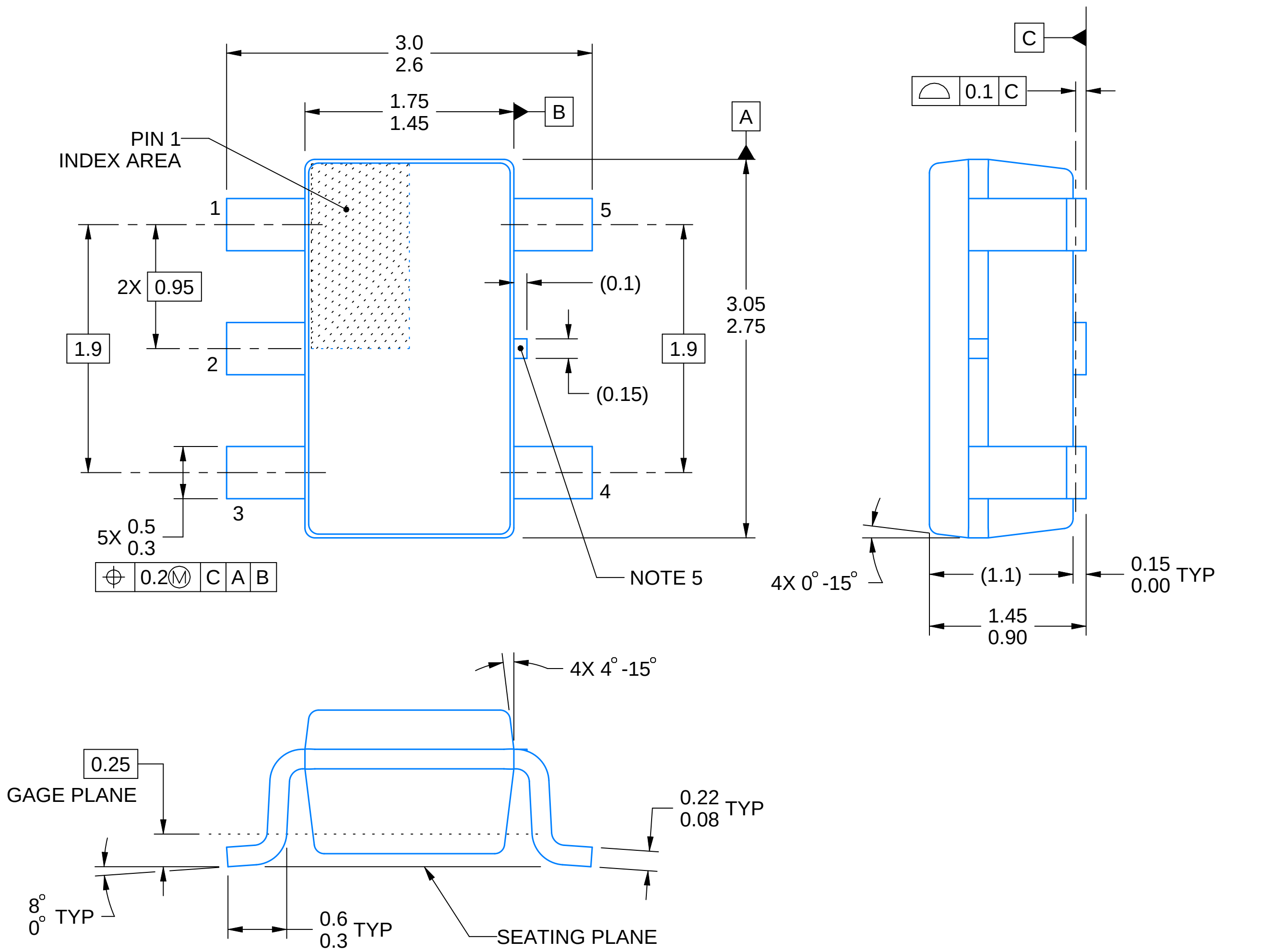
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G66DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74LVC1G66DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74LVC1G66DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G66DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74LVC1G66DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G66DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G66DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G66DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74LVC1G66YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

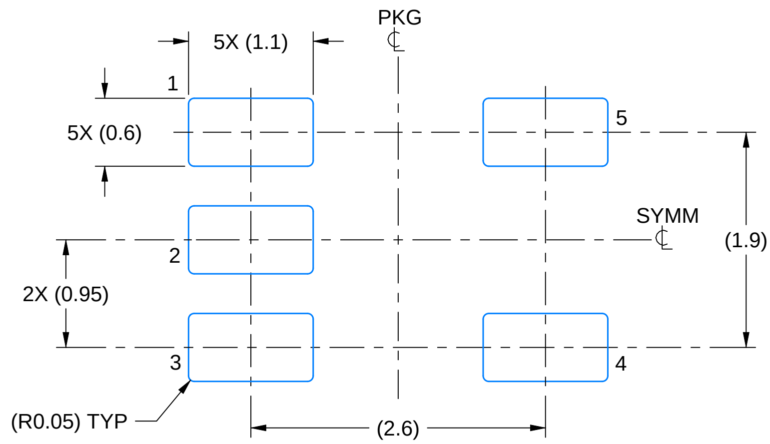
SMALL OUTLINE TRANSISTOR



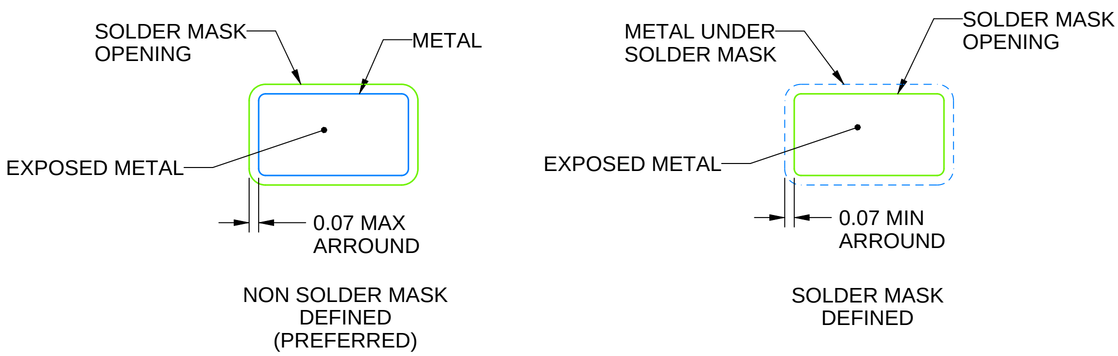
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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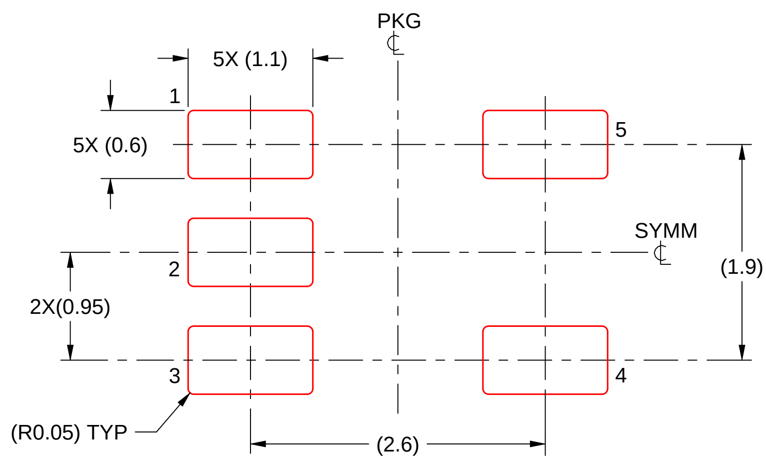
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



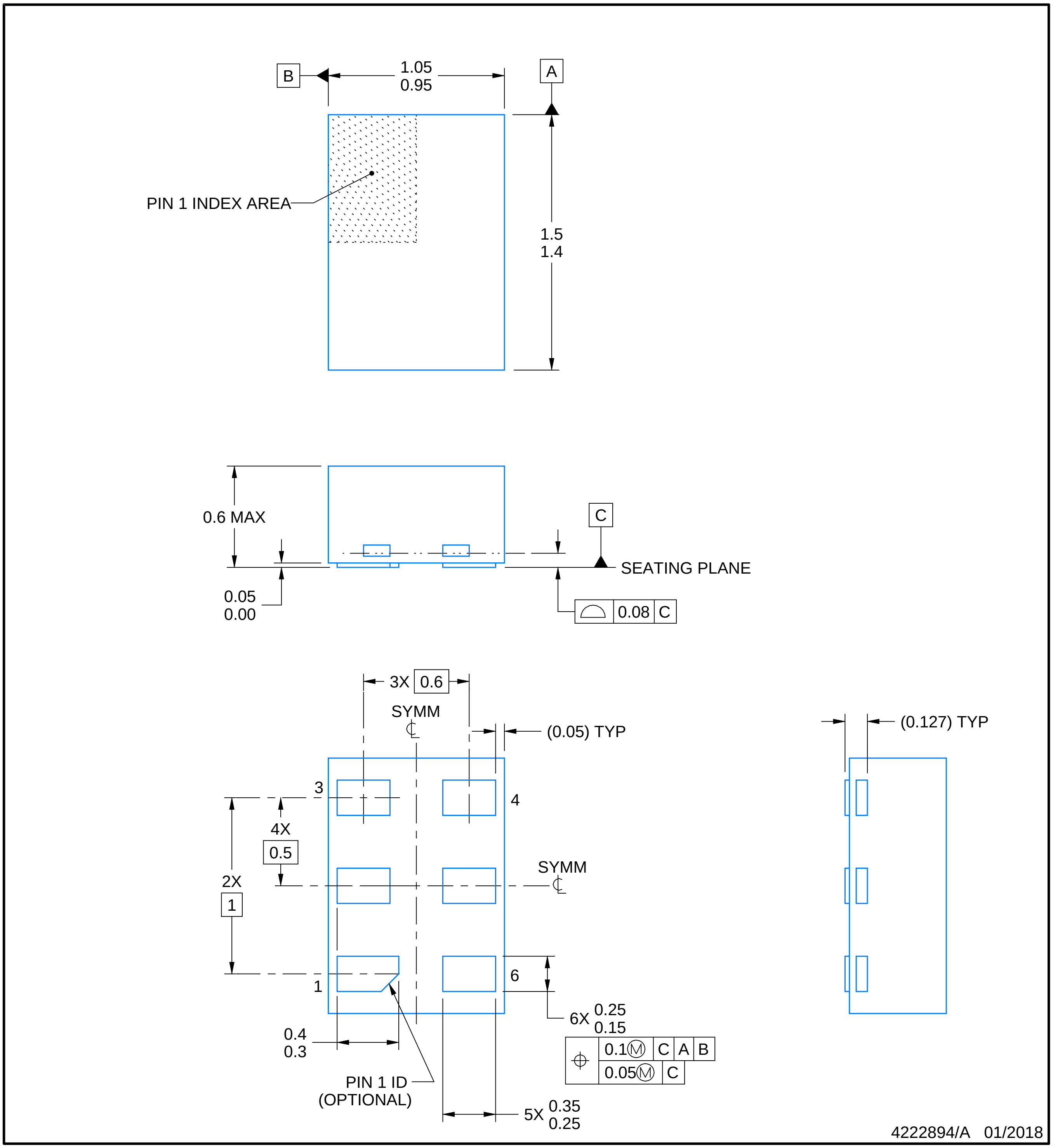
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

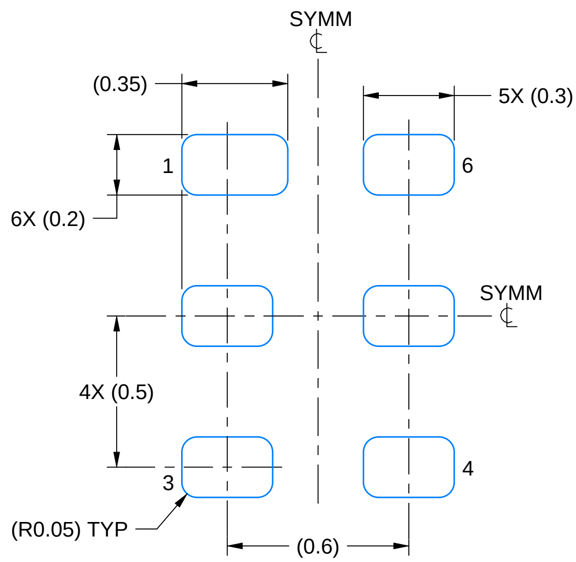
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

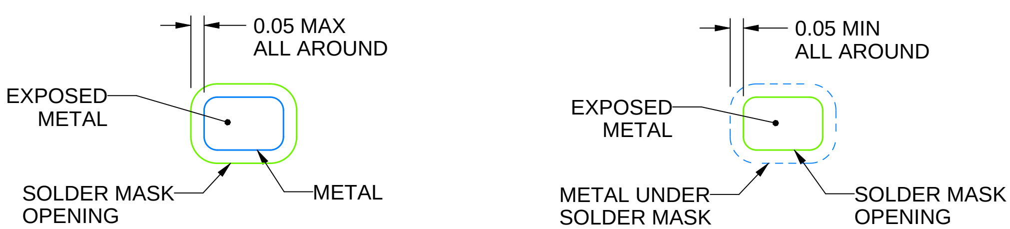


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X

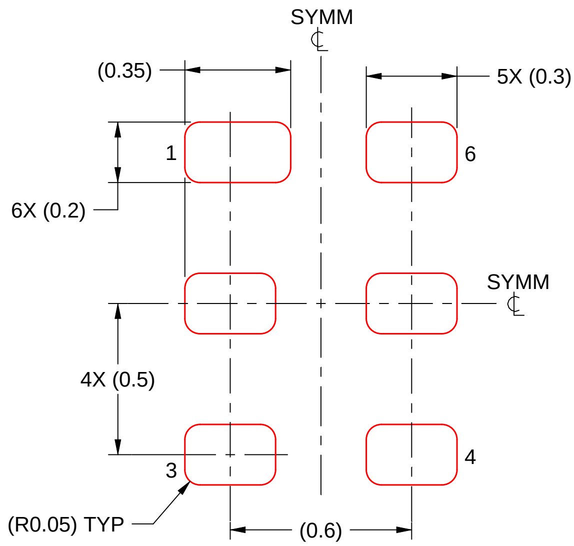


SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

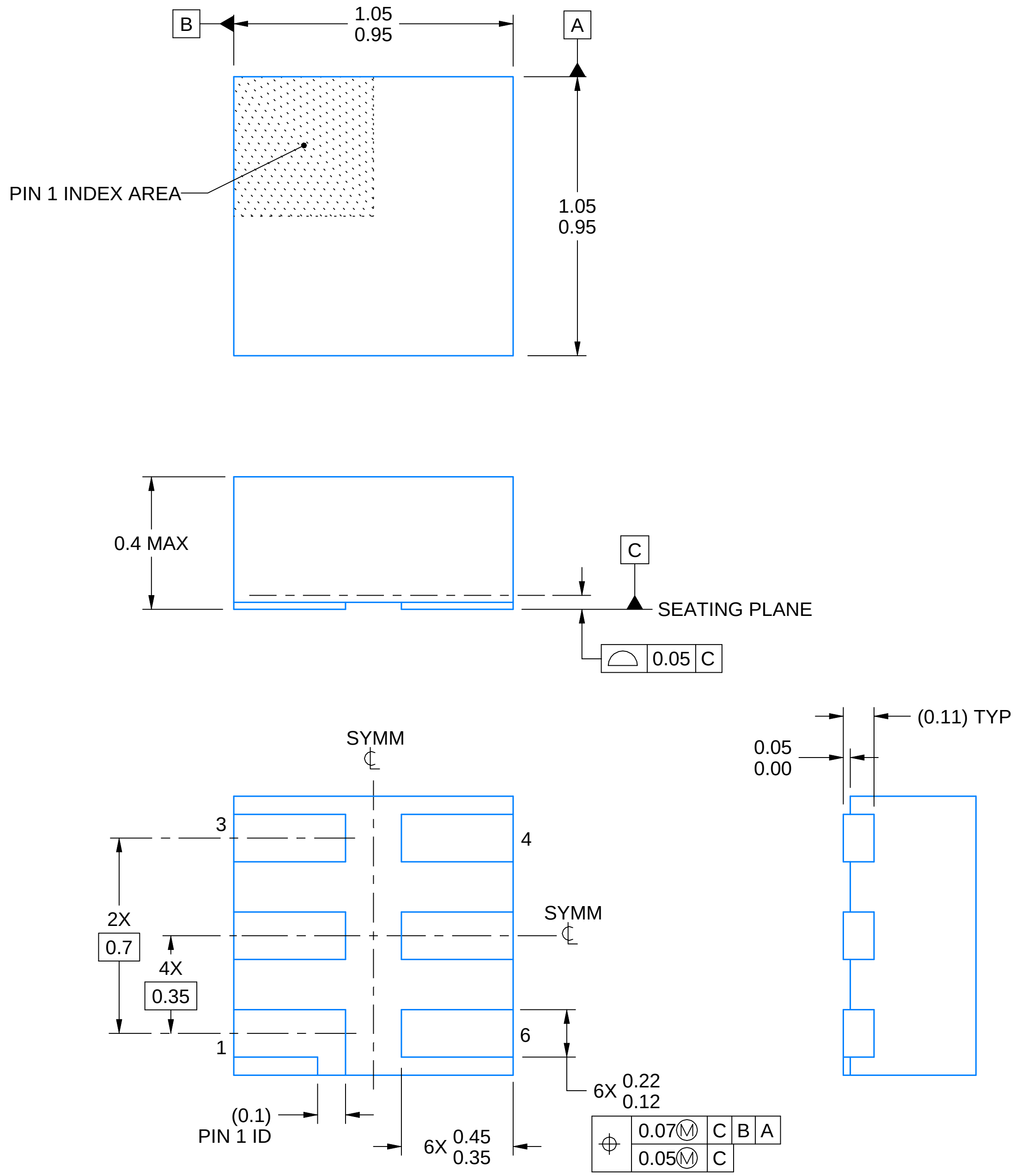


SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

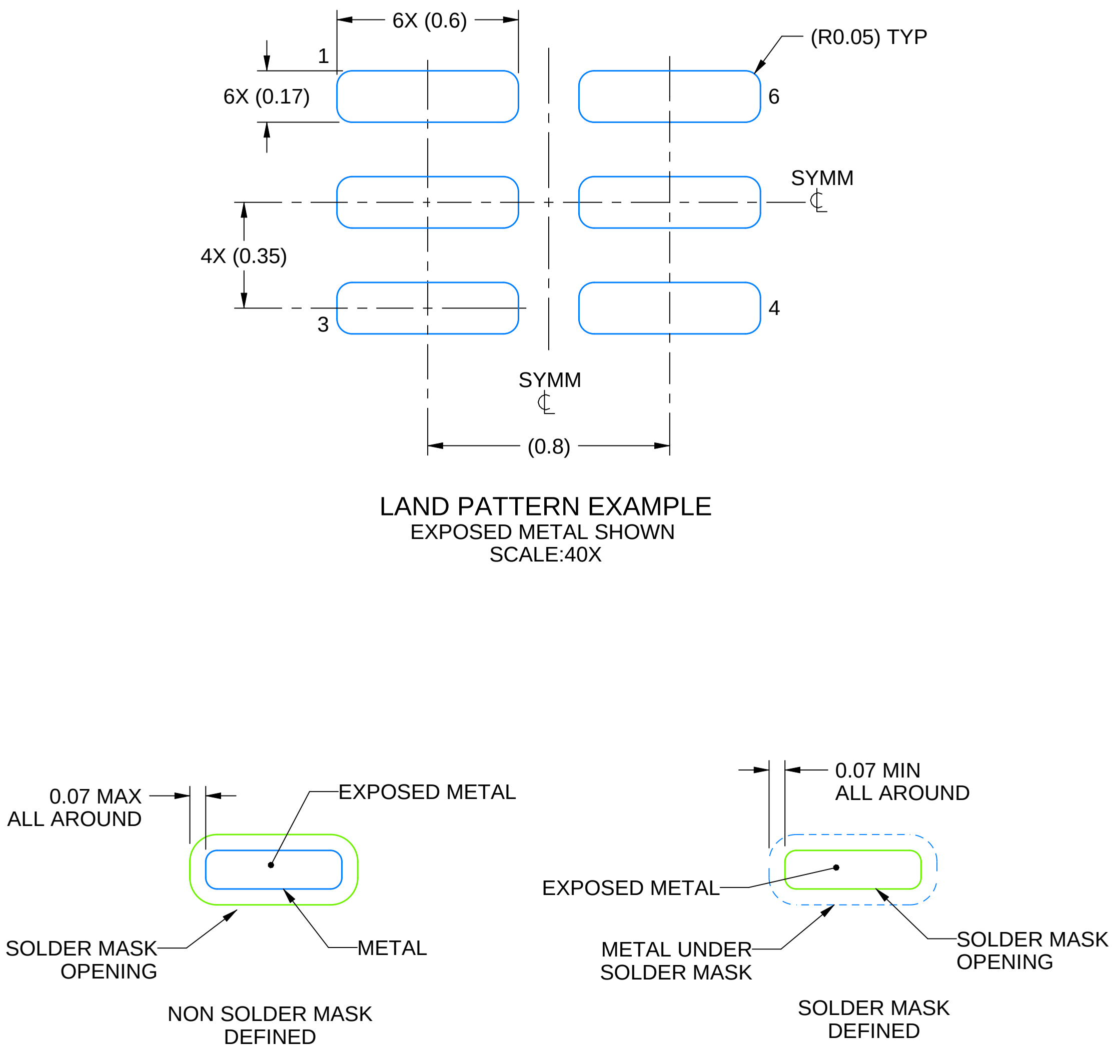
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



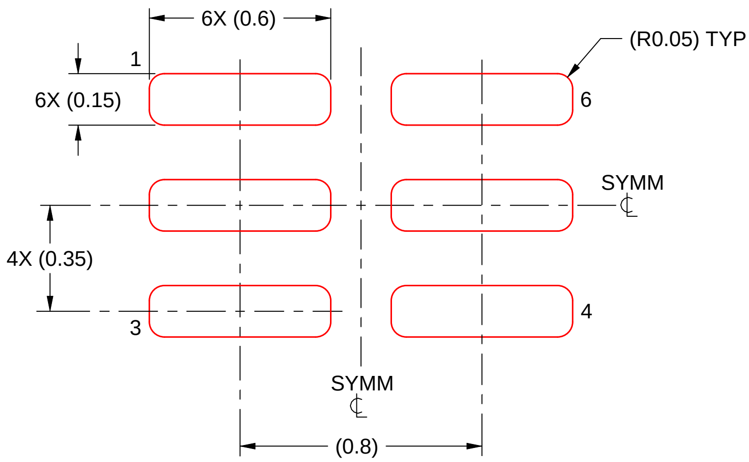
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X

SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

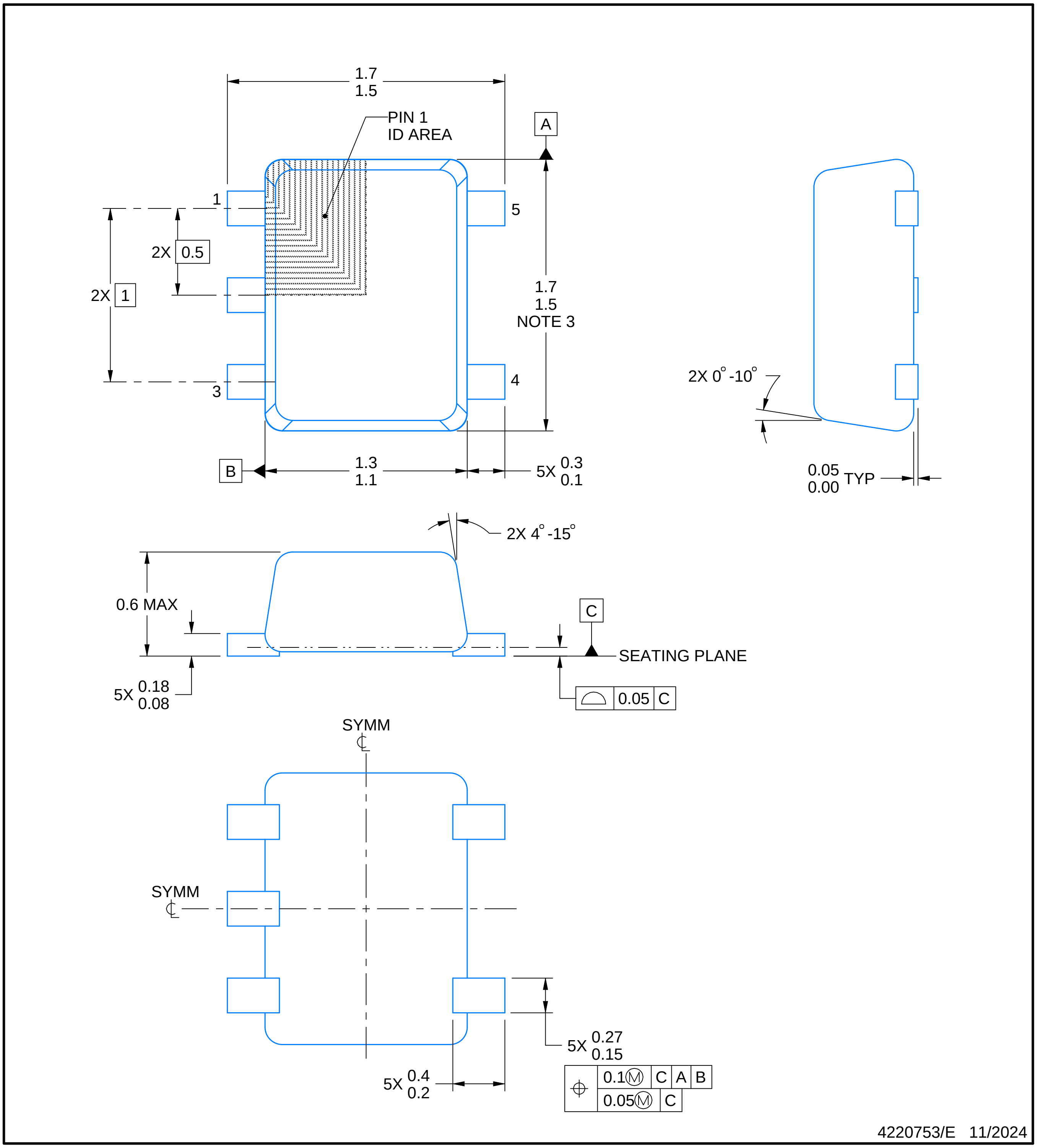


SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

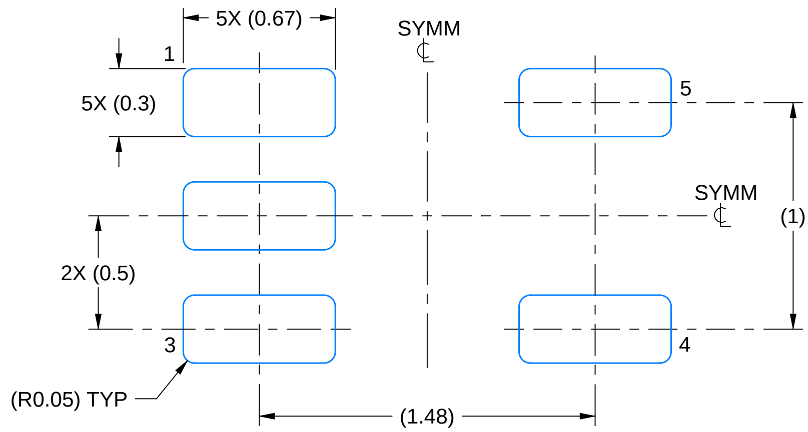
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



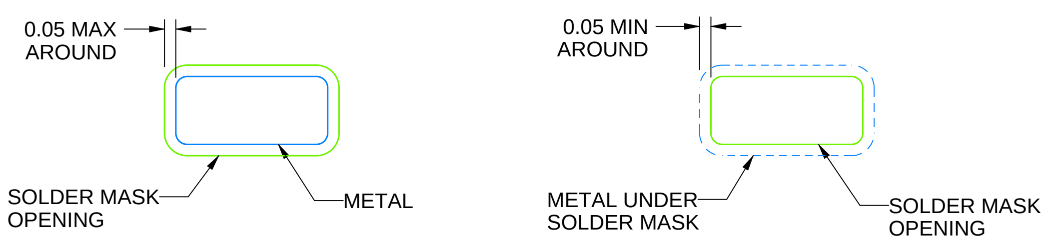
4220753/E 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1



LAND PATTERN EXAMPLE
SCALE:30X



NON SOLDER MASK
DEFINED
(PREFERRED)

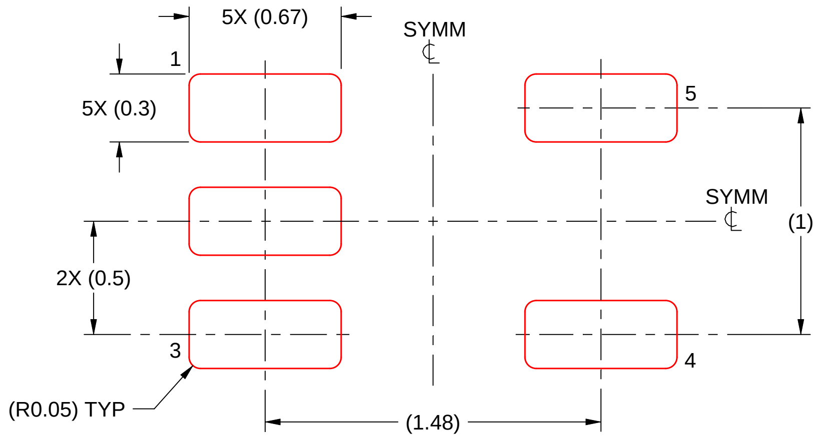
SOLDER MASK
DEFINED

SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

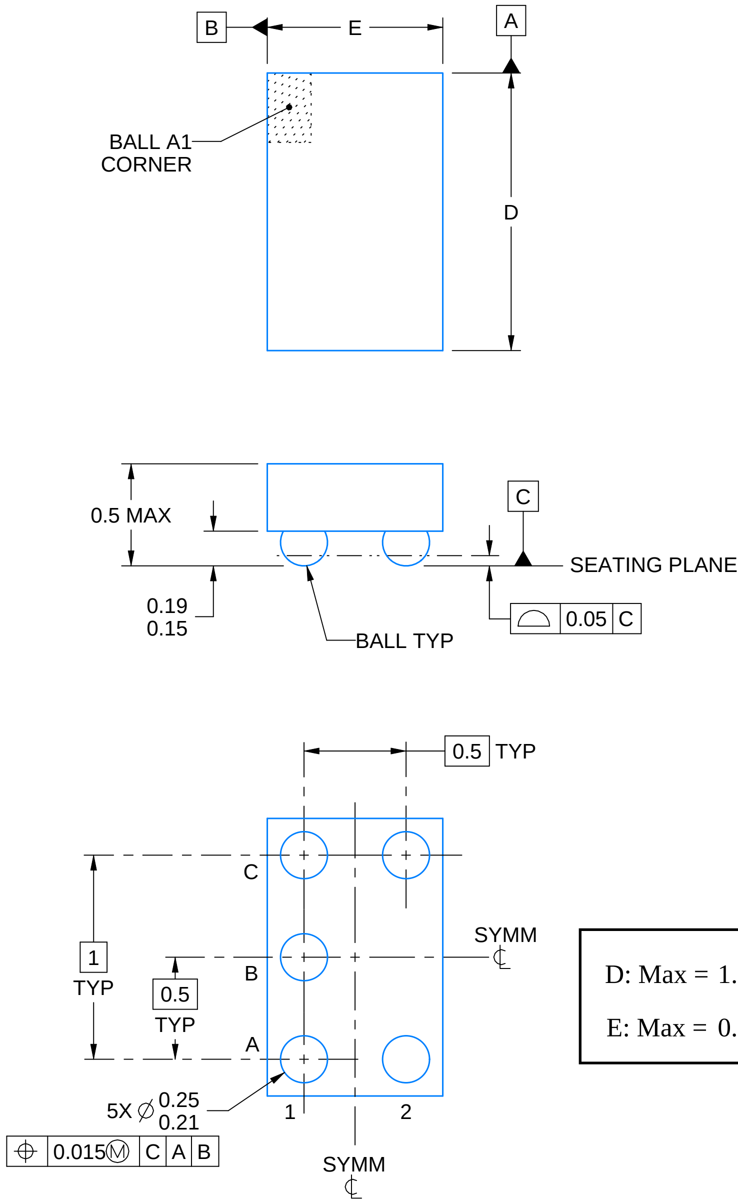
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

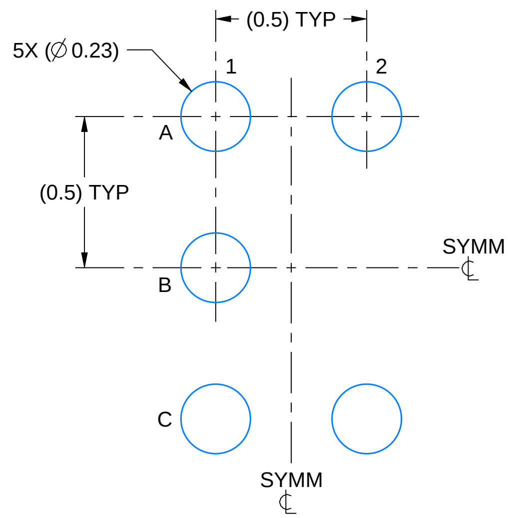


D: Max =	1.418 mm, Min =1.358 mm
E: Max =	0.918 mm, Min =0.858 mm

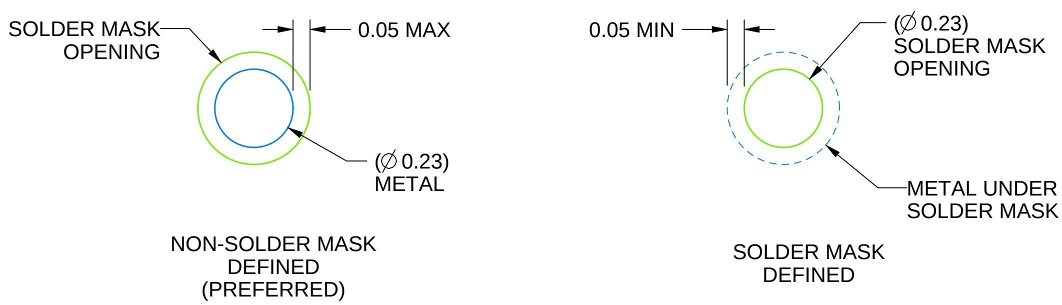
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

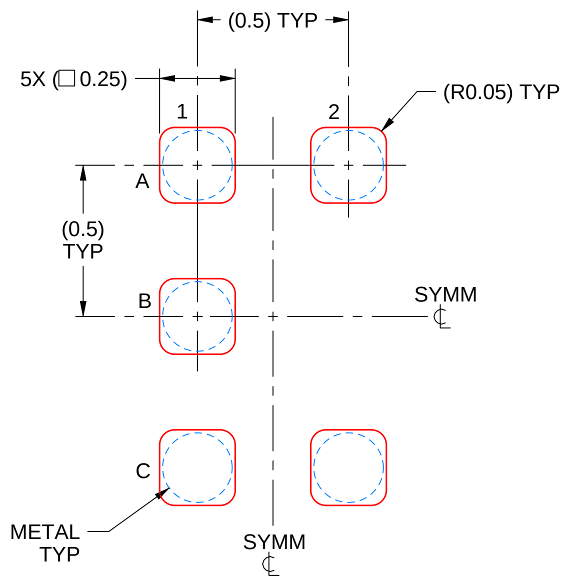


SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

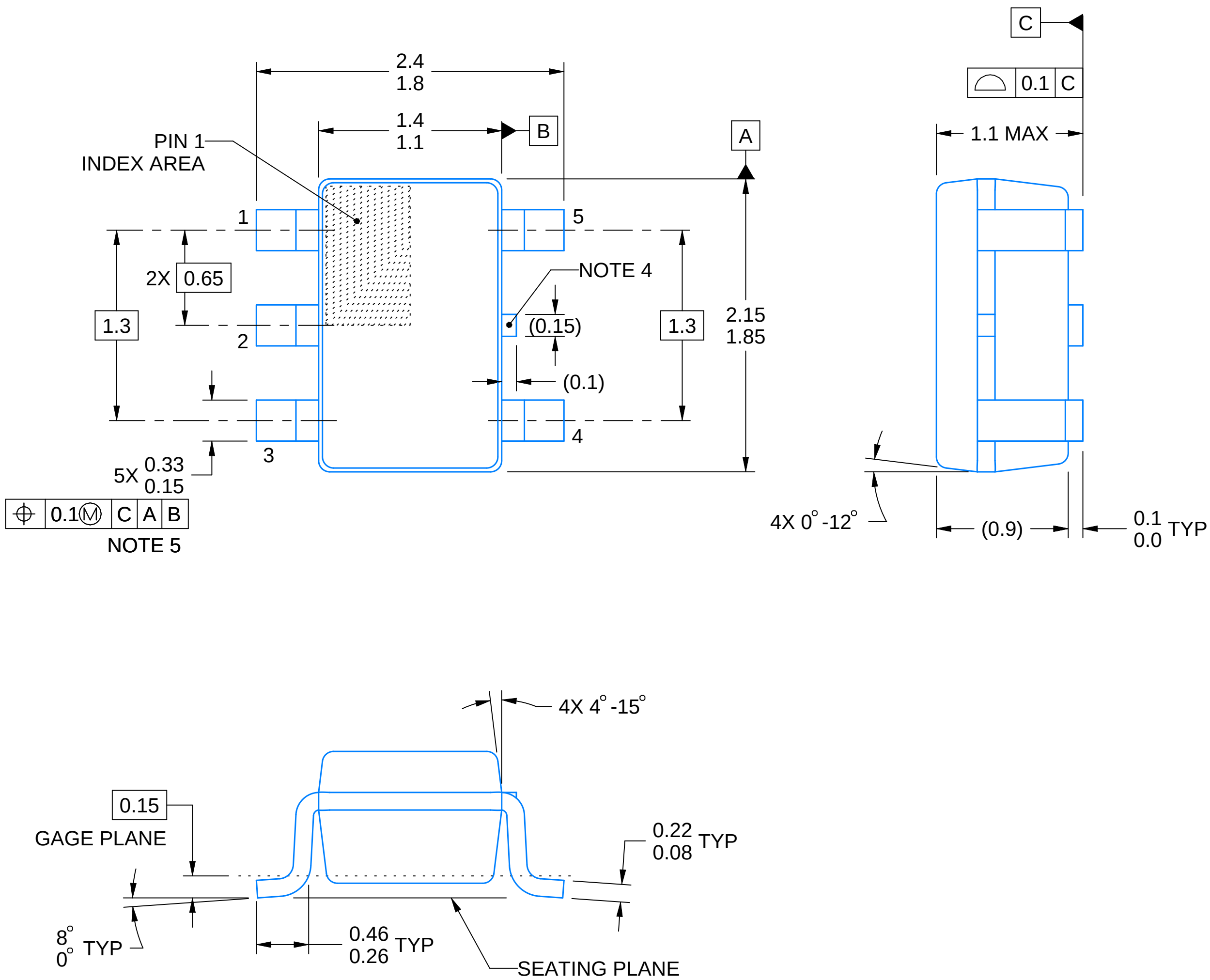


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

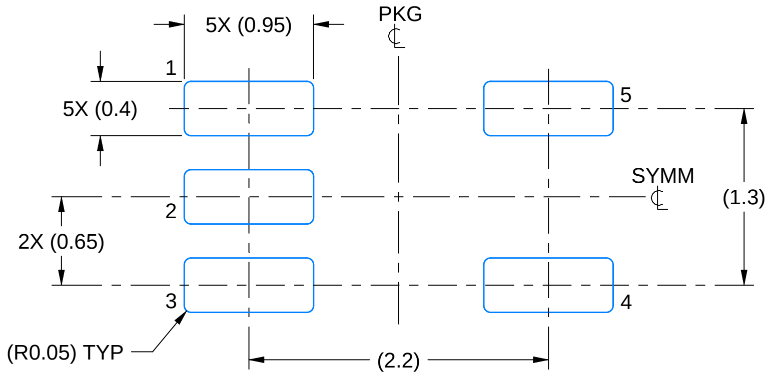
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



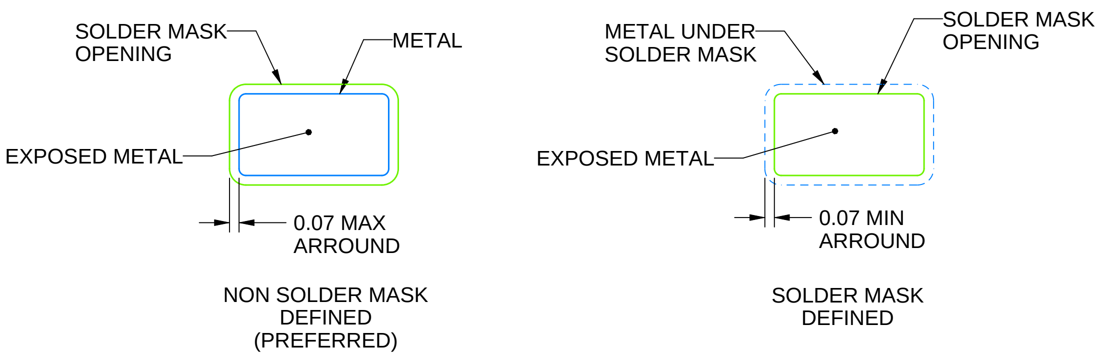
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

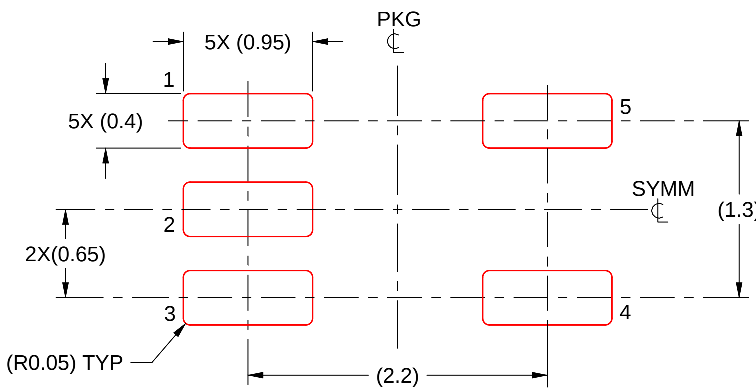


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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