SN74LVC1T45 1 ビット デュアル電源バス トランシーバ、可変電圧変換設定、3 ステート出力

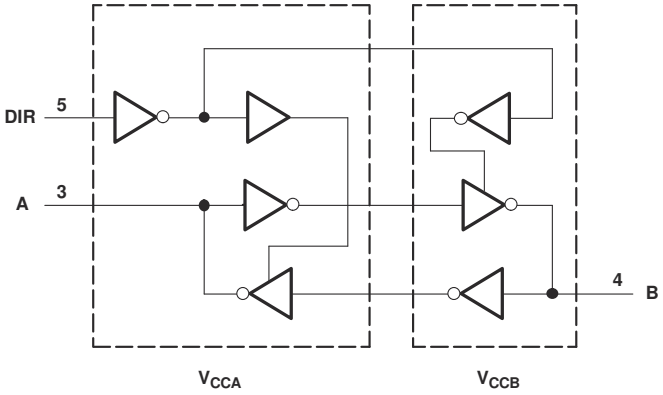
1 特長

- JESD 22 を上回る ESD 保護:
  - 2000V、人体モデル (A114-A)
  - 200V、マシン モデル(A115-A)
  - 1000V、デバイス帯電モデル (C101)
- テキサス・インスツルメンツの NanoFree™ パッケージで供給
- 完全に構成可能なデュアル レール設計により、1.65V ～5.5V の電源電圧の全範囲にわたって各ポートが動作可能
- V_{CC} 絶縁機能:いずれかの V_{CC} 入力が GND レベルになると、両方のポートがハイ インピーダンス状態に移行
- V_{CCA} を基準とする DIR 入力回路
- 低い消費電力、I_{CC} 最大値 4µA
- 3.3V で ±24mA の出力駆動能力
- I_{off} により部分的パワーダウン モードでの動作をサポート
- 最大データ レート
  - 420Mbps (3.3V から 5V への変換)
  - 210Mbps (3.3V への変換)
  - 140Mbps (2.5V への変換)
  - 75Mbps (1.8V への変換)
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能

2 アプリケーション

- パーソナル・エレクトロニクス
- 産業用
- エンタープライズ
- テレコム

機能ブロック図



3 概要

この 1 ビット非反転バス トランシーバは、設定可能な 2 本の独立した電源レールを使用します。A ポートは V_{CCA} に追従するように設計されています。V_{CCA} ピンには、1.65V ～5.5V の電源電圧を入力できます。B ポートは、V_{CCB} に追従する設計になっています。V_{CCB} ピンには、1.65V～5.5V の電源電圧を入力できます。これにより、1.8V、2.5V、3.3V、5V の任意の電圧ノード間での低電圧双方向変換が可能です。

SN74LVC1T45 は、2 つのデータ バス間の非同期通信用に設計されています。方向制御 (DIR) 入力のロジック レベルにより、B ポート出力と A ポート出力のどちらかがアクティブになります。本デバイスは、B ポート出力をアクティブにした場合、A バスから B バスにデータを送信し、A ポート出力をアクティブにした場合、B バスから A バスにデータを送信します。A ポートと B ポートの両方の入力回路は常にアクティブであるため、I_{CC} と I_{CCZ} が過剰に流れないようにロジック High または Low レベルを印加する必要があります。

SN74LVC1T45 は、DIR 入力が V_{CCA} によって給電されるように設計されています。このデバイスは、I_{off} を使用する部分的パワーダウン アプリケーション用の動作が完全に規定されています。I_{off} 回路で出力をディセーブルすることにより、電源切断時にデバイスに電流が逆流して損傷するのを回避できます。V_{CC} 絶縁機能は、いずれかの V_{CC} 入力が GND レベルになると、両方のポートがハイ インピーダンス状態になるよう設計されています。

ダイをパッケージとして使用する NanoFree™ パッケージ技術は、IC パッケージの概念を大きく覆すものです。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
SN74LVC1T45	DRL (SOT、6)	1.6mm × 1.6mm
	DBV (SOT-23、6)	2.9mm × 2.8mm
	DCK (SC70、6)	2mm × 2.1mm
	DPK (USON、6)	1.6mm × 1.6mm
	YZP (DSBGA、6)	1mm × 0.5mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

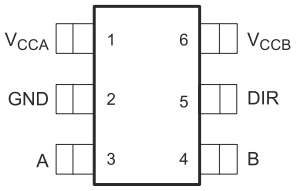


図 4-1. DBV Package, 6-Pin SOT-23 (Top View)

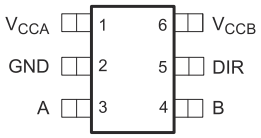


図 4-2. DCK Package, 6-Pin SC70 (Top View)

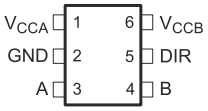


図 4-3. DRL Package, 6-Pin SOT (Top View)

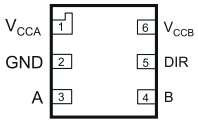


図 4-4. DPK Package, 6-Pin USON (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	DBV, DCK, DRL, DPK		
V_{CCA}	1	P	SYSTEM-1 supply voltage (1.65V to 5.5V)
GND	2	G	Device GND
A	3	I/O	Output level depends on V_{CC1} voltage.
B	4	I/O	Input threshold value depends on V_{CC2} voltage.
DIR	5	I	GND (low level) determines B-port to A-port direction.
V_{CCB}	6	P	SYSTEM-2 supply voltage (1.65V to 5.5V)

(1) P = power, G = ground, I/O = input and output, I = input

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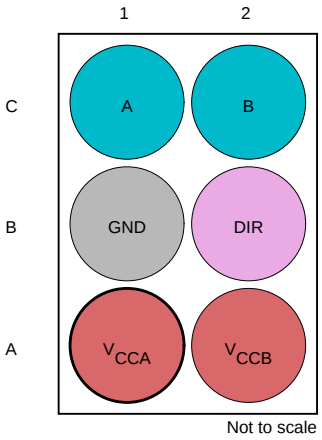


図 4-5. YZP Package, 6-Pin DSBGA (Bottom View)

Legend	
Power	Input
Input or Output	Ground

表 4-2. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
A1	V_{CCA}	P	SYSTEM-1 supply voltage (1.65V to 5.5V)
A2	V_{CCB}	P	SYSTEM-2 supply voltage (1.65V to 5.5V)
B1	GND	G	Device GND
B2	DIR	I	GND (low level) determines B-port to A-port direction.
C1	A	I/O	Output level depends on V_{CC1} voltage.
C2	B	I/O	Input threshold value depends on V_{CC2} voltage.

(1) P = power, G = ground, I/O = input and output, I = input

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage		–0.5	6.5	V
V_I	Input voltage(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine Model	±200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

See (1) (2) (3)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.65	5.5	V
V_{CCB}					1.65	5.5	
V_{IH}	High-level input voltage	Data inputs(4)	1.65 o 1.95V		V_{CCI} × 0.65		V
			2.3 to 2.7V		1.7		
			3 to 3.6V		2		
			4.5 to 5.5V		V_{CCI} × 0.7		
V_{IL}	Low-level input voltage	Data inputs(4)	1.65 o 1.95V			V_{CCI} × 0.35	V
			2.3 to 2.7V			0.7	
			3 to 3.6V			0.8	
			4.5 to 5.5V			V_{CCI} × 0.3	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})(5)	1.65 to 1.95V		V_{CCA} × 0.65		V
			2.3 to 2.7V		1.7		
			3 to 3.6V		2		
			4.5 to 5.5V		V_{CCA} × 0.7		

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5.3 Recommended Operating Conditions (続き)

See (1) (2) (3)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})(5)	1.65 to 1.95V			V_{CCA} × 0.35	V
			2.3 to 2.7V			0.7	
			3 to 3.6V			0.8	
			4.5 to 5.5V			V_{CCA} × 0.3	
V_I	Input voltage				0	5.5	V
V_O	Output voltage				0	V_{CCO}	V
I_{OH}	High-level output current			1.65 to 1.95V		–4	mA
				2.3 to 2.7V		–8	
				3 to 3.6V		–24	
				4.5 to 5.5V		–32	
I_{OL}	Low-level output current			1.65 to 1.95V		4	mA
				2.3 to 2.7V		8	
				3 to 3.6V		24	
				4.5 to 5.5V		32	
Δt/Δv	Input transition rise or fall rate	Data inputs	1.65 to 1.95V			20	ns/V
			2.3 to 2.7V			20	
			3 to 3.6V			10	
			4.5 to 5.5V			5	
		Control inputs	1.65 to 5.5V			5	
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs* , SCBA004.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7V, V_{IL} max = V_{CCI} × 0.3V.
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7V, V_{IL} max = V_{CCA} × 0.3V.

5.4 Thermal Information

THERMAL METRIC(1)		SN74LVC1T45					UNIT
		DBV (SOT-23)	DCK (SC70)	DPK (USON)	DRL (SOT)	YZP (DSBGA)	
		6 PINS					
$R_{\theta JA}$	Junction-to-ambient thermal resistance	215.1	210.9	278.3	223.7	131.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	136.5	139.2	133.4	88.7	1.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	96.6	72	174.1	58.4	22.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	71.5	54.9	23.4	5.9	5.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	96.3	71.7	173.5	58.1	22.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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5.5 Electrical Characteristics

over recommended operating free-air temperature range, T_A = –40 to +85°C (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}		MIN	TYP	MAX	UNIT
V_{OH}		I_{OH} = –100µA	$V_I = V_{IH}$	1.65 to 4.5V	1.65 to 4.5V		V_{CCO} – 0.1			V
		I_{OH} = –4mA		1.65V	1.65V		1.2			
		I_{OH} = –8mA		2.3V	2.3V		1.9			
		I_{OH} = –24mA		3V	3V		2.4			
		I_{OH} = –32mA		4.5V	4.5V		3.8			
V_{OL}		I_{OL} = 100µA	$V_I = V_{IL}$	1.65 to 4.5V	1.65 to 4.5V				0.1	V
		I_{OL} = 4mA		1.65V	1.65V				0.45	
		I_{OL} = 8mA		2.3V	2.3V				0.3	
		I_{OL} = 24mA		3V	3V				0.55	
		I_{OL} = 32mA		4.5V	4.5V				0.55	
I_I	DIR	$V_I = V_{CCA}$ or GND		1.65 to 5.5V	1.65 to 5.5V	T_A = 25 °C			±1	µA
						T_A = –40 to +85°C			±2	
I_{off}	A port	V_I or V_O = 0 to 5.5V		0V	0 to 5.5V	T_A = 25 °C			±1	µA
						T_A = –40 to +85°C			±2	
	B port			0 to 5.5V	0V	T_A = 25 °C			±1	
						T_A = –40 to +85°C			±2	
I_{OZ}	A or B port	$V_O = V_{CCO}$ or GND		1.65 to 5.5V	1.65 to 5.5V	T_A = 25 °C			±1	µA
						T_A = –40 to +85°C			±2	
I_{CCA}		$V_I = V_{CCI}$ or GND, I_O = 0		1.65 to 5.5V	1.65 to 5.5V				3	µA
				5.5V	0V				2	
				0V	5.5V				–2	
I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0		1.65 to 5.5V	1.65 to 5.5V				3	µA
				5.5V	0V				–2	
				0V	5.5V				2	
$I_{CCA} + I_{CCB}$ (see 表 7-1)		$V_I = V_{CCI}$ or GND, I_O = 0		1.65 to 5.5V	1.65 to 5.5V				4	µA
ΔI_{CCA}	A port	A port at V_{CCA} – 0.6V, DIR at V_{CCA}, B port = open		3 to 5.5V	3 to 5.5V				50	µA
	DIR	DIR at V_{CCA} – 0.6V, B port = open, A port at V_{CCA} or GND							50	
ΔI_{CCB}	B port	B port at V_{CCB} – 0.6V, DIR at GND, A port = open		3 to 5.5V	3 to 5.5V				50	µA
C_i	DIR	$V_I = V_{CCA}$ or GND		3.3V	3.3V	T_A = 25 °C		2.5		pF
C_{io}	A or B port	$V_O = V_{CCA/B}$ or GND		3.3V	3.3V	T_A = 25 °C		6		pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.

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5.6 Switching Characteristics (V_{CCA} = 1.8V ± 0.15V)

over recommended operating free-air temperature range, V_{CCA} = 1.8V ± 0.15V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ±0.15V		V_{CCB} = 2.5V ±0.2V		V_{CCB} = 3.3V ±0.3V		V_{CCB} = 5V ±0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3	17.7	2.2	10.3	1.7	8.3	1.4	7.2	ns
t_{PHL}			2.8	14.3	2.2	8.5	1.8	7.1	1.7	7	
t_{PLH}	B	A	3	17.7	2.3	16	2.1	15.5	1.9	15.1	ns
t_{PHL}			2.8	14.3	2.1	12.9	2	12.6	1.8	12.2	
t_{PHZ}	DIR	A	5.2	19.4	4.8	18.5	4.7	18.4	5.1	17.1	ns
t_{PLZ}			2.3	10.5	2.1	10.5	2.4	10.7	3.1	10.9	
t_{PHZ}	DIR	B	5.2	21.9	4.9	11.5	4.6	10.3	2.8	8.2	ns
t_{PLZ}			4.2	16	3.7	9.2	3.3	8.4	2.4	6.4	
t_{PZH} (1)	DIR	A		33.7		25.2		23.9		21.5	ns
t_{PZL} (1)				36.2		24.4		22.9		20.4	
t_{PZH} (1)	DIR	B		28.2		20.8		19		18.1	ns
t_{PZL} (1)				33.7		27		25.5		24.1	

(1) The enable time is a calculated value, derived using the formula shown in the *Enable Times* section.

5.7 Switching Characteristics (V_{CCA} = 2.5V ± 0.2V)

over recommended operating free-air temperature range, V_{CCA} = 2.5V ± 0.2V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ±0.15V		V_{CCB} = 2.5V ±0.2V		V_{CCB} = 3.3V ±0.3V		V_{CCB} = 5V ±0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.3	16	1.5	8.5	1.3	6.4	1.1	5.1	ns
t_{PHL}			2.1	12.9	1.4	7.5	1.3	5.4	0.9	4.6	
t_{PLH}	B	A	2.2	10.3	1.5	8.5	1.4	8	1	7.5	ns
t_{PHL}			2.2	8.5	1.4	7.5	1.3	7	0.9	6.2	
t_{PHZ}	DIR	A	3	8.1	3.1	8.1	2.8	8.1	3.2	8.1	ns
t_{PLZ}			1.3	5.9	1.3	5.9	1.3	5.9	1	5.8	
t_{PHZ}	DIR	B	5.2	23.7	4.1	11.4	3.9	10.2	2.4	7.1	ns
t_{PLZ}			3.9	18.9	3.2	9.6	2.8	8.4	1.8	5.3	
t_{PZH} (1)	DIR	A		29.2		18.1		16.4		12.8	ns
t_{PZL} (1)				32.2		18.9		17.2		13.3	
t_{PZH} (1)	DIR	B		21.9		14.4		12.3		10.9	ns
t_{PZL} (1)				21		15.6		13.5		12.7	

(1) The enable time is a calculated value, derived using the formula shown in the *Enable Times* section.

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5.8 Switching Characteristics (V_{CCA} = 3.3V ± 0.3V)

over recommended operating free-air temperature range, V_{CCA} = 3.3V ± 0.3V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ±0.15V		V_{CCB} = 2.5V ±0.2V		V_{CCB} = 3.3V ±0.3V		V_{CCB} = 5V ±0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.1	15.5	1.4	8	0.7	5.8	0.7	4.4	ns
t_{PHL}			2	12.6	1.3	7	0.8	5	0.7	4	
t_{PLH}	B	A	1.7	8.3	1.3	6.4	0.7	5.8	0.6	5.4	ns
t_{PHL}			1.8	7.1	1.3	5.4	0.8	5	0.7	4.5	
t_{PHZ}	DIR	A	2.9	7.3	3	7.3	2.8	7.3	3.4	7.3	ns
t_{PLZ}			1.8	5.6	1.6	5.6	2.2	5.7	2.2	5.7	
t_{PHZ}	DIR	B	5.4	20.5	3.9	10.1	2.9	8.8	2.4	6.8	ns
t_{PLZ}			3.3	14.5	2.9	7.8	2.4	7.1	1.7	4.9	
t_{PZH} (1)	DIR	A		22.8		14.2		12.9		10.3	ns
t_{PZL} (1)				27.6		15.5		13.8		11.3	
t_{PZH} (1)	DIR	B		21.1		13.6		11.5		10.1	ns
t_{PZL} (1)				19.9		14.3		12.3		11.3	

(1) The enable time is a calculated value, derived using the formula shown in the *Enable Times* section.

5.9 Switching Characteristics (V_{CCA} = 5V ±0.5V)

over recommended operating free-air temperature range, V_{CCA} = 5V ±0.5V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ±0.15V		V_{CCB} = 2.5V ±0.2V		V_{CCB} = 3.3V ±0.3V		V_{CCB} = 5V ±0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.9	15.1	1	7.5	0.6	5.4	0.5	3.9	ns
t_{PHL}			1.8	12.2	0.9	6.2	0.7	4.5	0.5	3.5	
t_{PLH}	B	A	1.4	7.2	1	5.1	0.7	4.4	0.5	3.9	ns
t_{PHL}			1.7	7	0.9	4.6	0.7	4	0.5	3.5	
t_{PHZ}	DIR	A	2.1	5.4	2.2	5.4	2.2	5.5	2.2	5.4	ns
t_{PLZ}			0.9	3.8	1	3.8	0.7	3.7	0.7	3.7	
t_{PHZ}	DIR	B	4.8	20.2	2.5	9.8	1	8.5	2.5	6.5	ns
t_{PLZ}			3.2	14.8	2.5	7.4	2.5	7	1.6	4.5	
t_{PZH} (1)	DIR	A		22		12.5		11.4		8.4	ns
t_{PZL} (1)				27.2		14.4		12.5		10	
t_{PZH} (1)	DIR	B		18.9		11.3		9.1		7.6	ns
t_{PZL} (1)				17.6		11.6		10		8.6	

(1) The enable time is a calculated value, derived using the formula shown in the *Enable Times* section.

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5.10 Operating Characteristics

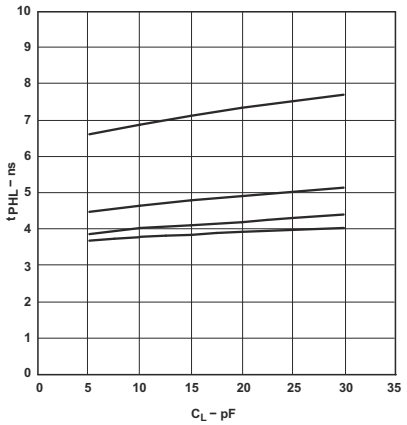
T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.8V	V_{CCA} = V_{CCB} = 2.5V	V_{CCA} = V_{CCB} = 3.3V	V_{CCA} = V_{CCB} = 5V	UNIT
			TYP	TYP	TYP	TYP	
C_{pdA} (1)	A-port input, B-port output	C_L = 0 pF, f = 10 MHz, $t_r = t_f$ = 1 ns	3	4	4	4	pF
	B-port input, A-port output		18	19	20	21	
C_{pdB} (1)	A-port input, B-port output	C_L = 0 pF, f = 10 MHz, $t_r = t_f$ = 1 ns	18	19	20	21	pF
	B-port input, A-port output		3	4	4	4	

(1) Power dissipation capacitance per transceiver

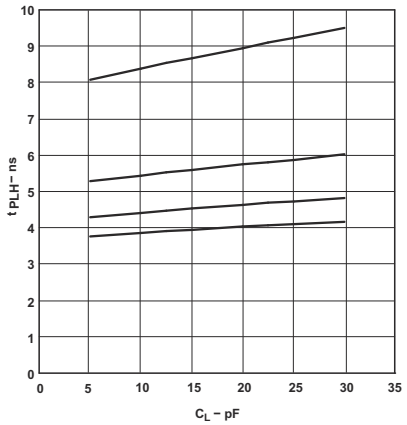
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5.11 Typical Characteristics



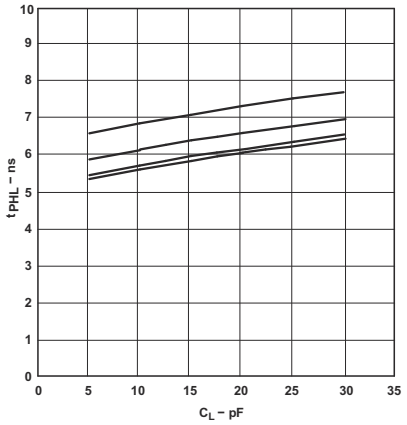
T_A = 25°C, V_{CCA} = 1.8V

図 5-1. Typical Propagation Delay (A to B) vs Load Capacitance



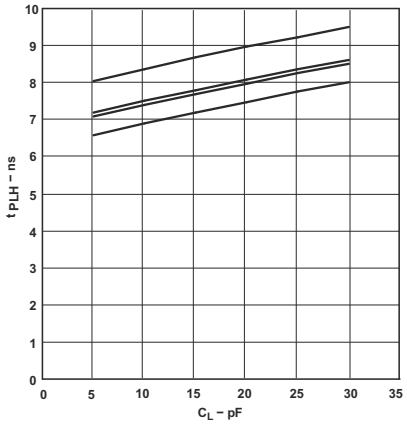
T_A = 25°C, V_{CCA} = 1.8V

図 5-2. Typical Propagation Delay (B to A) vs Load Capacitance



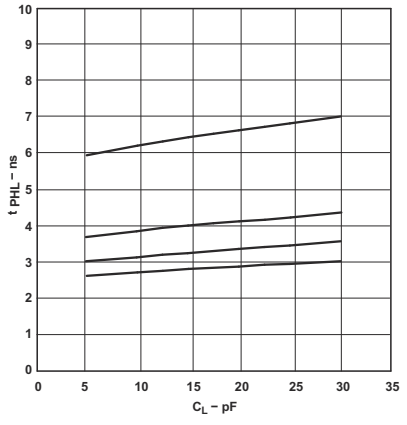
T_A = 25°C, V_{CCA} = 2.5V

図 5-3. Typical Propagation Delay (A to B) vs Load Capacitance



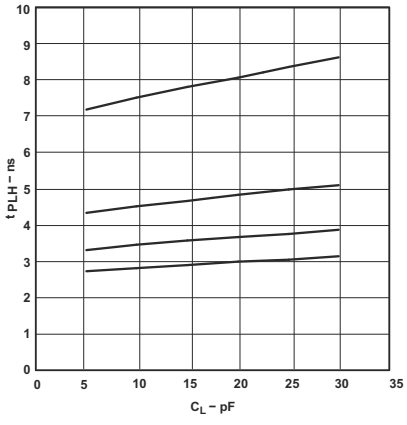
T_A = 25°C, V_{CCA} = 2.5V

図 5-4. Typical Propagation Delay (B to A) vs Load Capacitance



T_A = 25°C, V_{CCA} = 3.3V

図 5-5. Typical Propagation Delay (A to B) vs Load Capacitance

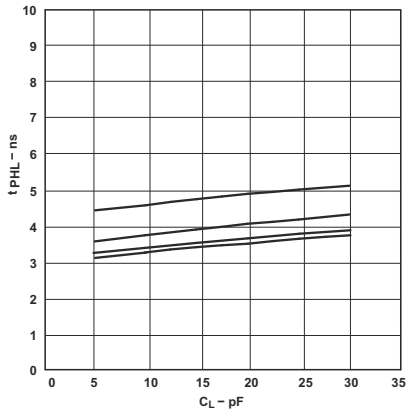


T_A = 25°C, V_{CCA} = 3.3V

図 5-6. Typical Propagation Delay (B to A) vs Load Capacitance

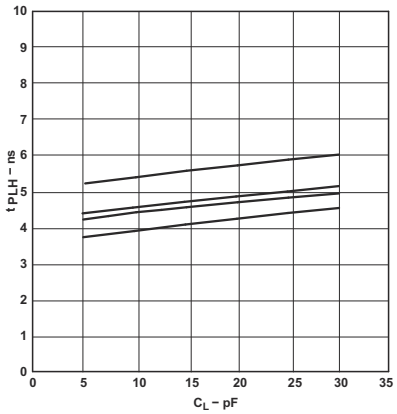
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5.11 Typical Characteristics (continued)



T_A = 25°C, V_{CCA} = 5V

図 5-7. Typical Propagation Delay (A to B) vs Load Capacitance

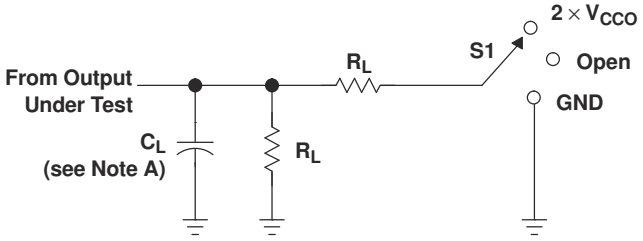


T_A = 25°C, V_{CCA} = 5V

図 5-8. Typical Propagation Delay (B to A) vs Load Capacitance

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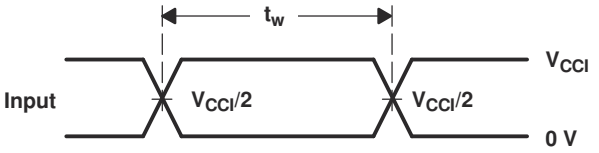
6 Parameter Measurement Information



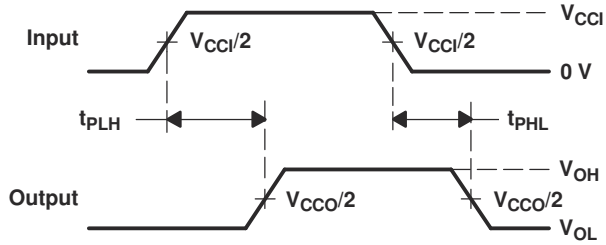
TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open $2 \times V_{CCO}$ GND

LOAD CIRCUIT

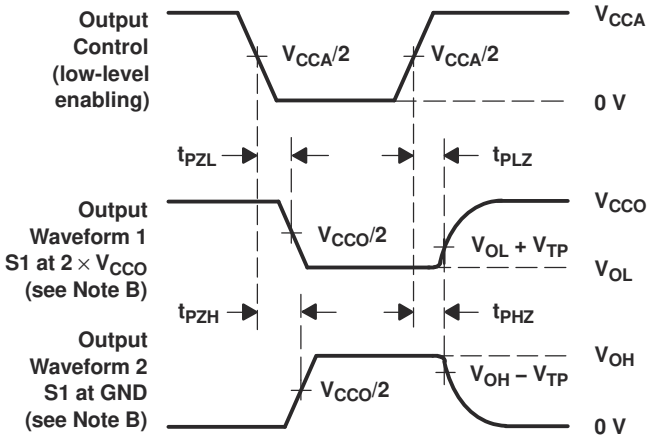
V_{CCO}	C_L	R_L	V_{TP}
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V
5 V ± 0.5 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.
J. All parameters and waveforms are not applicable to all devices.

図 6-1. Load Circuit and Voltage Waveforms

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7 Detailed Description

7.1 Overview

The SN74LVC1T45 is a single-bit, dual-supply, noninverting voltage level transceiver. Pin A and the direction control pin (DIR) are supported by V_{CCA} and pin B is supported by V_{CCB}. The A port is able to accept I/O voltages ranging from 1.65V to 5.5V, while the B port can accept I/O voltages from 1.65V to 5.5V. The high on the DIR allows data transmissions from A to B and a low on the DIR allows data transmissions from B to A.

7.2 Functional Block Diagram

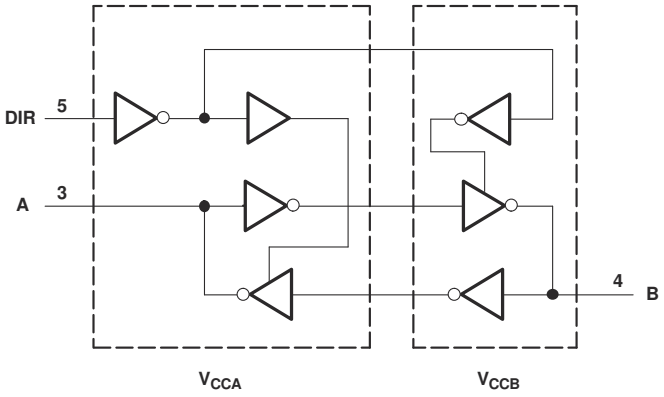


図 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65V to 5.5V Power-Supply Range

Both V_{CCA} and V_{CCB} can be supplied at any voltage between 1.65V and 5.5V, making the device suitable for translating between any of the voltage nodes (1.8V, 2.5V, 3.3V, and 5V).

7.3.2 Support High Speed Translation

The SN74LVC1T45 device supports high data rate applications. The translated signal data rate can be up to 420Mbps when the signal is translated from 3.3V to 5V.

7.3.3 I_{off} Supports Partial Power-Down Mode Operation

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Charateristics* .

7.3.4 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so impedance matching and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Two outputs can be connected together for a stronger output drive strength. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

7.3.5 Glitch-Free Power Supply Sequencing

Either supply rail may be powered on or off in any order without producing a glitch on the I/Os (that is, where the output erroneously transitions to VCC when it should be held low or vice versa). Glitches of this nature can be misinterpreted by a peripheral as a valid data bit, which could trigger a false device reset of the peripheral, a false device configuration of the peripheral, or even a false data initialization by the peripheral.

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7.3.6 V_{cc} Isolation

The I/Os of both ports will enter a high-impedance state when either of the supplies are at GND, while the other supply is still connected to the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

7.4 Device Functional Modes

表 7-1. Function Table (1)

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

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8 Applications and Implementation

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8.1 Application Information

The SN74LVC1T45 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The maximum data rate can be up to 420Mbps when device translates signals from 3.3V to 5V.

8.2 Typical Application

8.2.1 Unidirectional Logic Level-Shifting Application

図 8-1 shows an example of the SN74LVC1T45 being used in a unidirectional logic level-shifting application.

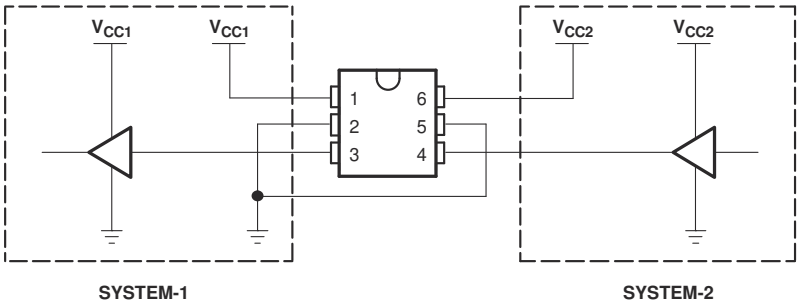


図 8-1. Unidirectional Logic Level-Shifting Application

8.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 8-1.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.65V to 5.5V
Output voltage range	1.65V to 5.5V

8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

• Input voltage range

- Use the supply voltage of the device that is driving the SN74LVC1T45 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.

• Output voltage range

- Use the supply voltage of the device that the SN74LVC1T45 device is driving to determine the output voltage range.

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8.2.1.3 Application Curve

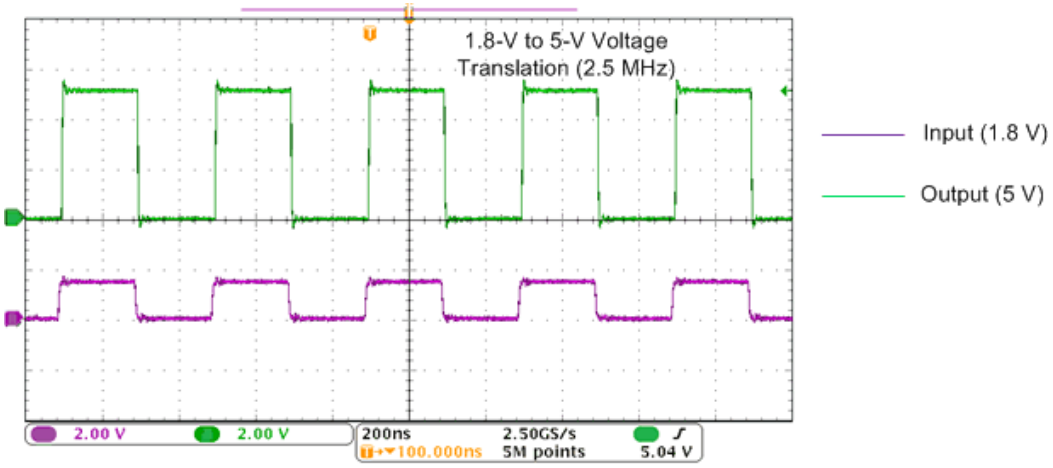


図 8-2. Translation Up (1.8V to 5V) at 2.5 MHz

8.2.2 Bidirectional Logic Level-Shifting Application

図 8-3 shows the SN74LVC1T45 being used in a bidirectional logic level-shifting application. Because the SN74LVC1T45 does not have an output-enable ($\overline{OE}$) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.

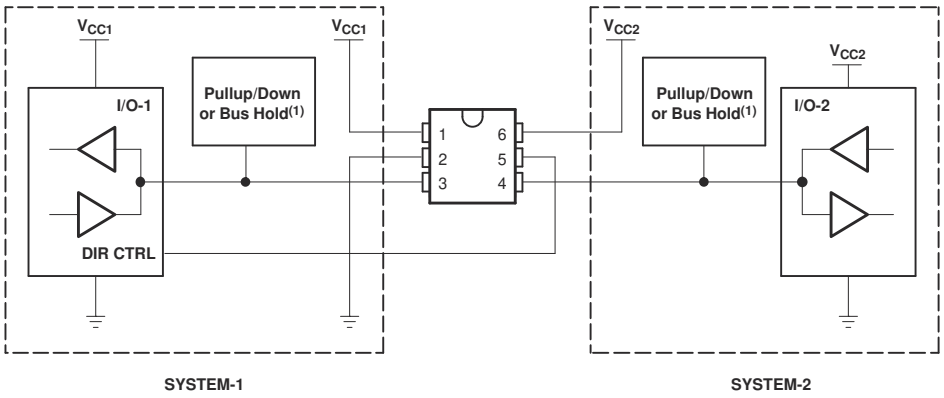


図 8-3. Bidirectional Logic Level-Shifting Application

8.2.2.1 Design Requirements

See *セクション 8.2.1.1* .

8.2.2.2 Detailed Design Procedure

表 8-2 shows data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

表 8-2. SYSTEM-1 and SYSTEM-2 Data Transmission

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	H	Out	In	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on pullup or pulldown.(1)
3	L	Hi-Z	Hi-Z	DIR bit is flipped. I/O-1 and I/O-2 still are disabled. The bus-line state depends on pullup or pulldown.(1)

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表 8-2. SYSTEM-1 and SYSTEM-2 Data Transmission (続き)

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
4	L	In	Out	SYSTEM-2 data to SYSTEM-1

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, that is, both pullup or both pulldown.

8.2.2.2.1 Enable Times

Calculate the enable times for the SN74LVC1T45 using the following formulas:

- t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A)
- t_{PZL} (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A)
- t_{PZH} (DIR to B) = t_{PLZ} (DIR to A) + t_{PLH} (A to B)
- t_{PZL} (DIR to B) = t_{PHZ} (DIR to A) + t_{PHL} (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74LVC1T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

8.2.2.3 Application Curve

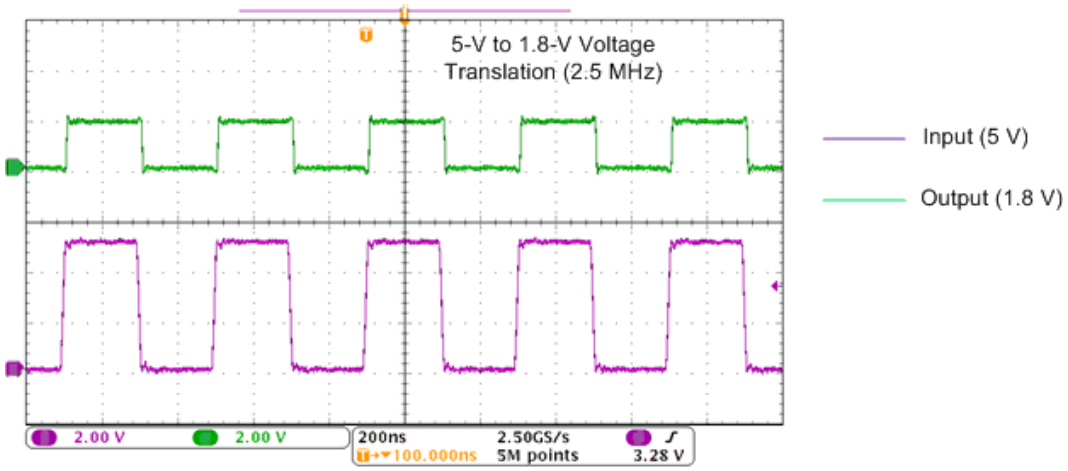


図 8-4. Translation Down (5V to 1.8V) at 2.5 MHz

8.3 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate.

This device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices, as described in *Glitch-free Power Supply Sequencing* .

8.4 Layout

8.4.1 Layout Guidelines

To ensure reliability of the device, the following common printed-circuit board layout guidelines are recommended:

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depends on the system requirements

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8.4.2 Layout Example

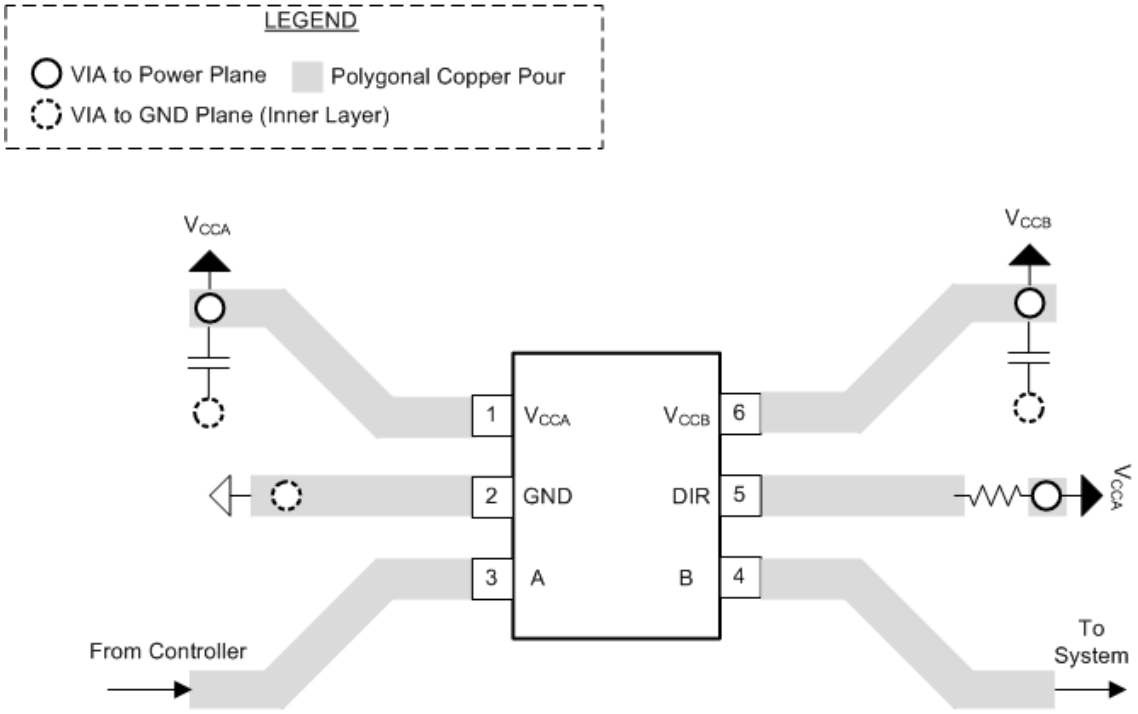


図 8-5. Layout Example

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9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision M (November 2022) to Revision N (June 2024)	Page
• Updated the *Power Supply Recommendations* section	17

Changes from Revision L (February 2017) to Revision M (November 2022)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• Updated the thermals in the *Thermal Information* section	5
• Updated the *Switching Characterisitcs* sections: extended some minimum specifications for lower delays	7
• Updated the I_{off} *Supports Partial Power-Down Mode Operation* section	13
• Added the *Balanced High-Drive CMOS Push-Pull Outputs* and V_{CC} *Isolation* sections	13

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1T45DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(2PUH, CT15, CT1F, CT1R)
SN74LVC1T45DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(2PUH, CT15, CT1F, CT1R)
SN74LVC1T45DBVRE4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CT15, CT1F, CT1R)
SN74LVC1T45DBVRE4.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CT15, CT1F, CT1R)
SN74LVC1T45DBVRG4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CT15, CT1F, CT1R)
SN74LVC1T45DBVRG4.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CT15, CT1F, CT1R)
SN74LVC1T45DBVRG4.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
SN74LVC1T45DBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(CT15, CT1F, CT1R)
SN74LVC1T45DBVT.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CT15, CT1F, CT1R)
SN74LVC1T45DBVTG4	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CT15, CT1F, CT1R)
SN74LVC1T45DBVTG4.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CT15, CT1F, CT1R)
SN74LVC1T45DCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)
SN74LVC1T45DCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)
SN74LVC1T45DCKR.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)
SN74LVC1T45DCKRE4	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	No	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)
SN74LVC1T45DCKRE4	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)
SN74LVC1T45DCKRE4.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	No	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)
SN74LVC1T45DCKRE4.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)
SN74LVC1T45DCKRE4.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)
SN74LVC1T45DCKRE4.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	No	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)
SN74LVC1T45DCKRG4	Active	Production	SC70 (DCK) | 6	3000 | null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)
SN74LVC1T45DCKRG4	Active	Production	SC70 (DCK) | 6	3000 | null	No	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1T45DCKRG4.A	Active	Production	SC70 (DCK) | 6	3000 | null	No	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)
SN74LVC1T45DCKRG4.A	Active	Production	SC70 (DCK) | 6	3000 | null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)
SN74LVC1T45DCKRG4.B	Active	Production	SC70 (DCK) | 6	3000 | null	No	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)
SN74LVC1T45DCKRG4.B	Active	Production	SC70 (DCK) | 6	3000 | null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)
SN74LVC1T45DCKT	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)
SN74LVC1T45DCKT.A	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)
SN74LVC1T45DCKT.B	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)
SN74LVC1T45DCKTE4	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)
SN74LVC1T45DCKTG4	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)
SN74LVC1T45DCKTG4.A	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)
SN74LVC1T45DCKTG4.B	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TA5, TAF, TAR)
SN74LVC1T45DPKR	Active	Production	USON (DPK) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TA7
SN74LVC1T45DPKR.B	Active	Production	USON (DPK) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TA7
SN74LVC1T45DPKRG4	Active	Production	USON (DPK) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TA7
SN74LVC1T45DPKRG4.B	Active	Production	USON (DPK) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TA7
SN74LVC1T45DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(1JX, TA7, TAR)
SN74LVC1T45DRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(1JX, TA7, TAR)
SN74LVC1T45DRLR.B	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(1JX, TA7, TAR)
SN74LVC1T45DRLRG4	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(1JX, TA7, TAR)
SN74LVC1T45YZPR	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TA2, TA7, TAN)
SN74LVC1T45YZPR.B	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TA2, TA7, TAN)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVC1T45 :

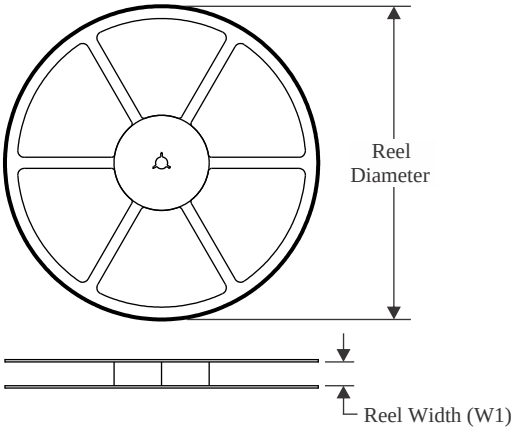
- Automotive : SN74LVC1T45-Q1
- Enhanced Product : SN74LVC1T45-EP

NOTE: Qualified Version Definitions:

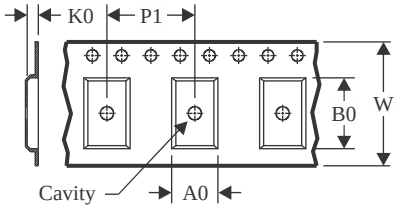
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

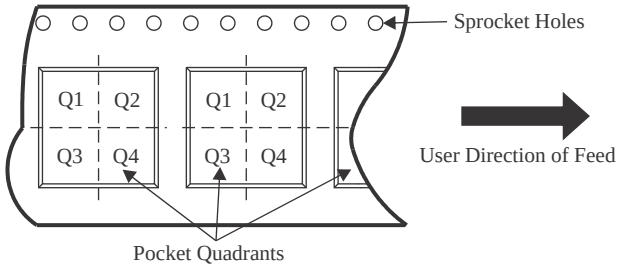


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

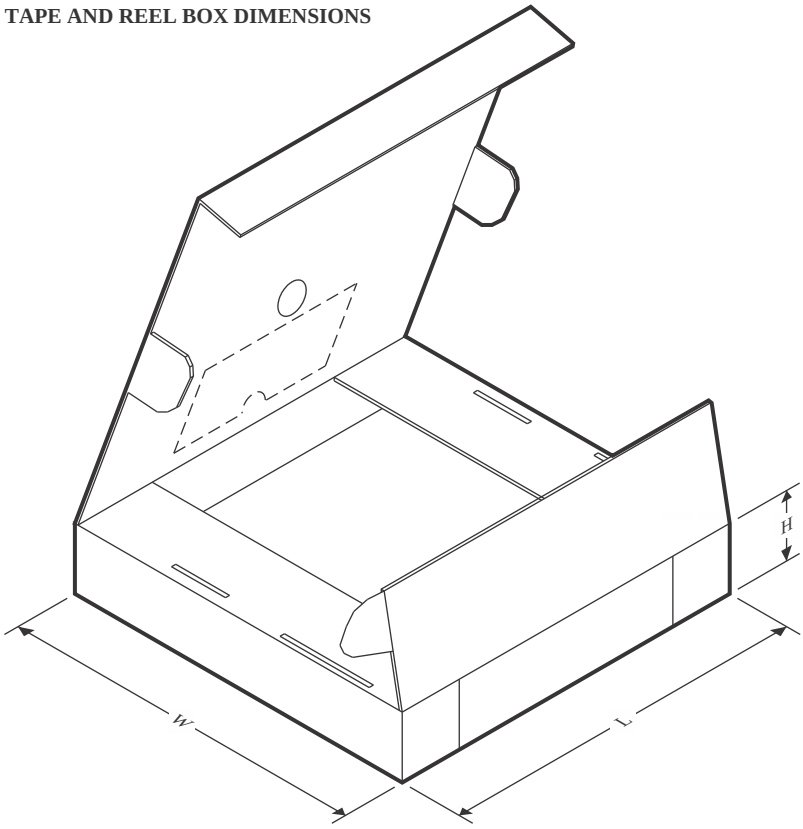


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1T45DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1T45DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1T45DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1T45DBVR	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1T45DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1T45DBVRE4	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1T45DBVRE4	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1T45DBVRG4	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1T45DBVRG4	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1T45DBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1T45DBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1T45DBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1T45DBVTG4	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1T45DBVTG4	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1T45DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1T45DCKR	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1T45DCKR	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74LVC1T45DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1T45DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1T45DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74LVC1T45DCKRE4	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1T45DCKRE4	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74LVC1T45DCKRE4	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1T45DCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1T45DCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1T45DCKT	SC70	DCK	6	250	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1T45DCKTG4	SC70	DCK	6	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1T45DCKTG4	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74LVC1T45DCKTG4	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1T45DCKTG4	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1T45DPKR	USON	DPK	6	5000	180.0	9.5	1.75	1.75	0.7	4.0	8.0	Q2
SN74LVC1T45DPKRG4	USON	DPK	6	5000	180.0	9.5	1.75	1.75	0.7	4.0	8.0	Q2
SN74LVC1T45DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
SN74LVC1T45DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1T45YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1T45DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
SN74LVC1T45DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
SN74LVC1T45DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
SN74LVC1T45DBVR	SOT-23	DBV	6	3000	208.0	191.0	35.0
SN74LVC1T45DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
SN74LVC1T45DBVRE4	SOT-23	DBV	6	3000	210.0	185.0	35.0
SN74LVC1T45DBVRE4	SOT-23	DBV	6	3000	210.0	185.0	35.0
SN74LVC1T45DBVRG4	SOT-23	DBV	6	3000	210.0	185.0	35.0
SN74LVC1T45DBVRG4	SOT-23	DBV	6	3000	210.0	185.0	35.0
SN74LVC1T45DBVT	SOT-23	DBV	6	250	210.0	185.0	35.0
SN74LVC1T45DBVT	SOT-23	DBV	6	250	210.0	185.0	35.0
SN74LVC1T45DBVT	SOT-23	DBV	6	250	210.0	185.0	35.0
SN74LVC1T45DBVTG4	SOT-23	DBV	6	250	210.0	185.0	35.0
SN74LVC1T45DBVTG4	SOT-23	DBV	6	250	210.0	185.0	35.0
SN74LVC1T45DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1T45DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1T45DCKR	SC70	DCK	6	3000	208.0	191.0	35.0
SN74LVC1T45DCKR	SC70	DCK	6	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1T45DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1T45DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74LVC1T45DCKRE4	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1T45DCKRE4	SC70	DCK	6	3000	202.0	201.0	28.0
SN74LVC1T45DCKRE4	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1T45DCKT	SC70	DCK	6	250	180.0	180.0	18.0
SN74LVC1T45DCKT	SC70	DCK	6	250	180.0	180.0	18.0
SN74LVC1T45DCKT	SC70	DCK	6	250	210.0	185.0	35.0
SN74LVC1T45DCKTG4	SC70	DCK	6	250	180.0	180.0	18.0
SN74LVC1T45DCKTG4	SC70	DCK	6	250	202.0	201.0	28.0
SN74LVC1T45DCKTG4	SC70	DCK	6	250	180.0	180.0	18.0
SN74LVC1T45DCKTG4	SC70	DCK	6	250	180.0	180.0	18.0
SN74LVC1T45DPKR	USON	DPK	6	5000	184.0	184.0	19.0
SN74LVC1T45DPKRG4	USON	DPK	6	5000	184.0	184.0	19.0
SN74LVC1T45DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
SN74LVC1T45DRLR	SOT-5X3	DRL	6	4000	202.0	201.0	28.0
SN74LVC1T45YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

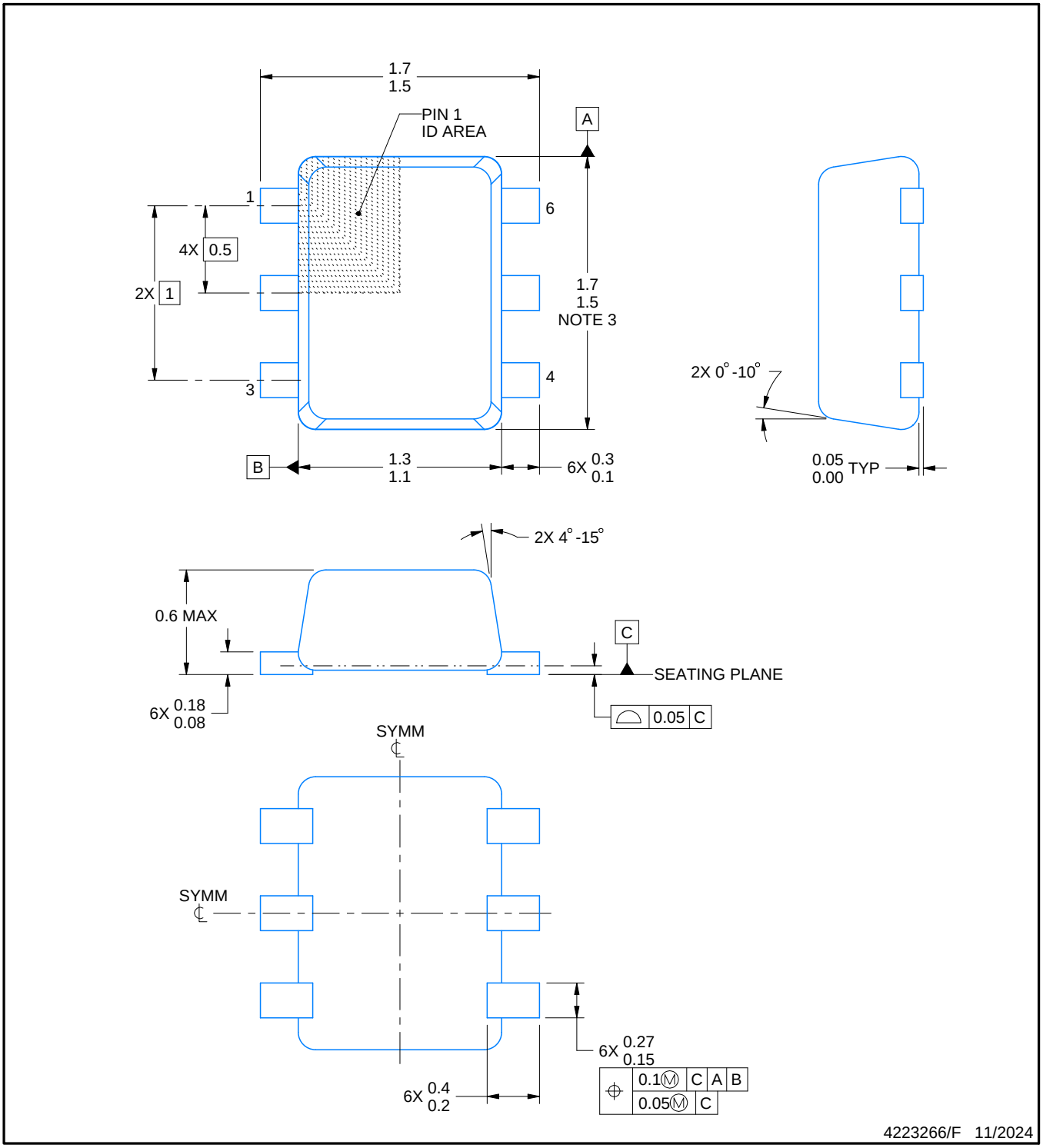


PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

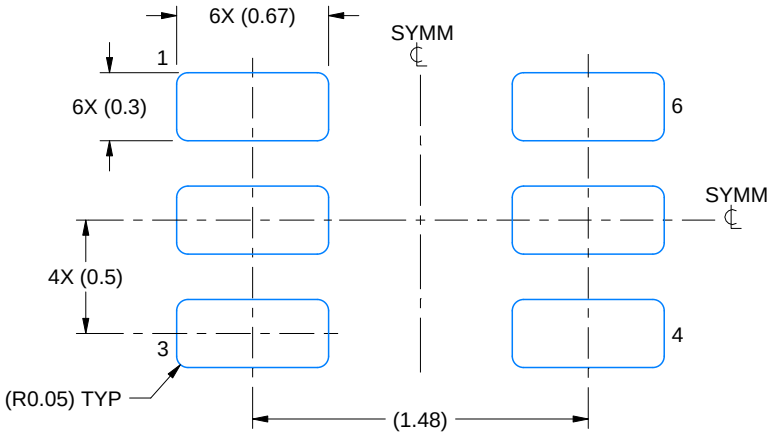
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

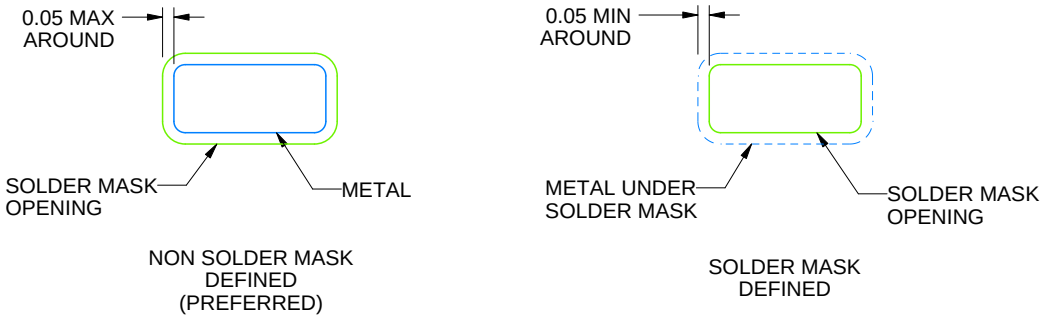
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

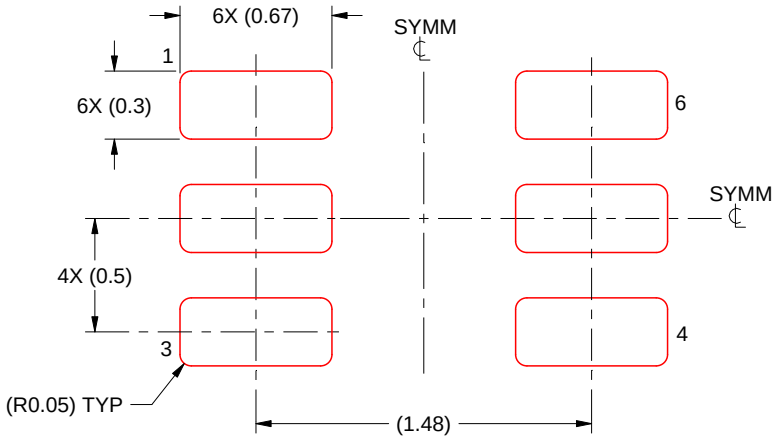
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

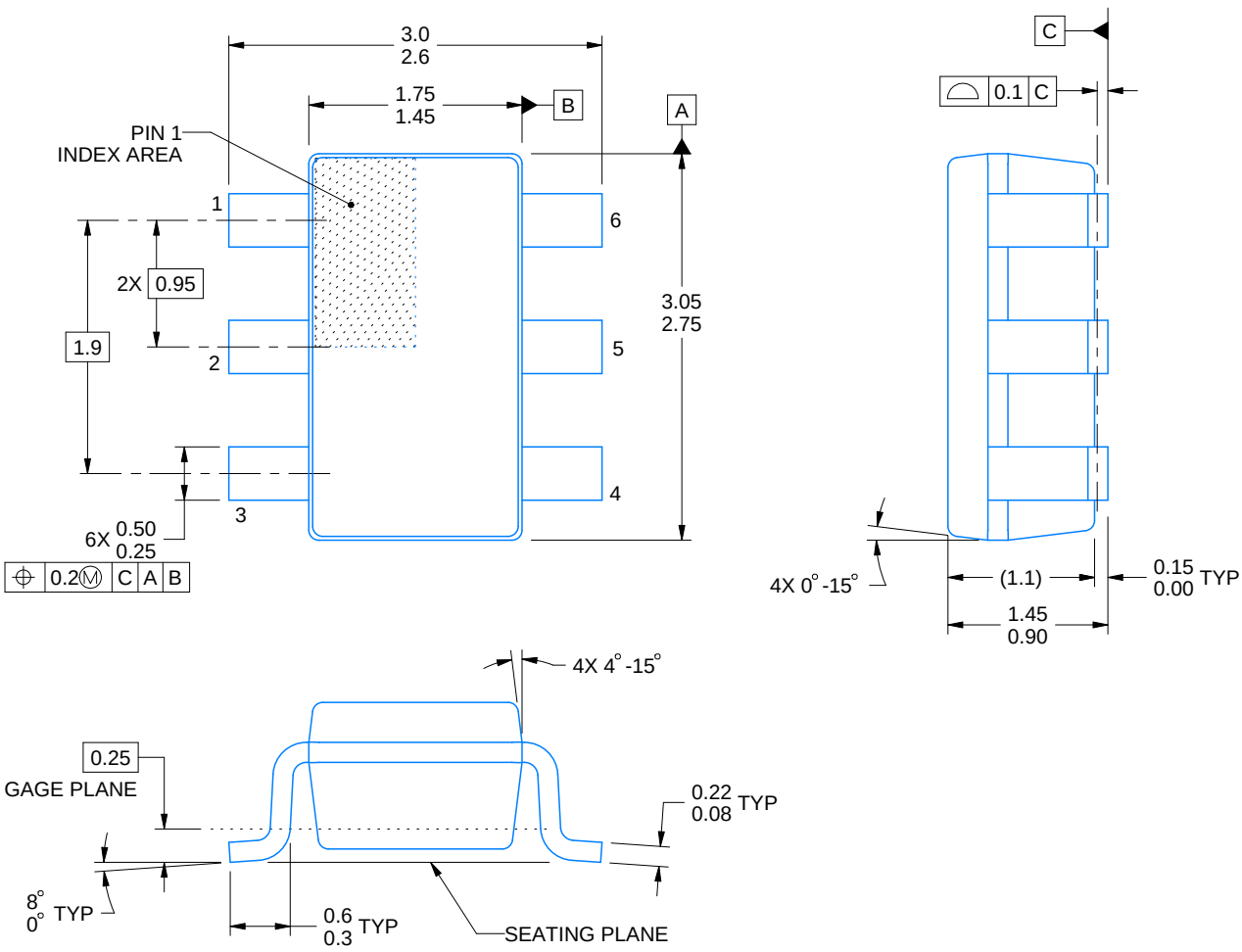
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

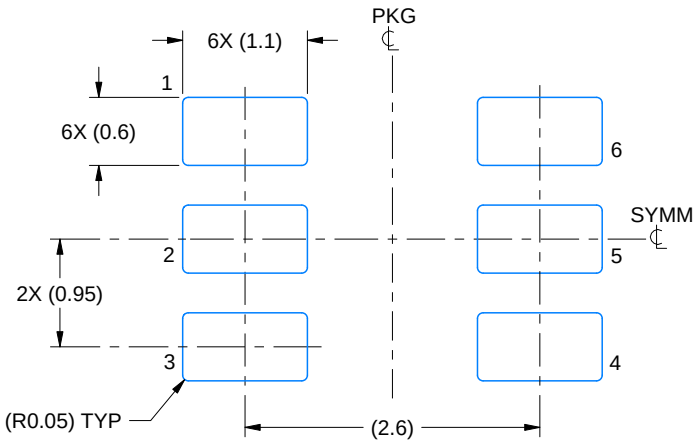
SMALL OUTLINE TRANSISTOR



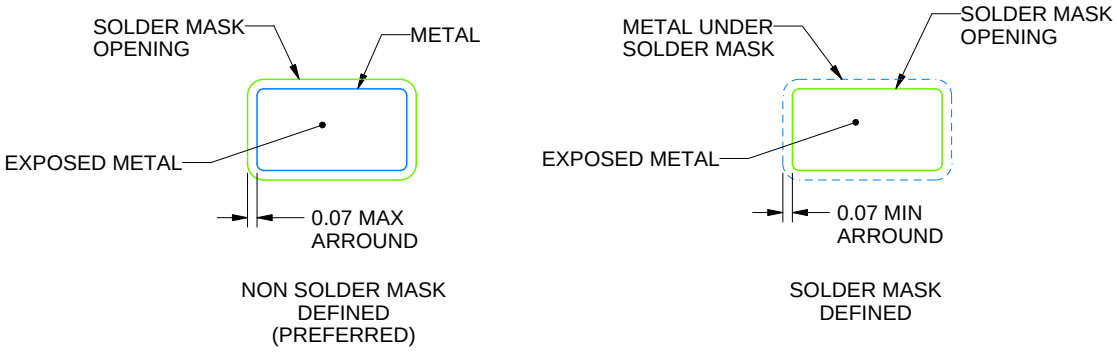
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

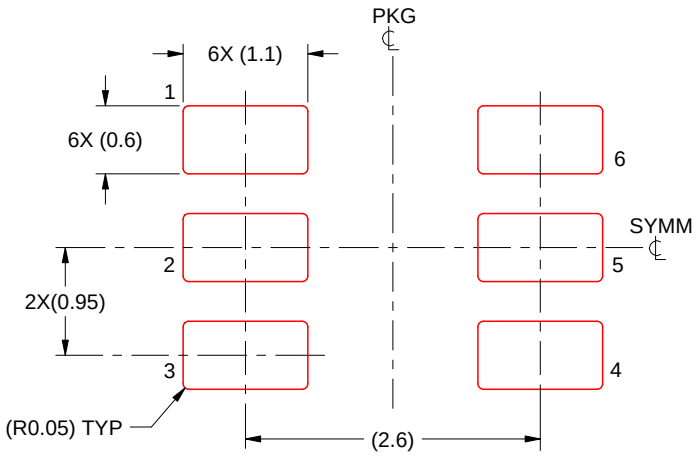


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



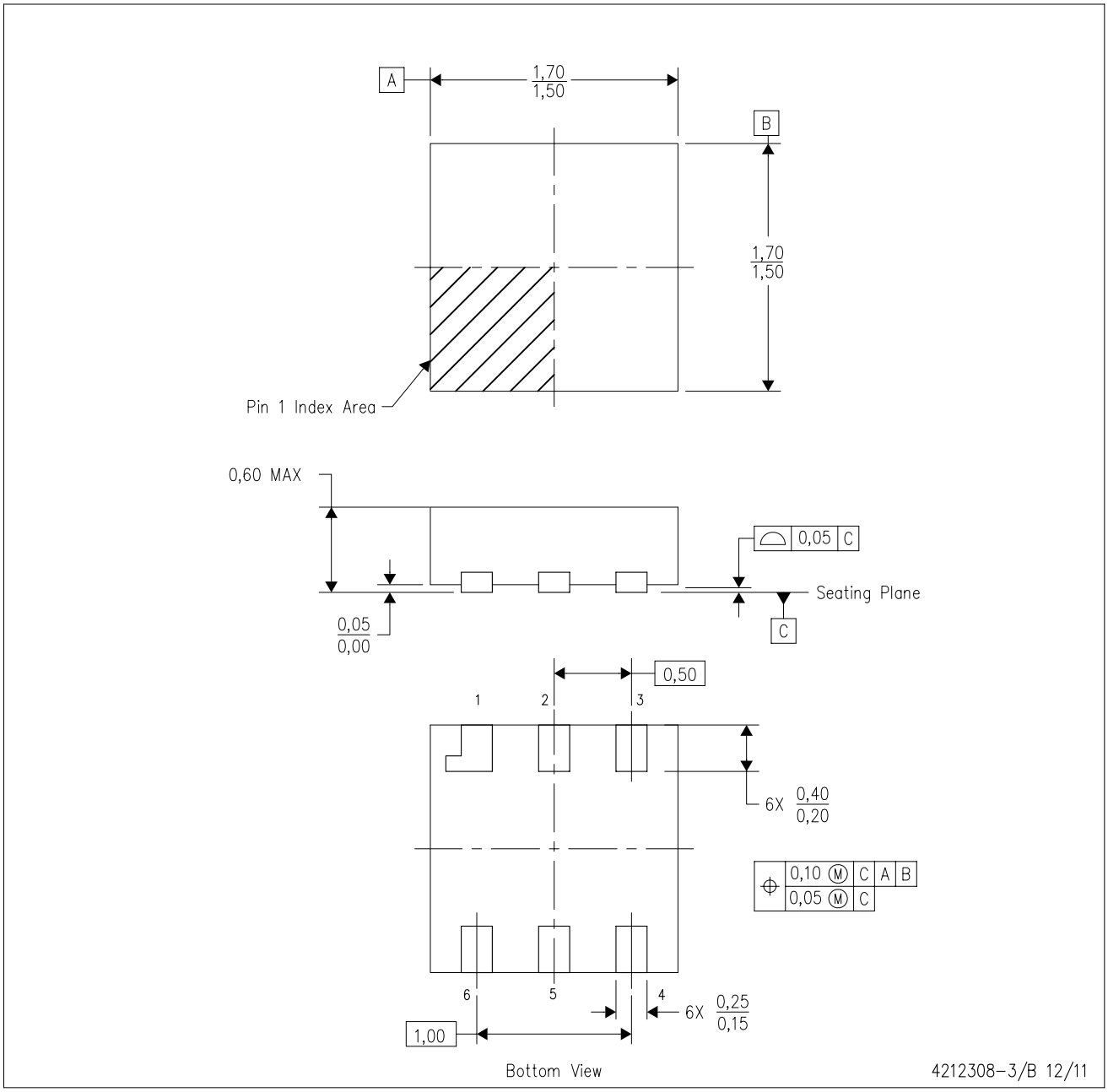
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

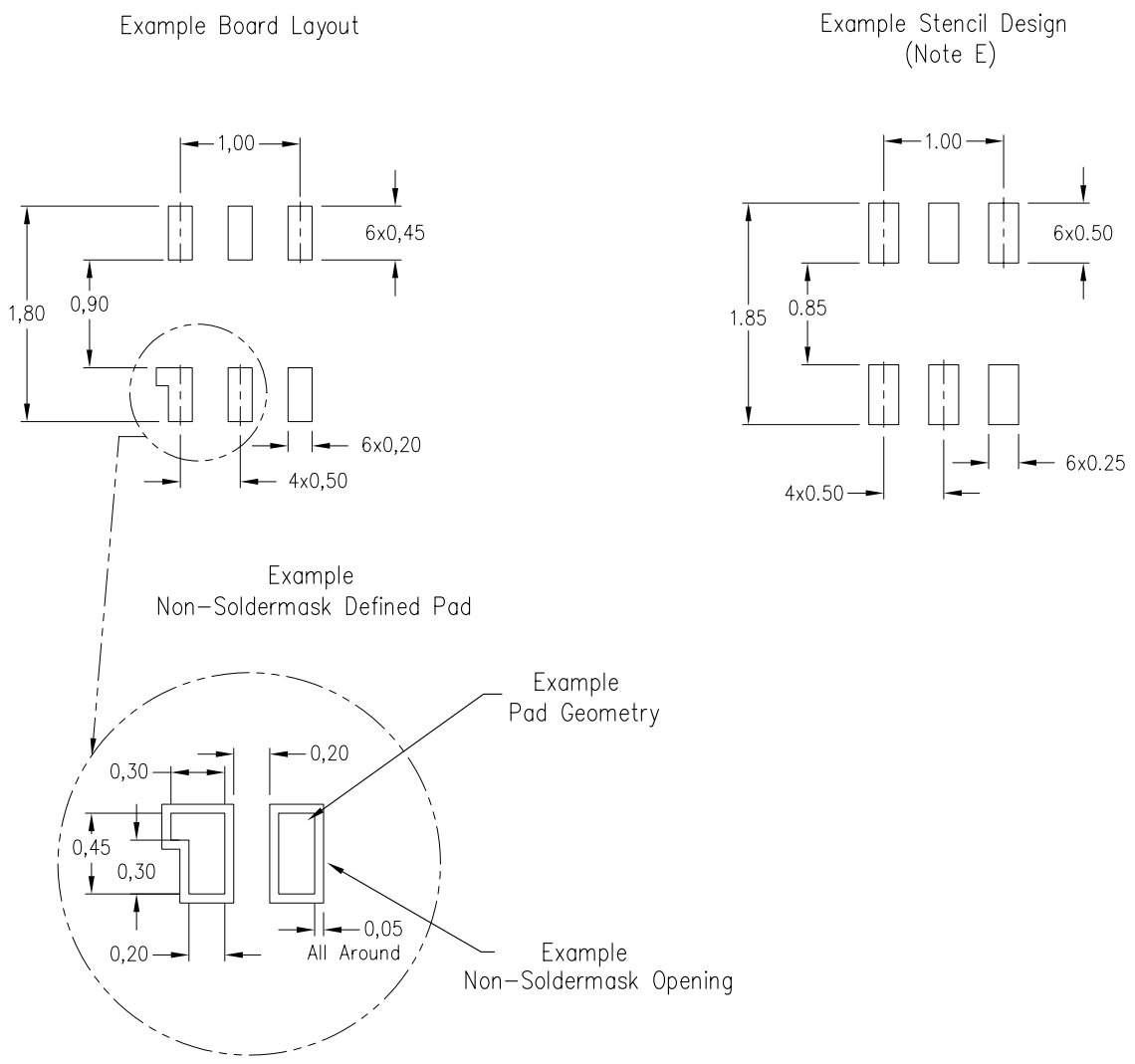
DPK (S–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.

DPK (S–PUSON–N6)

PLASTIC SMALL OUTLINE NO–LEAD



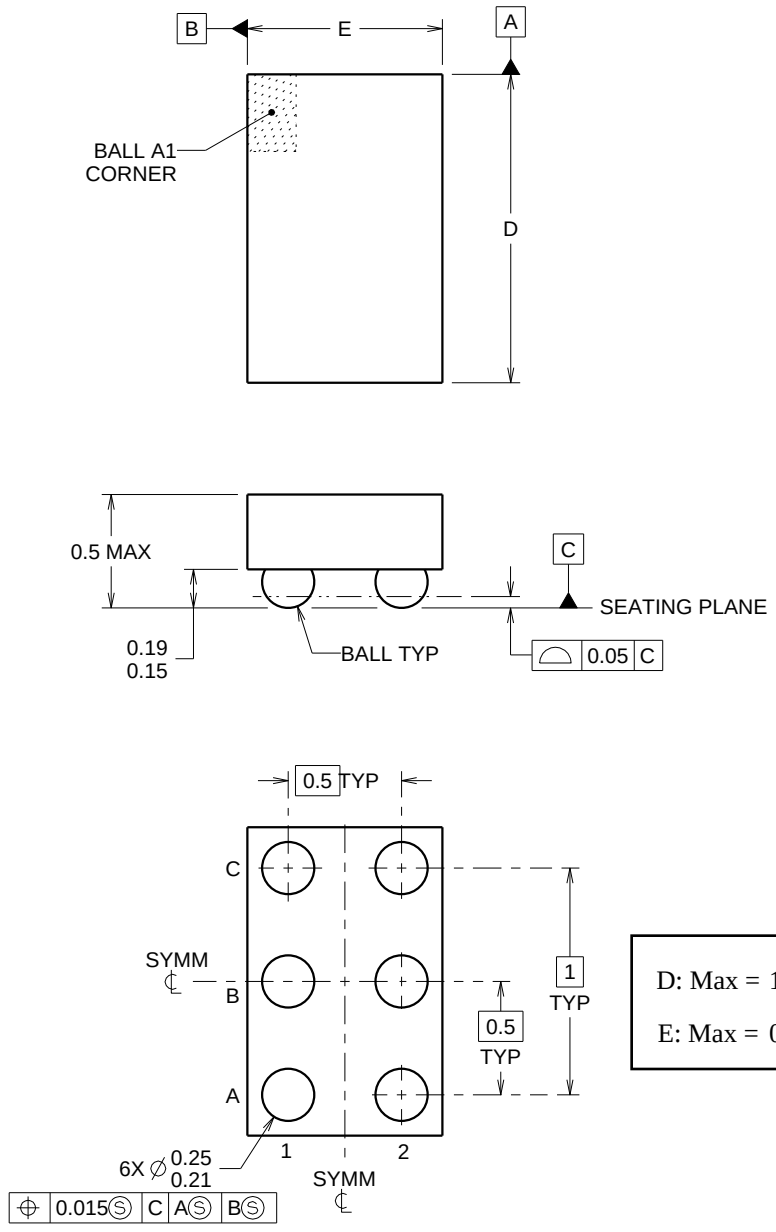
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

PACKAGE OUTLINE

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min =1.358 mm

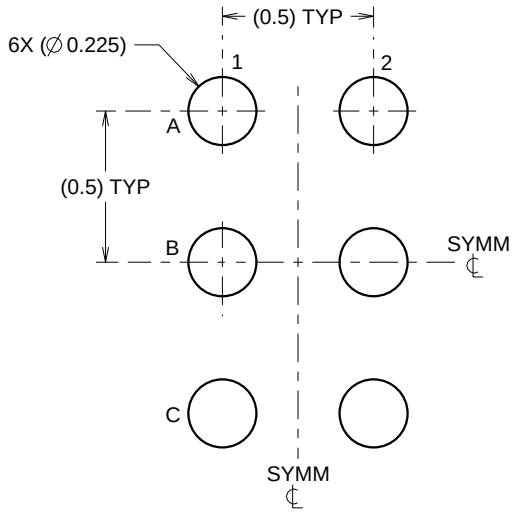
E: Max = 0.918 mm, Min =0.858 mm

4219524/A 06/2014

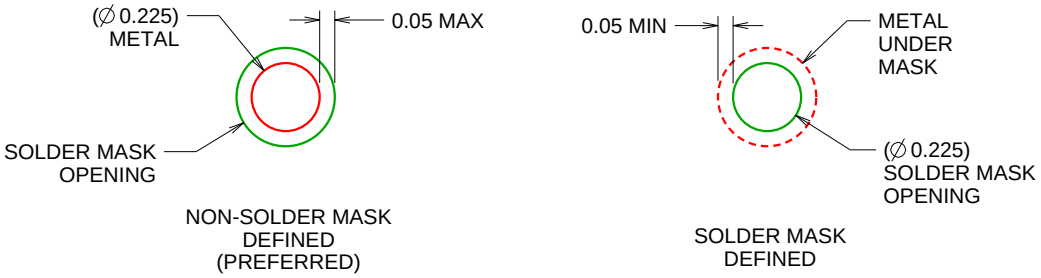
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
SCALE:40X

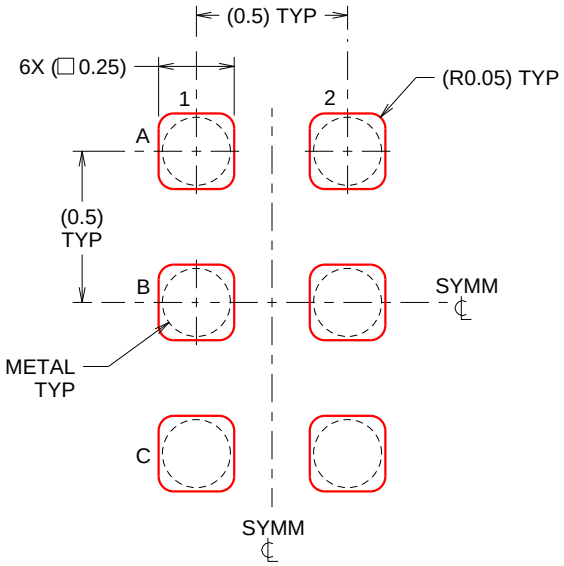


SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

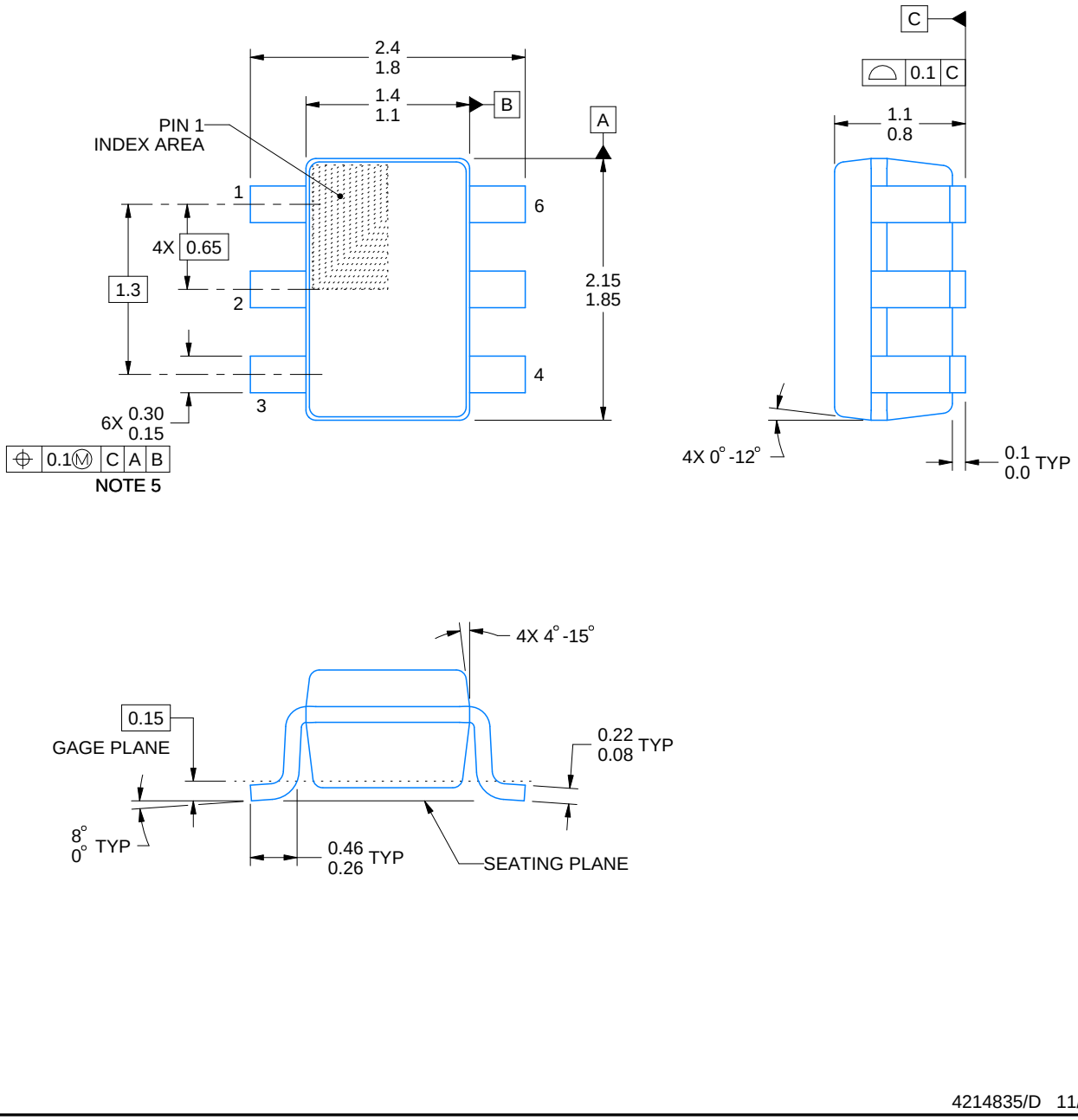
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

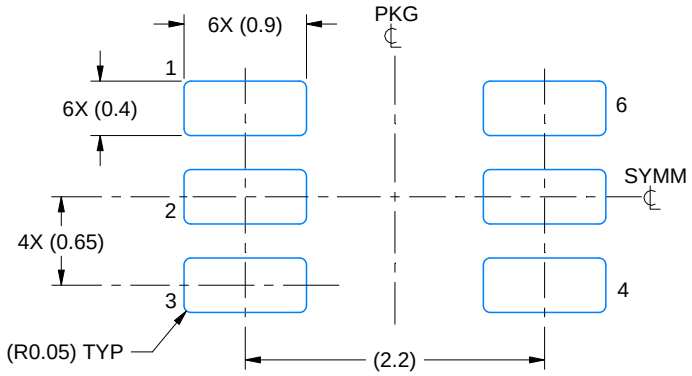
SMALL OUTLINE TRANSISTOR



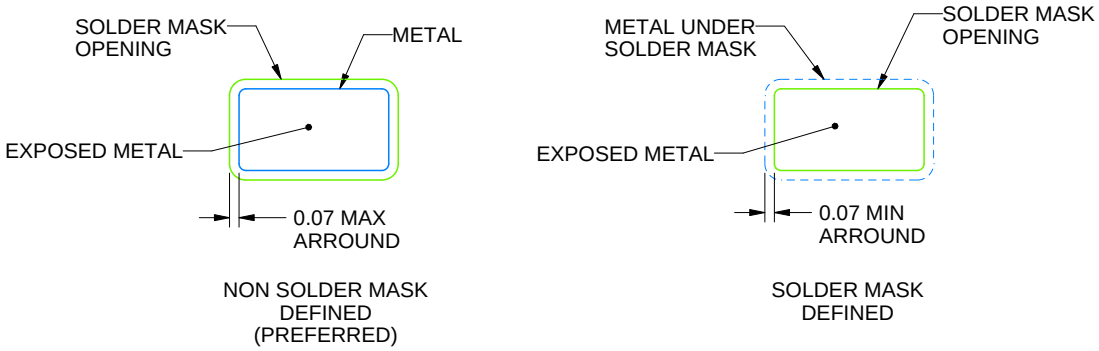
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

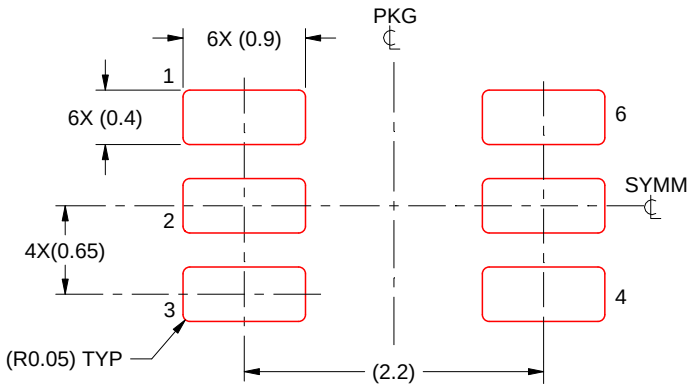


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月