

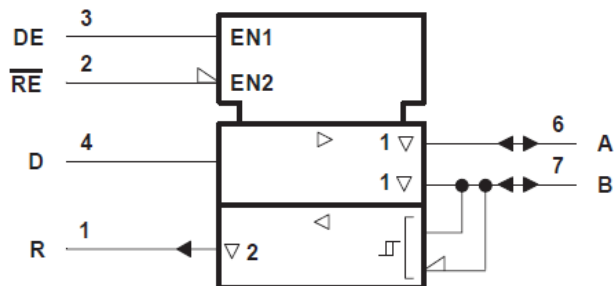
## SNx5ALS176、SN75ALS176A、SN75ALS176B 差動バス・トランシーバ

### 1 特長

- TIA/EIA-422-B、TIA/EIA-485-A の要件以上に適合。<sup>1</sup> また、ITU 勧告 V.11 および X.27 に準じます
- 最大 35Mbaud のデータ・レートで動作
- 4 つのスキュー制限が利用可能：
  - SN65ALS176 : 15ns
  - SN75ALS176 : 10ns
  - SN75ALS176A : 7.5ns
  - SN75ALS176B : 5ns
- ノイズの多い環境での、長いバス・ラインによるマルチポイント伝送向けの設計
- 低消費電流要件 : 30mA 以下
- 入力 / 出力における正および負の広いバス電圧範囲
- サーマル・シャットダウン保護機能
- ドライバの正 / 負電流制限
- レシーバ入力ヒステリシス
- グリッチ・フリーのパワーアップ / パワーダウン保護機能
- レシーバの開放回路フェイルセーフ設計

### 2 概要

SN65ALS176 および SN75ALS176 シリーズ差動バス・トランシーバは、マルチポイント・バス伝送線路での双方向データ通信を目的として設計されています。これらのデバイスは平衡伝送線路用に設計されており、TIA/EIA-422-B、TIA/EIA-485-A、ITU 勧告 V.11 および X.27 に適合しています。



A. この記号は ANSI/IEEE Std 91-1984 と IEC Publication 617-12 に準拠しています。

#### 論理記号

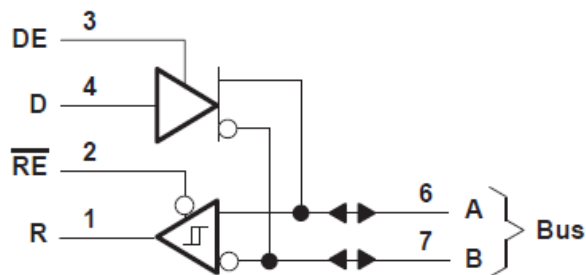
SN65ALS176 および SN75ALS176 は、3 ステートの、差動ライン・ドライバと差動入力ライン・レシーバを統合しており、このどちらも 5V 単一電源で動作します。ドライバとレシーバはそれぞれアクティブ High、アクティブ Low のイネーブルを備えており、それらのイネーブルを外部で互いに接続することで、方向制御として機能させることができます。ドライバの差動出力とレシーバの差動入力、差動入出力 (I/O) バス・ポートを構成するように内部で接続されています。これらのポートは、ドライバがディスエーブルされている場合、または  $V_{CC} = 0$  の場合、バスへの負荷を最小化するように設計されています。このポートは広い正負の同相電圧範囲を持っているため、本デバイスはパーティライン・アプリケーションに適しています。

SN65ALS176 は  $-40^{\circ}\text{C} \sim 85^{\circ}\text{C}$  で、SN75ALS176 は  $0^{\circ}\text{C} \sim 70^{\circ}\text{C}$  での動作が規定されています。

#### パッケージ情報

| 部品番号        | パッケージ <sup>(1)</sup> | 本体サイズ (公称)      |
|-------------|----------------------|-----------------|
| SNx5ALS176  | D (SOIC)             | 4.9mm × 3.91mm  |
|             | P (PDIP)             | 9.81mm × 6.35mm |
| SN75ALS176A | D (SOIC)             | 4.9mm × 3.91mm  |
|             | P (PDIP)             | 9.81mm × 6.35mm |
| SN75ALS176B | D (SOIC)             | 4.9mm × 3.91mm  |
|             | P (PDIP)             | 9.81mm × 6.35mm |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



#### 論理図 (正論理)

<sup>1</sup> これらのデバイスの特性は、TIA/EIA-485-A の要件を満たすがそれを上回りますが、ジェネレータ競合テスト (para.3.4.2)、およびジェネレータ電流制限 ( para 3.4.3) の場合は、これはあてはまりません。適用されるテスト電圧範囲は、SN75ALS176、SN75ALS176A、SN75ALS176B では  $-6\text{V} \sim 8\text{V}$ 、SN65ALS180 では  $-4\text{V} \sim 8\text{V}$  です。



## Table of Contents

|                                                |          |                                                                  |           |
|------------------------------------------------|----------|------------------------------------------------------------------|-----------|
| <b>1 特長</b> .....                              | <b>1</b> | <b>6 Parameter Measurement Information</b> .....                 | <b>11</b> |
| <b>2 概要</b> .....                              | <b>1</b> | <b>7 Detailed Description</b> .....                              | <b>14</b> |
| <b>3 改訂履歴</b> .....                            | <b>2</b> | 7.1 Functional Block Diagram.....                                | 14        |
| <b>4 Pin Configuration and Functions</b> ..... | <b>3</b> | 7.2 Device Functional Modes.....                                 | 14        |
| <b>5 Specifications</b> .....                  | <b>4</b> | <b>8 Application and Implementation</b> .....                    | <b>15</b> |
| 5.1 Absolute Maximum Ratings .....             | 4        | 8.1 Application Information.....                                 | 15        |
| 5.2 推奨動作条件.....                                | 4        | 8.2 Typical Application.....                                     | 15        |
| 5.3 Thermal Information.....                   | 4        | <b>9 Device and Documentation Support</b> .....                  | <b>16</b> |
| 5.4 Electrical Characteristics - Driver.....   | 5        | 9.1 Documentation Support.....                                   | 16        |
| 5.5 Switching Characteristics - Driver.....    | 5        | 9.2 ドキュメントの更新通知を受け取る方法.....                                      | 16        |
| 5.6 Switching Characteristics - Driver.....    | 6        | 9.3 サポート・リソース.....                                               | 16        |
| 5.7 Symbol Equivalents.....                    | 6        | 9.4 Trademarks.....                                              | 16        |
| 5.8 Electrical Characteristics - Receiver..... | 7        | 9.5 静電気放電に関する注意事項.....                                           | 16        |
| 5.9 Switching Characteristics - Receiver.....  | 7        | 9.6 用語集.....                                                     | 16        |
| 5.10 Switching Characteristics - Receiver..... | 8        | <b>10 Mechanical, Packaging, and Orderable Information</b> ..... | <b>16</b> |
| 5.11 Typical Characteristics.....              | 9        |                                                                  |           |

### 3 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision H (June 2000) to Revision I (January 2023)                       | Page |
|----------------------------------------------------------------------------------------|------|
| • ドキュメントをテキサス・インスツルメンツの最新フォーマットに変更.....                                                | 1    |
| • Deleted the Package thermal impedance from the <i>Absolute Maximum Ratings</i> ..... | 4    |
| • Added the <i>Thermal Information</i> table.....                                      | 4    |
| • Changed the <i>Typical Characteristics</i> graphs.....                               | 9    |

## 4 Pin Configuration and Functions

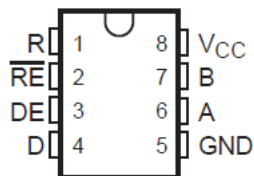


图 4-1. D or P Package (Top View)

表 4-1. Pin Functions

| NO | Name            | Type   | Description                                          |
|----|-----------------|--------|------------------------------------------------------|
| 1  | R               | O      | Receive data output                                  |
| 2  | RE              | I      | Receiver enable, active low                          |
| 3  | DE              | i      | Driver enable, active high                           |
| 4  | D               | I      | Driver data input                                    |
| 5  | GND             | GND    | Local device ground                                  |
| 6  | A               | I/O    | Driver output or receiver input (complementary to B) |
| 7  | B               | I/O    | Driver output or receiver input (complementary to A) |
| 8  | V <sub>CC</sub> | SUPPLY | 4.75-V to 5.25-V supply                              |

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                                              | MIN | MAX | UNIT |
|------------------|--------------------------------------------------------------|-----|-----|------|
| V <sub>CC</sub>  | Supply voltage <sup>(2)</sup>                                |     | 7   | V    |
|                  | Voltage range at any bus terminal                            | -7  | 12  | V    |
| V <sub>I</sub>   | Enable input voltage                                         |     | 5.5 | V    |
|                  | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |     | 260 | °C   |
| T <sub>stg</sub> | Storage temperature range                                    | -65 | 150 | °C   |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

### 5.2 推奨動作条件

(特に記述のない限り)

|                                    |                            |                 | 最小値  | 公称値 | 最大値      | 単位 |
|------------------------------------|----------------------------|-----------------|------|-----|----------|----|
| V <sub>CC</sub>                    | 電源電圧                       |                 | 4.75 | 5   | 5.25     | V  |
| V <sub>I</sub> または V <sub>IC</sub> | 任意のバス端子での入力電圧 (個別または同相モード) |                 |      |     | 12<br>-7 | V  |
| V <sub>IH</sub>                    | High レベル入力電圧               | D、DE、および RE     | 2    |     |          | V  |
| V <sub>IL</sub>                    | Low レベル入力電圧                | D、DE、および RE     |      |     | 0.8      | V  |
| V <sub>ID</sub>                    | 差動入力電圧 <sup>(1)</sup>      |                 |      |     | ±12      | V  |
| I <sub>OH</sub>                    | High レベル出力電流               | ドライバ            |      |     | -60      | mA |
|                                    |                            | レシーバ            |      |     | -400     | μA |
| I <sub>OL</sub>                    | Low レベル出力電流                | ドライバ            |      |     | 60       | mA |
|                                    |                            | レシーバ            |      |     | 8        |    |
| T <sub>A</sub>                     | 自由気流での動作温度                 | SN65ALS176      | -40  |     | 85       | °C |
|                                    |                            | SN75ALS176 シリーズ | 0    |     | 70       |    |

- (1) 差動入出力バス電圧は、反転端子 B を基準とした非反転端子 A の値として測定しています。

### 5.3 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | P (PDIP) | D (SOIC)<br>SN65 Devices | D (SOIC)<br>SN75 Devices | UNIT |
|-------------------------------|----------------------------------------------|----------|--------------------------|--------------------------|------|
|                               |                                              | 8-Pins   | 8-Pins                   | 8-Pin                    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 65.7     | 116.7                    | 110                      | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case thermal resistance          | 54.7     | 56.3                     | 44.1                     | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 42.1     | 63.4                     | 53.5                     | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 23       | 8.8                      | 4.8                      | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 41.7     | 62.6                     | 52.7                     | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | N/A      | N/A                      | N/A                      | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.4 Electrical Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER         |                                                                   | TEST CONDITIONS <sup>(1)</sup>    |                                                | MIN                                    | TYP <sup>(2)</sup> | MAX       | UNIT |
|-------------------|-------------------------------------------------------------------|-----------------------------------|------------------------------------------------|----------------------------------------|--------------------|-----------|------|
| V <sub>IK</sub>   | Input clamp voltage                                               | I <sub>I</sub> = –18 mA           |                                                |                                        |                    | –1.5      | V    |
| V <sub>O</sub>    | Output voltage                                                    | I <sub>O</sub> = 0                |                                                | 0                                      |                    | 6         | V    |
| V <sub>OD1</sub>  | Differential output voltage                                       | I <sub>O</sub> = 0                |                                                | 1.5                                    |                    | 6         | V    |
| V <sub>OD2</sub>  | Differential output voltage                                       | R <sub>L</sub> = 100 Ω            | See <a href="#">Figure 6-1</a>                 | ½ V <sub>OD1</sub> or 2 <sup>(3)</sup> |                    |           | V    |
|                   |                                                                   | R <sub>L</sub> = 54 Ω             | See <a href="#">Figure 6-1</a>                 | 1.5                                    | 2.5                | 5         | V    |
| V <sub>OD3</sub>  | Differential output voltage                                       | V <sub>test</sub> = –7 V to 12 V, | See <a href="#">Figure 6-2</a>                 | 1.5                                    |                    | 5         | V    |
| Δ V <sub>OD</sub> | Change in magnitude of differential output voltage <sup>(4)</sup> | R <sub>L</sub> = 54 Ω or 100 Ω    | See <a href="#">Figure 6-1</a>                 |                                        |                    | ±0.2      | V    |
| V <sub>OC</sub>   | Common-mode output voltage                                        | R <sub>L</sub> = 54 Ω or 100 Ω    | See <a href="#">Figure 6-1</a>                 |                                        |                    | 3<br>–1   | V    |
| Δ V <sub>OC</sub> | Change in magnitude of common-mode output voltage <sup>(4)</sup>  | R <sub>L</sub> = 54 Ω or 100 Ω    | See <a href="#">Figure 6-1</a>                 |                                        |                    | ±0.2      | V    |
| I <sub>O</sub>    | Output current                                                    | Outputs disabled <sup>(6)</sup>   | V <sub>O</sub> = 12 V<br>V <sub>O</sub> = –7 V |                                        |                    | 1<br>–0.8 | mA   |
| I <sub>IH</sub>   | High-level input current                                          | V <sub>I</sub> = 2.4 V            |                                                |                                        |                    | 20        | μA   |
| I <sub>IL</sub>   | Low-level input current                                           | V <sub>I</sub> = 0.4 V            |                                                |                                        |                    | –400      | μA   |
| I <sub>OS</sub>   | Short-circuit output current <sup>(5)</sup>                       | V <sub>O</sub> = –4 V             | SN65ALS176                                     |                                        |                    | –250      | mA   |
|                   |                                                                   | V <sub>O</sub> = –6 V             | SN75ALS176                                     |                                        |                    | –250      |      |
|                   |                                                                   | V <sub>O</sub> = 0                |                                                |                                        |                    | –150      |      |
|                   |                                                                   | V <sub>O</sub> = V <sub>CC</sub>  |                                                |                                        |                    | 250       |      |
|                   |                                                                   | V <sub>O</sub> = 8 V              |                                                |                                        |                    | 250       |      |
| I <sub>CC</sub>   | Supply current                                                    | No load                           | Outputs enabled                                |                                        | 23                 | 30        | mA   |
|                   |                                                                   |                                   | Outputs disabled                               |                                        | 19                 | 26        |      |

- (1) The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.  
(2) All typical values are at V<sub>CC</sub> = 5 V and T<sub>A</sub> = 25°C.  
(3) The minimum V<sub>OD2</sub> with a 100-Ω load is either 1/2 V<sub>OD1</sub> or 2 V, whichever is greater.  
(4) Δ|V<sub>OD</sub>| and Δ|V<sub>OC</sub>| are the changes in magnitude of VOD and VOC, respectively, that occur when the input is changed from one logic state to the other.  
(5) Duration of the short circuit should not exceed one second for this test.  
(6) This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

## 5.5 Switching Characteristics - Driver

### SN65ALS176

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER            |                                     | TEST CONDITIONS        |                         |                                | MIN | TYP <sup>(1)</sup> | MAX | UNIT |
|----------------------|-------------------------------------|------------------------|-------------------------|--------------------------------|-----|--------------------|-----|------|
| t <sub>d(OD)</sub>   | Differential output delay time      | R <sub>L</sub> = 54 Ω  | C <sub>L</sub> = 50 pF, | See <a href="#">Figure 6-3</a> |     |                    | 15  | ns   |
| t <sub>sk(p)</sub>   | Pulse skew <sup>(2)</sup>           | R <sub>L</sub> = 54 Ω  | C <sub>L</sub> = 50 pF, | See <a href="#">Figure 6-3</a> |     | 0                  | 2   | ns   |
| t <sub>sk(lim)</sub> | Pulse skew <sup>(3)</sup>           | R <sub>L</sub> = 54 Ω  | C <sub>L</sub> = 50 pF, | See <a href="#">Figure 6-3</a> |     |                    | 15  | ns   |
| t <sub>t(OD)</sub>   | Differential output transition time | R <sub>L</sub> = 54 Ω  | C <sub>L</sub> = 50 pF, | See <a href="#">Figure 6-3</a> |     | 8                  |     | ns   |
| t <sub>PZH</sub>     | Output enable time to high level    | R <sub>L</sub> = 110 Ω | C <sub>L</sub> = 50 pF, | See <a href="#">Figure 6-4</a> |     |                    | 80  | ns   |
| t <sub>PZL</sub>     | Output enable time to low level     | R <sub>L</sub> = 110 Ω | C <sub>L</sub> = 50 pF, | See <a href="#">Figure 6-5</a> |     |                    | 30  | ns   |
| t <sub>PHZ</sub>     | Output disable time from high level | R <sub>L</sub> = 110 Ω | C <sub>L</sub> = 50 pF, | See <a href="#">Figure 6-4</a> |     |                    | 50  | ns   |
| t <sub>PLZ</sub>     | Output disable time from low level  | R <sub>L</sub> = 110 Ω | C <sub>L</sub> = 50 pF, | See <a href="#">Figure 6-5</a> |     |                    | 30  | ns   |

- (1) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

- (2) Pulse skew is defined as the  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.  
(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

## 5.6 Switching Characteristics - Driver

### SN75ALS176, SN75ALS176A, SN75ALS176B

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER     |                                     |          | TEST CONDITIONS    |                       |                         | MIN | TYP <sup>(1)</sup> | MAX  | UNIT |
|---------------|-------------------------------------|----------|--------------------|-----------------------|-------------------------|-----|--------------------|------|------|
| $t_{d(OD)}$   | Differential output delay time      | 'ALS176  | $R_L = 54 \Omega$  | $C_L = 50 \text{ pF}$ | See <a href="#">6-3</a> | 3   | 8                  | 13   | ns   |
|               |                                     | 'ALS176A |                    |                       |                         | 4   | 7                  | 11.5 |      |
|               |                                     | 'ALS176B |                    |                       |                         | 5   | 8                  | 10   |      |
| $t_{sk(p)}$   | Pulse skew <sup>(2)</sup>           |          | $R_L = 54 \Omega$  | $C_L = 50 \text{ pF}$ | See <a href="#">6-3</a> |     | 0                  | 2    | ns   |
| $t_{sk(lim)}$ | Pulse skew <sup>(3)</sup>           | 'ALS176  | $R_L = 54 \Omega$  | $C_L = 50 \text{ pF}$ | See <a href="#">6-3</a> |     |                    | 10   | ns   |
|               |                                     | 'ALS176A |                    |                       |                         |     |                    | 7.5  |      |
|               |                                     | 'ALS176B |                    |                       |                         |     |                    | 5    |      |
| $t_{i(OD)}$   | Differential output transition time |          | $R_L = 54 \Omega$  | $C_L = 50 \text{ pF}$ | See <a href="#">6-3</a> |     | 8                  |      | ns   |
| $t_{PZH}$     | Output enable time to high level    |          | $R_L = 110 \Omega$ | $C_L = 50 \text{ pF}$ | See <a href="#">6-4</a> |     | 23                 | 50   | ns   |
| $t_{PZL}$     | Output enable time to low level     |          | $R_L = 110 \Omega$ | $C_L = 50 \text{ pF}$ | See <a href="#">6-5</a> |     | 14                 | 20   | ns   |
| $t_{PHZ}$     | Output disable time from high level |          | $R_L = 110 \Omega$ | $C_L = 50 \text{ pF}$ | See <a href="#">6-4</a> |     | 20                 | 35   | ns   |
| $t_{PLZ}$     | Output disable time from low level  |          | $R_L = 110 \Omega$ | $C_L = 50 \text{ pF}$ | See <a href="#">6-5</a> |     | 8                  | 17   | ns   |

- (1) All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .  
(2) Pulse skew is defined as the  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.  
(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

## 5.7 Symbol Equivalents

| DATA-SHEET<br>PARAMETER | TIA/EIA-422-B           | TIA/EIA-485-A                             |
|-------------------------|-------------------------|-------------------------------------------|
| $V_O$                   | $V_{oa}, V_{ob}$        | $V_{oa}, V_{ob}$                          |
| $ V_{OD1} $             | $V_o$                   | $V_o$                                     |
| $ V_{OD2} $             | $V_t(R_L = 100 \Omega)$ | $V_t(R_L = 54 \Omega)$                    |
| $ V_{OD3} $             | None                    | $V_t$<br>(test termination measurement 2) |
| $\Delta V_{OD} $        | $  V_t  -  V_t  $       | $  V_t  -  V_t  $                         |
| $V_{OC}$                | $ V_{os} $              | $ V_{os} $                                |
| $\Delta V_{OC} $        | $ V_{os} - V_{os} $     | $ V_{os} - V_{os} $                       |
| $I_{OS}$                | $ I_{sa} ,  I_{sb} $    | None                                      |
| $I_O$                   | $ I_{xa} ,  I_{xb} $    | $I_{ia}, I_{ib}$                          |

## 5.8 Electrical Characteristics - Receiver

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)

| PARAMETER        |                                                           | TEST CONDITIONS                                             |                            | MIN                 | TYP <sup>(1)</sup> | MAX  | UNIT |
|------------------|-----------------------------------------------------------|-------------------------------------------------------------|----------------------------|---------------------|--------------------|------|------|
| V <sub>IT+</sub> | Positive-going input threshold voltage                    | V <sub>O</sub> = 2.7 V,                                     | I <sub>O</sub> = –0.4 mA   |                     |                    | 0.2  | V    |
| V <sub>IT–</sub> | Negative-going input threshold voltage                    | V <sub>O</sub> = 0.5 V,                                     | I <sub>O</sub> = 8 mA      | –0.2 <sup>(2)</sup> |                    |      | V    |
| V <sub>hys</sub> | Hysteresis voltage (V <sub>IT+</sub> – V <sub>IT–</sub> ) |                                                             |                            |                     | 60                 |      | mV   |
| V <sub>IK</sub>  | Enable-input clamp voltage                                | I <sub>I</sub> = –18 mA                                     |                            |                     |                    | –1.5 | V    |
| V <sub>OH</sub>  | High-level output voltage                                 | V <sub>ID</sub> = 200 mV,<br>See <a href="#">Figure 6-6</a> | I <sub>OH</sub> = –400 mA, | 2.7                 |                    |      | V    |
| V <sub>OL</sub>  | Low-level output voltage                                  | V <sub>ID</sub> = –200 mV,<br>See <a href="#">Figure 6</a>  | I <sub>OL</sub> = 8 mA,    |                     |                    | 0.45 | V    |
| I <sub>OZ</sub>  | High-impedance-state output current                       | V <sub>O</sub> = 0.4 V to 2.4 V                             |                            |                     |                    | ±20  | μA   |
| V <sub>I</sub>   | Line input current                                        | Other input = 0 V <sup>(3)</sup>                            | V <sub>I</sub> = 12 V      |                     |                    | 1    | mA   |
|                  |                                                           |                                                             | V <sub>I</sub> = –7 V      |                     |                    | –0.8 |      |
| I <sub>IH</sub>  | High-level-enable input current                           | V <sub>IH</sub> = 2.7 V                                     |                            |                     |                    | 20   | μA   |
| I <sub>IL</sub>  | Low-level-enable input current                            | V <sub>IL</sub> = 0.4 V                                     |                            |                     |                    | –100 | μA   |
| r <sub>I</sub>   | Input resistance                                          |                                                             |                            | 12                  | 20                 |      | kΩ   |
| I <sub>OS</sub>  | Short-circuit output current                              | V <sub>ID</sub> = 200 mV,                                   | V <sub>O</sub> = 0         | –15                 |                    | –85  | mA   |
| I <sub>CC</sub>  | Supply current                                            | No load                                                     | Outputs enabled            |                     | 23                 | 30   | mA   |
|                  |                                                           |                                                             | Outputs disabled           |                     | 19                 | 26   |      |

(1) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

(3) This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions.

## 5.9 Switching Characteristics - Receiver

### SN65ALS176

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER            |                                     | TEST CONDITIONS                                                      |                                | MIN | TYP <sup>(1)</sup> | MAX | UNIT |
|----------------------|-------------------------------------|----------------------------------------------------------------------|--------------------------------|-----|--------------------|-----|------|
| t <sub>pd</sub>      | Propagation time                    | V <sub>ID</sub> = –1.5 V to 1.5 V,<br>See <a href="#">Figure 6-7</a> | C <sub>L</sub> = 15 pF,        |     |                    | 25  | ns   |
| t <sub>sk(p)</sub>   | Pulse skew <sup>(2)</sup>           | V <sub>ID</sub> = –1.5 V to 1.5 V,<br>See <a href="#">Figure 6-7</a> | C <sub>L</sub> = 15 pF,        |     | 0                  | 2   | ns   |
| t <sub>sk(lim)</sub> | Pulse skew <sup>(3)</sup>           | R <sub>L</sub> = 54 Ω<br>See <a href="#">Figure 6-3</a>              | C <sub>L</sub> = 50 pF,        |     |                    | 15  | ns   |
| t <sub>PZH</sub>     | Output enable time to high level    | C <sub>L</sub> = 15 pF,                                              | See <a href="#">Figure 6-8</a> |     | 11                 | 18  | ns   |
| t <sub>PZL</sub>     | Output enable time to low level     | C <sub>L</sub> = 15 pF,                                              | See <a href="#">Figure 6-8</a> |     | 11                 | 18  | ns   |
| t <sub>PHZ</sub>     | Output disable time from high level | C <sub>L</sub> = 15 pF,                                              | See <a href="#">Figure 6-8</a> |     |                    | 50  | ns   |
| t <sub>PLZ</sub>     | Output disable time from low level  | C <sub>L</sub> = 15 pF,                                              | See <a href="#">Figure 6-8</a> |     |                    | 30  | ns   |

(1) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

(2) Pulse skew is defined as the |t<sub>PLH</sub> – t<sub>PHL</sub>| of each channel of the same device.

(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

## 5.10 Switching Characteristics - Receiver

### SN75ALS176, SN75ALS176A, SN75ALS176B

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER     |                                     |          | TEST CONDITIONS                                                       |                         | MIN  | TYP <sup>(1)</sup> | MAX  | UNIT |
|---------------|-------------------------------------|----------|-----------------------------------------------------------------------|-------------------------|------|--------------------|------|------|
| $t_{pd}$      | Propagation time                    | 'ALS176  | $V_{ID} = -1.5\text{ V to }1.5\text{ V}$ ,<br>See <a href="#">6-7</a> | $C_L = 15\text{ pF}$ ,  | 9    | 14                 | 19   | ns   |
|               |                                     | 'ALS176A |                                                                       |                         | 10.5 | 14                 | 18   |      |
|               |                                     | 'ALS176B |                                                                       |                         | 11.5 | 13                 | 16.5 |      |
| $t_{sk(p)}$   | Pulse skew <sup>(2)</sup>           |          | $V_{ID} = -1.5\text{ V to }1.5\text{ V}$ ,<br>See <a href="#">6-7</a> | $C_L = 15\text{ pF}$ ,  |      | 0                  | 2    | ns   |
| $t_{sk(lim)}$ | Pulse skew <sup>(3)</sup>           | 'ALS176  | $R_L = 54\ \Omega$<br>See <a href="#">6-3</a>                         | $C_L = 50\text{ pF}$ ,  |      |                    | 10   | ns   |
|               |                                     | 'ALS176A |                                                                       |                         |      |                    | 7.5  |      |
|               |                                     | 'ALS176B |                                                                       |                         |      |                    | 5    |      |
| $t_{PZH}$     | Output enable time to high level    |          | $C_L = 15\text{ pF}$ ,                                                | See <a href="#">6-8</a> |      | 7                  | 14   | ns   |
| $t_{PZL}$     | Output enable time to low level     |          | $C_L = 15\text{ pF}$ ,                                                | See <a href="#">6-8</a> |      | 20                 | 35   | ns   |
| $t_{PHZ}$     | Output disable time from high level |          | $C_L = 15\text{ pF}$ ,                                                | See <a href="#">6-8</a> |      | 20                 | 35   | ns   |
| $t_{PLZ}$     | Output disable time from low level  |          | $C_L = 15\text{ pF}$ ,                                                | See <a href="#">6-8</a> |      | 8                  | 17   | ns   |

(1) All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(2) Pulse skew is defined as the  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.

(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

## 5.11 Typical Characteristics

Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

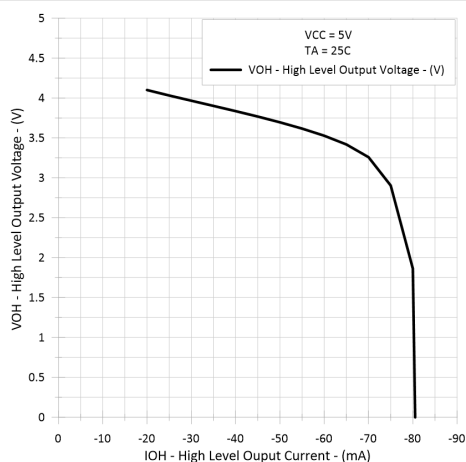


Figure 5-1. Driver High-Level Output Voltage vs High-Level Output Current

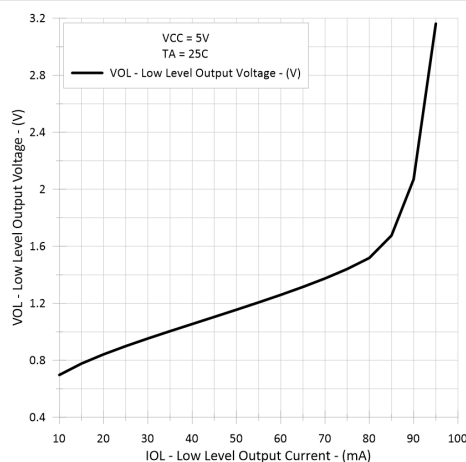


Figure 5-2. Driver Low-Level Output Voltage vs Low-Level Output Current

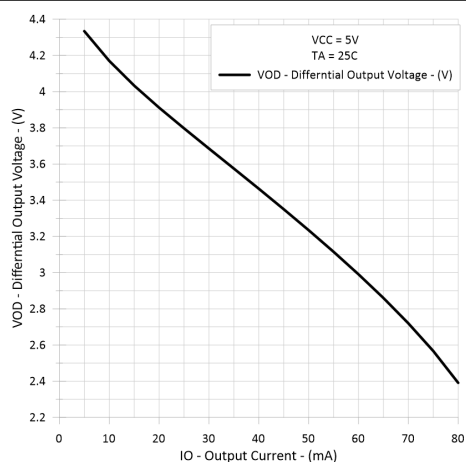


Figure 5-3. Driver Differential Output Voltage vs Output Current

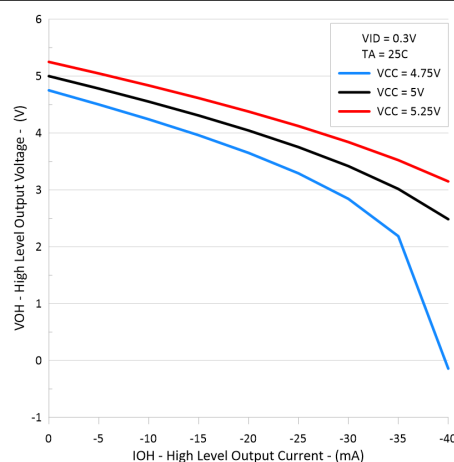


Figure 5-4. Receiver High-Level Output Voltage vs High-Level Output Current

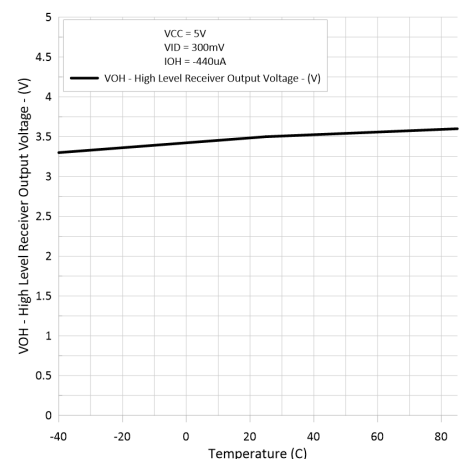


Figure 5-5. Receiver High-Level Output Voltage vs Free-Air Temperature

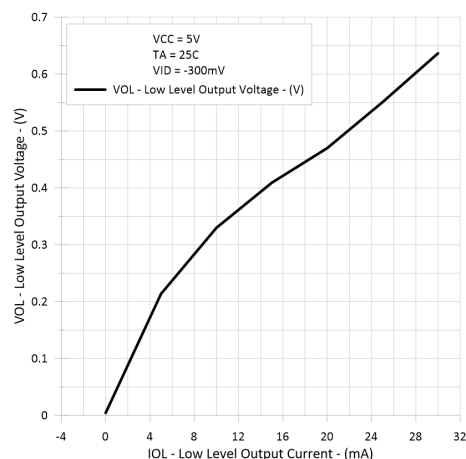
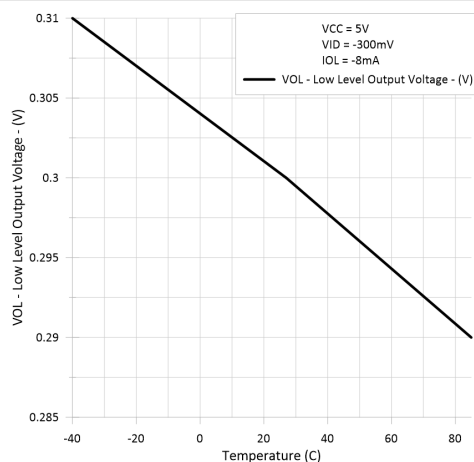


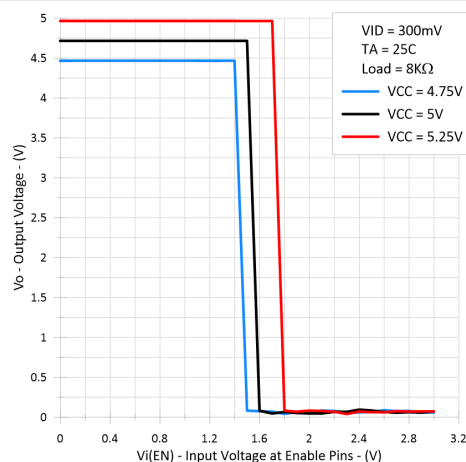
Figure 5-6. Receiver Low-Level Output Voltage vs Low-Level Output Current

## 5.11 Typical Characteristics (continued)

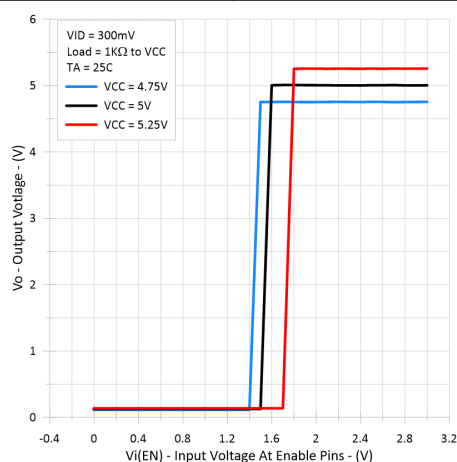
Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.



5-7. Receiver Low-Level Output Voltage vs Free-Air Temperature



5-8. Receiver Output Voltage vs Enable Voltage



5-9. Receiver Output Voltage vs Enable Voltage

## 6 Parameter Measurement Information

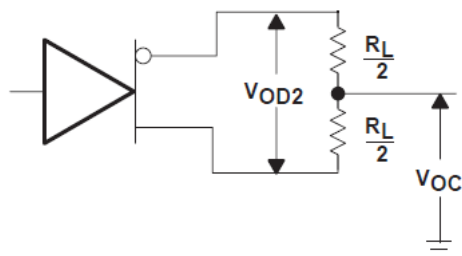


图 6-1. Driver  $V_{OD2}$  and  $V_{OC}$

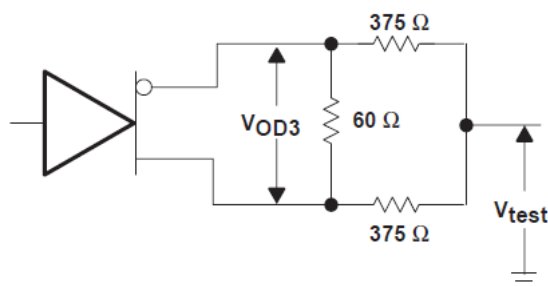
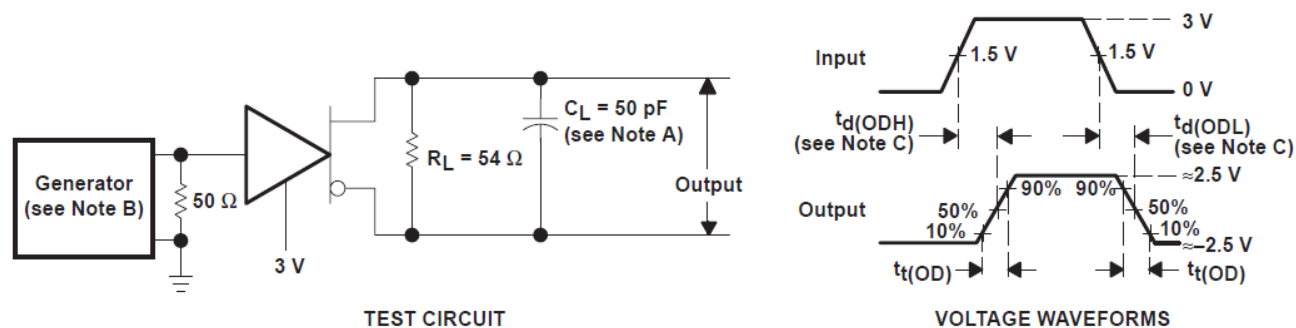
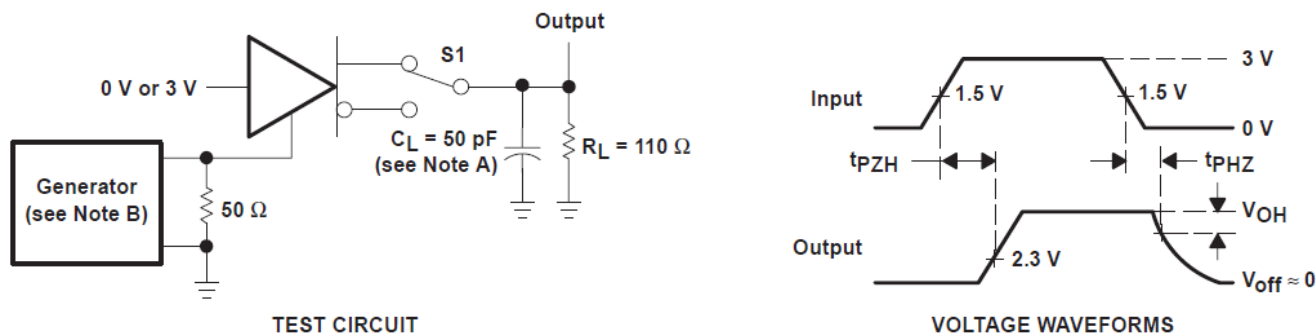


图 6-2. Driver  $V_{OD3}$



- A.  $C_L$  includes probe and jig capacitance.  
B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .

图 6-3. Driver Test Circuit and Voltage Waveforms



- A.  $C_L$  includes probe and jig capacitance.

- B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .

图 6-4. Driver Test Circuit and Voltage Waveforms

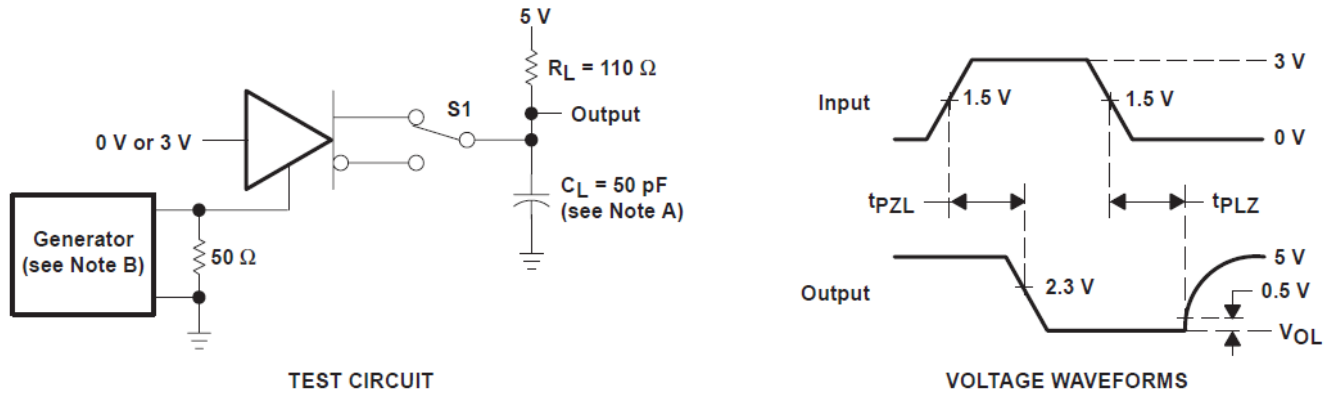


图 6-5. Driver Test Circuit and Voltage Waveforms

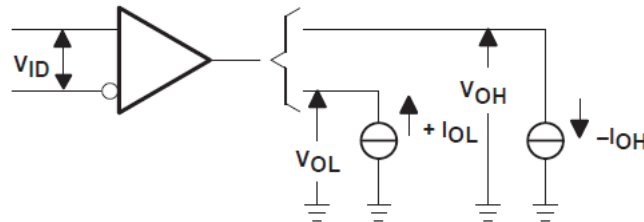
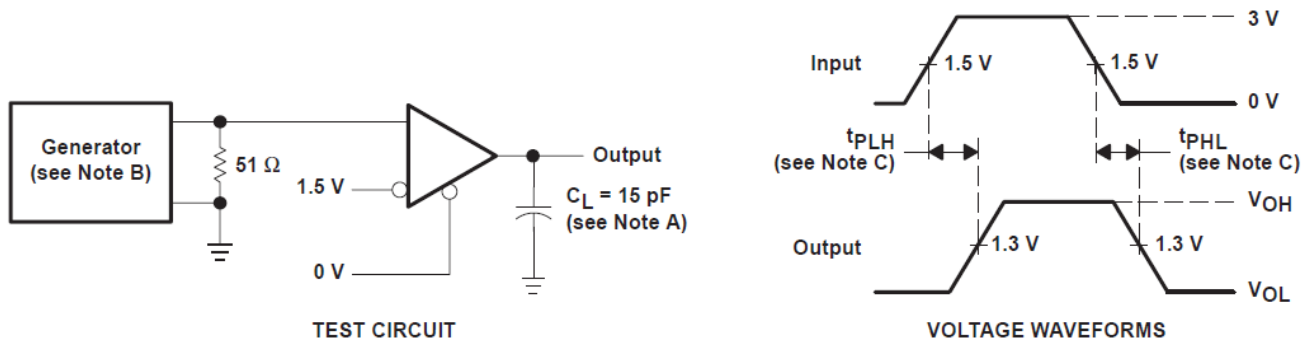
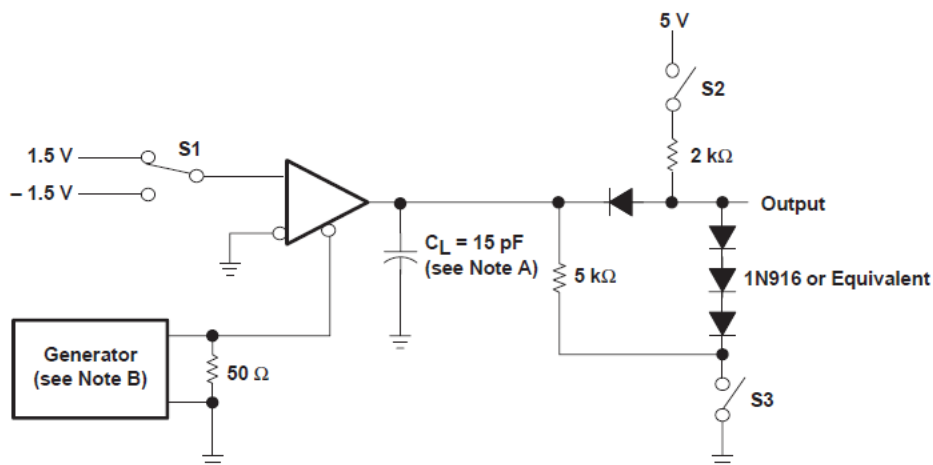


图 6-6. Receiver  $V_{OH}$  and  $V_{OL}$  Test Circuit

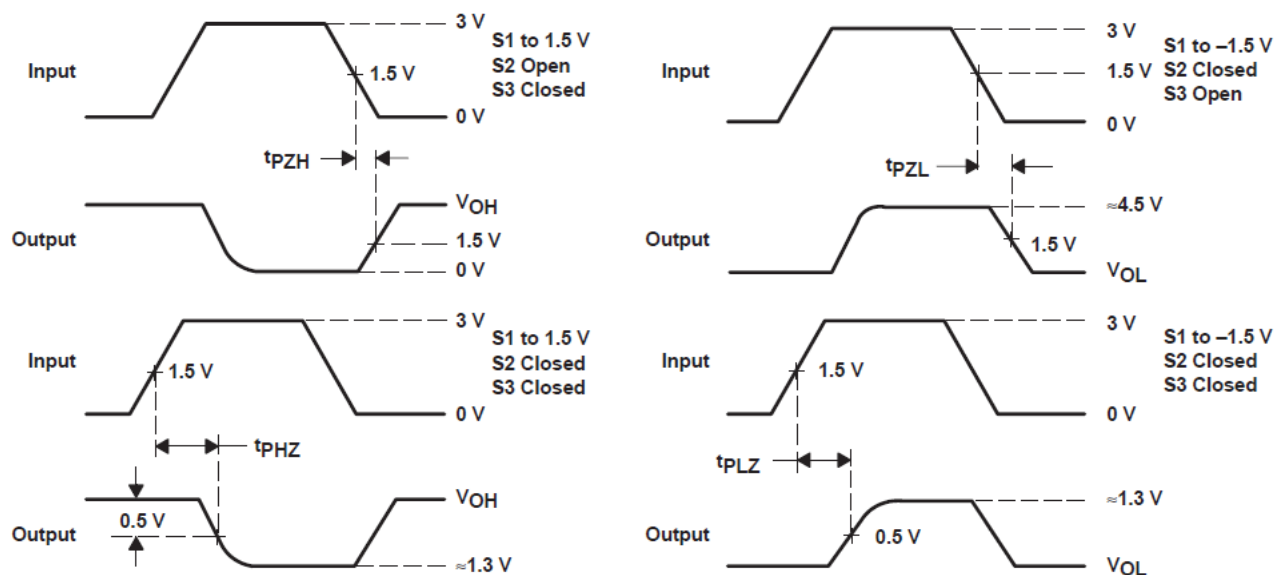


- A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .  
 C.  $t_{pd} = t_{PLH}$  or  $t_{PHL}$ .

图 6-7. Receiver Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

- A.  $C_L$  includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .

图 6-8. Receiver Test Circuit and Voltage Waveforms

## 7 Detailed Description

### 7.1 Functional Block Diagram

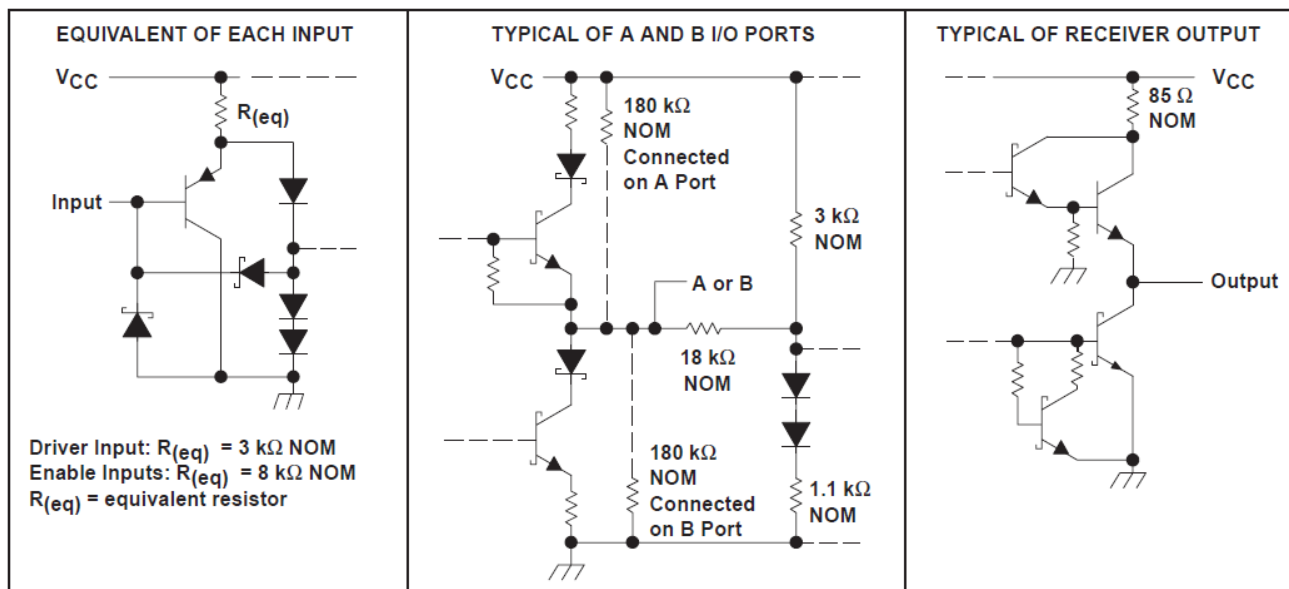


图 7-1. Schematic of Inputs and Outputs

### 7.2 Device Functional Modes

#### Function Tables

表 7-1. Driver<sup>(1)</sup>

| INPUT<br>D | ENABLE<br>DE | OUTPUTS |   |
|------------|--------------|---------|---|
|            |              | A       | B |
| H          | H            | H       | L |
| L          | H            | L       | H |
| X          | L            | Z       | Z |

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

表 7-2. Receiver<sup>(1)</sup>

| DIFFERENTIAL INPUTS<br>A-B                | ENABLE<br>RE | OUTPUT<br>R |
|-------------------------------------------|--------------|-------------|
| $V_{ID} \geq 0.2 \text{ V}$               | L            | H           |
| $-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$ | L            | ?           |
| $V_{ID} \leq -0.2 \text{ V}$              | L            | L           |
| X                                         | H            | Z           |
| Inputs open                               | L            | H           |

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

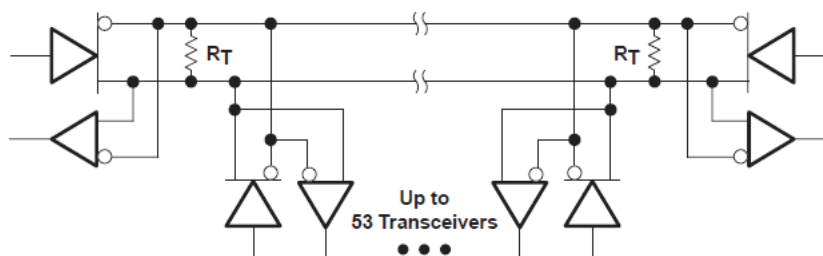
## 8 Application and Implementation

### 注

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### 8.1 Application Information

### 8.2 Typical Application



- A. The line should terminate at both ends in its characteristic impedance ( $R_T = Z_0$ ). Stub lengths off the main line should be kept as short as possible.

図 8-1. Typical Application Circuit

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

### 9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](https://ti.com) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 9.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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### 9.4 Trademarks

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### 9.5 静電気放電に関する注意事項



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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 9.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN65ALS176D</a>   | Obsolete      | Production           | SOIC (D)   8   | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | 65A176              |
| <a href="#">SN65ALS176DR</a>  | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 65A176              |
| SN65ALS176DR.A                | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 65A176              |
| SN65ALS176DR1G4               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 65A176              |
| SN65ALS176DR1G4.A             | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 65A176              |
| <a href="#">SN75ALS176AD</a>  | Active        | Production           | SOIC (D)   8   | 75   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 7A176A              |
| SN75ALS176AD.A                | Active        | Production           | SOIC (D)   8   | 75   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 7A176A              |
| <a href="#">SN75ALS176ADR</a> | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 7A176A              |
| SN75ALS176ADR.A               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 7A176A              |
| SN75ALS176ADRG4               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 7A176A              |
| <a href="#">SN75ALS176AP</a>  | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | 75ALS176A           |
| SN75ALS176AP.A                | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | 75ALS176A           |
| <a href="#">SN75ALS176BD</a>  | Obsolete      | Production           | SOIC (D)   8   | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | 7A176B              |
| <a href="#">SN75ALS176BDR</a> | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | (75A176, 7A176B)    |
| SN75ALS176BDR.A               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | (75A176, 7A176B)    |
| <a href="#">SN75ALS176BP</a>  | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | 75ALS176B           |
| SN75ALS176BP.A                | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | 75ALS176B           |
| <a href="#">SN75ALS176D</a>   | Obsolete      | Production           | SOIC (D)   8   | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | 75A176              |
| <a href="#">SN75ALS176P</a>   | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | 75ALS176            |
| SN75ALS176P.A                 | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | 75ALS176            |
| SN75ALS176PE4                 | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | 75ALS176            |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65ALS176DR    | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN65ALS176DR1G4 | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN75ALS176ADR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN75ALS176BDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65ALS176DR    | SOIC         | D               | 8    | 2500 | 340.5       | 336.1      | 25.0        |
| SN65ALS176DR1G4 | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| SN75ALS176ADR   | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| SN75ALS176BDR   | SOIC         | D               | 8    | 2500 | 340.5       | 336.1      | 25.0        |

## TUBE



\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN75ALS176AD   | D            | SOIC         | 8    | 75  | 507    | 8      | 3940   | 4.32   |
| SN75ALS176AD.A | D            | SOIC         | 8    | 75  | 507    | 8      | 3940   | 4.32   |
| SN75ALS176AP   | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| SN75ALS176AP.A | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| SN75ALS176BP   | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| SN75ALS176BP.A | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| SN75ALS176P    | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| SN75ALS176P.A  | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| SN75ALS176PE4  | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |



## PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

**D0008A**

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



## SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

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