TEXAS INSTRUMENTS
TAS5825P
JAJSI51A – MAY 2019 – REVISED JANUARY 2023

TAS5825P Hybrid-Pro アルゴリズム搭載、4.5V～26.4V、38W ステレオ、デジタル入力、高効率、閉ループ Class-D オーディオ・アンプ

Texas Instruments
Burr-Brown Audio

1 特長

- Hybrid-Pro による高効率の Class-D 動作
  - 固定電源電圧ソリューションと比べて、約 50% 長いバッテリ動作時間
  - 90% を超える電力効率、90mΩ の $R_{DS(on)}$
  - 低い静止電流：20mA 未満 (PVDD = 12V)
- 複数の出力構成をサポート
  - 1.0 モードで 1 × 53W (4Ω、22V、THD+N = 1%)
  - 1.0 モードで 1 × 65 W (4Ω、22V、THD+N = 10%)
  - 2.0 モードで 2 × 30W (8Ω、24V、THD+N = 1%)
  - 2.0 モードで 2 × 38W (8Ω、24V、THD+N = 10%)
- 優れたオーディオ性能：
  - THD+N ≤ 0.03% (1W、1kHz、PVDD = 12V)
  - SNR ≥ 110dB (A-weighted)、ICN ≤ 35μVRMS
- 柔軟なオーディオ I/O：
  - 32、44.1、48、88.2、96 kHz の SR をサポート
  - I^2S、LJ、RJ、TDM フォーマットをサポート
  - 3 線式のデジタル・オーディオ・インターフェイスをサポート
- 柔軟な処理機能
  - 3 バンドの高度な DRC + AGL、2 × 15 BQ
  - PVDD センシングにより、電圧レール降下時のクリッピング歪みを防止
  - 最大 4ms の先読み遅延バッファを使用した Hybrid-Pro アルゴリズムのオーディオ信号トラッキング
  - (オプション) 8 または 16 の Hybrid-Pro DC-DC 制御ステップ (最大 10ms のピーク・サンプル・ホールド付き)
- 柔軟な電源構成：
  - PVDD：4.5V～26.4V
  - DVDD および I/O：1.8V または 3.3V
- 優れた自己保護機能を内蔵：
  - 過電流エラー (OCE)
  - サイクル単位の電流制限
  - 過熱警告 (OTW)
  - 過熱エラー (OTE)
  - 低電圧/過電圧誤動作防止 (UVLO、OVLO)
- システム統合が簡単：
  - I^2C ソフトウェア制御
  - ソリューション・サイズの低減：
    - 5 × 5mm の小型パッケージ
    - 開ループの Class-D デバイスと比べて少ない受動部品数
    - ほとんどのアプリケーションでは、大容量電解コンデンサや大型のインダクタが不要

2 アプリケーション

- バッテリ駆動スピーカー
- セットトップ・ボックス (STB)
- サウンドバーまたはサブウーファー
- ワイヤレスまたは Bluetooth スピーカー
- 熱または効率の制約が厳しいオーディオ・システム

3 概要

TAS5825P は、先進の Hybrid-Pro アルゴリズムを備えたステレオ、高効率、閉ループ Class-D オーディオ・アンプであり、クリッピング歪みを発生させずにシステム効率を高めることができます。

通常、オーディオ・アンプの電源電圧 (PVDD) は DC-DC コンバータで供給されます。固定 PVDD に比べて、オーディオ信号に基づいて変化する可変 PVDD は、大幅に効率を向上させ、アイドル電流を低減し、発熱を低減します。

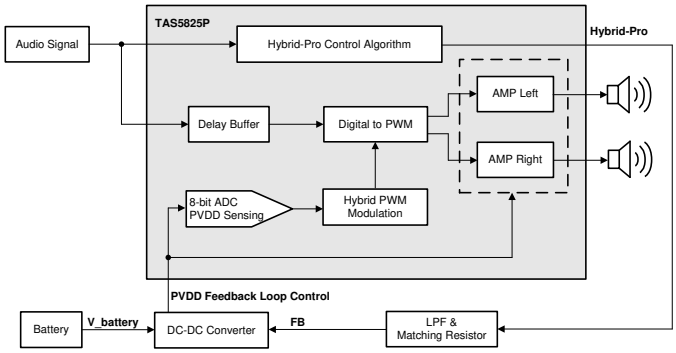
TAS5825P の強力なオーディオ DSP コアは、Hybrid-Pro と呼ぶ独自のアルゴリズムを実装しています。Hybrid-Pro アルゴリズムは、予測されるオーディオ電力の需要を検出し、Hybrid-Pro フィードバック・ピン (HPFB) により、前段の DC-DC コンバータに PWM 制御信号を出力します。TAS5825P は、オーディオ信号を先読みしてオーディオ・クリッピング歪みを防止するために最大 4ms の遅延バッファをサポートしています。各種の実験において TAS5825P は、連続的に音楽を再生しながら、1S および 2S バッテリの動作時間を 50% 以上延長しました。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
TAS5825P	VQFN (32) RHB	5.00mm × 5.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (May 2019) to Revision A (January 2023)	Page
• SPI に言及している場合、すべての旧式の用語をコントローラおよびペリフェラルに変更	1
• SPI に言及している場合、すべての旧式の用語を POCI および PICO に変更	1
• Changed figures in *Typical Characteristics* section	11

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5 Device Comparison Table

DEVICE NAME	$R_{DS(on)}$	DSP Audio Process Flows
TAS5825P	90 mΩ	Hybrid-Pro Algorithm for Audio Class-H Envelope Tracking
TAS5825M	90 mΩ	Flexible DSP Process Flows: Smart Amp, Sound Field Spatializer, 192 kHz Processing
TAS5805M	180 mΩ	ROM Fixed Process Flows

6 Pin Configuration and Functions

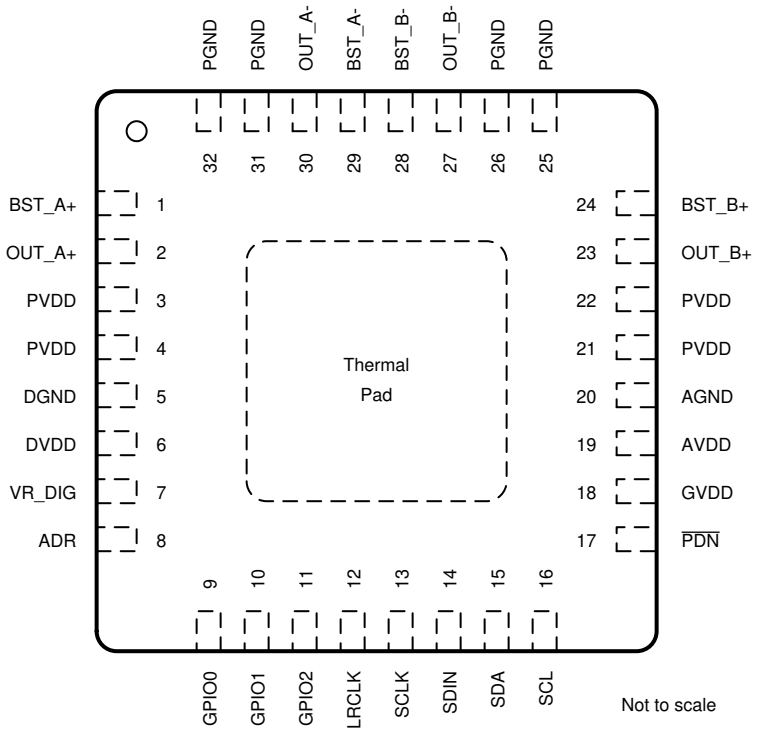


図 6-1. RHB Package 32-Pin VQFN

表 6-1. Pin Functions Table

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
DGND	5	P	Digital ground
DVDD	6	P	3.3-V or 1.8-V digital power supply
VR_DIG	7	P	Internally regulated 1.5-V digital supply voltage. This pin must not be used to drive external devices
ADR	8	AI	A table of resistor value (Pull down to GND) decides device I2C address. See 表 9-5.
GPIO0	9	DI/O	General-purpose input/output, function of this pin can be programmed by register (Register Address 0x60h and 0x61h). Can be configured to be CMOS output or Open drain output (HPFB: Hybrid-Pro Feedback, WARNZ or FAULTZ)
GPIO1	10	DI/O	General-purpose input/output, function of this pin can be programmed by register (Register Address 0x60h and 0x62h). Can be configured to be CMOS output or Open drain output (HPFB: Hybrid-Pro Feedback, WARNZ or FAULTZ)
GPIO2	11	DI/O	General-purpose input/output, function of this pin can be programmed by register (Register Address 0x60h and 0x63h). Can be configured to be CMOS output or Open drain output (HPFB: Hybrid-Pro Feedback, WARNZ or FAULTZ)
LRCLK	12	DI	Word select clock for the digital signal that is active on the serial port's input data line. In I^2S, LJ and RJ, this corresponds to the left channel and right channel boundary. In TDM mode, this corresponds to the frame sync boundary.
SCLK[2]	13	DI	Bit clock for the digital signal that is active on the input data line of the serial data port. Sometimes, this pin also be written as "bit clock (BCLK)"

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表 6-1. Pin Functions Table (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
SDIN	14	DI	Data line to the serial data port
SDA	15	DI/O	I2C serial control data interface input/output
SCL	16	DI	I2C serial control clock input
$\overline{\text{PDN}}$	17	DI	Power down, active-low. $\overline{\text{PDN}}$ place the amplifier in Shutdown, turn off all internal regulators.
GVDD	18	P	Gate drive internal regulator output. This pin must not be used to drive external devices
AVDD	19	P	Internally regulated 5-V analog supply voltage. This pin must not be used to drive external devices
AGND	20	P	Analog ground
PVDD	3	P	PVDD voltage input
	4	P	
	21	P	
	22	P	
PGND	25	P	Ground reference for power device circuitry. Connect this pin to system ground.
	26	P	
	31	P	
	32	P	
OUT_B+	23	O	Positive pin for differential speaker amplifier output B
BST_B+	24	P	Connection point for the OUT_B+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B+
OUT_B-	27	O	Negative pin for differential speaker amplifier output B
BST_B-	28	P	Connection point for the OUT_B- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B-
BST_A-	29	P	Connection point for the OUT_A- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A-
OUT_A-	30	O	Negative pin for differential speaker amplifier output A
BST_A+	1	P	Connection point for the OUT_A+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A+
OUT_A+	2	O	Positive pin for differential speaker amplifier output A
PowerPAD™		P	Connect to the system Ground

(1) AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, DI/O = Digital Bi-directional (input and output), P = Power, G = Ground (0 V)
(2) Typically written "bit clock (BCLK)" in some audio codecs.

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7 Specifications

7.1 Absolute Maximum Ratings

Free-air room temperature 25°C (unless otherwise noted) (1)

		MIN	MAX	UNIT
DVDD	Low-voltage digital supply	–0.3	3.9	V
PVDD	PVDD supply	–0.3	30	V
$V_{I(DigIn)}$	DVDD referenced digital inputs(2)	–0.5	V_{DVDD} + 0.5	V
$V_{I(SPK_OUTxx)}$	Voltage at speaker output pins	–0.3	32	V
T_A	Ambient operating temperature,	–25	85	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) DVDD referenced digital pins include: ADR, GPIO0, GPIO1,GPIO2, LRCLK, SCLK, SDIN,,SCL, SDA, $\overline{PDN}$

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(POWER)}$	Power supply inputs	DVDD	1.62		3.63	V
		PVDD	4.5		26.4	
R_{SPK}	Minimum speaker load	BTL Mode	3.2	4		Ω
		PBTL Mode	1.6	2		Ω
L_{OUT}	Minimum inductor value in LC filter under short-circuit condition		1	4.7		µH

7.4 Thermal Information

THERMAL METRIC(1)		TAS5825P VQFN (RHB) 32 PINS			UNIT
		JEDEC STANDARD 2-LAYER PCB	JEDEC STANDARD 4-LAYER PCB	TAS5825PEVM-4 4-LAYER PCB	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	N/A	30.0	24.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	N/A	19.1	19.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	9.9	9.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	N/A	0.2	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	N/A	10.5	8.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

Free-air room temperature 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital I/O						
|IIH|	Input logic high current level for DVDD referenced digital input pins	$V_{IN(DigIn)} = V_{DVDD}$			10	µA
|IIL|	Input logic low current level for DVDD referenced digital input pins	$V_{IN(DigIn)}$ = 0 V			–10	µA
$V_{IH(Digin)}$	Input logic high threshold for DVDD referenced digital inputs		70%			V_{DVDD}
$V_{IL(Digin)}$	Input logic low threshold for DVDD referenced digital inputs				30%	V_{DVDD}
$V_{OH(Digin)}$	Output logic high voltage level	I_{OH} = 4 mA	80%			V_{DVDD}
$V_{OL(Digin)}$	Output logic low voltage level	I_{OH} = –4 mA			20%	V_{DVDD}
I^2C Control Port						
$C_{L(I2C)}$	Allowable load capacitance for each I^2C Line				400	pF
$f_{SCL(fast)}$	Support SCL frequency	No wait states, fast mode			400	kHz
$f_{SCL(slow)}$	Support SCL frequency	No wait states, slow mode			100	kHz
Serial Audio Port						
t_{DLY}	Required LRCK/FS to SCLK rising edge delay		5			ns
D_{SCLK}	Allowable SCLK duty cycle		40%		60%	
f_S	Supported input sample rates		32		192	kHz
f_{SCLK}	Supported SCLK frequencies		32		64	f_S
f_{SCLK}	SCLK frequency				24.576	MHz
Speaker Amplifier (All Output Configurations)						
t_{off}	Turn-off Time	Excluding volume ramp			10	ms
I_{CC}	Quiescent supply current of DVDD	$\overline{PDN}$ = 2 V, DVDD = 3.3 V, Play mode, General Audio Process flow with full DSP running		25.5		mA
I_{CC}	Quiescent supply current of DVDD	$\overline{PDN}$ = 2 V, DVDD = 3.3 V, Sleep mode		0.87		mA
I_{CC}	Quiescent supply current of DVDD	$\overline{PDN}$ = 2 V, DVDD = 3.3 V, Deep Sleep mode		0.82		mA
I_{CC}	Quiescent supply current of DVDD	$\overline{PDN}$ = 0.8 V, DVDD = 3.3 V, Shutdown mode		7.4		µA
I_{CC}	Quiescent supply current of PVDD	$\overline{PDN}$ = 2 V, PVDD = 13.5 V, No Load, LC filter = 10 µH + 0.68 µF, F_{SW} = 384 kHz, Hybrid Modulation, Play Mode		29.5		mA
I_{CC}	Quiescent supply current of PVDD	$\overline{PDN}$ = 2 V, PVDD = 13.5 V, No Load, LC filter = 22 µH + 0.68 µF, F_{SW} = 384 kHz, Hybrid Modulation, Play Mode		20.5		mA
I_{CC}	Quiescent supply current of PVDD	$\overline{PDN}$ = 2 V, PVDD = 13.5 V, No Load, LC filter = 10 µH + 0.68 µF, F_{SW} = 384 kHz, Output Hiz Mode		10.7		mA
I_{CC}	Quiescent supply current of PVDD	$\overline{PDN}$ = 2 V, PVDD = 13.5 V, No Load, LC filter = 10 µH + 0.68 µF, Fsw = 384 kHz, Sleep Mode		7.26		mA
I_{CC}	Quiescent supply current of PVDD	$\overline{PDN}$ = 2 V, PVDD = 13.5 V, No Load, LC filter = 10 µH + 0.68 µF, F_{sw} = 384 kHz, Deep Sleep Mode		12.01		µA
I_{CC}	Quiescent supply current of PVDD	$\overline{PDN}$ = 0.8 V, PVDD = 13.5 V, No Load, LC filter = 10 µH + 0.68 µF, F_{SW} = 384 kHz, Shutdown Mode		7.8		µA
$A_{V(SPK_AMP)}$	Programmable Gain	Value represents the "peak voltage" disregarding clipping due to lower PVDD). Measured at 0 dB input (1FS)	4.87		29.5	V
$\Delta A_{V(SPK_AMP)}$	Amplifier gain error	Gain = 29.5 V_P		0.5		dB
f_{SPK_AMP}	Switching frequency of the speaker amplifier			384		kHz
				768		kHz

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7.5 Electrical Characteristics (continued)

Free-air room temperature 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(on)}$	Drain-to-source on resistance of the individual output MOSFETs	FET + Metallization.		90		mΩ
OCE_{THRES}	Over-Current Error Threshold	Any short to supply, ground, or other channels		7.5		A
	Over-Current cycle-by-cycle limit			6.5		A
$OVE_{THRES(PVDD}$	PVDD over voltage error threshold			28		V
$UVE_{THRES(PVDD}$	PVDD under voltage error threshold			4.2		V
OTE_{THRES}	Over temperature error threshold			160		°C
$OTE_{Hystersis}$	Over temperature error hysteresis			10		°C
OTW_{THRES}	Over temperature warning level 1	Read by register 0x73 bit0		112		°C
OTW_{THRES}	Over temperature warning level 2	Read by register 0x73 bit1		122		°C
OTW_{THRES}	Over temperature warning level 3	Read by register 0x73 bit2		134		°C
OTW_{THRES}	Over temperature warning level 4	Read by register 0x73 bit3		146		°C
Speaker Amplifier (Stereo BTL)						
$\|V_{OS}\|$	Amplifier offset voltage	Measured differentially with zero input data, programmable gain configured with 29.5 V_P gain, V_{PVDD} = 16 V	–7.5		7.5	mV
$P_{O(SPK)}$	Output Power (Per Channel)	V_{PVDD} = 14.4 V, SPK_GAIN = 29.5 V_P, R_{SPK} = 6 Ω, f = 1 kHz THD+N = 10%		17.8		W
		V_{PVDD} = 14.4 V, SPK_GAIN = 29.5 V_P, R_{SPK} = 6 Ω, f = 1 kHz THD+N = 1%		14.5		W
		V_{PVDD} = 24 V, SPK_GAIN = 29.5 V_P, R_{SPK} = 8 Ω, f = 1 kHz THD+N = 10% (Instantaneous Output Power)		38		W
		V_{PVDD} = 24 V, SPK_GAIN = 29.5 V_P, R_{SPK} = 8 Ω, f = 1 kHz THD+N = 1% (Continuous Output Power)		30		W
$THD+N_{SPK}$	Total harmonic distortion and noise (P_O = 1 W, f = 1 kHz, R_{SPK} = 6 Ω)	V_{PVDD} = 12 V, SPK_GAIN = 20.9 V_P LC-filter		0.03%		
		V_{PVDD} = 24 V, SPK_GAIN = 29.5 V_P, LC-filter		0.03%		
$I_{CN(SPK)}$	Idle channel noise (A-weighted, AES17)	V_{PVDD} = 12 V, LC-filter, Load = 6 Ω, Hybrid Modulation		32		μVrms
$I_{CN(SPK)}$		V_{PVDD} = 12 V, LC-filter, Load = 6 Ω, BD Modulation		40		
$I_{CN(SPK)}$		V_{PVDD} = 24 V, LC-filter ,Load = 6 Ω, Hybrid Modulation		35		
$I_{CN(SPK)}$		V_{PVDD} = 24 V, LC-filter ,Load = 6 Ω, BD Modulation		45		
DR	Dynamic range	A-Weighted, -60 dBFS method. P_{VDD} = 24 V, SPK_GAIN = 29.5 Vp		111		dB
SNR	Signal-to-noise ratio	A-Weighted, referenced to 1% THD+N Output Level, PVDD = 24 V		111		dB
		A-Weighted, referenced to 1% THD+N Output Level, PVDD = 14.4 V		108		dB
K_{SVR}	Power supply rejection ratio	Injected Noise = 1 kHz, 1 V_{rms}, P_{VDD} = 14.4 V, input audio signal = digital zero		72		dB
$Crosstalk_{SPK}$	Crosstalk (worst case between left-to-right and right-to-left coupling)	f = 1 kHz		-100		dB
Speaker Amplifier (Mono PBTL)						

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7.5 Electrical Characteristics (continued)

Free-air room temperature 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{O(SPK)}$	Output Power	V_{PVDD} = 19 V, SPK_GAIN = 29.5 V_P, R_{SPK} = 3 Ω, f = 1 kHz, THD+N = 1%		50		W
		V_{PVDD} = 19 V, SPK_GAIN = 29.5 V_P, R_{SPK} = 3 Ω, f = 1 kHz, THD+N = 10%		60		W
		V_{PVDD} = 22 V, SPK_GAIN = 29.5 V_P, R_{SPK} = 4 Ω, f = 1 kHz, THD+N = 1%		53		W
		V_{PVDD} = 22 V, SPK_GAIN = 29.5 V_P, R_{SPK} = 4 Ω, f = 1 kHz, THD+N = 10%		65		W
$THD+N_{SPK}$	Total harmonic distortion and noise (P_O = 1 W, f = 1 kHz	V_{PVDD} = 19 V, SPK_GAIN = 20.9 Vp, LC-filter R_{SPK} = 3 Ω)		0.03%		
		V_{PVDD} = 24 V, SPK_GAIN = 29.5 V_P, LC-filter R_{SPK} = 4 Ω)		0.03%		
DR	Dynamic range	A-Weighted, -60 dBFS method, PVDD=19V		109		dB
SNR	Signal-to-noise ratio	A-Weighted, referenced to 1% THD+N Output Level, PVDD = 19 V		109		dB
		A-Weighted, referenced to 1% THD+N Output Level, PVDD = 24 V		111		dB

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7.6 Timing Requirements

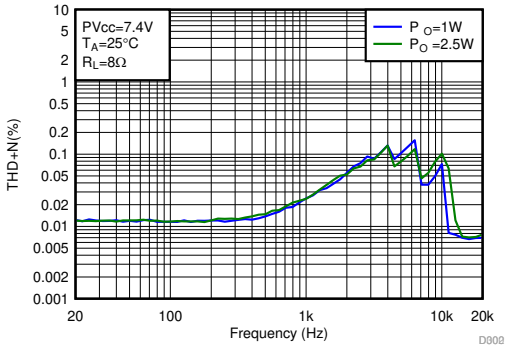
		MIN	NOM	MAX	UNIT
Serial Audio Port Timing – Peripheral Mode					
f_{SCLK}	SCLK frequency	1.024			MHz
t_{SCLK}	SCLK period	40			ns
t_{SCLKL}	SCLK pulse width, low	16			ns
t_{SCLKH}	SCLK pulse width, high	16			ns
t_{SL}	SCLK rising to LRCK/FS edge	8			ns
t_{LS}	LRCK/FS Edge to SCLK rising edge	8			ns
t_{SU}	Data setup time, before SCLK rising edge	8			ns
t_{DH}	Data hold time, after SCLK rising edge	8			ns
t_{DFS}	Data delay time from SCLK falling edge			15	ns
I^2C Bus Timing – Standard					ns
f_{SCL}	SCL clock frequency			100	kHz
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs
t_{LOW}	Low period of the SCL clock	4.7			µs
t_{HI}	High period of the SCL clock	4			µs
t_{RS-SU}	Setup time for (repeated) START condition	4.7			µs
t_{S-HD}	Hold time for (repeated) START condition	4			µs
t_{D-SU}	Data setup time	250			ns
t_{D-HD}	Data hold time	0		900	ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$		1000	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$		1000	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$		1000	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$		1000	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$		1000	ns
t_{P-SU}	Setup time for STOP condition	4			µs
I^2C Bus Timing – Fast					
f_{SCL}	SCL clock frequency			400	kHz
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
t_{LOW}	Low period of the SCL clock	1.3			µs
t_{HI}	High period of the SCL clock	600			ns
t_{RS-SU}	Setup time for (repeated)START condition	600			ns
t_{RS-HD}	Hold time for (repeated)START condition	600			ns
t_{D-SU}	Data setup time	100			ns
t_{D-HD}	Data hold time	0		900	ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$		300	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$		300	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$		300	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$		300	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$		300	ns
t_{P-SU}	Setup time for STOP condition	600			ns
t_{SP}	Pulse width of spike suppressed			50	ns

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7.7 Typical Characteristics

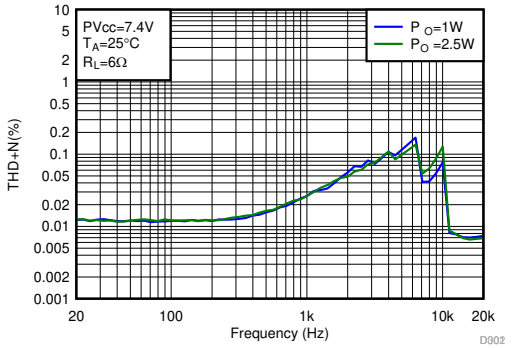
7.7.1 Bridge Tied Load (BTL) Configuration Curves with Hybrid Modulation

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5825PEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 384 kHz, the LC filter used was 10 µH / 0.68 µF, unless otherwise noted.



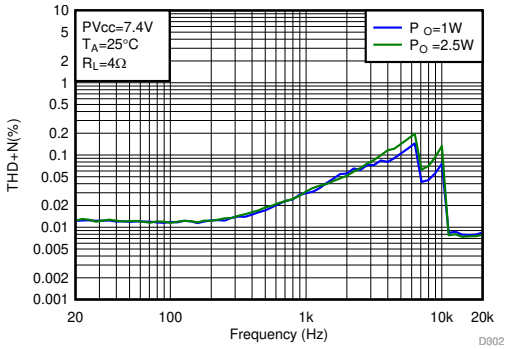
Hybrid Modulation P_O = 1W, 2.5W
F_{SW} = 384 kHz Load = 8 Ω BTL Mode

図 7-1. THD+N vs Frequency-BTL



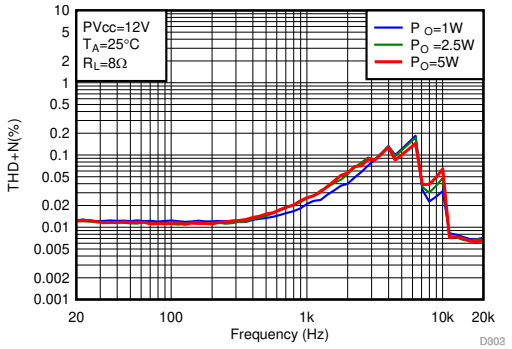
Hybrid Modulation P_O = 1W, 2.5W
F_{SW} = 384 kHz Load = Ω BTL Mode

図 7-2. THD+N vs Frequency-BTL



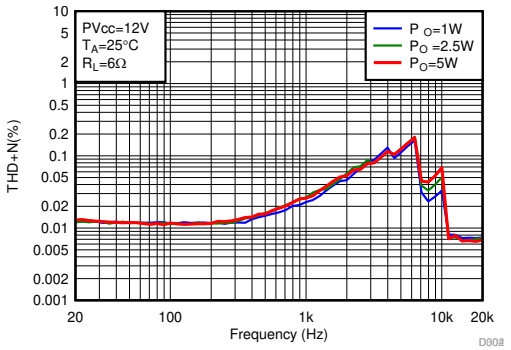
Hybrid Modulation P_O = 1W, 2.5W
F_{SW} = 384 kHz Load = 4 Ω BTL Mode

図 7-3. THD+N vs Frequency-BTL



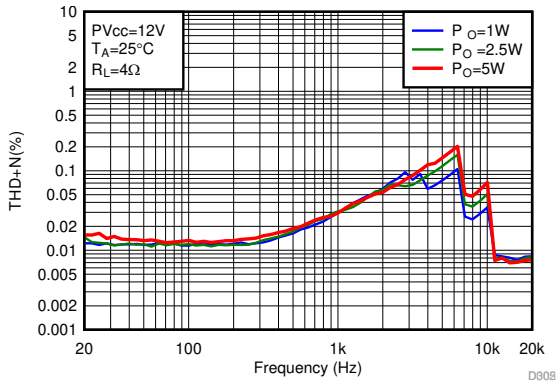
Hybrid Modulation P_O = 1W,2.5W,5W
F_{SW} = 384 kHz Load = 8 Ω BTL Mode

図 7-4. THD+N vs Frequency-BTL



Hybrid Modulation P_O = 1 W,2.5W,5W
F_{SW} = 384 kHz Load = 6 Ω BTL Mode

図 7-5. THD+N vs Frequency-BTL



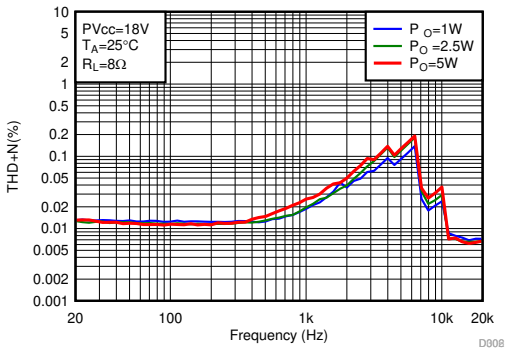
Hybrid Modulation P_O = 1W
F_{SW} = 384 kHz Load = 4 Ω BTL Mode

図 7-6. THD+N vs Frequency-BTL

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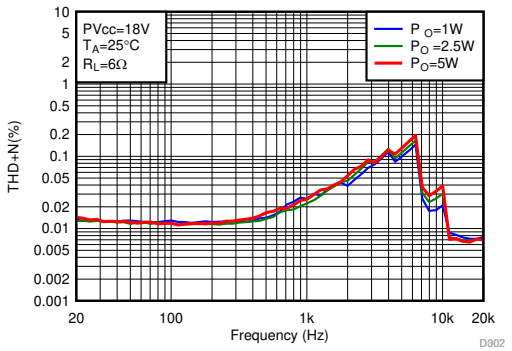
7.7.1 Bridge Tied Load (BTL) Configuration Curves with Hybrid Modulation (continued)

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5825PEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 384 kHz, the LC filter used was 10 µH / 0.68 µF, unless otherwise noted.



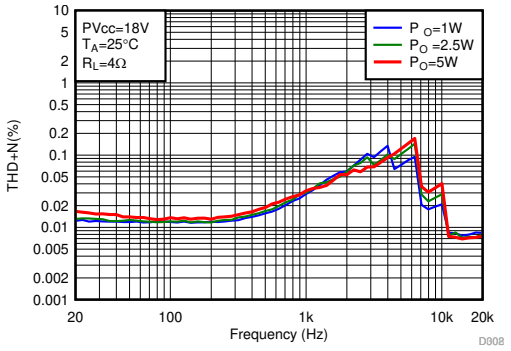
Hybrid Modulation P_O = 1W,2.5W,5W
F_{SW} = 384 kHz Load = 8 Ω BTL Mode

図 7-7. THD+N vs Frequency-BTL



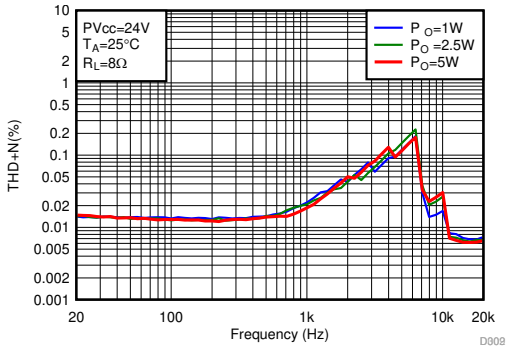
Hybrid Modulation P_O = 1W, 2.5W, 5W
F_{SW} = 384 kHz Load = 6 Ω BTL Mode

図 7-8. THD+N vs Frequency-BTL



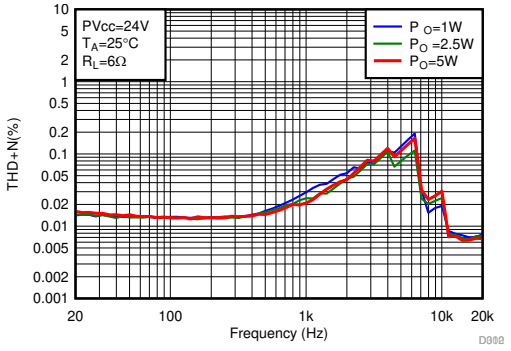
Hybrid Modulation P_O = 1W,2.5W,5W
F_{SW} = 384 kHz Load = 4 Ω BTL Mode

図 7-9. THD+N vs Frequency-BTL



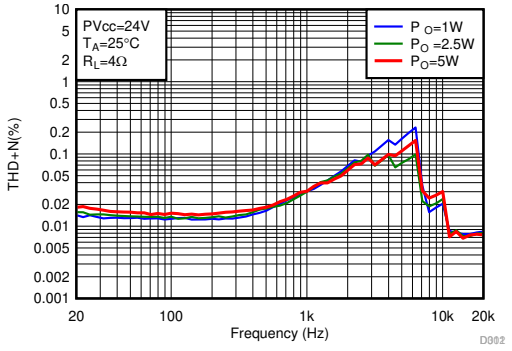
Hybrid Modulation P_O = 1W,2.5W,5W
F_{SW} = 384 kHz Load = 8 Ω BTL Mode

図 7-10. THD+N vs Frequency-BTL



Hybrid Modulation P_O = 1W,2.5W,5W
F_{SW} = 384 kHz Load = 6 Ω BTL Mode

図 7-11. THD+N vs Frequency-BTL



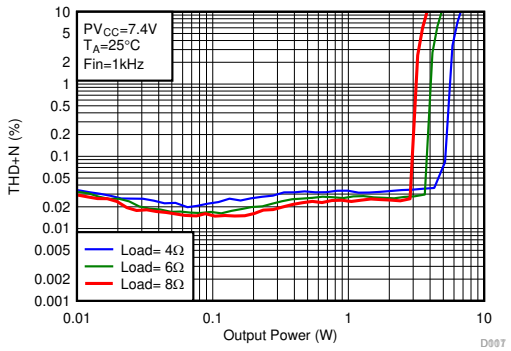
Hybrid Modulation P_O = 1W,2.5W,5W
F_{SW} = 384 kHz Load = 4 Ω BTL Mode

図 7-12. THD+N vs Frequency-BTL

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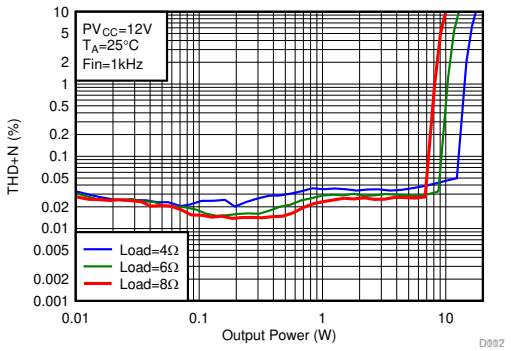
7.7.1 Bridge Tied Load (BTL) Configuration Curves with Hybrid Modulation (continued)

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5825PEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 384 kHz, the LC filter used was 10 µH / 0.68 µF, unless otherwise noted.



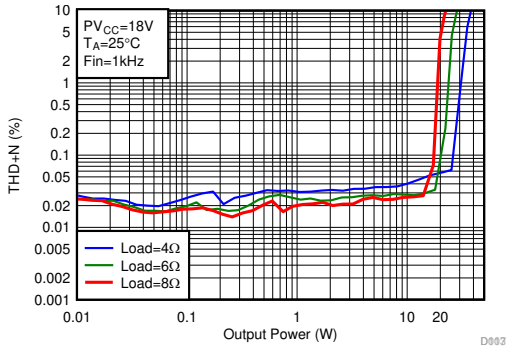
Hybrid Modulation F_{in} = 1 kHz
F_{SW} = 384 kHz Load = 4 Ω /6 Ω /8 Ω BTL Mode

図 7-13. THD+N vs Output Power-BTL



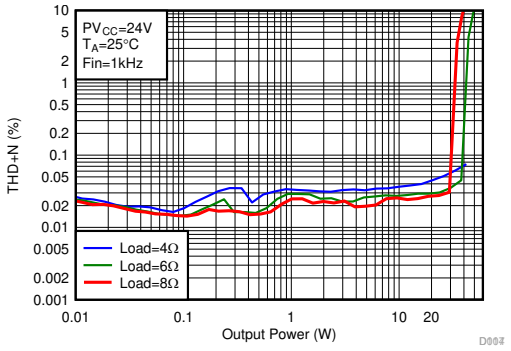
Hybrid Modulation F_{in} = 1 kHz
F_{SW} = 384 kHz Load = 4 Ω /6 Ω /8 Ω BTL Mode

図 7-14. THD+N vs Output Power-BTL



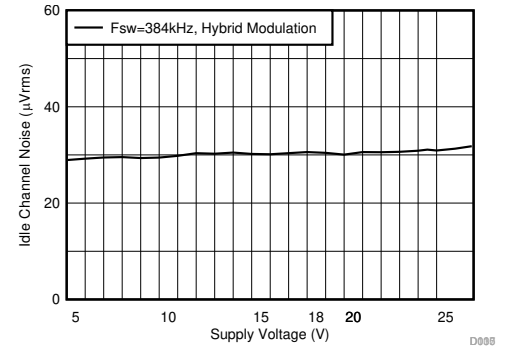
One channel run Hybrid Modulation F_{in} = 1 kHz
F_{SW} = 384 kHz Load = 4 Ω /6 Ω /8 Ω BTL Mode

図 7-15. THD+N vs Output Power-BTL



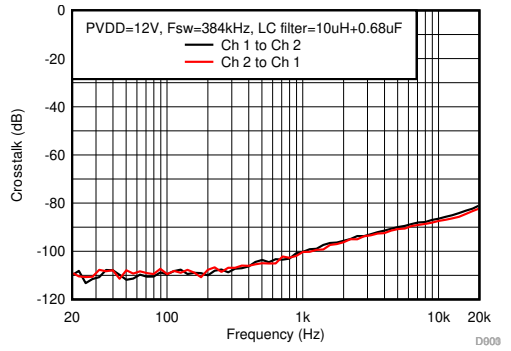
One Channel run Hybrid Modulation F_{in} = 1 kHz
F_{SW} = 384 kHz Load = 4 Ω /6 Ω /8 Ω BTL Mode

図 7-16. THD+N vs Output Power-BTL



Hybrid Modulation
F_{SW} = 384 kHz Load = 6 Ω BTL Mode

図 7-17. Idle Channel Noise vs Supply Voltage

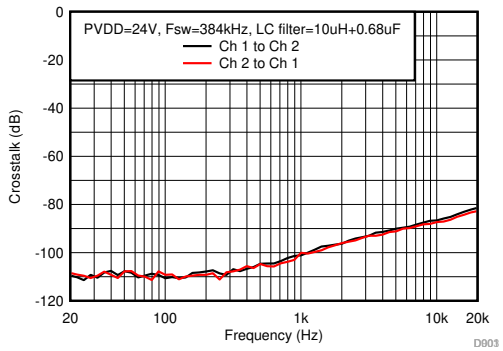


PVDD=12V Hybrid Modulation
F_{SW} = 384 kHz Load = 6 Ω BTL Mode

図 7-18. Crosstalk

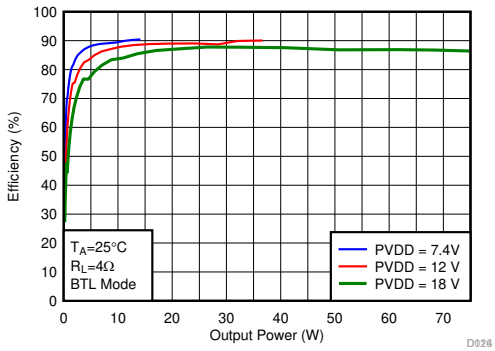
7.7.1 Bridge Tied Load (BTL) Configuration Curves with Hybrid Modulation (continued)

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5825PEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 384 kHz, the LC filter used was 10 µH / 0.68 µF, unless otherwise noted.



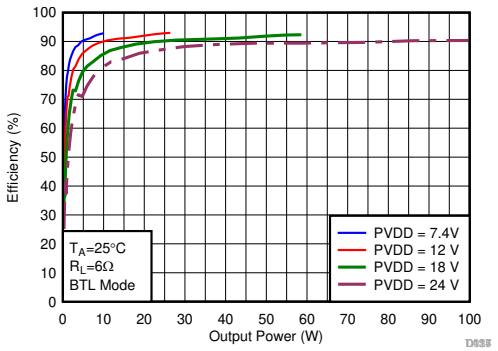
PVDD=24V Hybrid Modulation
F_{SW} = 384 kHz Load = 6 Ω BTL Mode

図 7-19. Crosstalk



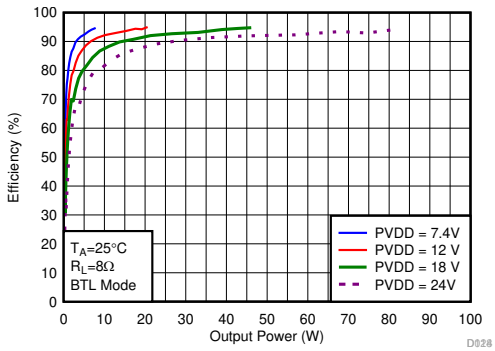
Hybrid Modulation
F_{SW} = 384 kHz Load = 4 Ω BTL Mode

図 7-20. Efficiency vs Output Power



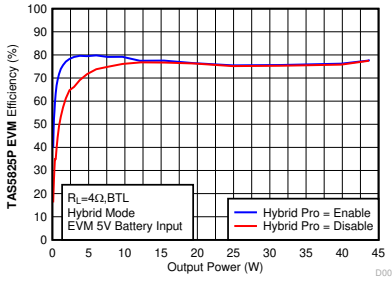
Hybrid Modulation
F_{SW} = 384 kHz Load = 6 Ω BTL Mode

図 7-21. Efficiency vs Output Power



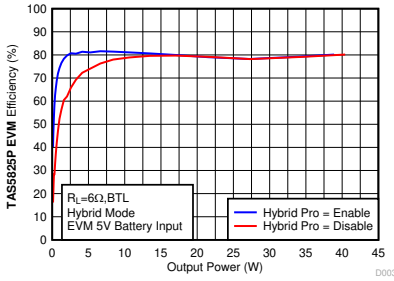
Hybrid Modulation
F_{SW} = 384 kHz Load = 8 Ω BTL Mode

図 7-22. Efficiency vs Output Power



Hybrid Modulation
F_{SW} = 384 kHz 5 V Battery Input Default PPC3 Setting
Load = 4 Ω, BTL approximately 5 V – (-5.5 dB AGAIN)
16 V Boost

図 7-23. EVM Efficiency Comparison ON/OFF Hybrid-Pro



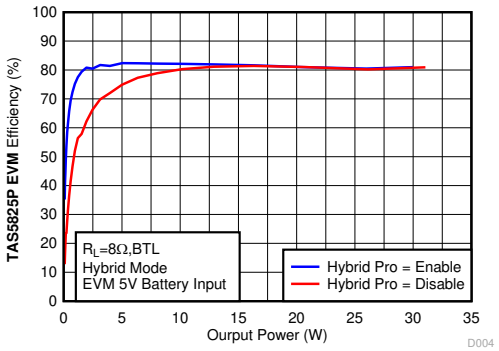
Hybrid Modulation
F_{SW} = 384 kHz 5 V Battery Input Default PPC3 Setting
Load=6Ω, BTL approximately 5 V – (-5.5 dB AGAIN)
16 V Boost

図 7-24. EVM Efficiency Comparison ON/OFF Hybrid-Pro

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7.7.1 Bridge Tied Load (BTL) Configuration Curves with Hybrid Modulation (continued)

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5825PEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 384 kHz, the LC filter used was 10 µH / 0.68 µF, unless otherwise noted.



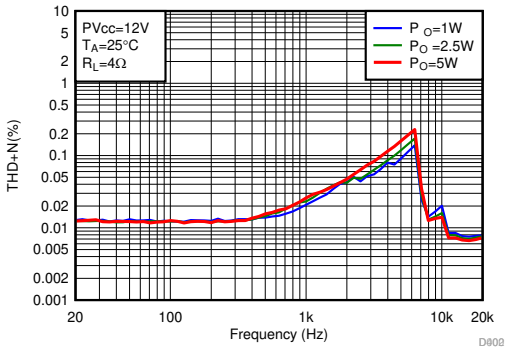
Hybrid Modulation

F_{SW} = 384 kHz Load = 8 Ω, BTL 5 V Battery Input approximately 5 V – 16 V Boost Default PPC3 Setting (-5.5 dB AGAIN)

図 7-25. EVM Efficiency Comparison ON/OFF Hybrid-Pro

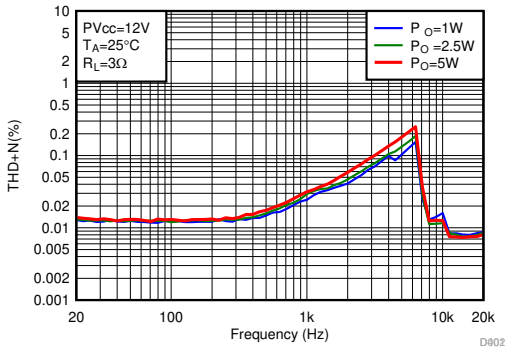
7.7.2 Parallel Bridge Tied Load (PBTL) Configuration With Hybrid Modulation

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5825PEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 384 kHz, the LC filter used was 10 µH / 0.68 µF（Pre-Filter PBTL, the merging of the two output channels in this device can be done before the inductor portion of the output filter, see connect method in セクション 10.2.6）, unless otherwise noted.



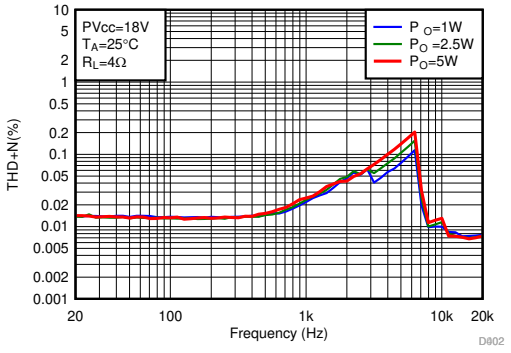
Hybrid Modulation P_O = 1W,2.5W,5W
F_{SW} = 384 kHz Load = 4 Ω PBTL Mode

図 7-26. THD+N vs Frequency-PBTL



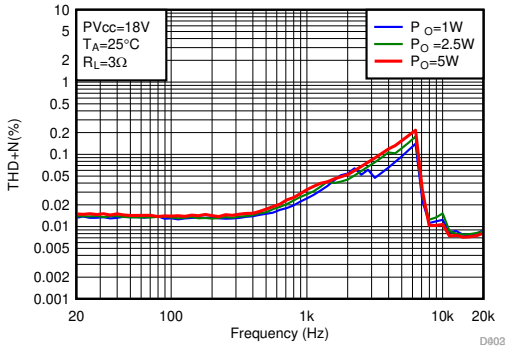
Hybrid Modulation P_O = 1W,2.5W,5W
F_{SW} = 384 kHz Load = 3 Ω PBTL Mode

図 7-27. THD+N vs Frequency-PBTL



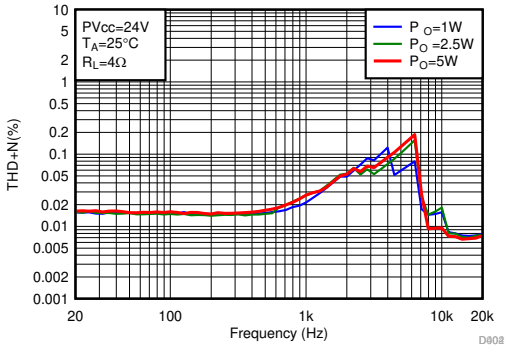
Hybrid Modulation P_O = 1W,2.5W,5W
F_{SW} = 384 kHz Load = 4 Ω PBTL Mode

図 7-28. THD+N vs Frequency-PBTL



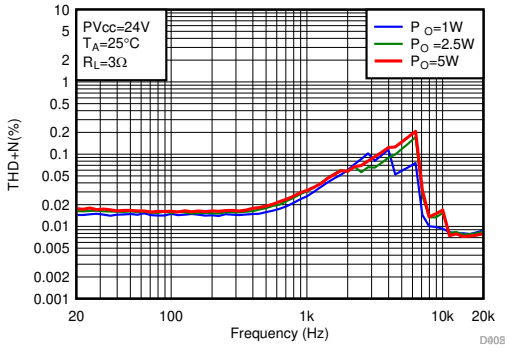
Hybrid Modulation P_O = 1W,2.5W,5W
F_{SW} = 384 kHz Load = 3 Ω PBTL Mode

図 7-29. THD+N vs Frequency-PBTL



Hybrid Modulation P_O = 1W,2.5W,5W
F_{SW} = 384 kHz Load = 4 Ω PBTL Mode

図 7-30. THD+N vs Frequency-PBTL



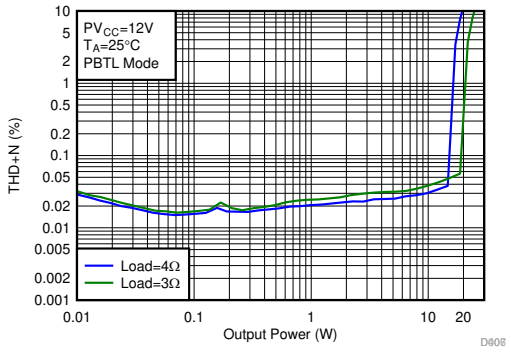
Hybrid Modulation P_O = 1W,2.5W,5W
F_{SW} = 384 kHz Load = 3 Ω PBTL Mode

図 7-31. THD+N vs Frequency-PBTL

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7.7.2 Parallel Bridge Tied Load (PBTL) Configuration With Hybrid Modulation (continued)

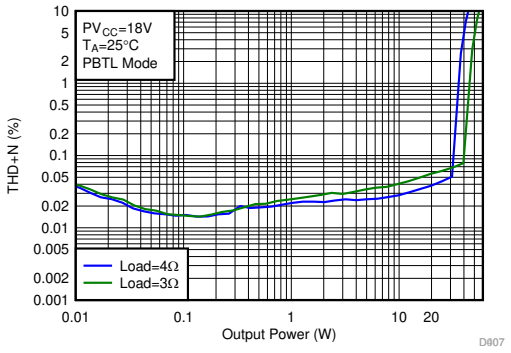
Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5825PEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 384 kHz, the LC filter used was 10 µH / 0.68 µF（Pre-Filter PBTL, the merging of the two output channels in this device can be done before the inductor portion of the output filter, see connect method in セクション 10.2.6）, unless otherwise noted.



Hybrid Modulation

F_{SW} = 384 kHz Load = 4 Ω, 3 Ω PBTL Mode

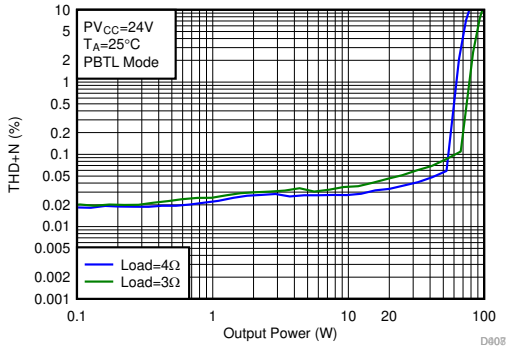
図 7-32. THD+N vs Output Power-PBTL



Hybrid Modulation

F_{SW} = 384 kHz Load = 4 Ω, 3 Ω PBTL Mode

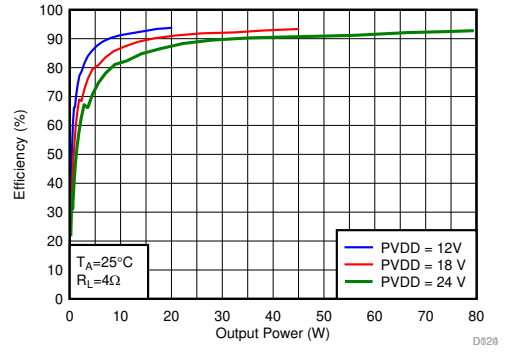
図 7-33. THD+N vs Output Power-PBTL



Hybrid Modulation

F_{SW} = 384 kHz Load = 4 Ω, 3 Ω PBTL Mode

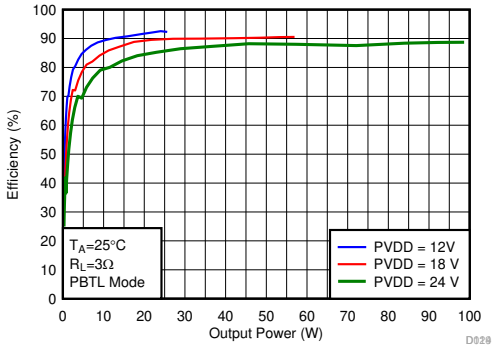
図 7-34. THD+N vs Output Power-PBTL



Hybrid Modulation

F_{SW} = 384 kHz Load = 4 Ω PBTL Mode

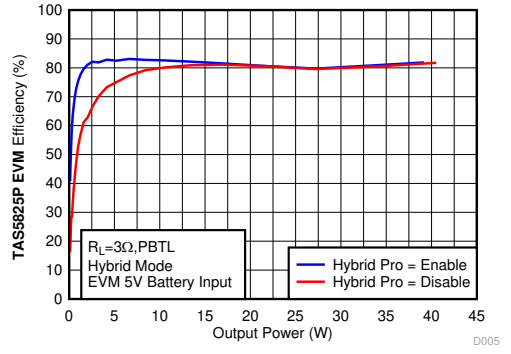
図 7-35. Efficiency vs Output Power



Hybrid Modulation

F_{SW} = 384 kHz Load = 3 Ω PBTL Mode

図 7-36. Efficiency vs Output Power



Hybrid Modulation

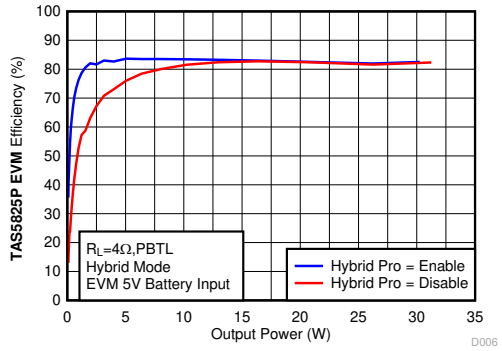
F_{SW} = 384 kHz Load=3Ω, PBTL 5 V Battery Input approximately 5 V – 16 V Boost Default PPC3 Setting (-5.5dB AGAIN)

図 7-37. EVM Efficiency Comparison ON/OFF Hybrid-Pro

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7.7.2 Parallel Bridge Tied Load (PBTL) Configuration With Hybrid Modulation (continued)

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5825PEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 384 kHz, the LC filter used was 10 µH / 0.68 µF（Pre-Filter PBTL, the merging of the two output channels in this device can be done before the inductor portion of the output filter, see connect method in セクション 10.2.6）, unless otherwise noted.

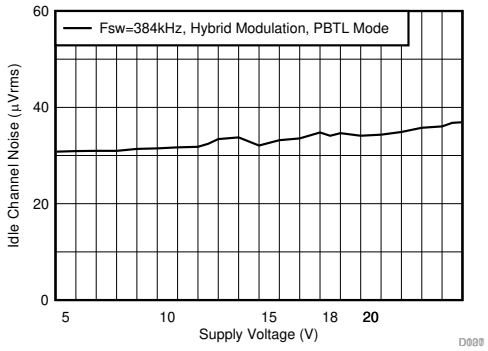


Hybrid Modulation

F_{SW} = 384 kHz　5 V Battery Input　Default PPC3 Setting

Load=4Ω, PBTL　approximately 5 V – 16 V Boost　(-5.5dB AGAIN)

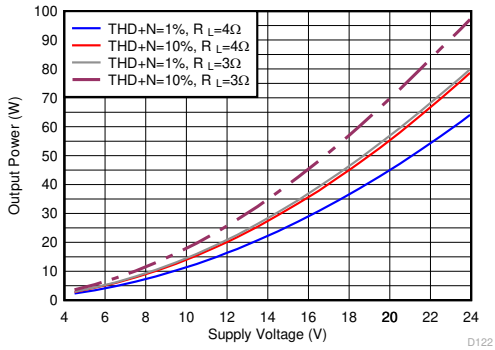
図 7-38. EVM Efficiency Comparison ON/OFF Hybrid-Pro



Hybrid Modulation

F_{SW} = 384 kHz　Load = 6 Ω　PBTL Mode

図 7-39. Idle Channel Noise vs Supply Voltage



Hybrid Modulation

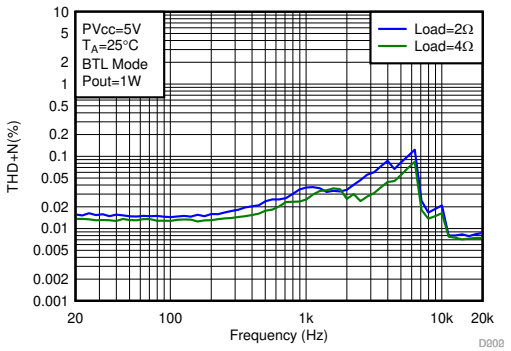
F_{SW} = 384 kHz　Load = 3 Ω, 4 Ω　PBTL Mode

図 7-40. Output Power vs Supply Voltage

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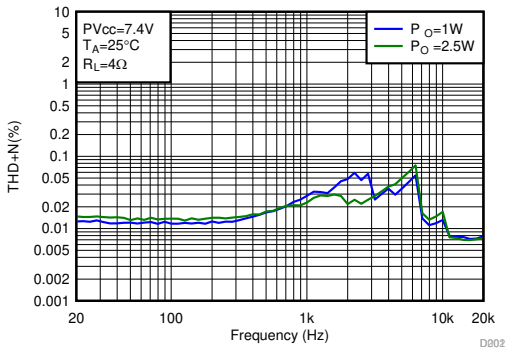
7.7.3 Bridge Tied Load (BTL) Configuration Curves with BD Modulation

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5825PEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 768 kHz, the LC filter used was 4.7µH / 0.68 µF, unless otherwise noted.



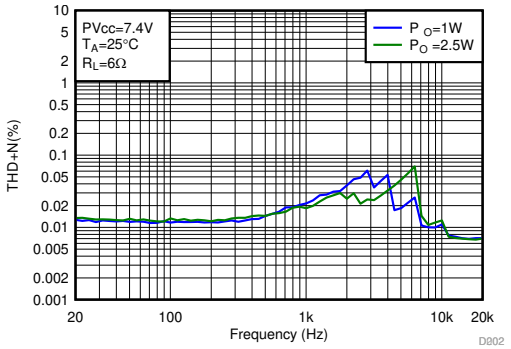
BD Modulation P_O = 1W
F_{SW} = 768 kHz Load = 2 Ω, 4 Ω BTL Mode

図 7-41. THD+N vs Frequency-BTL



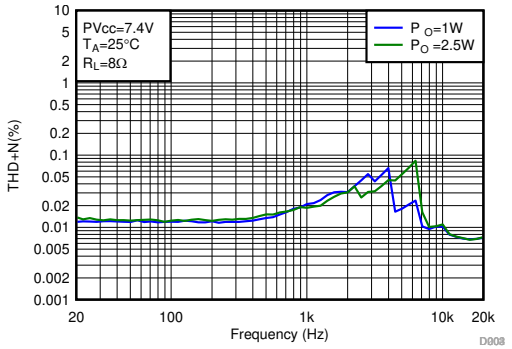
BD Modulation P_O = 1W, 2.5W
F_{SW} = 768 kHz Load = 4 Ω BTL Mode

図 7-42. THD+N vs Frequency-BTL



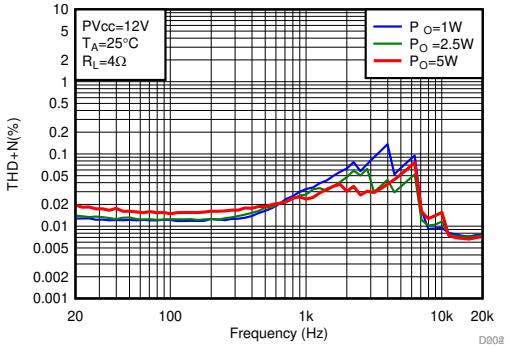
BD Modulation P_O = 1W, 2.5W
F_{SW} = 768 kHz Load = 6 Ω BTL Mode

図 7-43. THD+N vs Frequency-BTL



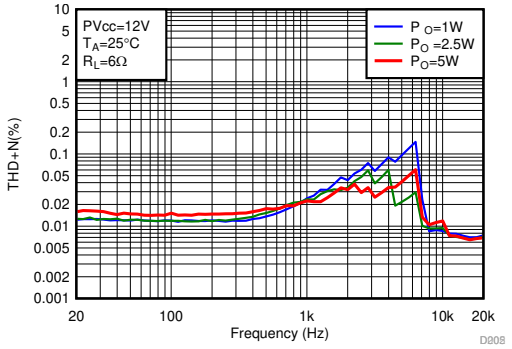
BD Modulation P_O = 1W, 2.5W
F_{SW} = 768 kHz Load = 8 Ω BTL Mode

図 7-44. THD+N vs Frequency-BTL



BD Modulation P_O = 1W,2.5W,5W
F_{SW} = 768 kHz Load = 4 Ω BTL Mode

図 7-45. THD+N vs Frequency-BTL



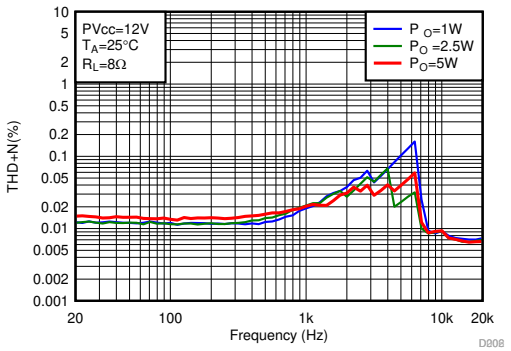
BD Modulation P_O = 1W,2.5W,5W
F_{SW} = 768 kHz Load = 6 Ω BTL Mode

図 7-46. THD+N vs Frequency-BTL

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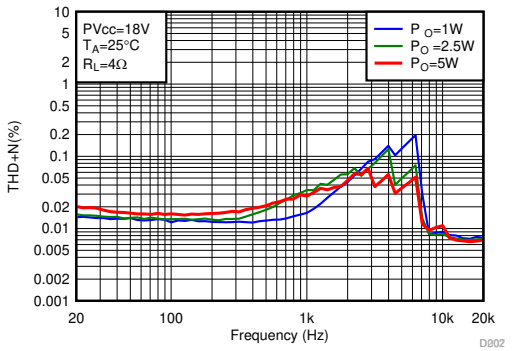
7.7.3 Bridge Tied Load (BTL) Configuration Curves with BD Modulation (continued)

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5825PEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 768 kHz, the LC filter used was 4.7µH / 0.68 µF, unless otherwise noted.



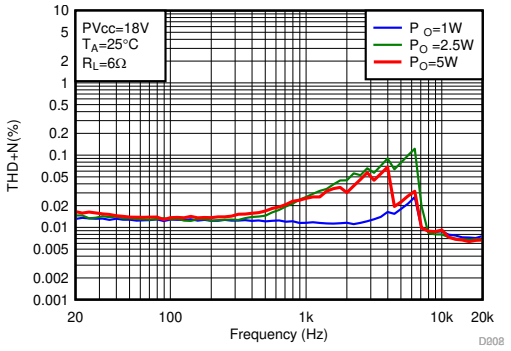
BD Modulation P_O = 1W,2.5W,5W
F_{SW} = 768 kHz Load = 8 Ω BTL Mode

図 7-47. THD+N vs Frequency-BTL



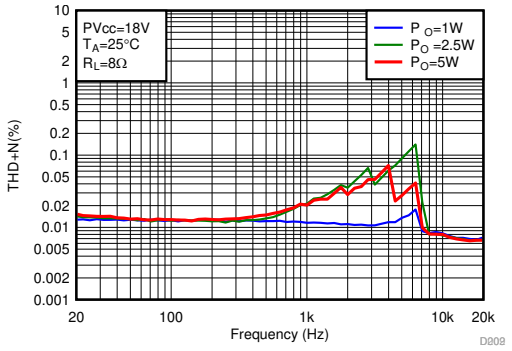
BD Modulation P_O = 1W,2.5W,5W
F_{SW} = 768 kHz Load = 4 Ω BTL Mode

図 7-48. THD+N vs Frequency-BTL



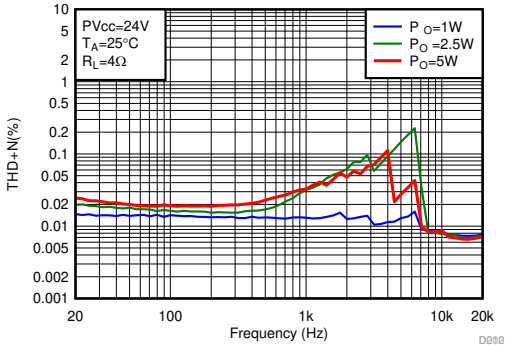
BD Modulation P_O = 1W,2.5W 5W
F_{SW} = 768 kHz Load = 6 Ω BTL Mode

図 7-49. THD+N vs Frequency-BTL



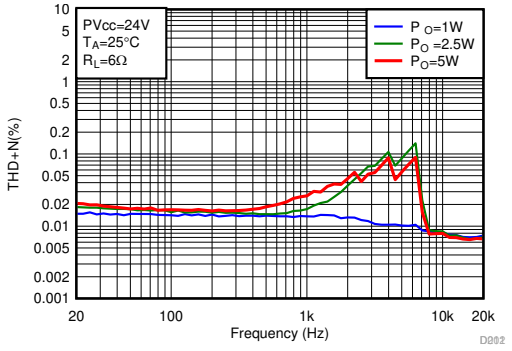
BD Modulation P_O = 1W,2.5W,5W
F_{SW} = 768 kHz Load = 8 Ω BTL Mode

図 7-50. THD+N vs Frequency-BTL



BD Modulation P_O = 1W,2.5W,5W
F_{SW} = 768 kHz Load = 4 Ω BTL Mode

図 7-51. THD+N vs Frequency-BTL



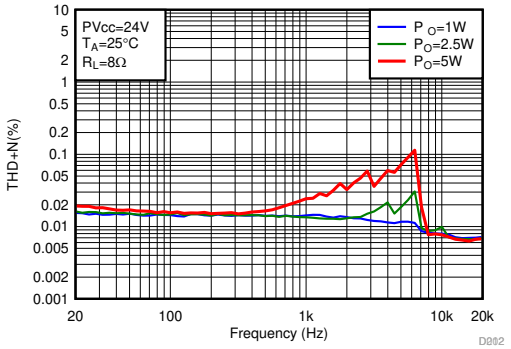
BD Modulation P_O = 1W,2.5W,5W
F_{SW} = 768 kHz Load = 6 Ω BTL Mode

図 7-52. THD+N vs Frequency-BTL

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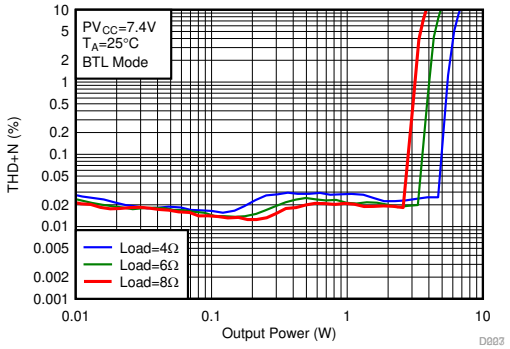
7.7.3 Bridge Tied Load (BTL) Configuration Curves with BD Modulation (continued)

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5825PEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 768 kHz, the LC filter used was 4.7µH / 0.68 µF, unless otherwise noted.



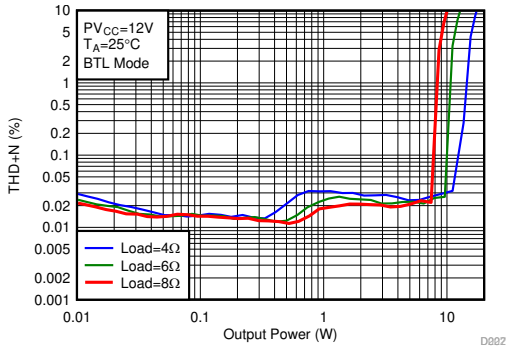
BD Modulation P_O = 1W,2.5W,5W
F_{SW} = 768 kHz Load = 8 Ω BTL Mode

図 7-53. THD+N vs Frequency-BTL



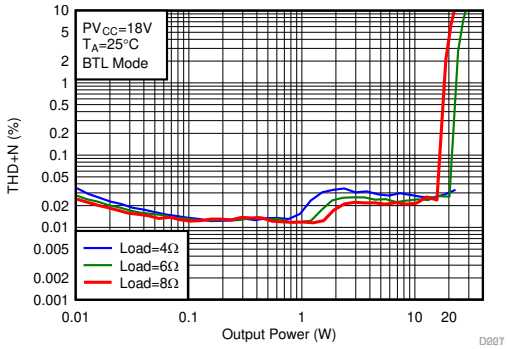
BD Modulation
F_{SW} = 768 kHz Load = 4 Ω, 6 Ω, 8 Ω BTL Mode

図 7-54. THD+N vs Output Power-BTL



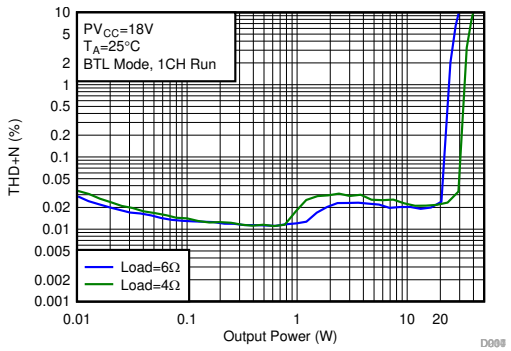
BD Modulation
F_{SW} = 768 kHz Load = 4 Ω, 6 Ω, 8 Ω BTL Mode

図 7-55. THD+N vs Output Power-BTL



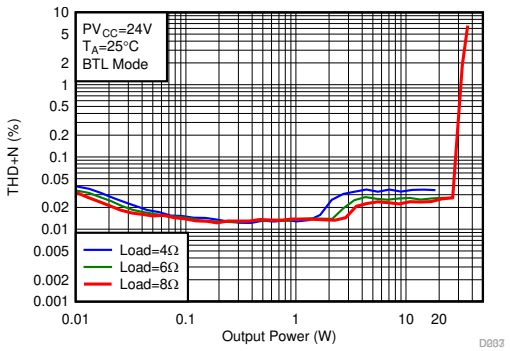
BD Modulation Two Channel Run
F_{SW} = 768 kHz Load = 4 Ω, 6 Ω, 8 Ω BTL Mode

図 7-56. THD+N vs Output Power-BTL



BD Modulation 1 Channel Run
F_{SW} = 768 kHz Load = 4 Ω, 6 Ω BTL Mode

図 7-57. THD+N vs Output Power-BTL



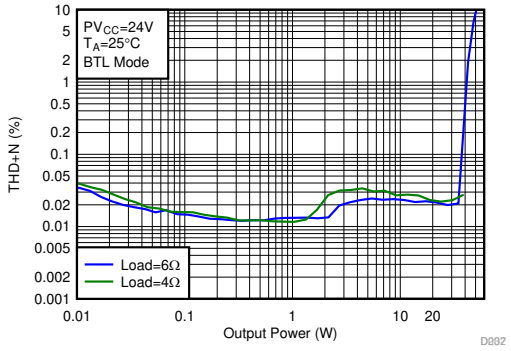
BD Modulation 2 Channel Run
F_{SW} = 768 kHz Load = 4 Ω, 6 Ω, 8 Ω BTL Mode

図 7-58. THD+N vs Output Power-BTL

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7.7.3 Bridge Tied Load (BTL) Configuration Curves with BD Modulation (continued)

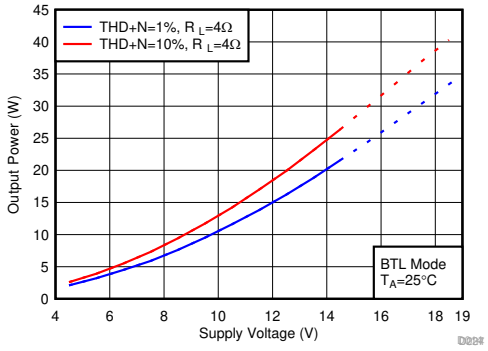
Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5825PEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 768 kHz, the LC filter used was 4.7µH / 0.68 µF, unless otherwise noted.



BD Modulation 1 Channel Run

F_{SW} = 768 kHz Load = 4 Ω, 6 Ω BTL Mode

図 7-59. THD+N vs Output Power-BTL

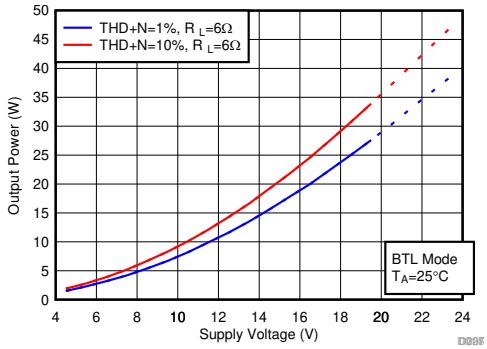


Dashed lines represent thermally limited region.

BD Modulation

F_{SW} = 768 kHz Load = 4 Ω BTL Mode

図 7-60. Output Power vs Supply Voltage

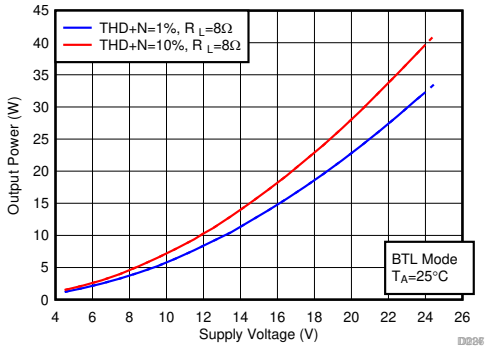


Dashed lines represent thermally limited region.

BD Modulation

F_{SW} = 768 kHz Load = 6 Ω BTL Mode

図 7-61. Output Power vs Supply Voltage

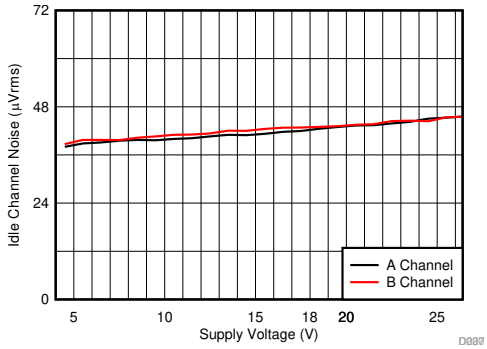


Dashed lines represent thermally limited region.

BD Modulation

F_{SW} = 768 kHz Load = 8 Ω BTL Mode

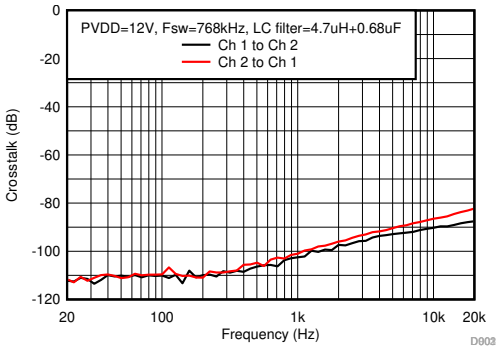
図 7-62. Output Power vs Supply Voltage



BD Modulation

F_{SW} = 768 kHz Load = 6 Ω BTL Mode

図 7-63. Idle Channel Noise vs Supply Voltage



PVDD=12V BD Modulation

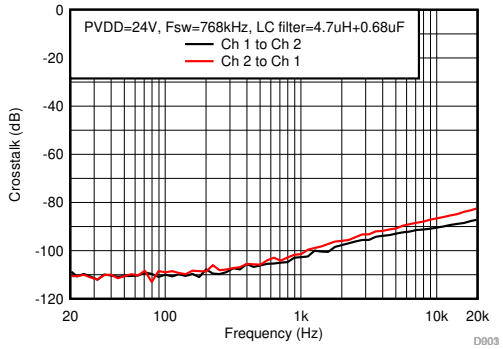
F_{SW} = 768 kHz Load = 6 Ω BTL Mode

図 7-64. Crosstalk

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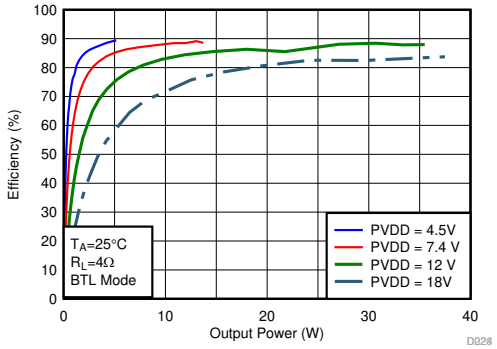
7.7.3 Bridge Tied Load (BTL) Configuration Curves with BD Modulation (continued)

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5825PEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 768 kHz, the LC filter used was 4.7µH / 0.68 µF, unless otherwise noted.



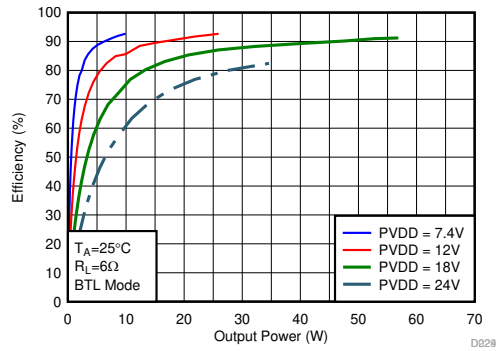
PVDD=12V BD Modulation
F_{SW} = 768 kHz Load = 6 Ω BTL Mode

図 7-65. Crosstalk



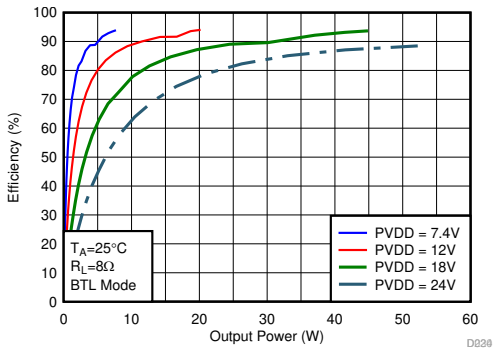
BD Modulation
F_{SW} = 768 kHz Load = 4 Ω BTL Mode

図 7-66. Efficiency vs Output Power



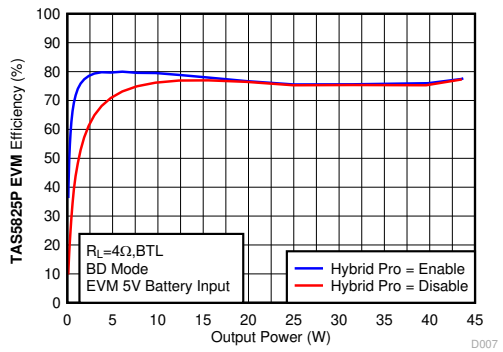
BD Modulation
F_{SW} = 768 kHz Load = 6 Ω BTL Mode

図 7-67. Efficiency vs Output Power



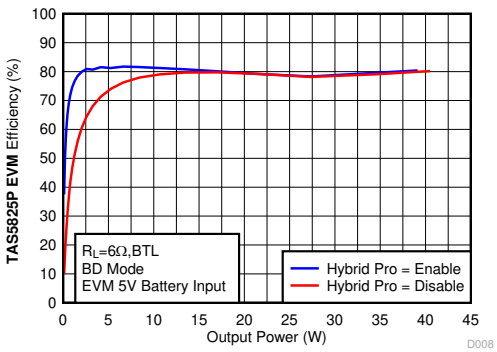
BD Modulation
F_{SW} = 768 kHz Load = 8 Ω BTL Mode

図 7-68. Efficiency vs Output Power



BD Modulation
F_{SW} = 384 kHz 5 V Battery Input Default PPC3 Setting
Load=4Ω, BTL approximately 5 V – 16 V Boost (-5.5 dB AGAIN)

図 7-69. EVM Efficiency Comparison ON/OFF Hybrid-Pro



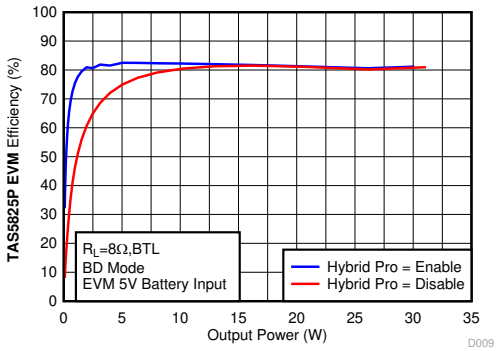
BD Modulation
F_{SW} = 384 kHz 5 V Battery Input Default PPC3 Setting
Load = 6 Ω, BTL approximately 5 V – 16 V Boost (-5.5 dB AGAIN)

図 7-70. EVM Efficiency Comparison ON/OFF Hybrid-Pro

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7.7.3 Bridge Tied Load (BTL) Configuration Curves with BD Modulation (continued)

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5825PEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 768 kHz, the LC filter used was 4.7µH / 0.68 µF, unless otherwise noted.



BD Modulation

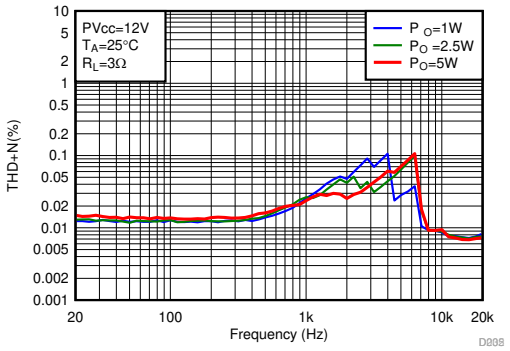
F_{SW} = 384 kHz Load=8Ω, BTL 5 V Battery Input approximately 5 V – 16 V Boost Default PPC3 Setting (-5.5 dB AGAIN)

図 7-71. EVM Efficiency Comparison ON/OFF Hybrid-Pro

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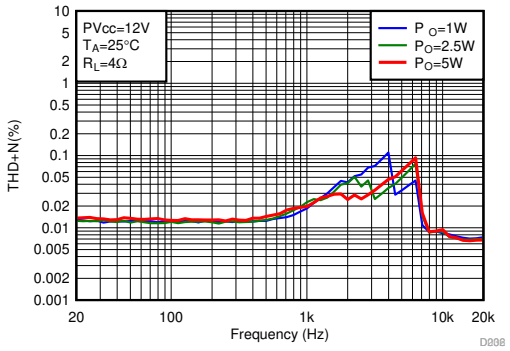
7.7.4 Parallel Bridge Tied Load (PBTL) Configuration With BD Modulation

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5825PEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 768 kHz, the LC filter used was 4.7 µH / 0.68 µF（Pre-Filter PBTL, the merging of the two output channels in this device can be done before the inductor portion of the output filter, see details in セクション 10.2.6）, unless otherwise noted.



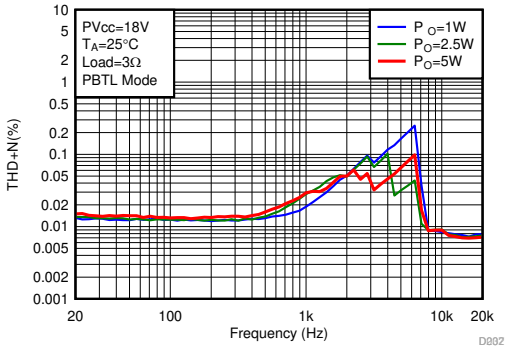
BD Modulation P_O = 1W,2.5W,5W
F_{SW} = 768 kHz Load = 3 Ω PBTL Mode

図 7-72. THD+N vs Frequency-PBTL



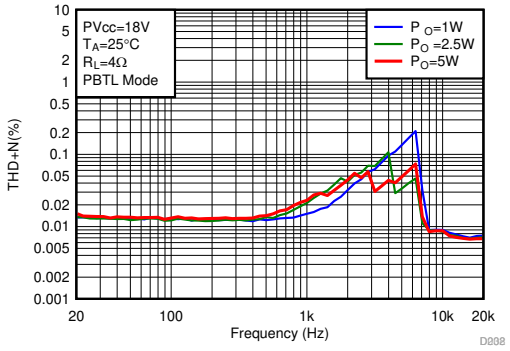
BD Modulation P_O = 1W,2.5W,5W
F_{SW} = 768 kHz Load = 4 Ω PBTL Mode

図 7-73. THD+N vs Frequency-PBTL



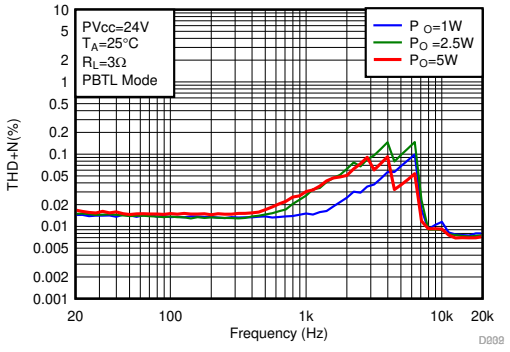
BD Modulation P_O = 1W,2.5W,5W
F_{SW} = 768 kHz Load = 3 Ω PBTL Mode

図 7-74. THD+N vs Frequency-PBTL



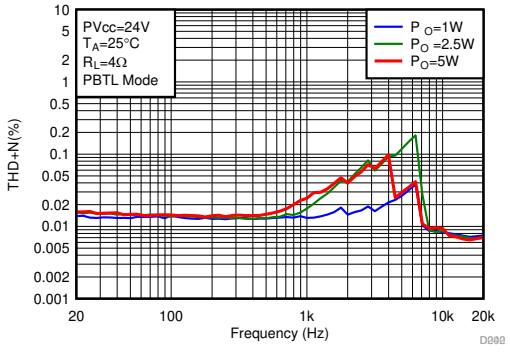
BD Modulation P_O = 1W,2.5W,5W
F_{SW} = 768 kHz Load = 4 Ω PBTL Mode

図 7-75. THD+N vs Frequency-PBTL



BD Modulation P_O = 1W,2.5W,5W
F_{SW} = 768 kHz Load = 3 Ω PBTL Mode

図 7-76. THD+N vs Frequency-PBTL



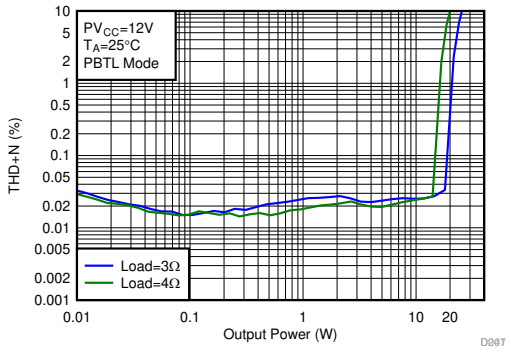
BD Modulation P_O = 1W,2.5W,5W
F_{SW} = 768 kHz Load = 4 Ω PBTL Mode

図 7-77. THD+N vs Frequency-PBTL

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7.7.4 Parallel Bridge Tied Load (PBTL) Configuration With BD Modulation (continued)

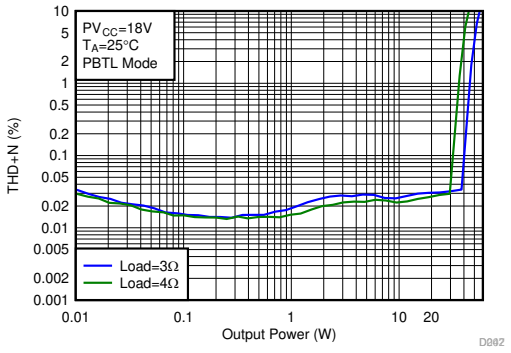
Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5825PEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 768 kHz, the LC filter used was 4.7 µH / 0.68 µF（Pre-Filter PBTL, the merging of the two output channels in this device can be done before the inductor portion of the output filter, see details in セクション 10.2.6）, unless otherwise noted.



BD Modulation

F_{SW} = 768 kHz Load = 3 Ω, 4 Ω PBTL Mode

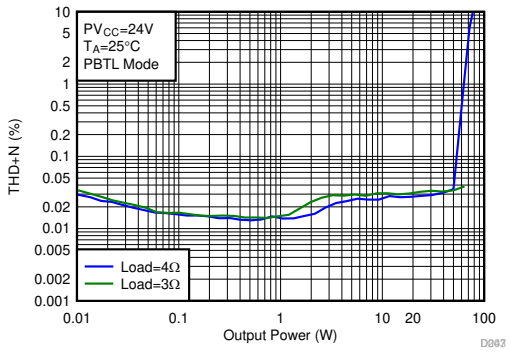
図 7-78. THD+N vs Output Power-PBTL



BD Modulation

F_{SW} = 768 kHz Load = 3 Ω, 4 Ω PBTL Mode

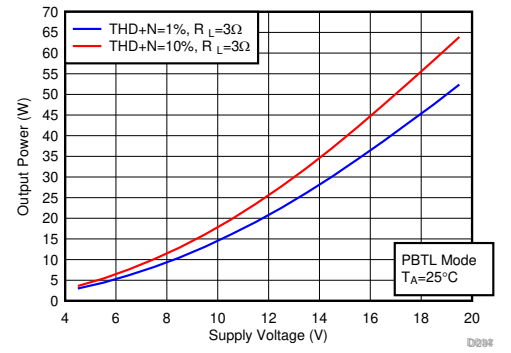
図 7-79. THD+N vs Output Power-PBTL



BD Modulation

F_{SW} = 768 kHz Load = 3 Ω, 4 Ω PBTL Mode

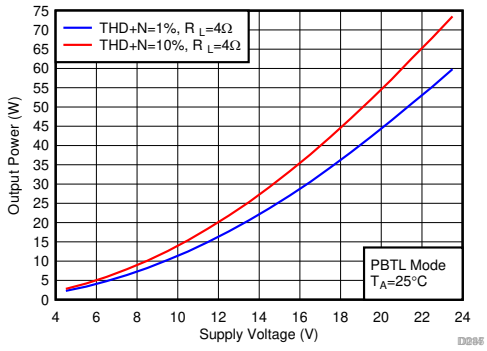
図 7-80. THD+N vs Output Power-PBTL



BD Modulation

F_{SW} = 768 kHz Load = 3 Ω PBTL Mode

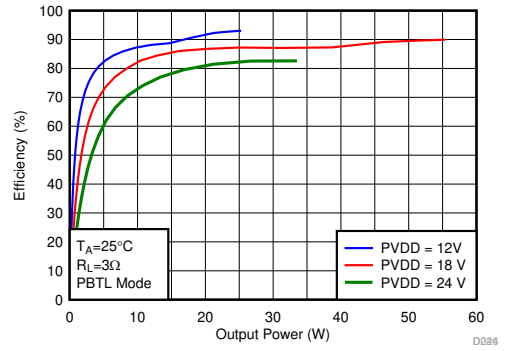
図 7-81. Output Power vs Supply Voltage



BD Modulation

F_{SW} = 768 kHz Load = 4 Ω PBTL Mode

図 7-82. Output Power vs Supply Voltage



BD Modulation

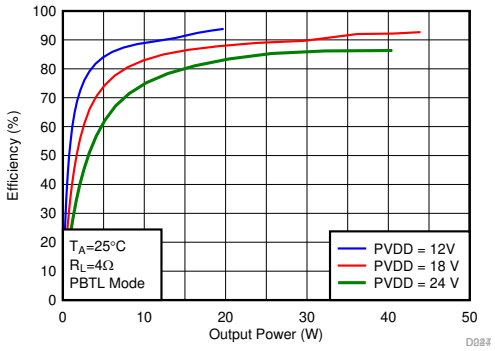
F_{SW} = 768 kHz Load = 3 Ω PBTL Mode

図 7-83. Efficiency vs Output Power

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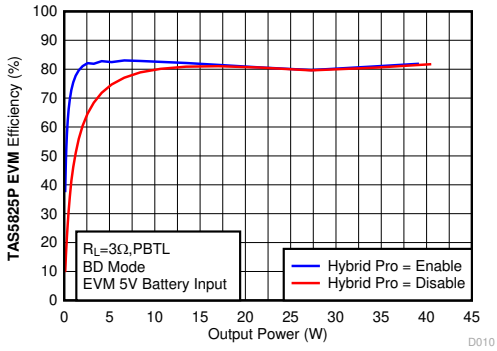
7.7.4 Parallel Bridge Tied Load (PBTL) Configuration With BD Modulation (continued)

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5825PEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 768 kHz, the LC filter used was 4.7 µH / 0.68 µF（Pre-Filter PBTL, the merging of the two output channels in this device can be done before the inductor portion of the output filter, see details in セクション 10.2.6）, unless otherwise noted.



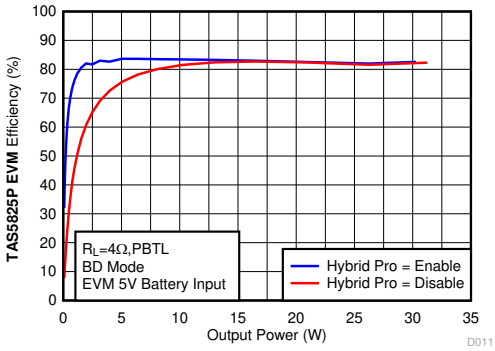
BD Modulation
F_{SW} = 768 kHz Load = 3 Ω, PBTL
5 V EVM Battery with default PPC3 setting (-5.5 dB AGAIN)

図 7-84. Efficiency vs Output Power



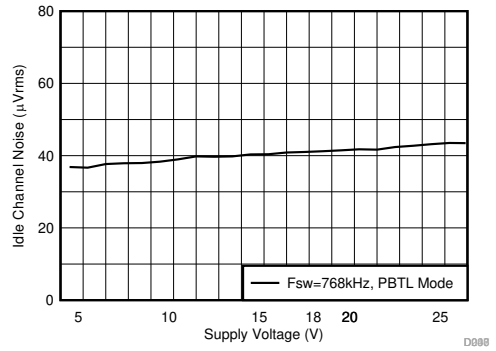
BD Modulation
F_{SW} = 384 kHz 5 V Battery Input Default PPC3 Setting
Load=3Ω, PBTL approximately 5 V – (-5.5 dB AGAIN)
16 V Boost

図 7-85. EVM Efficiency Comparison ON/OFF Hybrid-Pro



BD Modulation
F_{SW} = 384 kHz 5 V Battery Input Default PPC3 Setting
Load=4Ω, PBTL approximately 5 V – (-5.5 dB AGAIN)
16 V Boost

図 7-86. EVM Efficiency Comparison ON/OFF Hybrid-Pro



BD Modulation
F_{SW} = 768 kHz Load =4Ω PBTL Mode

図 7-87. Idle Channel Noise vs Supply Voltage

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8 Parameter Measurement Information

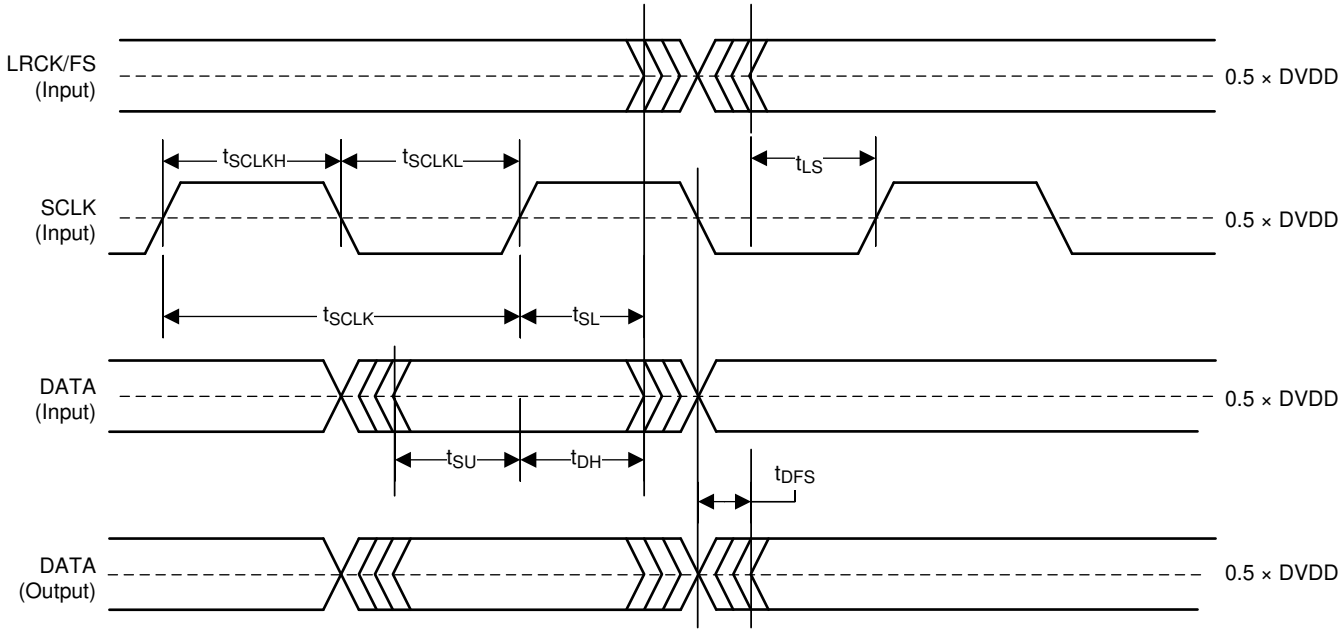


図 8-1. Serial Audio Port Timing in Peripheral Mode

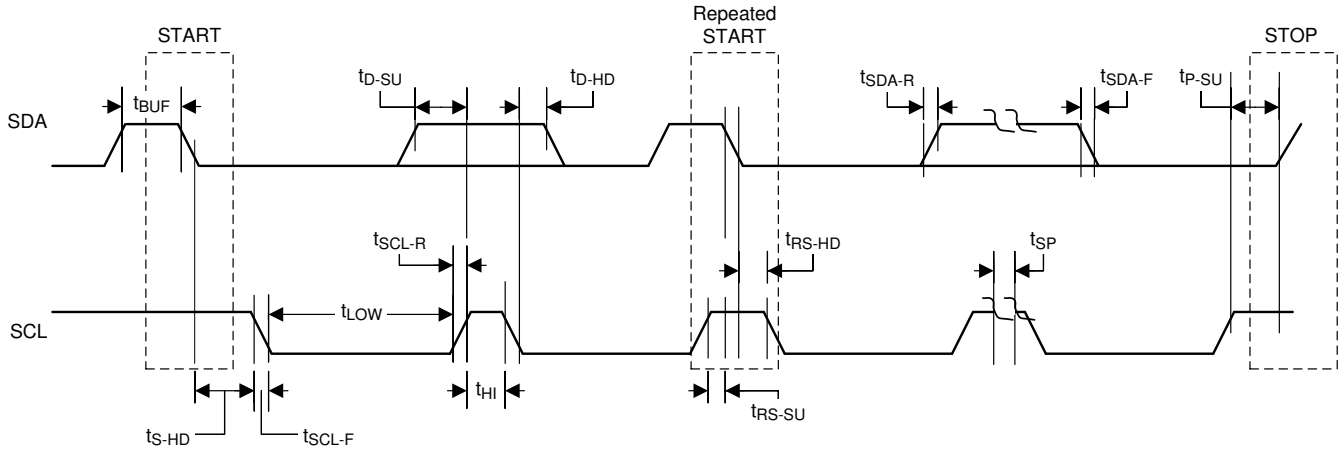


図 8-2. I²C Communication Port Timing Diagram

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9 Detailed Description

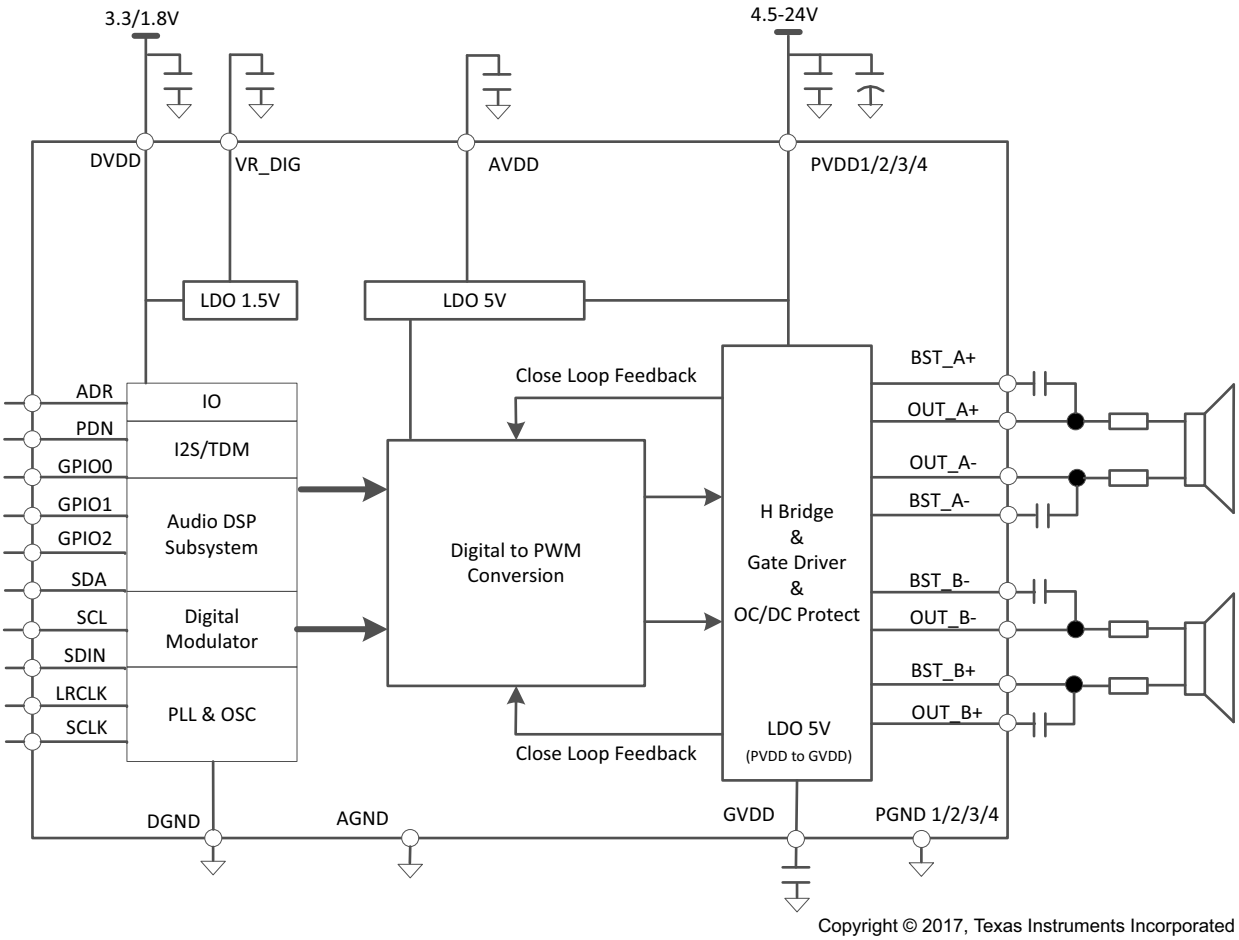
9.1 Overview

TAS5825P is a proprietary and comprehensive device to provide excellent audio performance and high system efficiency when paired with an external DC-DC converter. Audio performance is specified by the coherent whole signal path: digital I/O and processor, stereo digital to PWM modulator and Closed-Loop Class-D amplifier. Hybrid-Pro algorithm improves audio system efficiency by controlling the external supply voltage and maintaining just enough margin to provide high dynamic range without clipping distortion to save as much power as possible. More details can be found in セクション 9.3.7.

- Digital I/O and processor: I^{2}C control, serial audio port, three digital GPIO pins, audio DSP subsystem with Hybrid-Pro algorithm and rich audio processing blocks.
- A stereo digital to PWM modulator.
- A flexible Closed-Loop amplifier capable of operating in stereo or mono, at several different switching frequencies, and with a variety of output voltages and loads.

The device requires only two power supplies for proper operation. A DVDD supply is required to power the low voltage digital circuitry. Another supply, called PVDD, is required to provide power to the output stage of the audio amplifier. Two internal LDOs generate 5 V / 1.5 V for analog / digital supply voltage respectively.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 Power Supplies

For system design, TAS5825P needs one 3.3-V or 1.8-V digital supply and another power-stage supply. Two internal voltage regulators provide good voltage levels for the gate drive circuitry and internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs can result in reduced performance and damage to the device. Additionally, all circuitry requiring a floating voltage supply, that is, the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors. To provide good electrical and acoustical characteristics, the PWM signal path for the output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST_x). The gate drive voltages (GVDD) are derived from the PVDD voltage. Special attention must be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power-supply pins and decoupling capacitors must be avoided. For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_x) to the power-stage output pin (OUT_x). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive regulator output pin (GVDD) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a good voltage supply for the high-side gate driver.

9.3.2 Device Clocking

The TAS5825P devices have flexible systems for clocking. Internally, the device requires a number of clocks, mostly at related clock rates to function correctly. All of these clocks can be derived from the Serial Audio Interface.

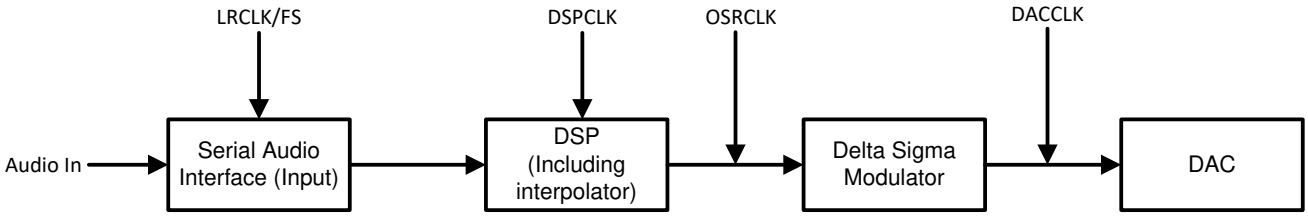


図 9-1. Audio Flow with Respective Clocks

図 9-1 shows the basic data flow and Clock Distribution.

The Serial Audio Interface typically has 3 connection pins which are listed as follows:

- SCLK (Bit Clock)
- LRCLK/FS (Left/Right Word Clock or Frame Sync)
- SDIN (Input Data)

The device has an internal PLL that is used to take SCLK and create the higher rate clocks required by the DSP and the DAC clock.

The TAS5825P device has an audio sampling rate detection circuit that automatically senses which frequency the sampling rate is operating. Common audio sampling frequencies of 32 kHz, 44.1kHz – 48 kHz, 88.2 kHz – 96 kHz are supported. The sampling frequency detector sets the clock for DAC and DSP automatically.

If the input LRCLK/SCLK stopped during music playing, the TAS5825P DSP switches to sleep state and waiting for the clock recovery (Class D output switches to Hiz automatically), once LRCLK/SCLK recovered, TAS5825P auto recovers to the play mode. There is no need to reload the DSP code.

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9.3.3 Serial Audio Port – Clock Rates

The serial audio interface port is a 3-wire serial port with the signals LRCLK/FS , SCLK , and SDIN. SCLK is the serial audio bit clock, used to clock the serial data present on SDIN into the serial shift register of the audio interface. Serial data is clocked into the TAS5825P device with SCLK. The LRCLK/FS pin is the serial audio left/right word clock or frame sync when the device is operated in TDM Mode.

表 9-1. Audio Data Formats, Bit Depths and Clock Rates

FORMAT	DATA BITS	MAXIMUM LRCLK/FS FREQUENCY (kHz)	SCLK RATE (f_S)
I^2S/LJ/RJ	32, 24, 20, 16	32 to 92	64, 32
TDM	32, 24, 20, 16	32	128
		44.1,48	128,256,512
		96	128,256

When Clock halt, non-supported SCLK to LRCLK(FS) ratio is detected, the device reports Clock Error in Register 113 (Register Address 0x71).

9.3.4 Clock Halt Auto-Recovery

As some of host processor halts the I^2S clock when there is no audio playing. When Clock halt, the device puts all channels into the Hi-Z state and reports Clock Error in Register 113 (Register Address 0x71). After audio clocks recovery, the device automatically returns to the previous state.

9.3.5 Sample Rate on the Fly Change

TAS5825P supports LRCLK(FS) rate on the fly change. For example, change LCRLK from 32 kHz to 48 kHz or 96 kHz, Host processor needs to put the LRCLK(FS)/SCLK to Halt state at least 10 ms before changing to the new sample rate.

9.3.6 Serial Audio Port - Data Formats and Bit Depths

The device supports industry-standard audio data formats, including standard I2S, left-justified, right-justified and TDM/DSP data. Data formats are selected via Register (Register Address 0x33h -D[5:4]). If the high width of LRCLK/FS in TDM/DSP mode is less than 8 cycles of SCK, then the register (Register Address 0x33h -D[3:2]) sets to 01. All formats require binary two's complement, MSB-first audio data; up to 32-bit audio data is accepted. All the data formats, word length and clock rate supported by this device are shown in Table 1. The data formats are detailed in 図 9-2 through 図 9-6. The word length are selected via Register (Register Address 0x33h -D[1:0]). The offsets of data are selected via Register (Register Address 0x33h -D[7]) and Register (Register Address 0x34h -D[7:0]). Default setting is I2S and 24 bit word length.

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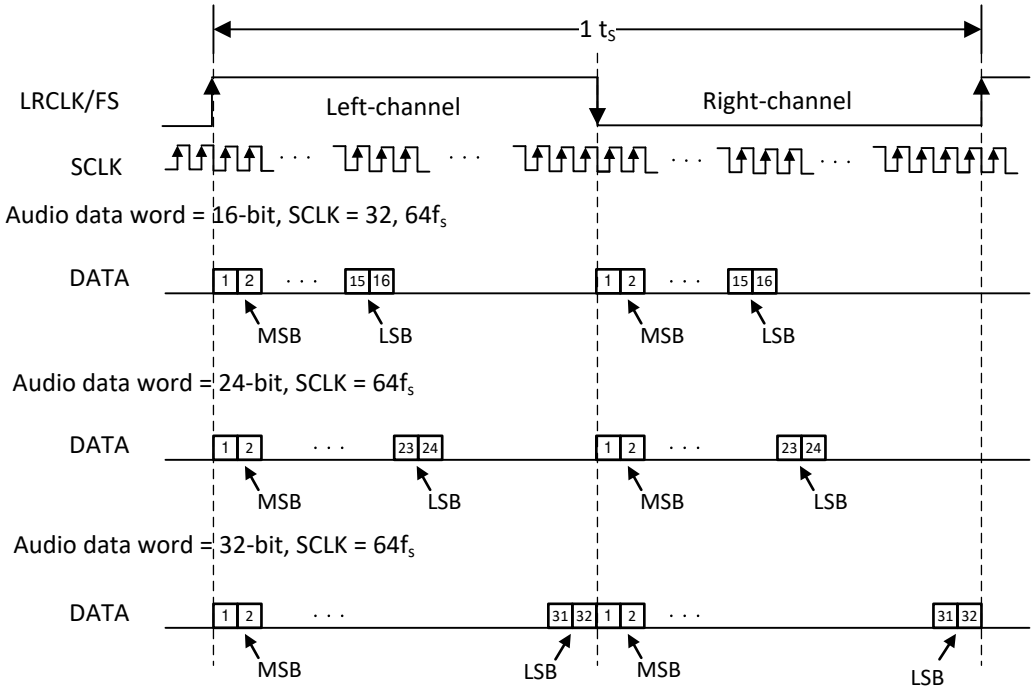
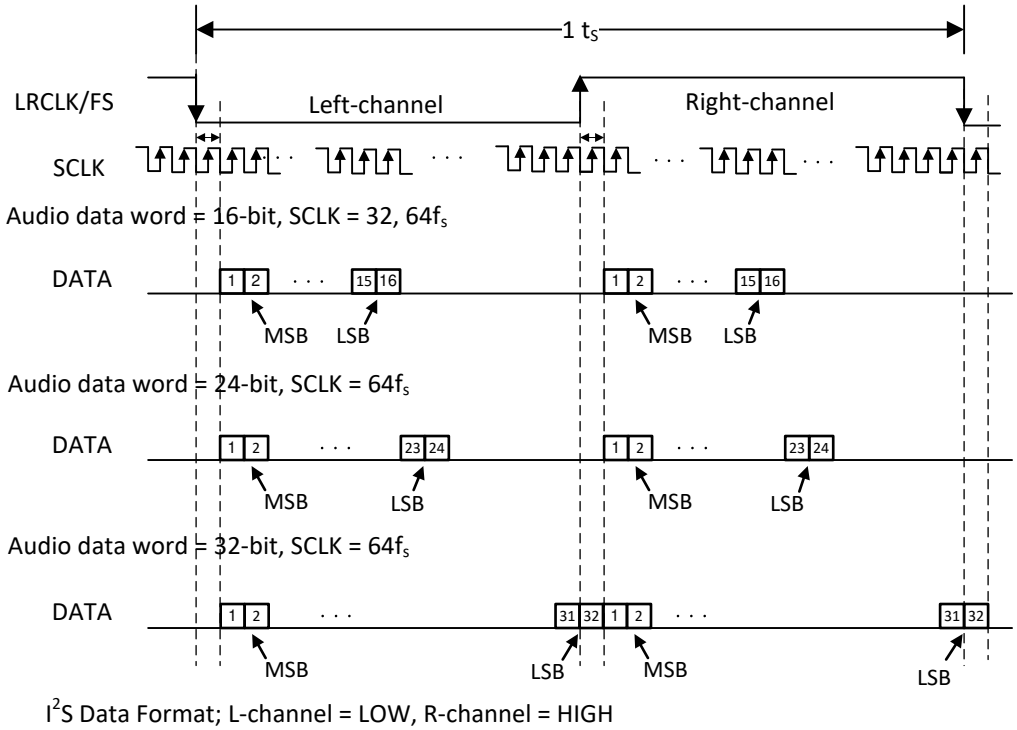


図 9-2. Left Justified Audio Data Format

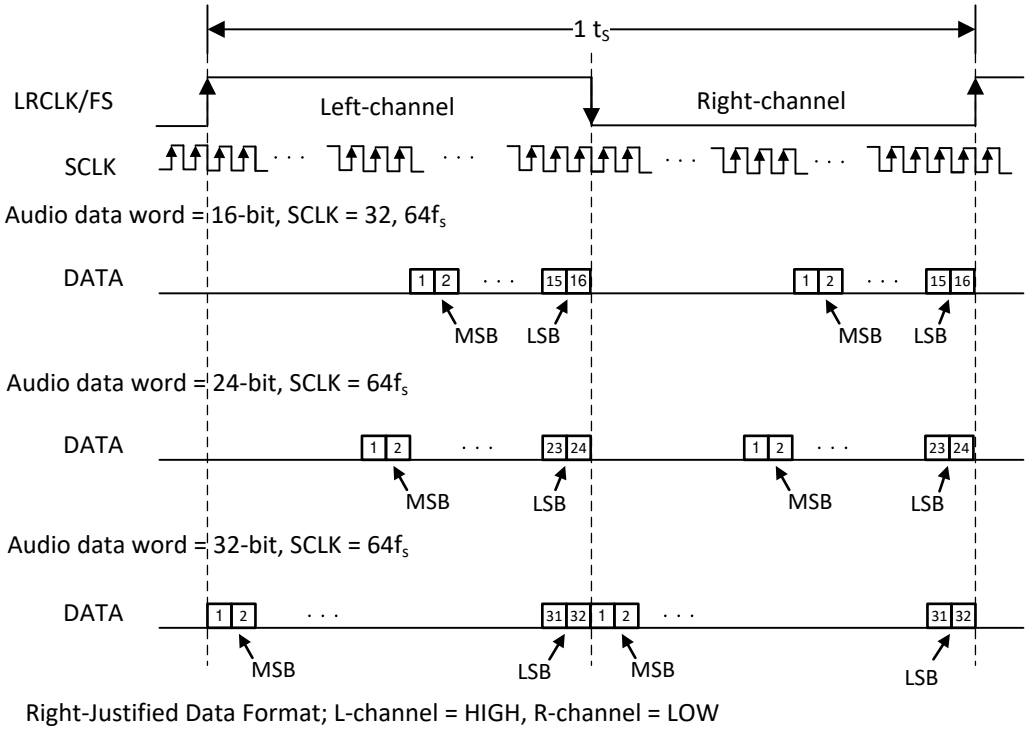


I^2S Data Format; L-channel = LOW, R-channel = HIGH

I^2S Data Format; L-channel = LOW, R-channel = HIGH

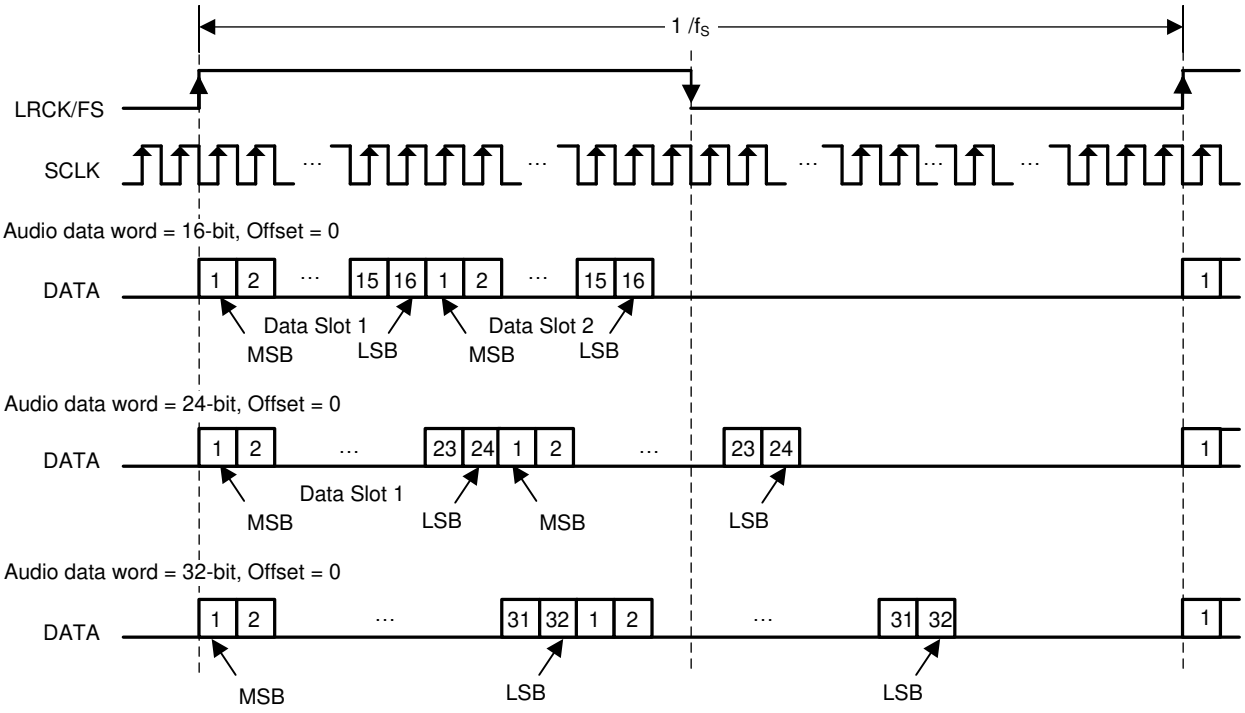
図 9-3. I^2S Audio Data Format

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Right Justified Data Format; L-channel = HIGH, R-channel = LOW

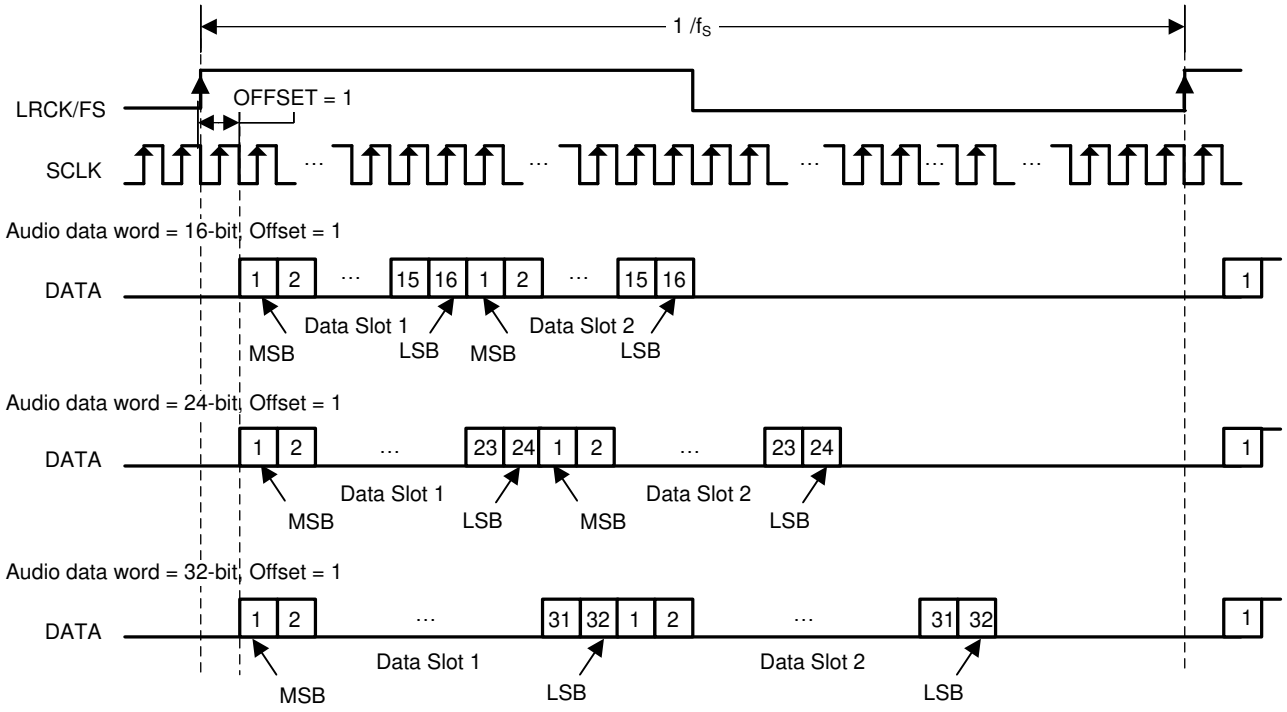
図 9-4. Right Justified Audio Data Format



TDM Data Format with OFFSET = 0

In TDM Modes, Duty Cycle of LRCK/FS must be 1x SCLK at minimum. Rising edge is considered frame start.

図 9-5. TDM 1 Audio Data Format



TDM Data Format with OFFSET = 1

In TDM Modes, Duty Cycle of LRCK/FS must be 1x SCLK at minimum. Rising edge is considered frame start.

図 9-6. TDM 2 Audio Data Format

9.3.7 Digital Audio Processing

TAS5825P digital audio processing includes three main functions: basic audio tuning blocks, Hybrid-Pro algorithm and advanced features.

Basic audio tuning blocks are SRC (sample rate converter), stereo channel Input Mixer, 15 BQs for each channel, pop click free Volume, multi-bands DRC, and AGL. Detailed introduction of each block can be found with TAS5825M Process Flows.

Hybrid-Pro can be used in conjunction with セクション 9.4.6.3, which is a remarkable Class-D internal PWM modulation scheme to improve efficiency even more without compromising THD+N performance. Hybrid-Pro goes beyond Hybrid PWM modulation from system efficiency perspective, by tracking audio signal envelope with advanced look-ahead DSP structure, controlling the external PVDD supply voltage rail, and maintaining just enough margin to provide high dynamic range without clipping distortion to save as much power as possible. Refer TAS5825P User Guide for more configurable options:

- Optional 8 steps 384 kHz PWM format or 16 steps 192 kHz PWM format Hybrid-Pro control waveform for external DC-DC converter.
- Configurable max 4 ms look-ahead audio signal delay buffer, which provides capability to fit various applications systems' DC-DC bandwidth and power supply coupling capacitance.
- Max 512 samples audio signal peak hold to optimize power supply voltage rail transition from large audio input to small level, which is useful to avoid clipping distortion.
- Hybrid-Pro Margin automatically adjusts audio signal trigger level and each step level. Fine tune the level to achieve the balance between efficiency and envelope tracking speed.

Advanced features include PVDD Sensing (Dynamic Headroom Tracking), Thermal Foldback and Hybrid PWM modulation. These features are implemented based on integrated 8-bit PVDD sense ADC and 4 level temperature sensor. Refer to application note: TAS5825M Advanced Features.

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9.3.8 Class-D Audio Amplifier

Following the digital clipper, the interpolated audio data is next sent to the Closed Loop Class-D amplifier, whose first stage is Digital to PWM Conversion (DPC) block. In this block, the stereo audio data is translated into two pairs of complimentary pulse width modulated (PWM) signals which are used to drive the outputs of the speaker amplifier. Feedback loops around the DPC make sure that the constant gain across supply voltages, reduce distortion, and increase immunity to power supply injected noise and distortion. The analog gain is also applied in the Class-D amplifier section of the device. The gain structures are discussed in detail below for both 図 9-7 and 表 9-2. The switching rate of the amplifier is configurable by register (Register Address 0x02h -D[6:4])

9.3.8.1 Speaker Amplifier Gain Select

A combination of digital gain and analog gain is used to provide the overall gain of the speaker amplifier. As seen in 図 9-7, the audio path of the TAS5825P consists of a digital audio input port, a digital audio path, a digital to PWM converter (DPC), a gate driver stage, a Class D power stage, and a feedback loop which feeds the output information back into the DPC block to correct for distortion sensed on the output pins. The total amplifier gain is comprised of digital gain, shown in the digital audio path and the analog gain from the input of the analog modulator to the output of the speaker amplifier power stage.

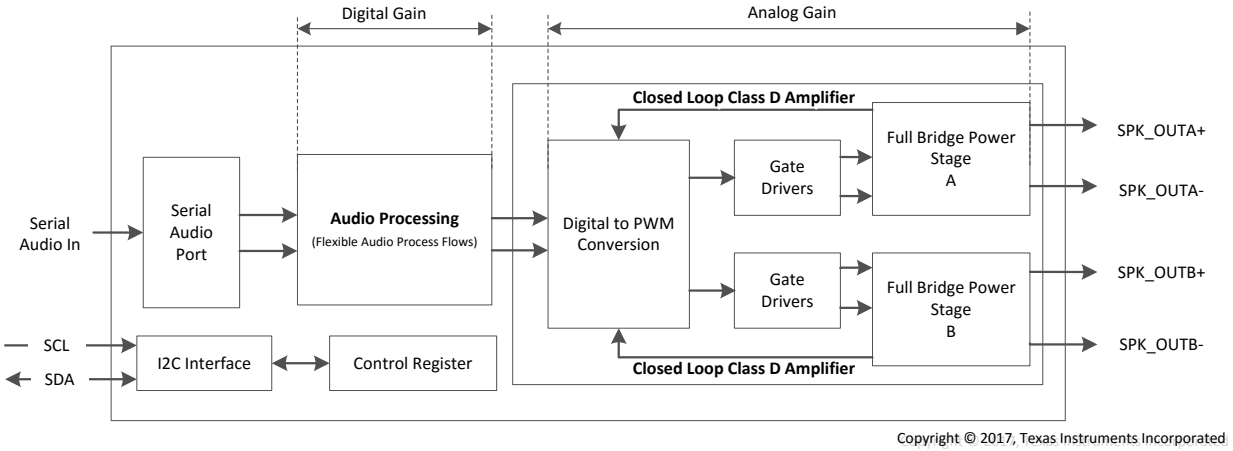


図 9-7. Speaker Amplifier Gain

As shown in 図 9-7, the first gain stage for the speaker amplifier is present in the digital audio path. The first gain stage consists of the volume control and the digital boost block. The volume control is set to 0 dB by default and does not change. For all settings of the register 0x54, AGAIN[4:0], the digital boost block remains at 0 dB. These gain settings make sure that the output signal is not clipping at different PVDD levels. 0dBFS output is 29.5-V peak output voltage

表 9-2. Analog Gain Setting

AGAIN <4:0>	GAIN (dBFS)	AMPLIFIER OUTPUT PEAK VOLTAGE (V)
00000	0	29.5
00001	-0.5	27.85
…….	……..	…….
11111	-15.5	4.95

9.3.8.2 Class D Loop Bandwidth and Switching Frequency Setting

TAS5825P closed loop structure provides Loop bandwidth setting option (Setting by register 83 -Register address 0x53h-D[6-5]) to co-work with different switching frequency (Setting by register 2 -Register address 0x02h-D[6-4]). 表 9-3 shows recommended settings for the Loop Bandwidth and Switching Frequency selection. Same Fsw, Better THD+N performance with higher BW.

表 9-3. Loop Bandwidth and Switching Frequency Setting

Modulation Scheme	Fsw	BW (Loop Band Width)	Notes
Hybrid, 1SPW	384 kHz	80 kHz	Principle: Fsw (Switching Frequency) ≥ 4.2 × Loop Bandwidth
	480 kHz	80 kHz, 100 kHz	
	576 kHz	80 kHz, 100 kHz, 120 kHz	
	768 kHz	80 kHz, 100 kHz, 120 kHz, 175 kHz	
BD	384 kHz	80 kHz, 100 kHz, 120 kHz	Principle: Fsw (Switching Frequency) ≥ 3 × Loop Bandwidth
	480 kHz	80 kHz, 100 kHz, 120 kHz	
	576 kHz	80 kHz, 100 kHz, 120 kHz, 175 kHz	
	768 kHz	80 kHz, 100 kHz, 120 kHz, 175 kHz	

9.4 Device Functional Modes

9.4.1 Software Control

The TAS5825P device is configured via an I^2C communication port.

The I^2C Communication Protocol is detailed in the I^2C Communication Port section. The I^2C timing requirements are described in the I^2C Bus Timing – Standard and I^2C Bus Timing – Fast sections.

There are two methods to program TAS5825P DSP memory.

- Loading with I^2C Communication Port by host processor. This method is recommend for most of applications.
- Fast loading from external EEPROM with SPI communication Port. This method can be used in some applications which need fast loading to save initialization time or release the Host Controller's loading. TAS5825P supports to load the DSP memory data from external EEPROM via SPI. The GPIOs can be configured as SI,SO and SCK for EEPROM via Register (0x60,0x61,0x62,0x63,0x64). The chip selection $\overline{CS}$ of EEPROM is controlled by the Host Processor. See application note: Load TAS5825M Configurations from EEPROM via SPI.

9.4.2 Speaker Amplifier Operating Modes

The TAS5825P device can be used with two different amplifier configurations, can be configured by Register 0x02h -D[2]:

- BTL Mode
- PBTL Mode

9.4.2.1 BTL Mode

In BTL mode, the TAS5825P amplifies two independent signals, which represent the left and right portions of a stereo signal. The amplified left signal is presented on differential output pair shown as OUT_A+ and OUT_A-, the amplified right signal is presented on differential output pair shown as OUT_B+ and OUT_B-.

9.4.2.2 PBTL Mode

The PBTL mode of operation is used to describe operation in which the two outputs of the device are placed in parallel with one another to increase the power sourcing capabilities of the device. On the output side of the TAS5825P device, the summation of the devices can be done before the filter in a configuration called Pre-Filter Parallel Bridge Tied Load (PBTL). However, the two outputs can be required to merge together after the inductor portion of the output filter. Doing so does require two additional inductors, but allows smaller, less expensive inductors to be used because the current is divided between the two inductors. The process is called Post-Filter PBTL. On the input side of the TAS5825P device, the input signal to the PBTL amplifier is left frame of I2S or TDM data.

9.4.3 Low EMI Modes

TAS5825P employs several modes to minimize EMI during playing audio, and can be used based on different applications.

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9.4.3.1 Spread Spectrum

Spread spectrum is used in some inductor free case to minimize EMI noise. The TAS5825P supports Spread Spectrum with triangle mode.

User need configure register SS_CTRL0 (0x6B) to Enable triangle mode and enable spread spectrum, select spread spectrum frequency and range with SS_CTRL1 (0x6C). For 384 kHz F_{SW} which configured by DEVICE_CTRL1 (0x02), the spread spectrum frequency and range are described in 表 9-4.

表 9-4. Triangle Mode Spread Spectrum Frequency and Range Selection

SS_TRI_CTRL[3:0]	0	1	2	3	4	5	6	7
Triangle Freq	24k				48k			
Spread Spectrum Range	5%	10%	20%	25%	5%	10%	20%	25%

User Application example: Central Switching Frequency is 384 kHz, Triangle Frequency is 24 kHz.

Register 0x6b = 0x03 // Enable Spread Spectrum

Register 0x6c = 0x03 // SS_CTRL[3:0]=0011, Triangle Frequency = 24 kHz, Spread Spectrum Range must be 25% (approximately 336 kHz – 432 kHz)

9.4.3.2 Channel to Channel Phase Shift

This device supports channel to channel 180-degree PWM phase shift to minimize the EMI. Bit 0 of Register 0x53 can be used to disable or enable the phase shift. If better pop/click performance is needed, then TI suggests to disable this function with BD mode.

注

セクション 9.4.3.2 and セクション 9.4.3.3 only works in セクション 9.4.6.1, but inoperative in セクション 9.4.6.2 and セクション 9.4.6.3.

9.4.3.3 Multi-Devices PWM Phase Synchronization

TAS5825P support up to 4 phases selection for the multi devices application system. For example, when a system integrated 4 TAS5825P devices, user can select phase0/1/2/3 for each device by register PHASE_CTRL(0x6A), which means there is a 45 degree phase shift between each device to minimize the EMI.

There are two methods for Multi-Device PWM phase synchronization. Phase Synchronization With I²S Clock In Startup Phase or Phase Synchronization With GPIO.

9.4.3.3.1 Phase Synchronization With I²S Clock In Startup Phase

1. Step 1: Halt I²S clock.
2. Step 2: Configure each device phase selection and enable the phase synchronization. For example: Register 0x6A=0x03 for device 0; Register 0x6A=0x07 for device 1; Register 0x6A=0x0B for device 2; Register 0x6A=0x0F for device 3.
3. Step 3: Configure each device into HIZ mode.
4. Step 4: Provide I²S to each device. Phase synchronization for all 4 devices is automatically done by internal sequence.
5. Step 5: Initialize the DSP code (This step can be skipped if only need to do the Phase Synchronization).
6. Step 6: Device to Device PWM phase shift must be fixed with 45 degree.

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9.4.3.3.2 Phase Synchronization With GPIO

1. Step 1: Connect GPIOx pin of each device to SOC's GPIO pin on PCB.
2. Step 2: Configure each device GPIOx as phase sync input usage by registers GPIO_CTRL (0X60) and GPIO_INPUT_SEL (0x64).
3. Step 3: Select different phase for each device and enable phase synchronization by register PHASE_CTRL (0x6A).
4. Step 4: Configure each device into PLAY mode by register DEVICE_CTRL2 (0x03) and monitor the POWER_STATE register (0x68) until device changed to HIZ state.
5. Step 5: Give a 0 to 1 toggle on SOC GPIO. Then all 4 devices enters into PLAY mode and device to Device PWM phase shift must be fixed with 45 degree.
6. Step 6: Phase Synchronization has been finished. Configure the GPIOx pin to other function based on the application.

9.4.4 Thermal Foldback

The Thermal Foldback (TFB), is designed to protect TAS5825P from excessive die temperature increases, in case the device operates beyond the recommended temperature/power limit, or with a weaker thermal system design than recommended. TFB allows the TAS5825P to play as loud as possible without triggering unexpected thermal shutdown. When the die temperature triggers the over-temperature warning (OTW) level (TAS5825P has four different temperature threshold, each threshold is indicated in I^2C register 0x73 bits 0,1,2 and 3), an internal AGL (Automatic Gain Limiter) reduces the digital gain gradually, lower value of OTW, smaller attenuation added, with the OTW warning goes higher, more attenuation added. Once the die temperature drops below the OTW, the device's digital gain gradually returns to the former setting. Both the attenuation gain and adjustable rate are programmable. The TFB gain regulation speed (attack rate and release rate) settings are the same as a regular AGL, which is also configurable with TAS5825P App in PurePathTM Console3.

9.4.5 Device State Control

Except Shutdown Mode, TAS5825P has other 4 states for different power dissipation which listed in *セクション 7.5*.

- Deep Sleep Mode: Register 0x03h -D[1:0]=00, Device stays in Deep Sleep Mode. In this mode, I^2 C block keep works. This mode can be used to extend the battery life time in some portable speaker application case, once the host processor stopped playing audio for a long time, TAS5825P can be set to Deep Sleep Mode to minimize power dissipation until host processor start playing audio again. Device returns back to Play Mode by setting Register 0x03h -D[1:0] to 11. Compare with Shutdown Mode (Pull $\overline{\text{PDN}}$ Low), enter or exit Deep Sleep Mode, DSP keeps active.
- Sleep Mode: Register 0x03h -D[1:0]=01, Device stays in Sleep Mode. In this mode, I^2 C block, Digital core, DSP Memory, 5 V Analog LDO keep works. Compare with Shutdown Mode (Pull $\overline{\text{PDN}}$ Low), enter or exit Sleep Mode, DSP keeps active.
- Output Hiz Mode: Register 0x03h -D[1:0]=10, Device stays in Hiz Mode. In this mode, only output driver set to be Hiz state, all other block work normally.
- Play Mode: Register 0x03h -D[1:0]=11, device stays in Play Mode.

9.4.6 Device Modulation

TAS5825P has 3 modulation schemes: BD modulation, 1SPW modulation and Hybrid modulation. Select modulation schemes for TAS5825P with Register 0x02 [1:0]-DAMP_MOD.

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9.4.6.1 BD Modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

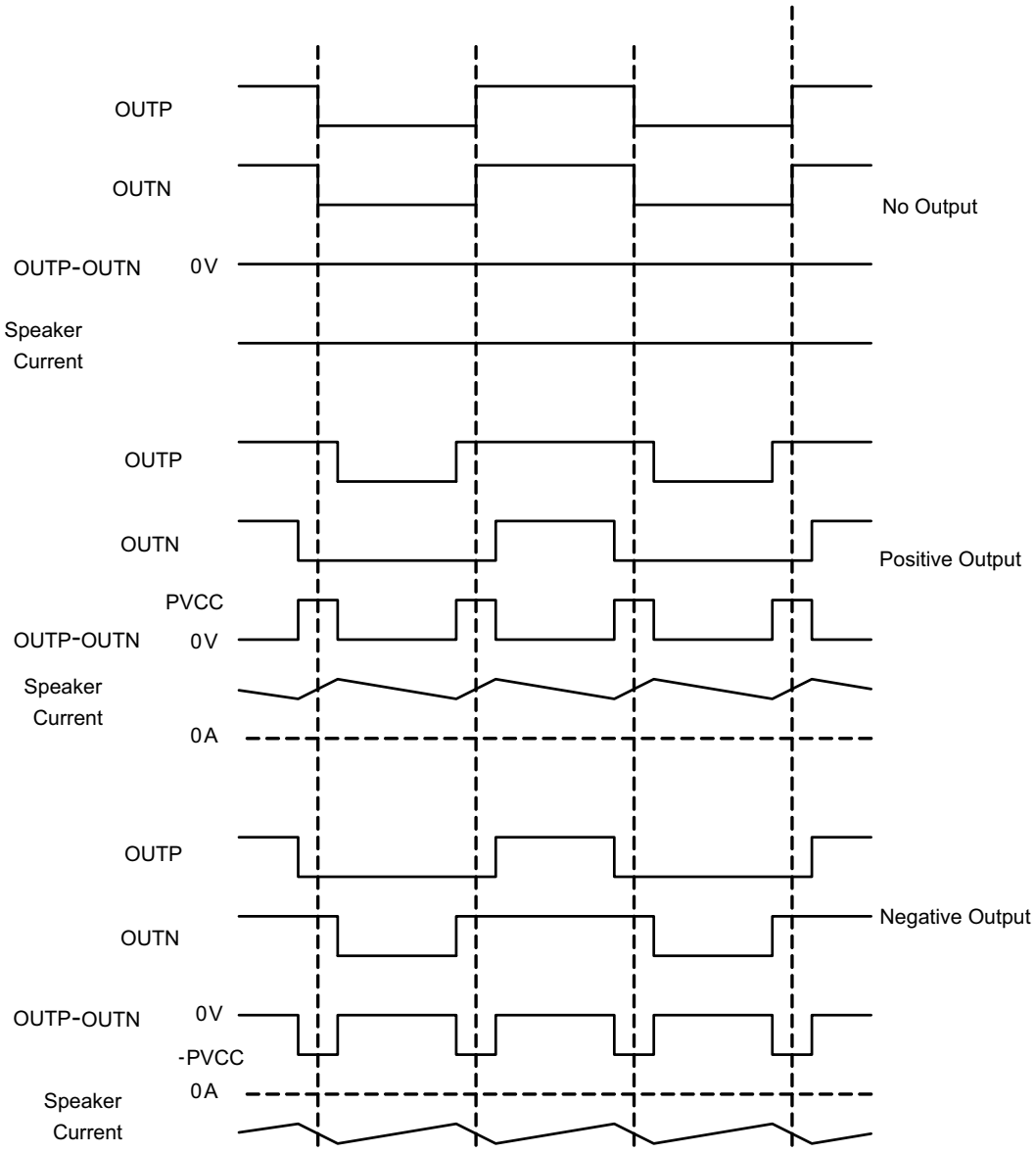


図 9-8. BD Mode Modulation

9.4.6.2 1SPW Modulation

The 1SPW mode alters the normal modulation scheme to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In Low Idle Current mode the outputs operate at approximately 17% modulation during idle conditions. When an audio signal is applied, one output decreases and one increases. The decreasing output signal rails to GND. At this point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses.

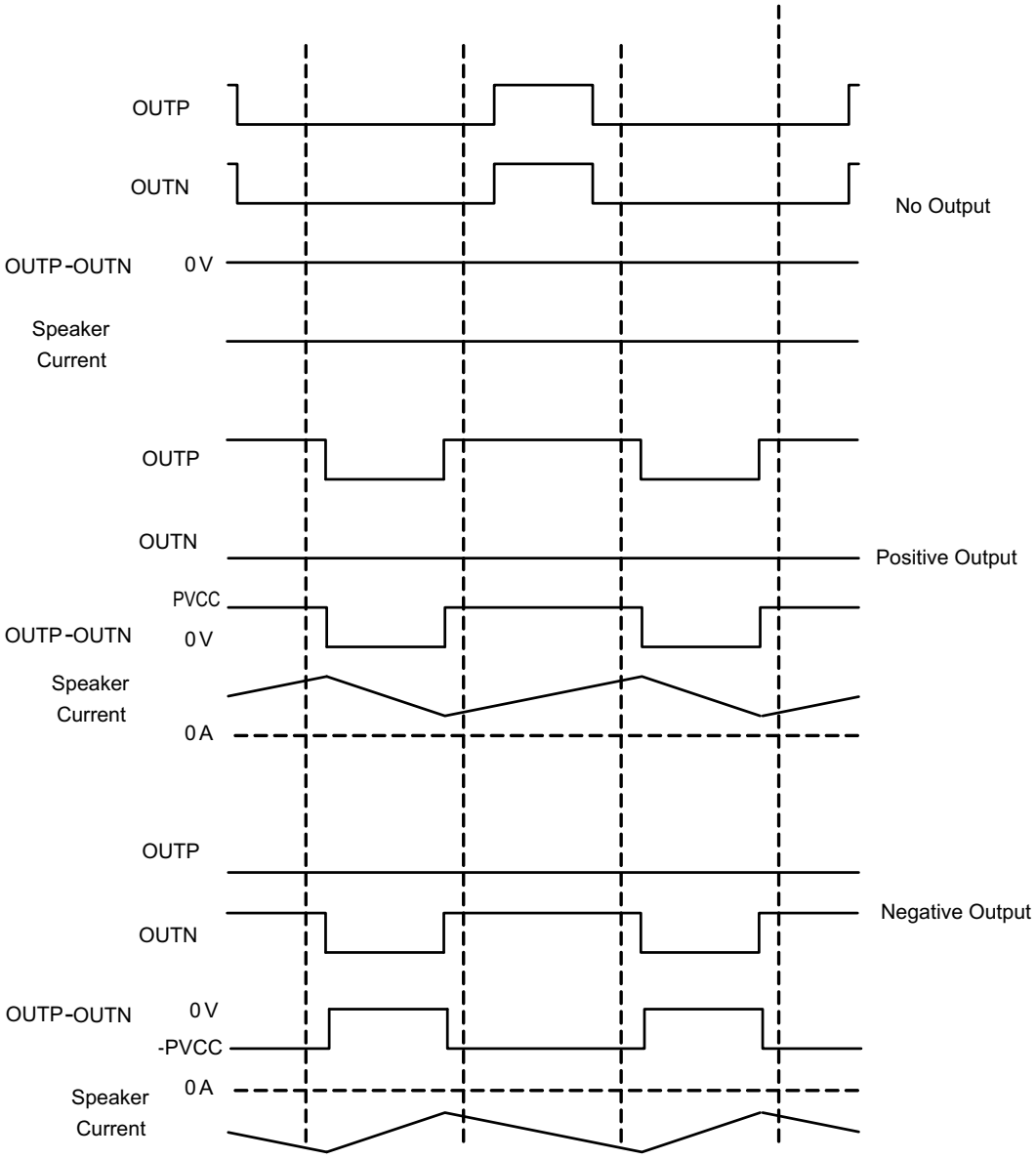


図 9-9. 1SPW Mode Modulation

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9.4.6.3 Hybrid Modulation

Hybrid Modulation is designed for minimized power loss without compromising the THD+N performance, and is optimized for battery-powered applications. With Hybrid modulation, TAS5825P detects the input signal level and adjust PWM duty cycle dynamically based on PVDD. Hybrid modulation achieves ultra low idle current and maintains the same audio performance level as the BD Modulation.

注

As Hybrid Modulation need the internal DSP to detect the input signal level and adjust PWM duty cycle dynamically. To use the Hybrid Modulation, users need to select the corresponding process flows which support Hybrid Modulation in TAS5825P PPC3 App. Look into TAS5825P PPC3 App for more information about TAS5825P flexible audio process flows.

9.5 Programming and Control

9.5.1 I^{2}C Serial Communication Bus

The device has a bidirectional serial control interface that is compatible with I^{2}C bus protocol and supports 100 and 400-kHz data transfer rates for random and sequential write and read operations as a peripheral device. Because the TAS5825P register map and DSP memory spans multi pages, the user must change from page to page before writing individual register or DSP memory. Changing from page to page is accomplished via register 0 on each page. This register value selects the page address, from 0 to 255. All registers listed in TAS5825P data sheet belongs to Page 0.

9.5.2 I^{2}C Peripheral Address

The TAS5825P device has 7 bits for the peripheral address. The first five bits (MSBs) of the peripheral address are factory preset to 10011(0x9x). The next two bits of address byte are the device select bits which can be user-defined by ADR pin in 表 9-5.

表 9-5. I^{2}C Peripheral Address Configuration

ADR PIN Configuration	MSBs					User Define		LSB
0 Ω to GND	1	0	0	1	1	0	0	R/ $\overline{W}$
1 kΩ to GND	1	0	0	1	1	0	1	R/ $\overline{W}$
4.7 kΩ to GND	1	0	0	1	1	1	0	R/ $\overline{W}$
15 kΩ to GND	1	0	0	1	1	1	1	R/ $\overline{W}$

9.5.2.1 Random Write

As shown in 図 9-10, a single-byte data-write transfer begins with the controller device transmitting a start condition followed by the I^{2}C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit is a 0. After receiving the correct I^{2}C device address and the read/write bit, the device responds with an acknowledge bit. Next, the controller transmits the address byte corresponding to the internal memory address being accessed. After receiving the address byte, the device again responds with an acknowledge bit. Next, the controller device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the device again responds with an acknowledge bit. Finally, the controller device transmits a stop condition to complete the single-byte data-write transfer.

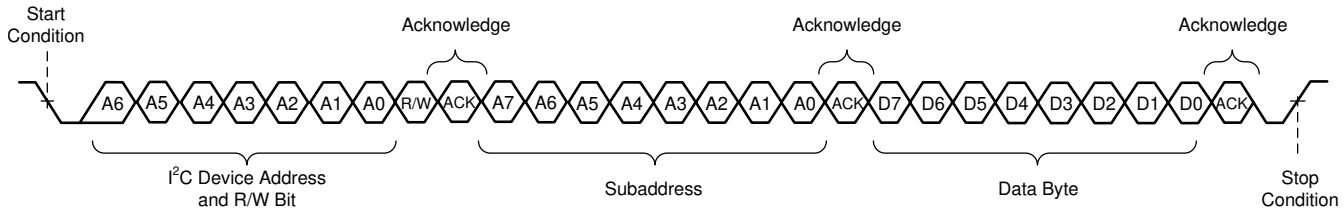


図 9-10. Random Write Transfer

9.5.2.2 Sequential Write

A sequential data-write transfer is identical to a single-byte data-write transfer except that multiple data bytes are transmitted by the controller to the device as shown in 図 9-11. After receiving each data byte, the device responds with an acknowledge bit and the I2 subaddress is automatically incremented by one.

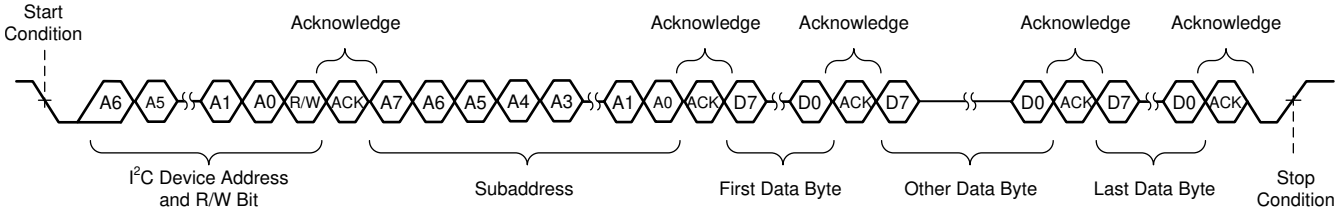


図 9-11. Sequential Write Transfer

9.5.2.3 Random Read

As shown in 図 9-12, a single-byte data-read transfer begins with the controller device transmitting a start condition followed by the I2C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is a 0. After receiving the address and the read/write bit, the device responds with an acknowledge bit. In addition, after sending the internal memory address byte, the controller device transmits another start condition followed by the address and the read/write bit again. This time the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the device again responds with an acknowledge bit. Next, the device transmits the data byte from the memory address being read. After receiving the data byte, the controller device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

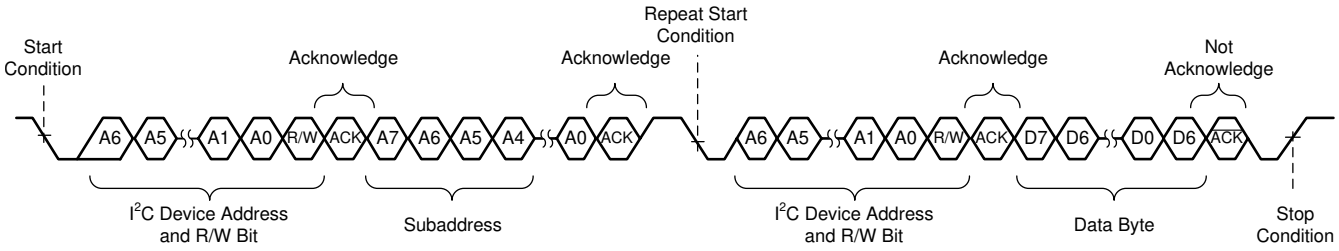


図 9-12. Random Read Transfer

9.5.2.4 Sequential Read

A sequential data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the device to the controller device as shown in 図 9-13. Except for the last data byte, the controller device responds with an acknowledge bit after receiving each data byte and automatically increments the I2C sub address by one. After receiving the last data byte, the controller device transmits a not-acknowledge followed by a stop condition to complete the transfer.

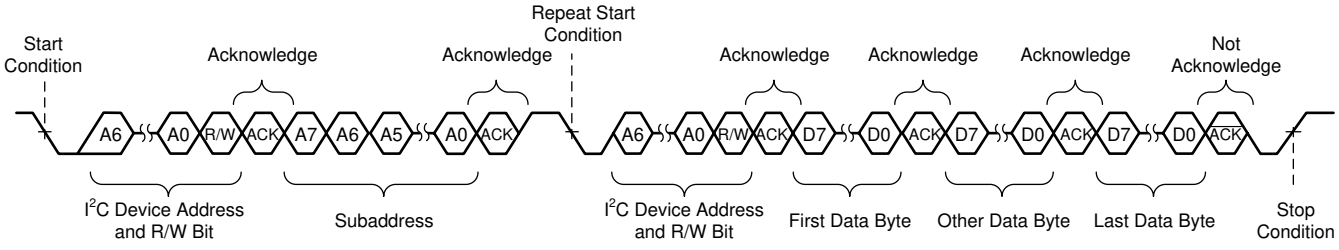


図 9-13. Sequential Read Transfer

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9.5.2.5 DSP Memory Book, Page and BQ update

On Page 0x00 of each book, Register 0x7f is used to change the book. Register 0x00 of each page is used to change the page. To change a Page first write 0x00 to Register 0x00 to switch to Page 0 then write the book number to Register 0x7f on Page 0. To switch between pages in a book, simply write the page number to register 0x00.

All the Biquad Filters coefficients are addressed in book 0xAA. The five coefficients of every Biquad Filter must be written entirely and sequentially from the lowest address to the highest address. The address of all Biquad Filters can be found in セクション 9.6.

All DSP/Audio Process Flow Related Register are listed in Application Note, TAS5825P Process Flows.

9.5.2.6 Checksum

This device supports two different check sum schemes, a cyclic redundancy check (CRC) checksum and an Exclusive (XOR) checksum. Register reads do not change checksum, but writes to even nonexistent registers changes the checksum. Both checksums are 8-bit checksums and both are available together simultaneously. The checksums can be reset by writing a starting value (eg. 0x 00 00 00 00) to their respective 4-byte register locations.

9.5.2.6.1 Cyclic Redundancy Check (CRC) Checksum

The 8-bit CRC checksum used is the 0x7 polynomial (CRC-8-CCITT I.432.1; ATM HEC, ISDN HEC and cell delineation, (1 + x1 + x2 + x8)). A major advantage of the CRC checksum is that the input order is sensitive. The CRC supports all I^2C transactions, excluding book and page switching. The CRC checksum is read from register 0x7E on page0 of any book (B_x, Page_0, Reg_126). The CRC checksum can be reset by writing 0x00 to the same register locations where the CRC checksum is valid.

9.5.2.6.2 Exclusive or (XOR) Checksum

The XOR checksum is a simpler checksum scheme. XOR checksum performs sequential XOR of each register byte write with the previous 8-bit checksum register value. XOR supports only Book 0x8C, and excludes page switching and all registers in Page 0x00 of Book 0x8C. XOR checksum is read from location register 0x7D on page 0x00 of book 0x8C (B_140, Page_0, Reg_125). The XOR Checksum can be reset by writing 0x00 to the same register location where XOR Checksum is read.

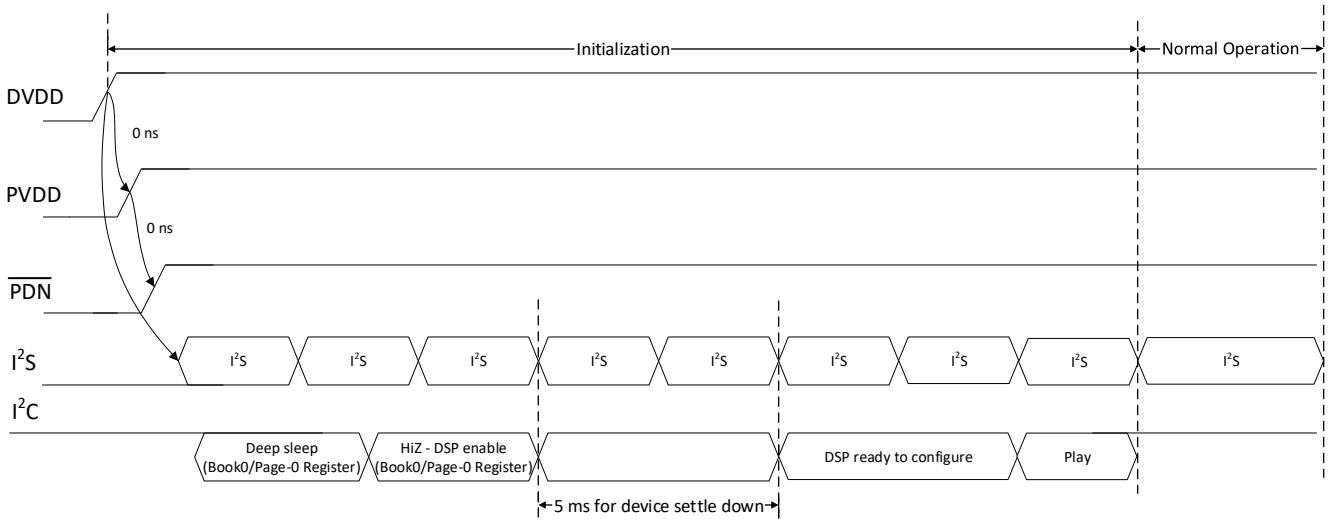
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9.5.3 Control via Software

- Startup Procedures
- Shutdown Procedures

9.5.3.1 Startup Procedures

1. Configure ADR pin with proper setting for I²C device address.
2. Bring up power supplies (it does not matter if PVDD or DVDD comes up first).
3. Once power supplies are stable, bring up $\overline{\text{PDN}}$ to High, then start SCLK, LRCLK.
4. Once I²S clock are stable, set the device into HiZ state and enable DSP via the I2C control port.
5. Wait 5 ms at least. Then initialize the DSP Coefficient, and set the device to Play state
6. The device is now in normal operation.



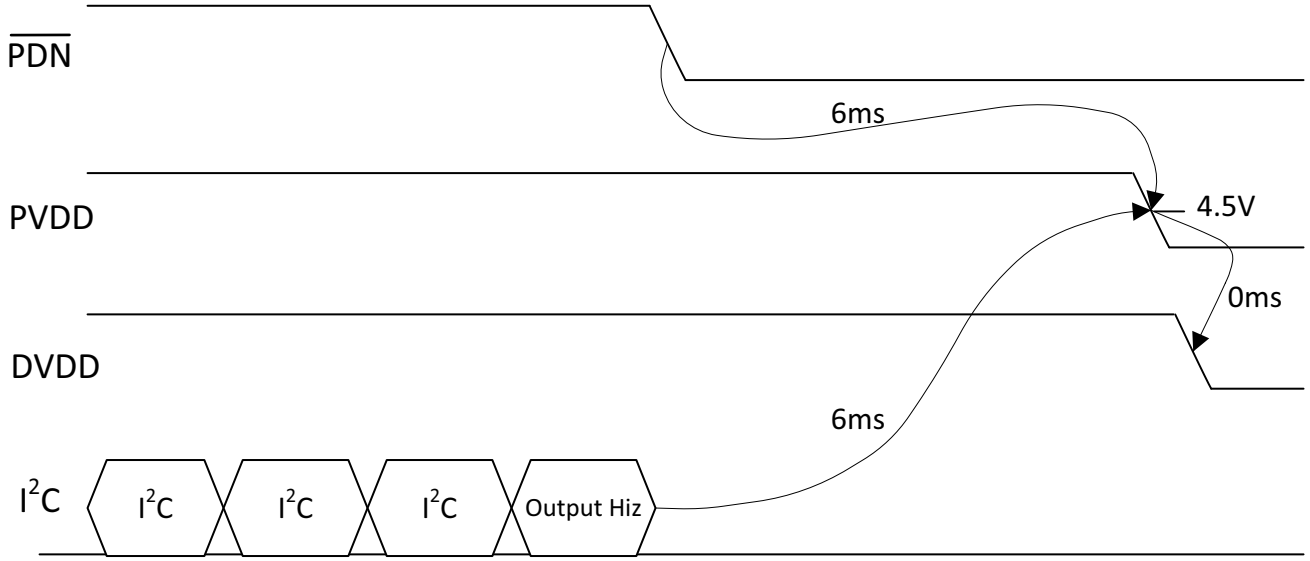
A. I²S only permits to start after DVDD fully powered up. But No sequence requirement with PDN.
B. I²C only response with PDN brought up to HIGH.
C. If I²C register is general register in Book 0, no sequence requirement, then write/read BEFORE or AFTER I2S clock ready. But if I²C register is DSP register (Other BOOK/PAGE), TI suggests to follow the 5 ms requirements and make sure I²S clock is ready (Especially for the first time initialization after power up).
D. No sequence requirement for PVDD and DVDD.

図 9-14. Start-up Sequence

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9.5.3.2 Shutdown Procedures

1. The device is in normal operation.
2. Configure the Register 0x03h -D[1:0]=10 (Hiz) via the I^2C control port or Pull $\overline{PDN}$ low.
3. Wait at least 6 ms (this time depends on the LRCLK rate ,digital volume and digital volume ramp down rate).
4. Bring down power supplies.
5. The device is now fully shutdown and powered off.



A. Before PVDD/DVDD power down, Class D Output driver needs to be disabled by PDN or by I^2C

B. At least 6 ms delay needed based on LRCLK (Fs) = 48 kHz, Digital volume ramp down update every sample period, decreased by 0.5 dB for each update, digital volume = 24 dB. Change the value of register 0x4C and 0x4E or change the LRCLK rate, the delay changes.

図 9-15. Power-Down Sequence

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9.5.3.3 Protection and Monitoring

9.5.3.3.1 Overcurrent Limit (Cycle-By-Cycle)

The CBC current-limiting circuit terminates each PWM pulse limit the output current flow to the average current limit (I_{LIM}) threshold. The overall effect on the audio in the case of a current overload is quite similar a voltage-clipping event, temporarily limiting power at the peaks of the music signal and normal operation continues without disruption on removal of the overload.

注

CBC (Cycle-By-Cycle) current-limiting only allows in BTL mode, not allowed under PBTL.

9.5.3.3.2 Overcurrent Shutdown (OCSD)

Under severe short-circuit event, such as a short to PVDD or ground, the device uses a peak-current detector, and the affected channel shuts down in < 100 ns if the peak current are enough. The shutdown speed depends on a number of factors, such as the impedance of the short circuit, supply voltage, and switching frequency. The user can restart the affected channel via I^2C. An OCSD event activates the fault pin, and the I^2 fault register saves a record. If the supply or ground short is strong enough to exceed the peak current threshold but not severe enough to trigger the OCSD, the peak current limiter prevents excess current from damaging the output FETs, and operation returns to normal after the short is removed.

9.5.3.3.3 DC Detect

If the TAS5825P device measures a DC offset in the output voltage, the FAULTZ line is pulled low and the OUTxx outputs transition to high impedance, signifying a fault.

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9.6 Register Maps

9.6.1 CONTROL PORT Registers

表 9-6 lists the memory-mapped registers for the CONTROL PORT. All register offset addresses not listed in 表 9-6 must be considered as reserved locations and the register contents must not be modified.

表 9-6. CONTROL PORT Registers

Offset	Acronym	Register Name	Section
1h	RESET_CTRL	Register 1	Go
2h	DEVICE_CTRL_1	Register 2	Go
3h	DEVICE_CTRL2	Register 3	Go
Fh	I2C_PAGE_AUTO_INC	Register 15	Go
28h	SIG_CH_CTRL	Register 40	Go
29h	CLOCK_DET_CTRL	Register 41	Go
30h	SDOUT_SEL	Register 48	Go
31h	I2S_CTRL	Register 49	Go
33h	SAP_CTRL1	Register 51	Go
34h	SAP_CTRL2	Register 52	Go
37h	FS_MON	Register 55	Go
38h	BCK (SCLK)_MON	Register 56	Go
39h	CLKDET_STATUS	Register 57	Go
40h	DSP_PGM_MODE	Register 64	Go
46h	DSP_CTRL	Register 70	Go
4Ch	DIG_VOL	Register 76	Go
4Eh	DIG_VOL_CTRL1	Register 78	Go
4Fh	DIG_VOL_CTRL2	Register 79	Go
50h	AUTO_MUTE_CTRL	Register 80	Go
51h	AUTO_MUTE_TIME	Register 81	Go
53h	ANA_CTRL	Register 83	Go
54h	AGAIN	Register 84	Go
55h	SPI_CLK	Register 85	Go
56h	EEPROM_CTRL0	Register 86	Go
57h	EEPROM_RD_CMD	Register 87	Go
58h	EEPROM_ADDR_START0	Register 88	Go
59h	EEPROM_ADDR_START1	Register 89	Go
5Ah	EEPROM_ADDR_START2	Register 90	Go
5Bh	EEPROM_BOOT_STATUS	Register 91	Go
5Ch	BQ_WR_CTRL1	Register 92	Go
5Eh	PVDD_ADC	Register 94	Go
60h	GPIO_CTRL	Register 96	Go
61h	GPIO0_SEL	Register 97	Go
62h	GPIO1_SEL	Register 98	Go
63h	GPIO2_SEL	Register 99	Go
64h	GPIO_INPUT_SEL	Register 100	Go
65h	GPIO_OUT	Register 101	Go
66h	GPIO_OUT_INV	Register 102	Go
67h	DIE_ID	Register 103	Go
68h	POWER_STATE	Register 104	Go

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表 9-6. CONTROL PORT Registers (continued)

Offset	Acronym	Register Name	Section
69h	AUTOMUTE_STATE	Register 105	Go
6Ah	PHASE_CTRL	Register 106	Go
6Bh	SS_CTRL0	Register 107	Go
6Ch	SS_CTRL1	Register 108	Go
6Dh	SS_CTRL2	Register 109	Go
6Eh	SS_CTRL3	Register 110	Go
6Fh	SS_CTRL4	Register 111	Go
70h	CHAN_FAULT	Register 112	Go
71h	GLOBAL_FAULT1	Register 113	Go
72h	GLOBAL_FAULT2	Register 114	Go
73h	WARNING	Register 115	Go
74h	PIN_CONTROL1	Register 116	Go
75h	PIN_CONTROL2	Register 117	Go
76h	MISC_CONTROL	Register 118	Go
77h	CBC_CONTROL	Register 119	Go
78h	FAULT_CLEAR	Register 120	Go

Complex bit access types are encoded to fit into small table cells. 表 9-7 shows the codes that are used for access types in this section.

表 9-7. CONTROL PORT Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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9.6.1.1 RESET_CTRL Register (Offset = 1h) [reset = 0x00]

RESET_CTRL is shown in 図 9-12 and described in 表 9-8.

Return to Summary Table.

図 9-16. RESET_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			RST_MOD	RESERVED			RST_REG
R/W			W	R			W

表 9-8. RESET_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4	RST_DIG_CORE	W	0	WRITE CLEAR BIT Reset DIG_CORE WRITE CLEAR BIT Reset Full Digital Core. This bit resets the Full Digital Signal Path (Include DSP coefficient RAM and I2C Control Port Registers), Since the DSP is also reset, the coeffient RAM content is also cleared by the DSP. 0: Normal 1: Reset Full Digital Signal Path
3-1	RESERVED	R	000	This bit is reserved
0	RST_REG	W	0	WRITE CLEAR BIT Reset Registers This bit resets the mode registers back to their initial values. Only reset Control Port Registers, The RAM content is not cleared. 0: Normal 1: Reset I^2C Control Port Registers

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9.6.1.2 DEVICE_CTRL_1 Register (Offset = 2h) [reset = 0x00]

DEVICE_CTRL_1 is shown in 図 9-13 and described in 表 9-9.

Return to Summary Table.

図 9-17. DEVICE_CTRL_1 Register

7	6	5	4	3	2	1	0
RESERVED	FSW_SEL			RESERVED	DAMP_PBTL	DAMP_MOD	
R/W	R/W			R/W	R/W	R/W	

表 9-9. DEVICE_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-4	FSW_SEL	R/W	000	SELECT FSW 000: 384K 010: 480K 011: 576K 100: 768K 001: Reserved 101: Reserved 110: Reserved 111: Reserved
3	RESERVED	R/W	0	This bit is reserved
2	DAMP_PBTL	R/W	0	0: SET DAMP TO BTL MODE 1: SET DAMP TO PBTL MODE
1-0	DAMP_MOD	R/W	00	00: BD MODE 01: 1SPW MODE 10: HYBRID MODE (Need to select supporting process flows in PPC3)

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9.6.1.3 DEVICE_CTRL2 Register (Offset = 3h) [reset = 00x10]

DEVICE_CTRL2 is shown in 図 9-14 and described in 表 9-10.

Return to Summary Table.

図 9-18. DEVICE_CTRL2 Register

7	6	5	4	3	2	1	0
RESERVED			DIS_DSP	MUTE_LEFT	RESERVED	CTRL_STATE	
R/W			R/W	R/W	R/W	R/W	

表 9-10. DEVICE_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4	DIS_DSP	R/W	1	DSP reset When the bit is made 0, DSP starts powering up and send out data. This needs to be made 0 only after all the input clocks are settled so that DMA channels do not go out of sync. 0: Normal operation 1: Reset the DSP
3	MUTE	R/W	0	Mute both Left and Right Channel This bit issues soft mute request for both left and right channel. The volume is smoothly ramped down/up to avoid pop/click noise. 0: Normal volume 1: Mute
2	RESERVED	R/W	0	This bit is reserved
1-0	CTRL_STATE	R/W	00	device state control register 00: Deep Sleep 01: Sleep 10: Hiz, 11: PLAY

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9.6.1.4 I2C_PAGE_AUTO_INC Register (Offset = Fh) [reset = 0x00]

I2C_PAGE_AUTO_INC is shown in 図 9-15 and described in 表 9-11.

Return to Summary Table.

図 9-19. I2C_PAGE_AUTO_INC Register

7	6	5	4	3	2	1	0
RESERVED				PAGE_AUTOINC_REG	RESERVED		
R/W				R/W	R/W		

表 9-11. I2C_PAGE_AUTO_INC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	This bit is reserved
3	PAGE_AUTOINC_REG	R/W	0	Page auto increment disable Disable page auto increment mode for non-zero books. When end of page is reached, the page goes back to 8th address location of next page when this bit is 0. When this bit is 1, the page goes to 0 th location of current page itself like in older part. 0: Enable Page auto increment 1: Disable Page auto increment
2-0	RESERVED	R/W	000	This bit is reserved

9.6.1.5 SIG_CH_CTRL Register (Offset = 28h) [reset = 0x00]

SIG_CH_CTRL is shown in 図 9-16 and described in 表 9-12.

Return to Summary Table.

図 9-20. SIG_CH_CTRL Register

7	6	5	4	3	2	1	0
SCLK_RATIO_CONFIGURE				FSMODE	RESERVED		
R/W				R/W	R/W		

表 9-12. SIG_CH_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	SCLK_RATIO_CONFIGURE	R/W	0000	These bits indicate the configured SCLK ratio, the number of SCLK clocks in one audio frame. Device sets this ratio automatically. 4'b0011:32FS 4'b0101:64FS 4'b0111:128FS 4'b1001:256FS 4'b1011:512FS
3	FSMODE	R/W	0	FS Speed Mode: These bits select the FS operation mode, which must be set according to the current audio sampling rate. Need to set the mode manually. If the input Fs is 44.1 kHz/88.2 kHz/176.4 kHz. 4 'b0000 Auto detection 4 'b0100 Reserved 4 'b0110 32 KHz 4 'b1000 44.1 KHz 4 'b1001 48 KHz 4'b1010 88.2 KHz 4 'b1011 96 KHz 4 'b1100 176.4 KHz 4 'b1101 192 KHz Others Reserved

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表 9-12. SIG_CH_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	RESERVED	R/W	000	This bit is reserved

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9.6.1.6 CLOCK_DET_CTRL Register (Offset = 29h) [reset = 0x00]

CLOCK_DET_CTRL is shown in 図 9-17 and described in 表 9-13.

Return to Summary Table.

図 9-21. CLOCK_DET_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	DIS_DET_PLL	DIS_DET_SCLK_RANGE	DIS_DET_FS	DIS_DET_SCLK	DIS_DET_MISS	RESERVED	DIS_DET_LOCK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

表 9-13. CLOCK_DET_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6	DIS_DET_PLL	R/W	0	Ignore PLL Overate Detection This bit controls whether to ignore the PLL overrate detection. The PLL must be slow than 150 MHz or an error is reported. When ignored, a PLL overrate error does not cause a clock error. 0: Regard PLL overrate detection. 1: Ignore PLL overrate detection.
5	DIS_DET_SCLK_RANGE	R/W	0	Ignore BCK Range Detection This bit controls whether to ignore the SCLK range detection. The SCLK must be stable between 256 KHz and 50 MHz or an error is reported. When ignored, a SCLK range error does not cause a clock error. 0: Regard BCK Range detection 1: Ignore BCK Range detection
4	DIS_DET_FS	R/W	0	Ignore FS Error Detection This bit controls whether to ignore the FS Error detection. When ignored, FS error does not cause a clock error. But CLKDET_STATUS reports fs error. 0: Regard FS detection 1: Ignore FS detection
3	DIS_DET_SCLK	R/W	0	Ignore SCLK Detection This bit controls whether to ignore the SCLK detection against LRCK. The SCLK must be stable between 32FS and 512FS inclusive or an error is reported. When ignored, a SCLK error does not cause a clock error. 0: Regard SCLK detection 1: Ignore SCLK detection
2	DIS_DET_MISS	R/W	0	Ignore SCLK Missing Detection This bit controls whether to ignore the SCLK missing detection. When ignored an SCLK missing does not cause a clock error. 0: Regard SCLK missing detection 1: Ignore SCLK missing detection
1	RESERVED	R/W	0	This bit is reserved
0	DIS_DET_LOCK	R/W	0	This bit is reserved

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9.6.1.7 SDOUT_SEL Register (Offset = 30h) [reset = 0x00]

SDOUT_SEL is shown in 図 9-19 and described in 表 9-14.

Return to Summary Table.

図 9-22. SDOUT_SEL Register

7	6	5	4	3	2	1	0
RESERVED					RESERVED		SDOUT_SEL
R/W					R/W		R/W

表 9-14. SDOUT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000000	These bits are reserved
0	SDOUT_SEL	R/W	0	SDOUT Select. This bit selects what is being output as SDOUT pin. 0: SDOUT is the DSP output (post-processing) 1: SDOUT is the DSP input (pre-processing)

9.6.1.8 I2S_CTRL Register (Offset = 31h) [reset = 0x00]

I2S_CTRL is shown in 図 9-19 and described in 表 9-15.

Return to Summary Table.

図 9-23. I2S_CTRL Register

7	6	5	4	3	2	1	0
RESERVED		SCLK_INV	RESERVED	RESERVED	RESERVED		RESERVED
R/W		R/W	R/W	R	R		R/W

表 9-15. I2S_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5	SCLK_INV	R/W	0	SCLK Polarity This bit sets the inverted SCLK mode. In inverted SCLK mode, the DAC assumes that the LRCK and DIN edges are aligned to the rising edge of the SCLK. Normally the LRCK and DIN edges are assumed to be aligned to the falling edge of the SCLK 0: Normal SCLK mode 1: Inverted SCLK mode
4	RESERVED	R/W	0	This bit is reserved
3	RESERVED	R	0	This bit is reserved
2-1	RESERVED	R/W	00	This bit is reserved
0	RESERVED	R/W	0	This bit is reserved

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9.6.1.9 SAP_CTRL1 Register (Offset = 33h) [reset = 0x02]

SAP_CTRL1 is shown in 図 9-20 and described in 表 9-16.

Return to Summary Table.

図 9-24. SAP_CTRL1 Register

7	6	5	4	3	2	1	0
I2S_SHIFT_MSB	RESERVED	DATA_FORMAT		I2S_LRCLK_PULSE		WORD_LENGTH	
R/W	R/W	R/W		R/W		R/W	

表 9-16. SAP_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2S_SHIFT_MSB	R/W	0	I2S Shift MSB
6	RESERVED	R/W	0	This bit is reserved
5-4	DATA_FORMAT	R/W	00	I2S Data Format These bits control both input and output audio interface formats for DAC operation. 00: I2S 01: TDM/DSP 10: RTJ 11: LTJ
3-2	I2S_LRCLK_PULSE	R/W	00	01: LRCLK pulse < 8 SCLK
1-0	WORD_LENGTH	R/W	10	I2S Word Length These bits control both input and output audio interface sample word lengths for DAC operation. 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits

9.6.1.10 SAP_CTRL2 Register (Offset = 34h) [reset = 0x00]

SAP_CTRL2 is shown in 図 9-21 and described in 表 9-17.

Return to Summary Table.

図 9-25. SAP_CTRL2 Register

7	6	5	4	3	2	1	0
I2S_SHIFT							
R/W							

表 9-17. SAP_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	I2S_SHIFT	R/W	00000000	I2S Shift LSB These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of SCLK from the starting (MSB) of audio frame to the starting of the desired audio sample. 000000000: offset = 0 SCLK (no offset) 000000001: offset = 1 SCLK 000000010: offset = 2 SCLKs and 111111111: offset = 512 SCLKs

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9.6.1.11 FS_MON Register (Offset = 37h) [reset = 0x00]

FS_MON is shown in 図 9-22 and described in 表 9-18.

Return to Summary Table.

図 9-26. FS_MON Register

7	6	5	4	3	2	1	0
RESERVED		SCLK_RATIO_HIGH		FS			
R/W		R		R			

表 9-18. FS_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5-4	SCLK_RATIO_HIGH	R	00	2 msbs of detected SCLK ratio
3-0	FS	R	0000	These bits indicate the currently detected audio sampling rate. 4 'b0000 FS Error 4 'b0100 16 KHz 4 'b0110 32 KHz 4 'b1000 Reserved 4 'b1001 48 KHz 4 'b1011 96 KHz 4 'b1101 192 KHz Others Reserved

9.6.1.12 BCK (SCLK)_MON Register (Offset = 38h) [reset = 0x00]

BCK_MON is shown in 図 9-23 and described in 表 9-19.

Return to Summary Table.

図 9-27. BCK (SCLK)_MON Register

7	6	5	4	3	2	1	0
BCLK (SCLK)_RATIO_LOW							
R							

表 9-19. BCK_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BCLK (SCLK)_RATIO_LOW	R	00000000	These bits indicate the currently detected BCK (SCLK) ratio, the number of BCK (SCLK) clocks in one audio frame. BCK (SCLK) = approximately 32 FS – 512 FS

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9.6.1.13 CLKDET_STATUS Register (Offset = 39h) [reset = 0x00]

CLKDET_STATUS is shown in 図 9-24 and described in 表 9-20.

Return to Summary Table.

図 9-28. CLKDET_STATUS Register

7	6	5	4	3	2	1	0
RESERVED		DET_STATUS					
R/W		R					

表 9-20. CLKDET_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5-0	DET_STATUS	R	000000	bit0: In auto detection mode(reg_fsmode=0), this bit indicated whether the audio sampling rate is valid or not. In non auto detection mode(reg_fsmode!=0), Fs error indicates that configured fs is different with detected fs. Even FS Error Detection Ignore is set, this flag is also asserted. bit1: This bit indicates whether the SCLK is valid or not. The SCLK ratio must be stable and in the range of 32-512FS to be valid. bit2: This bit indicates whether the SCLK is missing or not. bit3: This bit indicates whether the PLL is locked or not. The PLL is reported as unlocked when disabled. bits4: This bit indicates whether the PLL is overrate. bits5: This bit indicates whether the SCLK is overrate or underrate.

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9.6.1.14 DSP_PGM_MODE Register (Offset = 40h) [reset = 0x01]

DSP_PGM_MODE is shown in 図 9-25 and described in 表 9-21.

Return to Summary Table.

図 9-29. DSP_PGM_MODE Register

7	6	5	4	3	2	1	0
RESERVED				CH_A_HIZ	CH_B_HIZ	MODE_SEL	
R/W				R/W	R/W	R/W	

表 9-21. DSP_PGM_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	These bits are reserved
3	CH_A_HIZ	R/W	0	1: Force Channel A (L channel) to Hiz mode. 0: Exit Force Hi-Z mode, Channel A is now controlled by Register 0x03, see 表 9-10. Notes: If channel has been forced to Hiz, only method to exit Force Hi-Z mode is set this bit to 0. This function is disabled in PBTL mode.
2	CH_B_HIZ	R/W	0	1: Force Channel B (R channel) to Hiz mode. 0: Exit Force Hi-Z mode, Channel B is now controlled by Register 0x03, see 表 9-10. Notes: If channel has been forced to Hiz, only method to exit Force Hi-Z mode is set this bit to 0. This function is disabled in PBTL mode.
1-0	MODE_SEL	R/W	01	DSP Program Selection These bits select the DSP program to use for audio processing. 00 => ram mode 01 => rom mode 1 10 => rom mode 2 11 => rom mode 3

9.6.1.15 DSP_CTRL Register (Offset = 46h) [reset = 0x01]

DSP_CTRL is shown in 図 9-26 and described in 表 9-22.

Return to Summary Table.

図 9-30. DSP_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			USER_DEFINED_PROCESSING_RATE		RESERVED	BOOT_FROM_IRAM	USE_DEFAULT_COEFFS
R/W			R/W		R	R/W	R/W

表 9-22. DSP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4-3	USER_DEFINED_PROCESSING_RATE	R/W	00	00:input 01:48k 10:96k 11:192k
2	RESERVED	R	0	This bit is reserved
1	RESERVED	R	0	This bit is reserved

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表 9-22. DSP_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	USE_DEFAULT_COEFFS	R/W	1	Use default coefficients from ZROM this bit controls whether to use default coefficients from ZROM or use the non-default coefficients downloaded to device by the Host 0 : don't use default coefficients from ZROM 1 : use default coefficients from ZROM

9.6.1.16 DIG_VOL Register (Offset = 4Ch) [reset = 30h]

DIG_VOL is shown in 図 9-27 and described in 表 9-23.

Return to Summary Table.

図 9-31. DIG_VOL Register

7	6	5	4	3	2	1	0
PGA_LEFT							
R/W							

表 9-23. DIG_VOL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PGA	R/W	00110000	Digital Volume These bits control both left and right channel digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step. 00000000: +24.0 dB 00000001: +23.5 dB ..... and 00101111: +0.5 dB 00110000: 0.0 dB 00110001: -0.5 dB ..... 11111110: -103 dB 11111111: Mute

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9.6.1.17 DIG_VOL_CTRL1 Register (Offset = 4Eh) [reset = 0x33]

DIG_VOL_CTRL1 is shown in 図 9-28 and described in 表 9-24.

Return to Summary Table.

図 9-32. DIG_VOL_CTRL1 Register

7	6	5	4	3	2	1	0
PGA_RAMP_DOWN_SPEED		PGA_RAMP_DOWN_STEP		PGA_RAMP_UP_SPEED		PGA_RAMP_UP_STEP	
R/W		R/W		R/W		R/W	

表 9-24. DIG_VOL_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PGA_RAMP_DOWN_SPEED	R/W	00	Digital Volume Normal Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	PGA_RAMP_DOWN_STEP	R/W	11	Digital Volume Normal Ramp Down Step These bits control the step of the digital volume updates when the volume is ramping down. 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update 11: Decrement by 0.5 dB for each update
3-2	PGA_RAMP_UP_SPEED	R/W	00	Digital Volume Normal Ramp Up Frequency These bits control the frequency of the digital volume updates when the volume is ramping up. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly restore the volume (Instant unmute)
1-0	PGA_RAMP_UP_STEP	R/W	11	Digital Volume Normal Ramp Up Step These bits control the step of the digital volume updates when the volume is ramping up. 00: Increment by 4 dB for each update 01: Increment by 2 dB for each update 10: Increment by 1 dB for each update 11: Increment by 0.5 dB for each update

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9.6.1.18 DIG_VOL_CTRL2 Register (Offset = 4Fh) [reset = 0x30]

DIG_VOL_CTRL2 is shown in 図 9-29 and described in 表 9-25.

Return to Summary Table.

図 9-33. DIG_VOL_CTRL2 Register

7	6	5	4	3	2	1	0
FAST_RAMP_DOWN_SPEED		FAST_RAMP_DOWN_STEP		RESERVED			
R/W		R/W		R/W			

表 9-25. DIG_VOL_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	FAST_RAMP_DOWN_SPEED	R/W	00	Digital Volume Emergency Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	FAST_RAMP_DOWN_STEP	R/W	11	Digital Volume Emergency Ramp Down Step These bits control the step of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute. 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update 11: Decrement by 0.5 dB for each update
3-0	RESERVED	R/W	0000	This bit is reserved

9.6.1.19 AUTO_MUTE_CTRL Register (Offset = 50h) [reset = 0x07]

AUTO_MUTE_CTRL is shown in 図 9-30 and described in 表 9-26.

Return to Summary Table.

図 9-34. AUTO_MUTE_CTRL Register

7	6	5	4	3	2	1	0
RESERVED					REG_AUTO_MUTE_CTRL		
R/W					R/W		

表 9-26. AUTO_MUTE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	00000	This bit is reserved
2-0	REG_AUTO_MUTE_CTRL	R/W	111	bit0: 0: Disable left channel auto mute 1: Enable left channel auto mute bit1: 0: Disable right channel auto mute 1: Enable right channel auto mute bit2: 0: Auto mute left channel and right channel independently. 1: Auto mute left and right channels only when both channels are about to be auto muted.

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9.6.1.20 AUTO_MUTE_TIME Register (Offset = 51h) [reset = 0x00]

AUTO_MUTE_TIME is shown in 図 9-31 and described in 表 9-27.

Return to Summary Table.

図 9-35. AUTO_MUTE_TIME Register

7	6	5	4	3	2	1	0
RESERVED	AUTOMUTE_TIME_LEFT			RESERVED	AUTOMUTE_TIME_RIGHT		
R/W	R/W			R/W	R/W		

表 9-27. AUTO_MUTE_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-4	AUTOMUTE_TIME_LEFT	R/W	000	Auto Mute Time for Left Channel These bits specify the length of consecutive zero samples at left channel before the channel can be auto muted. The times shown are for 96 kHz sampling rate and are scaled with other rates. 000: 11.5 ms 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec
3	RESERVED	R/W	0	This bit is reserved
2-0	AUTOMUTE_TIME_RIGHT	R/W	000	Auto Mute Time for Right Channel These bits specify the length of consecutive zero samples at right channel before the channel can be auto muted. The times shown are for 96 kHz sampling rate and are scaled with other rates. 000: 11.5 ms 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec

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9.6.1.21 ANA_CTRL Register (Offset = 53h) [reset = 0h]

ANA_CTRL is shown in 図 9-32 and described in 表 9-28

Return to Summary Table

図 9-36. ANA_CTRL Register

7	6	5	4	3	2	1	0
AMUTE_DLY							
R/W							

表 9-28. ANA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-5	Class D bandwidth control	R/W	00	00: 100 kHz 01: 80 kHz 10: 120 kHz 11:175 kHz With Fsw=384 kHz, 100 kHz bandwidth is selected for high audio performance. With Fsw=768 kHz, 175 kHz bandwidth must be selected for high audio performance.
4-1	RESERVED	R/W	0000	These bits are reserved
0	L and R PWM output phase control	R/W	0	0: out of phase 1: in phase

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9.6.1.22 AGAIN Register (Offset = 54h) [reset = 0x00]

AGAIN is shown in 図 9-33 and described in 表 9-29.

Return to Summary Table.

図 9-37. AGAIN Register

7	6	5	4	3	2	1	0
RESERVED				ANA_GAIN			
R/W				R/W			

表 9-29. AGAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4-0	ANA_GAIN	R/W	00000	Analog Gain Control This bit controls the analog gain. 00000: 0 dB (29.5V peak voltage) 00001: -0.5db ... 11111: -15.5 dB

9.6.1.23 SPI_CLK Register (Offset = 55h) [reset = 0x00]

SPI_CLK is shown in 図 9-34 and described in 表 9-30.

Return to Summary Table.

図 9-38. SPI_CLK Register

7	6	5	4	3	2	1	0
RESERVED				SPI_CLK_SEL			
R/W				R/W			

表 9-30. SPI_CLK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	This bit is reserved
3-0	SPI_CLK_SEL	R/W	0000	00: 1.25M 01: 2.5M 10: 5M 11: 10M

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9.6.1.24 EEPROM_CTRL0 Register (Offset = 56h) [reset = 0x00]

EEPROM_CTRL0 is shown in 図 9-35 and described in 表 9-31.

Return to Summary Table.

図 9-39. EEPROM_CTRL0 Register

7	6	5	4	3	2	1	0
RESERVED		EEPROM_ADDR_24BITS_ENABLE	SPI_CLK_RATE		SPI_INV_POLAR	SPI_MST_LSB	LOAD_EEPROM_START
R/W		R/W	R/W		R/W	R/W	R/W

表 9-31. EEPROM_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5	EEPROM_ADDR_24BITS_ENABLE	R/W	0	enable 24 bits mode for EEPROM address
4-3	SPI_CLK_RATE	R/W	00	0: spi clock rate = 1.25 MHz 1: spi clock rate = 2.5 MHz 2: spi clock rate = 5 MHz 3: spi clock rate = 10 MHz
2	SPI_INV_POLAR	R/W	0	0: spi serial data change at post edge SCK 1: spi serial data change at neg edge SCK
1	SPI_MST_LSB	R/W	0	0: msb first 1: lsb first
0	LOAD_EEPROM_START	R/W	0	0: dsp coefficients read from host 1: dsp coefficients read from EEPROM

9.6.1.25 EEPROM_RD_CMD Register (Offset = 57h) [reset = 0x03]

EEPROM_RD_CMD is shown in 図 9-36 and described in 表 9-32.

Return to Summary Table.

図 9-40. EEPROM_RD_CMD Register

7	6	5	4	3	2	1	0
EEPROM_RD_CMD							
R/W-00000011							

表 9-32. EEPROM_RD_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEPROM_RD_CMD	R/W	00000011	EEPROM read command

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9.6.1.26 EEPROM_ADDR_START0 Register (Offset = 58h) [reset = 0x00]

EEPROM_ADDR_START0 is shown in 図 9-37 and described in 表 9-33.

Return to Summary Table.

図 9-41. EEPROM_ADDR_START0 Register

7	6	5	4	3	2	1	0
EEPROM_ADDR_START_HIGH							
R/W							

表 9-33. EEPROM_ADDR_START0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEPROM_ADDR_START_HIGH	R/W	00000000	8 msb of EEPROM read starting address for coefficient

9.6.1.27 EEPROM_ADDR_START1 Register (Offset = 59h) [reset = 0x00]

EEPROM_ADDR_START1 is shown in 図 9-38 and described in 表 9-34.

Return to Summary Table.

図 9-42. EEPROM_ADDR_START1 Register

7	6	5	4	3	2	1	0
EEPROM_ADDR_START_MIDDLE							
R/W							

表 9-34. EEPROM_ADDR_START1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEPROM_ADDR_START_MIDDLE	R/W	00000000	8 middle of EEPROM read starting address for coefficients

9.6.1.28 EEPROM_ADDR_START2 Register (Offset = 5Ah) [reset = 0h]

EEPROM_ADDR_START2 is shown in 図 9-39 and described in 表 9-35.

Return to Summary Table.

図 9-43. EEPROM_ADDR_START2 Register

7	6	5	4	3	2	1	0
EEPROM_ADDR_START_LOW							
R/W							

表 9-35. EEPROM_ADDR_START2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEPROM_ADDR_START_LOW	R/W	00000000	8 lsb of EEPROM read starting address for coefficients

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9.6.1.29 EEPROM_BOOT_STATUS Register (Offset = 5Bh) [reset = 0x00]

EEPROM_BOOT_STATUS is shown in 図 9-40 and described in 表 9-36.

Return to Summary Table.

図 9-44. EEPROM_BOOT_STATUS Register

7	6	5	4	3	2	1	0
RESERVED						LOAD_EEPROM_CRC_ERROR	LOAD_EEPROM_DONE
R						R	R

表 9-36. EEPROM_BOOT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000	This bit is reserved
1	LOAD_EEPROM_CRC_ERROR	R	0	0: CRC pass for EEPROM boot load 1: CRC don't pass for EEPROM boot load.
0	LOAD_EEPROM_DONE	R	0	Indicate that the EEPROM boot load has been finished.

9.6.1.30 BQ_WR_CTRL1 Register (Offset = 5Ch) [reset = 0x000]

BQ_WR_CTRL1 is shown in 図 9-41 and described in 表 9-37.

Return to Summary Table.

図 9-45. BQ_WR_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED							BQ_WR_FIRST_COEF
R/W							R/W

表 9-37. BQ_WR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000000	This bit is reserved
0	BQ_WR_FIRST_COEF	R/W	0	Indicate the first coefficient of a BQ is starting to write.

9.6.1.31 PVDD_ADC Register (Offset = 5Eh) [reset = 0h]

PVDD_ADC is shown in 図 9-42 and described in 表 9-38.

Return to Summary Table.

図 9-46. PVDD_ADC Register

7	6	5	4	3	2	1	0
ADC_DATA_OUT							
R							

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表 9-38. PVDD_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PVDD_ADC[7:0]	R	00000000	PVDD Voltage = PVDD_ADC[7:0] / 8.428 (V) 223: 26.45V 222: 26.34V 221:26.22V ... 39: 4.63V 38: 4.51V 37: 4.39V

9.6.1.32 GPIO_CTRL Register (Offset = 60h) [reset = 0x00]

GPIO_CTRL is shown in 図 9-43 and described in 表 9-39.

Return to Summary Table.

図 9-47. GPIO_CTRL Register

7	6	5	4	3	2	1	0
RESERVED					GPIO2_OE	GPIO1_OE	GPIO0_OE
R/W					R/W	R/W	R/W

表 9-39. GPIO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0000	This bit is reserved
2	GPIO2_OE	R/W	0	GPIO2 Output Enable This bit sets the direction of the GPIO2 pin 0: GPIO2 is input 1: GPIO2 is output
1	GPIO1_OE	R/W	0	GPIO1 Output Enable This bit sets the direction of the GPIO1 pin 0: GPIO1 is input 1: GPIO1 is output
0	GPIO0_OE	R/W	0	GPIO0 Output Enable This bit sets the direction of the GPIO0 pin 0: GPIO0 is input 1: GPIO0 is output

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9.6.1.33 GPIO0_SEL Register (Offset = 61h) [reset = 0x00]

GPIO0_SEL is shown in 図 9-44 and described in 表 9-40.

Return to Summary Table.

図 9-48. GPIO0_SEL Register

7	6	5	4	3	2	1	0
RESERVED				GPIO0_SEL			
R/W				R/W			

表 9-40. GPIO0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	This bit is reserved
3-0	GPIO0_SEL	R/W	0000	0000: off (low) 0001: Hybrid-Pro two level classG waveform control output 0010: Register GPIO0 output 0011: Auto mute flag (asserted when both L and R channels are auto muted) 0100: Auto mute flag for left channel 0101: Auto mute flag for right channel 0110: Clock invalid flag (clock error or clock missing) 0111: Reserved 1000: GPIO0 as WARNZ output 1001: Hybrid-Pro multi-level classH control waveform output 1011: GPIO0 as FAULTZ output 1100: GPIO0 as SPI CLK 1101: GPIO0 as SPI_PICO 1110: Reserved 1111: Reserved

9.6.1.34 GPIO1_SEL Register (Offset = 62h) [reset = 0x00]

GPIO1_SEL is shown in 図 9-45 and described in 表 9-41.

Return to Summary Table.

図 9-49. GPIO1_SEL Register

7	6	5	4	3	2	1	0
RESERVED				GPIO1_SEL			
R/W				R/W			

表 9-41. GPIO1_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	This bit is reserved

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表 9-41. GPIO1_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	GPIO1_SEL	R/W	0000	0000: off (low) 0001: Hybrid-Pro two level classG waveform control output 0010: Register GPIO1 output 0011: Auto mute flag (asserted when both L and R channels are auto muted) 0100: Auto mute flag for left channel 0101: Auto mute flag for right channel 0110: Clock invalid flag (clock error or clock missing) 0111: Reserved 1000: GPIO1 as WARNZ output 1001: Hybrid-Pro multi-level classH control waveform output 1011: GPIO1 as FAULTZ output 1100: GPIO1 as SPI CLK 1101: GPIO1 as SPI_PICO 1110: Reserved 1111: Reserved

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9.6.1.35 GPIO2_SEL Register (Offset = 63h) [reset = 0x00]

GPIO2_SEL is shown in 図 9-46 and described in 表 9-42.

Return to Summary Table.

図 9-50. GPIO2_SEL Register

7	6	5	4	3	2	1	0
RESERVED				GPIO2_SEL			
R/W				R/W			

表 9-42. GPIO2_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	This bit is reserved
3-0	GPIO2_SEL	R/W	0000	0000: off (low) 0001: Hybrid-Pro two level classG waveform control output 0010: Register GPIO2 output 0011: Auto mute flag (asserted when both L and R channels are auto muted) 0100: Auto mute flag for left channel 0101: Auto mute flag for right channel 0110: Clock invalid flag (clock error or clock missing) 0111: Reserved 1000: GPIO2 as WARNZ output 1001: Hybrid-Pro multi-level classH control waveform output 1011: GPIO2 as FAULTZ output 1100: GPIO2 as SPI CLK 1101: GPIO2 as SPI_PICO 1110: Reserved 1111: Reserved

9.6.1.36 GPIO_INPUT_SEL Register (Offset = 64h) [reset = 0x00]

GPIO_INPUT_SEL is shown in 図 9-47 and described in 表 9-43.

Return to Summary Table.

図 9-51. GPIO_INPUT_SEL Register

7	6	5	4	3	2	1	0
GPIO_SPI_PICO_SEL		GPIO_PHASE_SYNC_SEL		GPIO_RESETZ_SEL		GPIO_MUTEZ_SEL	
R/W		R/W		R/W		R/W	

表 9-43. GPIO_INPUT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	GPIO_SPI_PICO_SEL	R/W	00	00: N/A 01: GPIO0 10: GPIO1 11: GPIO2
5-4	GPIO_PHASE_SYNC_SEL	R/W	00	00: N/A 01: GPIO0 10: GPIO1 11: GPIO2
3-2	GPIO_RESETZ_SEL	R/W	00	00: N/A 01: GPIO0 10: GPIO1 11: GPIO2 can not be reset by GPIO reset

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表 9-43. GPIO_INPUT_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	GPIO_MUTEZ_SEL (Enable device into Hiz mode)	R/W	00	00: N/A 01: GPIO0 10: GPIO1 11: GPIO2

9.6.1.37 GPIO_OUT Register (Offset = 65h) [reset = 0x00]

GPIO_OUT is shown in 図 9-48 and described in 表 9-44.

Return to Summary Table.

図 9-52. GPIO_OUT Register

7	6	5	4	3	2	1	0
RESERVED						GPIO_OUT	
R/W						R/W	

表 9-44. GPIO_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	00000	This bit is reserved
2-0	GPIO_OUT	R/W	000	bit0: GPIO0 output bit1: GPIO1 output bit2: GPIO2 output

9.6.1.38 GPIO_OUT_INV Register (Offset = 66h) [reset = 0x00]

GPIO_OUT_INV is shown in 図 9-49 and described in 表 9-45.

Return to Summary Table.

図 9-53. GPIO_OUT_INV Register

7	6	5	4	3	2	1	0
RESERVED						GPIO_OUT	
R/W						R/W	

表 9-45. GPIO_OUT_INV Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	00000	This bit is reserved
2-0	GPIO_OUT	R/W	000	bit0: GPIO0 output invert bit1: GPIO1 output invert bit2: GPIO2 output invert

9.6.1.39 DIE_ID Register (Offset = 67h) [reset = 97h]

DIE_ID is shown in 図 9-50 and described in 表 9-46.

Return to Summary Table.

図 9-54. DIE_ID Register

7	6	5	4	3	2	1	0
DIE_ID							
R							

表 9-46. DIE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIE_ID	R	10010111	DIE ID

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9.6.1.40 POWER_STATE Register (Offset = 68h) [reset = 0x00]

POWER_STATE is shown in 図 9-51 and described in 表 9-47.

Return to Summary Table.

図 9-55. POWER_STATE Register

7	6	5	4	3	2	1	0
STATE_RPT							
R							

表 9-47. POWER_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	STATE_RPT	R	00000000	00: Deep sleep 01: Seep 10: HIZ 11: Play others: reserved

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9.6.1.41 AUTOMUTE_STATE Register (Offset = 69h) [reset = 0x00]

AUTOMUTE_STATE is shown in 図 9-52 and described in 表 9-48.

Return to Summary Table.

図 9-56. AUTOMUTE_STATE Register

7	6	5	4	3	2	1	0
RESERVED						ZERO_RIGHT_MON	ZERO_LEFT_MON
R						R	R

表 9-48. AUTOMUTE_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000	This bit is reserved
1	ZERO_RIGHT_MON	R	0	This bit indicates the auto mute status for right channel. 0: Not auto muted 1: Auto muted
0	ZERO_LEFT_MON	R	0	This bit indicates the auto mute status for left channel. 0: Not auto muted 1: Auto muted

9.6.1.42 PHASE_CTRL Register (Offset = 6Ah) [reset = 0]

PHASE_CTRL is shown in 図 9-53 and described in 表 9-49.

Return to Summary Table.

図 9-57. PHASE_CTRL Register

7	6	5	4	3	2	1	0
RESERVED				RAMP_PHASE_SEL		PHASE_SYNC_SEL	PHASE_SYNC_EN
R/W				R/W		R/W	R/W

表 9-49. PHASE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	This bit is reserved
3-2	RAMP_PHASE_SEL	R/WTAS	00	Select ramp clock phase when multi devices integrated in one system to reduce EMI and peak supply peak current, TI recommends to set all devices the same RAMP frequency and same spread spectrum. The devices must be set before driving device into PLAY mode if this feature is needed. 2'b00: phase 0 2'b01: phase 1 2'b10: phase 2 2'b11: phase 3 all of above have a 45 degree of phase shift
1	PHASE_SYNC_SEL	R/W	0	ramp phase sync sel, 0: is GPIO sync; 1: internal sync
0	PHASE_SYNC_EN	R/W	0	ramp phase sync enable

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9.6.1.43 RAMP_SS_CTRL0 Register (Offset = 6Bh) [reset = 0x00]

RAMP_SS_CTRL0 is shown in 図 9-54 and described in 表 9-50.

Return to Summary Table.

図 9-58. SS_CTRL0 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	SS_PRE_DIV_SEL	SS_MANUAL_MODE	RESERVED		SS_RDM_EN	SS_TRI_EN
R/W	R/W	R/W	R/W	R/W		R/W	R/W

表 9-50. RAMP_SS_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6	RESERVED	R/W	0	This bit is reserved
5	SS_PRE_DIV_SEL	R/W	0	select pll clock divide 2 as source clock in manual mode
4	SS_MANUAL_MODE	R/W	0	set ramp ss controller to manual mode
3-2	RESERVED	R/W	00	This bit is reserved
1	SS_RDM_EN	R/W	0	random SS enable
0	SS_TRI_EN	R/W	0	triangle SS enable

9.6.1.44 SS_CTRL1 Register (Offset = 6Ch) [reset = 0x00]

SS_CTRL1 is shown in 図 9-55 and described in 表 9-51.

Return to Summary Table.

図 9-59. SS_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED	SS_RDM_CTRL			SS_TRI_CTRL			
R/W	R/W			R/W			

表 9-51. SS_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-4	SS_RDM_CTRL	R/W	000	Add Dither
3-0	SS_TRI_CTRL	R/W	0000	triangle SS frequency and range control

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9.6.1.45 SS_CTRL2 Register (Offset = 6Dh) [reset = 0xA0]

SS_CTRL2 is shown in 図 9-56 and described in 表 9-52.

Return to Summary Table.

図 9-60. SS_CTRL2 Register

7	6	5	4	3	2	1	0
TM_FREQ_CTRL							
R/W							

表 9-52. SS_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TM_FREQ_CTRL	R/W	10100000	control ramp frequency in manual mode, F=61440000/N

9.6.1.46 SS_CTRL3 Register (Offset = 6Eh) [reset = 0x11]

SS_CTRL3 is shown in 図 9-57 and described in 表 9-53.

Return to Summary Table.

図 9-61. SS_CTRL3 Register

7	6	5	4	3	2	1	0
TM_DSTEP_CTRL				TM_USTEP_CTRL			
R/W				R/W			

表 9-53. SS_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	SS_TM_DSTEP_CTRL	R/W	0001	control triangle mode spread spectrum fall step in ramp ss manual mode
3-0	SS_TM_USTEP_CTRL	R/W	0001	control triangle mode spread spectrum rise step in ramp ss manual mode

9.6.1.47 SS_CTRL4 Register (Offset = 6Fh) [reset = 0x24]

SS_CTRL4 is shown in 図 9-58 and described in 表 9-54.

Return to Summary Table.

図 9-62. SS_CTRL4 Register

7	6	5	4	3	2	1	0
RESERVED	TM_AMP_CTRL		SS_TM_PERIOD_BOUNDRY				
R/W	R/W		R/W				

表 9-54. SS_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-5	TM_AMP_CTRL	R/W	01	control ramp amp ctrl in ramp ss manual model
4-0	SS_TM_PERIOD_BOUNDRY	R/W	00100	control triangle mode spread spectrum boundary in ramp ss manual mode

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9.6.1.48 CHAN_FAULT Register (Offset = 70h) [reset = 0x00]

CHAN_FAULT is shown in 図 9-59 and described in 表 9-55.

Return to Summary Table.

図 9-63. CHAN_FAULT Register

7	6	5	4	3	2	1	0
RESERVED				CH1_DC_1	CH2_DC_1	CH1_OC_I	CH2_OC_I
R				R	R	R	R

表 9-55. CHAN_FAULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000	This bit is reserved
3	CH1_DC_1	R	0	left channel DC fault
2	CH2_DC_1	R	0	right channel DC fault
1	CH1_OC_I	R	0	left channel over current fault
0	CH2_OC_I	R	0	right channel over current fault

9.6.1.49 GLOBAL_FAULT1 Register (Offset = 71h) [reset = 0h]

GLOBAL_FAULT1 is shown in 図 9-60 and described in 表 9-56.

Return to Summary Table.

図 9-64. GLOBAL_FAULT1 Register

7	6	5	4	3	2	1	0
OTP_CRC_ERROR	BQ_WR_ERROR	LOAD_EEPROM_ERROR	DVDD_UV_I	DVDD_OV_I	CLK_FAULT_I	PVDD_OV_I	PVDD_UV_I
R	R	R	R	R	R	R	R

表 9-56. GLOBAL_FAULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OTP_CRC_ERROR	R	0	Indicate OTP CRC check error.
6	BQ_WR_ERROR	R	0	the recent BQ is written failed
5	LOAD_EEPROM_ERROR	R	0	0: EEPROM boot load was done successfully 1: EEPROM boot load was done unsuccessfully
4-3	RESERVED	R	00	This bit is reserved
2	CLK_FAULT_I	R	0	clock fault
1	PVDD_OV_I	R	0	PVDD OV fault
0	PVDD_UV_I	R	0	PVDD UV fault

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9.6.1.50 GLOBAL_FAULT2 Register (Offset = 72h) [reset = 0h]

GLOBAL_FAULT2 is shown in 図 9-61 and described in 表 9-57.

Return to Summary Table.

図 9-65. GLOBAL_FAULT2 Register

7	6	5	4	3	2	1	0
RESERVED					CBC_FAULT_CH2_I	CBC_FAULT_CH1_I	OTSD_I
R					R	R	R

表 9-57. GLOBAL_FAULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0000	This bit is reserved
2	CBC_FAULT_CH2_I	R	0	right channel cycle by cycle over current fault
1	CBC_FAULT_CH1_I	R	0	left channel cycle by cycle over current fault
0	OTSD_I	R	0	over temperature shut down fault

9.6.1.51 WARNING Register (Offset = 73h) [reset = 0x00]

WARNING is shown in 図 9-62 and described in 表 9-58.

Return to Summary Table.

図 9-66. WARNING Register

7	6	5	4	3	2	1	0
RESERVED		CBCW_CH1_I	CBCW_CH2_I	OTW_LEVEL4_I	OTW_LEVEL3_I	OTW_LEVEL2_I	OTW_LEVEL1_I
R		R	R	R	R	R	R

表 9-58. WARNING Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0	This bit is reserved
5	CBCW_CH1_I	R	0	left channel cycle by cycle over current warning
4	CBCW_CH2_I	R	0	right channel cycle by cycle over current warning
3	OTW_LEVEL4_I	R	0	over temperature warning leve4, 146C
2	OTW_LEVEL3_I	R	0	over temperature warning leve3, 134C
1	OTW_LEVEL2_I	R	0	over temperature warning leve2, 122C
0	OTW_LEVEL1_I	R	0	over temperature warning leve1, 112C

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9.6.1.52 PIN_CONTROL1 Register (Offset = 74h) [reset = 0x00]

PIN_CONTROL1 is shown in 図 9-63 and described in 表 9-59.

Return to Summary Table.

図 9-67. PIN_CONTROL1 Register

7	6	5	4	3	2	1	0
MASK_OTSD	MASK_DVDD_UV	MASK_DVDD_OV	MASK_CLK_FAULT	RESERVED	MASK_PVDD_UV	MASK_DC	MASK_OC
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

表 9-59. PIN_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MASK_OTSD	R/W	0	mask OTSD fault report
6	MASK_DVDD_UV	R/W	0	mask DVDD UV fault report
5	MASK_DVDD_OV	R/W	0	mask DVDD OV fault report
4	MASK_CLK_FAULT	R/W	0	mask clock fault report
3	RESERVED	R	0	
2	MASK_PVDD_UV	R/W	0	mask PVDD UV fault report mask PVDD OV fault report
1	MASK_DC	R/W	0	mask DC fault report
0	MASK_OC	R/W	0	mask OC fault report

9.6.1.53 PIN_CONTROL2 Register (Offset = 75h) [reset = 0xF8]

PIN_CONTROL2 is shown in 図 9-64 and described in 表 9-60.

Return to Summary Table.

図 9-68. PIN_CONTROL2 Register

7	6	5	4	3	2	1	0
CBC_FAULT_LATCH_EN	CBC_WARN_LATCH_EN	CLKFLT_LATCH_EN	OTSD_LATCH_EN	OTW_LATCH_EN	MASK_OTW	MASK_CBCW	MASK_CBC_FAULT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

表 9-60. PIN_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CBC_FAULT_LATCH_EN	R/W	1	enable CBC fault latch
6	CBC_WARN_LATCH_EN	R/W	1	enable CBC warning latch
5	CLKFLT_LATCH_EN	R/W	1	enable clock fault latch
4	OTSD_LATCH_EN	R/W	1	enable OTSD fault latch
3	OTW_LATCH_EN	R/W	1	enable OT warning latch
2	MASK_OTW	R/W	0	mask OT warning report
1	MASK_CBCW	R/W	0	mask CBC warning report
0	MASK_CBC_FAULT	R/W	0	mask CBC fault report

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9.6.1.54 MISC_CONTROL Register (Offset = 76h) [reset = 0x00]

MISC_CONTROL is shown in 図 9-65 and described in 表 9-61.

Return to Summary Table.

図 9-69. MISC_CONTROL Register

7	6	5	4	3	2	1	0
DET_STATUS_LATCH	RESERVED		OTSD_AUTO_REC_EN	RESERVED			
R/W	R/W		R/W	R/W			

表 9-61. MISC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DET_STATUS_LATCH	R/W	0	1:latch clock detection status 0:don't latch clock detection status
6-5	RESERVED	R/W	00	This bit is reserved
4	OTSD_AUTO_REC_EN	R/W	0	OTSD auto recovery enable
3-0	RESERVED	R/W	0000	This bit is reserved

9.6.1.55 CBC_CONTROL Register (Offset = 77h) [reset = 0x00]

CBC_CONTROL is shown in 図 9-66 and described in 表 9-62.

Return to Summary Table.

図 9-70. CBC_CONTROL Register

7	6	5	4	3	2	1	0
RESERVED					CBC_EN	CBC_WARN_EN	CBC_FAULT_EN
R/W					R/W	R/W	R/W

表 9-62. CBC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	00000	This bit is reserved
2	CBC_EN	R/W	0	enable CBC function
1	CBC_WARN_EN	R/W	0	enable CBC warning
0	CBC_FAULT_EN	R/W	0	enable CBC fault

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9.6.1.56 FAULT_CLEAR Register (Offset = 78h) [reset = 0x00]

FAULT_CLEAR is shown in 図 9-67 and described in 表 9-63.

Return to Summary Table.

図 9-71. FAULT_CLEAR Register

7	6	5	4	3	2	1	0
ANALOG_FAULT_CLEAR	RESERVED						
W	R/W						

表 9-63. FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ANALOG_FAULT_CLEAR	W	0	WRITE CLEAR BIT once write this bit to 1, device clears analog fault
6-0	RESERVED	R/W	0000000	This bit is reserved

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10 Application and Implementation

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10.1 Application Information

This section details the information required to configure the device for several popular configurations and provides guidance on integrating the TAS5825P device into the larger system.

10.1.1 Bootstrap Capacitors

The output stage of the TAS5825P uses a high-side NMOS driver, rather than a PMOS driver. To generate the gate driver voltage for the high-side NMOS, a bootstrap capacitor for each output terminal acts as a floating power supply for the switching cycle. Use 0.22-µF capacitors to connect the appropriate output pin (OUT_X) to the bootstrap pin (BST_X). For example, connect a 0.22-µF capacitor between OUT_A and BST_A for bootstrapping the A channel. Similarly, connect another 0.22-µF capacitor between the OUT_B and BST_B pins for the B channel inverting output.

10.1.2 Inductor Selections

TI requires that the peak current is smaller than the OCP (Over current protection) value which is 7.5 A, there are 3 cases which cause high peak current flow through inductor.

1. During power up (idle state, no audio input), the duty cycle increases from 0 to θ.

$$I_{peak_power_up} \approx PVDD \times \sqrt{C/L} \times \sin(1/\sqrt{L \times C} \times \theta / F_{sw}) \quad (1)$$

注

θ=0.5 (BD Modulation), 0.14 (1SPW Modulation), 0.14 (Hybrid Modulation)

表 10-1. Peak Current During Power Up

PVDD	L (µH)	C (µF)	Fsw (kHz)	$I_{peak_power_up}$
24	4.7	0.68	384	6.07A
24	4.7	0.68	768	3.25A
24	10	0.68	384	3A
24	10	0.68	768	1.55A
12	4.7	0.68	384	3.32A
12	10	0.68	384	1.55A

2. During music playing, some audio burst signal (high frequency) with very hard PVDD clipping causes PWM duty cycle increase dramatically. This is the worst case and rarely happens.

$$I_{peak_clipping} \approx PVDD \times (1-\theta)/(F_{sw} \times L) \quad (2)$$

3. Peak current due to Max output power. Ignore the ripple current flow through capacitor here.

$$I_{peak_output_power} \approx \sqrt{2 \times Max_Output_Power / R_{speaker_Load}} \quad (3)$$

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Same PVDD and switching frequency, larger inductance means smaller idle current for lower power dissipation. It's suggested that inductor saturation current I_{SAT}, is larger than the amplifier peak current during power-up and play audio.

$$I_{SAT} \geq \max(I_{peak_power_up}, I_{peak_clipping}, I_{peak_output_power}) \quad (4)$$

In addition, the effective inductance at the peak current is required to be at least 80% of the inductance value in 表 10-2 to meet data sheet specifications.

表 10-2. Inductor Requirements

PVDD (V)	Switching Frequency (kHz)	Minimum Inductance (L) (µH)
≤ 12	384	4.7
> 12	384	10

For higher switching frequencies (Fsw), select the inductors with minimum inductance to be 384 kHz / Fsw × L.

10.1.3 Power Supply Decoupling

To make sure of high efficiency, low THD, and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short duration voltage spikes. These spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input must be decoupled with some good quality, low ESL, Low ESR capacitors larger than 22 µF. These capacitors bypasses low frequency noise to the ground plane. For high frequency decoupling, place 1-µF or 0.1-µF capacitors as close as possible to the PVDD pins of the device.

10.1.4 Output EMI Filtering

The TAS5825P device is often used with a low-pass filter, which is used to filter out the carrier frequency of the PWM modulated output. This filter is frequently referred to as the L-C Filter, due to the presence of an inductive element L and a capacitive element C to make up the 2-pole filter.

The L-C filter removes the carrier frequency, reducing electromagnetic emissions and smoothing the current waveform which is drawn from the power supply. The presence and size of the L-C filter is determined by several system level constraints. In some low-power use cases that have no other circuits which are sensitive to EMI, a simple ferrite bead or a ferrite bead plus a capacitor can replace the tradition large inductor and capacitor that are commonly used. In other high-power applications, large toroid inductors are required for maximum power and film capacitors can be used due to audio characteristics. Refer to the application report Class-D LC Filter Design (SLOA119) for a detailed description on the proper component selection and design of an L-C filter based upon the desired load and response.

For EMI performance and EMI Design consideration, reference to application report: TAS5825M Design Considerations for EMC.

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10.2 Typical Applications

10.2.1 2.0 (Stereo BTL) System

In the 2.0 system, two channels are presented to the amplifier via the digital input signal. These two channels are amplified and then sent to two separate speakers. In some cases, the amplified signal is further separated based upon frequency by a passive crossover network after the L-C filter. Even so, the application is considered 2.0.

10.2.2

Most commonly, the two channels are a pair of signals called a stereo pair, with one channel containing the audio for the left channel and the other channel containing the audio for the right channel. While certainly the two channels can contain any two audio channels, such as two surround channels of a multi-channel speaker system, the most popular occurrence in two channels systems is a stereo pair.

図 10-1 shows the 2.0 (Stereo BTL) system application.

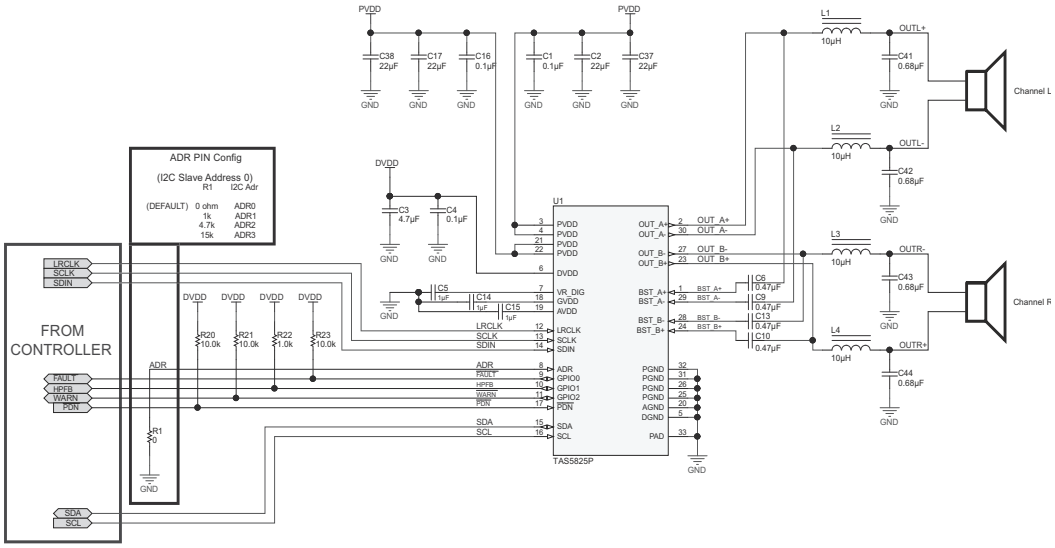


図 10-1. 2.0 (Stereo BTL) System Application Schematic

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10.2.3 Design Requirements

- Power supplies:
  - 3.3-V supply
  - 5-V to 24-V supply
- Communication: host processor serving as I^2C compliant controller
- External memory (such as EEPROM and FLASH) used for coefficients.

The requirements for the supporting components for the TAS5825P device in a Stereo 2.0 (BTL) system is provide in 表 10-3.

表 10-3. Supporting Component Requirements for Stereo 2.0 (BTL) Systems

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
C1, C16	0.1 µF	0402	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0402
C2, C17, C37, C38	22 µF	0805	CAP, CERM, 22 µF, 35 V, ±20%, JB, 0805
C3	4.7 µF	0603	CAP, CERM, 4.7 µF, 10 V, ±10%, X5R, 0603
C4	0.1 µF	0603	CAP, CERM, 0.1 µF, 16 V, ±10%, X7R, 0603
C5, C14, C15	1 µF	0603	CAP, CERM, 1 µF, 16 V, ±10%, X5R, 0603
C6, C9, C10, C13	0.47 µF	0603	CAP, CERM, 0.47 µF, 16 V, ±10%, X7R, 0603
C41, C42, C43, C44	0.68 µF	0805	CAP, CERM, 0.68 µF, 50 V, ±10%, X7R, 0805
L1, L2, L3, L4	10 µH		Inductor, Shielded, Ferrite, 10 µH, 4.4 A, 0.0304 Ω, SMD 1274AS-H-100M=P3
R1	0 Ω	0402	RES, 0, 5%, 0.063 W, 0402
R20, R21, R23	10 kΩ	0402	RES, 10.0 k, 1%, 0.063 W, 0402
R22	1 kΩ	0402	RES, 1.0 k, 1%, 0.063 W, 0402

10.2.4 Detailed Design procedures

This Design procedures can be used for both Stereo 2.0 and Mono Mode.

10.2.4.1 Step One: Hardware Integration

- Using the Typical Application Schematic as a guide, integrate the hardware into the system schematic.
- Following the recommended component placement, board layout, and routing given in the example layout above, integrate the device and the supporting components into the system PCB file.
  - The most critical sections of the circuit are the power supply inputs, the amplifier output signals, and the high-frequency signals, all of which go to the serial audio port. Constructing these signals to make sure that the signals are given precedent as design trade-offs are made is recommended.
  - For questions and support go to the E2E forums (e2e.ti.com). If deviating from the recommended layout is necessary, go to the E2E forum to request a layout review.

10.2.4.2 Step Two: Hardware Integration

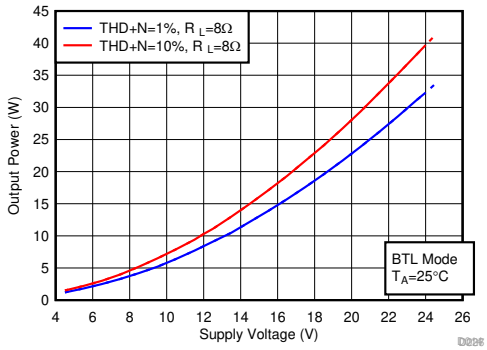
Using the TAS5825PEVM evaluation module and the PPC3 app to configure the desired device settings.

10.2.4.3 Step Three: Software Integration

- Using the End System Integration feature of the PPC3 app to generate a baseline configuration file.
- Generate additional configuration files based upon operating modes of the end-equipment and integrate static configuration information into initialization files.
- Integrate dynamic controls (such as volume controls, mute commands, and mode-based EQ curves) into the main system program.

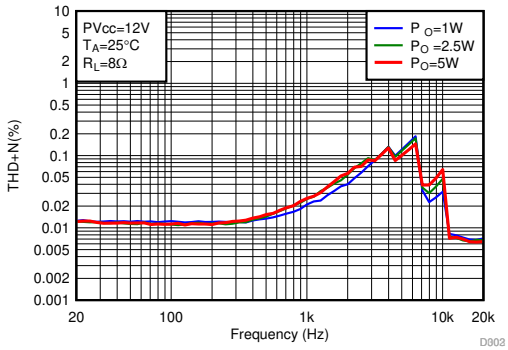
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10.2.5 Application Curves



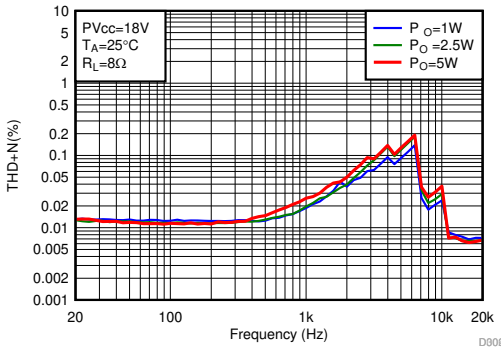
Load=8Ω Hybrid Modulation Fsw=384kHz

図 10-2. Output Power vs PVDD



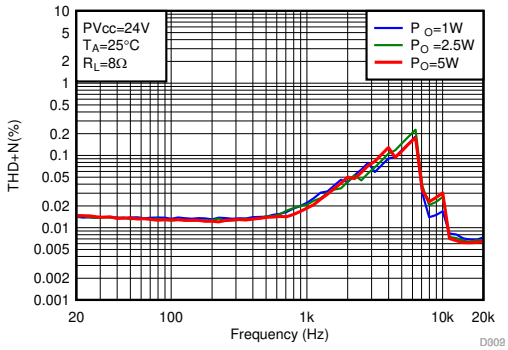
PVDD=12V Hybrid Modulation Fsw=384kHz

図 10-3. THD+N vs Frequency



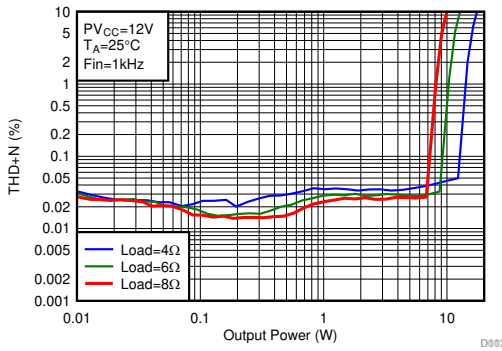
PVDD=18V Hybrid Modulation Fsw=384kHz

図 10-4. THD+N vs Frequency



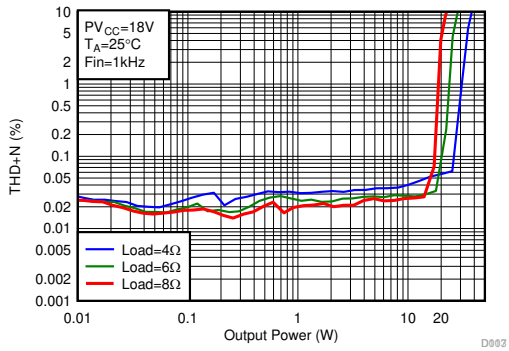
PVDD=24V Hybrid Modulation Fsw=384kHz

図 10-5. THD+N vs Frequency



PVDD=12V Hybrid Modulation Fsw=384kHz

図 10-6. THD+N vs Power



PVDD=18V Hybrid Modulation Fsw=384kHz

図 10-7. THD+N vs Power

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10.2.6 MONO (PBTL) Systems

In MONO mode, TAS5805M can be used as PBTL mode to drive sub-woofer with more output power.

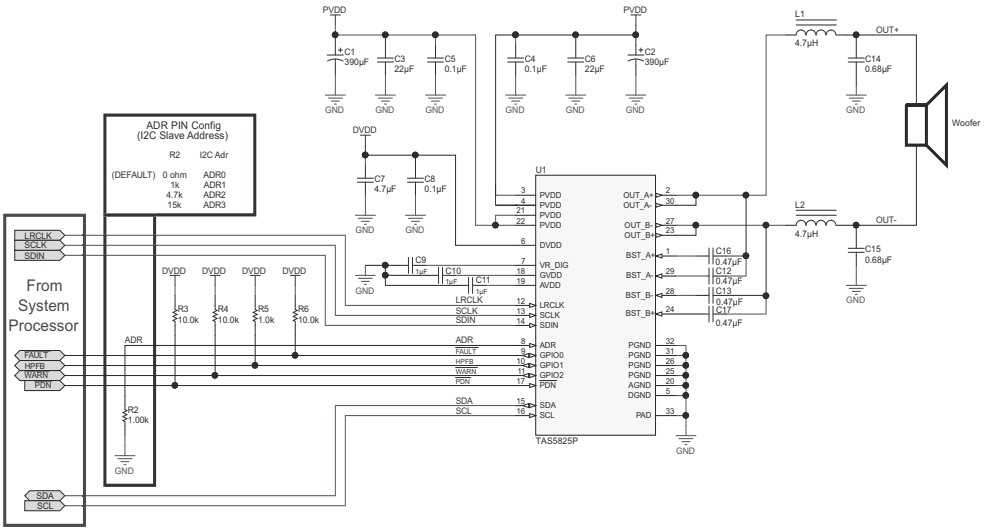


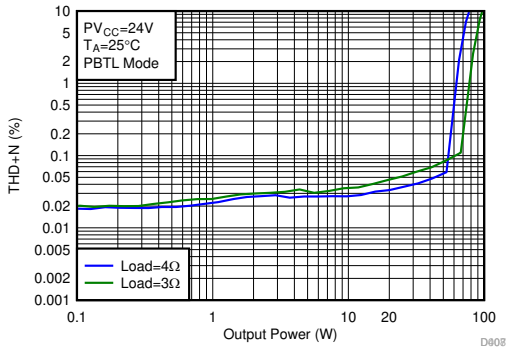
図 10-8. Sub-Woofer (PBTL) Application Schematic

表 10-4. Supporting Component Requirements for Sub-woofer (PBTL) Systems

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
C1, C2	390uF	10mmx10mm	CAP, AL, 390 µF, 35 V, +/- 20%, 0.08 ohm, SMD
C4, C5	0.1 µF	0402	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0402
C3, C6	22 µF	0805	CAP, CERM, 22 µF, 35 V, ±20%, JB, 0805
C7	4.7 µF	0603	CAP, CERM, 4.7 µF, 10 V, ±10%, X5R, 0603
C8	0.1 µF	0603	CAP, CERM, 0.1 µF, 16 V, ±10%, X7R, 0603
C9,C10,C11	1 µF	0603	CAP, CERM, 1 µF, 16 V, ±10%, X5R, 0603
C12,C13,C16,C17	0.47 µF	0603	CAP, CERM, 0.47 µF, 16 V, ±10%, X7R, 0603
C14,C15	0.68 µF	0805	CAP, CERM, 0.68 µF, 50 V, ±10%, X7R, 0805
L1,L2	4.7 µH		Inductor, Shielded, 4.7 µH, 8.7 A
R2, R5	1 kΩ	0402	RES, 1.0k, 1%, 0.063 W, 0402
R3,R4,R6	10 kΩ	0402	RES, 10.0 k, 1%, 0.063 W, 0402

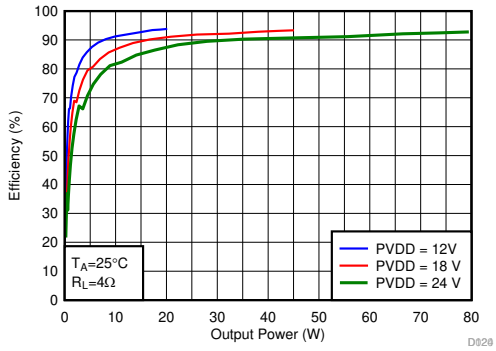
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10.2.7 Application Curves



PVDD = 18 V Hybrid Modulation Fsw = 384 kHz

図 10-9. THD+N vs Output Power



Load = 4 Ω Hybrid Modulation Fsw = 384 kHz

図 10-10. Efficiency vs Output Power

10.3 Power Supply Recommendations

The TAS5825P device requires two power supplies for proper operation. A high-voltage supply calls PVDD is required to power the output stage of the speaker amplifier and the associated circuitry. Additionally, one low-voltage power supply which is calls DVDD is required to power the various low-power portions of the device. The allowable voltage range for both PVDD and DVDD supply are listed in the *Recommended Operating Conditions* table. The two power supplies do not have a required powerup sequence. The power supplies can be powered on in any order.

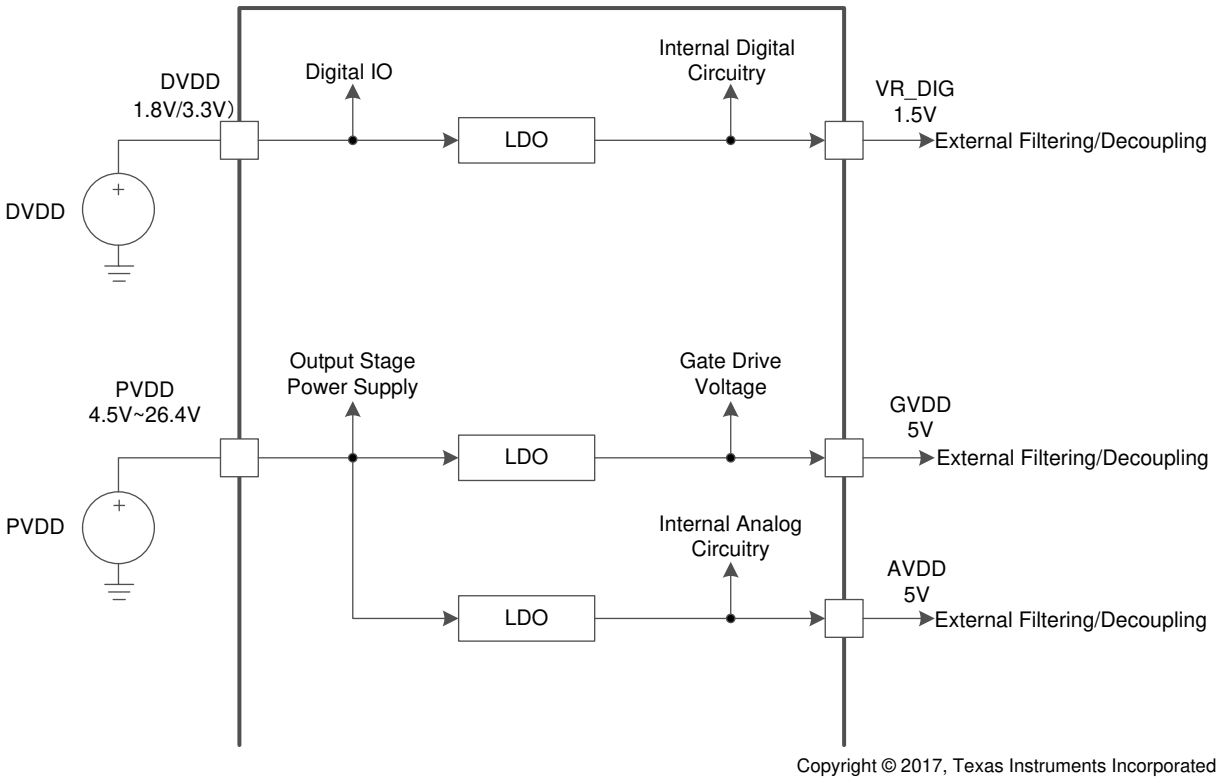


図 10-11. Power Supply Function Block Diagram

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10.3.1 DVDD Supply

The DVDD supply that is required from the system is used to power several portions of the device. As shown in 図 10-11, the DVDD supply provides power to the DVDD pin. Proper connection, routing and decoupling techniques are highlighted in *セクション 10* and *セクション 10.4.2* and must be followed as closely as possible for proper operation and performance.

Some portions of the device also require a separate power supply that is a lower voltage than the DVDD supply. To simplify the power supply requirements for the system, the TAS5825P device includes an integrated low dropout (LDO) linear regulator to create this supply. This linear regulator is internally connected to the DVDD supply and the output is presented on the DVDD_REG pin, providing a connection point for an external bypass capacitor. An important note is that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and must not be used to power any additional external circuitry. Additional loading on this pin can cause the voltage to sag, negatively affecting the performance and operation of the device.

10.3.2 PVDD Supply

The output stage of the speaker amplifier drives the load using the PVDD supply. This is the power supply which provides the drive current to the load during playback. Proper connection, routing, and decoupling techniques are highlighted in the TAS5825PEVM and must be followed as closely as possible for proper operation and performance. Due to the high-voltage switching of the output stage, TI recommends to properly decouple the output power stages in the manner described in セクション 10. Lack of proper decoupling, like that shown in *セクション 10*, results in voltage spikes which can damage the device.

A separate power supply is required to drive the gates of the MOSFETs used in the output stage of the speaker amplifier. This power supply is derived from the PVDD supply via an integrated linear regulator. A GVDD pin is provided for the attachment of decoupling capacitor for the gate drive voltage regulator. An important note is that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and must not be used to power any additional external circuitry. Additional loading on this pin can cause the voltage to sag, negatively affecting the performance and operation of the device.

Another separate power supply is derived from the PVDD supply via an integrated linear regulator is AVDD. AVDD pin is provided for the attachment of decoupling capacitor for the TAS5825P internal circuitry. An important note is that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and must not be used to power any additional external circuitry. Additional loading on this pin can cause the voltage to sag, negatively affecting the performance and operation of the device.

10.4 Layout

10.4.1 Layout Guidelines

10.4.1.1 General Guidelines for Audio Amplifiers

Audio amplifiers which incorporate switching output stages must have special attention paid to their layout and the layout of the supporting components used around them. The system level performance metrics, including thermal performance, electromagnetic compliance (EMC), device reliability, and audio performance are all affected by the device and supporting component layout.

The guidance provided in the applications section with regard to device and component selection can be followed by precise adherence to the layout guidance shown in *セクション 10.4.2*. These examples represent exemplary baseline balance of the engineering trade-offs involved with lying out the device. These designs can be modified slightly as needed to meet the needs of a given application. In some applications, for instance, solution size can be compromised to improve thermal performance through the use of additional contiguous copper neat the device. Conversely, EMI performance can be prioritized over thermal performance by routing on internal traces and incorporating a via picket-fence and additional filtering components. In all cases, TI recommends to start from the guidance shown in *セクション 10.4.2* and work with TI field application engineers or through the E2E community to modify based upon the application specific goals.

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10.4.1.2 Importance of PVDD Bypass Capacitor Placement on PVDD Network

Placing the bypassing and decoupling capacitors close to supply has long been understood in the industry. This applies to DVDD, AVDD, GVDD and PVDD. However, the capacitors on the PVDD net for the TAS5825P device deserve special attention.

The small bypass capacitors on the PVDD lines of the DUT must be placed as close to the PVDD pins as possible. Not only dose placing these device far away from the pins increase the electromagnetic interference in the system, but doing so can also negatively affect the reliability of the device. Placement of these components too far from the TAS5825P device can cause ringing on the output pins that can cause the voltage on the output pin to exceed the maximum allowable ratings shown in the *Absolute Maximum Ratings* table, damaging the deice . For that reason, the capacitors on the PVDD net must be no further away from their associated PVDD pins than what is shown in the example layouts in *セクション 10.4.2*.

10.4.1.3 Optimizing Thermal Performance

Follow the layout example shown in the 図 10-12 to achieve the best balance of solution size, thermal, audio, and electromagnetic performance. In some cases, deviation from this guidance can be required due to design constraints which cannot be avoided. In these instances, the system designer must make sure that the heat can get out of the device and into the ambient air surrounding the device. Fortunately, the heat created in the device naturally travels away from the device and into the lower temperature structures around the device.

10.4.1.3.1 Device, Copper, and Component Layout

Primarily, the goal of the PCB design is to minimize the thermal impedance in the path to those cooler structures. These tips must be followed to achieve that goal:

- Avoid placing other heat producing components or structures near the amplifier (including above or below in the end equipment).
- If possible, use a higher layer count PCB to provide more heat sinking capability for the TAS5825P device and to prevent traces and copper signal and power planes from breaking up the contiguous copper on the top and bottom layer.
- Place the TAS5825P device away from the edge of the PCB when possible to make sure that the heat can travel away from the device on all four sides.
- Avoid cutting off the flow of heat from the TAS5825P device to the surrounding areas with traces or via strings. Instead, route traces perpendicular to the device and line up vias in columns which are perpendicular to the device.
- Unless the area between two pads of a passive component is large enough to allow copper to flow in between the two pads, orient the pads so that the narrow end of the passive component is facing the TAS5825P device.
- Because the ground pins are the best conductors of heat in the package, maintain a contiguous ground plane from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible.

10.4.1.3.2 Stencil Pattern

The recommended drawings for the TAS5825P device PCB foot print and associated stencil pattern are shown at the end of this document in the package addendum. Additionally, baseline recommendations for the via arrangement under and around the device are given as a starting point for the PCB design. This guidance is designed to be an excellent choice for the majority of manufacturing capabilities in the industry and prioritizes manufacturability over all other performance criteria. In elevated ambient temperature or under high-power dissipation use-cases, this guidance can be too conservative and advanced PCB design techniques can be used to improve thermal performance of the system.

注

The customer must verify that deviation from the guidance shown in the package addendum, including the deviation explained in this section, meets the customer's quality, reliability, and manufacturability goals.

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10.4.1.3.2.1 PCB footprint and Via Arrangement

The PCB footprint (also known as a symbol or land pattern) communicates to the PCB fabrication vendor the shape and position of the copper patterns to which the TAS5825P device is soldered. This footprint can be followed directly from the guidance in the package addendum at the end of this data sheet. Making sure that the thermal pad, which connects electrically and thermally to the PowerPAD™ of the TAS5825P device, is made no smaller than what is specified in the package addendum is important. This method makes sure that the TAS5825P device has the largest interface possible to move heat from the device to the board.

The via pattern shown in the package addendum provides an improved interface to carry the heat from the device through to the layers of the PCB, because small diameter plated vias (with minimally-sized annular rings) present a low thermal-impedance path from the device into the PCB. Once into the PCB, the heat travels away from the device and into the surrounding structures and air. By increasing the number of vias, as shown in セクション 10.4.2, this interface can benefit from improved thermal performance.

注

Vias can obstruct heat flow if the vias are not constructed properly.

More notes on the construction and placement of vias are as follows:

- Remove thermal reliefs on thermal vias, because the vias impede the flow of heat through the via.
- Vias filled with thermally conductive material are best, but a simple plated via can be used to avoid the additional cost of filled vias.
- The diameter of the drill must be 8 mm or less. Also, the distance between the via barrel and the surrounding planes must be minimized to help heat flow from the via into the surrounding copper material. In all cases, minimum spacing must be determined by the voltages present on the planes surrounding the via and minimized wherever possible.
- Vias must be arranged in columns, which extend in a line radially from the heat source to the surrounding area. This arrangement is shown in セクション 10.4.2.
- Make sure that vias do not cut off power current flow from the power supply through the planes on internal layers. If needed, remove some vias that are farthest from the TAS5825P device to open up the current path to and from the device.

10.4.1.3.2.2 Solder Stencil

During the PCB assembly process, a piece of metal called a stencil on top of the PCB and deposits solder paste on the PCB wherever there is an opening (called an aperture) in the stencil. The stencil determines the quantity and the location of solder paste that is applied to the PCB in the electronic manufacturing process. In most cases, the aperture for each of the component pads is almost the same size as the pad itself. However, the thermal pad on the PCB is large and depositing a large, single deposition of solder paste can lead to manufacturing issues. Instead, the solder is applied to the board in multiple apertures, to allow the solder paste to outgas during the assembly process and reduce the risk of solder bridging under the device. This structure is called an aperture array, and is shown in セクション 10.4.2. Making sure that the total area of the aperture array (the area of all of the small apertures combined) covers between 70% and 80% of the area of the thermal pad itself is important.

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10.4.2 Layout Example

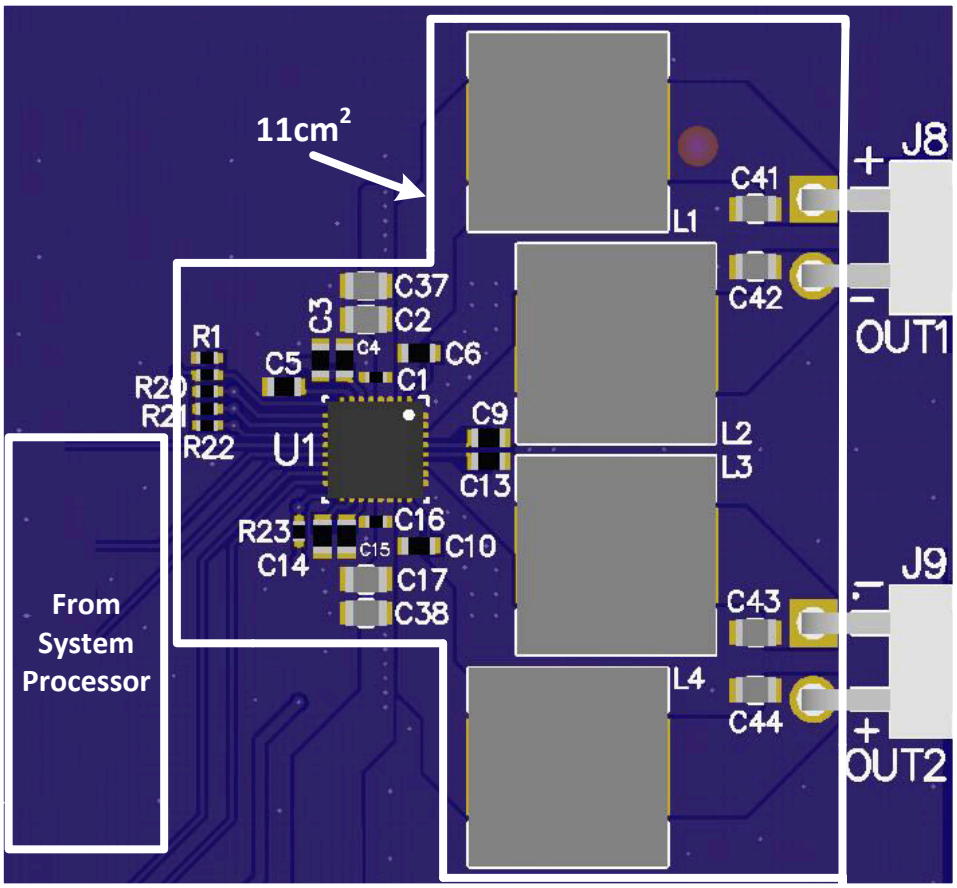


図 10-12. 2.0 (Stereo BTL) 3-D View

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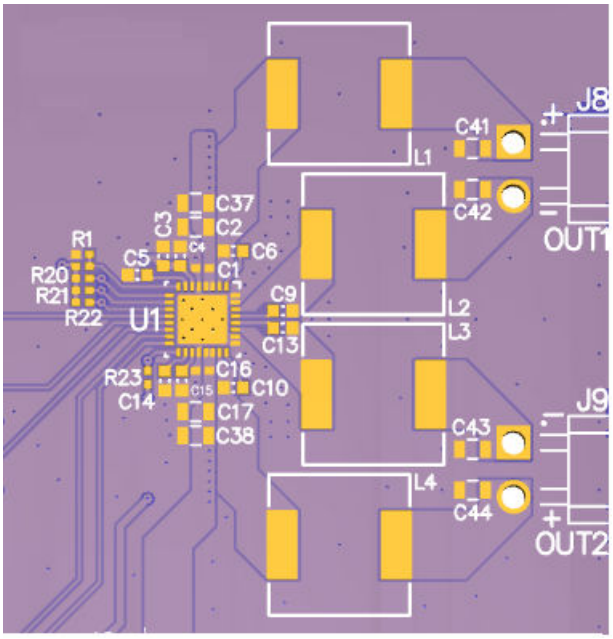


図 10-13. 2.0 (Stereo BTL) Top Copper View

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

The glossary listed in *セクション 11* is a general glossary with commonly used acronyms and words which are defined in accordance with a broad TI initiative to comply with industry standards such as JEDEC, IPC, IEEE, and others. The glossary provided in this section defines words, phrases, and acronyms that are unique to this product and documentation, collateral, or support tools and software used with this product. For any additional questions regarding definitions and terminology, please see the e2e Audio Amplifier Forum.

Bridge tied load (BTL) is an output configuration in which one terminal of the speaker is connected to one half-bridge and the other terminal is connected to another half-bridge.

DUT refers to a *device under test* to differentiate one device from another.

Closed-loop architecture describes a topology in which the amplifier monitors the output terminals, comparing the output signal to the input signal and attempts to correct for non-linearities in the output.

Dynamic controls are those which are changed during normal use by either the system or the end-user.

GPIO is a general purpose input/output pin. GPIO is a highly configurable, bi-directional digital pin which can perform many functions as required by the system.

Host processor (also known as System Processor, Scalar, Host, or System Controller) refers to device which serves as a central system controller, providing control information to devices connected as well as gathering audio source data from devices upstream and distributing to other devices. This device often configures the controls of the audio processing devices (like the TAS5825P) in the audio path to optimize the audio output of a loudspeaker based on frequency response, time alignment, target sound pressure level, safe operating area of the system, and user preference.

Maximum continuous output power refers to the maximum output power that the amplifier can continuously deliver without shutting down when operated in a 25°C ambient temperature. Testing is performed for the period of time required that their temperatures reach thermal equilibrium and are no longer increasing

Parallel bridge tied load (PBTL) is an output configuration in which one terminal of the speaker is connected to two half-bridges which have been placed in parallel and the other terminal is connected to another pair of half bridges placed in parallel

$R_{DS(on)}$ is a measure of the on-resistance of the MOSFETs used in the output stage of the amplifier.

Static controls/Static configurations are controls which do not change while the system is in normal use.

Vias are copper-plated through-hole in a PCB.

11.1.2 Development Support

For RDGUI software, please consult your local field support engineer.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

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11.4 Trademarks

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11.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

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11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAS5825PRHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	5825P
TAS5825PRHBR.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	5825P

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

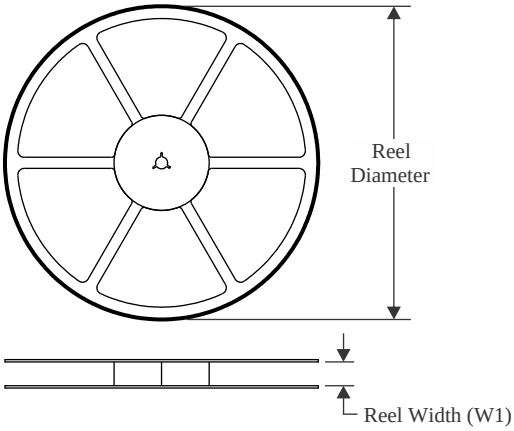
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

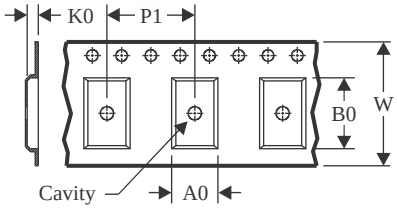
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

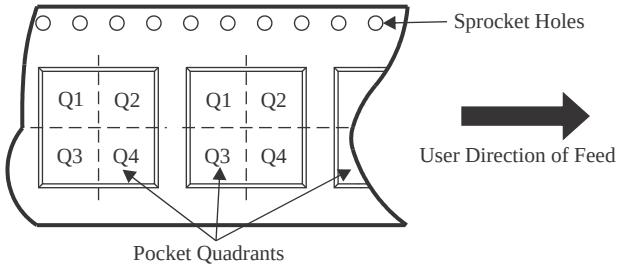


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

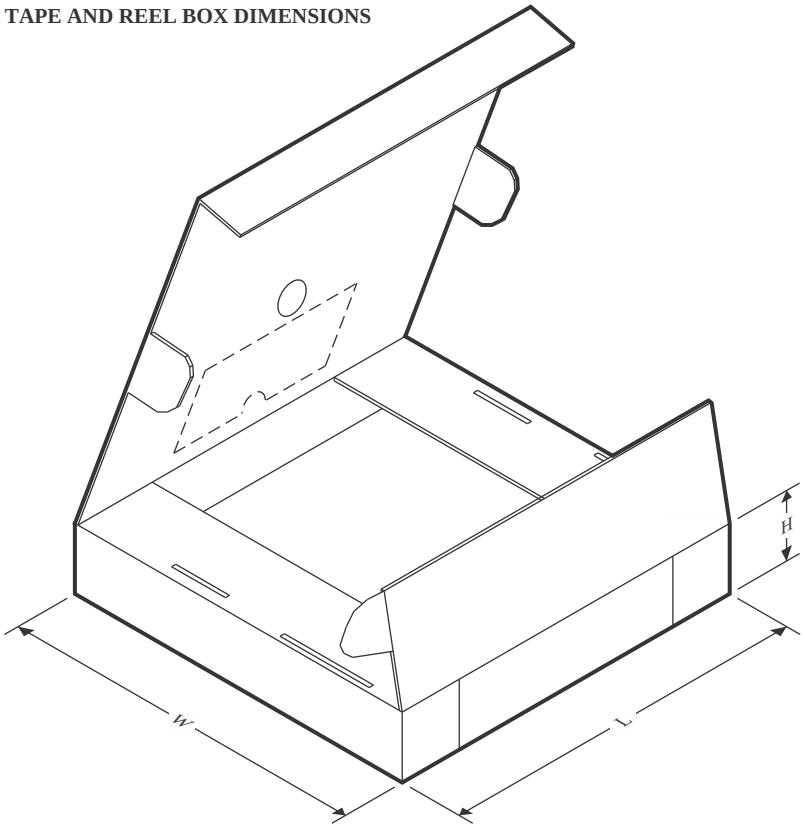
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5825PRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q2
TAS5825PRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5825PRHBR	VQFN	RHB	32	3000	356.0	356.0	36.0
TAS5825PRHBR	VQFN	RHB	32	3000	360.0	360.0	36.0

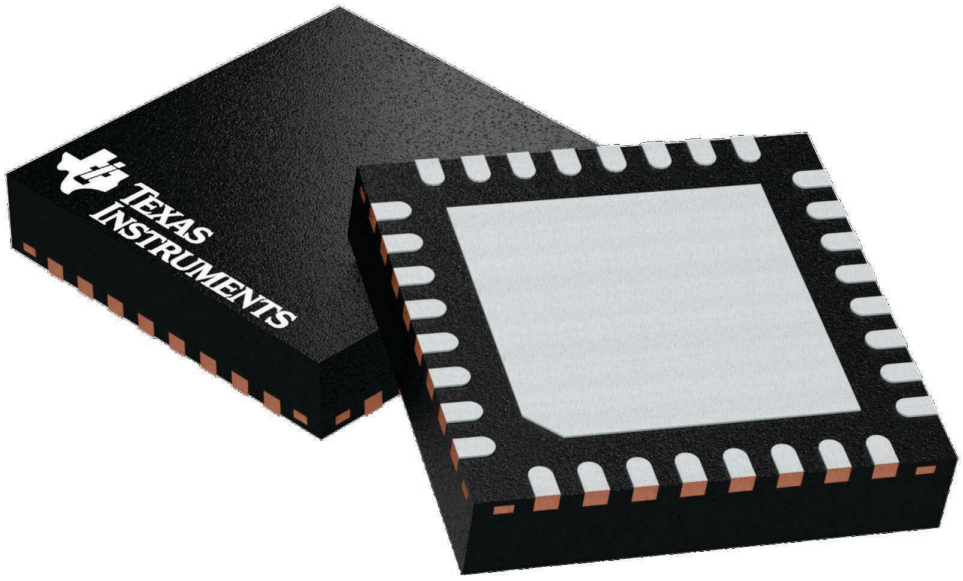
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

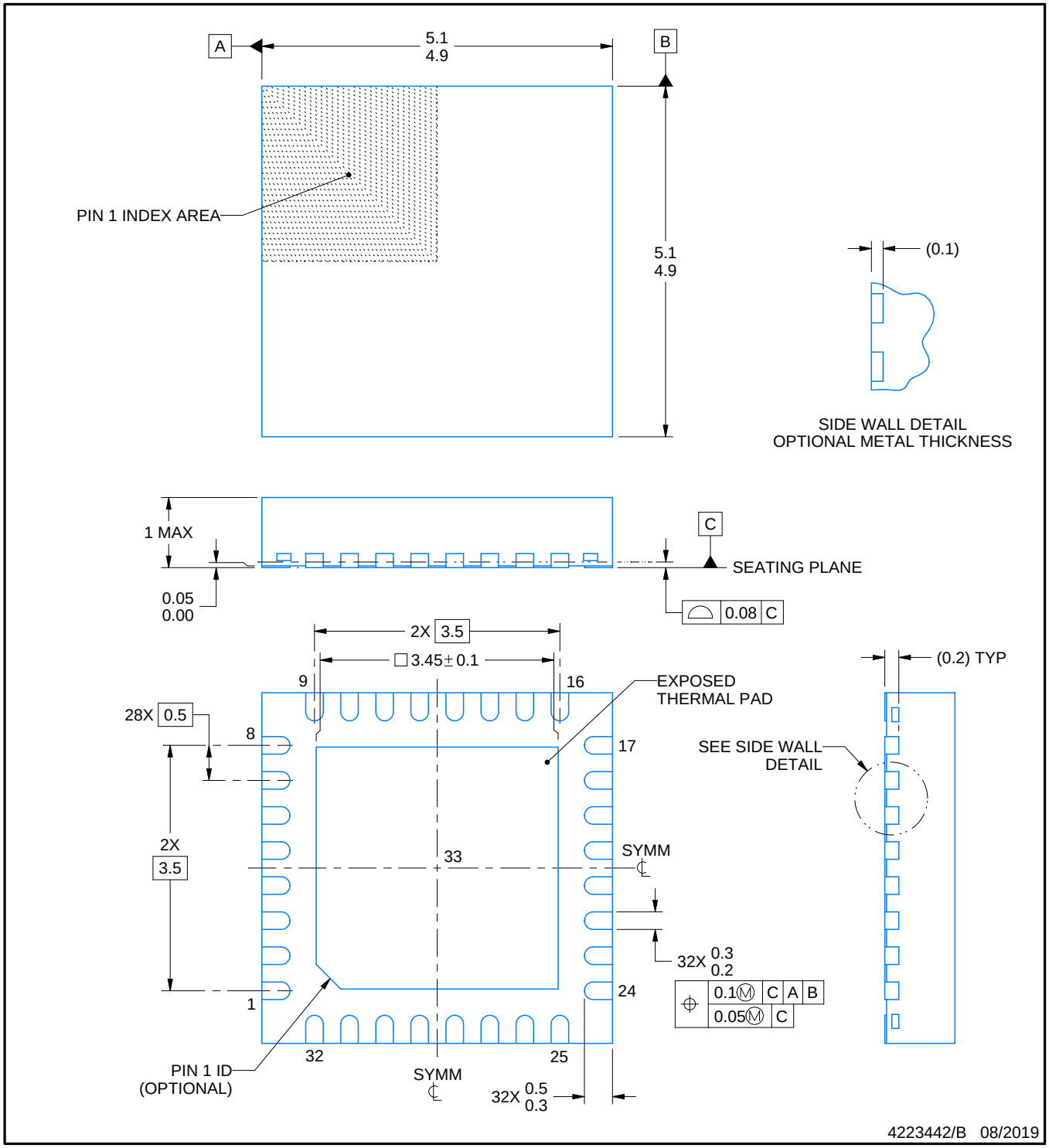
4224745/A

RHB0032E

PACKAGE OUTLINE

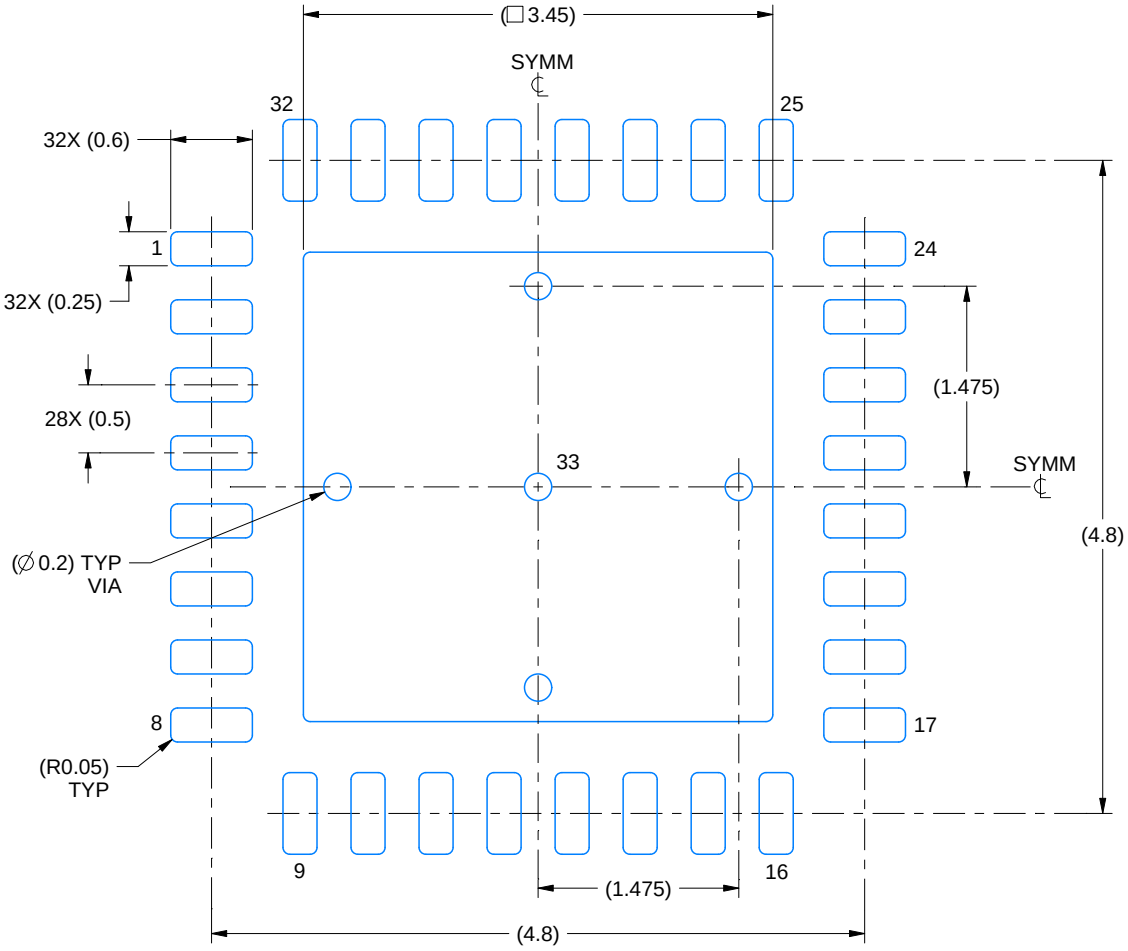
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

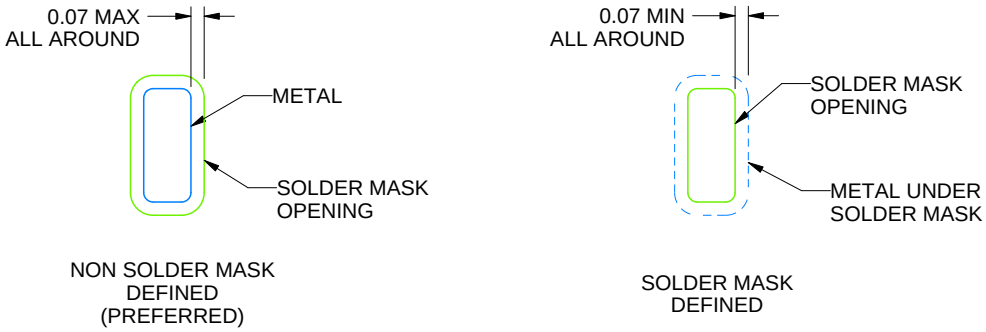


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

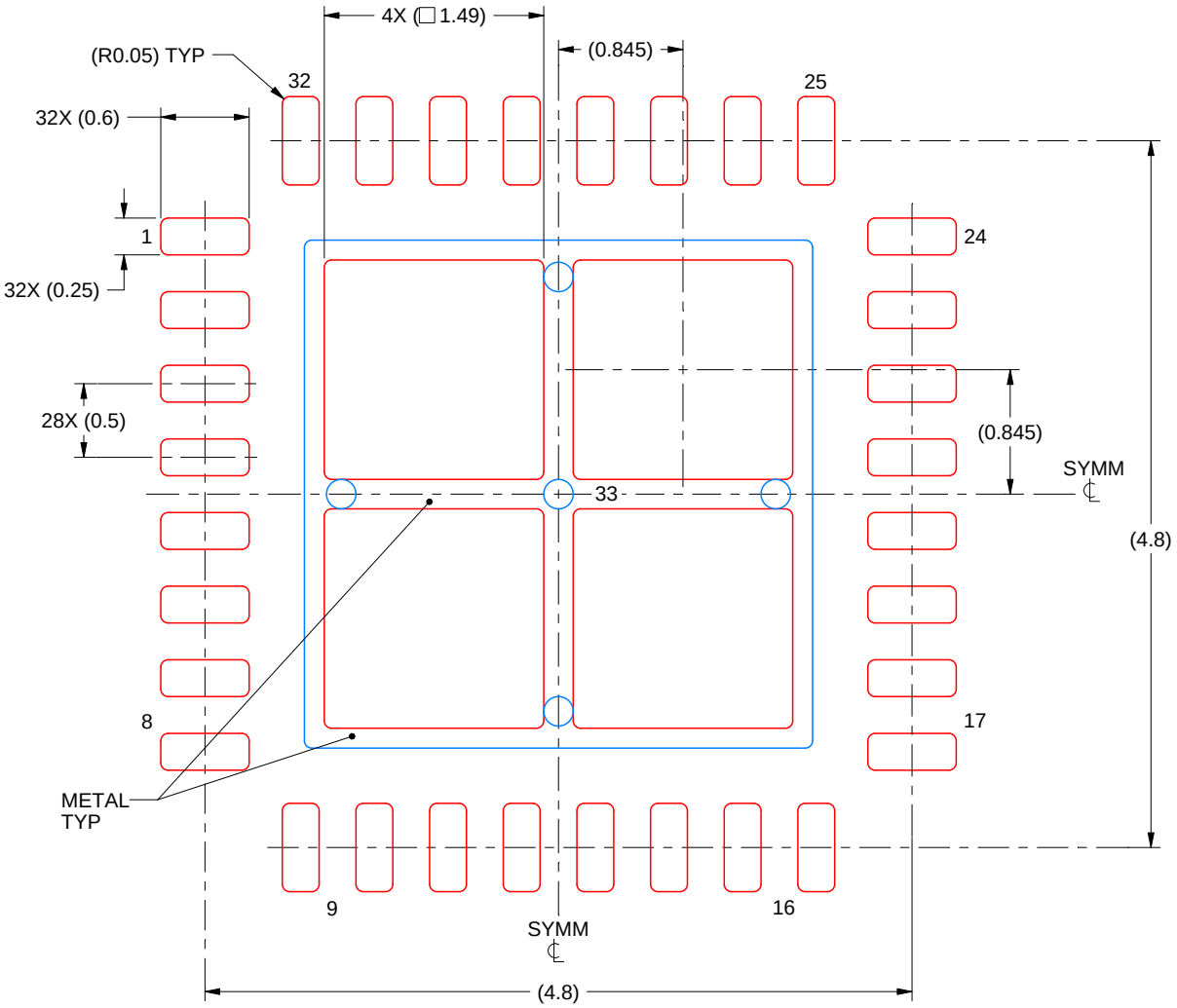


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月