TEXAS INSTRUMENTS
TCA4307
JAJSJK0B – AUGUST 2020 – REVISED NOVEMBER 2023

TCA4307 ホットスワップ可能 I²C バスおよび SMBus バッファ、スタック・バス・リカバリ付き

1 特長

- I²C バス信号の双方向データ転送をサポート
- 2.3V～5.5V の動作電源電圧範囲
- T_A 周囲空気温度範囲:-40℃～125℃
- スタック・バス回復によるバスの自動回復
- すべての SDA および SCL ラインの 1V プリチャージにより、活線挿入時の破損を防止
- Standard モードおよび Fast モードの I²C デバイスに対応
- クロックの延長、調停、同期をサポート
- 電源オフ時に高インピーダンスになる I²C ピン

2 アプリケーション

- サーバー
- エンタープライズ・スイッチング
- テレコム用スイッチング機器
- 基地局
- 産業オートメーション機器

3 概要

TCA4307 は、データおよびクロック・ラインを破損することなく、動作中のバックプレーンに I/O カードを挿入できる、ホットスワップ可能 I²C バス・バッファです。I/O カードでバスの競合が発生しないように、STOP コマンドが発行されるまで、またはバス・アイドル条件がバックプレーンで発生するまでの間、バックプレーン側の I²C ライン (in) がカード側の I²C ライン (out) に接続するのを制御回路が防止します。接続が行われると、このデバイスは双方向のバッファ処理を行い、バックプレーンとカードの容量を絶縁状態に維持します。挿入中、SDA および SCL ラインは 1V にプリチャージされ、デバイスの寄生容量を充電するのに必要な電流を最小限に抑えます。

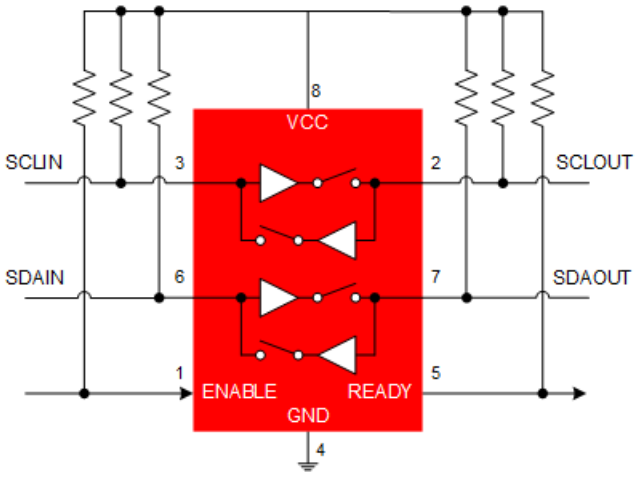
TCA4307 にはスタック・バス回復機能が備わっており、SDAOUT または SCLOUT が約 40ms にわたって Low であることを検出するとバスを自動的に切断します。バスが切断されると、本デバイスは SCLOUT に最大 16 パルスを自動的に生成し、バスを Low に保持しているデバイスをリセットしようと試みます。

I²C バスがアイドルのとき、TCA4307 は EN ピンを Low に設定することで、シャットダウン モードに移行して消費電力を低減できます。EN を High にすると、TCA4307 は通常動作を再開します。オープン・ドレインの READY 出力ピンも搭載されており、バックプレーンとカードの側が互いに接続されたことを示します。READY が High のとき、SDAIN および SCLIN は、SDAOUT および SCLOUT に接続されています。2 つの側が切断されているとき、READY は Low になります。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
TCA4307	VSSOP (DGK、8)	3mm × 4.9mm
	WSON (DRG、8)	3mm × 3mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図

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4 Pin Configuration and Functions

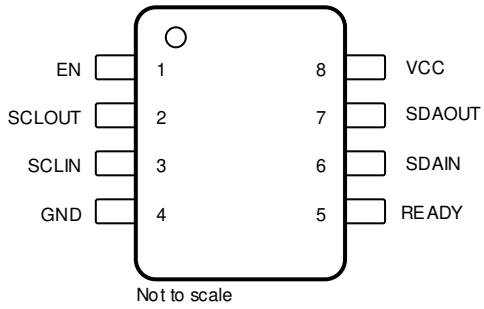


図 4-1. 8-Pin VSSOP, DGK Package (Top View)

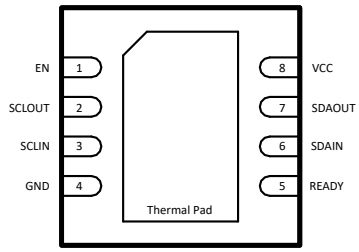


図 4-2. 8-Pin WSON, DRG Package (Top View)

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	1	I	Active-high chip enable pin. If EN is low, the TCA4307 is in a low current mode. It also disables the rise-time accelerators, disables the bus pre-charge circuitry, drives READY low, isolates SDAIN from SDAOUT and isolates SCLIN from SCLOUT. EN should be high (at VCC) for normal operation. Connect EN to VCC if this feature is not being used.
SCLOUT	2	I/O	Serial clock output. Connect this pin to the SCL bus on the card.
SCLIN	3	I/O	Serial clock input. Connect this pin to the SCL bus on the backplane.
GND	4	-	Supply ground
READY	5	O	Connection flag/rise-time accelerator control. Ready is low when either EN is low or the start-up sequence has not been completed. READY goes high when EN is high and start-up is complete. Connect a 10-kΩ resistor from this pin to V_{CC} to provide the pull-up current.
SDAIN	6	I/O	Serial data input. Connect this pin to the SDA bus on the backplane.
SDAOUT	7	I/O	Serial data output. Connect this pin to the SDA bus on the card.
VCC	8	-	Supply Power. Main input power supply from backplane. This is the supply voltage for the devices on the backplane I^2C buses. Connect pull-up resistors from SDAIN and SCLIN (and also from SDAOUT and SCLOUT) to this supply. It is recommended to place a bypass capacitor of 0.1 µF close to this pin for best results.

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Input Voltage	VCC		–0.5	7	V
	SDAIN, SCLIN, SDAOUT, SCLOUT		–0.5	7	V
	EN, READY		–0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current	SDAIN, SDAOUT, SCLIN, SCLOUT, EN, READY		±50	mA
I_{CC}	Continuous current through VCC or GND			±100	mA
T_J	Maximum junction temperature			130	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
V_I	Input voltage range	EN input	0	5.5	
V_{IO}	Input/output voltage range	SDAIN, SCLIN, SDAOUT, SCLOUT	0	5.5	
V_O	Output voltage range	READY	0	5.5	
T_A	Ambient temperature		–40	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TCA4307 DGK 8 Pin	TCA4307 DRG 8 Pin	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	177.1	58.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.5	61.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	99.6	31.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.5	2.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	97.9	31.4	°C/W

THERMAL METRIC(1)		TCA4307 DGK 8 Pin	TCA4307 DRG 8 Pin	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	14.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted). Typical specifications are at T_A = 25 °C, V_{CC} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{CC}	Supply current	VCC = 5.5V SDAIN, SCLIN = 0V SDAOUT, SCLOUT = 10k R_{PU}		2.5	4.5	mA
I_{SD}	Supply current in shutdown mode through the V_{CC} pin(1)	EN = 0 V SDAIN, SCLIN, SDAOUT, SCLOUT = 0V or V_{CC} READY pin = Hi-Z EN pulled low after bus connection event (disable precharge)		10	30	µA
UVLO	Under voltage lockout (rising)	EN = V_{CC} READY = 10 kΩ to V_{CC}		2.1		V
	Under voltage lockout (falling)			2		V
START-UP CIRCUITRY						
V_{PRE}	Pre-charge voltage	SDA, SCL = Hi-Z	0.8	1	1.2	V
RISE-TIME ACCELERATORS						
I_{PU}	RTA pull-up current(2)	Position transition on SDA, SCL $V_{SDA/SCL}$ = 0.6 V, Slew rate = 1.25 V/µs. VCC = 3.3 V	2	5		mA
INPUT-OUTPUT CONNECTION						
I_{LI}	Input pin leakage	SDA/SCL pins = 90% V_{CC}, EN = V_{CC}, GND SDA/SCL pins = 10% V_{CC}, EN = GND	-1		1	µA
V_{OS}	Input-output offset voltage (SCLIN to SCLOUT, SCLOUT to SCLIN and SDAIN to SDAOUT, SDAOUT to SDAIN	R_{PU} for SDA/SCL = 10 kΩ		60	100	mV
I_{I_RDY}	Ready pin leakage	EN = VCC, READY = V_{CC}, Bus connected	-1		1	µA
DIGITAL IO THRESHOLD						
V_{IH}	High-level input voltage	EN	0.7 × V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage	EN	0		0.3 × V_{CC}	
V_{OL}	Low-level output voltage	SDAIN, SCLIN, SDAOUT, SCLOUT I_{OL} = 4 mA V_{IN} = 0.1 V		0.15	0.4	
		READY I_{OL} = 3 mA	0		0.4	
DYNAMIC CHARACTERISTICS						

5.5 Electrical Characteristics (続き)

Over operating free-air temperature range (unless otherwise noted). Typical specifications are at T_A = 25 °C, V_{CC} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{IN\ (EN)}$	EN input capacitance	V_{EN} = 0 V or V_{CC} f = 400 kHz		1.6	4	pF
$C_{IO\ (READY)}$	READY output capacitance	V_{READY} = 0 V or V_{CC} f = 400 kHz		7	10	
$C_{IO\ (SDA/SCL)}$	SDA/SCL pin capacitance	V_{PIN} = 0 V or V_{CC} f = 400 kHz		5	10	
STUCK BUS RECOVERY						
$t_{STUCKBUS}$	Stuck bus timer		25	40	65	ms
f_{SB_SCLOUT}	Stuck bus recovery clock frequency		5.5	8.5	14	kHz
V_{OL}	Low level output during stuck bus clock output	I_{OL} = 4 mA	0		0.4	V

(1) In shutdown mode there will also be current flowing from V_{CC} through the ready pin as this pin is pulled down to indicate the bus is disconnected.
(2) Determined by design, not tested in production.

5.6 Timing Requirements

		MIN	NOM	MAX	UNIT
f_{SCL_MAX}	Maximum SCL clock frequency	400			kHz
t_{BUF} (1)	Bus free time between a STOP and START condition	1.3			µs
$t_{HD;STA}$ (1)	Hold time for a repeated START condition	0.6			µs
$t_{SU;STA}$ (1)	Set-up time for a repeated START condition	0.6			µs
$t_{SU;STO}$ (1)	Set-up time for a STOP condition	0.6			µs
$t_{HD;DAT}$ (1)	Data hold time	0			ns
$t_{SU;DAT}$ (1)	Data set-up time	100			ns
t_{LOW} (1)	LOW period of the SCL clock	1.3			µs
t_{HIGH} (1)	HIGH period of the SCL clock	0.6			µs
t_f (1)	Fall time of both SDA and SCL signals	20 × (V_{CC}/5.5 V)		300	ns
t_r (1)	Rise time of both SDA and SCL signals	20 × (V_{CC}/5.5 V)		300	ns

(1) These are system-level timing specs and are dependent upon bus capacitance and pull up resistor value. It is up to the system designer to ensure they are met

5.7 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted). Typical specifications are at T_A = 25 °C, V_{CC} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
START-UP CIRCUITRY						
$t_{PRECHARGE}$	Time from V_{CC} to precharge enabled	SDA,SCL = Hi-Z EN = V_{CC}, GND		15	60	µs
t_{EN}	Time from V_{POR} to digital being ready	VCC transition from 0V to V_{CC} Time from V_{PORR} to earliest stop bit recongized		35	95	µs

5.7 Switching Characteristics (続き)

Over operating free-air temperature range (unless otherwise noted). Typical specifications are at T_A = 25 °C, V_{CC} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{IDLE}	Bus idle time to READY active	SDA,SCL = 10 kΩ to V_{CC} EN = V_{CC} Measured at 0.5 × V_{CC}		95	150	µs
$t_{DISABLE}$	Time from EN high to low to READY low	SDA,SCL = 10 kΩ to V_{CC} READY = 10 kΩ to V_{CC} Measured at 0.5 × V_{CC}		30	200	ns
t_{STOP}	SDAIN to READY delay after stop condition	SDA,SCL = 10 kΩ to V_{CC} READY = 10 kΩ to V_{CC} Measured at 0.5 × V_{CC}		1.2	2	µs
t_{READY}	SCLOUT/SDAOUT to READY	SDA,SCL = 10 kΩ to V_{CC} READY = 10 kΩ to V_{CC} Measured at 0.5 × V_{CC}		0.8	1.5	µs
INPUT-OUTPUT CONNECTION						
t_{PLZ}	Low to high propagation delay	R_{PU} for SDA/SCL = 10 kΩ C_L = 100 pF per pin Measured at 0.5 × VCC		0	10	ns
t_{PZL}	High to low propagation delay	R_{PU} for SDA/SCL = 10 kΩ C_L = 100 pF per pin Measured at 0.5 × VCC		70	150	ns

6 Parameter Measurement Information

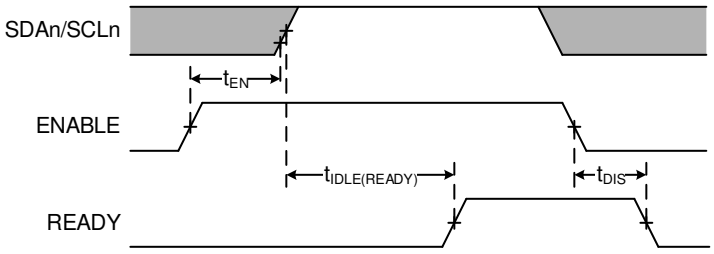


図 6-1. Timing for t_{EN}, $t_{IDLE(READY)}$, and t_{DIS}

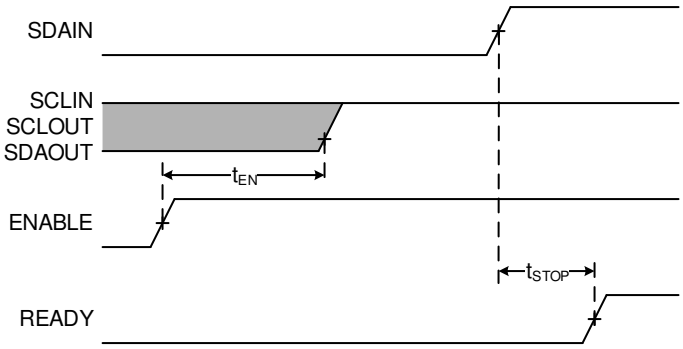


図 6-2. Timing for t_{STOP}

7 Detailed Description

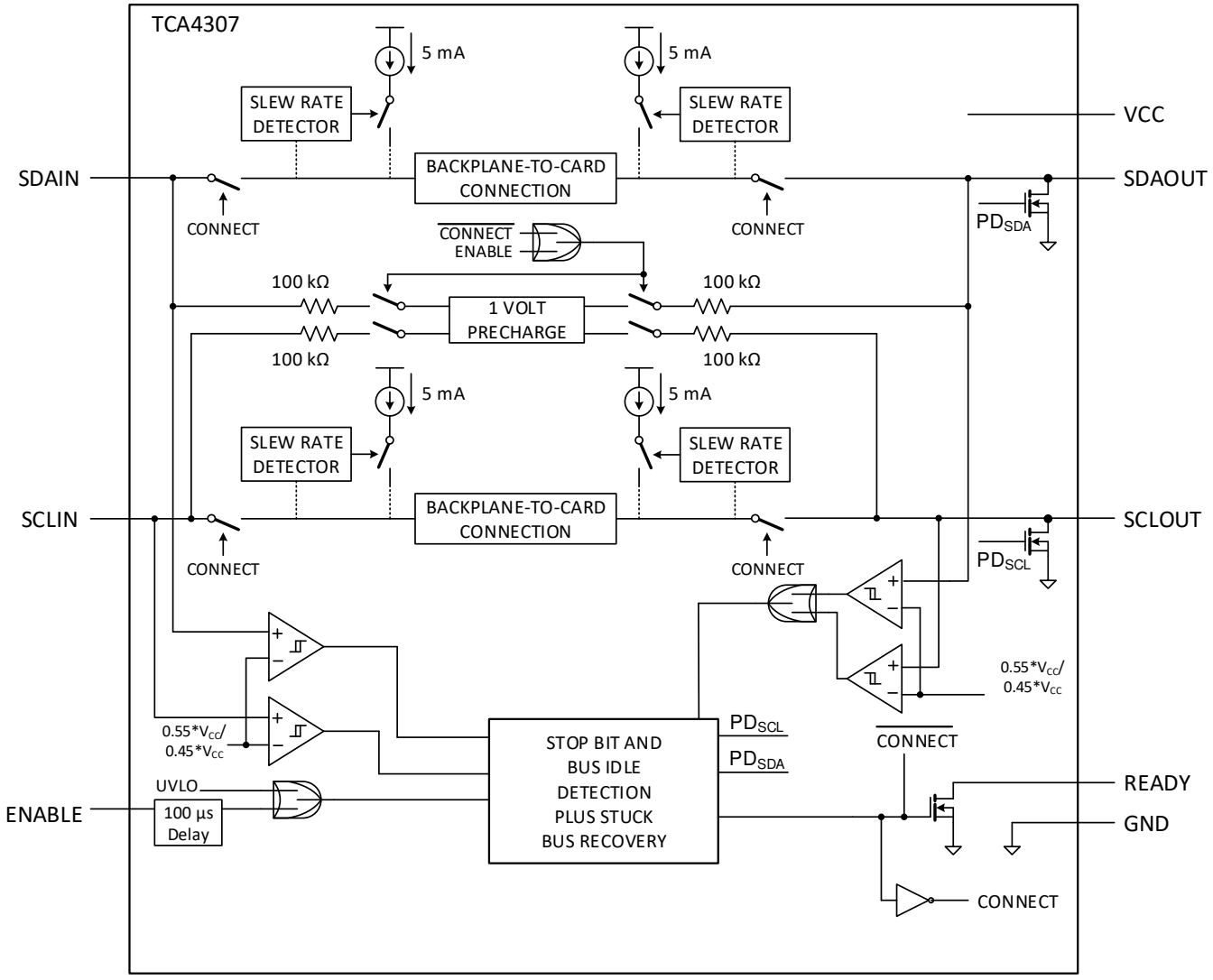
7.1 Overview

The TCA4307 is a hot-swappable I²C bus buffer that supports I/O card insertion into a live backplane without corruption of the data and clock buses. Control circuitry prevents the backplane from being connected to the card until a stop command or bus idle condition occurs on the backplane without bus contention on the card. When the connection is made, this device provides bidirectional buffering, keeping the backplane and card capacitances isolated. During insertion, the SDA and SCL lines are pre-charged to 1 V to minimize the current required to charge the parasitic capacitance of the device.

The TCA4307 has stuck bus recovery, which will automatically disconnect the bus if it detects that SDAOUT or SCLOUT are low for about 40 ms. Once the bus is disconnected, the device will automatically generate up to 16 pulses on SCLOUT to attempt to free the bus from the device which is holding it low.

When the I²C bus is idle, the TCA4307 is put into shutdown mode by setting the EN pin low. When EN is high, the TCA4307 resumes normal operation. It also includes an open drain READY output pin, which indicates that the backplane and card sides are connected together. When READY is high, the SDAIN and SCLIN are connected to SDAOUT and SCLOUT. When the two sides are disconnected, READY is low.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Hot bus insertion

During a hot bus insertion event, the TCA4307 keeps the buses disconnected to ensure that no data corruption occurs on either bus. Once the buses are idle or a stop bit on the IN side is detected, the TCA4307 connects the buses and READY goes high.

7.3.2 Pre-charge voltage

Both the SDA and SCL pins feature a 1-V pre-charge circuit through an internal 100 kΩ resistor prior to the pins being connected to an I^2C bus. This feature helps minimize disruptions as a result of a hot bus insertion event.

7.3.3 Rise time accelerators

The TCA4307 features a rise time accelerator (RTA) on all I^2C pins that during a positive bus transition, switches on a current source to quickly slew the bus pins high. This allows the use of weaker pull-up resistors, which can lower V_{OL}s and lower power system level power consumption.

7.3.4 Bus ready output indicator

The READY pin is an open drain output that provides an indicator to whether the buses are connected and ready for traffic. This pin is pulled low when the connection between IN/OUT is high impedance. Once the bus is idle or a stop condition on the IN side is detected, and the connection between IN/OUT is made, the READY pin is released and pulled high by an external pull-up resistor, signaling that it is ready for traffic.

7.3.5 Powered-off high impedance for I^2C and I/O pins

When the supply voltage is below the UVLO threshold, the I^2C and digital I/O pins are a high impedance state to prevent leakage currents from flowing through the device. When the EN pin is taken low, the device enters an isolation state, presenting a high impedance on all bus pins and pulling the READY pin low.

7.3.6 Supports clock stretching and arbitration

The TCA4307 supports full clock stretching, and arbitration without lock up.

7.3.7 Stuck bus recovery

When SDAOUT or SCLOUT is low, an internal timer is started. After the timer expires, the TCA4307 will disconnect the IN/OUT buses and then clock the SCLOUT pin in an attempt to unstick the bus, generating up to 16 clock pulses. Once the clock pulses are complete, the device will generate a stop bit and release the bus. The device will then look for the same connection requirements as described in セクション 7.4.2 before reconnecting the IN/OUT buses.

7.4 Device Functional Modes

7.4.1 Start-up and precharge

When the TCA4307 first receives power on the VCC pin, either during power-up or during live insertion, it starts in an under voltage lockout (UVLO) state, ignoring any activity on the SDA and SCL pins until V_{CC} rises above UVLO.

Once the ENABLE pin goes high, the ‘Stop Bit and Bus Idle’ detect circuit is enabled and the device enters the bus idle state.

When V_{CC} rises above UVLO, the precharge circuitry will activate, which biases the bus pins on both sides to about 1 V through an internal 100 kΩ resistor.

7.4.2 Bus idle

After the Stop Bit and Bus Idle detect circuits are enabled the device enters the bus idle state. The pre-charge circuitry becomes active and forces 1 V through 100 kΩ nominal resistors to the SCL and SDA pins. The pre-charge circuitry minimizes the voltage differential seen by the SCL/SDA pins during a hot insertion event. This minimizes the amount of disturbance seen by the I/O card.

The device waits for the SDAIN and SCLIN pins to be high for the bus idle time or a STOP condition to be observed on the IN pins. The SDAOUT and SCLOUT pins must be high and the SDAIN and SCLIN pins must meet 1 of the 2 qualifiers (idle timer or a STOP condition) before connecting SDAIN to SDAOUT and SCLIN to SCLOUT. Once the bus connections have been made, the pre-charge circuitry is disabled and the device enters the bus active state.

7.4.3 Bus active

In the bus active mode, the I^2C IN and OUT pins are connected, and the input is passed bi-directionally from IN/OUT side of the bus to the OUT/IN side respectively. The buses remain connected until the EN pin is taken low.

When the bus is connected, the driven-low side of the device is reflected on the opposite side, but with a small offset voltage. For example, if the input is pulled low to 100 mV, the output side will be pulled to roughly 160 mV. This offset allows the device to determine which side is currently being driven and avoid getting stuck low.

For the TCA4307, once a stuck bus event is detected (about 40 ms), the bus disconnects, even if EN is high.

7.4.4 Bus stuck

Once a stuck bus condition has been detected on SDAOUT or SCLOUT, the TCA4307 disconnects the bus and begins a sequence to attempt to recover the bus. First, the OUT side is disconnected from the IN side. READY will go low to signal that the bus is disconnected. Second, the TCA4307 will begin generating clocks on SCLOUT, up to 16. It will constantly monitor the state of SDAOUT to see if it has been released. Clocking will continue until 16 clocks are generated, or the SDAOUT releases. Once the SDAOUT releases, the TCA4307 will stop clocking and will generate a stop condition to terminate the recovery sequence. The last step is to go back to the bus-idle state and wait for an idle bus on both sides or a stop condition to ensure it's safe to connect the bus.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The typical application is to place the TCA4307 on the card that is being inserted or connected to a live bus, rather than being placed on the live bus. The reason for this is to provide maximum benefit by ensuring that the bus stays disconnected until an idle condition or stop condition is seen.

8.2 Typical Application

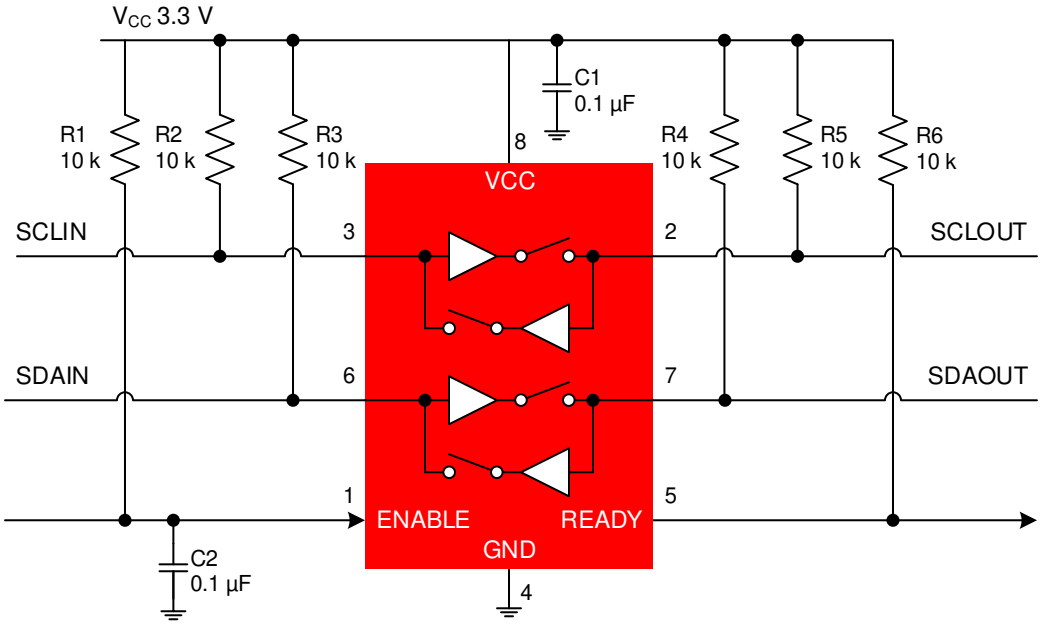


図 8-1. General Application Schematic

8.2.1 Design Requirements

8.2.1.1 Series connections

It is possible to have multiple buffers in series, but care must be taken when designing a system.

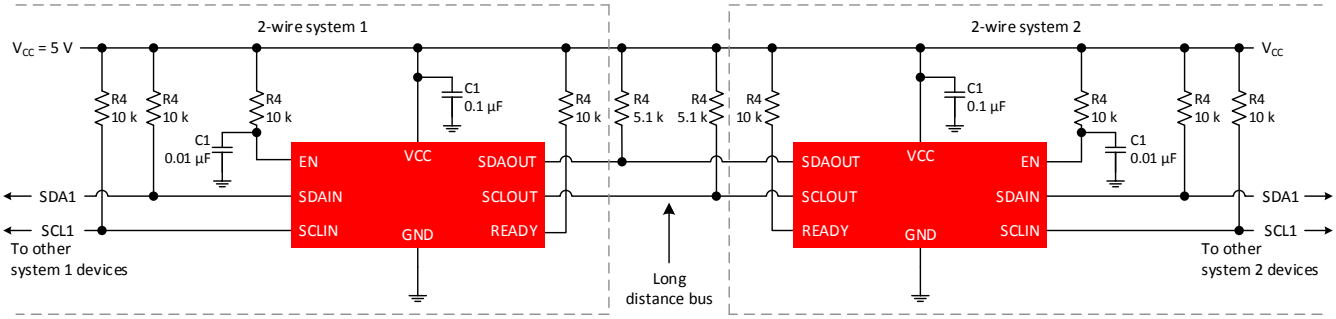


図 8-2. Series Buffer Connections

Each buffer adds approximately 60 mV of offset. Maximum offset (V_{OFFSET}) should be considered. The low level at the signal origination end is dependent upon bus load. The I^2C-bus specification requires that a 3 mA current produces no larger than a 0.4 V V_{OL}. As an example, if the V_{OL} at the controller is 0.1 V, and there are 4 buffers in series (each adding about 60 mV), then the V_{OL} at the farthest buffer is approximately 0.34 V. This device has a rise time accelerator (RTA) that activates at 0.6 V. With great care, a system with 4 buffers may work, but as the V_{OL} moves up, it may be possible to trigger the RTA, creating a false edge on the clock.

It is recommended to limit the number of buffers in series to two, and to keep the load light to minimize the offset.

Another special consideration of series connections is the effect on round-trip-delay. This is the sum of propagation delays through the buffers and any effects on rise time. It is possible that fast mode speeds (400 kHz) are not possible due to delays and bus loading.

8.2.1.2 Multiple connections to a common node

It is possible to have multiple buffers in connect to a common node, but care must be taken when designing a system.

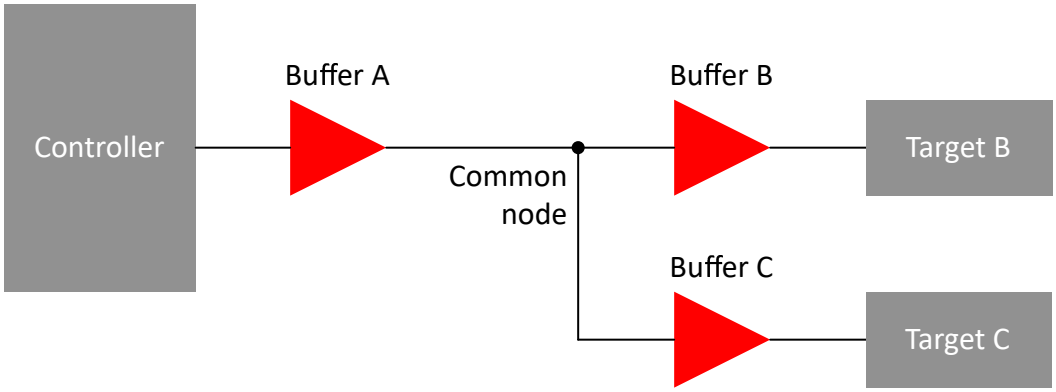


図 8-3. Connections to Common Node

It is important to try and avoid common node architectures. The multiple nodes sharing a common node can create glitches if the output voltage from a controller target device plus the offset voltage of the buffer are high enough to trip the RTA. Also keep in mind that the V_{OS} must be crossed in order for a device to begin to regulate the other side.

Consider a system with three buffers connected to a common node and communication between the Controller and Target B that are connected at either end of buffer A and buffer B in series as shown in 図 8-3. Consider if the V_{OL} at the input of buffer A is 0.3 V and the V_{OL} of Target B (when acknowledging) is 0.36 V with the direction changing from Controller and Target B and then from Taarget B to Controller. Before the direction change the user should observe V_{IL} at the input of buffer A of 0.3 V and its output, the common node, is ~0.36 V. The output of buffer B and buffer C would be ~0.42 V, but Target B is driving 0.4 V, so the voltage at Target B is 0.4 V. The output of buffer C is ~0.52 V. When the controller pull-down turns off, the input of buffer A rises and so does its output, the common node, because it is the only part driving the node. The common node rises to ~0.5 V before the buffer B output turns on, if the pull-up is strong the node may bounce. If the bounce goes above the threshold for the rising edge accelerator ~0.6 V, the accelerators on both buffer A and buffer C will fire, contending with the output of buffer B. The node on the input of buffer A goes high as will the input node of buffer C. After the common node voltage is stable for a while, the rising edge accelerators turn off, and the common node returns to ~0.5 V because the buffer B is still on. The voltage at both the Controller and Target C nodes then fall to ~0.6 V until Target B turned off. This does not cause a failure on the data line as long as the return to 0.5 V on the common node (~0.56 V at the Controller and Target C) occurred before the data setup time. If this were the SCL line, the parts on buffer A and buffer C would see a false clock rather than a stretched clock, which causes a system error.

8.2.1.3 Propagation delays

The delay for a rising edge is determined by the combined pull-up current from the bus resistors and the rise time accelerator current source and the effective capacitance on the lines. If the pull-up currents are the same, any difference in rise time is directly proportional to the difference in capacitance between the two sides. The t_{PLH} may be negative if the output capacitance is less than the input capacitance and would be positive if the output capacitance is larger than the input capacitance, when the currents are the same.

The t_{PHL} can never be negative because the output does not start to fall until the input is below 0.7 × V_{CC}, the output turn on has a non-zero delay, and the output has a limited maximum slew rate. Even if the input slew rate is slow enough that the output catches up, it would still lag the falling voltage of the input by the offset voltage. The maximum t_{PHL} occurs when the input is driven low with a very fast slew rate and the output is still limited by its turn-on delay and the falling edge slew rate.

8.2.2 Detailed Design Procedure

The system pull-up resistors must be strong enough to provide a positive slew rate of 1.25 V/µs on the SDA and SCL pins, in order to activate the boost pull-up currents during rising edges. Choose maximum resistor value using the formula given in 式 1.

$$R \leq 800 \times 10^3 \left(\frac{V_{CC\,(MIN)} - 0.6}{C} \right) \quad (1)$$

where R is the pull-up resistor value in Ω, $V_{CC(MIN)}$ is the minimum V_{CC} voltage in volts, and C is the equivalent bus capacitance in picofarads (pF).

In addition, regardless of the bus capacitance, always choose R_{PU} ≤ 65.7 kΩ for V_{CC} = 5.5 V, R_{PU} ≤ 45 kΩ for V_{CC} = 3.3 V, and R_{PU} ≤ 33 kΩ for V_{CC} = 2.5 V. The start-up circuitry requires logic HIGH voltages on SDAOUT and SCLOUT to connect the backplane to the card, and these pull-up values are needed to overcome the pre-charge voltage.

8.2.3 Application Curves

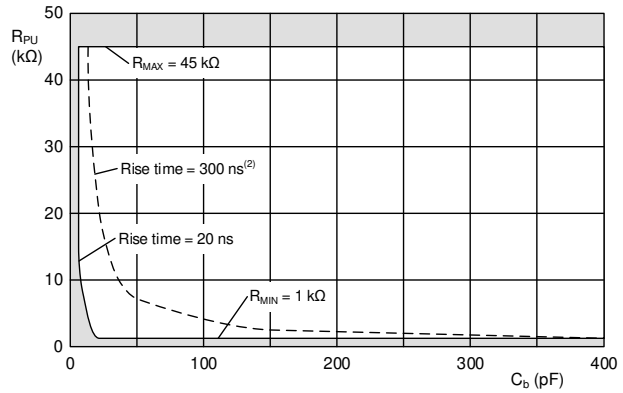


図 8-4. Example Bus Requirements for 3.3 V Systems

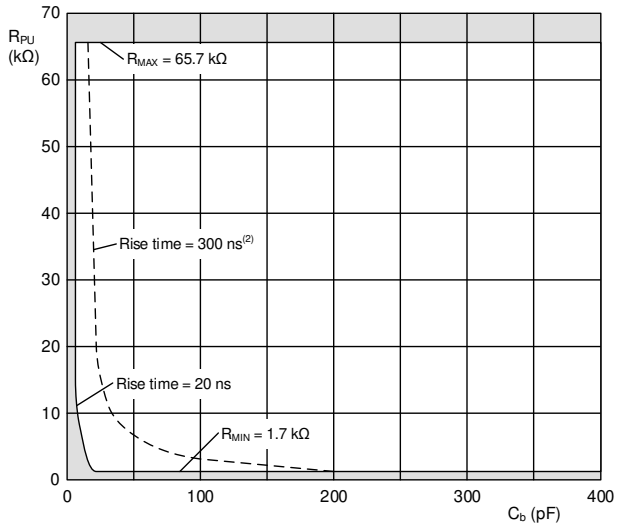


図 8-5. Example Bus Requirements for 5 V Systems

8.2.4 Typical Application on a Backplane

As shown in 図 8-6, the TCA4307 is used in a backplane connection. The TCA4307 is placed on the I/O peripheral card and connects the I^{2}C devices on the card to the backplane safely upon a hot insertion event. Note that if the I/O cards were plugged directly into the backplane, all of the backplane and card capacitances would add directly together, making rise time and fall time requirements difficult to meet. Placing a bus buffer on the edge of each card; however, isolates the card capacitance from the backplane. For a given I/O card, the TCA4307 drives the capacitance of everything on the card and the backplane must drive only the capacitance of the bus buffer, which is less than 10 pF, the connector, trace, and all additional cards on the backplane.

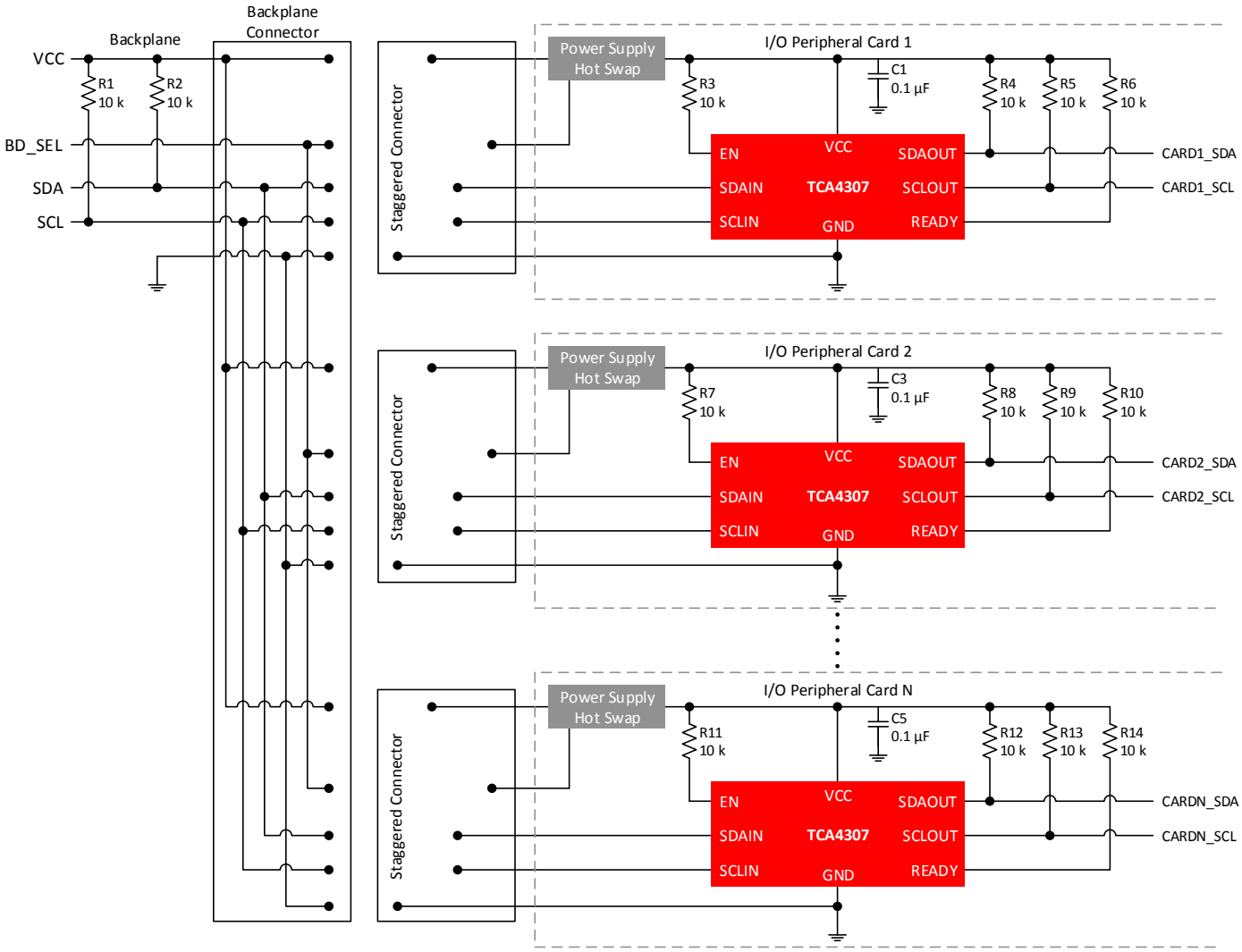


図 8-6. Backplane Application Schematic

8.2.4.1 Design Requirements

There are a few considerations when using these hot swap buffers. It is NOT recommended to place the TCA4307 on the backplane connector as it cannot isolate the cards from one another which will possibly result in disturbing on-going I^{2}C transactions. Instead, place the TCA4307 on the I/O peripheral card to maximize benefit.

8.2.4.2 Detailed Design Procedure

The design procedure is the same as outlined in セクション 8.2.2.

8.3 Power Supply Recommendations

8.3.1 Power Supply Best Practices

In order for the pre-charge circuitry to dampen the effect of hot-swap insertion of the TCA4307 into an active I^2C bus, V_{CC} must be applied before the SCL and SDA pins make contact to the main I^2C bus. This is essential when the TCA4307 is placed on the add-on card circuit board, as in セクション 8.2.4. Although the pre-charge circuitry exists on both the -IN and -OUT side, the example in セクション 8.2.4 shows SCLIN and SDAIN connecting to the main bus. The supply voltage to VCC can be applied early by ensuring that the VCC and GND pin contacts are physically longer than the contacts for the SCLIN and SDAIN pins. If a voltage supervisor is used to control the voltage supply on the add-on card, additional delay exists before the 1 V pre-charge voltage is present on the SCL and SDA pins.

8.3.2 Power-on Reset Requirements

Make sure the part starts up in the correct state. It is recommended that the power supply ramp rates meet the requirements in 表 8-1.

表 8-1. Recommended supply ramp rates

Parameter			MIN	MAX	UNIT
t_{RT}	Rise rate		0.1	1000	ms
t_{FT}	Fall rate		0.1	1000	ms

8.4 Layout

8.4.1 Layout Guidelines

For printed circuit board (PCB) layout of the TCA4307, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds. In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high frequency ripple. These capacitors should be placed as close to the TCA4307 as possible. These best practices are shown in セクション 8.4.2.

The layout example provided in セクション 8.4.2 shows a 4 layer board, which is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V_{CC} or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, shown in the セクション 8.4.2 for the VCC side of the resistor connected to the EN pin; however, this routing and via is not necessary if V_{CC} and GND are both full planes as opposed to the partial planes depicted.

8.4.2 Layout Example

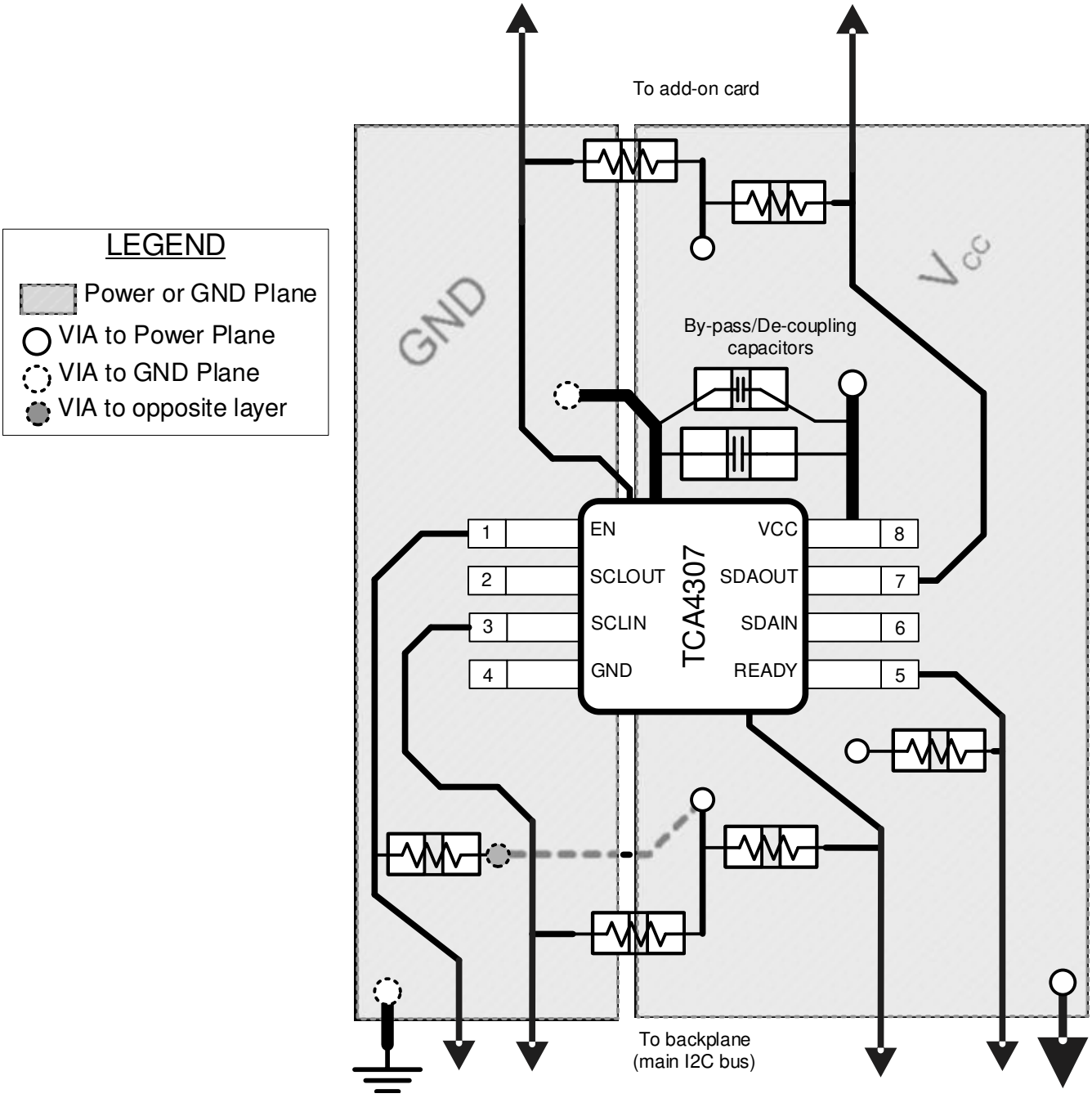


図 8-7. Layout example for TCA4307

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 サポート・リソース

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9.3 Trademarks

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9.4 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (October 2023) to Revision B (November 2023)	Page
• 「製品情報」表の DGR パッケージから製品プレビューの注を削除	1

Changes from Revision * (August 2020) to Revision A (October 2023)	Page
• I^2C に言及している場合、すべての旧式の用語をコントローラおよびターゲットに変更	1
• 「パッケージ情報」表に DRG パッケージを追加	1
• Added DRG to the *Thermal Information* table	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCA4307DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	4307
TCA4307DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4307
TCA4307DRGR	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	4307
TCA4307DRGR.A	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	4307

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

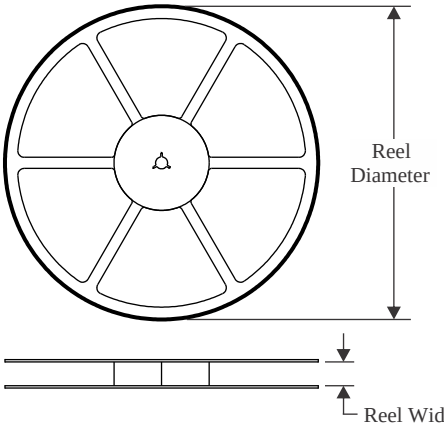
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

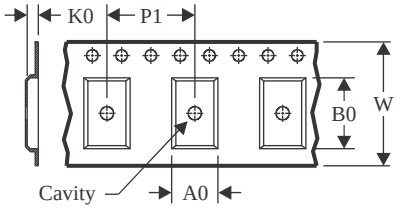
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

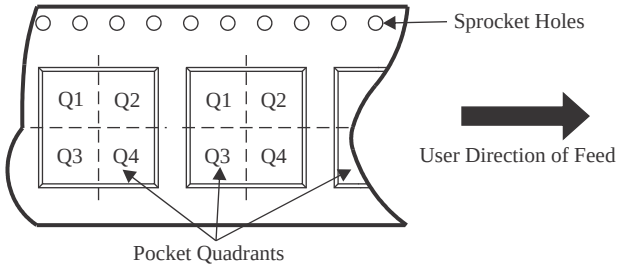


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

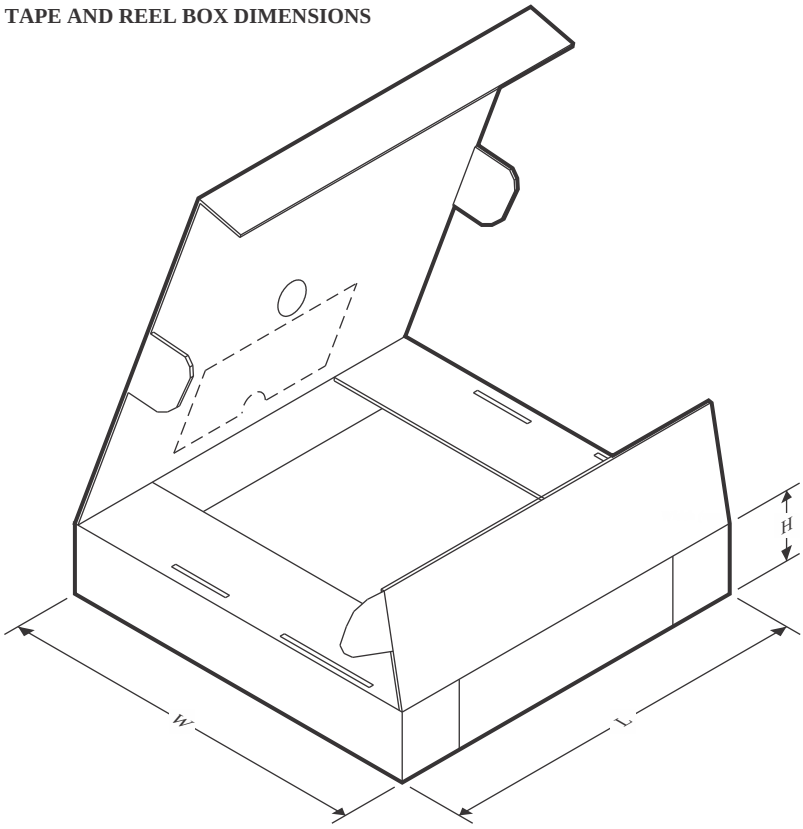
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA4307DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TCA4307DRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA4307DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TCA4307DRGR	SON	DRG	8	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

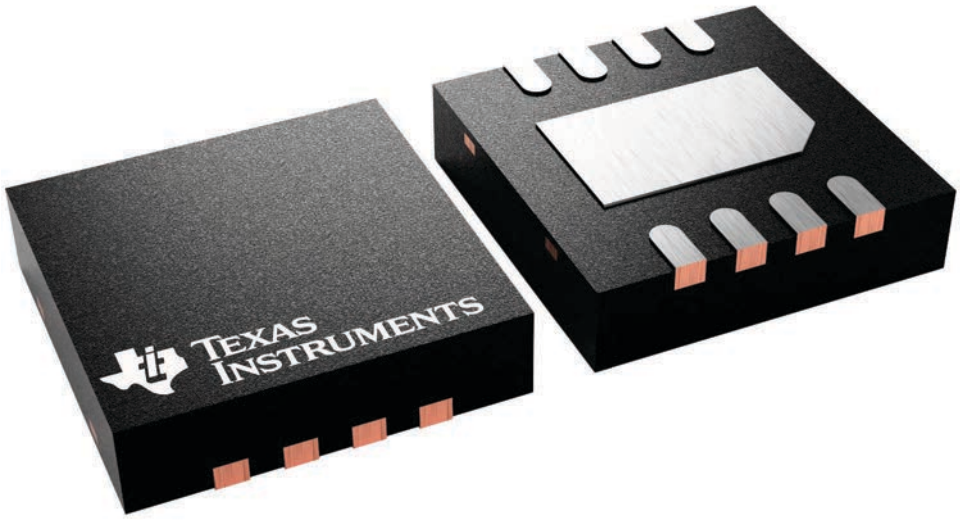
DRG 8

WSON - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



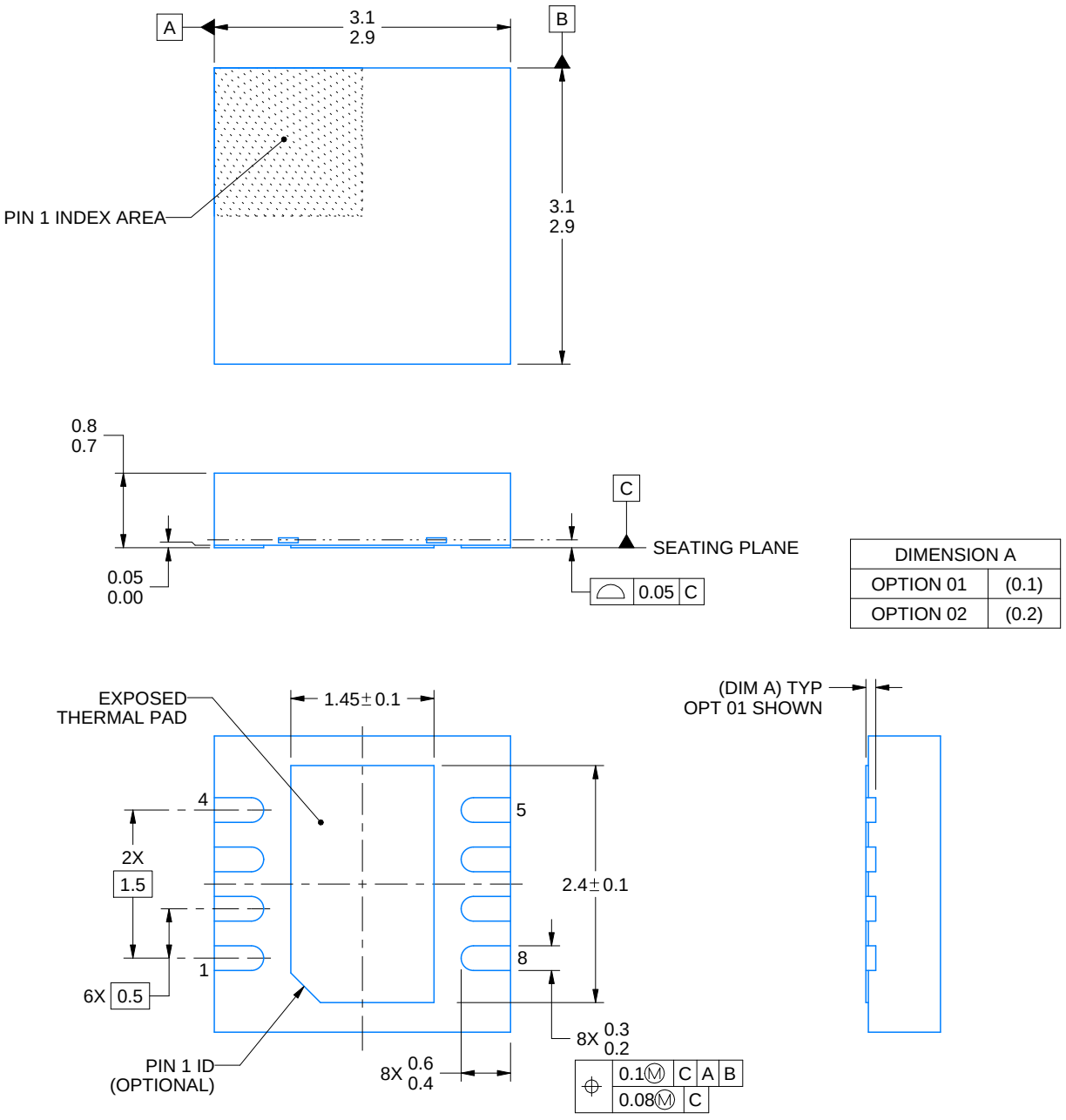
4225794/A

DRG0008B

PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

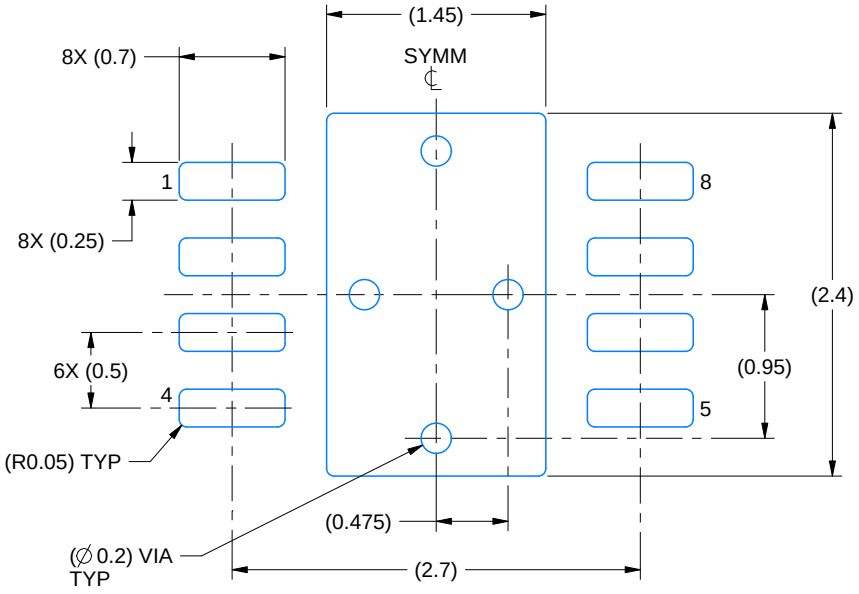


DIMENSION A	
OPTION 01	(0.1)
OPTION 02	(0.2)

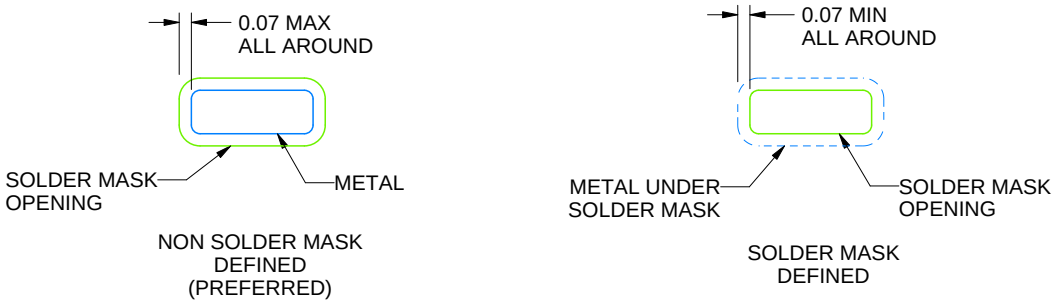
4218886/A 01/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

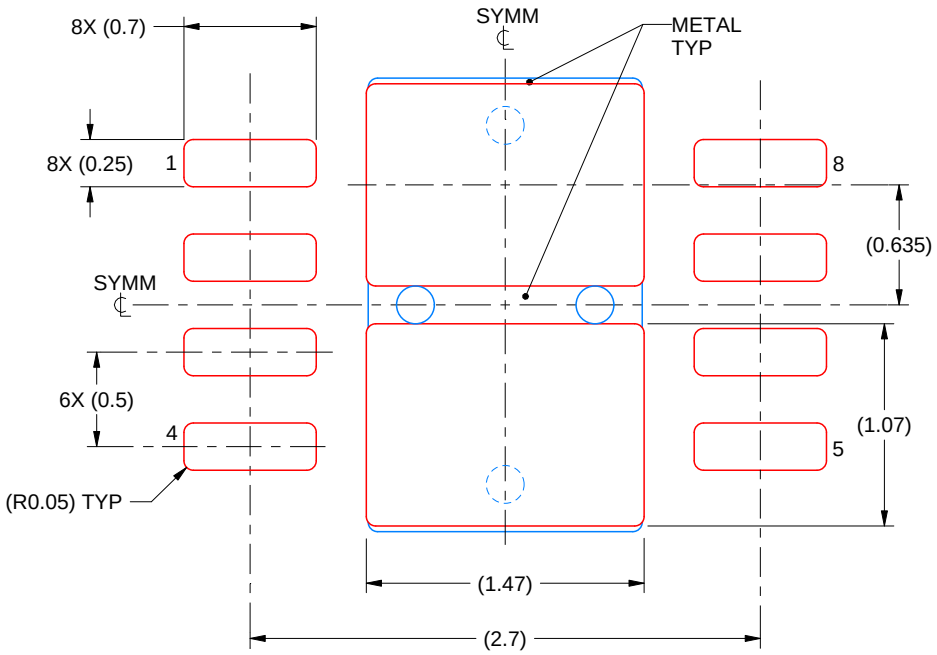


SOLDER MASK DETAILS

4218886/A 01/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218886/A 01/2020

NOTES: (continued)

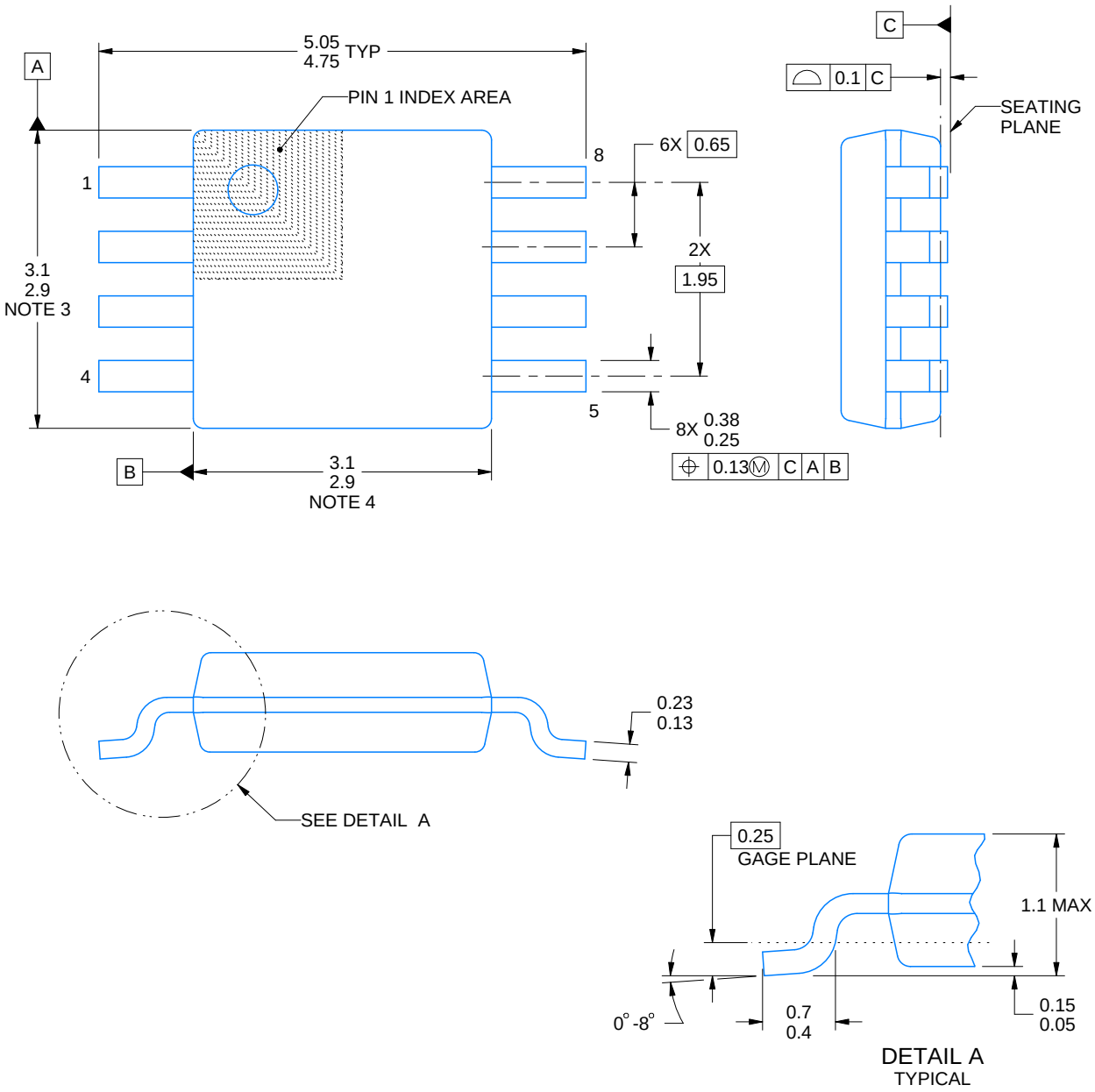
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

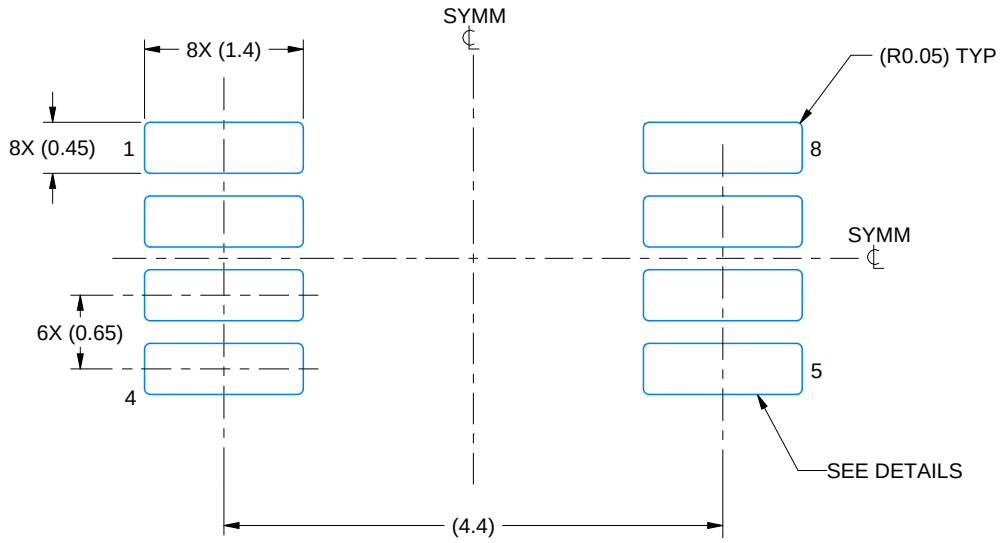
SMALL OUTLINE PACKAGE



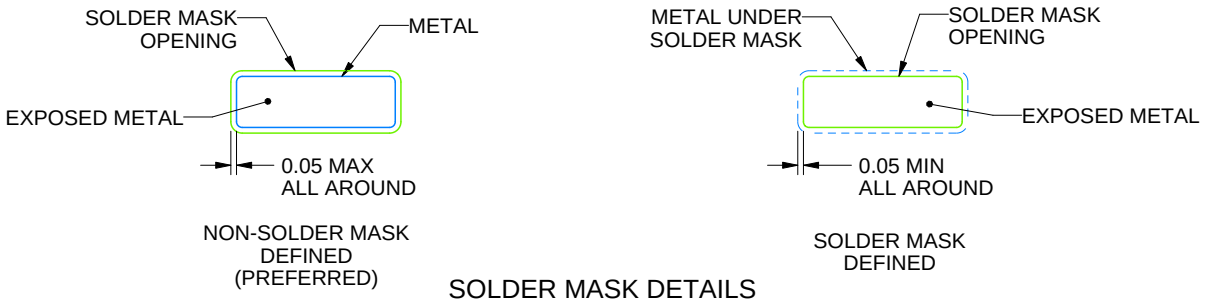
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

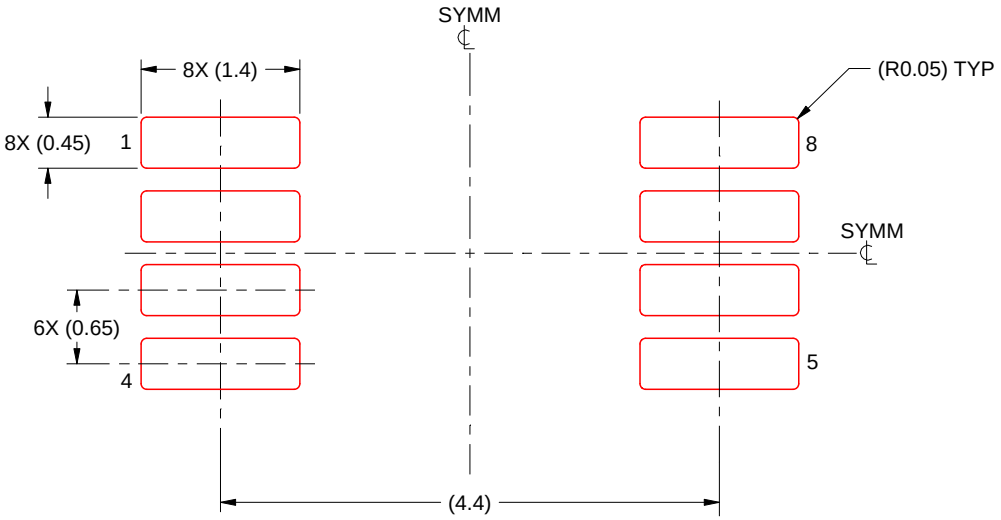


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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