TCAN1042-Q1, TCAN1042V-Q1, TCAN1042H-Q1, TCAN1042HV-Q1
TCAN1042G-Q1, TCAN1042GV-Q1, TCAN1042HG-Q1, TCAN1042HGV-Q1
JAJSH42D – FEBRUARY 2016 – REVISED OCTOBER 2021

TCAN1042-Q1 車載、フォルト保護機能搭載 CAN FD 付き CAN トランシーバ

1 特長

- AEC-Q100 (グレード 1): 車載アプリケーション認定済み
- ISO 11898-2:2016 および ISO 11898-5:2007 物理層規格に適合
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 「ターボ」CAN:
  - すべてのデバイスが Classic CAN および 2Mbps CAN FD (フレキシブル・データ・レート) をサポート、「G」オプションは 5Mbps をサポート
  - 短く対称的な伝搬遅延時間と高速なループ時間により、タイミング・マージンを強化
  - 負荷のある CAN ネットワークでより高いデータ・レートを実現
- EMC 性能: コモン・モード・チョークを使わずに SAE J2962-2 と IEC 62228-3 (最大 500kbps) をサポート
- 3.3V および 5V の MCU をサポートする I/O 電圧範囲
- 無電源時の理想的なパッシブ動作
  - バスおよびロジック端子は高インピーダンス (無負荷)
  - バスおよび RXD 出力は電源オン / 電源オフ時にグリッチ・フリーで動作
- 保護機能
  - IEC ESD 保護: 最大±15kV
  - バス・フォルト保護: ±58V (H バージョン以外) および ±70V (H バージョン)
  - V_{CC} および V_{IO} (V バージョンのみ) 電源端子の低電圧保護
  - ドライバ・ドミナント・タイムアウト (TXD DTO): データ・レート 10kbps まで対応
  - サーマル・シャットダウン保護 (TSD)
- レシーバの同相入力電圧: ±30V
- ループ遅延 (標準値): 110ns
- 接合部温度範囲: -55℃～150℃
- SOIC (8) および自動光学検査 (AOI) 機能を強化したリードレス VSON (8) パッケージ (3.0mm × 3.0mm) で供給

2 アプリケーション

- オートモーティブ / 交通システム
- すべてのデバイスが高負荷 CAN ネットワークをサポート
- 重機械 ISOBUS アプリケーション – ISO 11783
- SAE J2284 車載用高速 CAN
- GMW3122 デュアルワイヤ CAN 物理層
- SAE J2962、GIFT/ICT、ISO16845 の要件に適合

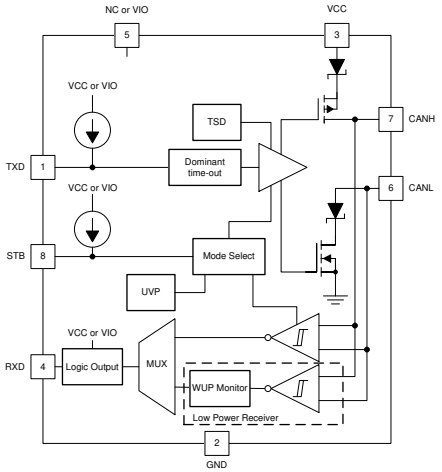
3 概要

この CAN トランシーバ・ファミリは、ISO11898-2 (2016) 高速 CAN (コントローラ・エリア・ネットワーク) の物理層規格に適合しています。すべてのデバイスが、最大 2Mbps (メガビット/秒) の CAN FD ネットワークで使用するよう設計されています。型番に「G」接尾辞が含まれているデバイスは最大 5Mbps のデータ・レート用に設計されており、「V」付きのバージョンには I/O レベル用のセカンダリ電源入力があり、入力ピンのスレッショルドと RXD 出力レベルがシフトされます。このファミリはリモート・ウェイク要求機能付きの低消費電力スタンバイ・モードを備えています。さらに、デバイスとネットワークの堅牢性の強化のため、すべてのデバイスに多くの保護機能が組み込まれています。

製品情報

部品番号	パッケージ(1)	本体サイズ
TCAN1042x-Q1	SOIC (8)	4.90mm × 3.91mm
	VSON (8)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



A. 端子 5 の機能はデバイスに依存します。「V」接尾辞なしのデバイスでは NC、「V」接尾辞ありのデバイスでは I/O レベルのシフト用の V_{IO} です。

B. RXD ロジックは、「V」接尾辞なしのデバイスでは V_{CC}、「V」接尾辞ありのデバイスでは V_{IO} に駆動されます。

機能ブロック図

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (March 2019) to Revision D (October 2021) — **Page**

- 「*特長*」に「EMC 性能：...」を追加 ... 1
- 「*特長*」に「機能安全対応」を追加 ... 1
- 車載用の特長を変更し、温度および分類レベルを削除 ... 1
- Deleted "Product Preview" from the DRB pin images in the *Pin Configurations and Functions* ... 5
- Added footnote to the GND pin in the *Pin Functions* table ... 5
- Changed the *ESD Ratings*table, added HBM and CDM classification levels ... 6
- Changed the DRB (VSON) values in the *Thermal Information* table ... 8
- Changed the title in セクション 9.3.7.1 ... 21
- Changed the title in セクション 9.3.7.2 ... 21

Changes from Revision B (May 2017) to Revision C (March 2019) — **Page**

- Changed the I_{CC} MAX value From: 180 mA To: 110 mA in the *Electrical Characteristics* ... 9
- Changed the t_{WK_FILTER} MAX value From: 1.85 µs To: 1.8 µs in the *Switching Characteristics* ... 12

Changes from Revision A (May 2016) to Revision B (May 2017) — **Page**

- 「*特長*」の「リリース済みの ISO 11898-2:2007 および ISO 11898-2:2003 物理層規格に適合」を「ISO 11898-2:2016 および ISO 11898-5:2007 物理層規格に適合」に変更 ... 1
- 「*特長*」の「2015 年 12 月 17 日ドラフト版 ISO 11898-2 物理層更新に適合」を削除 ... 1
- 「特長」の「すべてのデバイスが 2Mbps CAN FD...」を「すべてのデバイスが Classic CAN および 2Mbps CAN FD...」に変更 ... 1
- 「*特長*」に「...SOIC(8) パッケージとリードレス VSON(8) パッケージ (3.0mm x 3.0mm) で供給」を追加 ... 1
- 「アプリケーション」の「重機械 ISO11783」を「重機械 ISOBUS アプリケーション – ISO 11783」に変更 ... 1
- 「*アプリケーション*」の一覧を変更 ... 1
- 「特長」の「EMC：SAE J2962、GIFT/ICT、ISO 16845」を「SAE J2962、GIFT/ICT、ISO16845 の要件に適合」に変更 ... 1
- Added new devices to the *Device Comparison Table* ... 4
- Added Storage temperature range to the *Absolute Maximum Ratings* table ... 6
- Changed the *ESD Ratings* table to show the D(SOIC) and DRB (VSON) values ... 6

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- Changed Charged Device Model (CDM) From: ±750 To: ±1500 in the *ESD Ratings* table....6
- Changed TBD to values for the DRB (VSON) Package in the *ESD Ratings* table....6
- Added the DRB package to the *Thermal Information* table....8
- Added the *Power Rating* table....8
- Changed V_{SYM} in the *Driver Electrical Characteristics* table....9
- Changed V_{SYM_DC} in the *Driver Electrical Characteristics* table....9
- Deleted "V_I = 0.4 sin (4E6 π t) + 2.5 V" from the Test Condition of C_I in the *Receiver Electrical Characteristics* table....9
- Deleted "V_I = 0.4 sin (4E6 π t)" in the Test Condition of C_{ID} in the *Receiver Electrical Characteristics* table....9
- Added "-30 V ≤ V_{CM} ≤ +30" to the Test Condition of R_{ID} and R_{IN} in the *Receiver Electrical Characteristics* table....9
- Changed the t_{MODE} TYP value From: 1 µs To: 9 µS in the *Switching Characteristics* table....12
- Added Note 2 and Changed 表 9-2, BUS OUTPUT colum....20
- Changed *Standby Mode section*....23

Changes from Revision * (March 2016) to Revision A (May 2016) **Page**

- 「*特長*」に「リリース済みの ISO 11898-2:2007 および ISO 11898-2:2003 物理層規格に適合」を追加....1
- 「*特長*」の「ISO11898-2 (2016) の要件に適合」を「2015 年 12 月 17 日ドラフト版 ISO 11898-2 物理層更新に適合」に変更....1
- 「*アプリケーション*」の一覧を変更....1
- 「*製品情報*」表に VSON (8) ピン・パッケージを追加....1
- Added the VSON (8) pin package to the *Pin Configuration and Functions*....5
- Added $V_{(Diff)}$ to the *Absolute Maximum Ratings* table....6
- Changed OTP to TSD in the *Functional Block Diagram*....18
- Added Note 2 to 表 9-1....20
- Added Note 1 to 表 9-2....20
- Added pin number to the *Layout Example* image....31

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5 Device Comparison Table

DEVICE NUMBER	BUS FAULT PROTECTION	5-Mbps FLEXIBLE DATA RATE	3-V LEVEL SHIFTER INTEGRATED	PIN 8 MODE SELECTION
TCAN1042-Q1 (Base)	±58 V			Low Power Standby Mode with Remote Wake
TCAN1042G-Q1	±58 V	X		
TCAN1042GV-Q1	±58 V	X	X	
TCAN1042V-Q1	±58 V		X	
TCAN1042H-Q1	±70 V			
TCAN1042HG-Q1	±70 V	X		
TCAN1042HGV-Q1	±70 V	X	X	
TCAN1042HV-Q1	±70 V		X	

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6 Pin Configurations and Functions

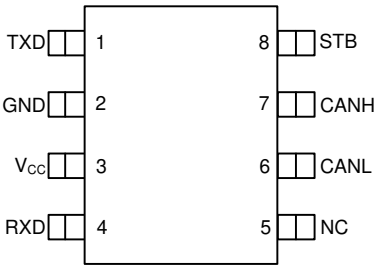


図 6-1. D Package for Base, (H), (G) and (HG) Devices8 PIN (SOIC) Top View

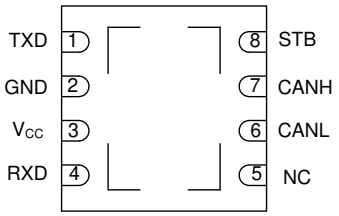


図 6-2. DRB Package for Base, (H), (G) and (HG) Devices 8 PIN (VSON) Top View

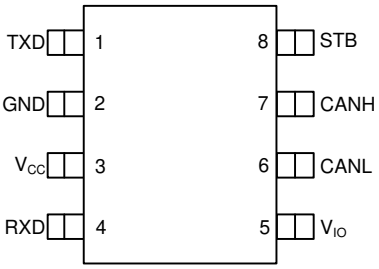


図 6-3. D Package for (V), (HV), (GV), and (HGV) Devices 8 PIN (SOIC) Top View

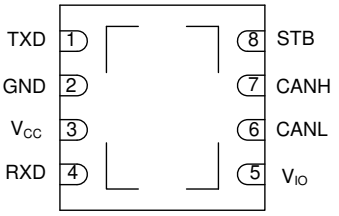


図 6-4. DRB Package for (V), (HV), (GV), and (HGV) Devices 8 PIN (VSON) Top View

表 6-1. Pin Functions

PINS			TYPE	DESCRIPTION
NAME	Base, (H), (G), (HG)	(V), (GV), (HV), (HGV)		
TXD	1	1	DIGITAL INPUT	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
GND(1)	2	2	GND	Ground connection
VCC	3	3	POWER	Transceiver 5-V supply voltage
RXD	4	4	DIGITAL OUTPUT	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
NC	5	—	—	No Connect
V_{IO}	—	5	POWER	Transceiver I/O level shifting supply voltage (Devices with "V" suffix only)
CANL	6	6	BUS I/O	Low level CAN bus input/output line
CANH	7	7	BUS I/O	High level CAN bus input/output line
STB	8	8	DIGITAL INPUT	Standby Mode control input (active high)

(1) For DRB (VSON) package options, the thermal pad may be connected to GND in order to optimize the thermal characteristics of the package.

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7 Specifications

over operating free-air temperature range (unless otherwise noted) (1) (2)

7.1 Absolute Maximum Ratings

			MIN	MAX	UNIT
V_{CC}	5-V bus supply voltage range		–0.3	7	V
V_{IO}	I/O Level Shifting Voltage Range	Devices with the "V" suffix	–0.3	7	V
V_{BUS}	CAN Bus I/O voltage range (CANH, CANL)	Devices without the "H" suffix	–58	58	V
$V_{(Diff)}$	Max differential voltage between CANH and CANL	Devices without the “H” suffix	–58	58	V
V_{BUS}	CAN Bus I/O voltage range (CANH, CANL)	Devices with the "H" suffix	–70	70	V
$V_{(Diff)}$	Max differential voltage between CANH and CANL	Devices with the “H” suffix	–70	70	V
$V_{(Logic_Input)}$	Logic input terminal voltage range (TXD, STB)		–0.3	7 and $V_I \le V_{IO} + 0.3$	V
$V_{(Logic_Output)}$	Logic output terminal voltage range (RXD)		–0.3	7 and $V_I \le V_{IO} + 0.3$	V
$I_{O(RXD)}$	RXD (Receiver) output current		–8	8	mA
T_J	Virtual junction temperature range (see *Thermal Information*)		–55	150	°C
T_{STG}	Storage temperature range (see *Thermal Information*)		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

7.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	HBM classification level 3A for all pins	±6000	V
			HBM classification level 3B for global pins CANH and CANL with respect to GND	±16000	V
		Charged-device model (CDM), per AEC Q100-011 CDM classification level C6 for all pins		±1500	V
		Machine Model (MM), in accordance to JEDEC Standard 22, Test Method A115		±200	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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7.3 ESD Ratings, Specifications

	TEST CONDITIONS		VALUE	UNIT
D (SOIC) Package				
System Level Electro-Static Discharge (ESD)	CAN bus terminals (CANH, CANL) to GND	SAE J2962-2 per ISO 10605: Powered Air Discharge	±15000	V
		SAE J2962-2 per ISO 10605: Powered Contact Discharge	±8000	
System Level Electro-Static Discharge (ESD)	CAN bus terminals (CANH, CANL) to GND	IEC 61000-4-2: Unpowered Contact Discharge	±15000	V
		IEC 61000-4-2: Powered on Contact Discharge	±8000	
System Level Electrical fast transient (EFT)	CAN bus terminals (CANH, CANL) to GND	IEC 61000-4-4: Criteria A	±4000	V
ISO7637-2 Transients according to GIFT - ICT CAN EMC test specification(1)	CAN bus terminals (CANH, CANL) to GND	Pulse 1	–100	V
		Pulse 2	+75	
		Pulse 3a	–150	
		Pulse 3b	+100	
ISO7637-3 Transients	CAN bus terminals (CANH, CANL) to GND	Direct Coupling Capacitor "Slow Transient Pulse" with 100 nF coupling capacitor - Powered	±85	
DRB (VSON) Package				
System Level Electro-Static Discharge (ESD)	CAN bus terminals (CANH, CANL) to GND	SAE J2962-2 per ISO 10605: Powered Air Discharge	±15000	V
		SAE J2962-2 per ISO 10605: Powered Contact Discharge	±8000	
System Level Electro-Static Discharge (ESD)	CAN bus terminals (CANH, CANL) to GND	IEC 61000-4-2: Unpowered Contact Discharge	±14000	V
		IEC 61000-4-2: Powered on Contact Discharge	±8000	
System Level Electrical fast transient (EFT)	CAN bus terminals (CANH, CANL) to GND	IEC 61000-4-4: Criteria A	±4000	V
ISO7637-2 Transients according to GIFT - ICT CAN EMC test specification(1)	CAN bus terminals (CANH, CANL) to GND	Pulse 1	–100	V
		Pulse 2	+75	
		Pulse 3a	–150	
		Pulse 3b	+100	
ISO7637-3 Transients	CAN bus terminals (CANH, CANL) to GND	Direct Coupling Capacitor "Slow Transient Pulse" with 100 nF coupling capacitor - Powered	±85	

(1) ISO7637 is a system level transient test. Results given here are specific to the GIFT-ICT CAN EMC Test specification conditions. Different system level configurations may lead to different results.

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7.4 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	5-V Bus Supply Voltage Range	4.5	5.5	V
V_{IO}	I/O Level-Shifting Voltage Range	3	5.5	
$I_{OH(RXD)}$	RXD terminal HIGH level output current	–2		mA
$I_{OL(RXD)}$	RXD terminal LOW level output current		2	

7.5 Thermal Information

Thermal Metric[1]		TEST CONDITIONS	TCAN1042-Q1		UNIT
			D (SOIC)	DRB (VSON)	
			8 Pins	8 Pins	
$R_{\theta JA}$	Junction-to-air thermal resistance	High-K thermal resistance[2]	105.8	48.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance[3]		46.8	17.2	°C/W
$R_{\theta JC(TOP)}$	Junction-to-case (top) thermal resistance[4]		48.3	37.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter[5]		8.7	1.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter[6]		46.2	17.1	°C/W
T_{TSD}	Thermal shutdown temperature		170	170	°C
T_{TSD_HYS}	Thermal shutdown hysteresis		5	5	°C

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(5) The junction-to-top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, Ψ_{JB} estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

7.6 Power Rating

PARAMETER		TEST CONDITIONS	POWER DISSIPATION	UNIT
P_D	Average power dissipation	V_{CC} = 5 V, V_{IO} = 5 V (if applicable), T_J = 27°C, R_L = 60 Ω, S at 0 V, Input to TXD at 250 kHz, C_{L_RXD} = 15 pF. Typical CAN operating conditions at 500 kbps with 25% transmission (dominant) rate.	52	mW
		V_{CC} = 5.5 V, V_{IO} = 5.5 V (if applicable), T_J = 150°C, R_L = 50 Ω, S at 0 V, Input to TXD at 500 kHz, C_{L_RXD} = 15 pF. Typical high load CAN operating conditions at 1 Mbps with 50% transmission (dominant) rate and loaded network.	124	mW

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7.7 Electrical Characteristics

Over recommended operating conditions with T_A = –55°C to 125°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Supply Characteristics							
I_{CC}	5-V supply current	Normal mode (dominant)	See 図 8-1, TXD = 0 V, R_L = 60 Ω, C_L = open, R_{CM} = open, STB = 0 V, Typical Bus Load		40	70	mA
			See 図 8-1, TXD = 0 V, R_L = 50 Ω, C_L = open, R_{CM} = open, STB = 0 V, High Bus Load		45	80	
		Normal mode (dominant – with bus fault)	See 図 8-1, TXD = 0 V, STB = 0 V, CANH = -12 V, R_L = open, C_L = open, R_{CM} = open			110	
		Normal mode (recessive)	See 図 8-1, TXD = V_{CC} or V_{IO}, R_L = 50 Ω, C_L = open, R_{CM} = open, STB = 0 V		1.5	2.5	
		Standby mode	Devices with the "V" suffix (I/O level-shifting), V_{CC} not needed in Standby mode, See 図 8-1, TXD = V_{IO}, R_L = 50 Ω, C_L = open, R_{CM} = open, STB = V_{IO}		0.5	5	µA
			Devices without the "V" suffix (5-V only), See 図 8-1, TXD = V_{CC}, R_L = 50 Ω, C_L = open, R_{CM} = open, STB = V_{CC}			22	
I_{IO}	I/O supply current	Normal mode	RXD floating, TXD = STB = 0 or 5.5 V		90	300	
		Standby mode	RXD floating, TXD = STB = V_{IO}, V_{CC} = 0 or 5.5 V		12	17	
UV_{VCC}	Rising undervoltage detection on V_{CC} for protected mode		All devices		4.2	4.4	V
	Falling undervoltage detection on V_{CC} for protected mode			3.8	4.0	4.25	
$V_{HYS(UVVCC)}$	Hysteresis voltage on UV_{VCC}				200		mV
UV_{VIO}	Undervoltage detection on V_{IO} for protected mode		Devices with the "V" suffix (I/O level-shifting)	1.3		2.75	V
$V_{HYS(UVVIO)}$	Hysteresis voltage on UV_{VIO} for protected mode				80		mV
STB Terminal (Mode Select Input)							
V_{IH}	High-level input voltage		Devices with the "V" suffix (I/O level-shifting)	0.7 x V_{IO}			V
			Devices without the "V" suffix (5-V only)	2			
V_{IL}	Low-level input voltage		Devices with the "V" suffix (I/O level-shifting)			0.3 x V_{IO}	
			Devices without the "V" suffix (5-V only)			0.8	
I_{IH}	High-level input leakage current		STB = V_{CC} = V_{IO} = 5.5 V	-2		2	µA
I_{IL}	Low-level input leakage current		STB = 0V, V_{CC} = V_{IO} = 5.5 V	–20	0	-2	
$I_{lkg(OFF)}$	Unpowered leakage current		STB = 5.5 V, V_{CC} = V_{IO} = 0 V	-1	0	1	
TXD Terminal (CAN Transmit Data Input)							
V_{IH}	High-level input voltage		Devices with the "V" suffix (I/O level-shifting)	0.7 x V_{IO}			V
			Devices without the "V" suffix (5-V only)	2			
V_{IL}	Low-level input voltage		Devices with the "V" suffix (I/O level-shifting)			0.3 x V_{IO}	
			Devices without the "V" suffix (5-V only)			0.8	
I_{IH}	High-level input leakage current		TXD = V_{CC} = V_{IO} = 5.5 V	–2.5	0	1	µA
I_{IL}	Low-level input leakage current		TXD = 0 V, V_{CC} = V_{IO} = 5.5 V	–100	-25	–7	
$I_{lkg(OFF)}$	Unpowered leakage current		TXD = 5.5 V, V_{CC} = V_{IO} = 0 V	–1	0	1	
C_I	Input capacitance		V_{IN} = 0.4 x sin(2 x π x 2 x 10^6 x t) + 2.5 V		5		pF

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7.7 Electrical Characteristics (continued)

Over recommended operating conditions with T_A = –55°C to 125°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
RXD Terminal (Can Receive Data Output)							
V_{OH}	High-level output voltage		Devices with the "V" suffix (I/O level-shifting), See 図 8-2, I_O = –2 mA.	0.8 × V_{IO}			V
			Devices without the "V" suffix (5V only), See 図 8-2, I_O = –2 mA.	4	4.6		
V_{OL}	Low-level output voltage		Devices with the "V" suffix (I/O level-shifting), See 図 8-2, I_O = +2 mA.			0.2 x V_{IO}	
			Devices without the "V" suffix (5-V only), See 図 8-2, I_O = +2 mA.		0.2	0.4	
$I_{lkg(OFF)}$	Unpowered leakage current		RXD = 5.5 V, V_{CC} = 0 V, V_{IO} = 0 V	–1	0	1	µA
Driver Electrical Characteristics							
$V_{O(DOM)}$	Bus output voltage (dominant)	CANH	See 図 8-1 and 図 9-3, TXD = 0 V, STB = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open	2.75		4.5	V
		CANL		0.5		2.25	
$V_{O(REC)}$	Bus output voltage (recessive)	CANH and CANL	See 図 8-1 and 図 9-3, TXD = V_{CC} or V_{IO}, V_{IO} = V_{CC}, STB = 0 V , R_L = open (no load), R_{CM} = open	2	0.5 × V_{CC}	3	
$V_{O(STB)}$	Bus output voltage (Standby mode)	CANH	See 図 8-1 and 図 9-3, STB = V_{IO}, R_L = open (no load), R_{CM} = open	-0.1	0	0.1	
		CANL		-0.1	0	0.1	
		CANH - CANL		-0.2	0	0.2	
$V_{OD(DOM)}$	Differential output voltage (dominant)	CANH - CANL	See 図 8-1 and 図 9-3, TXD = 0 V, STB = 0 V, 45 Ω ≤ R_L < 50 Ω, C_L = open, R_{CM} = open	1.4		3	
			See 図 8-1 and 図 9-3, TXD = 0 V, STB = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open	1.5		3	
			See 図 8-1 and 図 9-3, TXD = 0 V, STB = 0 V, R_L = 2240 Ω, C_L = open, R_{CM} = open	1.5		5	
$V_{OD(REC)}$	Differential output voltage (recessive)	CANH - CANL	See 図 8-1 and 図 9-3, TXD = V_{CC}, STB = 0 V, R_L = 60 Ω, C_L = open, R_{CM} = open	–120		12	mV
			See 図 8-1 and 図 9-3, TXD = V_{CC}, STB = 0 V, R_L = open (no load), C_L = open, R_{CM} = open	–50		50	
V_{SYM}	Output symmetry (dominant or recessive) ($V_{O(CANH)}$ + $V_{O(CANL)}$) / V_{CC}		See 図 8-1 and 図 10-2, STB at 0 V, R_{term} = 60 Ω, C_{split} = 4.7 nF, C_L = open, R_{CM} = open, T_{XD} = 250 kHz, 1 MHz	0.9		1.1	V/V
V_{SYM_DC}	DC Output symmetry (dominant or recessive) (V_{CC} – $V_{O(CANH)}$ – $V_{O(CANL)}$)		See 図 8-1 and 図 9-3, STB = 0 V, R_L = 60 Ω, C_L = open, R_{CM} = open	–0.4		0.4	V
$I_{OS(SS_DOM)}$	Short-circuit steady-state output current, dominant, Normal mode		See 図 9-3 and 図 8-7, STB at 0 V, V_{CANH} = -5 V to 40 V, CANL = open, TXD = 0 V	–100			mA
			See 図 9-3 and 図 8-7, STB at 0 V, V_{CANL} = -5 V to 40 V, CANH = open, TXD = 0 V			100	
$I_{OS(SS_REC)}$	Short-circuit steady-state output current, recessive, Normal mode		See 図 9-3 and 図 8-7, STB at 0 V, –27 V ≤ V_{BUS} ≤ 32 V, Where V_{BUS} = CANH = CANL, TXD = V_{CC}	–5		5	mA

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7.7 Electrical Characteristics (continued)

Over recommended operating conditions with T_A = –55°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Receiver Electrical Characteristics						
V_{CM}	Common mode range, Normal mode	See 図 8-2 and 表 8-1, STB = 0 V	-30		+30	V
V_{IT+}	Positive-going input threshold voltage, Normal mode	See 図 8-2, 表 9-5 and 表 8-1, STB = 0 V, -20 V ≤ V_{CM} ≤ +20 V			900	mV
$V_{IT–}$	Negative-going input threshold voltage, Normal mode		500			
V_{IT+}	Positive-going input threshold voltage, Normal mode	See 図 8-2, 表 9-5 and 表 8-1, STB = 0 V, -30 V ≤ V_{CM} ≤ +30 V			1000	
$V_{IT–}$	Negative-going input threshold voltage, Normal mode		400			
V_{HYS}	Hysteresis voltage (V_{IT+} - $V_{IT–}$), Normal mode	See 図 8-2, 表 9-5 and 表 8-1, STB = 0 V		120		
V_{CM}	Common mode range, Standby mode	Devices with the "V" suffix (I/O level-shifting), See 図 8-2, 表 9-5 and 表 8-1, STB = V_{IO}, 4.5 V ≤ V_{IO} ≤ 5.5 V	-12		12	V
		Devices with the "V" suffix (I/O level-shifting), See 図 8-2, 表 9-5 and 表 8-1, STB = V_{IO}, 3.0 V ≤ V_{IO} ≤ 4.5 V	-2		+7	
		Devices without the "V" suffix (5V only), See 図 8-2, 表 9-5 and 表 8-1, STB = V_{CC}	-12		12	
$V_{IT(STANDBY)}$	Input threshold voltage, Standby mode	STB = V_{CC} or V_{IO}	400		1150	mV
$I_{LKG(IOFF)}$	Power-off (unpowered) bus input leakage current	CANH = CANL = 5 V, V_{CC} = V_{IO} = 0 V			4.8	µA
C_I	Input capacitance to ground (CANH or CANL)	TXD = V_{CC}, V_{IO} = V_{CC}		24	30	pF
C_{ID}	Differential input capacitance (CANH to CANL)	TXD = V_{CC}, V_{IO} = V_{CC}		12	15	
R_{ID}	Differential input resistance	TXD = V_{CC} = V_{IO} = 5 V, STB = 0 V, -30 V ≤ V_{CM} ≤ +30 V	30		80	kΩ
R_{IN}	Input resistance (CANH or CANL)		15		40	
$R_{IN(M)}$	Input resistance matching: [1 – $R_{IN(CANH)}$ / $R_{IN(CANL)}$] × 100%	V_{CANH} = V_{CANL} = 5 V	–2%		+2%	

(1) All typical values are at 25°C and supply voltages of V_{CC} = 5 V and V_{IO} = 5 V (if applicable), R_L = 60 Ω.

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7.8 Switching Characteristics

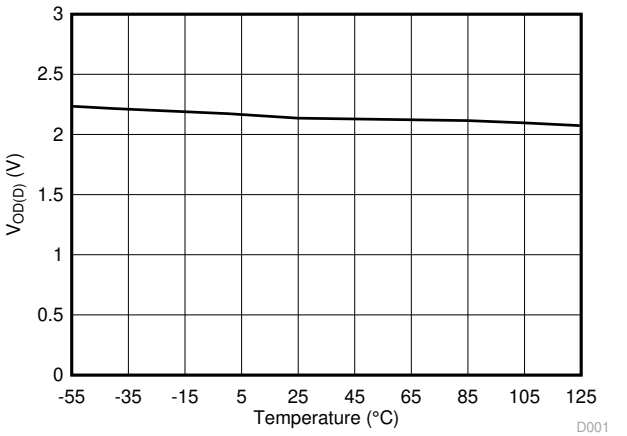
Over recommended operating conditions with T_A = -55°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Device Switching Characteristics						
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	See 図 8-4, STB = 0 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		100	160	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive			110	175	
t_{MODE}	Mode change time, from Normal to Standby or from Standby to Normal	See 図 8-3		9	45	µs
t_{WK_FILTER}	Filter time for valid wake up pattern		0.5		1.8	µs
Driver Switching Characteristics						
t_{pHR}	Propagation delay time, high TXD to driver recessive (dominant to recessive)	See 図 8-1, STB = 0 V, R_L = 60 Ω, C_L = 100 pF, R_{CM} = open		75		ns
t_{pLD}	Propagation delay time, low TXD to driver dominant (recessive to dominant)			55		
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHR} - t_{pLD} \rvert$)			20		
t_R	Differential output signal rise time			45		
t_F	Differential output signal fall time			45		
t_{TXD_DTO}	Dominant timeout	See 図 8-6, STB = 0 V, R_L = 60 Ω, C_L = open	1.2		3.8	ms
Receiver Switching Characteristics						
t_{pRH}	Propagation delay time, bus recessive input to high output (Dominant to Recessive)	See 図 8-2, STB = 0 V, $C_{L(RXD)}$ = 15 pF		65		ns
t_{pDL}	Propagation delay time, bus dominant input to low output (Recessive to Dominant)			50		ns
t_R	RXD Output signal rise time			10		ns
t_F	RXD Output signal fall time			10		ns
FD Timing Parameters						
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns, all devices	See 図 8-5 , STB = 0 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF, $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$	435		530	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns, G device variants only		155		210	
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500 ns, all devices		400		550	
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200 ns, G device variants only		120		220	
Δt_{REC}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500 ns, all devices		-65		40	
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200 ns, G device variants only		-45		15	

(1) All typical values are at 25°C and supply voltages of V_{CC} = 5 V and V_{IO} = 5 V (if applicable), R_L = 60 Ω

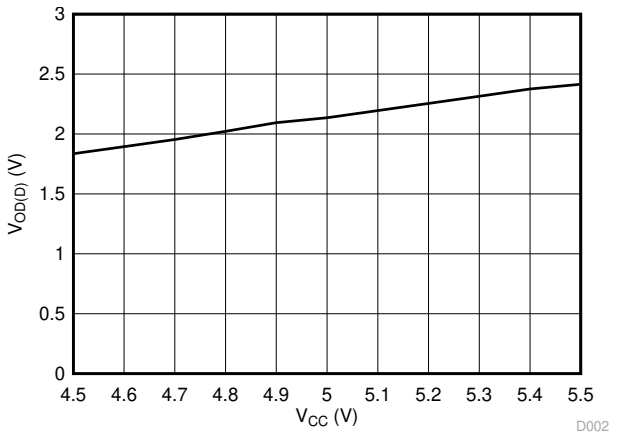
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7.9 Typical Characteristics



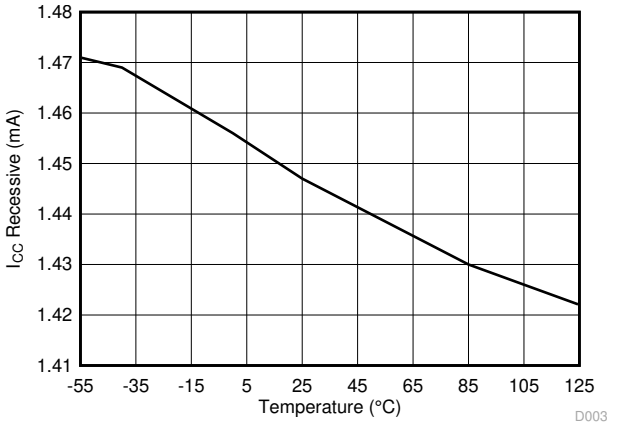
V_{CC} = 5 V　V_{IO} = 3.3 V　R_L = 60 Ω
C_L = Open　RCM = Open　STB = 0 V

図 7-1. $V_{OD(D)}$ over Temperature



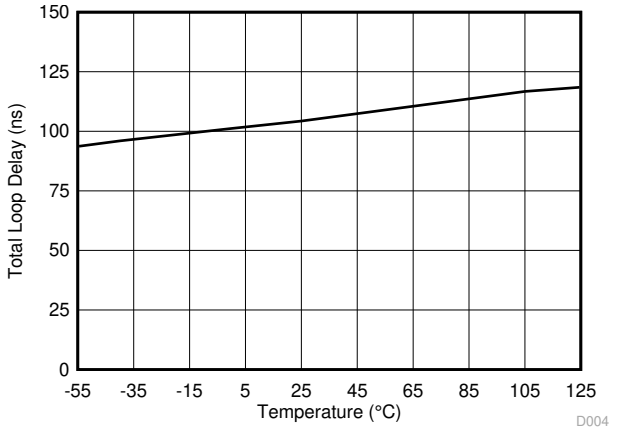
V_{IO} = 5 V　STB = 0 V　R_L = 60 Ω
C_L = Open　RCM = Open　Temp = 25°C

図 7-2. $V_{OD(D)}$ over V_{CC}



V_{CC} = 5 V　V_{IO} = 3.3 V　R_L = 60 Ω
C_L = Open　RCM = Open　STB = 0 V

図 7-3. I_{CC} Recessive over Temperature

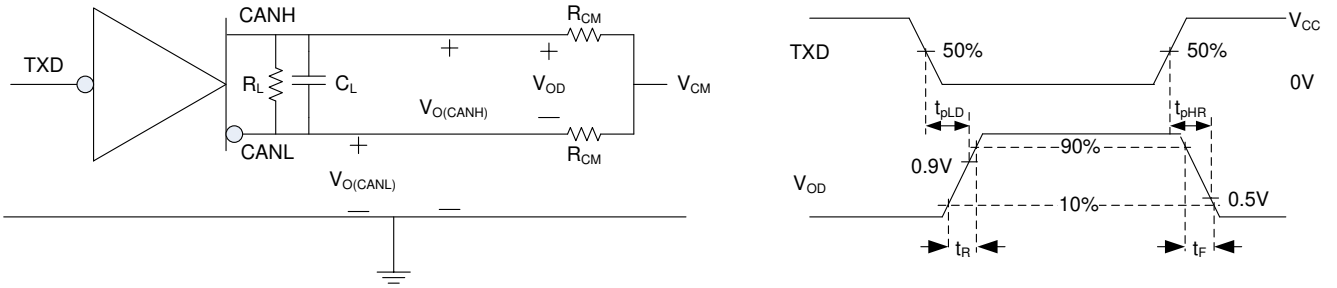


V_{CC} = 5 V　V_{IO} = 3.3 V　R_L = 60 Ω
C_L = 100 pF　C_{L_RXD} = 15 pF　STB = 0 V

図 7-4. Total Loop Delay over Temperature

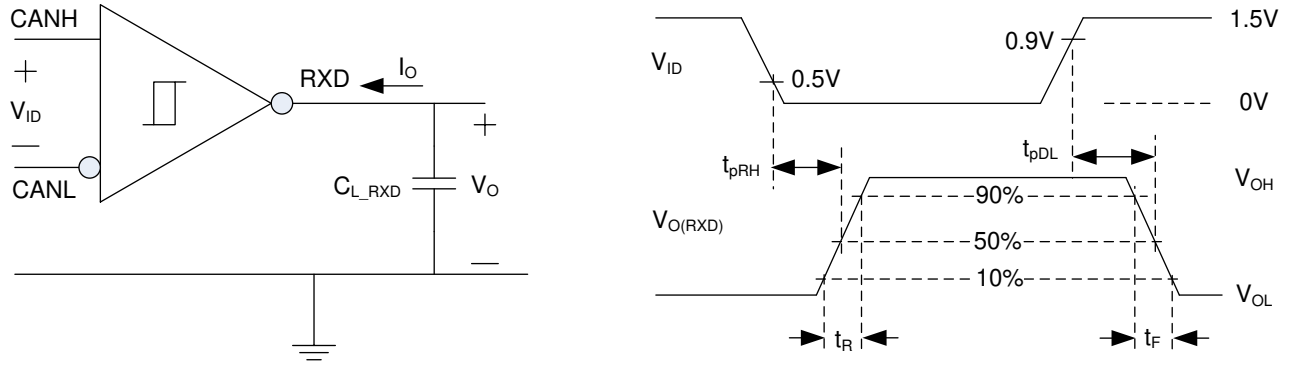
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8 Parameter Measurement Information



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図 8-1. Driver Test Circuit and Measurement



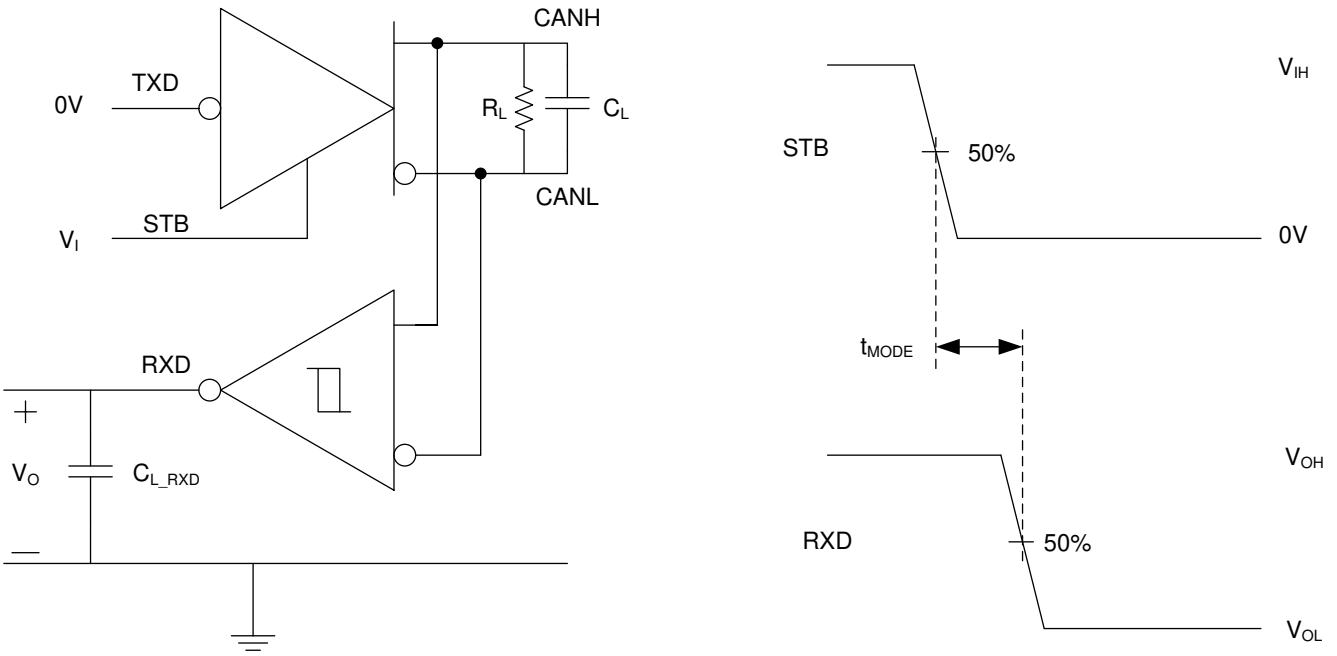
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図 8-2. Receiver Test Circuit and Measurement

表 8-1. Receiver Differential Input Voltage Threshold Test

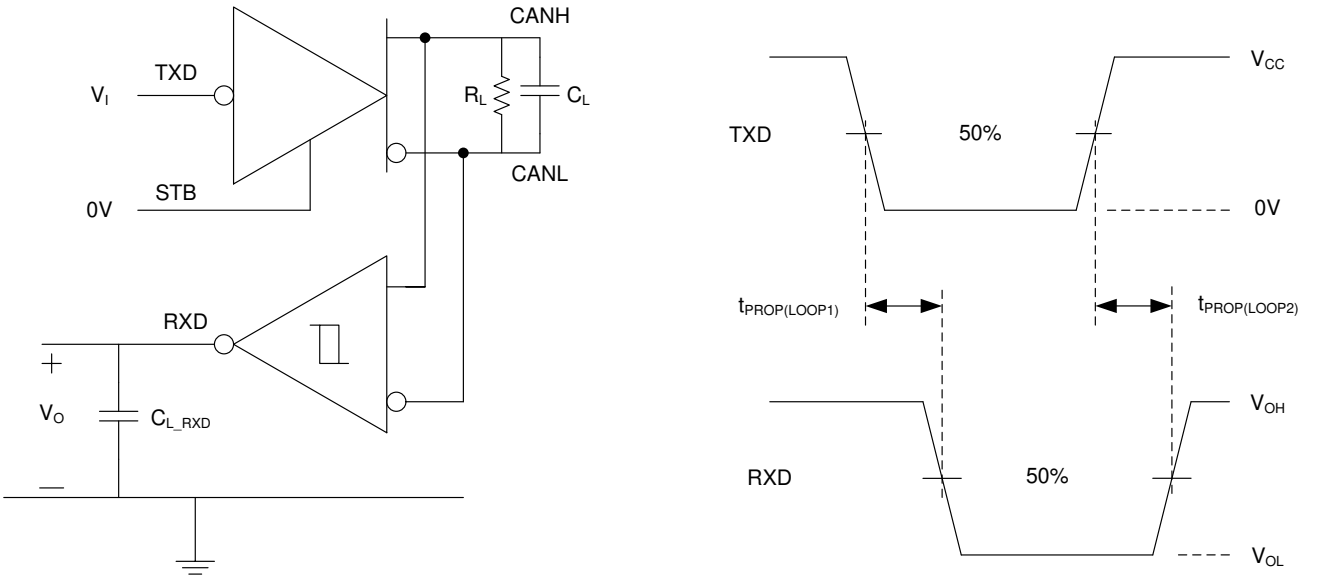
INPUT (See Receiver Test Circuit and Measurement			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	RXD	
-29.5 V	-30.5 V	1000 mV	L	V_{OL}
30.5 V	29.5 V	1000 mV	L	
-19.55 V	-20.45 V	900 mV	L	
20.45 V	19.55 V	900 mV	L	
-19.75 V	-20.25 V	500 mV	H	V_{OH}
20.25 V	19.75 V	500 mV	H	
-29.8 V	-30.2 V	400 mV	H	
30.2 V	29.8 V	400 mV	H	
Open	Open	X	H	

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図 8-3. t_{MODE} Test Circuit and Measurement



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図 8-4. $T_{PROP(LOOP)}$ Test Circuit and Measurement

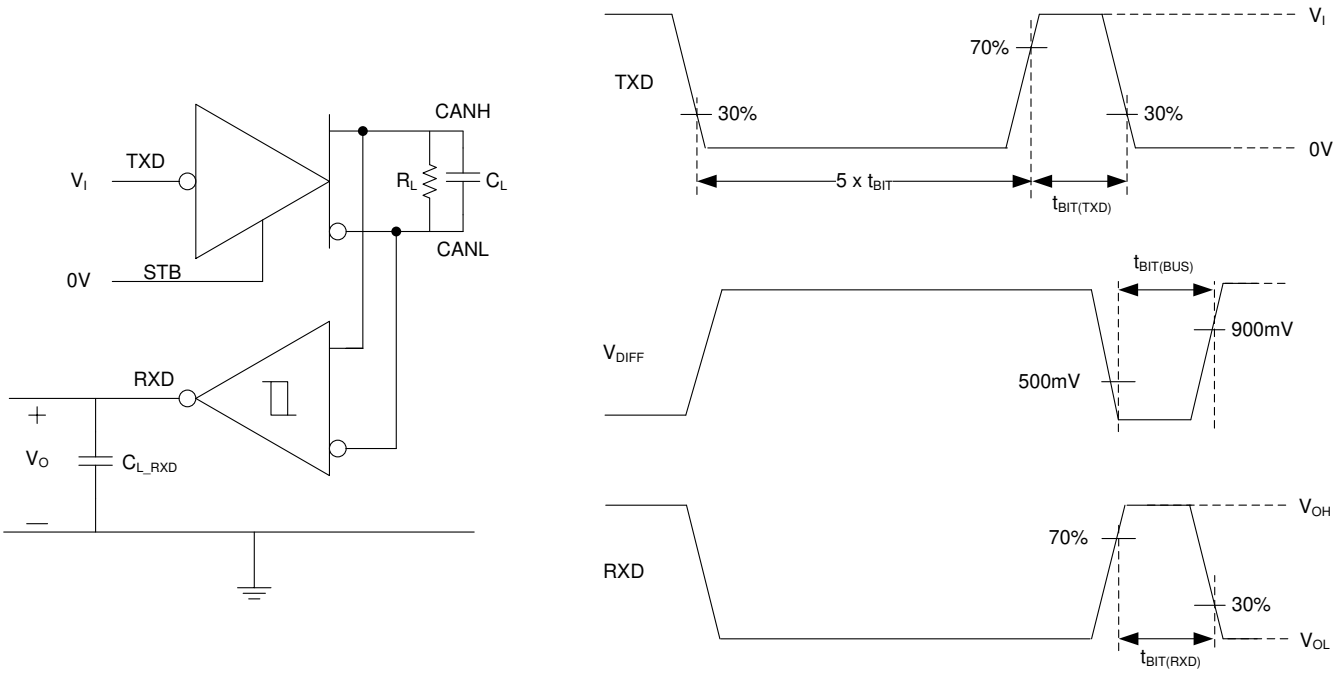
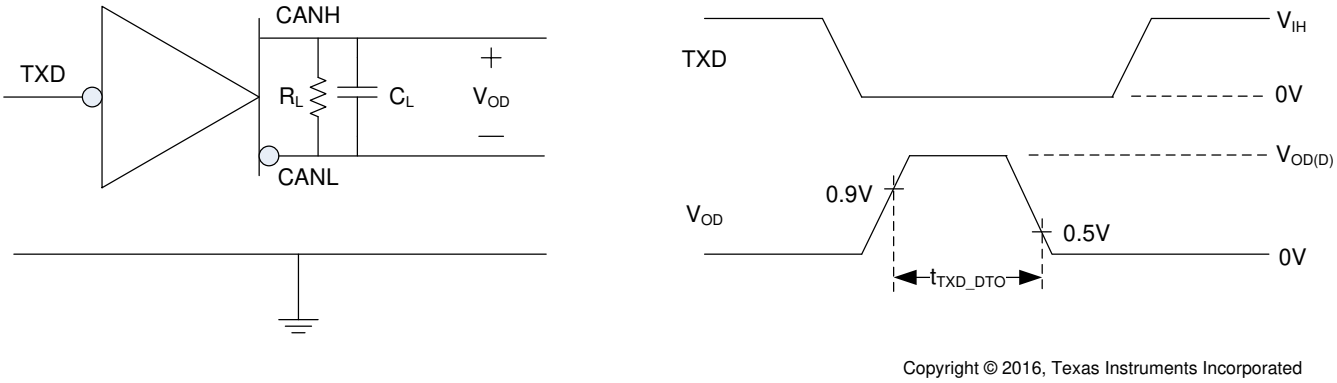


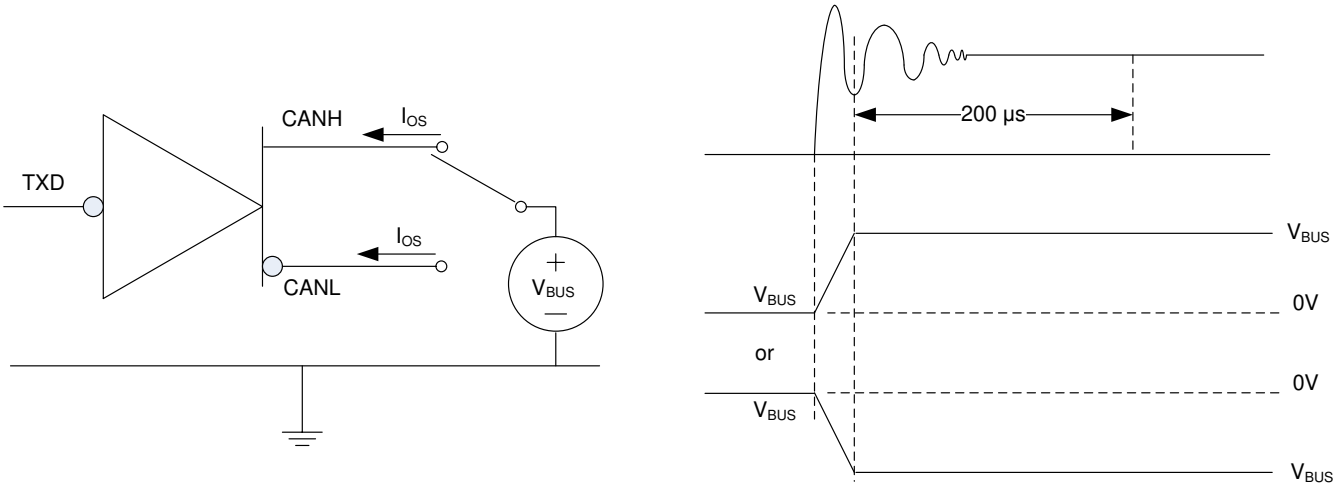
図 8-5. CAN FD Timing Parameter Measurement



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図 8-6. TXD Dominant Timeout Test Circuit and Measurement

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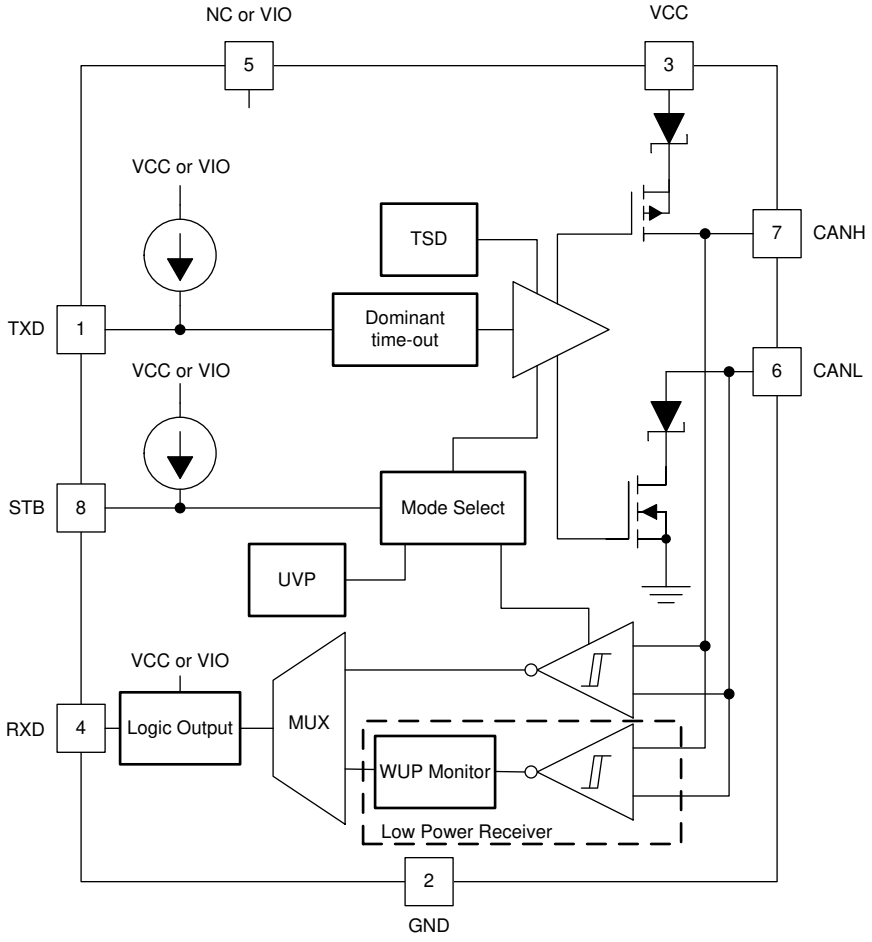
図 8-7. Driver Short Circuit Current Test and Measurement

9 Detailed Description

9.1 Overview

These CAN transceivers meet the ISO11898-2 (2016) High Speed CAN (Controller Area Network) physical layer standard. They are designed for data rates in excess of 1 Mbps for CAN FD and enhanced timing margin / higher data rates in long and highly-loaded networks. These devices provide many protection features to enhance device and CAN robustness.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 TXD Dominant Timeout (DTO)

During normal mode (the only mode where the CAN driver is active), the TXD DTO circuit prevents the transceiver from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The DTO circuit timer starts on a falling edge on TXD. The DTO circuit disables the CAN bus driver if no rising edge is seen before the timeout period expires. This frees the bus for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal is seen on the TXD terminal, thus clearing the TXD DTO condition. The receiver and RXD terminal still reflect activity on the CAN bus, and the bus terminals are biased to the recessive level during a TXD dominant timeout.

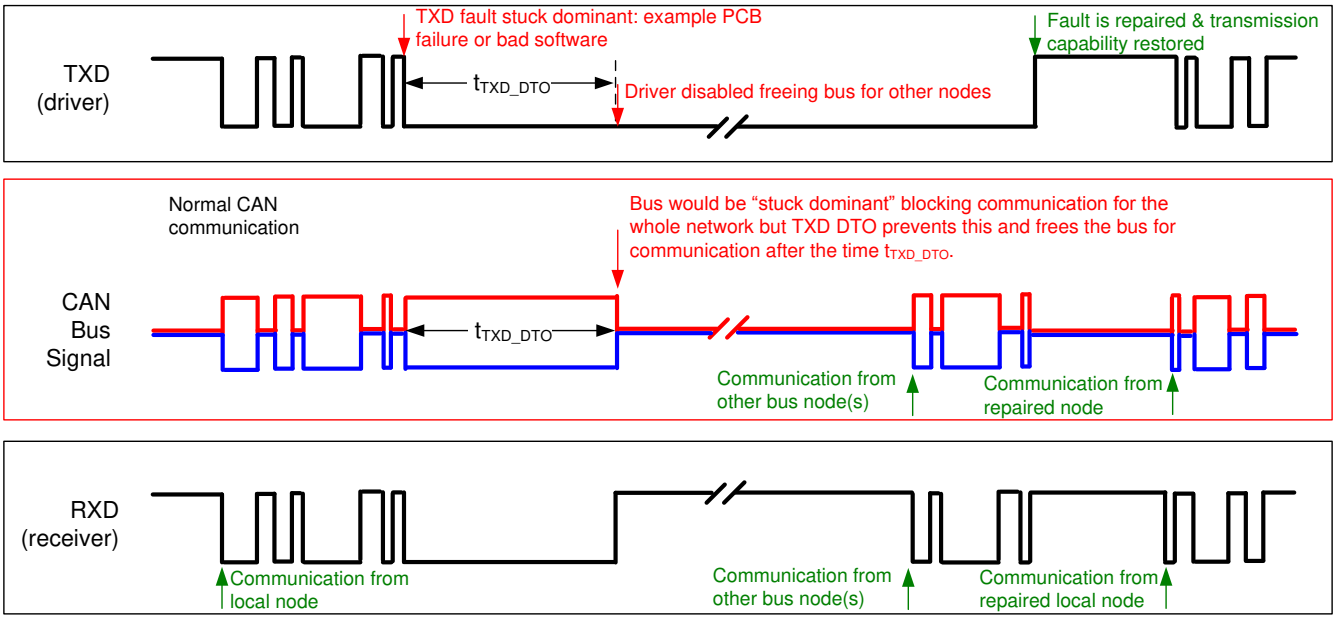


図 9-1. Example Timing Diagram for TXD DTO

Note

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{TXD_DTO} minimum, limits the minimum data rate. Calculate the minimum transmitted data rate by: Minimum Data Rate = 11 / t_{TXD_DTO}.

9.3.2 Thermal Shutdown (TSD)

If the junction temperature of the device exceeds the thermal shutdown threshold (T_{TSD}), the device turns off the CAN driver circuits thus blocking the TXD-to-bus transmission path. The CAN bus terminals are biased to the recessive level during a thermal shutdown, and the receiver-to-RXD path remains operational. The shutdown condition is cleared when the junction temperature drops at least the thermal shutdown hysteresis temperature (T_{TSD_HYS}) below the thermal shutdown temperature (T_{TSD}) of the device.

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9.3.3 Undervoltage Lockout

The supply terminals have undervoltage detection that places the device in protected mode. This protects the bus during an undervoltage event on either the V_{CC} or V_{IO} supply terminals.

表 9-1. Undervoltage Lockout 5 V Only Devices (Devices without the "V" Suffix)

V_{CC}	DEVICE STATE(1)	BUS OUTPUT	RXD
> UV_{VCC}	Normal	Per TXD	Mirrors Bus(2)
< UV_{VCC}	Protected	High Impedance	High Impedance

(1) See the V_{IT} section of the Electrical Characteristics.
(2) Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

表 9-2. Undervoltage Lockout I/O Level Shifting Devices (Devices with the "V" Suffix)

V_{CC}	V_{IO}	DEVICE STATE	BUS OUTPUT	RXD
> UV_{VCC}	> UV_{VIO}	Normal	Per TXD	Mirrors Bus(1)
< UV_{VCC}	> UV_{VIO}	STB = High: Standby Mode	Recessive	Bus Wake RXD Request(2)
		STB =Low: Protected Mode	High Impedance	High (Recessive)
> UV_{VCC}	< UV_{VIO}	Protected	High Impedance	High Impedance
< UV_{VCC}	< UV_{VIO}	Protected	High Impedance	High Impedance

(1) Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.
(2) Refer to セクション 9.4.3.1

Note

After an undervoltage condition is cleared and the supplies have returned to valid levels, the device typically resumes normal operation within 50 µs.

9.3.4 Unpowered Device

The device is designed to be 'ideal passive' or 'no load' to the CAN bus if it is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered to avoid loading down the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains in operation. The logic terminals also have extremely low leakage currents when the device is unpowered to avoid loading down other circuits that may remain powered.

9.3.5 Floating Terminals

These devices have internal pull ups on critical terminals to place the device into known states if the terminals float. The TXD terminal is pulled up to V_{CC} or V_{IO} to force a recessive input level if the terminal floats. The STB terminal is also pulled up to force the device into low power Standby mode if the terminal floats.

9.3.6 CAN Bus Short Circuit Current Limiting

The device has two protection features that limit the short circuit current when a CAN bus line is short-circuit fault condition: driver current limiting (both dominant and recessive states) and TXD dominant state time out to prevent permanent higher short circuit current of the dominant state during a system fault. During CAN communication the bus switches between dominant and recessive states, thus the short circuit current may be viewed either as the instantaneous current during each bus state or as an average current of the two states. For system current (power supply) and power considerations in the termination resistors and common-mode choke ratings, use the average short circuit current. Determine the ratio of dominant and recessive bits by the data in the CAN frame plus the following factors of the protocol and PHY that force either recessive or dominant at certain times:

- Control fields with set bits
- Bit stuffing
- Interframe space

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- TXD dominant time out (fault case limiting)

These ensure a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits. The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated with the following formula:

$$I_{OS(AVG)} = \%Transmit \times [(\%REC_Bits \times I_{OS(SS)_REC}) + (\%DOM_Bits \times I_{OS(SS)_DOM})] + [\%Receive \times I_{OS(SS)_REC}] \quad (1)$$

Where:

- $I_{OS(AVG)}$ is the average short circuit current
- %Transmit is the percentage the node is transmitting CAN messages
- %Receive is the percentage the node is receiving CAN messages
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)_REC}$ is the recessive steady state short circuit current
- $I_{OS(SS)_DOM}$ is the dominant steady state short circuit current

Note

Consider the short circuit current and possible fault cases of the network when sizing the power ratings of the termination resistance and other network components.

9.3.7 Digital Inputs and Outputs

9.3.7.1 Devices with V_{CC} Only (Devices without the "V" Suffix):

The 5-V V_{CC} only devices are supplied by a single 5-V rail. The digital inputs have TTL input thresholds and are therefore 5 V and 3.3 V compatible. The RXD outputs on these devices are driven to the V_{CC} rail for logic high output. Additionally, the TXD and STB pins are internally pulled up to V_{CC}. The internal bias of the mode pins may only place the device into a known state if the terminals float, they may not be adequate for system-level biasing during transients or noisy environments.

Note

TXD pull up strength and CAN bit timing require special consideration when these devices are used with CAN controllers with an open-drain TXD output. An adequate external pull up resistor must be used to ensure that the CAN controller output of the microcontroller maintains adequate bit timing to the TXD input.

9.3.7.2 Devices with V_{IO} I/O Level Shifting (Devices with "V" Suffix):

These devices use a 5 V V_{CC} power supply for the CAN driver and high speed receiver blocks. These transceivers have a second power supply for I/O level-shifting (V_{IO}). This supply is used to set the CMOS input thresholds of the TXD and pins and the RXD high level output voltage. Additionally, the internal pull ups on TXD and STB are pulled up to V_{IO}.

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9.4 Device Functional Modes

The device has two main operating modes: Normal mode and Standby mode. Operating mode selection is made via the STB input terminal.

表 9-3. Operating Modes

STB Terminal	MODE	DRIVER	RECEIVER	RXD Terminal
LOW	Normal Mode	Enabled (ON)	Enabled (ON)	Mirrors Bus State(1)
HIGH	Standby Mode	Disabled (OFF)	Disabled (OFF) (Low Power Bus Monitor is Active)	High (Unless valid WUP has been received)

(1) Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

9.4.1 CAN Bus States

The CAN bus has two states during powered operation of the device: *dominant* and *recessive*. A dominant bus state is when the bus is driven differentially, corresponding to a logic low on the TXD and RXD terminal. A recessive bus state is when the bus is biased to V_{CC} / 2 via the high-resistance internal input resistors R_{IN} of the receiver, corresponding to a logic high on the TXD and RXD terminals.

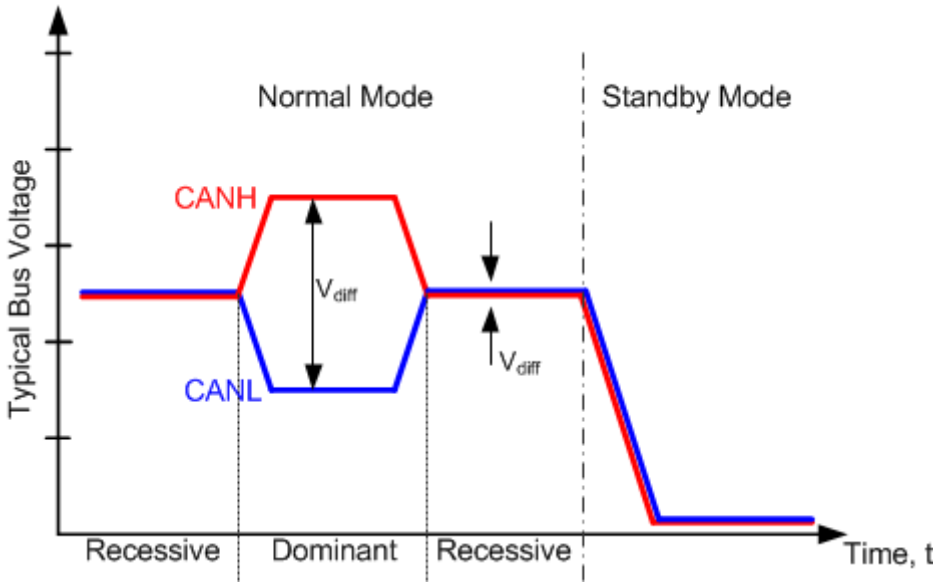


図 9-2. Bus States (Physical Bit Representation)

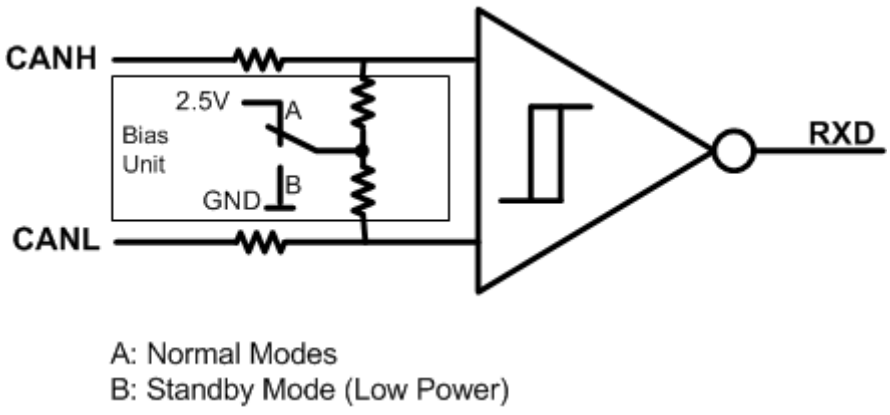


図 9-3. Bias Unit (Recessive Common Mode Bias) and Receiver

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9.4.2 Normal Mode

Select the *Normal mode* of device operation by setting STB terminal low. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver translates a digital input on TXD to a differential output on CANH and CANL. The receiver translates the differential signal from CANH and CANL to a digital output on RXD.

9.4.3 Standby Mode

Activate low power Standby mode by setting STB terminal high. In this mode the bus transmitter will not send data nor will the normal mode receiver accept data as the bus lines are biased to ground minimizing the system supply current. Only the low power receiver will be actively monitoring the bus for activity. RXD indicates a valid wake up event after a wake-up pattern (WUP) has been detected on the Bus. The low power receiver is powered using only the V_{IO} pin. This allows V_{CC} to be removed reducing power consumption further.

The bus lines are biased to ground in Standby mode to minimize the required system supply current. The low power receiver is supplied by V_{IO} and is capable of detecting CAN bus activity even if V_{IO} is the only supply voltage available to the transceiver.

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9.4.3.1 Remote Wake Request via Wake Up Pattern (WUP) in Standby Mode

The family offers a remote wake request feature that is used to indicate to the host microcontroller that the bus is active and the node should return to normal operation.

These devices use the multiple filtered dominant wake up pattern (WUP) from the ISO11898-2 (2016) to qualify bus activity. Once a valid WUP has been received the wake request will be indicated to the microcontroller by a falling edge and low corresponding to a "filtered" dominant on the RXD output terminal.

The WUP consists of a filtered dominant pulse, followed by a filtered recessive pulse, and finally by a second filtered dominant pulse. These filtered dominant, recessive, dominant pulses do not need to occur in immediate succession. There is no timeout that will occur between filtered bits of the WUP. Once a full WUP has been detected the device will continue to drive the RXD output low every time an additional filtered dominant signal is received from the bus.

For a dominant or recessive signal to be considered "filtered", the bus must continually remain in that state for more than t_{WK_FILTER}. Due to variability in the t_{WK_FILTER}, the following three scenarios can exist:

1. Bus signals that last less than $t_{WK_FILTER(MIN)}$ will never be detected as part of a valid WUP
2. Bus signals that last more than $t_{WK_FILTER(MIN)}$ but less than $t_{WK_FILTER(MAX)}$ may be detected as part of a valid WUP
3. Bus signals that last more than $t_{WK_FILTER(MAX)}$ will always be detected as part of a valid WUP

Once the first filtered dominant signal is received, the device is now waiting on a filtered recessive signal, other bus traffic will not reset the bus monitor. Once the filtered recessive signal is received, the monitor is now waiting on a second filtered dominant signal, and again other bus traffic will not reset the monitor. After reception of the full WUP, the device will transition to driving the RXD output pin low for the remainder of any dominant signal that remains on the bus for longer than t_{WK_FILTER}.

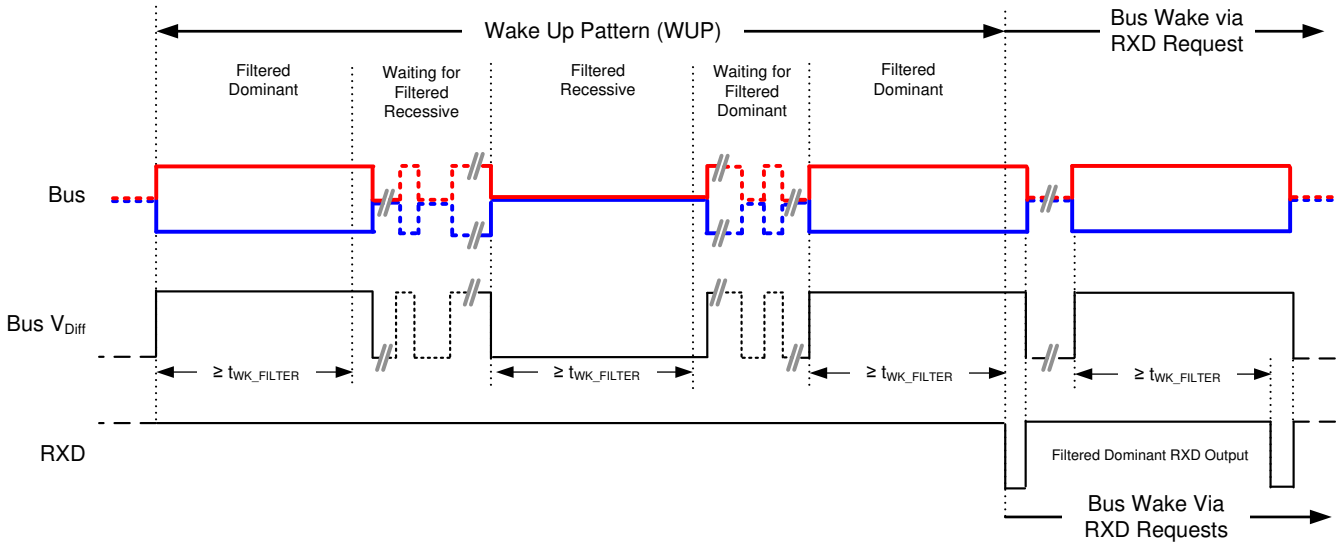


図 9-4. Wake Up Pattern (WUP)

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9.4.4 Driver and Receiver Function Tables

表 9-4. Driver Function Table

DEVICE	INPUTS		OUTPUTS		DRIVEN BUS STATE
	STB (1)	TXD(1) (2)	CANH(1)	CANL(1)	
All Devices	L	L	H	L	Dominant
		H or Open	Z	Z	Recessive
	H or Open	X	Z	Z	Recessive

(1) H = high level, L = low level, X = irrelevant, Z = common mode (recessive) bias to V_{CC} / 2. See CAN Bus States for bus state and common mode bias information.
(2) Devices have an internal pull up to V_{CC} or V_{IO} on TXD terminal. If the TXD terminal is open, the terminal is pulled high and the transmitter remain in recessive (non-driven) state.

表 9-5. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} – V_{CANL}$	BUS STATE	RXD TERMINAL(1)
Normal	$V_{ID} \geq V_{IT+(MAX)}$	Dominant	L(2)
	$V_{IT-(MIN)} < V_{ID} < V_{IT+(MAX)}$	?	?(2)
	$V_{ID} \leq V_{IT-(MIN)}$	Recessive	H(2)
	Open ($V_{ID} \approx 0$ V)	Open	H

(1) H = high level, L = low level, ? = indeterminate.
(2) See *Receiver Electrical Characteristics* section for input thresholds.

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10 Application Information Disclaimer

Note

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10.1 Application Information

These CAN transceivers are typically used in applications with a host microprocessor or FPGA that includes the data link layer portion of the CAN protocol. Below are typical application configurations for both 5 V and 3.3 V microprocessor applications. The bus termination is shown for illustrative purposes.

10.2 Typical Applications

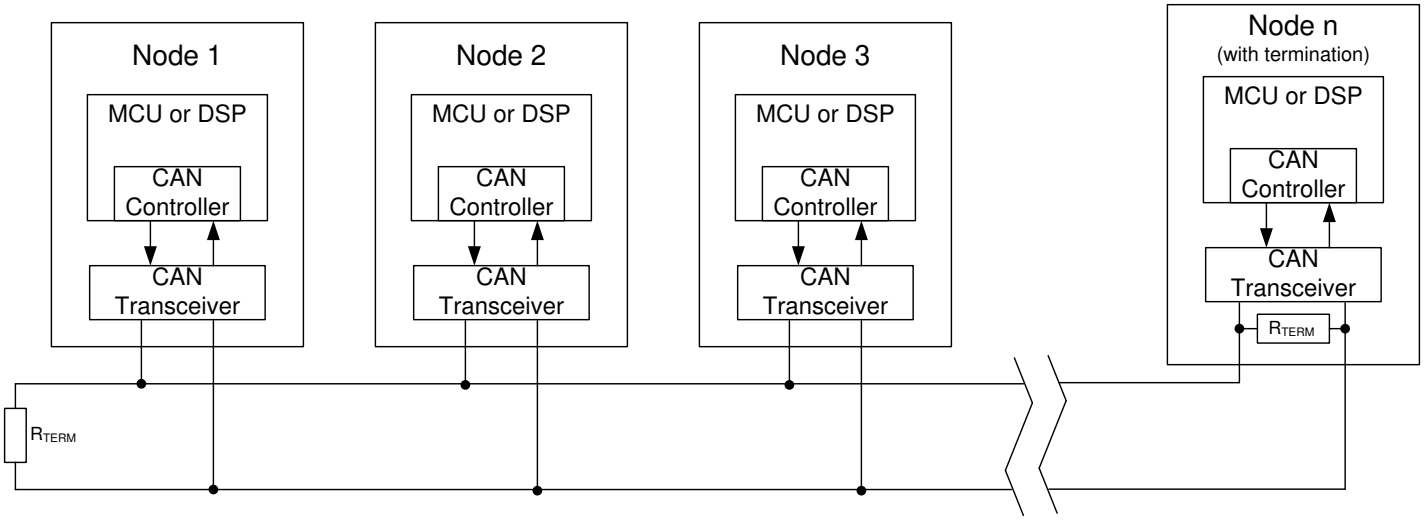


図 10-1. Typical CAN Bus Application

10.2.1 Design Requirements

10.2.1.1 Bus Loading, Length and Number of Nodes

The ISO 11898-2 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires transceivers with high input impedance such as the TCAN1042 family of transceivers.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2. They have made system-level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, DeviceNet and NMEA2000.

The TCAN1042 family is specified to meet the 1.5 V requirement with a 50Ω load, incorporating the worst case including parallel transceivers. The differential input resistance of the TCAN1042 family is a minimum of 30 kΩ. If 100 TCAN1042 family transceivers are in parallel on a bus, this is equivalent to a 300Ω differential load worst case. That transceiver load of 300 Ω in parallel with the 60Ω gives an equivalent loading of 50 Ω. Therefore, the TCAN1042 family theoretically supports up to 100 transceivers on a single bus segment. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is typically much lower. Bus length may also be extended beyond the original ISO 11898 standard of 40 m by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

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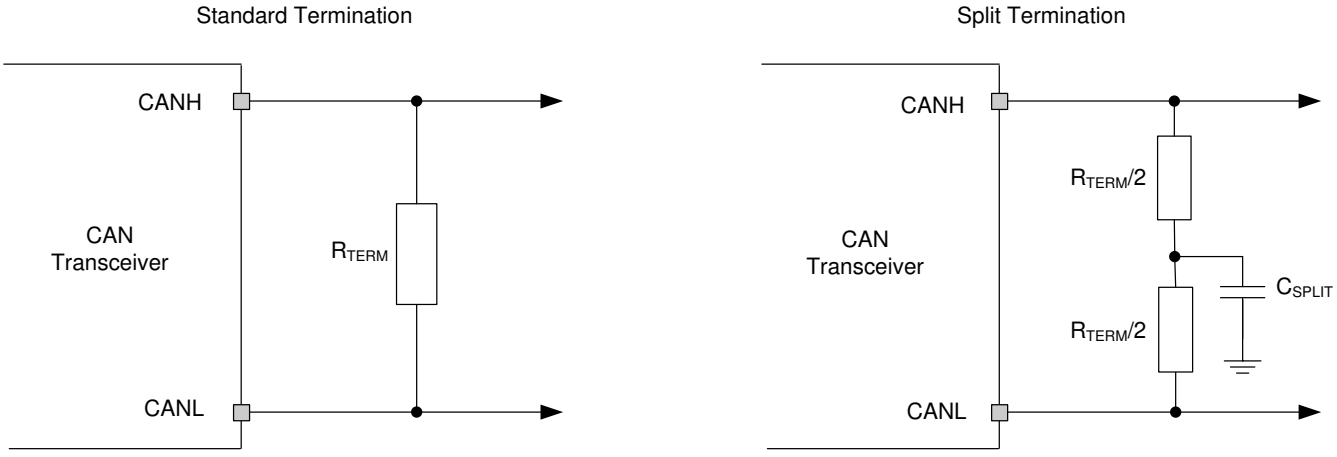
This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. In using this flexibility comes the responsibility of good network design and balancing these tradeoffs.

10.2.2 Detailed Design Procedures

10.2.2.1 CAN Termination

The ISO 11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus, the termination must be carefully placed so that two terminations always exist on the network.

Termination may be a single 120-Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used. (See 図 10-2). Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.



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図 10-2. CAN Bus Termination Concepts

The family of transceivers have variants for both 5-V only applications and applications where level shifting is needed for a 3.3-V microcontroller.

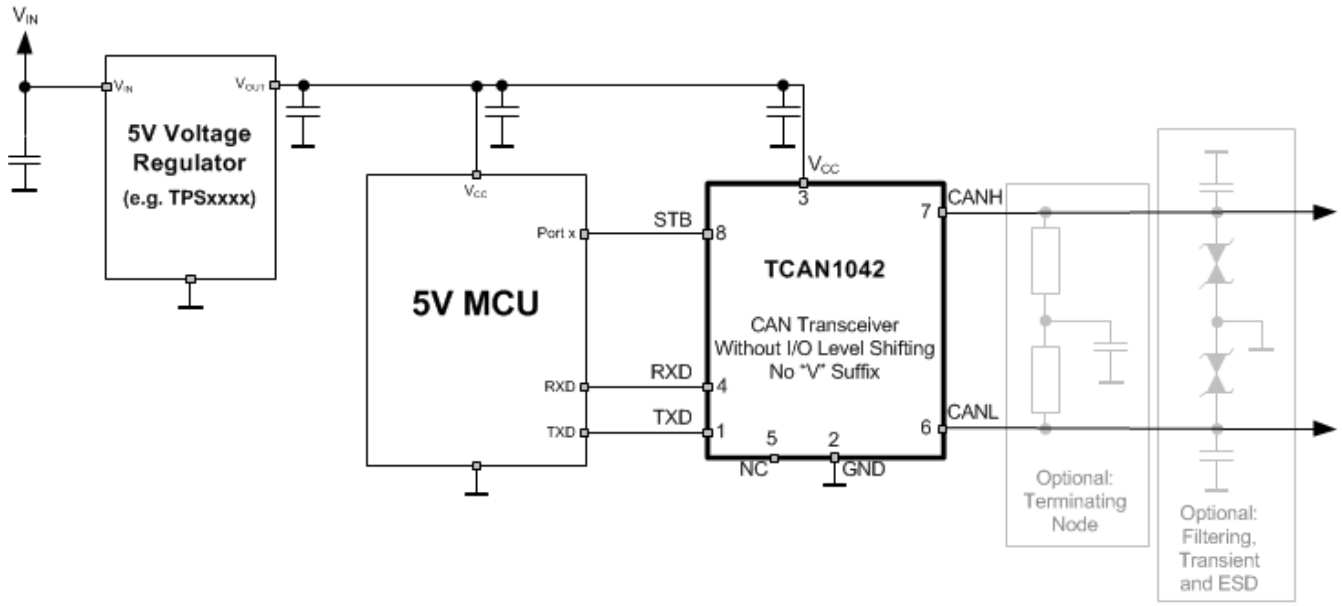


図 10-3. Typical CAN Bus Application Using 5V CAN Controller

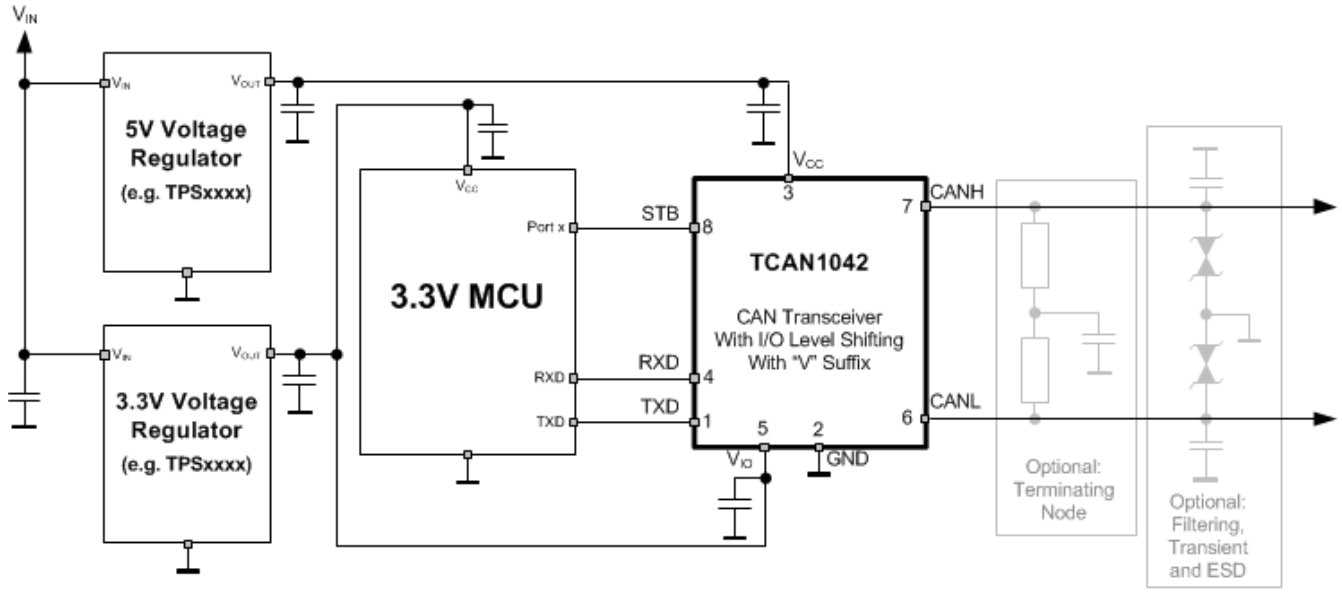


図 10-4. Typical CAN Bus Application Using 3.3 V CAN Controller

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10.2.3 Application Curves

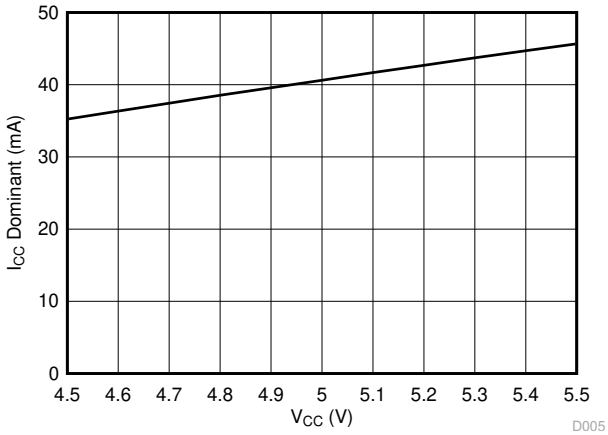


図 10-5. I_{CC} Dominant Current over V_{CC} Supply Voltage

11 Power Supply Recommendations

These devices are designed to operate from a V_{CC} input supply voltage range between 4.5 V and 5.5 V. Some devices have an output level shifting supply input, V_{IO}, designed for a range between 3 V and 5.5 V. Both supply inputs must be well regulated. A bulk capacitance, typically 4.7 µF, should be placed near the CAN transceiver's main V_{CC} supply output, and in addition a bypass capacitor, typically 0.1 µF, should be placed as close to the device V_{CC} and V_{IO} supply terminals. This helps to reduce supply voltage ripple present on the outputs of the switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes and traces.

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Layout

Robust and reliable bus node design often requires the use of external transient protection device in order to protect against EFT and surge transients that may occur in industrial environments. Because ESD and transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design. The family comes with high on-chip IEC ESD protection, but if higher levels of system level immunity are desired external TVS diodes can be used. TVS diodes and bus filtering capacitors should be placed as close to the on-board connectors as possible to prevent noisy transient events from propagating further into the PCB and system.

12.1 Layout Guidelines

- Place the protection and filtering circuitry as close to the bus connector, J1, to prevent transients, ESD and noise from propagating onto the board. In this layout example a transient voltage suppression (TVS) device, D1, has been used for added protection. The production solution can be either bi-directional TVS diode or varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors C4 and C5. Additionally (not shown) a series common mode choke (CMC) can be placed on the CANH and CANL lines between the transceiver U1 and connector J1.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Use supply (V_{CC}) and ground planes to provide low inductance.

Note

High-frequency currents follows the path of least impedance and not the path of least resistance.

- Use at least two vias for supply (V_{CC}) and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.
- Bypass and bulk capacitors should be placed as close as possible to the supply terminals of transceiver, examples are C1, C2 on the V_{CC} supply and C6 and C7 on the V_{IO} supply.
- Bus termination: this layout example shows split termination. This is where the termination is split into two resistors, R6 and R7, with the center or split tap of the termination connected to ground via capacitor C3. Split termination provides common mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to ensure the terminating node is not removed from the bus thus also removing the termination. See the application section for information on power ratings needed for the termination resistor(s).
- To limit current of digital lines, serial resistors may be used. Examples are R2, R3, and R4. These are not required.
- Terminal 1: R1 is shown optionally for the TXD input of the device. If an open drain host processor is used, this is mandatory to ensure the bit timing into the device is met.
- Terminal 5: For "V" variants of the family, bypass capacitors should be placed as close to the pin as possible (example C6 and C7). For device options without V_{IO} I/O level shifting, this pin is not internally connected and can be left floating or tied to any existing net, for example a split pin connection.
- Terminal 8: is shown assuming the mode terminal, STB, will be used. If the device will only be used in normal mode, R4 is not needed and R5 could be used for the pull down resistor to GND.

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12.2 Layout Example

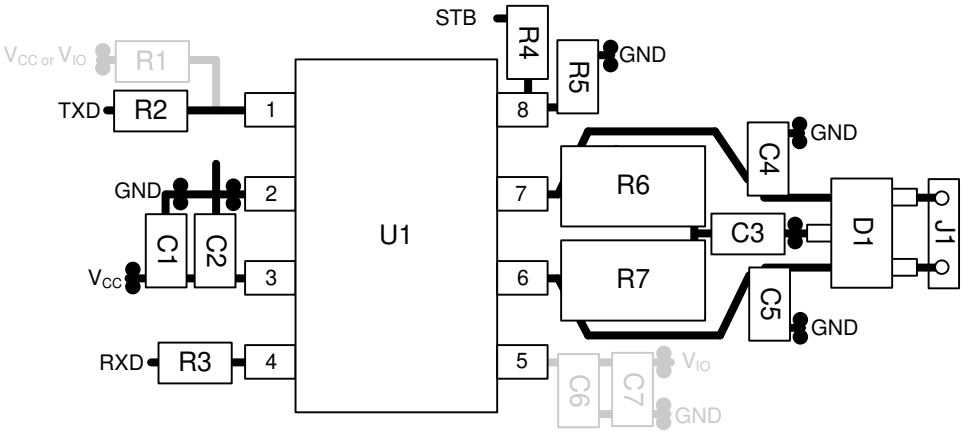


図 12-1. Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 サポート・リソース

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12.3 Trademarks

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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCAN1042DQ1	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-55 to 125	1042
TCAN1042DRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1042
TCAN1042DRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042
TCAN1042DRBRQ1.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042
TCAN1042DRBTQ1	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1042
TCAN1042DRBTQ1.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042
TCAN1042DRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042
TCAN1042DRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042
TCAN1042DRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042
TCAN1042GDQ1	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-55 to 125	1042
TCAN1042GDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1042
TCAN1042GDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042
TCAN1042GDRBRQ1.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042
TCAN1042GDRBTQ1	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1042
TCAN1042GDRBTQ1.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042
TCAN1042GDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042
TCAN1042GDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042
TCAN1042GDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042
TCAN1042GVDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042GVDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042GVDRBRQ1.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042GVDRBTQ1	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042GVDRBTQ1.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042GVDRBTQ1.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042GVDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042V
TCAN1042GVDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042V
TCAN1042GVDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042V
TCAN1042HDQ1	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-55 to 125	1042
TCAN1042HDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1042

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCAN1042HDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042
TCAN1042HDRBRQ1.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042
TCAN1042HDRBTQ1	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1042
TCAN1042HDRBTQ1.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042
TCAN1042HDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042
TCAN1042HDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042
TCAN1042HDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042
TCAN1042HGDQ1	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-55 to 125	1042
TCAN1042HGDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1042
TCAN1042HGDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042
TCAN1042HGDRBRQ1.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042
TCAN1042HGDRBTQ1	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1042
TCAN1042HGDRBTQ1.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042
TCAN1042HGDRBTQ1.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042
TCAN1042HGDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042
TCAN1042HGDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042
TCAN1042HGDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042
TCAN1042HGVDQ1	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-55 to 125	1042V
TCAN1042HGVDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042HGVDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042HGVDRBRQ1.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042HGVDRBTQ1	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042HGVDRBTQ1.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042HGVDRBTQ1.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042HGVDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042V
TCAN1042HGVDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042V
TCAN1042HGVDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042V
TCAN1042HVDQ1	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-55 to 125	1042V
TCAN1042HVDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042HVDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042HVDRBRQ1.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042V

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCAN1042HVDRBTQ1	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042HVDRBTQ1.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042HVDRBTQ1.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042HVDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042V
TCAN1042HVDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042V
TCAN1042HVDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042V
TCAN1042VDQ1	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-55 to 125	1042V
TCAN1042VDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042VDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042VDRBRQ1.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042VDRBTQ1	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042VDRBTQ1.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042VDRBTQ1.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1042V
TCAN1042VDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042V
TCAN1042VDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042V
TCAN1042VDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042V

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TCAN1042H-Q1, TCAN1042HG-Q1, TCAN1042HGV-Q1, TCAN1042HV-Q1 :

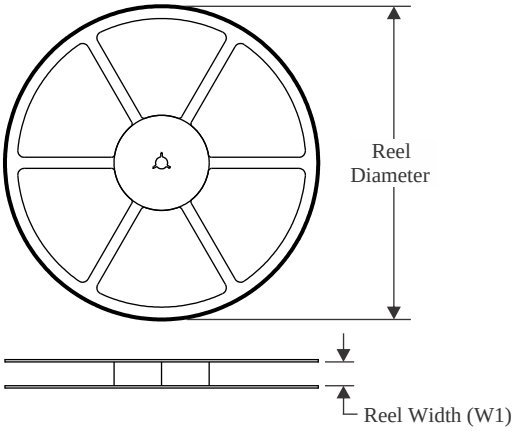
- Catalog : TCAN1042H, TCAN1042HG, TCAN1042HGV, TCAN1042HV

NOTE: Qualified Version Definitions:

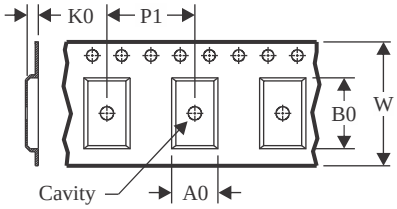
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

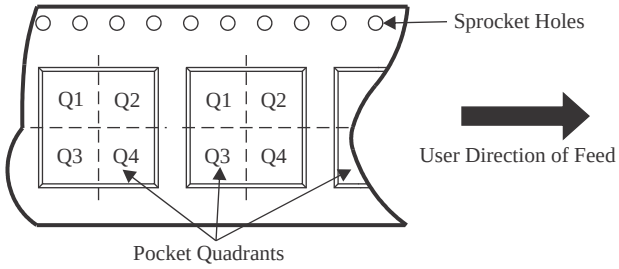


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

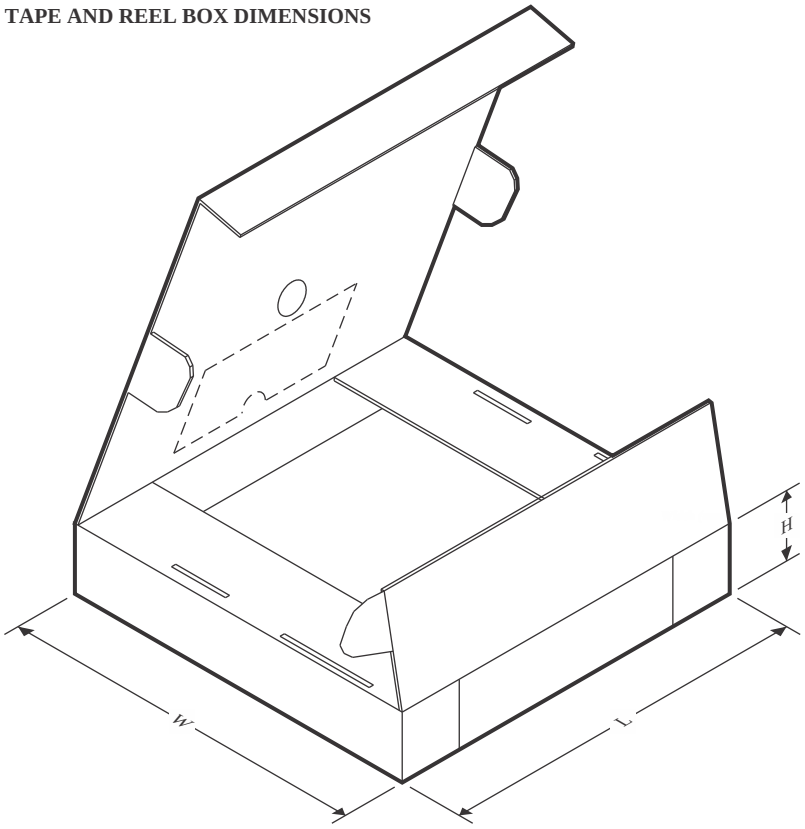


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1042DRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TCAN1042DRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TCAN1042DRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1042GDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TCAN1042GDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1042GDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1042GDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TCAN1042GDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1042GVDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1042GVDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TCAN1042GVDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1042GVDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TCAN1042GVDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1042HDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1042HDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TCAN1042HDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1042HDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1042HDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1042HGDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1042HGDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TCAN1042HGDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1042HGDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TCAN1042HGDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1042HGVDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TCAN1042HGVDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1042HGVDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TCAN1042HGVDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1042HGVDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1042HGVDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1042HVDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TCAN1042HVDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1042HVDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TCAN1042HVDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1042HVDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1042VDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TCAN1042VDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1042VDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1042VDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TCAN1042VDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1042DRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN1042DRBTQ1	SON	DRB	8	250	210.0	185.0	35.0
TCAN1042DRQ1	SOIC	D	8	2500	353.0	353.0	32.0
TCAN1042GDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN1042GDRBRQ1	SON	DRB	8	3000	346.0	346.0	35.0
TCAN1042GDRBTQ1	SON	DRB	8	250	200.0	183.0	25.0
TCAN1042GDRBTQ1	SON	DRB	8	250	210.0	185.0	35.0
TCAN1042GDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
TCAN1042GVDRBRQ1	SON	DRB	8	3000	346.0	346.0	35.0
TCAN1042GVDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN1042GVDRBTQ1	SON	DRB	8	250	200.0	183.0	25.0
TCAN1042GVDRBTQ1	SON	DRB	8	250	210.0	185.0	35.0
TCAN1042GVDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
TCAN1042HDRBRQ1	SON	DRB	8	3000	346.0	346.0	35.0
TCAN1042HDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN1042HDRBTQ1	SON	DRB	8	250	210.0	185.0	35.0
TCAN1042HDRBTQ1	SON	DRB	8	250	200.0	183.0	25.0
TCAN1042HDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1042HGDRBRQ1	SON	DRB	8	3000	346.0	346.0	35.0
TCAN1042HGDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN1042HGDRBTQ1	SON	DRB	8	250	200.0	183.0	25.0
TCAN1042HGDRBTQ1	SON	DRB	8	250	210.0	185.0	35.0
TCAN1042HGDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
TCAN1042HGVDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN1042HGVDRBRQ1	SON	DRB	8	3000	346.0	346.0	35.0
TCAN1042HGVDRBTQ1	SON	DRB	8	250	210.0	185.0	35.0
TCAN1042HGVDRBTQ1	SON	DRB	8	250	200.0	183.0	25.0
TCAN1042HGVDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
TCAN1042HGVDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
TCAN1042HVDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN1042HVDRBRQ1	SON	DRB	8	3000	346.0	346.0	35.0
TCAN1042HVDRBTQ1	SON	DRB	8	250	210.0	185.0	35.0
TCAN1042HVDRBTQ1	SON	DRB	8	250	200.0	183.0	25.0
TCAN1042HVDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
TCAN1042VDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN1042VDRBRQ1	SON	DRB	8	3000	346.0	346.0	35.0
TCAN1042VDRBTQ1	SON	DRB	8	250	200.0	183.0	25.0
TCAN1042VDRBTQ1	SON	DRB	8	250	210.0	185.0	35.0
TCAN1042VDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

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最終更新日：2025 年 10 月