TCAN1046V-Q1 車載用、フォルト保護、デュアル CAN トランシーバ

1 特長

- AEC-Q100: 車載アプリケーション認定済み
  - 温度グレード 1: -40℃～125℃、T_A
- 独立したモード制御を備えた 2 つの高速 CAN トランシーバ
- ISO 11898-2:2016 および ISO 11898-5:2007 物理層規格の要件に適合
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- Classical CAN のサポートと最適化された CAN FD 性能 (2、5、8Mbps)
  - 短く対称的な伝搬遅延時間によりタイミング・マージンを強化
  - 負荷のある CAN ネットワークでより高いデータ・レートを実現
- の I/O 電圧範囲は 1.7V～5.5V をサポート
  - 1.8V、2.5V、3.3V、5V のアプリケーションをサポート
- 保護機能:
  - バス・フォルト保護: ±58V
  - 低電圧保護
  - TXD ドミナント・タイムアウト (DTO)
    - 最低 9.2kbps のデータ・レート
  - サーマル・シャットダウン保護 (TSD)
- 動作モード:
  - 通常モード
  - リモート・ウェイクアップ要求をサポートする、低消費電力スタンバイ・モード
- 電源非接続時の最適化された挙動
  - バスおよびロジック端子は高インピーダンス (動作中のバスやアプリケーションに対して無負荷)
  - 活線挿抜対応: バスおよび RXD 出力において電源オン / オフ時のグリッチのない動作
- 接合部温度範囲: –40℃～150℃
- レシーバの同相入力電圧: ±12V
- SOIC (14) パッケージ、自動光学検査 (AOI) 性能を向上させたリードレス VSON (14) パッケージ (4.5mm × 3.0mm) で供給

2 アプリケーション

- 車両および輸送システム
  - 車体制御モジュール
  - 車載ゲートウェイ
  - 先進運転支援システム (ADAS)
  - インフォテインメント

3 概要

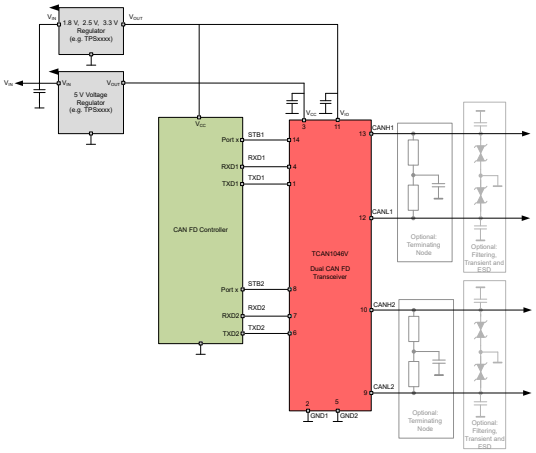
TCAN1046V-Q1 は、ISO 11898-2:2016 高速 CAN (Controller Area Network) 仕様の物理層要件を満たすデュアル高速 CAN トランシーバです。

TCAN1046V-Q1 トランシーバは Classical CAN ネットワークおよび最高 8 メガビット/秒 (Mbps) の CAN FD ネットワークの両方に対応しています。TCAN1046V-Q1 は V_{IO} 端子によるロジック・レベル変換を内蔵しているため、1.8V、2.5V、3.3V、5V のロジック I/O に直接接続できます。2 つの CAN チャネルは、スタンバイ・ピンによる独立したモード制御をサポートしています。これにより、他の CAN チャネルの状態に影響を与えずに、低消費電力状態であるスタンバイ・モードに各トランシーバを移行できます。TCAN1046V-Q1 は、スタンバイ・モードのとき、ISO 11898-2:2016 に定義されたウェイクアップ・パターン (WUP) によるリモート・ウェイクアップをサポートします。TCAN1046V-Q1 トランシーバは、サーマル・シャットダウン (TSD)、TXD ドミナント・タイムアウト (DTO)、電源低電圧検出、最高 ±58V のバス・フォルト保護を含む多くの保護および診断機能も備えています。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TCAN1046V-Q1	VSON (14)	4.50mm × 3.00mm
	SOIC (14)	8.95mm × 3.91mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (December 2019) to Revision C (February 2022) — **Page**

- データシートから TCAN1048V-Q1 を削除 ... 1
- TCAN104xV-Q1 をすべて TCAN1046V-Q1 に変更 ... 1
- 「*特長*」に「機能安全対応」を追加 ... 1
- Deleted nSTB1 and nSTB2 pin from the *Pin Configuration and Functions* and throughout this document ... 3
- Changed the Test Conditions for $I_{OS(SS_DOM)}$ in the *Electrical Characteristics* table ... 7
- Deleted the "EMC requirements:" from the *Overview* secton ... 14
- Added footnotes to 表 8-1 ... 19
- Removed section Related Links from the ... 29

Changes from Revision A (August 2019) to Revision B (December 2019) — **Page**

- データシートの最初の公開リリース ... 1
- Changed 図 9-2 ... 24

Changes from Revision * (September 2018) to Revision A (August 2019) — **Page**

- データシートを*事前情報*から*量産データ*に変更 ... 1

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5 Pin Configuration and Functions

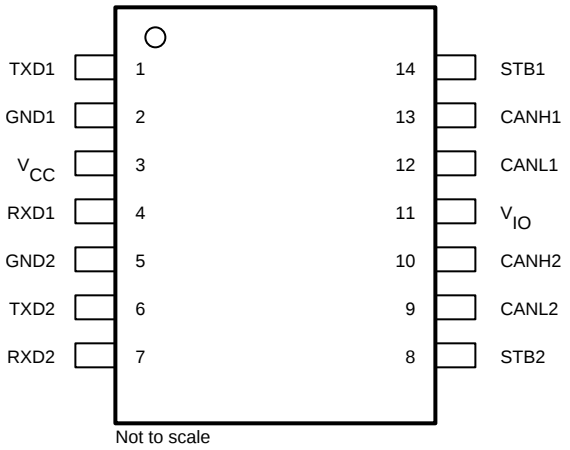


図 5-1. D (SOIC) Package, 14 Pin (Top View)

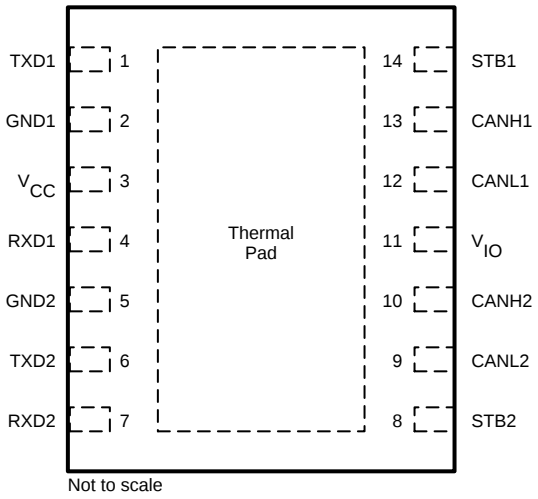


図 5-2. DMT (VSON) Package, 14 Pin (Top View)

表 5-1. Pin Functions

Pins		Type	Description
Name	No.		
TXD1	1	Digital Input	CAN transmit data input 1, integrated pull-up
GND1	2	GND	Ground connection
V_{CC}	3	Supply	5-V supply voltage
RXD1	4	Digital Output	CAN receive data output 1, tri-state when $V_{IO} < UV_{VIO}$
GND2	5	GND	Ground connection
TXD2	6	Digital Input	CAN transmit data input 2, integrated pull-up
RXD2	7	Digital Output	CAN receive data output 2, tri-state when $V_{IO} < UV_{VIO}$
STB2	8	Digital Input	Standby input 2 for mode control, integrated pull-up
CANL2	9	Bus IO	Low-level CAN bus 2 input or output line
CANH2	10	Bus IO	High-level CAN bus 2 input or output line
V_{IO}	11	Supply	IO supply voltage
CANL1	12	Bus IO	Low-level CAN bus 1 input or output line
CANH1	13	Bus IO	High-level CAN bus 1 input or output line
STB1	14	Digital Input	Standby input 1 for mode control, integrated pull-up
Thermal Pad (VSON only)		—	Electrically connected to GND, connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
V_{IO}	Supply voltage I/O level shifter	–0.3	6	V
V_{BUS}	CAN Bus IO voltage CANH1, CANL1 & CANH2, CANL2	–58	58	V
V_{DIFF}	Max differential voltage between CANH1, CANL1 & CANH2, CANL2	–45	45	V
V_{Logic_Input}	Logic input terminal voltage	–0.3	6	V
V_{RXD}	RXD output terminal voltage range (V_{RXD1}, V_{RXD2})	–0.3	6	V
$I_{O(RXD)}$	RXD output current (I_{ORXD1}, I_{ORXD2})	–8	8	mA
T_J	Operating virtual junction temperature range	–40	150	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential IO bus voltages, are with respect to ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	HBM classification level 3A for all pins	±3000	V
			HBM classification level 3B for global pins CANH & CANL	±10000	V
		Charged-device model (CDM), per AEC Q100-011 CDM classification level C5 for all pins		±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings - IEC Ratings

				VALUE	UNIT
V_{Tran}	ISO 7637-2 Transients immunity(1)	CAN bus terminals (CANH1, CANL1 and CANH2, CANL2) to GND	Pulse 1	–100	V
			Pulse 2a	75	V
			Pulse 3a	–150	V
			Pulse 3b	100	V
	ISO 7637-3 DCC transient immunity(2)		DCC slow transient pulse	±85	V

(1) Tested according to IEC 62228-3
(2) Tested according to ISO 7637-3 (2017); Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines

6.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IO}	Supply voltage for I/O level shifter	1.7		5.5	V
$I_{OH(RXD)}$	RXD terminal high level output current – $I_{OH(RXD1)}$ & $I_{OH(RXD2)}$	–2			mA
$I_{OL(RXD)}$	RXD terminal low level output current – $I_{OL(RXD1)}$ & $I_{OL(RXD2)}$			2	mA
T_A	Operating ambient temperature	–40		125	°C

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6.5 Thermal Characteristics

THERMAL METRIC[1]		TCAN1046V-Q1		UNIT
		D (SOIC)	DMT (VSON)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70.8	34.8	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33	38.2	℃/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.9	12.8	℃/W
Ψ_{JT}	Junction-to-top characterization parameter	5.9	2.0	℃/W
Ψ_{JB}	Junction-to-board characterization parameter	32.5	12.8	℃/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	3.1	℃/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Supply Characteristics

Over recommended operating conditions with T_A = -40℃ to 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Supply current normal mode	Dominant One channel[1]	TXDx = 0 V, TXDy = V_{IO} STB1 = STB2 = 0 V R_L = 60 Ω, C_L = open See 図 7-1		50	77.5	mA
			TXDx = 0 V, TXDy = V_{IO} STB1 = STB2 = 0 V R_L = 50 Ω, C_L = open See 図 7-1		55	87.5	mA
		Dominant Two channels	TXD1 = TXD2 = 0 V STB1 = STB2 = 0 V R_L = 60 Ω, C_L = open See 図 7-1		95	140	mA
			TXD1 = TXD2 = 0 V STB1 = STB2 = 0 V R_L = 50 Ω, C_L = open See 図 7-1		100	160	mA
		Recessive Two channels	TXD1 = TXD2 = V_{IO} STB1 = STB2 = 0 V R_L = 50 Ω, C_L = open See 図 7-1		10	15	mA
		Dominant with bus fault CANx, CANy recessive[1] [2]	TXDx = 0 V, TXDy = V_{IO} STB1 = STB2 = 0 V CANHx = CANLx = ±25 V R_{Lx} = open, R_{Ly} = 50 Ω, C_L = open See 図 7-1		90	137.5	mA
		Dominant with bus fault CANx, CANy dominant[2]	TXD1 = TXD2 = 0 V STB1 = STB2 = 0 V CANHx = CANLx = ±25 V R_{Lx} = open, R_{Ly} = 50 Ω, C_L = open See 図 7-1		135	210	mA
		Dominant with bus fault CANx and CANy[2]	TXD1 = TXD2 = 0 V STB1 = STB2 = 0 V CANH1 = CANL1 = ±25 V CANH2 = CANL2 = ±25 V R_{Lx} = R_{Ly} = open, C_L = open See 図 7-1		170	260	mA
	Supply current standby mode		TXD1 = TXD2 = V_{IO} STB1 = STB2 = V_{IO} R_L = 60 Ω, C_L = open See 図 7-1		0.4	2	µA

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6.6 Supply Characteristics (continued)

Over recommended operating conditions with T_A = -40℃ to 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{IO}	IO supply current normal mode	Dominant One channel(1)	TXDx = 0 V & TXDy = V_{IO} (2) STB1 = STB2 = 5 V RXD floating		150	348	µA
		Dominant Two channels	TXD1 = TXD2 = 0 V STB1 = STB2 = 5 V RXD floating		255	600	µA
		Recessive Two channels	TXD1 = TXD2 = V_{IO} STB1 = STB2 = 5 V RXD floating		50	96	µA
	IO supply current standby mode		TXD1 = TXD2 = V_{IO} STB1 = STB2 = V_{IO} RXD1 = RXD2 = floating		17	27	µA
UV_{VCC}	Rising under voltage detection on V_{CC} for protected mode				4.2	4.4	V
UV_{VCC}	Falling under voltage detection on V_{CC} for protected mode			3.5	4	4.25	V
UV_{VIO}	Rising under voltage detection on V_{IO}				1.56	1.65	V
UV_{VIO}	Falling under voltage detection on V_{IO}			1.4	1.51	1.59	V

(1) TXD1 and TXD2 are interchangeable for TXDx and TXDy
(2) CAN1 and CAN2 are interchangeable for CANx and CANy

6.7 Dissipation Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Average power dissipation one channel Normal mode	V_{CC} = 5 V, V_{IO} = 1.8 V, T_J= 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		130		mW
P_D	Average power dissipation one channel Normal mode	V_{CC} = 5 V, V_{IO} = 3.3 V, T_J= 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		130		mW
P_D	Average power dissipation one channel Normal mode	V_{CC} = 5 V, V_{IO} = 5 V, T_J= 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		130		mW
P_D	Average power dissipation one channel Normal mode	V_{CC} = 5.5 V, V_{IO} = 1.8 V, T_J= 150°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		140		mW
P_D	Average power dissipation one channel Normal mode	V_{CC} = 5.5 V, V_{IO} = 3.3 V, T_J= 150°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		140		mW
P_D	Average power dissipation one channel Normal mode	V_{CC} = 5.5 V, V_{IO} = 5 V, T_J= 150°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		140		mW
T_{TSD}	Thermal shutdown temperature			192		℃
T_{TSD_HYS}	Thermal shutdown hysteresis			10		

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6.8 Electrical Characteristics

Over recommended operating conditions with T_A = -40℃ to 125℃ (unless otherwise noted); CAN electrical parameters apply to both channels

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Electrical Characteristics							
$V_{O(DOM)}$	Dominant output voltage Normal mode	CANH	TXD = 0 V, STB = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open See 図 7-2 and 図 8-3,	2.75		4.5	V
		CANL		0.5		2.25	V
$V_{O(REC)}$	Recessive output voltage Normal mode	CANH and CANL	TXD = V_{IO}, STB = 0 V, R_L = open (no load), R_{CM} = open See 図 7-2 and 図 8-3	2	0.5 V_{CC}	3	V
V_{SYM}	Driver symmetry ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{CC}		STB = 0 V, R_L = 60 Ω, C_{SPLIT} = 4.7 nF, C_L = open, R_{CM} = open, TXD = 250 kHz, 1 MHz, 2.5 MHz See 図 7-2 and 図 9-2	0.9		1.1	V/V
V_{SYM_DC}	DC output symmetry (V_{CC} - $V_{O(CANH)}$ - $V_{O(CANL)}$)		STB = 0 V, R_L = 60 Ω, C_L = open See 図 7-2 and 図 8-3	–400		400	mV
$V_{OD(DOM)}$	Differential output voltage Normal mode Dominant	CANH - CANL	TXD = 0 V, STB = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open See 図 7-2 and 図 8-3	1.5		3	V
			TXD = 0 V, STB = 0 V, 45 Ω ≤ R_L ≤ 70 Ω, C_L = open See 図 7-2 and 図 8-3	1.4		3.3	V
			TXD = 0 V, STB = 0 V, R_L = 2240 Ω, C_L = open See 図 7-2 and 図 8-3	1.5		5	V
$V_{OD(REC)}$	Differential output voltage Normal mode Recessive	CANH - CANL	TXD = V_{IO}, STB = 0 V, R_L = 60 Ω, C_L = open See 図 7-2 and 図 8-3	–120		12	mV
			TXD = V_{IO}, STB = 0 V, R_L = open, C_L = open See 図 7-2 and 図 8-3	–50		50	mV
$V_{O(STB)}$	Bus output voltage Standby mode	CANH	STB = V_{IO}, R_L = open (no load) See 図 7-2 and 図 8-3	-0.1		0.1	V
		CANL		-0.1		0.1	V
		CANH - CANL		-0.2		0.2	V
$I_{OS(SS_DOM)}$	Short-circuit steady-state output current, dominant Normal mode		STB = 0 V, $V_{(CANH)}$ = -15 V to 40 V, CANL = open, TXD = 0 V See 図 7-7 and 図 8-3	–115			mA
			STB = 0 V, $V_{(CAN_L)}$ = -15 V to 40 V, CANH = open, TXD = 0 V See 図 7-7 and 図 8-3			115	mA
$I_{OS(SS_REC)}$	Short-circuit steady-state output current, recessive Normal mode		STB = 0 V, –27 V ≤ V_{BUS} ≤ 32 V, where V_{BUS} = CANH = CANL, TXD = V_{IO} See 図 7-7 and 図 8-3	–5		5	mA
Receiver Electrical Characteristics							
V_{IT}	Input threshold voltage Normal mode		STB = 0 V, -12 V ≤ V_{CM} ≤ 12 V See 図 7-3, 表 7-1, and 表 8-5	500		900	mV
$V_{IT(STB)}$	Input threshold Standby mode		STB = V_{IO}, -12 V ≤ V_{CM} ≤ 12 V See 図 7-3, 表 7-1, and 表 8-5	400		1150	mV
V_{DOM}	Dominant state differential input voltage range Normal mode		STB = 0 V, -12 V ≤ V_{CM} ≤ 12 V See 図 7-3, 表 7-1, and 表 8-5	0.9		9	V
V_{REC}	Recessive state differential input voltage range Normal mode		STB = 0 V, -12 V ≤ V_{CM} ≤ 12 V See 図 7-3, 表 7-1, and 表 8-5	-4		0.5	V
$V_{DOM(STB)}$	Dominant state differential input voltage range Standby mode		STB = V_{IO}, -12 V ≤ V_{CM} ≤ 12 V See 図 7-3, 表 7-1, and 表 8-5	1.15		9	V
$V_{REC(STB)}$	Recessive state differential input voltage range Standby mode		STB = V_{IO}, -12 V ≤ V_{CM} ≤ 12 V See 図 7-3, 表 7-1, and 表 8-5	-4		0.4	V
V_{HYS}	Hysteresis voltage for input threshold Normal mode		STB = 0 V, -12 V ≤ V_{CM} ≤ 12 V See 図 7-3, 表 7-1, and 表 8-5		100		mV
V_{CM}	Common mode range Normal and standby modes		See 図 7-3 and 表 8-5 表 8-5	–12		12	V

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6.8 Electrical Characteristics (continued)

Over recommended operating conditions with T_A = -40℃ to 125℃ (unless otherwise noted); CAN electrical parameters apply to both channels

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LKG(IOFF)}$	Unpowered bus input leakage current	CANH = CANL = 5 V, V_{CC} = V_{IO} = GND			5	µA
C_I	Input capacitance to ground (CANH or CANL)	TXD = V_{IO}(1)			20	pF
C_{ID}	Differential input capacitance				10	pF
R_{ID}	Differential input resistance	TXD = V_{IO}(1), STB = 0 V, -12 V ≤ V_{CM} ≤ 12 V	40		90	kΩ
R_{IN}	Single ended input resistance (CANH or CANL)		20		45	kΩ
TXD Terminal (CAN Transmit Data Input)						
V_{IH}	High-level input voltage		0.7 V_{IO}			V
V_{IL}	Low-level input voltage				0.3 V_{IO}	V
I_{IH}	High-level input leakage current	TXD = V_{CC} = V_{IO} = 5.5 V	–2.5	0	1	µA
I_{IL}	Low-level input leakage current	TXD = 0 V, V_{CC} = V_{IO} = 5.5 V	–200	-100	–20	µA
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 5.5 V, V_{CC} = V_{IO} = 0 V	–1	0	1	µA
RXD Terminal (CAN Receive Data Output)						
V_{OH}	High-level output voltage	I_O = –2 mA, See 図 7-3	0.8 V_{IO}			V
V_{OL}	Low-level output voltage	I_O = –2 mA, See 図 7-3			0.2 V_{IO}	V
STB Terminal (Standby Mode Input)						
V_{IH}	High-level input voltage		0.7 V_{IO}			V
V_{IL}	Low-level input voltage				0.3 V_{IO}	V
I_{IH}	High-level input leakage current	V_{CC} = V_{IO} = STB = 5.5 V	–2		2	µA
I_{IL}	Low-level input leakage current	V_{CC} = V_{IO} = 5.5 V, STB = 0 V	–20		–2	µA
$I_{LKG(OFF)}$	Unpowered leakage current	STB = 5.5V, V_{CC} = V_{IO} = 0 V	–1	0	1	µA

(1) V_{IO} = V_{CC} in non-V variants of device

6.9 Switching Characteristics

Over recommended operating conditions with T_A = -40℃ to 125℃ (unless otherwise noted); Timing parameters apply to both CAN channels

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	Normal mode, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF, V_{IO} = 2.8 V to 5.5 V, See 図 7-4		125	210	ns
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	Normal mode, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF, V_{IO} = 1.7 V, See 図 7-4		165	255	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive	Normal mode, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF, V_{IO} = 2.8 V to 5.5 V, See 図 7-4		150	210	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive	Normal mode, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF, V_{IO} = 1.7 V, See 図 7-4		180	255	ns
t_{MODE}	Mode change time, from normal to standby or from standby to normal	See 図 7-5			20	µs
t_{WK_FILTER}	Filter time for a valid wake-up pattern	See 図 8-5	0.5		1.8	µs
$t_{WK_TIMEOUT}$	Bus wake-up timeout	See 図 8-5	0.8		6	ms
Driver Switching Characteristics						

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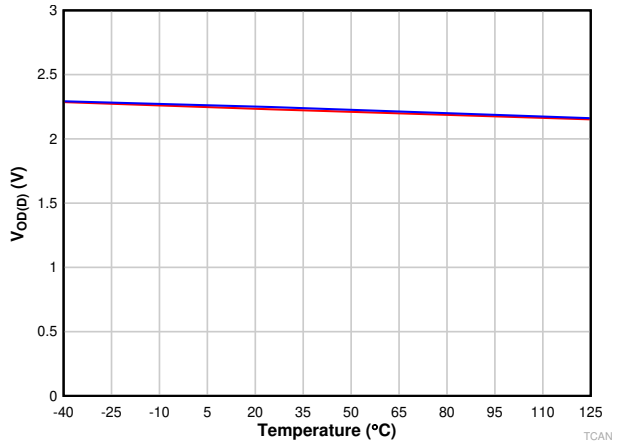
6.9 Switching Characteristics (continued)

Over recommended operating conditions with T_A = -40℃ to 125℃ (unless otherwise noted); Timing parameters apply to both CAN channels

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pHR}	Propagation delay time, high TXD to driver recessive (dominant to recessive)	STB = 0 V, R_L = 60 Ω, C_L = 100 pF See 図 7-2 and 図 7-6		80		ns
t_{pLD}	Propagation delay time, low TXD to driver dominant (recessive to dominant)			70		ns
$t_{sk(p)}$	Pulse skew (|tpHR - tpLD|)			20		ns
t_R	Differential output signal rise time			30		ns
t_F	Differential output signal fall time			50		ns
t_{TXD_DTO}	Dominant timeout		1.2		4.0	ms
Receiver Switching Characteristics						
t_{pRH}	Propagation delay time, bus recessive input to high output (dominant to recessive)	STB = 0 V, $C_{L(RXD)}$ = 15 pF See 図 7-3		90		ns
t_{pDL}	Propagation delay time, bus dominant input to low output (recessive to dominant)			65		ns
t_R	RXD output signal rise time			10		ns
t_F	RXD output signal fall time			10		ns
FD Timing Characteristics						
$t_{BIT(BUS)}$	Bit time on CAN bus output pins $t_{BIT(TXD)}$ = 500 ns	STB = 0 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$ See 図 7-4	450		530	ns
$t_{BIT(BUS)}$	Bit time on CAN bus output pins $t_{BIT(TXD)}$ = 200 ns		155		210	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins $t_{BIT(TXD)}$ = 500 ns		400		550	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins $t_{BIT(TXD)}$ = 200 ns		120		220	ns
t_{REC}	Receiver timing symmetry $t_{BIT(TXD)}$ = 500 ns		-50		20	ns
t_{REC}	Receiver timing symmetry $t_{BIT(TXD)}$ = 200 ns		-45		15	ns

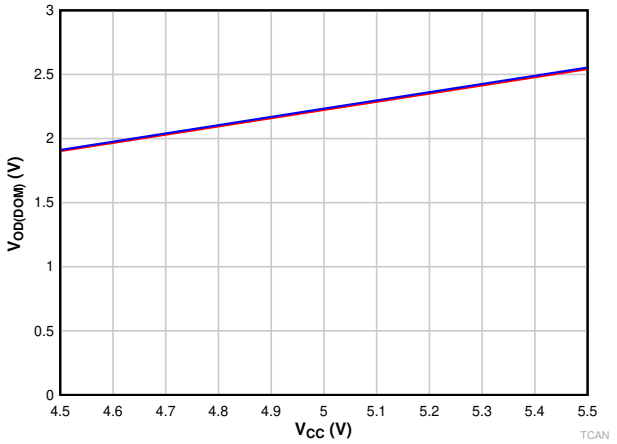
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6.10 Typical Characteristics



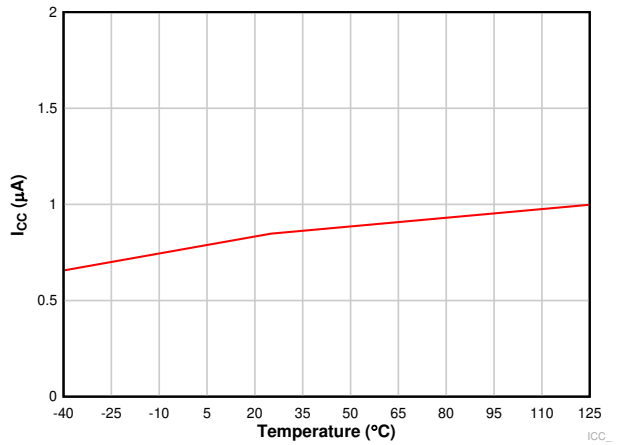
V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω

図 6-1. $V_{OD(DOM)}$ Over Temperature $V_{OD(DOM)}$ vs V_{CC} Transceiver 1 and Transceiver 2



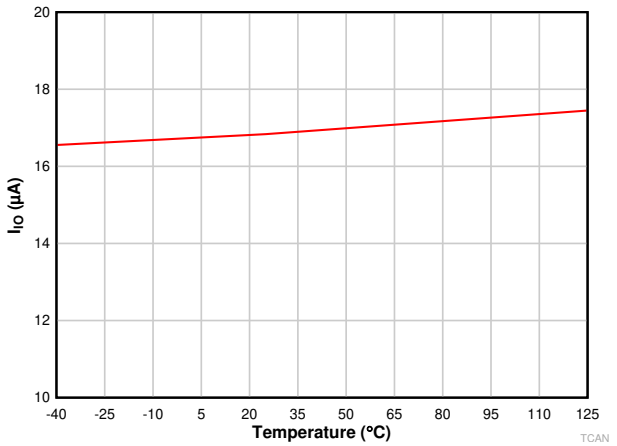
Temp = 25 °C R_L = 60 Ω

図 6-2. $V_{OD(DOM)}$ Over V_{CC} $V_{OD(DOM)}$ vs V_{CC} Transceiver 1 and Transceiver 2



V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω

図 6-3. I_{CC} Standby vs Temperature



V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω

図 6-4. I_{IO} Standby vs Temperature

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7 Parameter Measurement Information

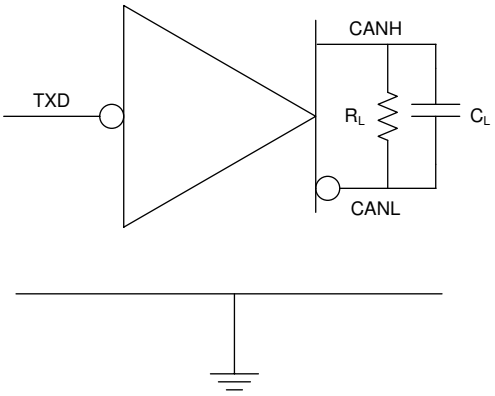


図 7-1. I_{CC} Test Circuit

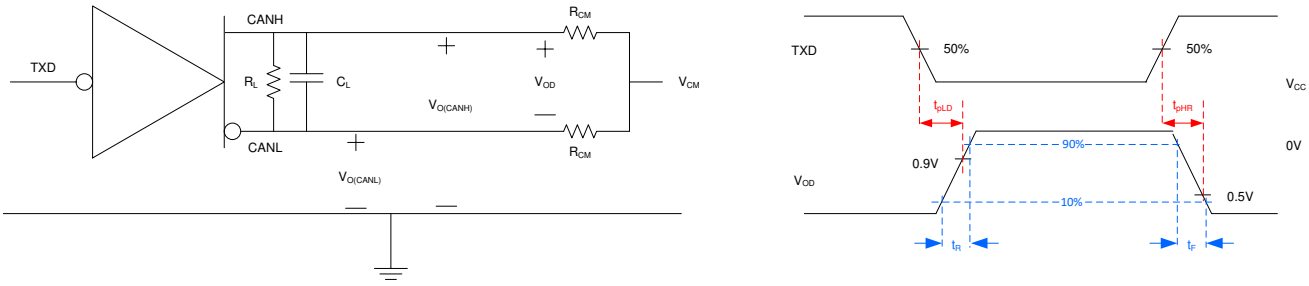


図 7-2. Driver Test Circuit and Measurement

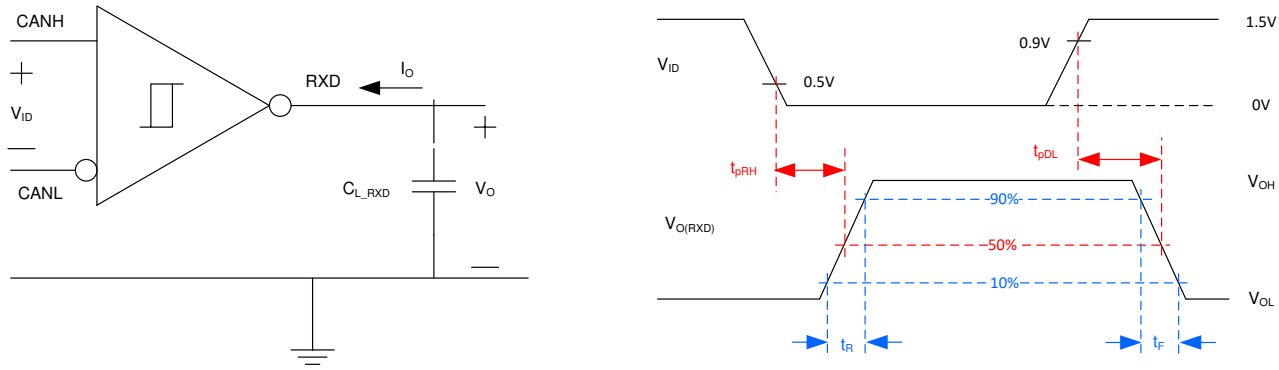


図 7-3. Receiver Test Circuit and Measurement

表 7-1. Receiver Differential Input Voltage Threshold Test

Input (See 図 7-3)			Output	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	RXD	
-11.5 V	-12.5 V	1000 mV	Low	V_{OL}
12.5 V	11.5 V	1000 mV		
-8.55 V	-9.45 V	900 mV		
9.45 V	8.55 V	900 mV		
-8.75 V	-9.25 V	500 mV	High	V_{OH}
9.25 V	8.75 V	500 mV		
-11.8 V	-12.2 V	400 mV		
12.2 V	11.8 V	400 mV		
Open	Open	X		

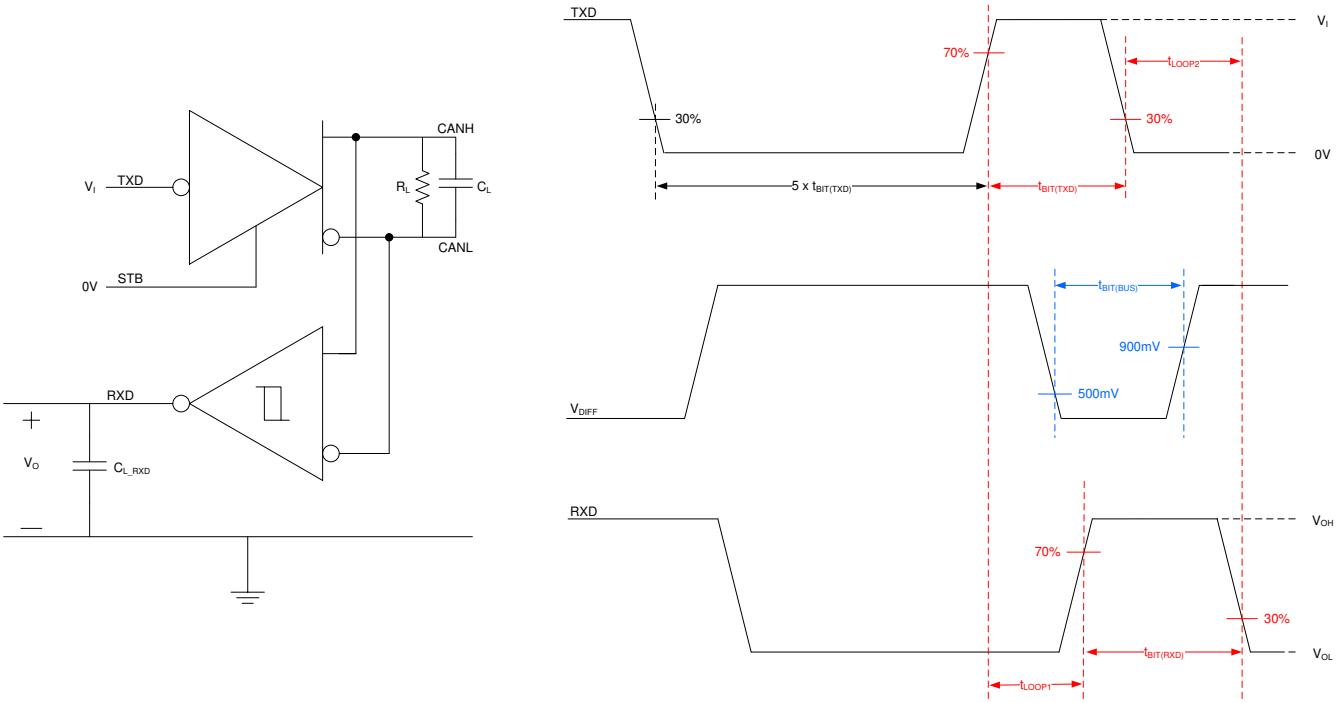


図 7-4. Transmitter and Receiver Timing Test Circuit and Measurement

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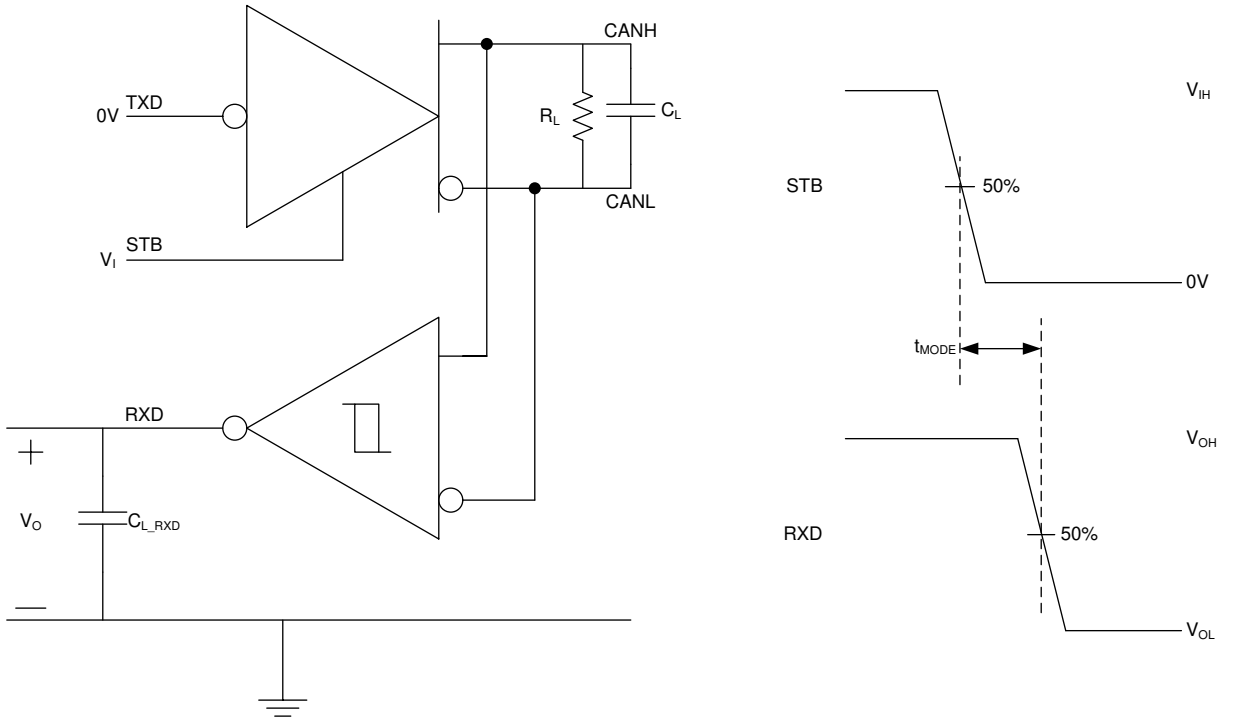


図 7-5. TCAN1046V-Q1 t_{MODE} Test Circuit and Measurement

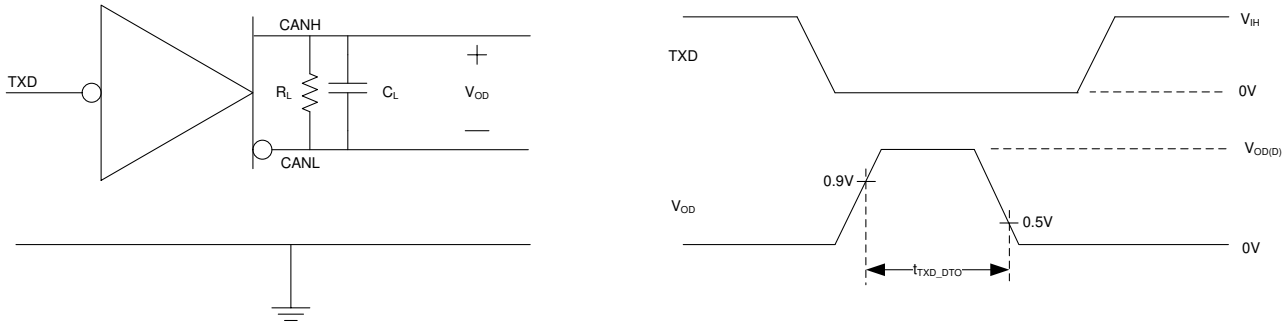


図 7-6. TXD Dominant Timeout Test Circuit and Measurement

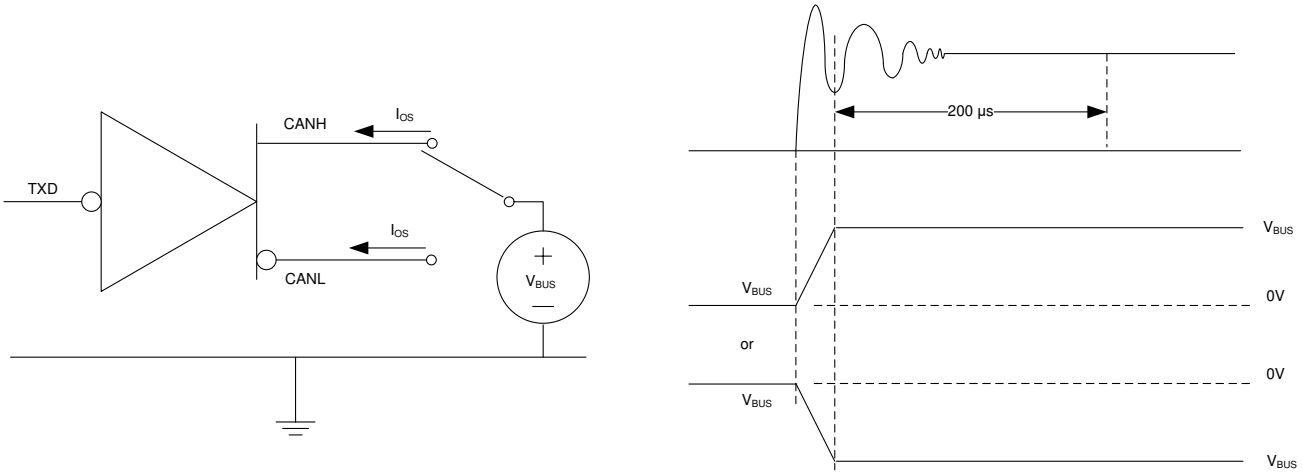


図 7-7. Driver Short-Circuit Current Test and Measurement

8 Detailed Description

8.1 Overview

The TCAN1046V-Q1 meets or exceeds the specifications of the ISO 11898-2:2016 high speed CAN (Controller Area Network) physical layer standard. The device has been certified to the requirements of ISO 11898-2:2016 and ISO 11898-5:2007 physical layer requirements according to the GIFT/ICT high speed CAN test specification. The transceiver provides a number of different protection features making it ideal for the stringent automotive system requirements while also supporting CAN FD data rates up to 8 Mbps.

The TCAN1046V-Q1 conforms to the following CAN standards:

- CAN transceiver physical layer standards:
  - ISO 11898-2:2016 High speed medium access unit
  - ISO 11898-5:2007 High speed medium access unit with low-power mode
  - SAE J2284-1: High Speed CAN (HSC) for Vehicle Applications at 125 kbps
  - SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250 kbps
  - SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500 kbps
  - SAE J2284-4: High-Speed CAN (HSC) for Vehicle Applications at 500 kbps with CAN FD Data at 2 Mbps
  - SAE J2284-5: High-Speed CAN (HSC) for Vehicle Applications at 500 kbps with CAN FD Data at 5 Mbps
  - ARINC 825-4 General Standardization of CAN (Controller Area Network) Bus Protocol For Airborne Use
- Conformance test requirements:
  - ISO 16845-2 Road vehicles – Controller area network (CAN) conformance test plan Part 2: High-speed medium access unit conformance test plan

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8.2 Functional Block Diagram

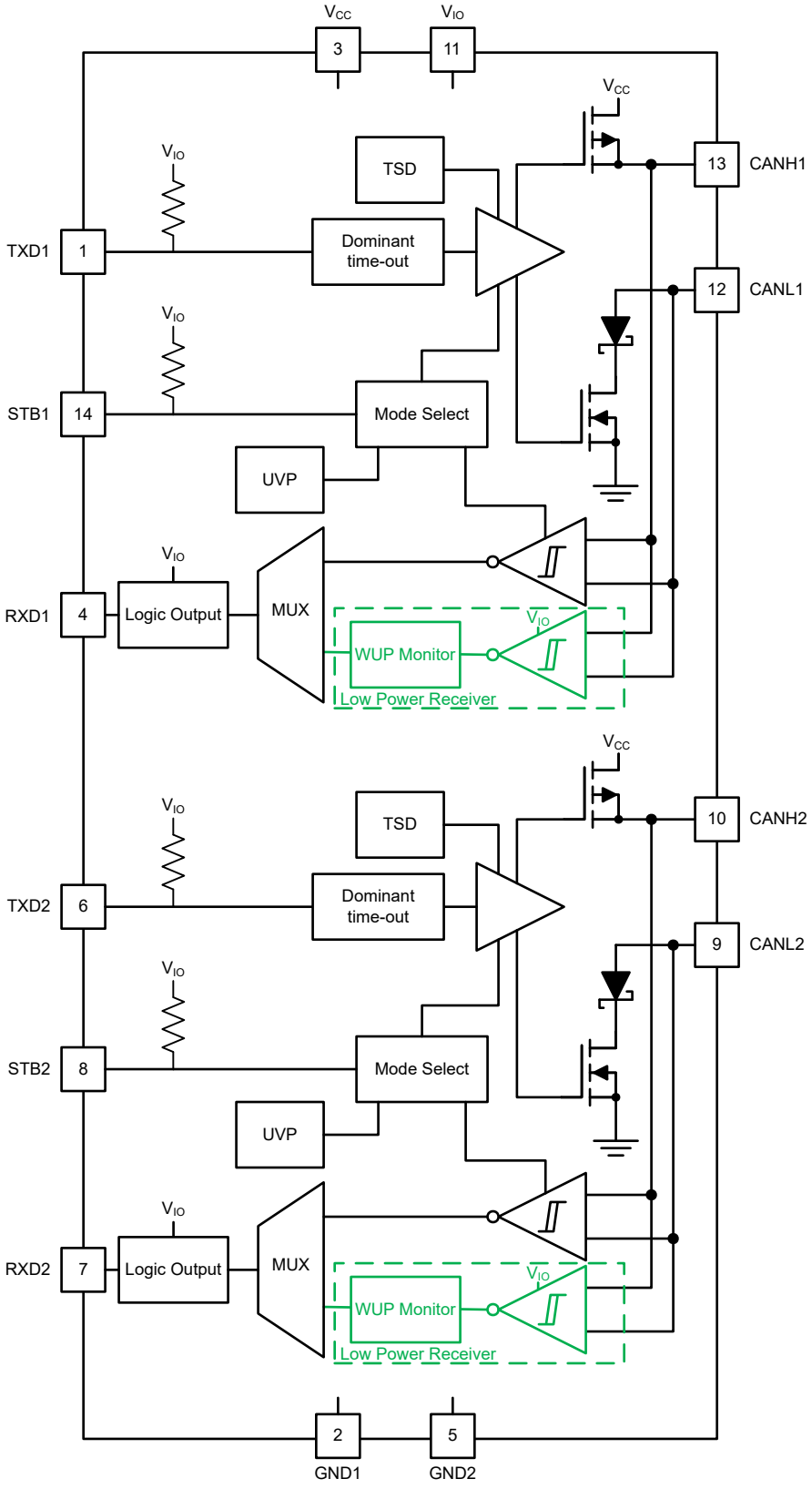


図 8-1. Block Diagram

8.3 Feature Description

8.3.1 Pin Description

8.3.1.1 TXD1 and TXD2

TXD1 and TXD2 are the logic-level signals, referenced to either V_{CC} or V_{IO}, from a CAN controller to the device.

8.3.1.2 GND1 and GND2

GND1 and GND2 are ground pins of the transceiver, both must be connected to the PCB ground.

8.3.1.3 V_{CC}

V_{CC} provides the 5-V power supply to the CAN transceiver.

8.3.1.4 RXD1 and RXD2

RXD1 and RXD2 are the logic-level signals, referenced to V_{IO}, from the TCAN1046V-Q1 to a CAN controller. This pin is only driven once V_{IO} is present.

8.3.1.5 V_{IO}

The V_{IO} pin provides the digital I/O voltage to match the CAN controller voltage thus avoiding the requirement for a level shifter. It supports voltages from 1.7 V to 5.5 V providing the widest range of controller support.

8.3.1.6 CANH and CANL

These are the CAN high and CAN low differential bus pins. These pins are connected to the CAN transceiver and the low-voltage WUP CAN receiver.

8.3.1.7 STB1 and STB2 (Standby)

The STB1 and STB2 pins are input pins used for mode control of the transceiver.

The TCAN1046V-Q1 implements STB1 and STB2 which can be supplied from either the system processor or from a static system voltage source. If normal mode is the only intended mode of operation than the STB pins can be tied directly to GND.

8.3.2 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See 図 8-2 and 図 8-3.

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD1, TXD2, RXD1 and RXD2 pins. A recessive bus state occurs when the bus is biased to V_{CC}/2 via the high-resistance internal input resistors R_{IN}) of the receiver and corresponds to a logic high on the TXD1, TXD2, RXD1 and RXD2 pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.

The TCAN1046V-Q1 transceiver implements a low-power standby (STB) mode which enables a third bus state where the bus pins are weakly biased to ground via the high resistance internal resistors of the receiver. See 図 8-2 and 図 8-3.

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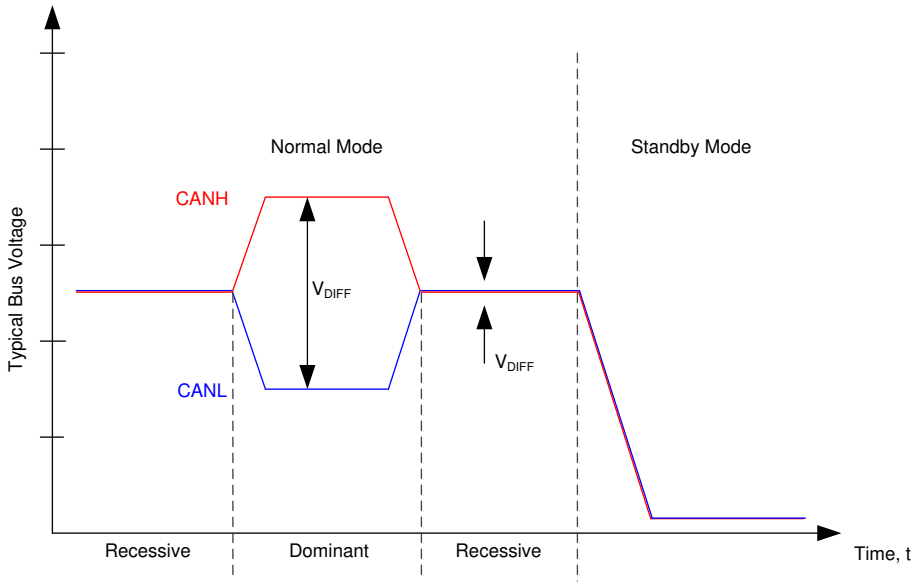
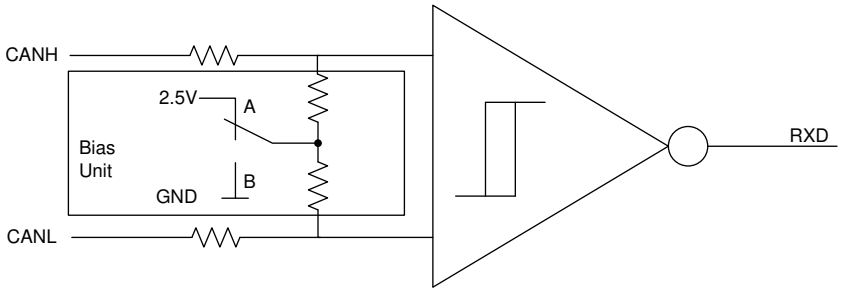


図 8-2. Bus States



A. Normal Mode
B. Standby Mode

図 8-3. Simplified Recessive Common Mode Bias Unit and Receiver

8.3.3 TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit, t_{TXD_DTO}, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin, thus clearing the dominant timeout. The receiver remains active and biased to $V_{CC}/2$ and the RXD output reflects the activity on the CAN bus during the TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using 式 1.

$$\text{Minimum Data Rate} = 11 \text{ bits} / t_{TXD_DTO} = 11 \text{ bits} / 1.2 \text{ ms} = 9.2 \text{ kbps} \quad (1)$$

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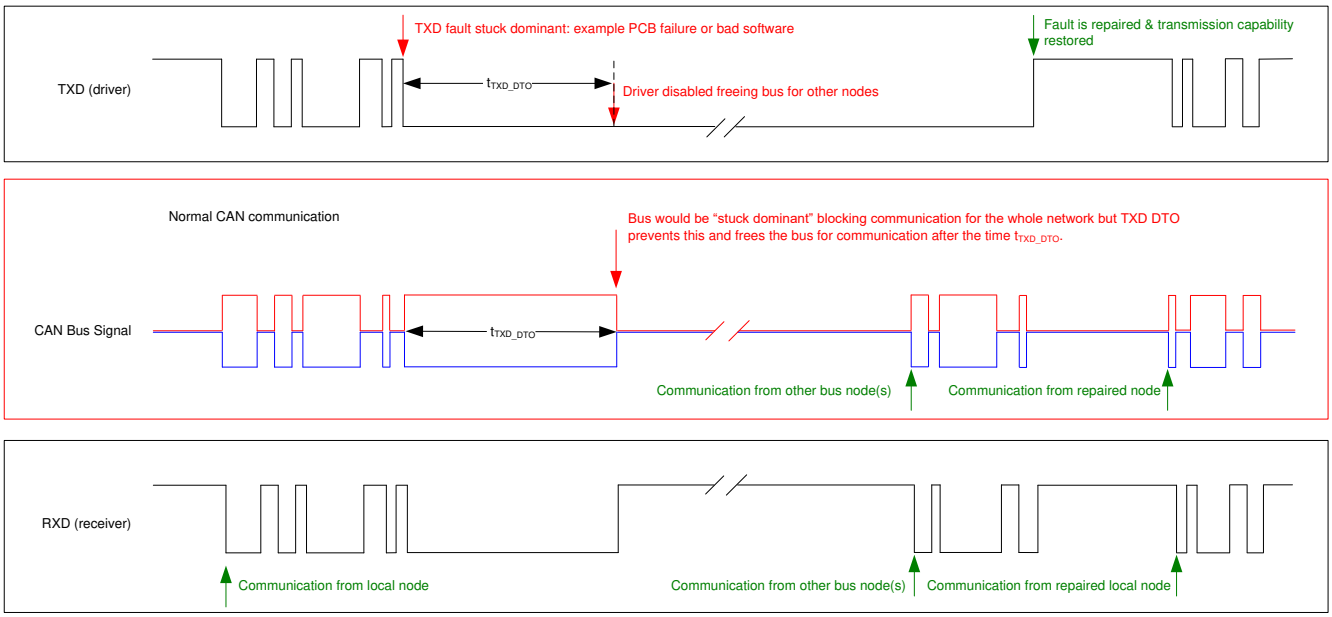


図 8-4. Example Timing Diagram for TXD Dominant Timeout

8.3.4 CAN Bus Short Circuit Current Limiting

The TCAN1046V-Q1 has several protection features that limit the short circuit current when a CAN bus line is shorted. These include CAN driver current limiting in the dominant and recessive states and TXD dominant state timeout which prevents permanently having the higher short circuit current of a dominant state in case of a system fault. During CAN communication the bus switches between the dominant and recessive states, thus the short circuit current may be viewed as either the current during each bus state or as a DC average current. When selecting termination resistors or a common mode choke for the CAN design the average power rating, $I_{OS(AVG)}$, should be used. The percentage dominant is limited by the TXD DTO and the CAN protocol which has forced state changes and recessive bits due to bit stuffing, control fields, and interframe space. These ensure there is a minimum amount of recessive time on the bus even if the data field contains a high percentage of dominant bits.

The average short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated using 式 2.

$$I_{OS(AVG)} = \%\ \text{Transmit} \times [(\%\ \text{REC_Bits} \times I_{OS(SS)_REC}) + (\%\ \text{DOM_Bits} \times I_{OS(SS)_DOM})] + [\%\ \text{Receive} \times I_{OS(SS)_REC}] \quad (2)$$

Where:

- $I_{OS(AVG)}$ is the average short circuit current
- % Transmit is the percentage the node is transmitting CAN messages
- % Receive is the percentage the node is receiving CAN messages
- % REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- % DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)_REC}$ is the recessive steady state short circuit current
- $I_{OS(SS)_DOM}$ is the dominant steady state short circuit current

This short circuit current and the possible fault cases of the network should be taken into consideration when sizing the power supply used to generate the transceivers V_{CC} supply.

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8.3.5 Thermal Shutdown (TSD)

If the junction temperature of the TCAN1046V-Q1 exceeds the thermal shutdown threshold, T_{TSD}, the device turns off the CAN driver circuitry and blocks the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below T_{TSD}. The CAN bus pins are biased to $V_{CC}/2$ during a TSD fault and the receiver to RXD path remains operational. The TCAN1046V-Q1 TSD circuit includes hysteresis which prevents the CAN driver output from oscillating during a TSD fault.

8.3.6 Undervoltage Lockout

The supply pins, V_{CC} and V_{IO}, have undervoltage detection that places the device into a protected state. This protects the bus during an undervoltage event on either supply pin.

表 8-1. Undervoltage Lockout - TCAN1046V-Q1

V_{CC}	V_{IO}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	> UV_{VIO}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	> UV_{VIO}	STB = V_{IO}: Standby mode	High impedance Weak pull-down to ground(1)	V_{IO}: Remote wake request(2)
		STB = GND: Protected mode		Recessive
> UV_{VCC}	< UV_{VIO}	Protected		High impedance
< UV_{VCC}	< UV_{VIO}	Protected		High impedance

(1) V_{CC} = GND, see $I_{LKG(OFF)}$
(2) See セクション 8.4.3.1

Once the undervoltage condition is cleared and t_{MODE} has expired the TCAN1046V-Q1 transitions to normal mode and the host controller can send and receive CAN traffic again.

8.3.7 Unpowered Device

The TCAN1046V-Q1 is designed to be an ideal passive or no load to the CAN bus if the device is unpowered. The bus pins were designed to have low leakage currents when the device is unpowered, so they do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational.

The logic pins also have low leakage currents when the device is unpowered, so they do not load other circuits which may remain powered.

8.3.8 Floating pins

The TCAN1046V-Q1 has internal pull-ups or pull-downs on critical pins which place the device into known states if the pin floats. This internal bias should not be relied upon by design though, especially in noisy environments, but instead should be considered a failsafe protection feature.

When a CAN controller supporting open-drain outputs is used an adequate external pull-up resistor must be chosen. This ensures that the TXD output of the CAN controller maintains acceptable bit time to the input of the CAN transceiver. See 表 8-2 for details on pin bias conditions.

表 8-2. Pin Bias

Pin	Pull-up or Pull-down	Comment
TXD1 and TXD2	Pull-up	Weakly biases TXD1 and TXD2 towards recessive to prevent bus blockage or TXD DTO triggering
STB1 and STB2	Pull-up	Weakly biases STB1 and STB2 towards low-power standby mode to prevent excessive system power

8.4 Device Functional Modes

8.4.1 Operating Modes

The TCAN1046V-Q1 has two main operating modes; normal mode and standby mode. Operating mode selection is made by applying a high or low level to the STB pin on the device.

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表 8-3. Operating Modes

STB	Device Mode	Driver	Receiver	RXD Pin
High	Standby mode	Disabled	Low-power receiver with bus monitor enable	High (recessive) until valid WUP is received See section 8.3.3.1
Low	Normal Mode	Enabled	Enabled	Mirrors bus state

8.4.2 Normal Mode

This is the normal operating mode of the TCAN1046V-Q1. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on the TXD1 and TXD2 inputs to a differential output on the CANH1, CANL1 and CANH2, CANL2 bus pins. The receiver is translating the differential signal from CANH1, CANL1 and CANH2, CANL2 to a digital output on the RXD1 and RXD2 outputs.

8.4.3 Standby Mode

This is the low-power mode of the TCAN1046V-Q1. The CAN driver and main receiver are switched off and bi-directional CAN communication is not possible. The low-power receiver and bus monitor circuits are enabled to allow for RXD wake-up requests via the CAN bus. A wake-up request is output to RXD1 or RXD2 depending on the channel which received the WUP as shown in 図 8-5. The local CAN protocol controller should monitor RXD1 and RXD2 for transitions (high-to-low) and reactivate the device to normal mode by pulling the STB1 and STB2 pin low. The CAN bus pins are weakly pulled to GND in this mode; see 図 8-2 and 図 8-3.

In standby mode, only the V_{IO} supply is required therefore the V_{CC} may be switched off for additional system level current savings.

8.4.3.1 Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

The TCAN1046V-Q1 supports a remote wake-up request that is used to indicate to the host controller that the bus is active and the node should return to normal operation.

The device uses the multiple filtered dominant wake-up pattern (WUP) from the ISO 11898-2:2016 standard to qualify bus activity. Once a valid WUP has been received, the wake request is indicated to the controller by a falling edge and low period corresponding to a filtered dominant on the RXD1 or RXD2 output of the TCAN1046V-Q1.

The WUP consists of a filtered dominant pulse, followed by a filtered recessive pulse, and finally by a second filtered dominant pulse. The first filtered dominant initiates the WUP, and the bus monitor then waits on a filtered recessive; other bus traffic does not reset the bus monitor. Once a filtered recessive is received the bus monitor is waiting for a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon reception of the second filtered dominant the bus monitor recognizes the WUP and drives the RXD1 or RXD2 output low every time an additional filtered dominant signal is received from the bus.

For a dominant or recessive to be considered filtered, the bus must be in that state for more than the t_{WK_FILTER} time. Due to variability in t_{WK_FILTER} the following scenarios are applicable. Bus state times less than $t_{WK_FILTER(MIN)}$ are never detected as part of a WUP and thus no wake request is generated. Bus state times between $t_{WK_FILTER(MIN)}$ and $t_{WK_FILTER(MAX)}$ may be detected as part of a WUP and a wake-up request may be generated. Bus state times greater than $t_{WK_FILTER(MAX)}$ are always detected as part of a WUP, and thus a wake request is always generated. See 図 8-5 for the timing diagram of the wake-up pattern.

The pattern and t_{WK_FILTER} time used for the WUP prevents noise and bus stuck dominant faults from causing false wake-up requests while allowing any valid message to initiate a wake-up request.

The ISO 11898-2:2016 standard has defined times for a short and long wake-up filter time. The t_{WK_FILTER} timing for the device has been picked to be within the minimum and maximum values of both filter ranges. This timing has been chosen such that a single bit time at 500 kbps, or two back-to-back bit times at 1 Mbps triggers the filter in either bus state. Any CAN frame at 500 kbps or less would contain a valid WUP.

For an additional layer of robustness and to prevent false wake-ups, the device implements a wake-up timeout feature. For a remote wake-up event to successfully occur, the entire WUP must be received within the timeout value $t \leq t_{WK_TIMEOUT}$. If not, the internal logic is reset and the transceiver remains in its current state without

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waking up. The full pattern must then be transmitted again, conforming to the constraints mentioned in this section. See 図 8-5 for the timing diagram of the wake-up pattern with wake timeout feature.

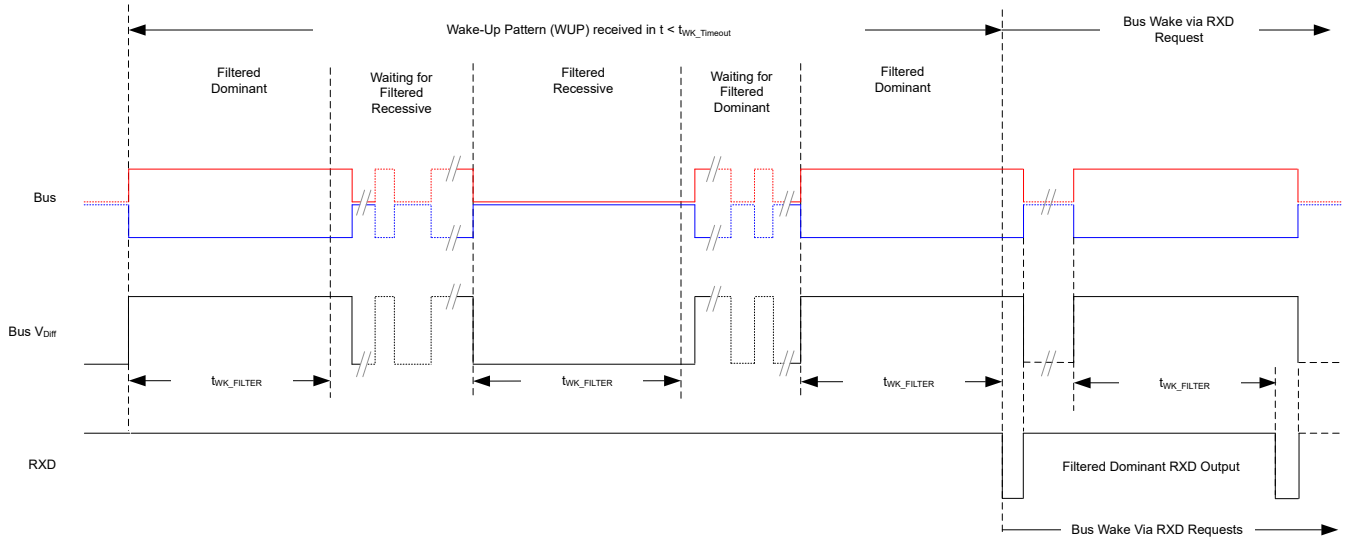


図 8-5. Wake-Up Pattern (WUP) with $t_{WK_TIMEOUT}$

8.4.4 Driver and Receiver Function

The digital logic input and output levels for the TCAN1046V-Q1 are CMOS levels with respect to V_{IO} for compatibility with protocol controllers having 1.8 V, 2.5 V, 3.3 V, or 5 V I/O levels.

表 8-4. Driver Function Table

Device Mode	TXD Input(1)	Bus Outputs		Driven Bus State(2)
		CANH	CANL	
Normal	Low	High	Low	Dominant
	High or open	High impedance	High impedance	Biased recessive
Standby	X	High impedance	High impedance	Biased to ground

(1) X = irrelevant
(2) For bus state and bias see 図 8-2 and 図 8-3

表 8-5. Receiver Function Table Normal and Standby Mode

Device Mode	CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus State	RXD Pin
Normal	$V_{ID} \geq 0.9$ V	Dominant	Low
	0.5 V < V_{ID} < 0.9 V	Undefined	Undefined
	$V_{ID} \leq 0.5$ V	Recessive	High
Standby	$V_{ID} \geq 1.15$ V	Dominant	High Low if a remote wake event occurred See 図 8-5
	0.4 V < V_{ID} < 1.15 V	Undefined	
	$V_{ID} \leq 0.4$ V	Recessive	
Any	Open ($V_{ID} \approx 0$ V)	Open	High

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9 Application and Implementation

Note

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9.1 Application Information

9.2 Typical Application

The TCAN1046V-Q1 transceiver can be used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. 図 9-1 shows a typical configuration for 5 V controller applications. The bus termination is shown for illustrative purposes.

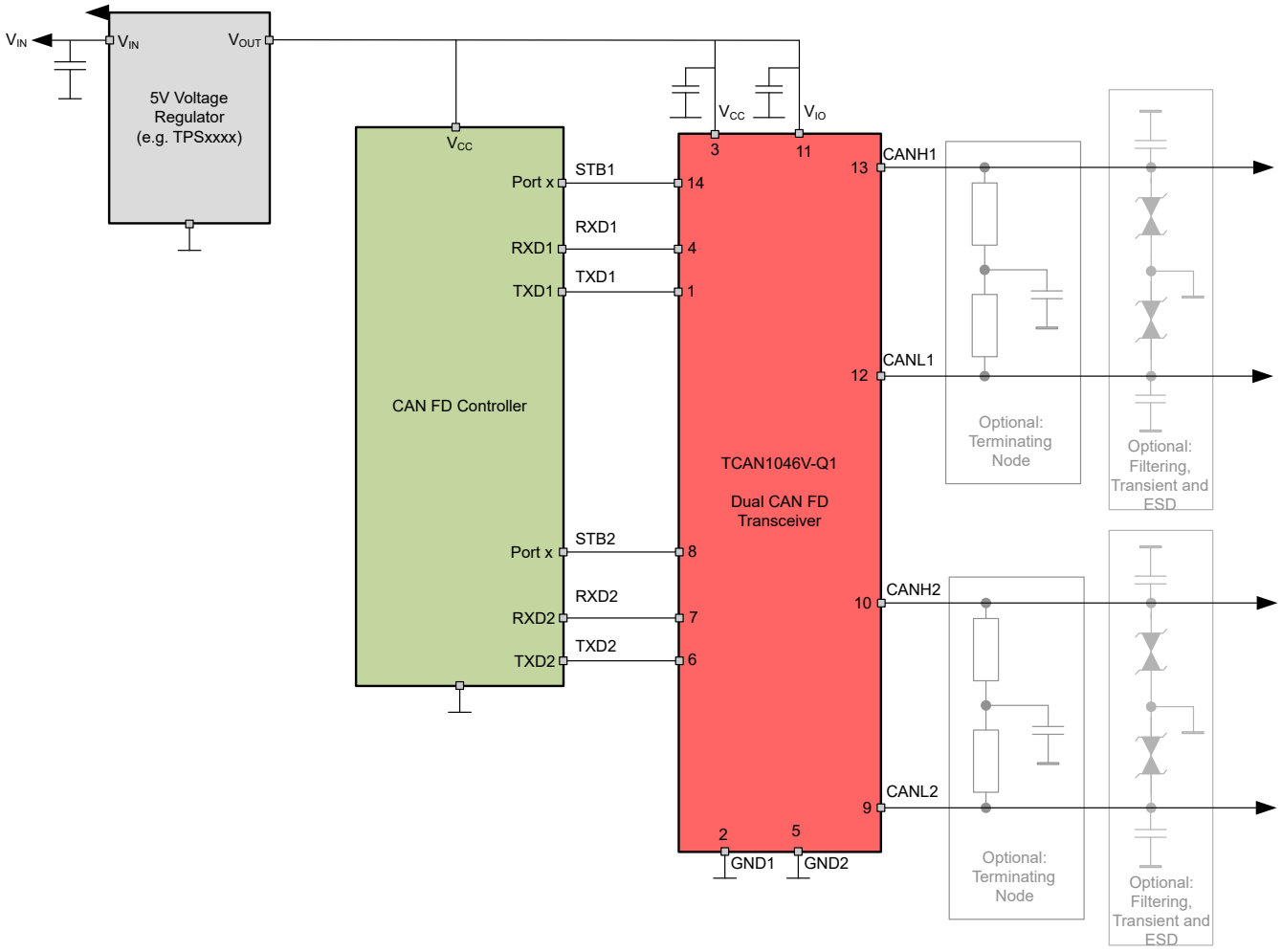


図 9-1. Transceiver Application Using 5 V I/O Connections

9.2.1 Design Requirements

9.2.1.1 CAN Termination

Termination may be a single 120-Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired then split termination may be used, see 図 9-2. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

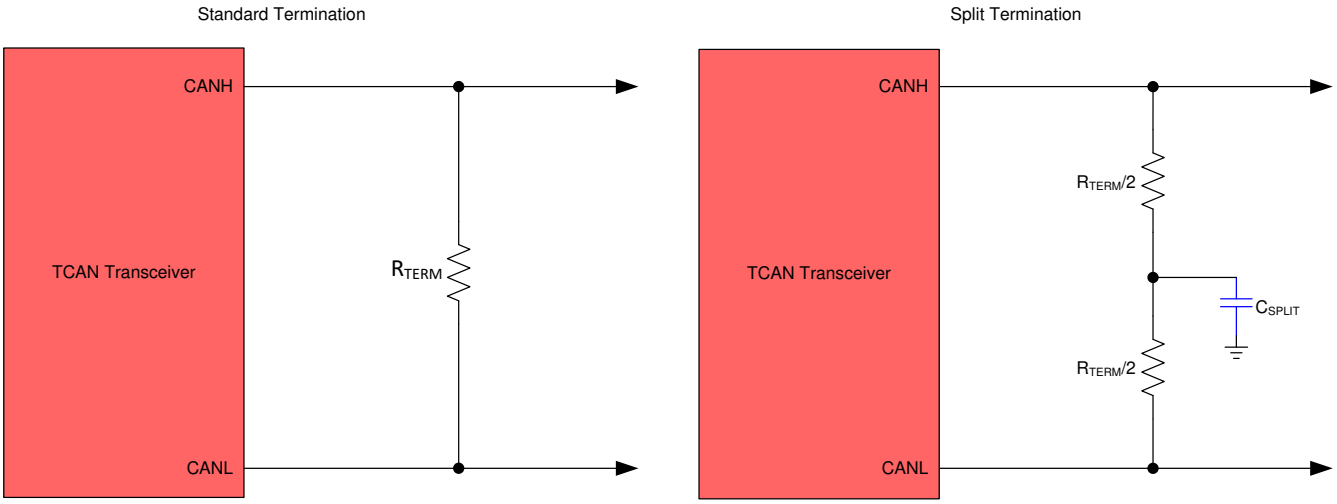


図 9-2. CAN Bus Termination Concepts

9.2.2 Detailed Design Procedures

9.2.2.1 Bus Loading, Length and Number of Nodes

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN1046V-Q1.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2016 specification the driver differential output is specified with a bus load that can range from 50 Ω to 65 Ω where the differential output must be greater than 1.5 V. The TCAN1046V-Q1 family is specified to meet the 1.5 V requirement down to 50 Ω and is specified to meet 1.4 V differential output at 45Ω bus load. The differential input resistance of the TCAN1046V-Q1 is a minimum of 40 kΩ. If 100 TCAN1046V-Q1 transceivers are in parallel on a bus, this is equivalent to a 400-Ω differential load in parallel with the nominal 60 Ω bus termination which gives a total bus load of approximately 52 Ω. Therefore, the TCAN1046V-Q1 family theoretically supports over 100 transceivers on a single bus segment. However, for a CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility, the CAN network system designer must take the responsibility of good network design to ensure robust network operation.

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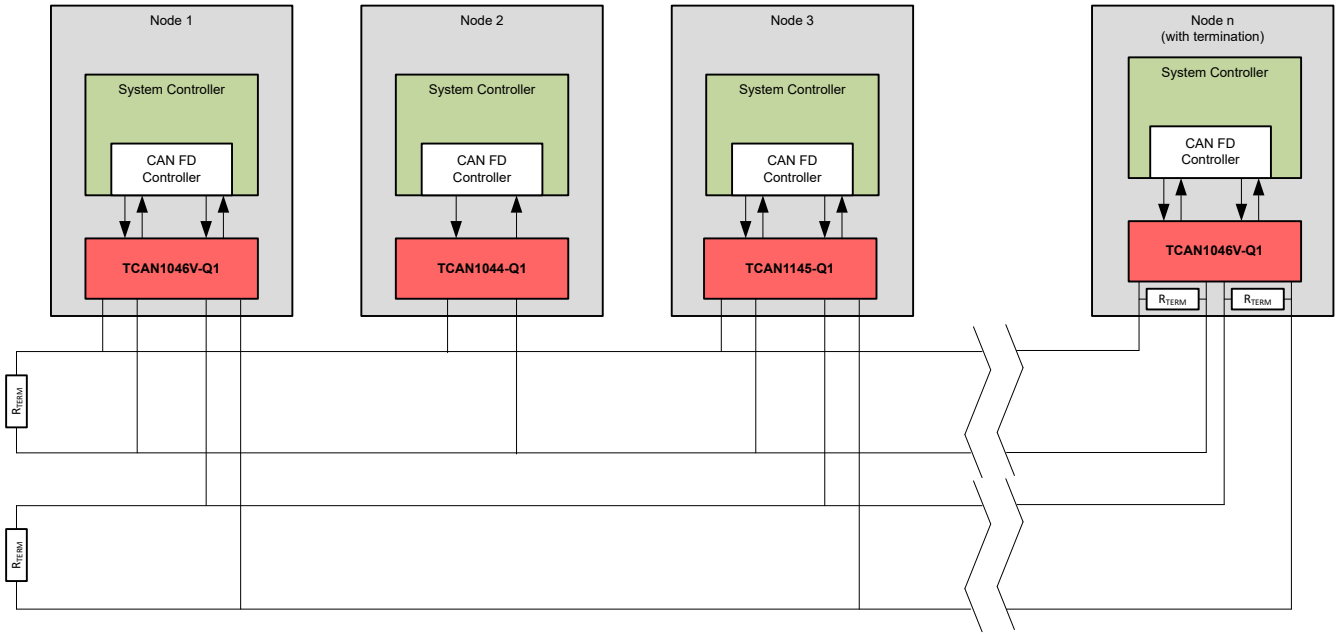
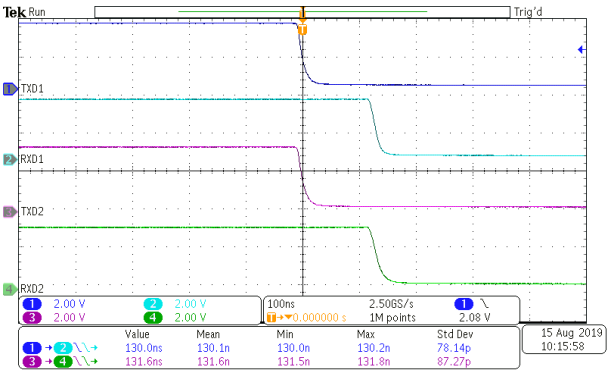


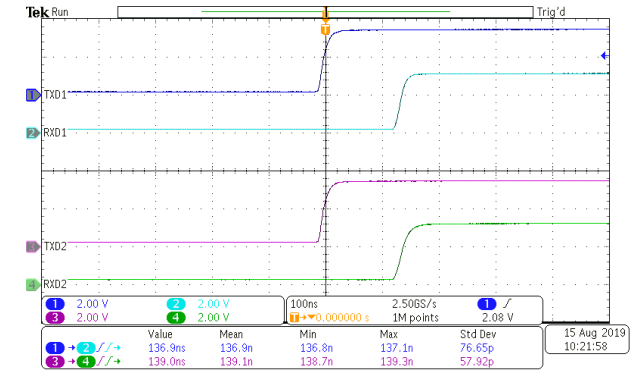
図 9-3. Typical CAN Bus

9.2.3 Application Curves



V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω

図 9-4. $t_{PROP(LOOP1)}$ TRX1 & TRX2



A. V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω

図 9-5. $t_{PROP(LOOP2)}$ TRX1 & TRX2

9.3 System Examples

The TCAN1046V-Q1 CAN transceiver is typically used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. A 1.8 V, 2.5 V, or 3.3 V application is shown in 図 9-6. The bus termination is shown for illustrative purposes.

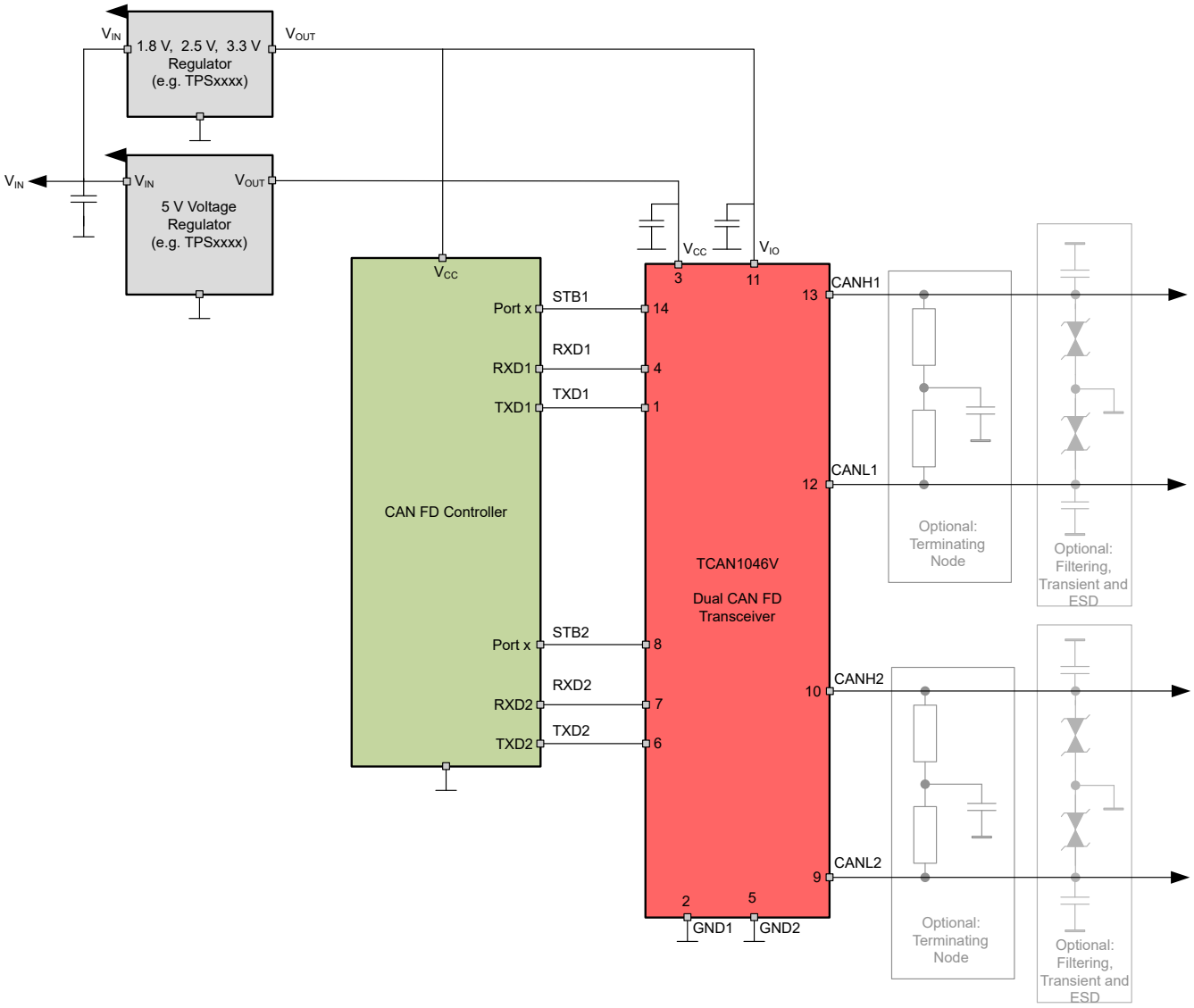


図 9-6. Transceiver Application Using 1.8 V, 2.5 V, 3.3 V I/O Connections

10 Power Supply Recommendations

The TCAN1046V-Q1 device is designed to operate with a main V_{CC} input voltage supply range between 4.5 V and 5.5 V. The device has an IO level shifting supply input, V_{IO}, designed for a range between 1.8 V and 5.5 V. Both supply inputs must be well regulated. A decoupling capacitor, typically 100 nF, should be placed near the CAN transceiver's main V_{CC} and V_{IO} supply pins in addition to bypass capacitors.

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11 Layout

Robust and reliable CAN node design may require special layout techniques depending on the application and automotive design requirements. Since transient disturbances have high frequency content and a wide bandwidth, high-frequency layout techniques should be applied during PCB design.

11.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connectors, J1 and J2, to prevent transients, ESD, and noise from propagating onto the board. This layout example shows optional transient voltage suppression (TVS) diodes, D1 and D2, which may be implemented if the system-level requirements exceed the specified rating of the transceiver. This example also shows optional bus filter capacitors C6, C8, C9, and C11.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

Note

High frequency current follows the path of least impedance and not the path of least resistance.

- This layout example shows how split termination could be implemented on the CAN node. The termination is split into two pairs of resistors, R8, R9, R10, and R11, with the center or split tap of the termination connected to ground via capacitors C7 and C10. Split termination provides common mode filtering for the bus. See セクション 9.2.1.1, セクション 8.3.4, and 式 2 for information on termination concepts and power ratings needed for the termination resistor(s).
- To limit current of digital lines series resistors may be used. Examples are R2, R3, R5, R6, R7, and R12.
- Pin 1 and pin 6 are shown for the TXD1 and TXD2 inputs of the device with R1 and R4 as optional pull-up resistors. If an open drain host controller is used this is mandatory to ensure the bit timing into the device is met.
- Pin 8 and 14 are shown assuming the mode pin STB is used. If the device is only used in normal mode then only a pull-down resistor is needed.

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11.2 Layout Example

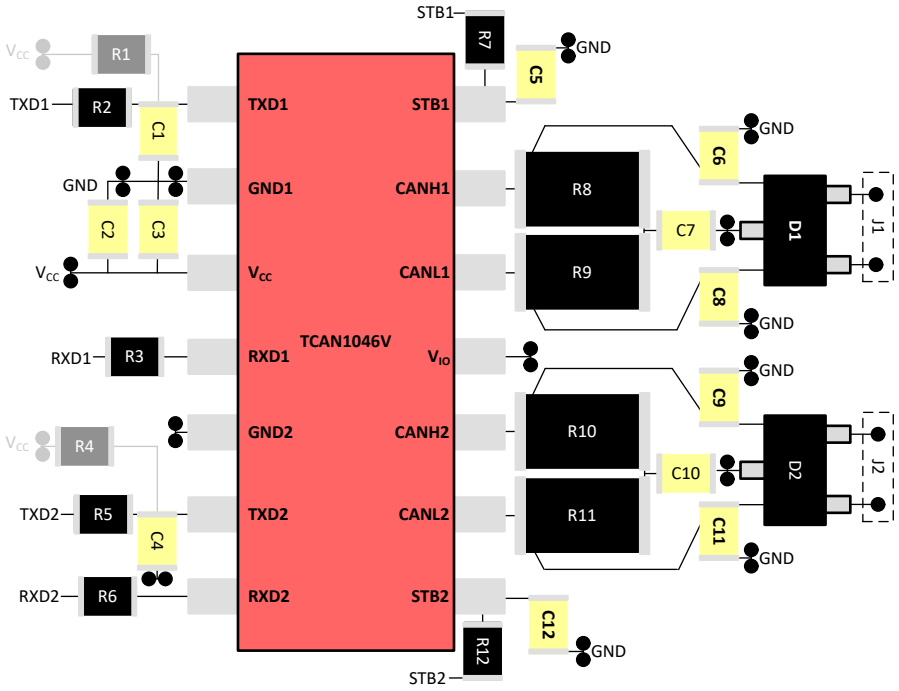


図 11-1. Example Layout

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12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCAN1046VDMTRQ1	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	1046V
TCAN1046VDMTRQ1.A	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1046V

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

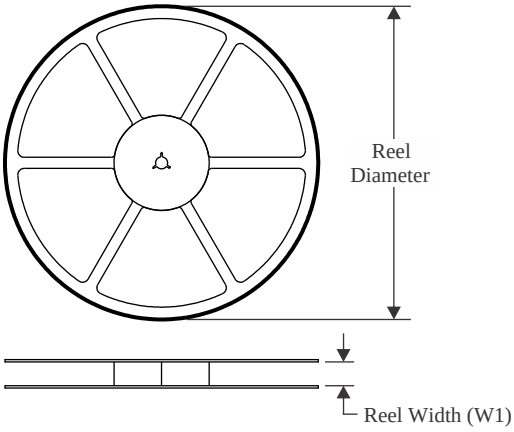
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

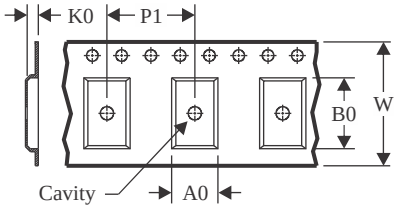
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

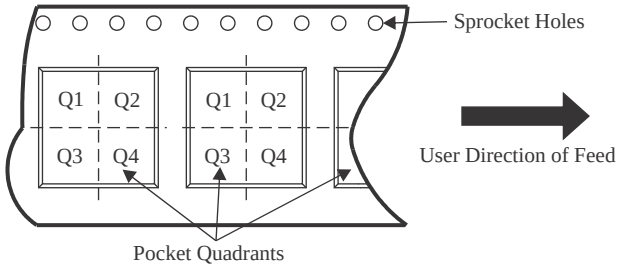


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

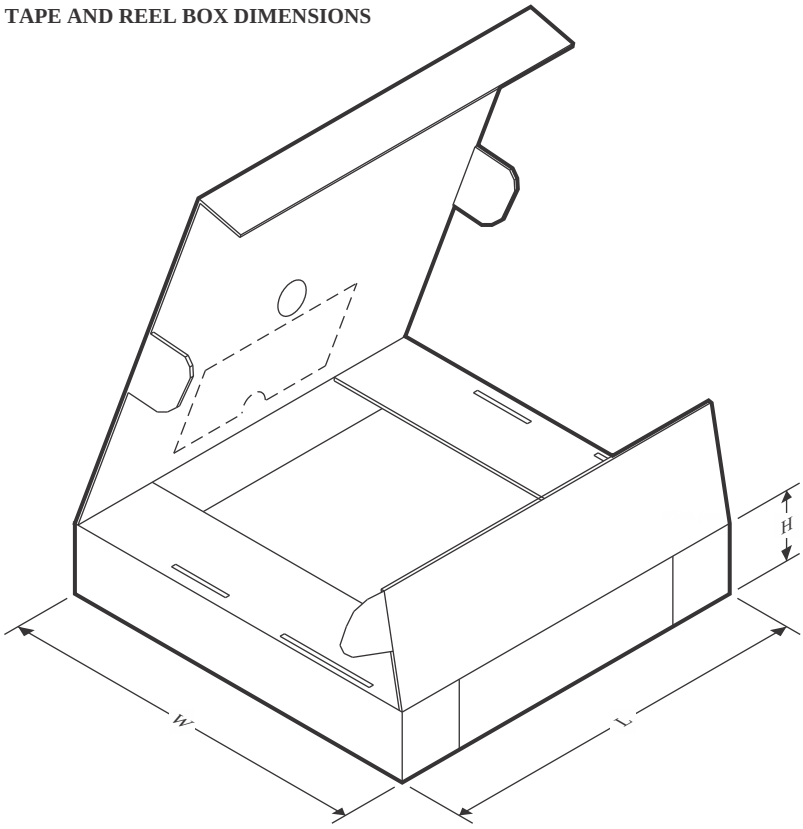
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1046VDMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.2	4.7	1.15	8.0	12.0	Q1
TCAN1046VDMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TCAN1046VDMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1046VDMTRQ1	VSON	DMT	14	3000	367.0	367.0	38.0
TCAN1046VDMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0
TCAN1046VDMTRQ1	VSON	DMT	14	3000	346.0	346.0	33.0

GENERIC PACKAGE VIEW

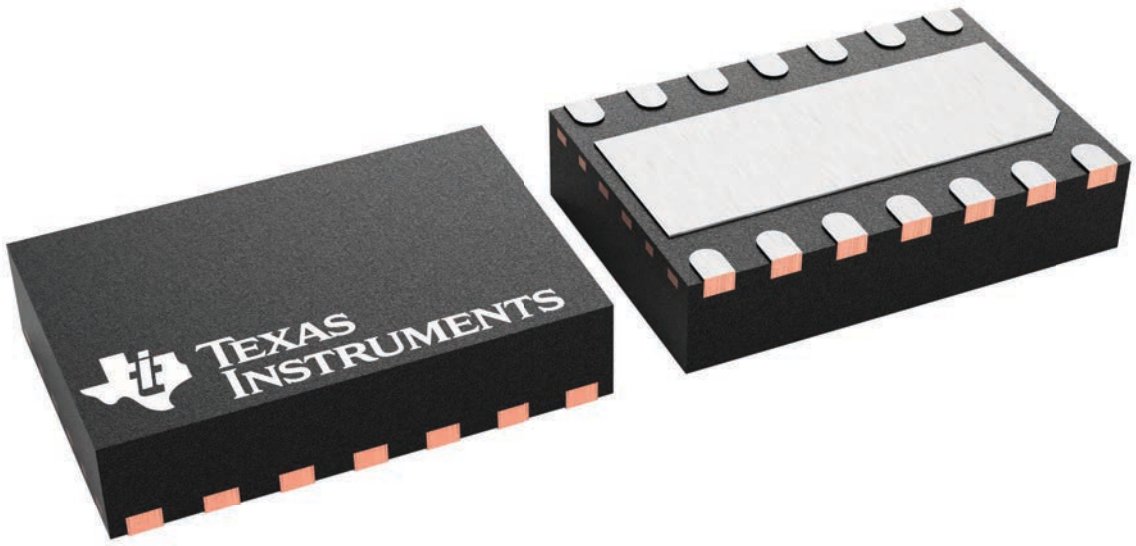
DMT 14

VSON - 0.9 mm max height

3 x 4.5, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



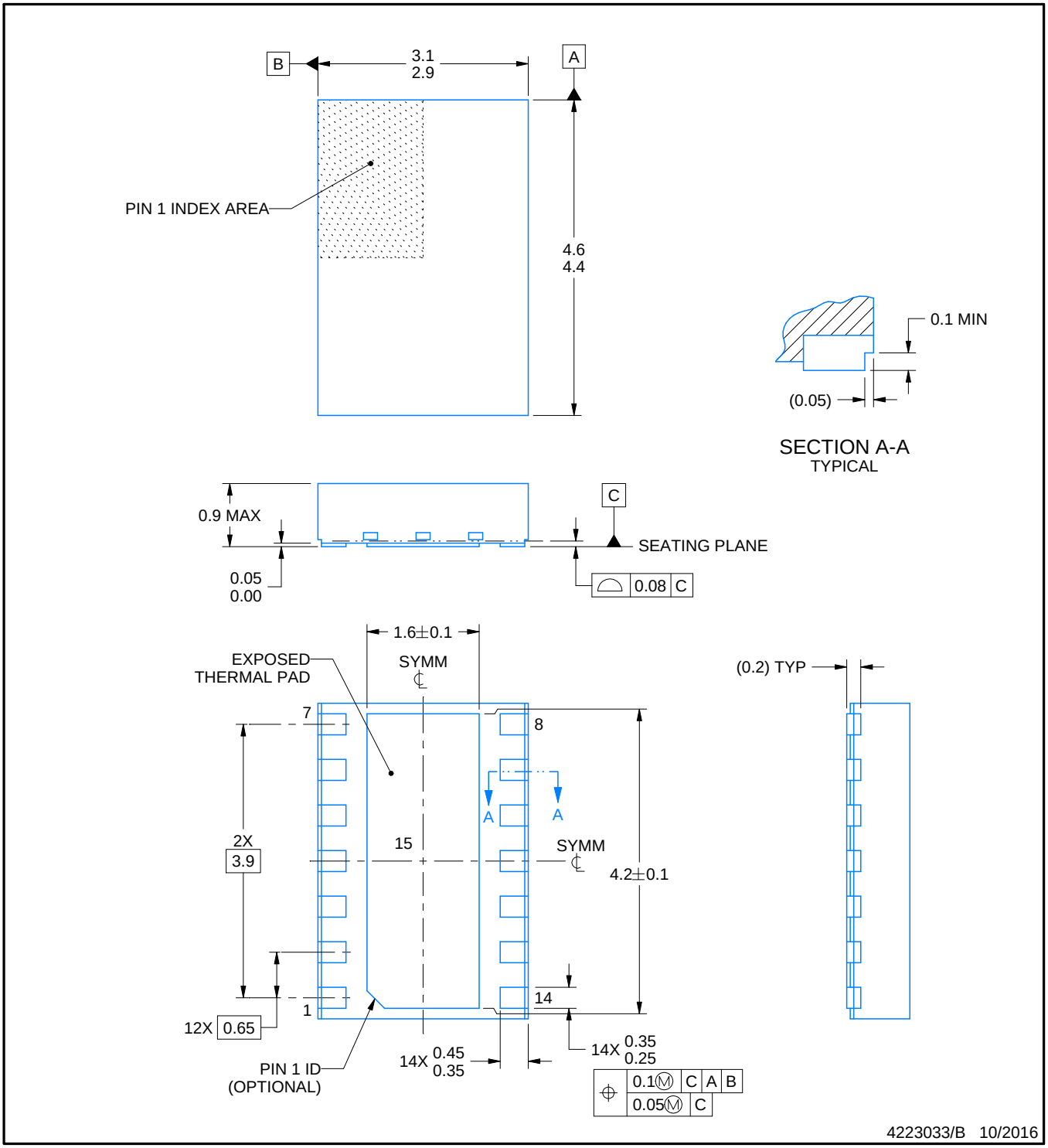
4225088/A

PACKAGE OUTLINE

DMT0014A

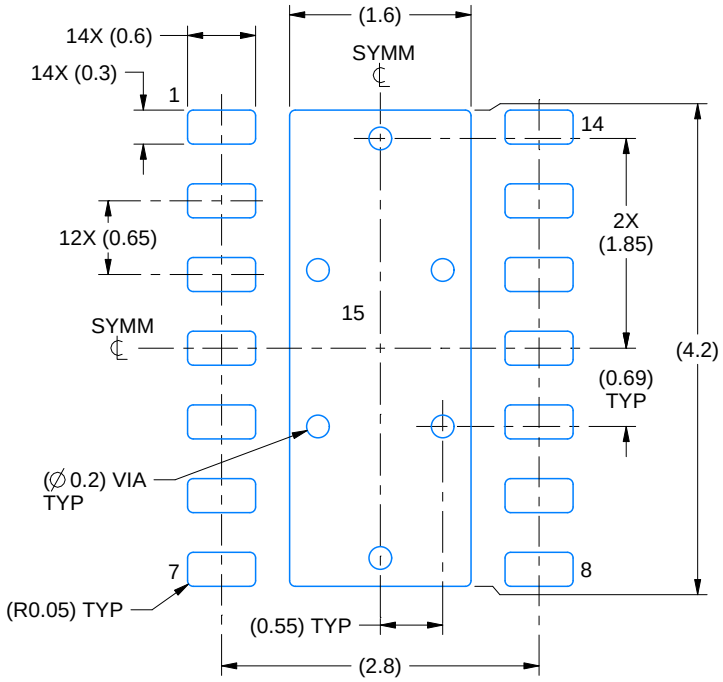
VSON - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

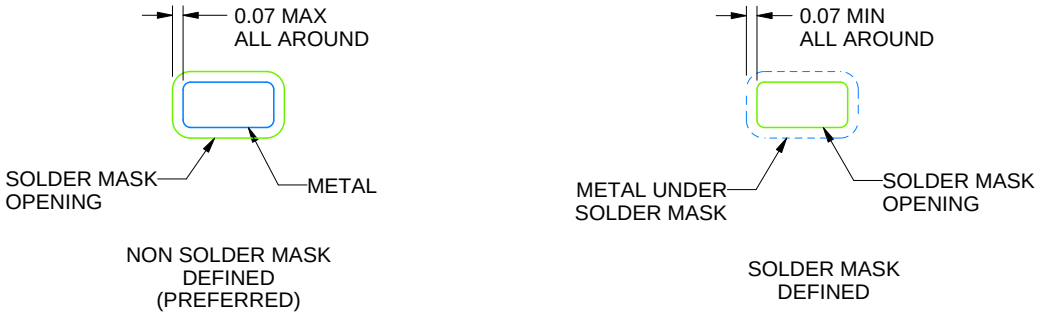


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

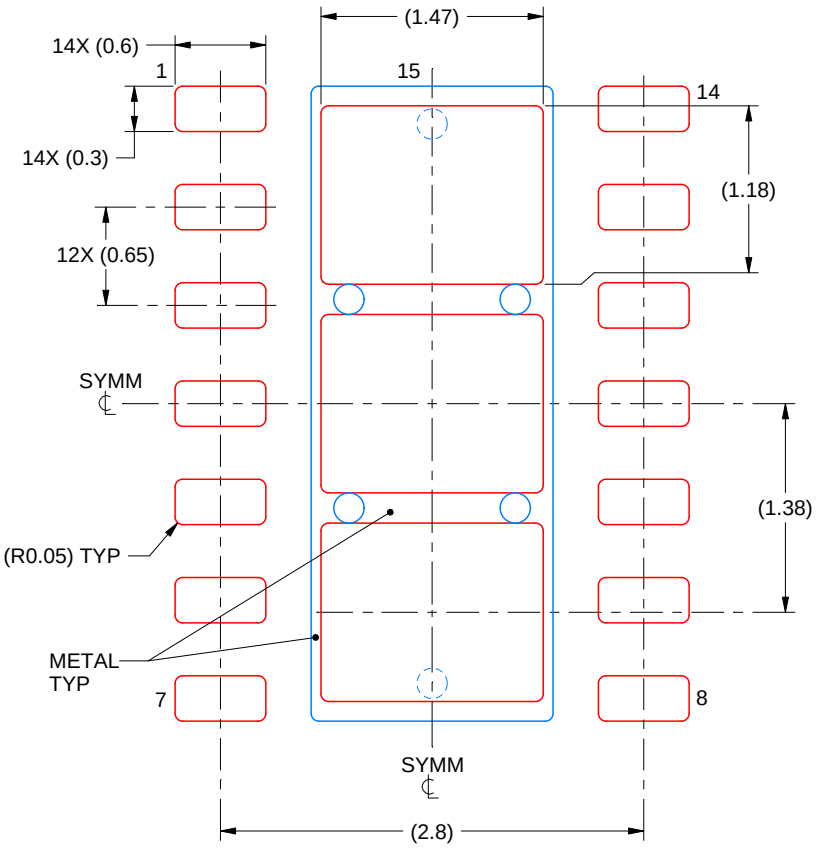


SOLDER MASK DETAILS

4223033/B 10/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4223033/B 10/2016

NOTES: (continued)

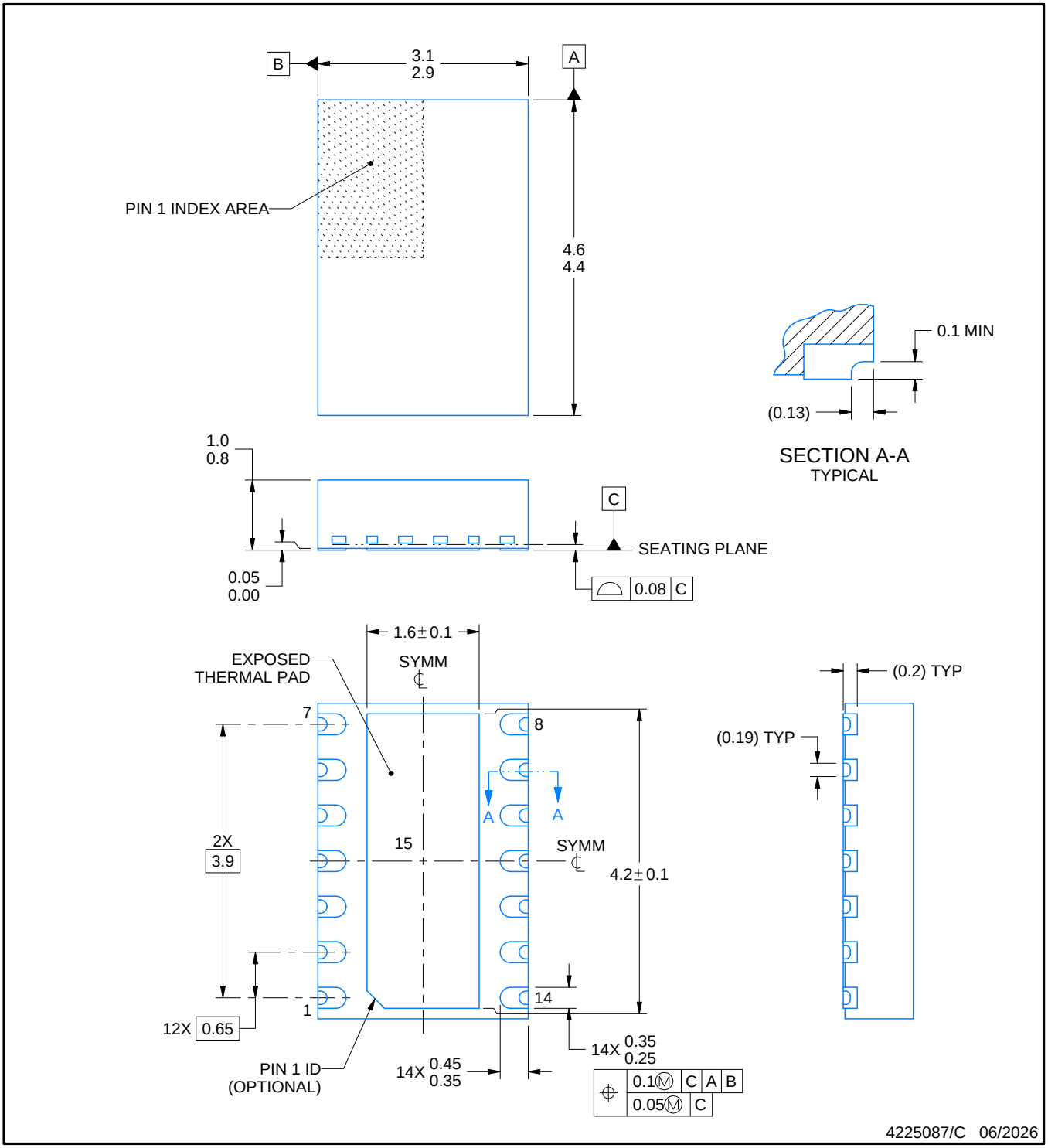
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DMT0014B

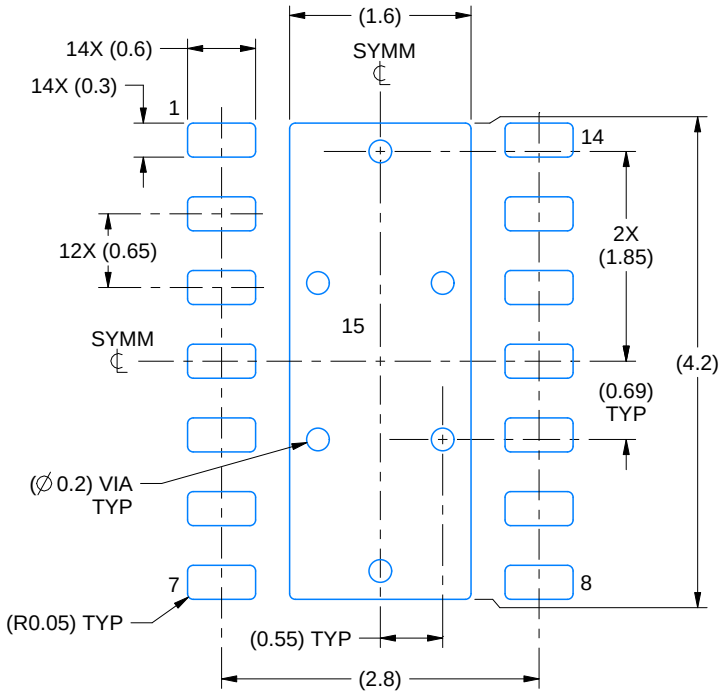
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

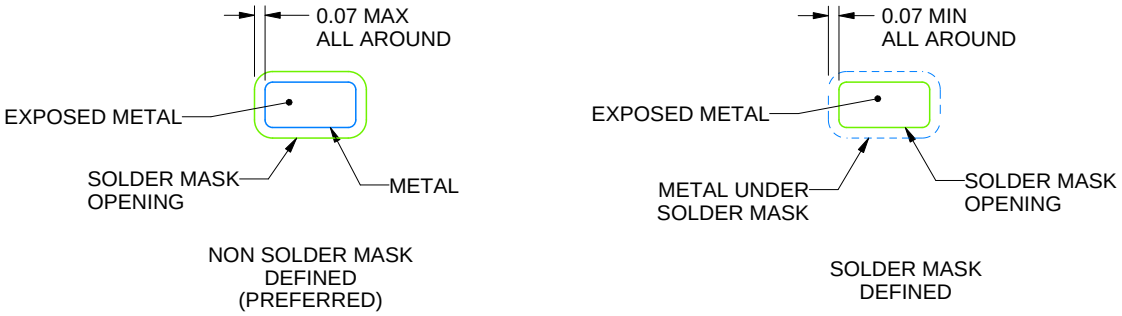


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Exposed side wall metal may vary is shape, size and quantity.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

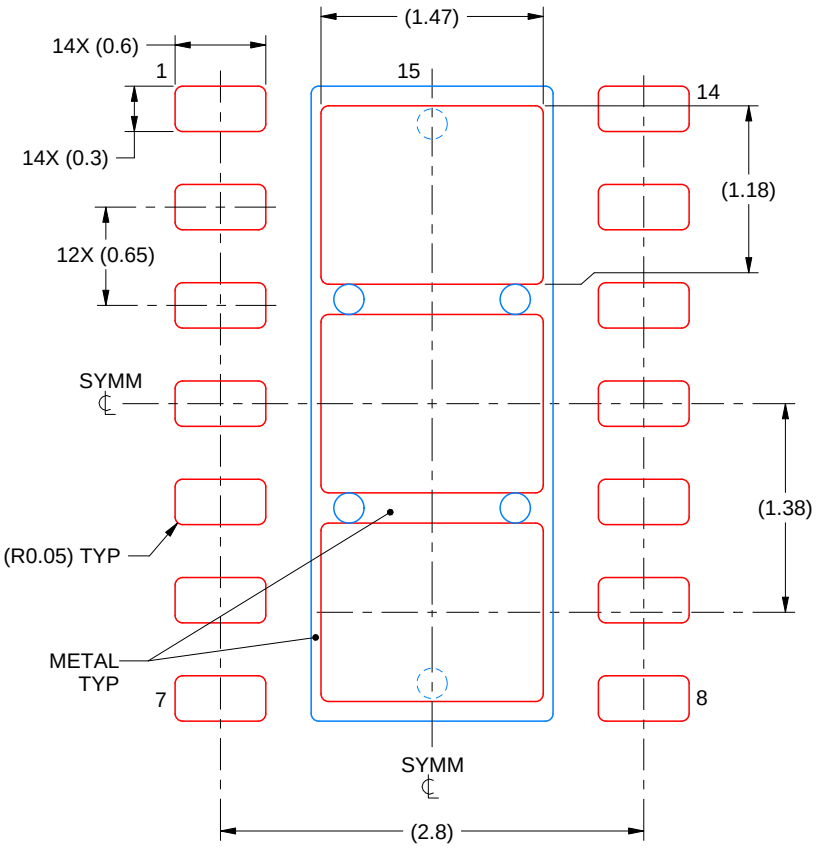


SOLDER MASK DETAILS

4225087/C 06/2026

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4225087/C 06/2026

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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