TCAN1463-Q1 車載用、信号改善機能付き CAN FD トランシーバ、スリープ・モード付き

1 特長

- AEC-Q100 (グレード 1): 車載アプリケーション認定済み
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- ISO 11898-2:2016 の要件に適合
- CiA 601-4 で定義されている信号改善機能 (SIC) を実装
  - リンギングを排除してビット対称性を強化し、バス信号をアクティブに改善
- 最大 8Mbps の classic CAN および CAN FD をサポート
- 広い動作入力電圧範囲
- V_{IO} レベル・シフト対応: 1.7V～5.5V
- 動作モード:
  - 通常モード
  - サイレント・モード
  - スタンバイ・モード
  - 低消費電力スリープ・モード
- システム電源制御のための高電圧 INH 出力
- INH_MASK ピンにより、スプリアス・ウェイクアップ・イベント時に INH をディセーブルに維持
- WAKE ピンによるローカル・ウェイクアップのサポート
- スリープ・ウェイク・エラー (SWE) タイマにより、システム電源障害やソフトウェア障害が発生した場合でも、スタンバイ・モードからスリープ・モードへの安全な移行を実現
  - パワーアップ時間延長に対応可能
- 電源非接続時の規定された挙動
  - バスおよび入出力端子は高インピーダンス (動作中のバスまたはアプリケーションに対して無負荷)
- 保護機能:
  - ±58V の CAN バス・フォルト耐性
  - V_{SUP} でのロード・ダンプのサポート
  - IEC ESD 保護
  - 低電圧保護
  - サーマル・シャットダウン保護
  - TXD ドミナント状態タイムアウト (TXD DTO)
- 14 ピンのリード付き (SOT および SOIC) パッケージ、および自動光学検査 (AOI) 性能向上のためのウェッタブル・フランク付きリードレス (VSON) パッケージで供給

2 アプリケーション

- ボディ・エレクトロニクスおよび照明
- 車載ゲートウェイ
- 先進運転支援システム (ADAS)
- インフォテインメントとクラスタ
- ハイブリッド、電気、パワートレイン・システム
- 個人用移動車両: 電動バイク
- 産業用輸送

3 概要

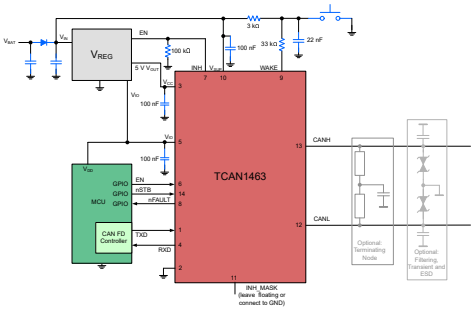
TCAN1463-Q1 は、High Speed CAN (Controller Area Network) トランシーバであり、ISO 11898-2:2016 High Speed CAN 仕様および CiA 601-4 SIC 仕様の物理層要件を満たしています。本デバイスは、Classical CAN と、データ・レートが最高 8 メガビット/秒 (Mbps) の CAN FD (Flexible Data Rate) の両方に対応しています。

TCAN1463-Q1 は、ドミナントからリセッシブへのエッジで信号リンギングを低減し、複雑なネットワーク・トポロジで高いスループットを実現します。SIC により、アプリケーションは複数の未終端スタブを持つ大規模ネットワークで 2Mbps、5Mbps、あるいはそれ以上で動作できるため、CAN FD の真のメリットが引き出されます。INH_MASK 機能を使用しない場合 (INH_MASK ピンがフローティング状態、または GND に接続されている場合)、本デバイスは、TCAN1043A-Q1 や TCAN1043-Q1 などの Classical CAN FD トランシーバとピン互換です。

製品情報

部品番号	パッケージ 1	本体サイズ (公称)
TCAN1463-Q1	SOT (DYY)	4.20mm × 2.00mm
	SOIC (D)	8.65mm × 3.90mm
	VSON (DMT)	4.50mm × 3.00mm

1. 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

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Table of Contents

1 特長.....1
2 アプリケーション.....1
3 概要.....1
4 Revision History.....2
5 概要 (続き).....2
6 Pin Configuration and Functions.....3
7 Specifications.....4
7.1 Absolute Maximum Ratings.....4
7.2 ESD Ratings.....4
7.3 ESD Ratings - IEC Specifications.....4
7.4 Recommended Operating Conditions.....5
7.5 Thermal Information.....5
7.6 Power Dissipation Ratings.....5
7.7 Power Supply Characteristics.....6
7.8 Electrical Characteristics.....7
7.9 Timing Requirements.....9
7.10 Switching Characteristics.....10
7.11 Typical Characteristics.....12
8 Parameter Measurement Information.....13
9 Detailed Description.....18
9.1 Overview.....18
9.2 Functional Block Diagram.....20
9.3 Feature Description.....21
9.4 Device Functional Modes.....28
10 Application Information Disclaimer.....38
10.1 Application Information.....38
11 Device and Documentation Support.....43
11.1 Documentation Support.....43
11.2 ドキュメントの更新通知を受け取る方法.....43
11.3 サポート・リソース.....43
11.4 商標.....43
11.5 静電気放電に関する注意事項.....43
11.6 用語集.....43
12 Mechanical, Packaging, and Orderable Information.....43

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (November 2022) to Revision C (December 2022) **Page**

- 「製品情報」表の D パッケージから製品プレビューの注を削除.....1
- Changed text From: "The CAN Transceiver blocks its transmitter and receiver" To: "The CAN transceiver blocks its transmitter" in the *CAN Active* section.....36

Changes from Revision A (July 2022) to Revision B (November 2022) **Page**

- 「製品情報」表の DYY パッケージから製品プレビューの注を削除.....1

Changes from Revision * (March 2021) to Revision A (July 2022) **Page**

- ドキュメントのステータスを「事前情報」から「量産データ」に変更.....1

5 概要 (続き)

TCAN1463-Q1 を使用すると、システムに存在する各種電源供給の有効・無効を INH 出力ピンで切り替えることにより、バッテリの消費電流をシステム・レベルで低減できます。これにより、CAN バスを監視しながら、TCAN1463-Q1 を除くすべてのシステム・コンポーネントの電源が遮断される低電流スリープ状態を実現します。ウェイクアップ・イベントが検出された場合、TCAN1463-Q1 は INH を High に駆動することでシステムの起動を開始します。

TCAN1463-Q1 は、スタンバイ・モードでの 4 分間 ($t_{INACTIVE}$) の非アクティブ状態の後でスリープ・モードへ安全に移行できるように SWE タイマを備えています。これにより、MCU がデバイスを通常モードに移行できなかった場合に、デバイスは必ず低消費電力のスリープ・モードに移行します。

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6 Pin Configuration and Functions

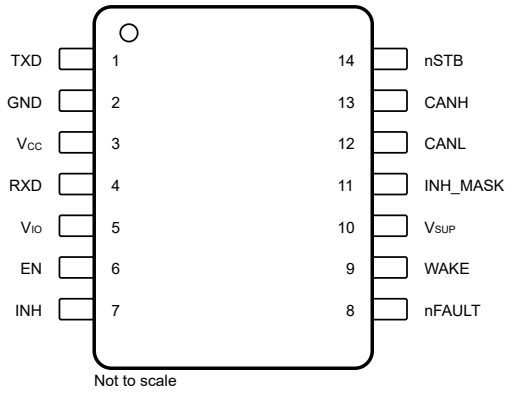


図 6-1. D and DYY Packages, 14 Pin (SOIC) and (SOT) (Top View)

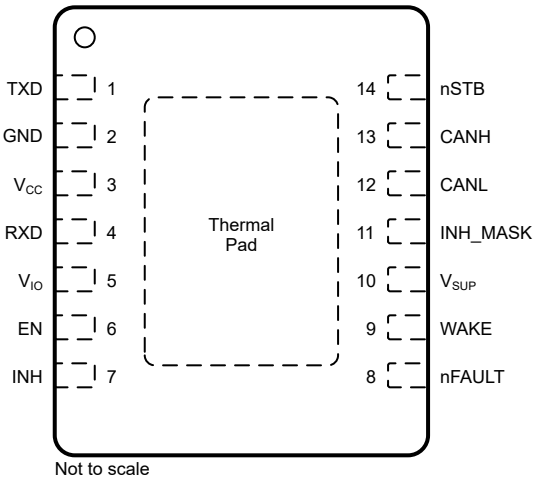


図 6-2. DMT Package, 14 Pin (VSON) (Top View)

PINS		TYPE (1)	DESCRIPTION
NAME	NO.		
TXD	1	I	CAN transmit data input, integrated pull-up
GND	2	GND	Ground connection
V_{CC}	3	P	5 V transceiver supply
RXD	4	O	CAN receive data output, tri-state when $V_{IO} < UV_{IO}$
V_{IO}	5	P	I/O supply voltage
EN	6	I	Enable input for mode control, integrated pull-down
INH	7	O	Inhibit pin to control system voltage regulators and supplies, high-voltage
nFAULT	8	O	Fault output, inverted logic
WAKE	9	I	Local WAKE input terminal, high voltage
V_{SUP}	10	P	High-voltage supply from battery
INH_MASK	11	I	INH_MASK pin used to activate/deactivate INH functionality. Internal pull-down to GND. Can be left floating or connected to GND if INH_MASK functionality is not needed. Do not connect to power supply.
CANL	12	I/O	Low-level CAN bus input/output line
CANH	13	I/O	High-level CAN bus input/output line
nSTB	14	I	Standby mode control input, integrated pull-down
Thermal Pad	—		Connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief

(1) I = input, O = output, P = power, GND = ground

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{SUP}	Supply voltage(2)	–0.3	45	V
V_{CC}	Supply voltage	–0.3	6	V
V_{IO}	Supply voltage I/O level shifter	–0.3	6	V
V_{BUS}	CAN bus I/O voltage (CANH, CANL)	–58	58	V
V_{DIFF}	CAN bus differential voltage (V_{DIFF} = V_{CANH} - V_{CANL})	-58	58	V
V_{WAKE}	WAKE input voltage	–45	45 and $V_I \leq V_{SUP}$+0.3	V
V_{INH}	INH pin voltage	-0.3	45 and $V_O \leq V_{SUP}$+0.3	V
V_{LOGIC}	Logic pin voltage	–0.3	6	V
$I_{O(LOGIC)}$	Logic pin output current		8	mA
$I_{O(INH)}$	Inhibit pin output current		6	mA
$I_{O(WAKE)}$	WAKE pin output current		3	mA
T_J	Junction temperature	–40	165	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Able to support load dumps of up to 45 V for 300ms

7.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	V_{SUP}, CANH, CANL, and WAKE with respect to ground. HBM ESD classification level 3B	± 8000	V
			All pins except V_{SUP}, CANH, CANL, and WAKE. HBM ESD classification level 3A	± 4000	V
		Charged device model (CDM), per AEC Q100-011	All pins. CDM ESD classification level C5	± 750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 ESD Ratings - IEC Specifications

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	CANH, CANL, V_{SUP}, and WAKE terminal to GND	Unpowered Contact Discharge per ISO 10605 (1)	± 8000	V
V_{ESD}	Electrostatic discharge	CANH and CANL terminal to GND	SAE J2962-2 per ISO 10605 Powered Contact Discharge (2)	± 8000	V
V_{ESD}	Electrostatic discharge	CANH and CANL terminal to GND	SAE J2962-2 per ISO 10605 Powered Air discharge (2)	± 15000	V

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				VALUE	UNIT
V_{TRAN}	Transient voltage per ISO-7637-2 (1)	CAN, V_{SUP}, WAKE terminal to GND	Pulse 1	- 100	V
			Pulse 2	75	V
			Pulse 3a	- 150	V
			Pulse 3b	100	V
	Transient voltage per ISO-7637-3 (2)	CAN terminal to GND	Direct coupling capacitor "slow transient pulse" with 100 nF coupling capacitor - powered	± 30	V

(1) Results given here are specific to the IEC 62228-3 Integrated circuits – EMC evaluation of transceivers – Part 3: CAN transceivers. Testing performed by IBEE Zwickau, EMC report available upon request.
(2) Results given here are specific to the SAE J2962-2 Communication Transceivers Qualification Requirements - CAN. Testing performed by OEM-approved independent 3rd party, EMC report available upon request.

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{SUP}	Supply voltage	4.5		40	V
V_{IO}	I/O supply voltage	1.7		5.5	V
V_{CC}	CAN transceiver supply voltage	4.5		5.5	V
$I_{OH(DO)}$	Digital output high-level current	–2			mA
$I_{OL(DO)}$	Digital output low-level current			2	mA
$I_{O(INH)}$	Inhibit output current			4	mA
T_J	Operating junction temperature	-40		150	°C
T_{SDR}	Thermal shutdown	175			°C
T_{SDF}	Thermal shutdown release	160			°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis		10		°C

7.5 Thermal Information

THERMAL METRIC (1)		TCAN1463-Q1			UNIT
		D (SOIC)	DMT (VSON)	DYY (SOT)	
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	87.1	39.7	91.0	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	41.8	41.1	41.7	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	43.7	15.9	25.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.5	0.9	25.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	43.3	15.9	1.1	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	6.6	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.6 Power Dissipation Ratings

PARAMETER		TEST CONDITIONS	POWER DISSIPATION	UNIT
P_D	Average power dissipation	V_{SUP} = 14 V, V_{CC} = 5 V, V_{IO} = 5 V, T_J = 27°C, R_L = 60 Ω, nSTB = 5 V, EN = 5 V, C_{L_RXD} = 15 pF. Typical CAN operating conditions at 500 kbps with 25% transmission (dominant) rate.	62	mW
		V_{SUP} = 14 V, V_{CC} = 5.5 V, V_{IO} = 5.5 V, T_J = 150°C, R_L = 50 Ω, nSTB = 5.5 V, EN = 5.5 V, C_{L_RXD} = 15 pF. Typical high load CAN operating conditions at 1 Mbps with 50% transmission (dominant) rate and loaded network.	135	mW

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7.7 Power Supply Characteristics

Over recommended operating conditions with T_J = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V, V_{IO} = 3.3 V, V_{CC} = 5 V and R_L = 60 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage and Current Characteristics						
I_{SUP_NORMAL}	Supply current CAN active	Normal mode, silent mode, and go-to-sleep mode			140	µA
I_{SUP_STBY}	Supply current, Standby mode CAN autonomous: inactive	Standby mode (2)			60	µA
I_{SUP_SLEEP}	Supply current CAN autonomous: inactive	Sleep mode		18	30	µA
I_{SUP_BIAS}	Supply current Additional current when in CAN autonomous: active	5.5 V < V_{SUP} ≤ 28 V (1) See 8-3			50	µA
$UV_{SUP(R)}$	Undervoltage V_{SUP} threshold rising	Ramp up	3.85		4.4	V
$UV_{SUP(F)}$	Undervoltage V_{SUP} threshold falling	Ramp down	3.5		4.25	V
I_{CC_NORMAL}	Supply current CAN active: dominant	Normal mode TXD = 0 V, R_L = 60 Ω, C_L = open See 8-3			60	mA
	Supply current CAN active: dominant	Normal mode TXD = 0 V, R_L = 50 Ω, C_L = open See 8-3			70	mA
	V_{CC} supply current normal mode Dominant with bus fault	Normal mode TXD = 0 V, R_L = open, C_L = open, CANH = -25 V See 8-3			110	mA
I_{CC_NORMAL}	Supply current CAN active: recessive	Normal mode TXD = 0 V, R_L = 50 Ω, C_L = open See 8-3			5	mA
I_{CC_STBY}	Supply current CAN autonomous: inactive	Standby mode, T_J = -40 °C to 85 °C EN = nSTB = 0 V See 8-3			2	µA
I_{CC_STBY}	Supply current CAN autonomous: inactive	Standby mode EN = nSTB = 0 V See 8-3			5	µA
I_{CC_SILENT}	Supply current	Silent and go-to-sleep mode TXD = nSTB = V_{IO}, R_L = 50 Ω, C_L = open See 8-3			2.5	mA
I_{CC_SLEEP}	Supply current CAN autonomous: inactive	Sleep mode, T_J = -40 °C to 85 °C EN = 0 V or V_{IO}, nSTB = 0 V See 8-3			2	µA
	Supply current CAN autonomous: inactive	Sleep mode EN = 0 V or V_{IO}, nSTB = 0 V See 8-3			5	µA
$UV_{CC(R)}$	Undervoltage V_{CC} threshold rising	Ramp up		4.1	4.4	V
$UV_{CC(F)}$	Undervoltage V_{CC} threshold falling	Ramp down	3.5	3.9		V
$V_{HYS(UVCC)}$	Hysteresis voltage on UV_{CC}		50	250	320	mV
I_{IO_NORMAL}	I/O supply current	Normal mode RXD floating, TXD = 0 V			350	µA
	I/O supply current	Normal mode, standby mode, or go-to-sleep mode RXD floating, TXD = V_{IO}			5	µA
I_{IO_SLEEP}	I/O supply current	Sleep mode, T_J = -40 °C to 85 °C nSTB = 0 V			2.5	µA
	I/O supply current	Sleep mode nSTB = 0 V			5	µA
$UV_{IO(R)}$	Under voltage V_{IO} threshold rising	Ramp up		1.4	1.65	V
$UV_{IO(F)}$	Under voltage V_{IO} threshold falling	Ramp down	1	1.25		V
$V_{HYS(UVIO)}$	Hysteresis voltage on UV_{IO}		30	60	160	mV

(1) $I_{SUP(BIAS)}$ is calculated by subtracting the supply current in CAN autonomous inactive mode from the total supply current in CAN autonomous active mode

(2) After a valid wake-up, the CAN transceiver switches to CAN autonomous active mode and the $I_{SUP(BIAS)}$ current needs to be added to the specified I_{SUP} current in CAN autonomous inactive mode.

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7.8 Electrical Characteristics

Over recommended operating conditions with T_J = –40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V, V_{IO} = 3.3 V, V_{CC} = 5 V and R_L = 60 Ω

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
CAN Driver Characteristics							
$V_{O(D)}$	Dominant output voltage Bus biasing active	CANH	TXD = 0 V, 50 ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open See 図 8-1 and 図 8-4	2.75		4.5	V
		CANL		0.5		2.25	V
$V_{O(R)}$	Recessive output voltage Bus biasing active		TXD = V_{IO}, R_L = open (no load), R_{CM} = open See 図 8-1 and 図 8-4	2		3	V
V_{SYM}	Driver symmetry Bus biasing active ($V_{O(CANH)}$ + $V_{O(CANL)}$) / V_{CC}		nSTB= V_{IO}, R_L = 60 Ω, C_{SPLIT} = 4.7 nF, C_L = Open, R_{CM} = Open, TXD = 250 kHz, 1 MHz, 2.5 MHz See 図 8-1 and 図 8-4	0.9		1.1	V/V
V_{SYM_DC}	DC Driver symmetry Bus biasing active V_{CC} – $V_{O(CANH)}$ – $V_{O(CANL)}$		nSTB= V_{IO}, R_L = 60 Ω, C_L = open See 図 8-1 and 図 8-4	–400		400	mV
$V_{OD(DOM)}$	Differential output voltage Bus biasing active Dominant	CANH - CANL	nSTB =V_{IO}, TXD = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open See 図 8-1 and 図 8-4	1.5		3	V
		CANH - CANL	nSTB =V_{IO}, TXD = 0 V, 45 Ω ≤ R_L ≤ 70 Ω, CL = open See 図 8-1 and 図 8-4	1.4		3.3	V
		CANH - CANL	nSTB =V_{IO}, TXD = 0 V, R_L = 2240 Ω, C_L = open See 図 8-1 and 図 8-4	1.5		5	V
$V_{OD(REC)}$	Differential output voltage Bus biasing active Recessive	CANH - CANL	nSTB =V_{IO}, TXD = V_{IO}, R_L = open Ω, C_L = open See 図 8-1 and 図 8-4	–50		50	mV
$V_{OD(STB)}$	Differential output voltage Bus biasing inactive Recessive	CANH	nSTB =0 V, TXD = V_{IO}, R_L = open (no load), C_L = open See 図 8-1 and 図 8-4	-0.1		0.1	V
		CANL	nSTB =0 V, TXD = V_{IO}, R_L = open (no load), C_L = open See 図 8-1 and 図 8-4	-0.1		0.1	V
		CANH - CANL	nSTB =0 V, TXD = V_{IO}, R_L = open (no load), C_L = open See 図 8-1 and 図 8-4	-0.2		0.2	V
$I_{OS(DOM)}$	Short-circuit steady-state output current Bus biasing active Dominant		nSTB = V_{IO}, TXD = 0 V -15 V ≤ $V_{(CANH)}$ ≤ 40 V See 図 8-1 and 図 8-8	–100			mA
			nSTB = V_{IO}, TXD = 0 V -15 V ≤ $V_{(CANL)}$ ≤ 40 V See 図 8-1 and 図 8-8			100	mA
$I_{OS(REC)}$	Short-circuit steady-state output current Bus biasing active Recessive		nSTB = V_{IO}, V_{BUS} = CANH = CANL -27 V ≤ V_{BUS} ≤ 42 V See 図 8-1 and 図 8-8	–3		3	mA
$R_{ID(dom)}$	Differential input resistance in dominant phase		See 図 9-2		40		ohm
$R_{ID(active_rec)}$	Differential input resistance in active recessive drive phase		See 図 9-2		60		ohm
CAN Receiver Characteristics							
$V_{IT(DOM)}$	Receiver dominant state input voltage range Bus biasing active		nSTB = V_{IO}, -12 V ≤ V_{CM} ≤ 12 V See 図 8-5 and 表 9-6	0.9		8	V
$V_{IT(REC)}$	Receiver recessive state input voltage range Bus biasing active			-3		0.5	V
V_{HYS}	Hysteresis voltage for input threshold Bus biasing active		nSTB = V_{IO} See 図 8-5 and 表 9-6		135		mV
$V_{DIFF(DOM)}$	Receiver dominant state input voltage range Bus biasing inactive		nSTB = 0 V, -12 V ≤ V_{CM} ≤ 12 V See 図 8-5 and 表 9-6	1.150		8	V
$V_{DIFF(REC)}$	Receiver recessive state input voltage range Bus biasing inactive			-3		0.4	V

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7.8 Electrical Characteristics (continued)

Over recommended operating conditions with T_J = –40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V, V_{IO} = 3.3 V, V_{CC} = 5 V and R_L = 60 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CM}	Common mode range	nSTB = V_{IO} See 図 8-5 and 表 9-6	–12		12	V
$I_{OFF(LKG)}$	Power-off (unpowered) bus input leakage current	V_{SUP} = 0 V, CANH = CANL = 5 V			2.5	µA
C_I	Input capacitance to ground (CANH or CANL) (1)	TXD = V_{CC} = V_{IO}			40	pF
C_{ID}	Differential input capacitance (1)	TXD = V_{CC} = V_{IO}			20	pF
R_{ID}	Differential input resistance	TXD = V_{CC} = V_{IO} = 5 V, nSTB = 5 V -12 V ≤ V_{CM} ≤ 12 V	30		100	kΩ
R_{IN}	Input resistance (CANH or CANL)		15		50	kΩ
$R_{IN(M)}$	Input resistance matching: [1 – $R_{IN(CANH)}$ / $R_{IN(CANL)}$] × 100%	$V_{(CANH)}$ = $V_{(CANL)}$ = 5 V	–3		3	%
R_{CBF}	Valid differential load impedance range for bus fault circuitry	R_{CM} = R_L, C_L = open	45		70	Ω
TXD Characteristics						
V_{IH}	High-level input voltage		0.7			V_{IO}
V_{IL}	Low-level input voltage				0.3	V_{IO}
I_{IH}	High-level input leakage current	TXD = V_{IO} = 5.5 V	–2.5		1	µA
I_{IL}	Low-level input leakage current	TXD = 0 V, V_{IO} = 5.5 V	–115		–2.5	µA
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 5.5 V, V_{SUP} = V_{IO} = 0 V	–1		1	µA
R_{PU}	Pull-up resistance to V_{IO}		40	60	80	kΩ
C_I	Input Capacitance	V_{IN} = 0.4 x sin(2 × π × 2 × 10^6 × t) + 2.5 V		5		pF
RXD Characteristics						
V_{OH}	High-level output voltage	I_O = –2 mA See 図 8-5	0.8			V_{IO}
V_{OL}	Low-level output voltage	I_O = 2 mA See 図 8-5			0.2	V_{IO}
$I_{LKG(OFF)}$	Unpowered leakage current	RXD = 5.5 V, V_{SUP} = V_{IO} = 0 V	-1		1	µA
nSTB Characteristics						
V_{IH}	High-level input voltage		0.7			V_{IO}
V_{IL}	Low-level input voltage				0.3	V_{IO}
I_{IH}	High-level input leakage current	nSTB = V_{IO} = 5.5 V	0.5		115	µA
I_{IL}	Low-level input leakage current	nSTB = 0 V, V_{IO} = 5.5 V	–1		1	µA
$I_{LKG(OFF)}$	Unpowered leakage current	nSTB = 5.5 V, V_{IO} = 0 V	–1		1	µA
R_{PD}	Pull-down resistance to GND		40	60	80	kΩ
nFAULT Characteristics						
V_{OH}	High-level output voltage	I_O = -2 mA	0.8			V_{IO}
V_{OL}	Low-level output voltage	I_O = 2 mA			0.2	V_{IO}
$I_{LKG(OFF)}$	Unpowered leakage current	nFAULT = 5.5 V, V_{IO} = 0 V	–1		1	µA
INH_MASK Characteristics						
V_{IH}	High-level input voltage		0.7			V_{IO}
V_{IL}	Low-level input voltage				0.3	V_{IO}
I_{IH}	High-level input leakage current	INH_MASK = V_{CC} = V_{IO} = 5.5 V	0.5		115	µA
I_{IL}	Low-level input leakage current	INH_MASK = 0 V, V_{CC} = V_{IO} = 5.5 V	-1		1	µA
$I_{LKG(OFF)}$	Unpowered leakage current	INH_MASK = 5.5 V, V_{CC} = V_{IO} = 0 V	-1		1	µA
R_{PD}	Pull-down resistance to GND (1)		40	60	80	kΩ
EN Characteristics						
V_{IH}	High-level input voltage		0.7			V_{IO}
V_{IL}	Low-level input voltage				0.3	V_{IO}
I_{IH}	High-level input leakage current	EN = V_{CC} = V_{IO} = 5.5 V	0.5		115	µA

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7.8 Electrical Characteristics (continued)

Over recommended operating conditions with T_J = –40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V, V_{IO} = 3.3 V, V_{CC} = 5 V and R_L = 60 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Low-level input leakage current	EN = 0 V, V_{CC} = V_{IO} = 5.5 V	-1		1	µA
$I_{LKG(OFF)}$	Unpowered leakage current	EN = 5.5 V, V_{CC} = V_{IO} = 0 V	-1		1	µA
R_{PD}	Pull-down resistance to GND		40	60	80	kΩ
WAKE Characteristics						
V_{IH}	High-level input voltage	Sleep mode	V_{SUP} - 2			V
V_{IL}	Low-level input voltage				V_{SUP} - 3.5	V
I_{IH}	High-level input leakage current	WAKE = V_{SUP} – 1 V	-3			µA
I_{IL}	Low-level input leakage current	WAKE = 1 V			3	µA
INH Characteristics						
ΔV_H	High-level voltage drop from V_{SUP} to INH (V_{SUP} - V_{INH})	I_{INH} = –6 mA		0.5	1	V
$I_{LKG(INH)}$	Sleep mode leakage current	INH = 0 V	–0.5		0.5	µA
R_{PD}	Pull-down resistance	Sleep mode	2.5	4	5.6	MΩ

(1) Specified by design and verified via bench characterization

7.9 Timing Requirements

Over recommended operating conditions with T_J = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V, V_{IO} = 3.3 V, V_{CC} = 5 V and R_L = 60 Ω

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Characteristics							
t_{PWRUP}	Time required for INH active after V_{SUP} ≥ $UV_{SUP(R)}$		See 図 8-12		340		µs
t_{UV}	Undervoltage filter time V_{CC} and V_{IO} (1)		V_{CC} ≤ UV_{CC} or V_{IO} ≤ UV_{IO}	100		350	ms
$t_{UV(RE-ENABLE)}$	Re-enable time after undervoltage event (1)		Time for device to return to normal operation from a UV_{CC} or UV_{IO} undervoltage event			200	µs
Device Characteristics							
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD) Recessive to dominant		R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF See 図 8-6		100	190	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD) Dominant to recessive		R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF See 図 8-6		110	190	ns
$t_{WK(TIMEOUT)}$	Bus wake-up timeout value (1)			0.8		2	ms
$t_{WK(FILTER)}$	Bus time to meet filtered bus requirements for wake-up request (1)			0.5		1.8	µs
$t_{SILENCE}$	Timeout for bus inactivity (1)		Timer is reset and restarted, when bus changes from dominant to recessive or vice versa	0.6		1.2	s
$t_{INACTIVE}$	Standby mode hardware timer for power-up inactivity			3	4	5	min
t_{BIAS}	Bus bias reaction time (1)	Measured from the start of a dominant-recessive-dominant sequence (each phase 6 µs) until V_{SYM} ≥ 0.1	nSTB = EN = 0 V, R_L = 60 Ω, C_{SPLIT} = 4.7 nF See 図 8-9 and 図 10-3			200	µs
t_{CBF}	Bus fault-detection time		45 ≤ R_{CM} ≤ 70 Ω C_L = open	2.5			µs
t_{WAKE_HT}	Hold time for which WAKE pin voltage should be stable after the rising or falling edge on WAKE pin to recognize LWU			5		50	µs
Mode Change Characteristics							
$t_{INH_SLP_STB}$	Time after WUP or LWU event until INH asserted (1)					100	µs
t_{INH_MASK}	Hold time for which INH_MASK should be stable after the rising or falling edge to enable/disable INH_MASK function See 図 8-10 and 図 8-11			50			µs
t_{MODE1}	Mode change time from leaving the Sleep mode to entering Normal or Silent mode (1)		Time measured from VCC and VIO crossing UV thresholds to entering normal or silent mode.			20	µs
t_{MODE2}	Mode change time between normal, silent and standby mode and from sleep to standby mode (1)		Mode change time between normal, silent and standby mode and from sleep to standby mode			10	µs

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7.9 Timing Requirements (continued)

Over recommended operating conditions with T_J = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V, V_{IO} = 3.3 V, V_{CC} = 5 V and R_L = 60 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{GOTOSLEEP}$	Minimum hold time for transition to sleep mode (1)	EN = H and nSTB = L	20		50	µs

(1) Specified by design and verified via bench characterization

7.10 Switching Characteristics

Over recommended operating conditions with T_J = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V, V_{IO} = 3.3 V, V_{CC} = 5 V and R_L = 60 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Characteristics						
$t_{prop(TxD-busdom)}$	Propagation delay time, high-to-low TXD edge to bus dominant (recessive to dominant)	R_L = 60 Ω, C_L = 100 pF, R_{CM} = open See 図 8-4			80	ns
$t_{prop(TxD-busrec)}$	Propagation delay time, low-to-high TXD edge to bus recessive (dominant to recessive)				80	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{prop(TxD-busdom)} - t_{prop(TxD-busrec)} \rvert$)	R_L = 60 Ω, C_L = 100 pF, R_{CM} = open See 図 8-4		3		ns
t_R	Differential output signal rise time			25		ns
t_F	Differential output signal fall time			25		ns
t_{TXDDTO}	Dominant timeout	TXD = 0 V, R_L = 60 Ω, C_L = open See 図 8-7	1.2		3.8	ms
Receiver Characteristics						
$t_{prop(busdom-RxD)}$	Propagation delay time, bus dominant input to RxD low output	$C_{L(RXD)}$ = 15 pF See 図 8-5			110	ns
$t_{prop(busrec-RxD)}$	Propagation delay time, bus to recessive input to RXD high output				110	ns
t_R	Output signal rise time (RXD)	$C_{L(RXD)}$ = 15 pF See 図 8-5		3		ns
t_F	Output signal fall time (RXD)			3		ns
t_{BUSDOM}	Dominant time out	R_L = 60 Ω, C_L = open See 図 8-5	1.4		3.8	ms
CAN FD Characteristics						
$t_{BIT(BUS)}$ (1)	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns	R_L = 60 Ω, C_{L1} = open, C_{L2} = 100 pF, $C_{L(RXD)}$ = 15 $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$ See 図 8-6	490		510	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns		190		210	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 125 ns(2)		115		135	ns
$t_{BIT(RXD)}$ (1)	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500 ns		470		520	ns
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200 ns		170		210	ns
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 125 ns(2)		95		135	ns
Δt_{REC} (1)	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500 ns		–20		15	ns
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200 ns		–20		15	ns
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 125 ns(2)		–20		15	ns
Signal Improvement Characteristics						
$t_{SIC_TX_base}$	Signal improvement time TX-based	Time from rising edge of the TxD signal to the end of the signal improvement phase			530	ns
$\Delta t_{Bit(Bus)}$	Transmitted bit width variation	Bus recessive bit length variation relative to TxD bit length, see 図 8-6 $\Delta t_{Bit(Bus)} = t_{Bit(Bus)} - t_{Bit(TxD)}$	–10		10	ns
$\Delta t_{BIT(RxD)}$	Received bit width variation	RxD recessive bit length variation relative to TXD bit length, see 図 8-6 $\Delta t_{Bit(RxD)} = t_{Bit(RxD)} - t_{Bit(TxD)}$	–30		20	ns
Δt_{REC}	Receiver timing symmetry	RXD recessive bit length variation relative to bus bit length, see 図 8-6 $\Delta t_{REC} = t_{Bit(RxD)} - t_{Bit(Bus)}$	–20		15	ns

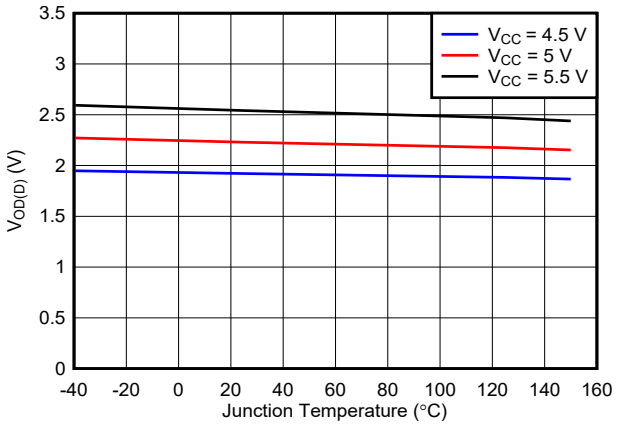
(1) The input signal on TXD shall have rise times and fall times (10% to 90%) of less than 10 ns

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(2) Specified by design and verified via bench characterization

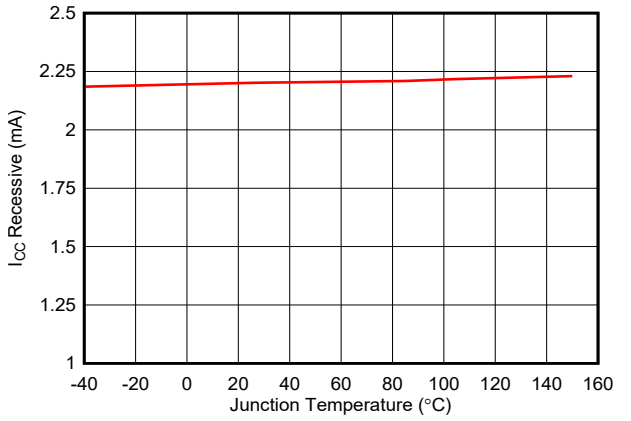
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7.11 Typical Characteristics



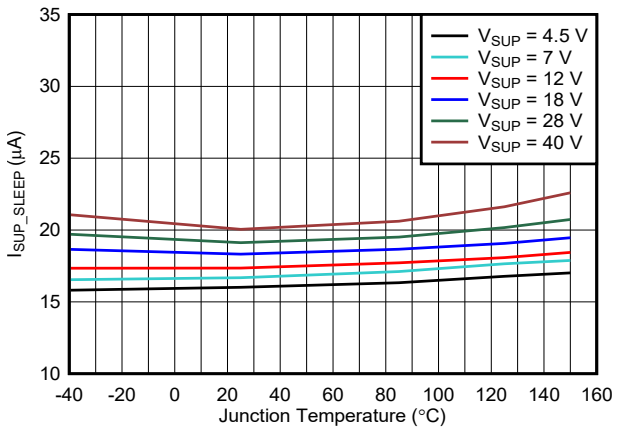
R_L = 60 Ω C_L = Open R_{CM} = Open
V_{IO} = 3.3 V

図 7-1. $V_{OD(DOM)}$ vs Temperature and V_{CC}



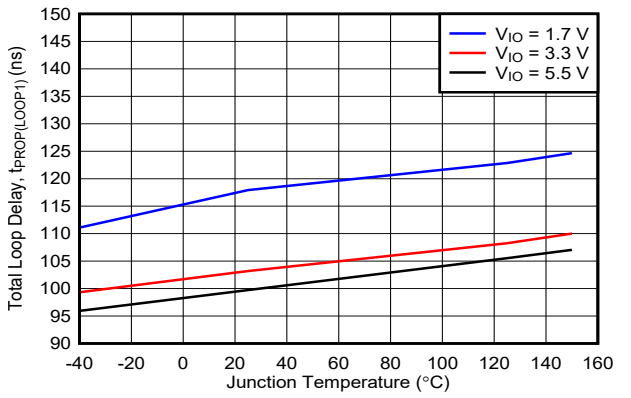
R_L = 60 Ω C_L = Open R_{CM} = Open
V_{CC} = 5 V V_{IO} = 3.3 V

図 7-2. I_{CC} Recessive vs Temperature



R_L = 60 Ω C_L = Open R_{CM} = Open
V_{CC} = 5 V V_{IO} = 3.3 V

図 7-3. I_{SUP} in Sleep Mode vs V_{SUP} and Temperature



R_L = 60 Ω C_L = 100 pF $C_{L(RXD)}$ = 15 pF
V_{CC} = 5 V V_{SUP} = 12 V

図 7-4. Loop Propagation Delay vs V_{IO} and Temperature

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8 Parameter Measurement Information

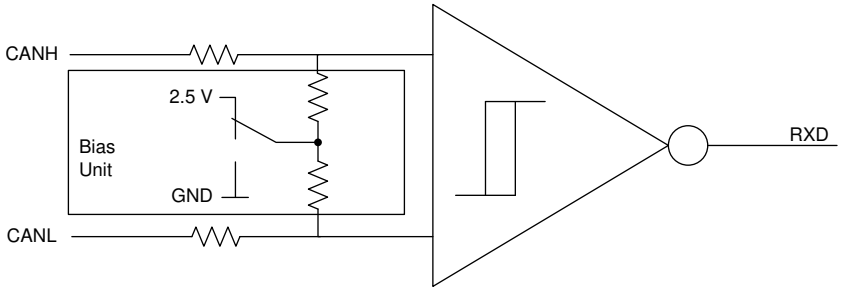


図 8-1. Common-Mode Bias Unit and Receiver

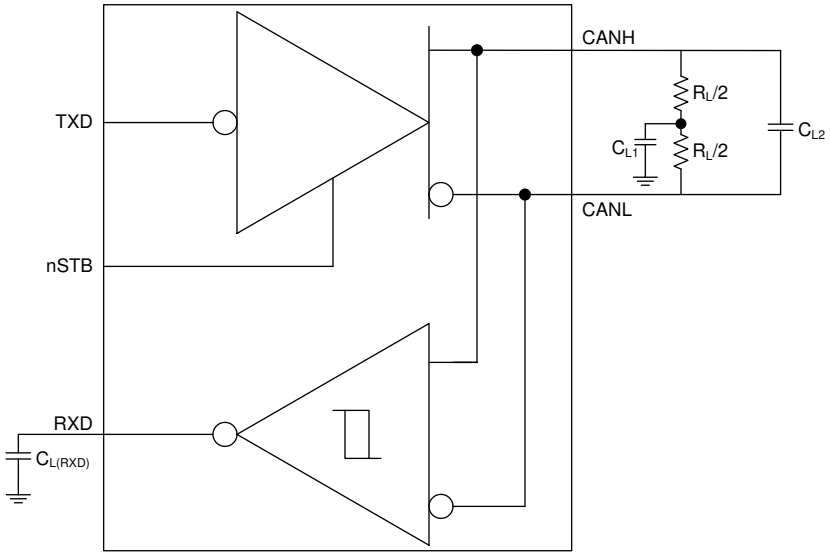


図 8-2. Test Circuit

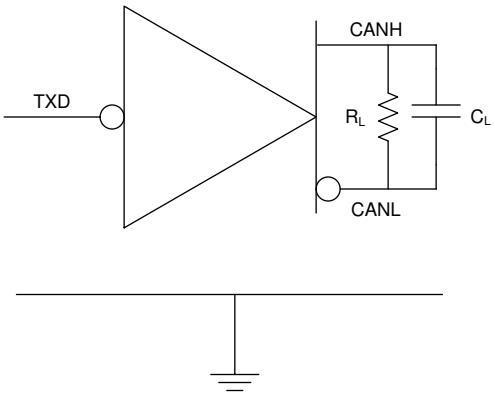


図 8-3. Supply Test Circuit

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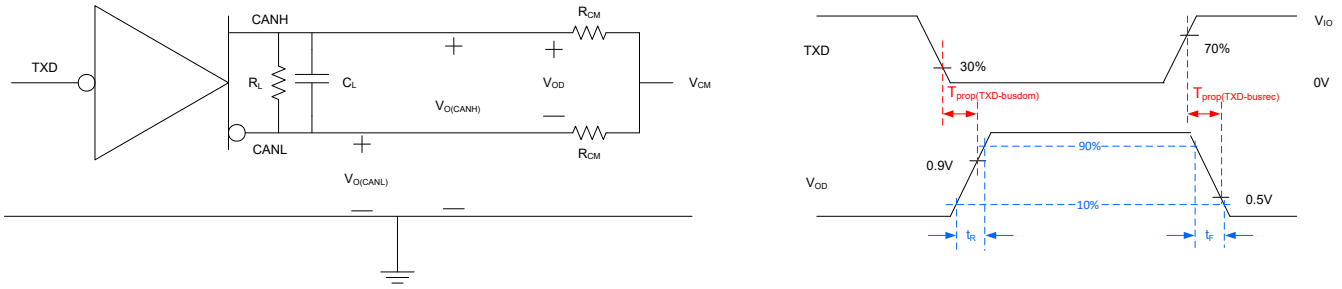


図 8-4. Driver Test Circuit and Measurement

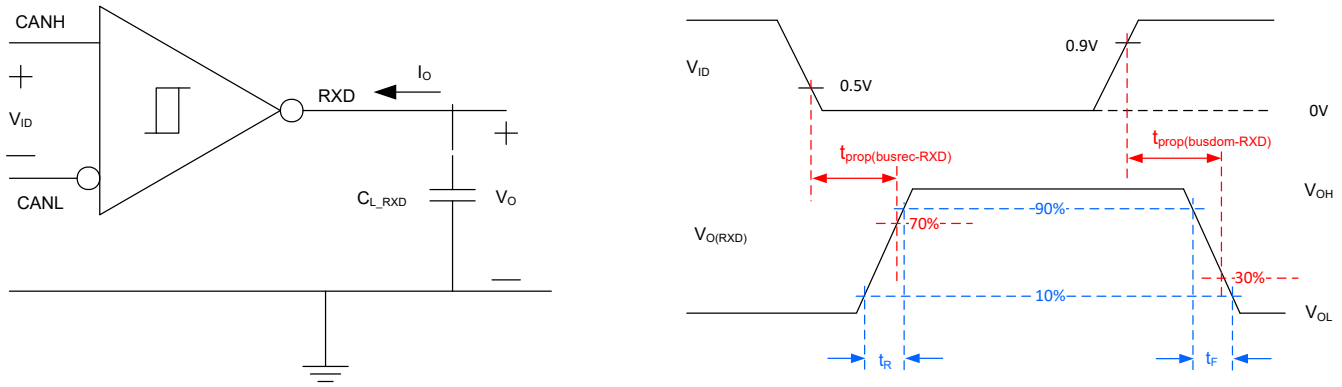


図 8-5. Receiver Test Circuit and Measurement

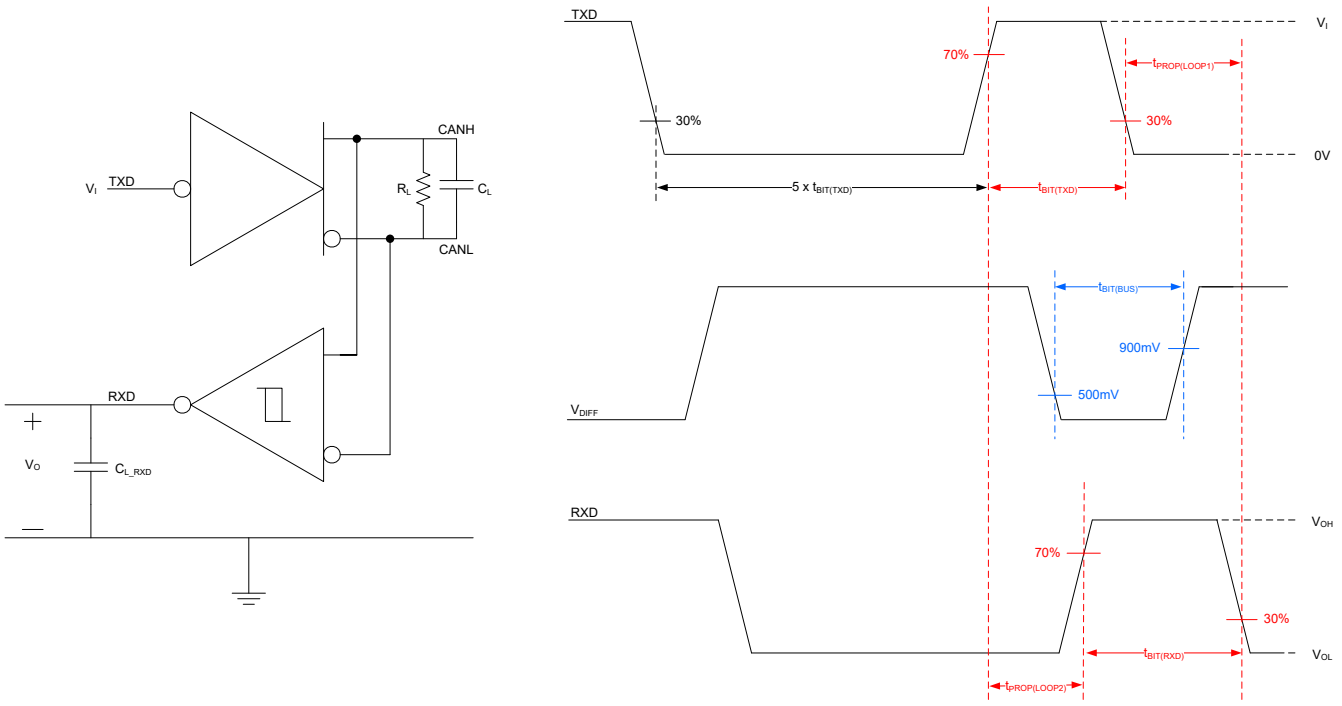


図 8-6. Transmitter and Receiver Timing Behavior Test Circuit and Measurement

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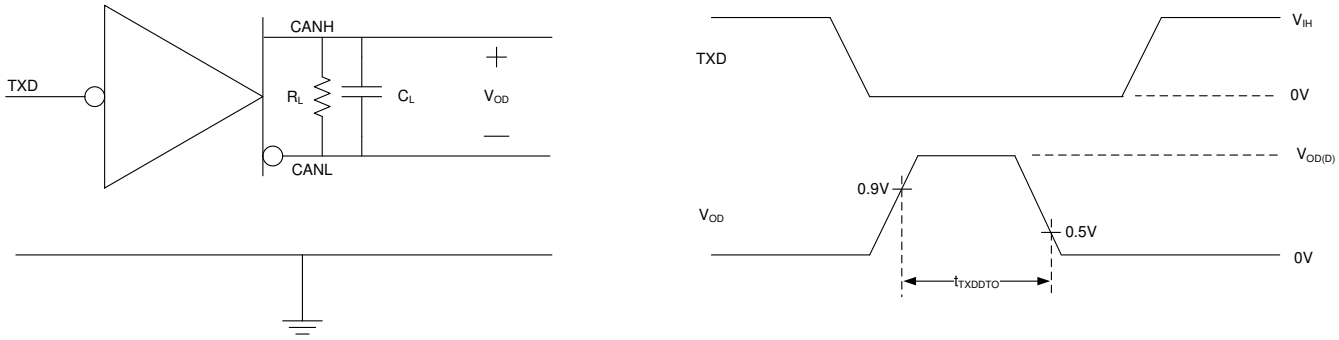


図 8-7. TXD Dominant Time Out Test Circuit and Measurement

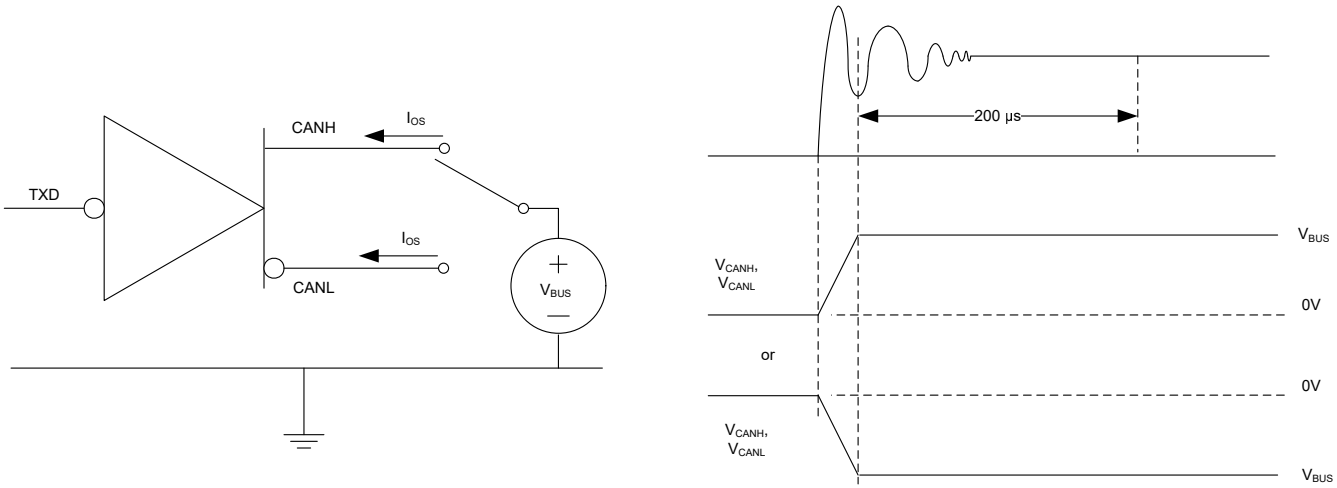


図 8-8. Driver Short-Circuit Current Test and Measurement

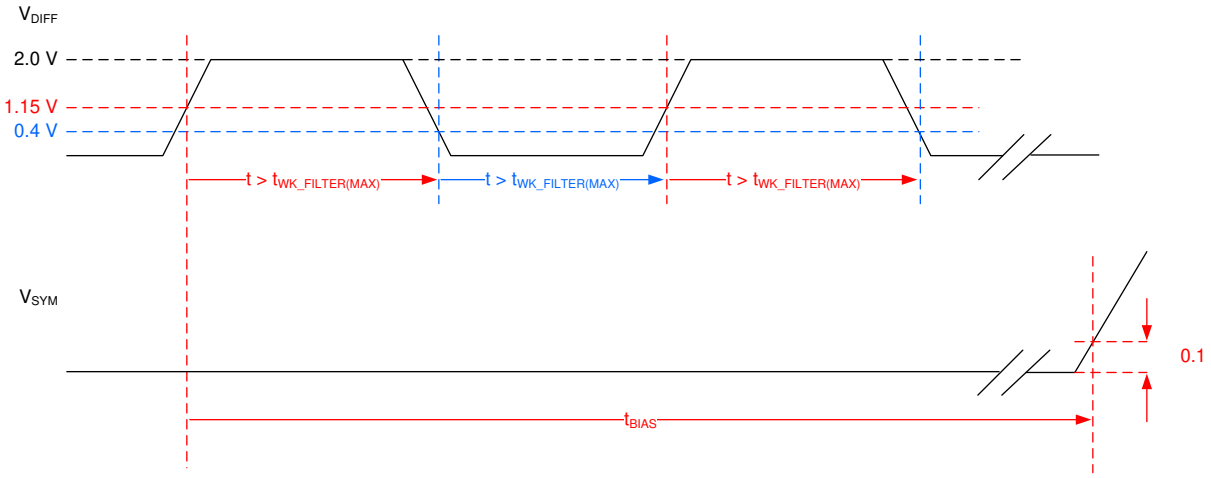
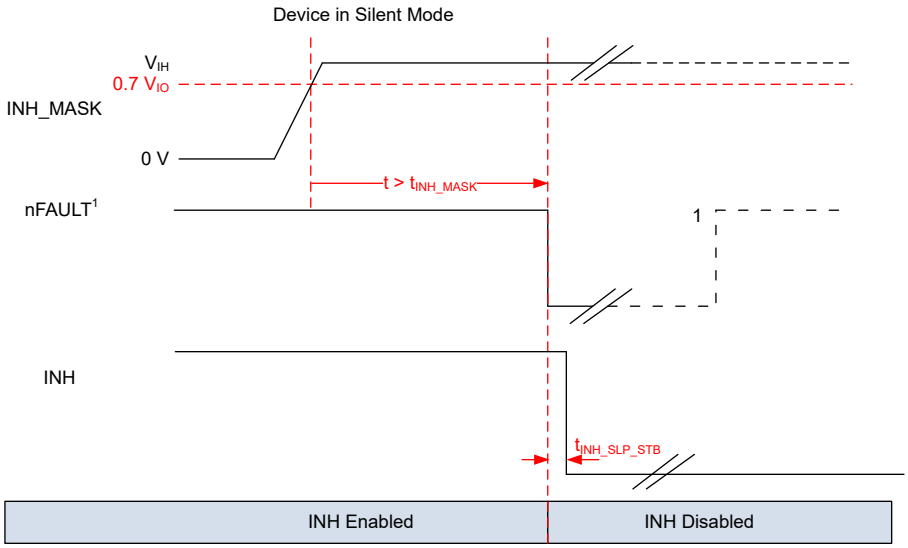
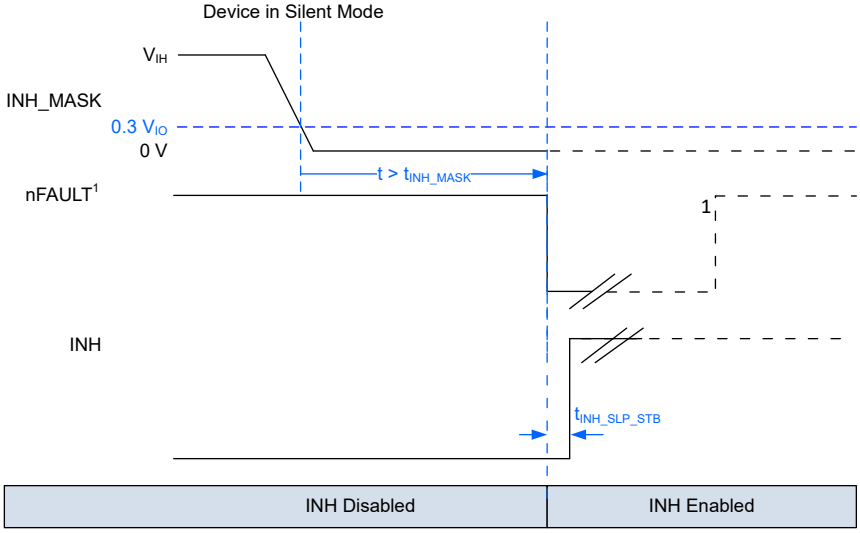


図 8-9. Bias Reaction Time Measurement



1. nFAULT clears upon exiting silent mode

図 8-10. INH Disable Timing Diagram



1. nFAULT clears upon exiting silent mode

図 8-11. INH Enable Timing Diagram

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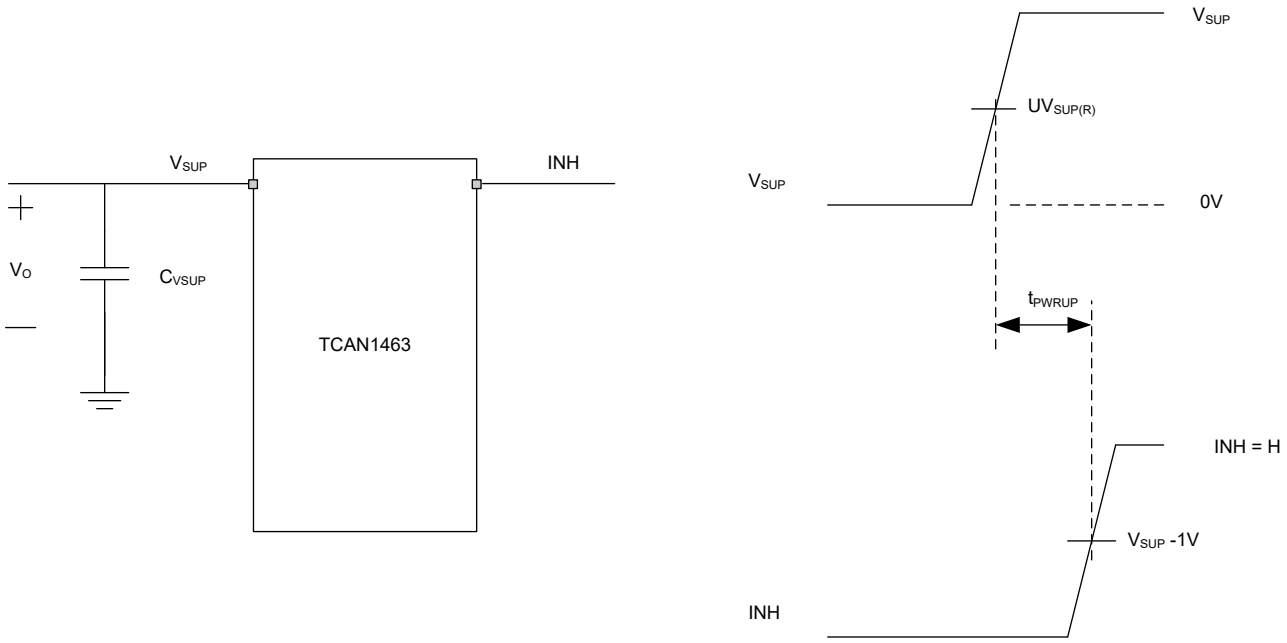


図 8-12. Power-Up Timing

9 Detailed Description

9.1 Overview

The TCAN1463-Q1 is a high-speed Controller Area Network (CAN) transceiver that meets the physical layer requirements of the ISO 11898-2:2016 and CiA 601-4 high speed CAN specifications. The TCAN1463-Q1 is data rate agnostic making it backward compatible for supporting classical CAN applications while also supporting CAN FD networks up to 8 megabits per second (Mbps).

The transceiver has three separate supply inputs, V_{SUP}, V_{CC}, and V_{IO}. By using V_{IO}, the TCAN1463-Q1 can interface directly to a 1.8 V, 2.5 V, 3.3 V, or 5 V controller without the need for a level shifter. The TCAN1463-Q1 allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that may be present in the system via the INH output pin. This enables a low-current sleep state in which power is gated to all system components except for the TCAN1463-Q1, which remains in a low-power state while monitoring the CAN bus. When a wake-up pattern is detected on the bus or when a local wake up is requested via the WAKE input, the device initiates node start-up by driving INH high.

The TCAN1463-Q1 includes many protection and diagnostic features including undervoltage detection, CAN bus fault detection, SWE timer, battery connection detection, thermal shutdown (TSD), driver dominant timeout (TXD DTO), and bus fault protection up to ±58 V.

9.1.1 Signal Improvement

The TCAN1463-Q1 includes the Signal Improvement Capability (SIC) that enhances the maximum data rate achievable in complex star topologies by minimizing signal ringing. Signal ringing is the result of reflections caused by impedance mismatch at various points in a complex CAN network.

An example of a star network is shown 図 9-1.

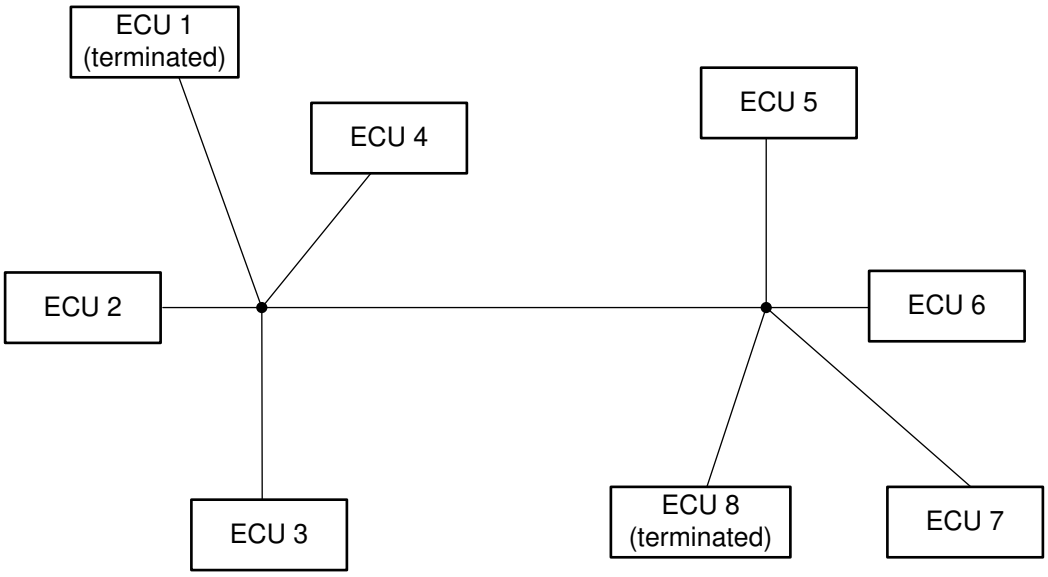


図 9-1. CAN network: Star Topology

Recessive-to-dominant signal edge is usually clean as it's strongly driven by the transmitter. Transmitter output impedance of CAN transceiver is $R_{ID(dom)}$ and matches to the network characteristic impedance. For a regular CAN FD transceiver, dominant-to-recessive edge is when the driver output impedance goes to ~60 kΩ and signal reflected back experiences impedance mismatch which causes ringing. The TCAN1463-Q1 resolves this issue by TX-based Signal improvement capability (SIC). The TCAN1463-Q1 continues to drive the bus recessive strongly till $t_{SIC_TX_base}$ to minimize the reflections and the recessive bit is clean at the sampling point. In the active recessive phase, transmitter output impedance is low ($R_{ID(active_rec)}$). After this phase, the device enters into a passive recessive phase where the driver goes into high impedance state. This phenomenon is explained

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using 図 9-2. For further information, please refer to the white paper on how SIC unlocks the real potential of CAN-FD transceivers.

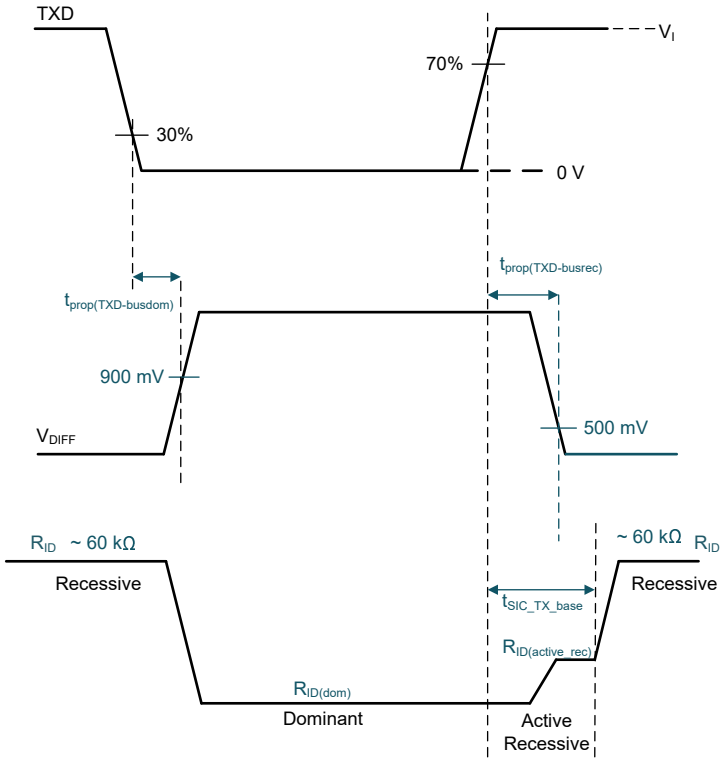
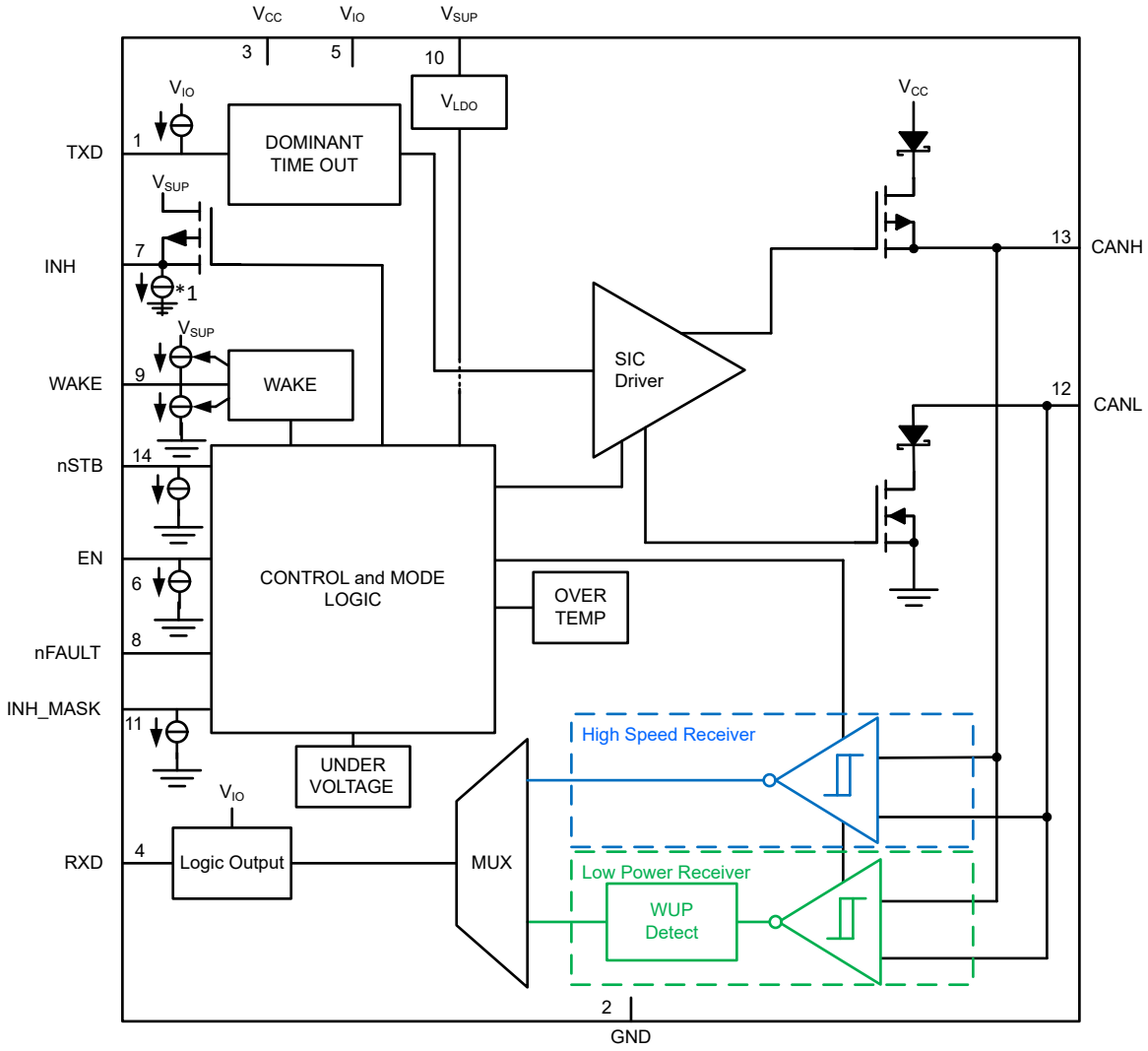


図 9-2. TX based Signal Improvement Capability

9.2 Functional Block Diagram



1. A pull-down resistor of 4 MΩ (typical) is activated on INH pin when the device is in Sleep mode.

図 9-3. TCAN1463-Q1 Functional Block Diagram

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9.3 Feature Description

9.3.1 Supply Pins

The TCAN1463-Q1 implements three independent supply inputs for regulating different portions of the device.

9.3.1.1 V_{SUP} Pin

This pin is connected to the battery supply. It provides the supply to the internal regulators that support the digital core and the low power CAN receiver.

9.3.1.2 V_{CC} Pin

This pin provides the 5 V supply voltage for the CAN transceiver.

9.3.1.3 V_{IO} Pin

This pin provides the digital I/O voltage to match the CAN FD controller's I/O voltage. It supports I/O voltages from 1.7 V to 5.5 V providing a wide range of controller support.

9.3.2 Digital Inputs and Outputs

9.3.2.1 TXD Pin

TXD is a logic-level input signal, referenced to V_{IO}, from a CAN FD controller to the TCAN1463-Q1. TXD is biased to the V_{IO} level to force a recessive input in case the pin floats.

9.3.2.2 RXD Pin

RXD is a logic-level signal output, referenced to V_{IO}, from the TCAN1463-Q1 to a CAN FD controller. The RXD pin is driven to the V_{IO} level as logic-high outputs once a valid V_{IO} is present.

When a power-on or wake-up event takes place, the RXD pin is pulled low.

9.3.2.3 nFAULT Pin

nFAULT is a logic-level output signal, referenced to V_{IO}, from the TCAN1463-Q1 to a CAN FD controller. The nFAULT output is driven to the V_{IO} level as logic-high output.

The nFAULT output is used to transmit the TCAN1463-Q1 status indicator flags to the CAN FD controller. Please see 表 9-1 for the specific fault scenarios that are indicated externally via the nFAULT pin. The TCAN1463-Q1 puts the nFAULT pin in the high-impedance state in the Sleep mode to conserve power because there are no fault scenarios that are indicated externally in the Sleep mode.

9.3.2.4 EN Pin

EN is a logic-level input signal, referenced to V_{IO}, from a CAN FD controller to the TCAN1463-Q1. The EN input pin is for mode selection in conjunction with the nSTB pin. EN is internally pulled low to prevent excessive system power and false wake-up events.

9.3.2.5 nSTB Pin

nSTB is a logic-level input signal, referenced to V_{IO}, from a CAN FD controller to the TCAN1463-Q1. The nSTB input pin is for mode selection in conjunction with the EN pin. nSTB is internally pulled low to prevent excessive system power and false wake-up events.

9.3.2.6 INH_MASK Pin

INH_MASK is a logic-level input signal, referenced to V_{IO}, from a CAN FD controller to the TCAN1463-Q1. The INH_MASK input pin can be used to disable and enable the INH function when in Silent mode. This feature can be used to control the power supply to any power-intensive system blocks to avoid powering up the system blocks from low-power mode due to spurious wake-up events. INH_MASK function should not be used if the INH is used to control the power supply to the transceiver or the controller behind the transceiver - using INH_MASK in such a scenario would prevent the device from entering silent mode and enabling the INH function. See 図 10-2 for an example application schematic for using INH_MASK function.

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INH_MASK has a pull-down resistor that forces the INH feature to the enable state upon a cold start. To activate INH_MASK, the transceiver must be in silent mode. Once in silent mode, the INH_MASK pin is pulled high for t > t_{INH_MASK}, disabling INH. The TCAN1463-Q1 latches this value and retains it through V_{CC} and V_{IO} power cycles and state transitions. The latched value is lost if the TCAN1463-Q1 enters an undervoltage fault on V_{SUP}. To enable INH function again, the transceiver must be in Silent mode, and the INH_MASK pin must be pulled low for t > t_{INH_MASK}. See 図 8-10 and 図 8-11 for the procedure to use the INH_MASK feature.

The TCAN1463-Q1 reports a change in state of INH_MASK to the system controller by the driving nFAULT low while in silent mode. To use nFAULT=low as an acknowledgment for the change in state of INH_MASK , nFAULT must be high (that is, no pre-existing faults) before initiating the change in state of INH_MASK. A mode transition into normal, standby, go-to-sleep, or sleep mode clears the nFAULT pin.

9.3.3 GND

GND is the ground pin of the transceiver, it must be connected to the PCB ground.

9.3.4 INH Pin

The INH pin is a high-voltage output. It can be used to control external regulators. These regulators are usually used to support the microprocessor and V_{IO} pin. The INH function is on in all modes except for sleep mode. In sleep mode, the INH pin is turned off, going into a high-impedance state. This allows the node to be placed into the lowest power state while in sleep mode. A 100 kΩ load can be added to the INH output for a fast transition time from the driven high state to the low state and to force the pin low when left floating.

This terminal should be considered a high-voltage logic terminal, not a power output. The INH pin should be used to drive the EN terminal of the system's power management device and should not be used as a switch for the power management supply itself. This terminal is not reverse-battery protected and thus should not be connected outside the system module.

The INH function can be disabled/enabled using the INH_MASK pin in Silent mode. Refer to INH_MASK Pin for details.

9.3.5 WAKE Pin

The WAKE pin is a high-voltage reverse-blocked input used for the local wake-up (LWU) function. The WAKE pin is bi-directional edge-triggered and recognizes a local wake-up (LWU) on either a rising or falling edge of WAKE pin transition. The LWU function is explained further in the Local Wake-Up (LWU) via WAKE Input Terminal section.

9.3.6 CAN Bus Pins

These are the CAN high and CAN low, CANH and CANL, differential bus pins. These pins are internally connected to the CAN transceiver and the low-voltage wake receiver.

9.3.7 Faults

9.3.7.1 Internal and External Fault Indicators

The following device status indicator flags are implemented to allow for the MCU to determine the status of the device and the system. In addition to faults, the nFAULT terminal also signals wake-up requests and a "cold" power-up sequence on the V_{SUP} battery terminal so the system can do any diagnostics or cold booting sequence necessary. The RXD terminal indicates wake-up request and the faults are multiplexed (ORed) to the nFAULT output.

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表 9-1. TCAN1463-Q1 Transceiver Status Indicator

EVENT	FLAG NAME	CAUSE	INDICATORS(1)	FLAG IS CLEARED	COMMENT
Power-up	*PWRON*	Power up on V_{SUP} and any return of V_{SUP} after it has been below UV_{SUP}	nFAULT = low upon entering silent mode from standby or sleep mode	After a transition to normal mode	A cold start condition generates a local wake-up WAKERQ, *WAKESR* and a PWRON flag.
Wake-up Request	*WAKERQ* (2)	Wake-up event on CAN bus, state transition on WAKE pin, or initial power up	nFAULT = RXD = low after wake-up upon entering standby mode	After a transition to normal mode or $V_{CC} < UV_{CC(F)}$ or $V_{IO} < UV_{IO(F)}$ for $t \geq t_{UV}$	Wake-up request may only be set from standby, go-to-sleep, or sleep mode. Resets timers for UV_{VCC} or UV_{VIO}.
Wake-up Source Recognition(3)	*WAKESR*		Available upon entering normal mode(4) nFAULT = low indicates a local wake-up event from the WAKE pin nFAULT = high indicates a remote wake-up event from the CAN bus	After four recessive-to-dominant edges on TXD in normal mode, leaving normal mode, or $V_{CC} < UV_{CC(F)}$ or $V_{IO} < UV_{IO(F)}$ for $t \geq t_{UV}$	A cold start condition generates a local wake-up WAKERQ, *WAKESR* and a PWRON flag.
INH_MASK Change	*INHMASK*	INH_MASK value changed	nFAULT = low after entering silent mode	A mode transition into normal, standby, go-to-sleep, or sleep modes	To use nFAULT as the flag indicator, nFAULT must be high before initiating change in state of INH_MASK (e.g. there should be no pre-existing faults)
Undervoltage	UV_{CC}	$V_{CC} < UV_{CC(F)}$	Not externally indicated	$V_{CC} > UV_{CC(R)}$, or a wake-up request occurs	
	UV_{IO}	$V_{IO} < UV_{IO(F)}$	Not externally indicated	$V_{IO} > UV_{IO(R)}$, or a wake-up request occurs	
	UV_{SUP}	$V_{SUP} < UV_{SUP(F)}$	Not externally indicated	$V_{SUP} > UV_{SUP(R)}$	A V_{SUP} undervoltage event generates a cold start condition once $V_{SUP} > UV_{SUP(R)}$
CAN Bus Fault	*CBF*	See CAN Bus Fault	nFAULT = low in normal mode only(5)	Upon leaving normal mode, or if no CAN bus fault is detected for four consecutive dominant-to-recessive transitions of the TXD pin while in normal mode	CAN bus fault must persist for four consecutive dominant-to-recessive transitions
Local Faults	*TXDCLP*	TXD low when CAN active mode is entered	nFAULT = low upon entering silent mode from normal mode	RXD = low & TXD = high, TXD = high & a mode transition into normal, standby, go-to-sleep, or sleep modes	CAN driver remains disabled until the *TXDCLP* is cleared. CAN receiver remains active during the TXDCLP fault
	TXDDTO	TXD dominant time out, dominant (low) signal for $t \geq t_{TXDDTO}$			CAN driver remains disabled until the *TXDDTO* is cleared. CAN receiver remains active during the TXDDTO fault
	TXDRXD	TXD and RXD pins are shorted together for $t \geq t_{TXDDTO}$			CAN driver remains disabled until the *TXDRXD* is cleared. CAN receiver remains active during the TXDRXD fault
	CANDOM	CAN bus dominant fault, when dominant bus signal received for $t \geq t_{BUSDOM}$		RXD = high, or a transition into normal, standby, go-to-sleep, or sleep modes	CAN driver remains enabled during *CANDOM* fault
	TSD	Thermal shutdown, $T_J \geq T_{SDR}$		$T_J < T_{SDF}$ and RXD = low & TXD = high, or transition into normal, standby, go-to-sleep, or sleep modes	CAN driver remains disabled until the *TSD* event is cleared

(1) V_{IO} and V_{SUP} are present
(2) Transitions to go-to-sleep mode is blocked until WAKERQ flag is cleared
(3) Wake-up source recognition reflects the first wake up source. If additional wake-up events occur the source still indicates the original wake-up source
(4) Indicator is only available in normal mode until the flag is cleared
(5) CAN Bus failure flag is indicated after four dominant-to-recessive edges on TXD

9.3.7.1.1 Power-Up (*PWRON* Flag)

This is an internal and external flag that can be used to control the power-up sequence of the system. When a new battery connection to the transceiver is made the *PWRON* flag is set signifying a cold start condition. The TCAN1463-Q1 treats any undervoltage conditions on the V_{SUP}, $V_{SUP} < UV_{SUP(F)}$, as a cold start. Therefore, when the $V_{SUP} > UV_{SUP(R)}$ condition is met the TCAN1463-Q1 sets the *PWRON* flag which can be used by the system to enter a routine that is only called upon in cold start situations. The *PWRON* flag is indicated by nFAULT driven low after entering silent mode from either standby mode or sleep mode. This flag is cleared after a transition to normal mode.

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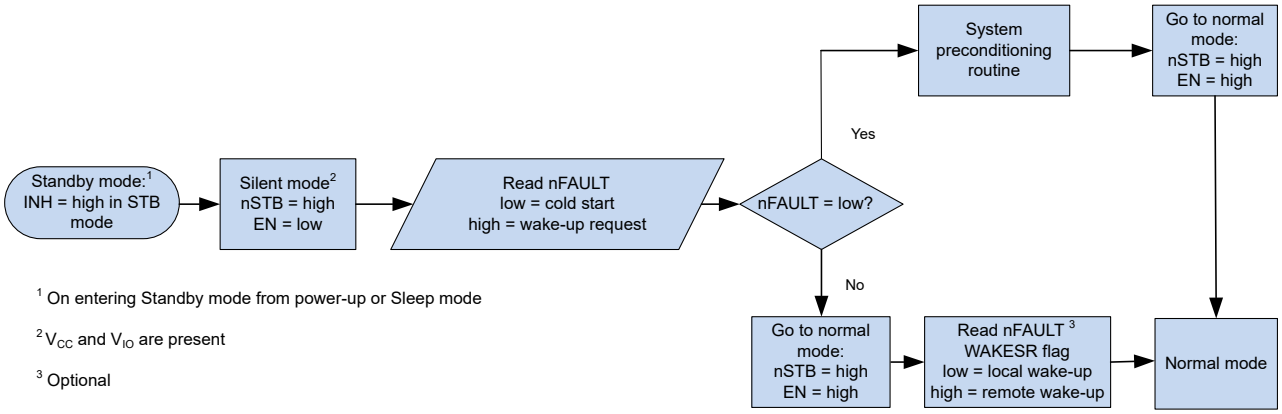


図 9-4. Distinguishing between *PWRON* and Wake Request by Entering Silent Mode

9.3.7.1.2 Wake-Up Request (*WAKERQ* Flag)

This is an internal and external flag that can be set in standby, go-to-sleep, or sleep mode. This flag is set when either a valid local wake-up (LWU) request occurs, or a valid remote wake request occurs, or on power up on V_{SUP}. The setting of this flag clears the t_{UV} timer for the UV_{CC} or UV_{IO} fault detection. This flag is cleared upon entering normal mode or during an undervoltage event on V_{CC} or V_{IO}.

9.3.7.1.3 Undervoltage Faults

The TCAN1463-Q1 device implements undervoltage detection circuits on all supply terminals: V_{SUP}, V_{CC}, and V_{IO}. The undervoltage flags are internal indicator flags and are not indicated on the nFAULT output pin.

9.3.7.1.3.1 Undervoltage on V_{SUP}

UV_{SUP} is set when the voltage on V_{SUP} drops below the undervoltage detection voltage threshold, UV_{SUP}. The PWRON and WAKERQ flags are set once $V_{SUP} > UV_{SUP(R)}$.

9.3.7.1.3.2 Undervoltage on V_{CC}

UV_{CC} is set when the voltage on V_{CC} drops below the undervoltage detection voltage threshold, UV_{CC}, for longer than the t_{UV} undervoltage filter time.

9.3.7.1.3.3 Undervoltage on V_{IO}

UV_{IO} is set when the voltage on V_{IO} drops below the undervoltage detection voltage threshold, UV_{IO}, for longer than the t_{UV} undervoltage filter time.

9.3.7.1.4 CAN Bus Fault (*CBF* Flag)

The TCAN1463-Q1 device can detect the following six fault conditions and set the nFAULT pin low as an interrupt so that the controller can be notified and act if a CAN bus fault exists. These failures are detected while transmitting a dominant signal on the CAN bus. If one of these fault conditions persists for four consecutive dominant-to-recessive bit transitions, the nFAULT indicates a CAN bus failure flag in Normal mode by driving the nFAULT pin low. The CAN bus driver remains active. 表 9-2 shows what fault conditions can be detected by the TCAN1463-Q1.

表 9-2. Bus Fault Pin State and Detection Table

FAULT	Condition
1	CANH Shorted to V_{BAT}
2	CANH Shorted to V_{CC}
3	CANH Shorted to GND
4	CANL Shorted to V_{BAT}
5	CANL Shorted to V_{CC}
6	CANL Shorted to GND

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Bus fault detection is a system level situation. If the fault is occurring at the ECU the general communication of the bus may be compromised. Until a diagnostic determination can be made the transceiver remains in CAN active mode during a CAN bus fault enabling the ECU to transmit data to the CAN bus and receive data from the CAN bus. For complete coverage of a node, a system level diagnostic step should be performed for each node and the information should be communicated back to a central point.

While in normal mode, if no CAN bus fault is detected for four consecutive dominant-to-recessive transitions on the TXD pin then the CBF flag is cleared and nFAULT is driven high. The bus fault failure circuitry is able to detect bus faults for a range of differential resistance loads (R_{CBF}) and for any time greater than t_{CBF}.

9.3.7.1.5 TXD Clamped Low (*TXDCLP* Flag)

TXDCLP is an external flag that is set if the transceiver detects that the TXD is clamped low before entering CAN active mode. If a *TXDCLP* condition exists the nFAULT pin is driven low upon entering silent mode from normal mode and the CAN bus driver is disabled until the fault is cleared. The *TXDCLP* flag is cleared at power-up, when entering CAN active mode with TXD recessive, or when TXD is recessive while RXD is dominant, if no other local failures exist.

9.3.7.1.6 TXD Dominant State Timeout (*TXDDTO* Flag)

TXDDTO is an external flag that is set if the TXD pin is held dominant for $t > t_{TXDDTO}$. If a TXD DTO condition exists, the nFAULT pin is driven low upon entering silent mode from normal mode. The *TXDDTO* flag is cleared on the next dominant-to-recessive transition on TXD or upon a transition into normal, standby, go-to-sleep, or sleep modes.

9.3.7.1.7 TXD Shorted to RXD Fault (*TXDRXD* Flag)

TXDRXD is an external flag that is set if the transceiver detects that the TXD and RXD lines have been shorted together for $t \geq t_{TXDDTO}$. If a *TXDRXD* condition exists the nFAULT pin is driven low upon entering silent mode from normal mode and the CAN bus driver is disabled until the *TXDRXD* fault is cleared. The *TXDRXD* flag is cleared on the next dominant-to-recessive transition with TXD high and RXD low or upon a transition into normal, standby, go-to-sleep, or sleep modes.

9.3.7.1.8 CAN Bus Dominant Fault (*CANDOM* Flag)

CANDOM is an external flag that is set if the CAN bus is stuck dominant state for $t > t_{BUSDOM}$. If a *CANDOM* condition exists the nFAULT pin is driven low upon entering silent mode from normal mode. The *CANDOM* flag is cleared on the next dominant-to-recessive transition on RXD or upon a transition into normal, standby, go-to-sleep, or sleep modes.

9.3.8 Local Faults

Local faults are detected in both normal mode and silent mode, but are only indicated via the nFAULT pin when the TCAN1463-Q1 transitions from normal mode to silent mode. All other mode transitions clear the local fault flag indicators.

9.3.8.1 TXD Clamped Low (TXDCLP)

If the TXD pin is clamped low prior to entering CAN active mode the CAN driver is disabled releasing the bus line to the recessive level. The CAN driver will be activated again when entering normal mode with TXD recessive, when TXD is recessive while RXD is dominant, if no other local failures exist, or on power-up. During a *TXDCLP* fault the high-speed receiver remains active and the RXD output pin will mirror the CAN bus.

9.3.8.2 TXD Dominant Timeout (TXD DTO)

While the CAN driver is in active mode a TXD dominant state timeout circuit prevents the local node from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the timeout period, $t > t_{TXDDTO}$. The TXD dominant state timeout circuit is triggered by a falling edge on the TXD pin. If no rising edge is seen before on TXD before $t > t_{TXDDTO}$ than the CAN driver is disabled releasing the bus lines to the recessive level. This keeps the bus free for communication between other nodes on the network.

The CAN driver will be activated again on the next dominant-to-recessive transition on the TXD pin. During a *TXDDTO* fault the high-speed receiver remains active and the RXD output pin will mirror the CAN bus.

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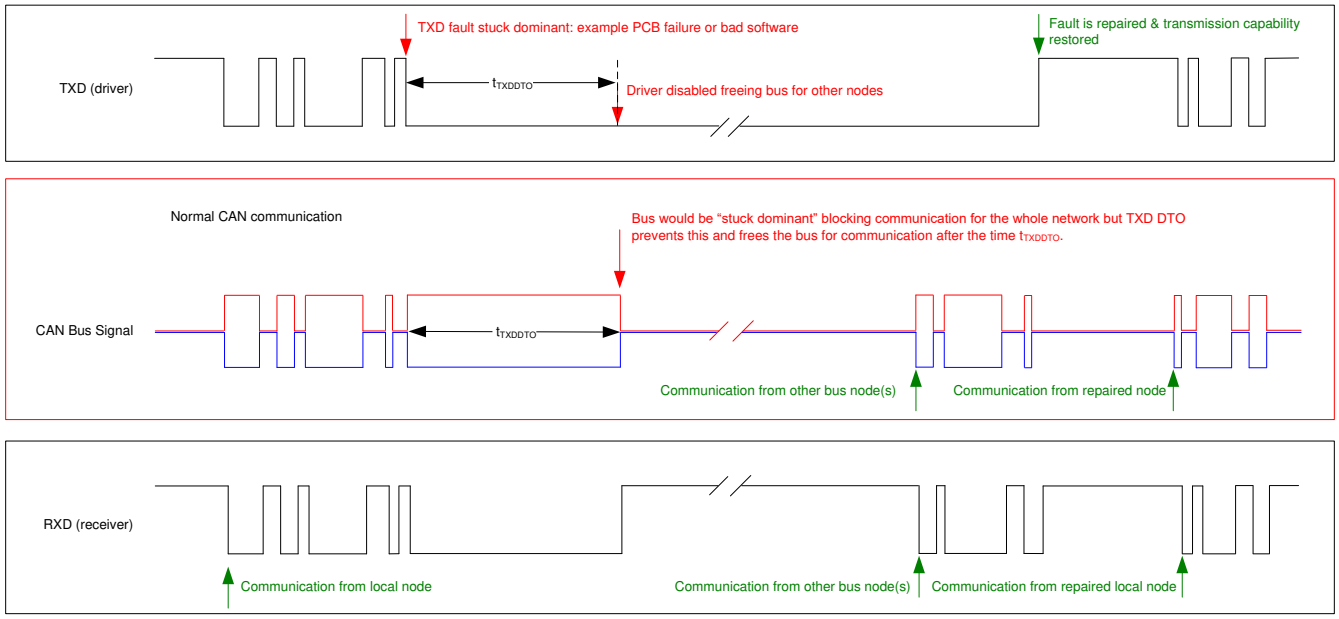


図 9-5. Timing Diagram for TXD DTO

The minimum dominant TXD time allowed by the dominant state timeout circuit limits the minimum possible transmitted data rate of the transceiver. The CAN protocol allows a maximum of eleven successive dominant bits to be transmitted in the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using the minimum t_{TXDDTO} time in 式 1.

$$\text{Minimum Data Rate} = 11 \text{ bits} / t_{TXDDTO} = 11 \text{ bits} / 1.2 \text{ ms} = 9.2 \text{ kbps} \quad (1)$$

9.3.8.3 Thermal Shutdown (TSD)

If the junction temperature of the TCAN1463-Q1 exceeds the thermal shutdown threshold the device turns off the CAN driver circuits thus blocking the TXD to bus transmission path. The CAN bus terminals are biased to recessive level during a *TSD* fault and the receiver to RXD path remains operational. The *TSD* fault condition is cleared when the junction temperature, T_J, of the device drops below the thermal shutdown release temperature, T_{SDF}, of the device. If the fault condition that caused the *TSD* fault is still present, the temperature may rise again and the device will enter thermal shutdown again. Prolonged operation with *TSD* fault conditions may affect device reliability. The TSD circuit includes hysteresis to avoid any oscillation of the driver output. During the fault the *TSD* fault condition is indicated to the CAN FD controller via the nFAULT terminal.

9.3.8.4 Undervoltage Lockout (UVLO)

The supply terminals, V_{SUP}, V_{IO} and V_{CC}, are monitored for undervoltage events. If an undervoltage event occurs the TCAN1463-Q1 enters a protected state where the bus pins present no load to the CAN bus. This protects the CAN bus and system from unwanted glitches and excessive current draw that could impact communication between other CAN nodes on the CAN bus.

If an undervoltage event occurs on V_{SUP} in any mode, the TCAN1463-Q1 CAN transceiver enters the CAN off state.

If an undervoltage event occurs on $V_{CC,}$ the TCAN1463-Q1 remains in normal or silent mode but the CAN transceiver changes to the CAN autonomous active state. During a UV_{CC} event, RXD remains high as long as V_{IO} is present and the wake-up circuitry is inactive. See 図 9-12. If the undervoltage event persists longer than t_{UV}, the TCAN1463-Q1 transitions to sleep mode.

If an undervoltage event occurs on the V_{IO}, the TCAN1463-Q1 transitions to standby mode. If the undervoltage event persists longer than t_{UV}, the TCAN1463-Q1 transitions to sleep mode.

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Once an undervoltage condition is cleared and the supplies have returned to valid levels, the device typically needs 200 µs to transition to normal operation.

9.3.8.5 Unpowered Devices

The device is designed to be a passive or no load to the CAN bus if it is unpowered. The CANH and CANL pins have low leakage currents when the device is unpowered, so they present no load to the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains in operation.

The logic terminals also have low leakage currents when the device is unpowered so they do not load down other circuits which may remain powered.

9.3.8.6 Floating Terminals

The TCAN1463-Q1 has internal pull-ups and pull-downs on critical pins to make sure a known operating behavior if the pins are left floating. See 表 9-3 for the pin fail-safe biasing protection description.

表 9-3. Pin Fail-safe Biasing

PIN	FAIL-SAFE PROTECTION	VALUE	COMMENT
TXD	Recessive level	60 kΩ	Weak pull-up to V_{IO}
EN	Low-power mode		Weak pull-down to GND
nSTB	Low-power mode		Weak pull-down to GND
INH_MASK	INH_MASK pin pulled to GND to disable INH_MASK function at powerup and when the feature is not needed.		Weak pull-down to GND

This internal bias should not be relied upon by design but rather a fail-safe option. Special care needs to be taken when the transceiver is used with a CAN FD controller that has open-drain outputs. The TCAN1463-Q1 implements a weak internal pull-up resistor on the TXD pin. The bit timing requirements for CAN FD data rates require special consideration and the pull-up strength should be considered carefully when using open-drain outputs. An adequate external pull-up resistor must be used to make sure the TXD output of the CAN FD controller maintains proper bit timing input to the CAN device.

9.3.8.7 CAN Bus Short-Circuit Current Limiting

The TCAN1463-Q1 has several protection features that limit the short-circuit current when a CAN bus line is shorted. These include CAN driver current limiting in the dominant and recessive states and TXD dominant state timeout which prevents permanently having the higher short-circuit current of a dominant state in case of a system fault.

During CAN communication the bus switches between the dominant and recessive states, thus the short-circuit current may be viewed either as the current during each bus state or as an average current. The average short-circuit current should be used when considering system power for the termination resistors and common-mode choke. The percentage of time that the driver can be dominant is limited by the TXD dominant state timeout and the CAN protocol which has forced state changes and recessive bits such as bit stuffing, control fields, and interframe spacing. These makes sure there is a minimum recessive time on the bus even if the data field contains a high percentage of dominant bits.

The short-circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short-circuit currents. The average short-circuit current may be calculated using 式 2.

$$I_{OS(AVG)} = \%Transmit \times [(\%REC_Bits \times I_{OS(SS)_REC}) + (\%DOM_Bits \times I_{OS(SS)_DOM})] + [\%Receive \times I_{OS(SS)_REC}] \quad (2)$$

Where:

- $I_{OS(AVG)}$ is the average short-circuit current
- %Transmit is the percentage the node is transmitting CAN messages
- %Receive is the percentage the node is receiving CAN messages
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages

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- $I_{OS(SS)_REC}$ is the recessive steady state short-circuit current
- $I_{OS(SS)_DOM}$ is the dominant steady state short-circuit current

The short-circuit current and possible fault cases of the network should be taken into consideration when sizing the power ratings of the termination resistance and other network components.

9.4 Device Functional Modes

The TCAN1463-Q1 has six operating modes: normal, standby, silent, go-to-sleep, sleep, and off mode. Operating mode selection is controlled using the nSTB pin and EN pin in conjunction with supply conditions, temperature conditions, and wake events.

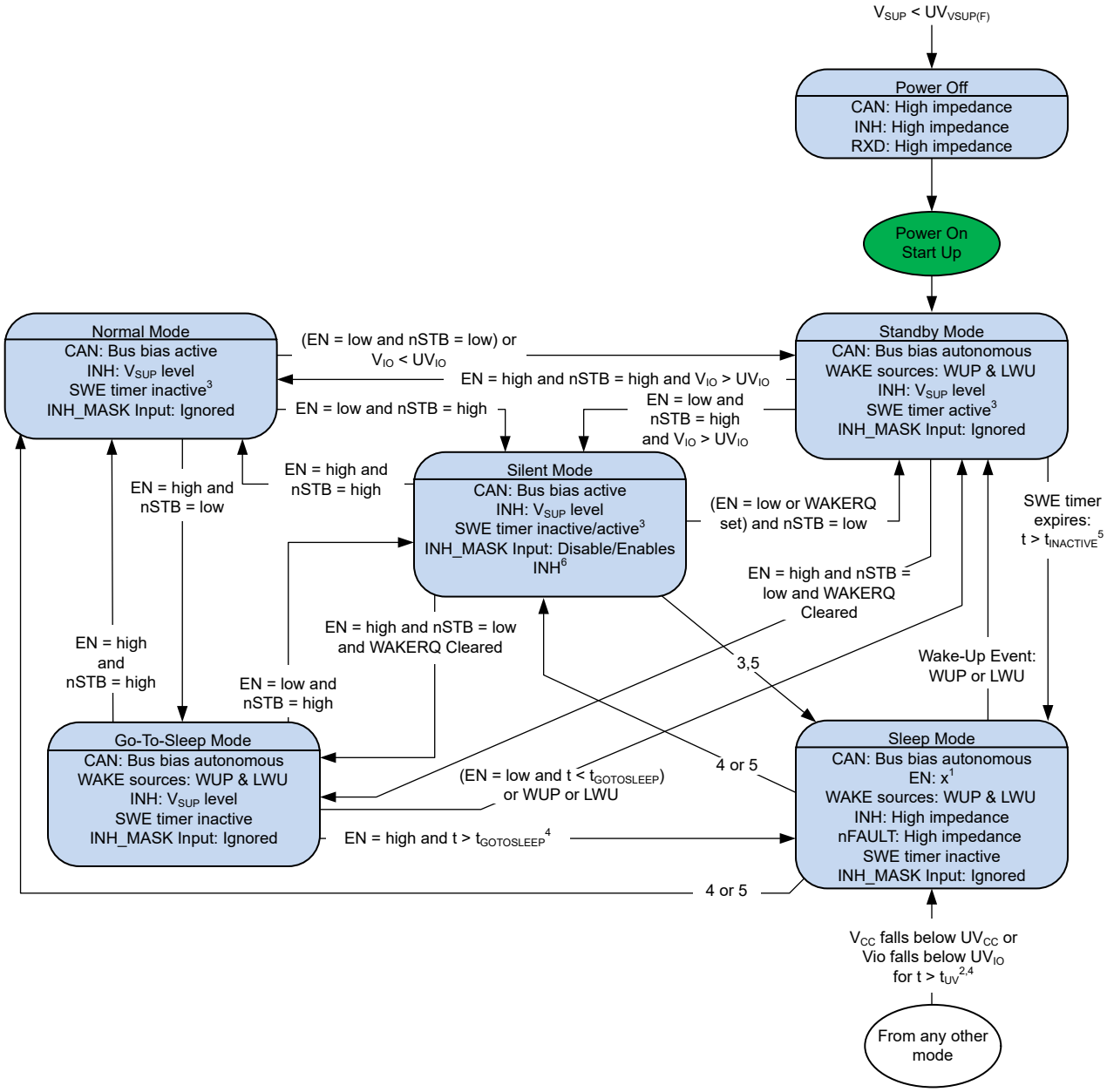
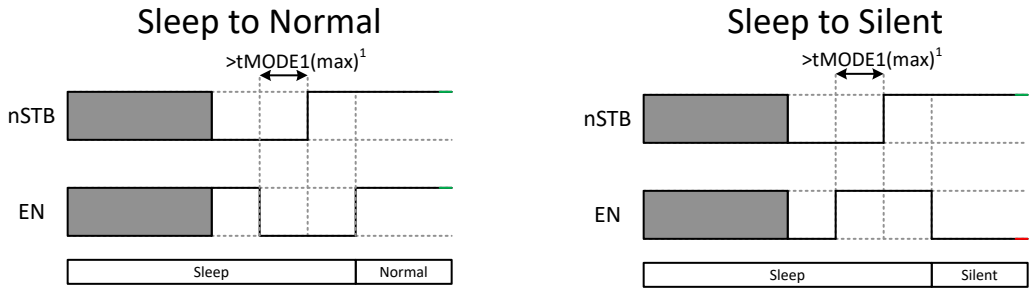


図 9-6. TCAN1463-Q1 State Machine

1. The enable pin can be in a logical high or low state while in sleep mode but since it has an internal pull-down, the lowest possible power consumption occurs when the pin is left either floating or pulled low externally.

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2. At power-up, the undervoltage timers for V_{CC} and V_{IO} are disabled, allowing for longer period for V_{CC} and V_{IO} supplies to power up (up to $t_{INACTIVE}$). V_{CC} or V_{IO} need to be above $UV_{CC(R)}$ and $UV_{IO(R)}$ respectively to enable their respective t_{UV} timers. The V_{CC} undervoltage timer starts when V_{CC} falls below $UV_{CC(F)}$, while V_{IO} undervoltage timer starts when V_{IO} falls below $UV_{IO(F)}$. When either of these timers exceed t_{UV}, the device enters sleep mode.
3. The Sleep Wake Error (SWE) timer starts as soon as the device enters Standby mode. The timer halts and resets as soon as the device enters Normal mode. If the device enters Silent mode from Standby mode, the SWE timer does not halt and the device needs to be transitioned to Normal mode before the SWE timer expires. If the device enters Silent mode from Normal mode, the SWE timer will not be active in Silent mode.
4. When the Sleep mode is entered from Go-To-Sleep Mode or from a UV_{CC} or UV_{IO} event, a low-to-high transition on nSTB is required to move the device into Normal or Silent mode. If EN is high during the rising edge on nSTB, the device moves to Normal mode. If EN is low during the rising edge on nSTB, the device moves to Silent mode. V_{IO} must be above $UV_{IO(R)}$ in order to leave Sleep mode using the EN and nSTB signals.
5. When Sleep mode is entered due to an SWE timer timeout (>$t_{INACTIVE}$), there is an extra requirement to exit Sleep mode and transition into Normal or Silent mode directly using the EN and nSTB signals. To move to Normal mode, the nSTB pin must be high and a low-to-high transition must occur on EN. To move to Silent mode, the nSTB pin must be high and a high-to-low transition must occur on EN. If the device entered Sleep mode while the nSTB was already high, there must be a transition on the EN pin while nSTB is low prior to the sequence described above. See 図 9-7 for more information. V_{IO} must be above $UV_{IO(R)}$ to leave Sleep mode by using the EN and nSTB signals.
6. The device recognizes the change in state of INH_MASK pin only in Silent mode to enable/disable INH functionality. Device latches the changed value of INH_MASK in Silent mode and retains this value through mode transitions. The latched value is lost only due to an UV_{SUP} event. The INH_MASK input is ignored in all other modes.



1. nSTB must remain low for a minimum of t_{MODE1} after the edge on EN. Once this t_{MODE1} has elapsed, nSTB may be driven high. The following edge on EN will cause the device to exit Sleep mode. The final edge on EN does not have any minimum delay from the rising edge of nSTB. The enable pin can be in a logical high or low state while in sleep mode, but since it has an internal pull-down, the lowest possible power consumption occurs when the pin is left either floating or pulled low externally.

図 9-7. TCAN1463-Q1 Transitioning from Sleep Mode to Normal or Silent Mode if Sleep Mode is Entered Due to SWE Timer Timeout

表 9-4. TCAN1463-Q1 Mode Overview

MODE	V_{CC} and V_{IO}	V_{SUP}	EN	nSTB	WAKERQ FLAG	DRIVER	RECEIVER	RXD	INH
Normal	> UV_{CC} and > UV_{IO}	> UV_{SUP}	High	High	X	Enabled	Enabled	Mirrors bus state	On
Silent	> UV_{CC} and > UV_{IO}	> UV_{SUP}	Low	High	X	Disabled	Enabled	Mirrors bus state	On
Standby	> UV_{CC} and > UV_{IO}	> UV_{SUP}	High	Low	Set	Disabled	Low power bus monitor enabled	Low signals wake-up	On
	> UV_{CC} and > UV_{IO}	> UV_{SUP}	Low	Low	X	Disabled	Low power bus monitor enabled	Low signals wake-up	On
	> UV_{CC} and < UV_{IO}	> UV_{SUP}	Low	Low	X	Disabled	Low power bus monitor enabled	High impedance	On
Go-to-sleep(1)	> UV_{CC} and > UV_{IO}	> UV_{SUP}	High	Low	Cleared	Disabled	Low power bus monitor enabled	High or high impedance (no V_{IO})	On(2)

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表 9-4. TCAN1463-Q1 Mode Overview (continued)

MODE	V_{CC} and V_{IO}	V_{SUP}	EN	nSTB	WAKERQ FLAG	DRIVER	RECEIVER	RXD	INH
Sleep[3]	> UV_{CC} and > UV_{IO}	> UV_{SUP}	High	Low	Cleared	Disabled	Low power bus monitor enabled	High or high impedance (no V_{IO})	High Impedance
	< UV_{CC} or <UV_{IO}	> UV_{SUP}	X	X	X	Disabled	Low power bus monitor enabled	High or high impedance (no V_{IO})	High impedance
Protected	X	< UV_{SUP}	X	X	X	Disabled	Disabled	High impedance	High impedance

(1) Go-to-sleep: Transitional mode for EN = H, nSTB = L until $t_{GOTOSLEEP}$ timer has expired.
(2) The INH pin transitions to high impedance after the $t_{GOTOSLEEP}$ timer has expired.
(3) Mode change from go-to-sleep mode to sleep mode once $t_{GOTOSLEEP}$ timer has expired.

9.4.1 Operating Mode Description

9.4.1.1 Normal Mode

This is the normal operating mode of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD.

Entering normal mode clears both the WAKERQ and the PWRON flags.

The SWE timer halts and resets upon entering normal mode.

9.4.1.2 Silent Mode

Silent mode is commonly referred to as listen only and receive only mode. In this mode, the CAN driver is disabled but the receiver is fully operational and CAN communication is unidirectional into the device. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD terminal.

In silent mode, PWRON and Local Failure flags are indicated on the nFAULT pin.

If the device enters silent mode from standby mode, the SWE timer does not halt and the device needs to be transitioned to normal mode before the SWE timer expires. If the SWE timer expires in silent mode, the device is transitioned to sleep mode.

9.4.1.3 Standby Mode

Standby mode is a low-power mode where the driver and receiver are disabled, reducing current consumption. However, this is not the lowest power mode of the device since the INH terminal is on, allowing the rest of the system to resume normal operation.

During standby mode, a wake-up request (*WAKERQ*) is indicated by the RXD terminal being low. The wake-up source is identified via the nFAULT pin after the device is returned to normal mode.

In standby mode, a fail-safe timer called Sleep Wake Error (SWE) timer is enabled. The timer adds an additional layer of protection by requiring the system controller to configure the transceiver to normal mode before it expires. This feature forces the TCAN1463-Q1 to transition to its lowest power mode, sleep mode, after $t_{INACTIVE}$ if the processor does not come up properly and fails to transition the device to Normal mode.

9.4.1.4 Go-To-Sleep Mode

Go-to-sleep mode is the transitional mode of the device from any state to sleep. In this state the driver and receiver are disabled, reducing the current consumption. The INH pin is active in order to supply an enable to the V_{IO} controller which allows the rest of the system to operate normally. If the device is held in this state for $t \geq t_{GOTOSLEEP}$ the device transitions to sleep mode and the INH turns off transitioning to the high impedance state.

If any wake-up events persist, the TCAN1463-Q1 remains in standby mode until the device is switched into normal mode to clear the pending wake-up events.

9.4.1.5 Sleep Mode

Sleep mode is the lowest power mode of the TCAN1463-Q1. In sleep mode, the CAN transmitter and the main receiver are switched off and the transceiver cannot send or receive data. The low power receiver is able to monitor the bus for any activity that validates the wake-up pattern (WUP) requirements, and the WAKE

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monitoring circuit monitors for state changes on the WAKE terminal for a local wake-up (LWU) event. I_{SUP} current is reduced to its minimum level when the CAN transceiver is in CAN autonomous inactive state. The INH pin is switched off in sleep mode causing any system power supplies controlled by INH to be switched off thus reducing system power consumption.

Sleep mode is exited:

- If a valid wake-up pattern (WUP) is received via the CAN bus pins
- On a local WAKE (LWU) event
- On a low-to-high transition of the nSTB pin

When the Sleep mode is entered due to an SWE timer timeout (>$t_{INACTIVE}$), there is an extra requirement to enter Normal or Silent mode directly (without entering Standby mode via LWU or WUP) using the EN and nSTB signals. In order to move to the Normal mode, the nSTB pin must be high and a low-to-high transition must occur on EN. In order to move to the Silent mode, the nSTB pin must be high and a high-to-low transition must occur on EN. If the device entered the Sleep mode while the nSTB was already high, there must be a transition on the EN pin while nSTB is low prior to the sequence described above. See 図 9-7 for more information. V_{IO} must be above $UV_{IO(R)}$ in order to leave the Sleep mode using the EN and nSTB signals.

9.4.1.5.1 Remote Wake Request via Wake-Up Pattern (WUP)

The TCAN1463-Q1 implements a low-power wake receiver in the standby and sleep mode that uses the multiple filtered dominant wake-up pattern (WUP) defined in the ISO11898-2:2016 standard.

The wake-up pattern (WUP) consists of a filtered dominant bus, then a filtered recessive bus time followed by a second filtered dominant bus time. The first filtered dominant initiates the WUP and the bus monitor is now waiting on a filtered recessive; other bus traffic will not reset the bus monitor. Once a filtered recessive is received the bus monitor is now waiting on a filtered dominant, and again, other bus traffic will not reset the bus monitor. Immediately upon receiving of the second filtered dominant the bus monitor will recognize the WUP and drive the RXD terminal low, if a valid V_{IO} is present signaling to the controller the wake-up request. If a valid V_{IO} is not present when the wake-up pattern is received the transceiver drives the RXD output pin low once V_{IO} > UV_{IOR}.

The WUP consists of:

- A filtered dominant bus of at least $t_{WK(FILTER)}$ followed by
- A filtered recessive bus time of at least $t_{WK(FILTER)}$ followed by
- A second filtered dominant bus time of at least $t_{WK(FILTER)}$

For a dominant or recessive to be considered “filtered,” the bus must be in that state for more than $t_{WK(FILTER)}$ time. Due to variability in the $t_{WK(FILTER)}$ the following scenarios are applicable. Bus state times less than the $t_{WK(FILTER)}$ minimum will never be detected as part of a WUP and thus no wake request will be generated. Bus state times between $t_{WK(FILTER)}$ minimum and $t_{WK(FILTER)}$ maximum may be detected as part of a WUP and a wake request may be generated. Bus state times more than $t_{WK(FILTER)}$ maximum will always be detected as part of a WUP and thus a wake request will always be generated. See 図 9-8 for the timing diagram of the WUP.

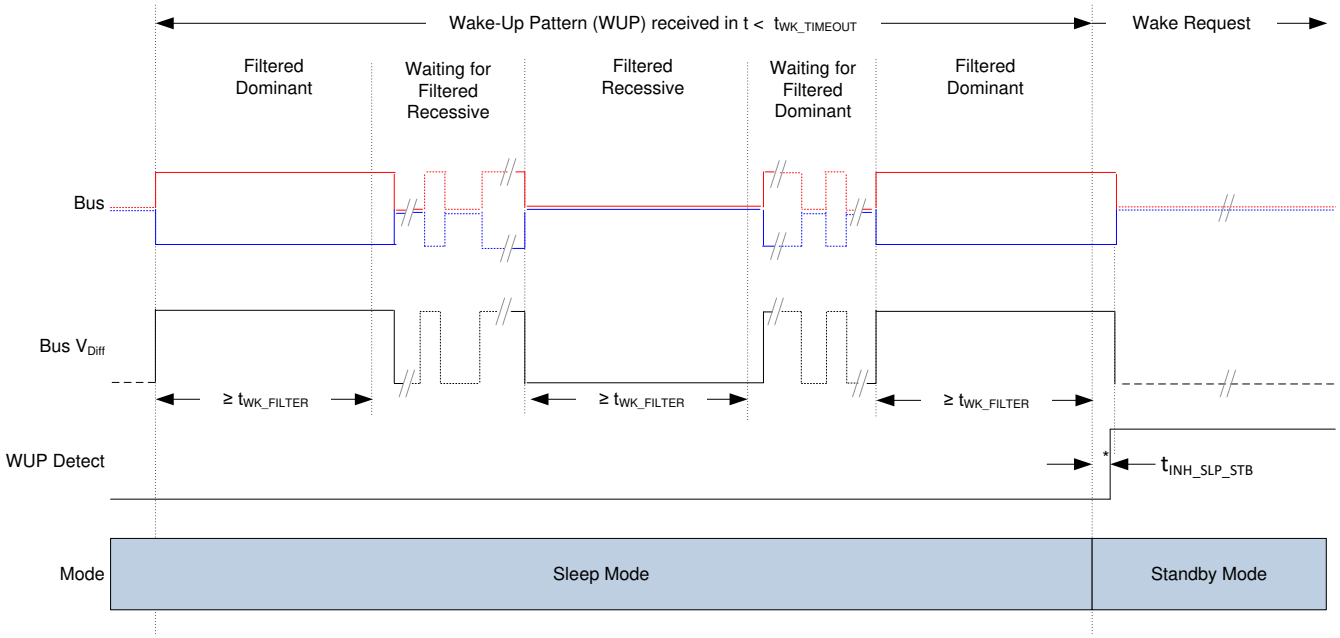
The pattern and $t_{WK(FILTER)}$ time used for the WUP and wake request prevents noise and bus stuck dominant faults from causing false wake requests while allowing any CAN or CAN FD message to initiate a wake request.

ISO11898-2:2016 has two sets of times for a short and long wake-up filter times. The $t_{WK(FILTER)}$ timing for the TCAN1463-Q1 has been picked to be within the min and max values of both filter ranges. This timing has been chosen such that a single bit time at 500 kbps, or two back to back bit times at 1 Mbps will trigger the filter in either bus state.

For an additional layer of robustness and to prevent false wake-ups, the transceiver implements the $t_{WK(TIMEOUT)}$ timer. For a remote wake-up event to successfully occur, the entire wake-up pattern must be received within the timeout value. If the full wake-up pattern is not received before the $t_{WK(TIMEOUT)}$ expires then the internal logic is reset and the transceiver remains in sleep mode without waking up. The full pattern must then be transmitted again within the $t_{WK(TIMEOUT)}$ window. See 図 9-8.

A recessive bus of at least $t_{WK(FILTER)}$ must separate the next WUP pattern if the CAN bus is dominant when the $t_{WK(TIMEOUT)}$ expires.

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*The RXD pin is only driven once V_{IO} is present.

図 9-8. Wake-Up Pattern (WUP)

9.4.1.5.2 Local Wake-Up (LWU) via WAKE Input Terminal

The WAKE terminal is a bi-directional high-voltage reverse-battery protected input which can be used for local wake-up (LWU) requests via a voltage transition. A LWU event is triggered on either a low-to-high or high-to-low transition since it has bi-directional input thresholds. The WAKE pin could be used with a switch to V_{SUP} or to ground. If the terminal is unused it should be pulled to V_{SUP} or ground to avoid unwanted parasitic wake-up events.

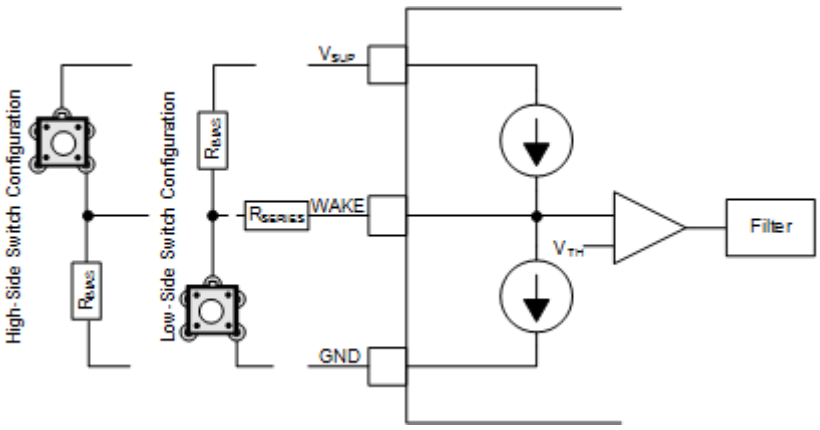


図 9-9. WAKE Circuit Example

図 9-9 shows two possible configurations for the WAKE pin, a low-side and high-side switch configuration. The objective of the series resistor, R_{SERIES}, is to protect the WAKE input of the device from over current conditions that may occur in the event of a ground shift or ground loss. The minimum value of R_{SERIES} can be calculated using the maximum supply voltage, V_{SUPMAX}, and the maximum allowable current of the WAKE pin, $I_{IO(WAKE)}$. R_{SERIES} is calculated using:

$$R_{SERIES} = V_{SUPMAX} / I_{IO(WAKE)} \quad (3)$$

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With absolute maximum voltage, V_{SUPMAX}, of 45 V and maximum allowable $I_{IO(WAKE)}$ of 3 mA, the minimum required R_{SERIES} value is 15 kΩ.

The R_{BIAS} resistor is used to set the static voltage level of the WAKE input when the switch is released. When the switch is in use in a high-side switch configuration, the R_{BIAS} resistor in combination with the R_{SERIES} resistor sets the WAKE pin voltage above the V_{IH} threshold. The maximum value of R_{BIAS} can be calculated using the maximum supply voltage, V_{SUPMAX}, the maximum WAKE threshold voltage V_{IH}, the maximum WAKE input current I_{IH} and the series resistor value R_{SERIES}. R_{BIAS} is calculated using:

$$R_{BIAS} < ((V_{SUPMAX} - V_{IH}) / I_{IH}) - R_{SERIES} \quad (4)$$

With V_{SUPMAX} of 45 V, V_{IH} of 44 V at I_{IH} of 3 µA, the R_{BIAS} resistor value must be less than 330 kΩ. It is recommended to use R_{Series} less than 50 kΩ to provide better margin for the WAKE pin voltage to rise above V_{IH} when the switch is released.

The LWU circuitry is active in sleep mode.

The WAKE circuitry is switched off in normal mode.

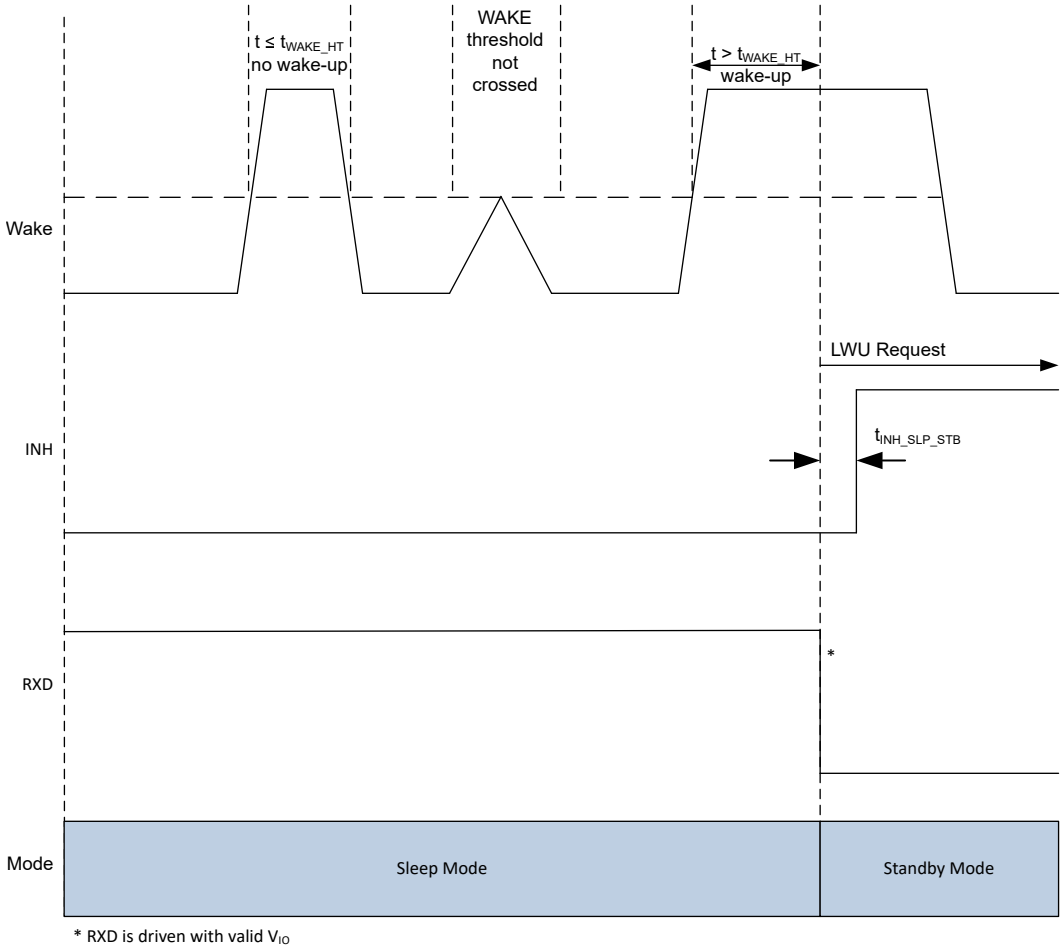


図 9-10. LWU Request Rising Edge

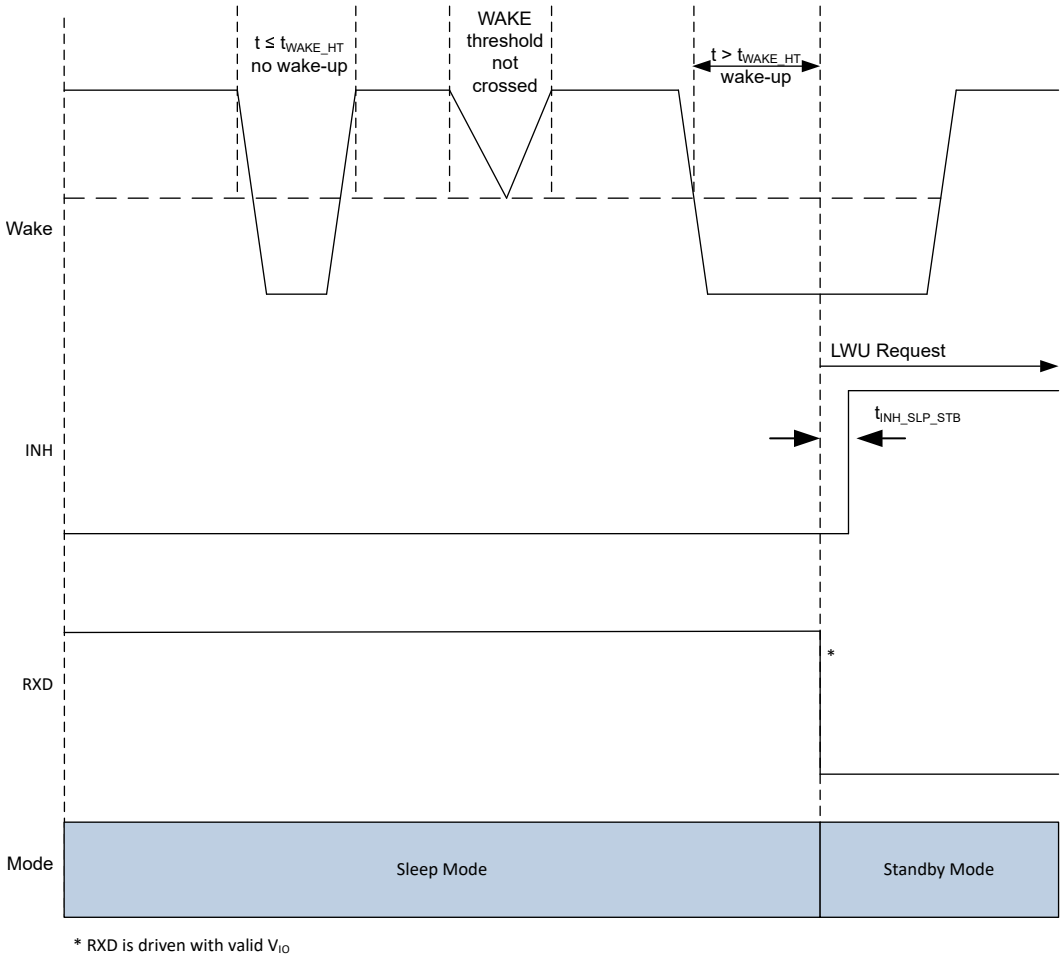


図 9-11. LWU Request Falling Edge

9.4.2 CAN Transceiver

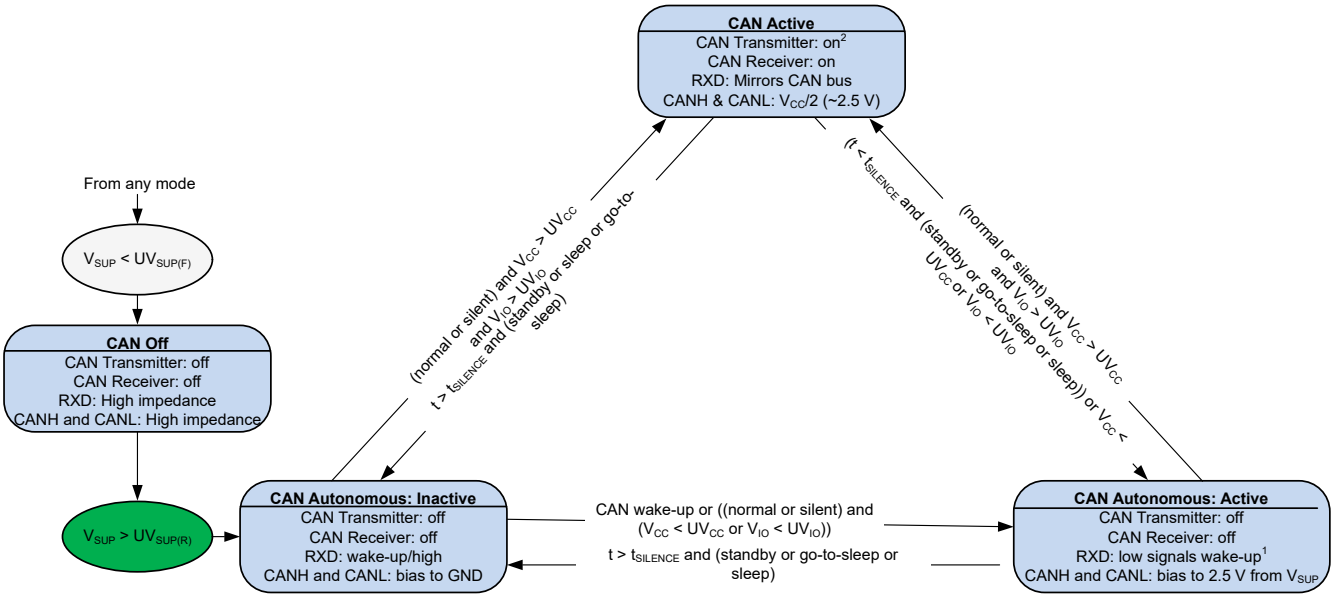
9.4.2.1 CAN Transceiver Operation

The TCAN1463-Q1 supports the ISO 11898-2:2016 CAN physical layer standard autonomous bus biasing scheme. Autonomous bus biasing enables the transceiver to switch between CAN active, CAN autonomous active, and CAN autonomous inactive which helps to reduce RF emissions.

9.4.2.1.1 CAN Transceiver Modes

The TCAN1463-Q1 CAN transceiver has four modes of operation; CAN off, CAN autonomous active, CAN autonomous inactive and CAN active.

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1. Wake-up is inactive in normal or silent mode.
2. CAN transmitter is off in silent mode.

図 9-12. TCAN1463-Q1 CAN Transceiver State Machine

9.4.2.1.1.1 CAN Off Mode

In CAN off mode, the CAN transceiver is switched off and the CAN bus lines are truly floating. In this mode, the device presents no load to the CAN bus while preventing reverse currents from flowing into the device if the battery or ground connection is lost.

The CAN off state is entered if:

- $V_{SUP} < UV_{SUPF}$

The CAN transceiver switches between the CAN off state and CAN autonomous inactive mode if:

- $V_{SUP} > UV_{SUPR}$

9.4.2.1.1.2 CAN Autonomous: Inactive and Active

When the CAN transceiver is in standby, go-to-sleep or sleep mode, the bias circuit can be in either the CAN autonomous inactive or CAN autonomous active state. In the autonomous inactive state, the CAN pins are biased to GND. When a remote wake-up (WUP) event occurs, the CAN bus is biased to 2.5 V and the CAN transceiver enters the CAN autonomous active state. If the controller does not transition the transceiver into normal mode before the $t_{SILENCE}$ timer expires, the CAN transceiver enters the CAN autonomous inactive state.

The CAN transceiver switches to the CAN autonomous mode if any of the following conditions are met:

- The operating mode changes from CAN off mode to CAN autonomous inactive
- The operating mode changes from normal or silent mode to standby, go-to-sleep, or sleep mode:
  - If the bus was inactive for $t < t_{SILENCE}$ before the mode change, the transceiver enters autonomous active state
  - If the bus was inactive for $t > t_{SILENCE}$ before the mode change, the transceiver enters autonomous inactive state
- $V_{CC} < UV_{CC(F)}$
- $V_{IO} < UV_{IO(F)}$

The CAN transceiver switches from the CAN autonomous inactive mode to the CAN autonomous active mode if:

- A remote wake-up event occurs
- The transceiver transitions to normal or silent mode and $V_{CC} < UV_{CC(F)}$ or $V_{IO} < UV_{IO(F)}$

The CAN transceiver switches from the CAN autonomous active mode to the CAN autonomous inactive mode if:

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- The transceiver is in standby, go-to-sleep, or sleep mode and t > $t_{SILENCE}$

9.4.2.1.1.3 CAN Active

When the transceiver is in normal or silent mode, the CAN transceiver is in active mode. In normal mode, the CAN driver and receiver are fully operational and CAN communication is bi-directional. In silent mode, the CAN driver is off but the CAN receiver is fully operational. The CAN bias voltage in CAN active mode is derived from V_{CC} and is held at V_{CC}/2

The CAN transceiver switches from the CAN autonomous inactive or CAN autonomous active modes to the CAN active mode if:

- The transceiver transitions to normal mode and V_{CC} > $UV_{CC(R)}$, V_{IO} > $UV_{IO(R)}$

The CAN transceiver blocks its transmitter after entering CAN active mode if the TXD pin is asserted low before leaving standby mode. This prevents disruptions to CAN bus in the event that the TXD pin is stuck Low (TXDCLP).

The CAN transceiver switches from the CAN active mode to the CAN autonomous inactive mode if:

- The transceiver switches to standby, go-to-sleep, or sleep modes and t > $t_{SILENCE}$

The CAN transceiver switches from the CAN active mode to the CAN autonomous active mode if:

- The transceiver switches to standby, go-to-sleep, or sleep modes and t < $t_{SILENCE}$
- V_{CC} < $UV_{CC(F)}$
- V_{IO} < $UV_{IO(F)}$

9.4.2.1.2 Driver and Receiver Function Tables

表 9-5. Driver Function Table

DEVICE MODE	TXD INPUTS(1)	BUS OUTPUTS		DRIVEN BUS STATE(2)
		CANH	CANL	
Normal	Low	High	Low	Dominant
	High or Open	High impedance	High impedance	V_{CC}/2
Silent	x	High impedance	High impedance	V_{CC}/2
Standby	x	High impedance	High impedance	Autonomous biasing
Sleep	x	High impedance	High impedance	Autonomous biasing

(1) x = irrelevant
(2) For bus states and typical bus voltages see 図 9-13

表 9-6. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} - V_{CANL}$	BUS STATE	RXD TERMINAL
Normal / Silent	V_{ID} ≥ 0.9 V	Dominant	Low
	0.5 V < V_{ID} < 0.9 V	Indeterminate	Indeterminate
	V_{ID} ≤ 0.5 V	Recessive	High
	Open (V_{ID} ≈ 0 V)	Open	High
Standby	V_{ID} ≥ 1.15 V	Dominant	High Low if wake-up event persists
	0.4 V < V_{ID} < 1.15 V	Indeterminate	
	V_{ID} ≤ 0.4	Recessive	
	Open (V_{ID} ≈ 0 V)	Open	
Sleep / Go-to-sleep(1)	V_{ID} ≥ 1.15 V	Dominant	High Tri-state if V_{IO} or V_{SUP} are not present
	0.4 V < V_{ID} < 1.15 V	Indeterminate	
	V_{ID} ≤ 0.4 V	Recessive	
	Open (V_{ID} ≈ 0 V)	Open	

(1) Low power wake-up receiver is active

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9.4.2.1.3 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See 図 9-13.

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to one half of the CAN transceiver supply voltage via the high resistance internal input resistors (R_{IN}) of the receiver and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the CAN bus is greater than the differential voltage of a single CAN driver. The TCAN1463-Q1 CAN transceiver implements low-power standby and sleep modes which enable a third bus state where, if the CAN bus is inactive for t > $t_{SILENCE}$, the bus pins are biased to ground via the high-resistance internal resistors of the receiver.

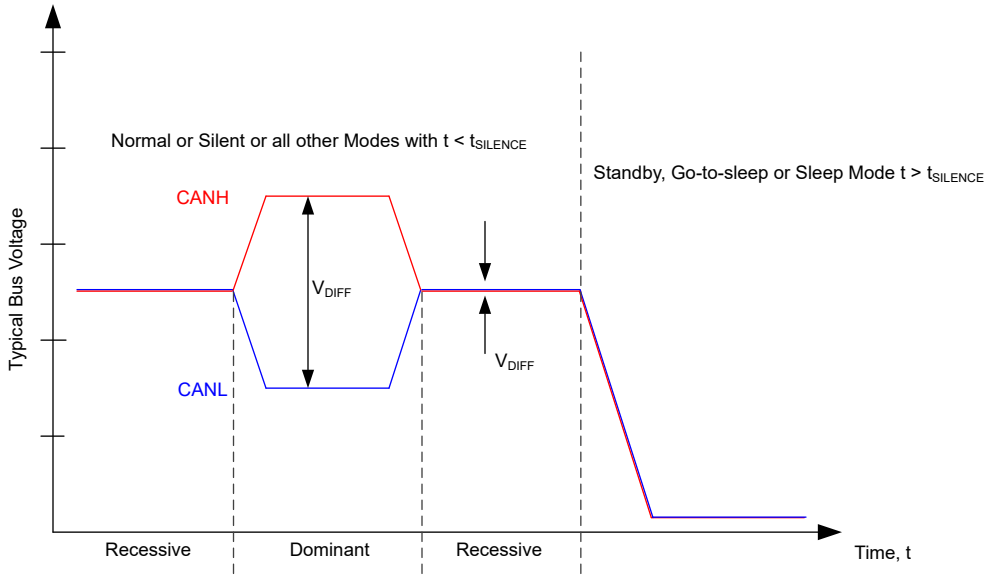


図 9-13. Bus States

10 Application Information Disclaimer

注

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10.1 Application Information

The TCAN1463-Q1 transceiver is typically used in applications with a host microprocessor or FPGA that includes the data link layer portion of the CAN protocol. These types of applications usually also include power management technology that allows for power to be gated to the application via an enable (EN) or inhibit (INH) pin. A single 5-V regulator can be used to drive both V_{CC} and V_{IO}, or independent 5-V and 3.3-V regulators can be used to drive V_{CC} and V_{IO} separately as shown in 図 10-1. The bus termination is shown for illustrative purposes.

The TCAN1463-Q1 features an INH_MASK feature. The INH_MASK input pin can be used to disable and enable the INH function as long as the INH is not controlling the power supply to the transceiver or the controller behind the transceiver. This feature can be used to control the power supply to any power-intensive system blocks to avoid powering up the system blocks from low-power mode due to spurious wake-up events which saves power. See 図 10-2 for an example application schematic.

10.1.1 Typical Application

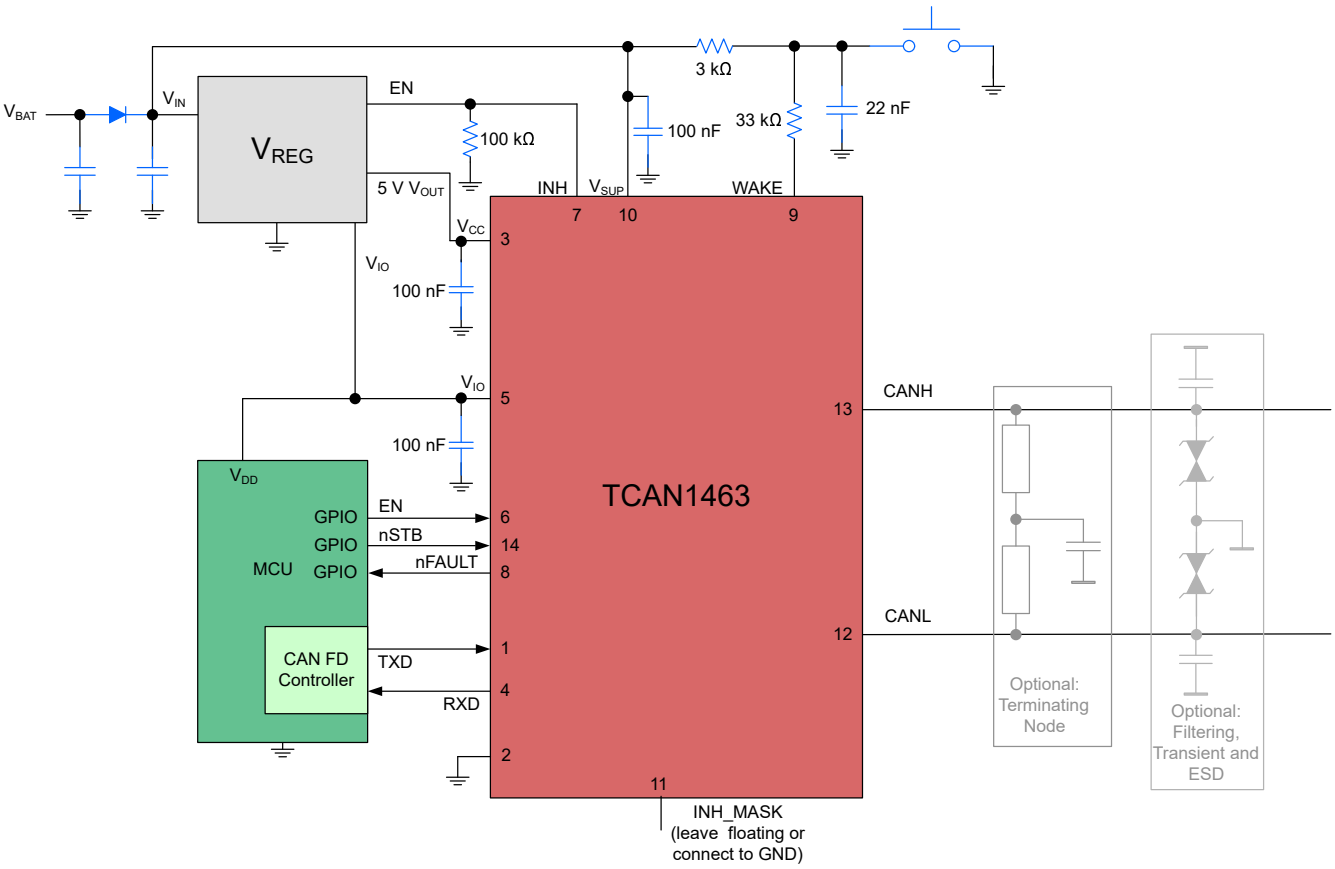


図 10-1. Typical Application (Not Using INH_MASK feature)

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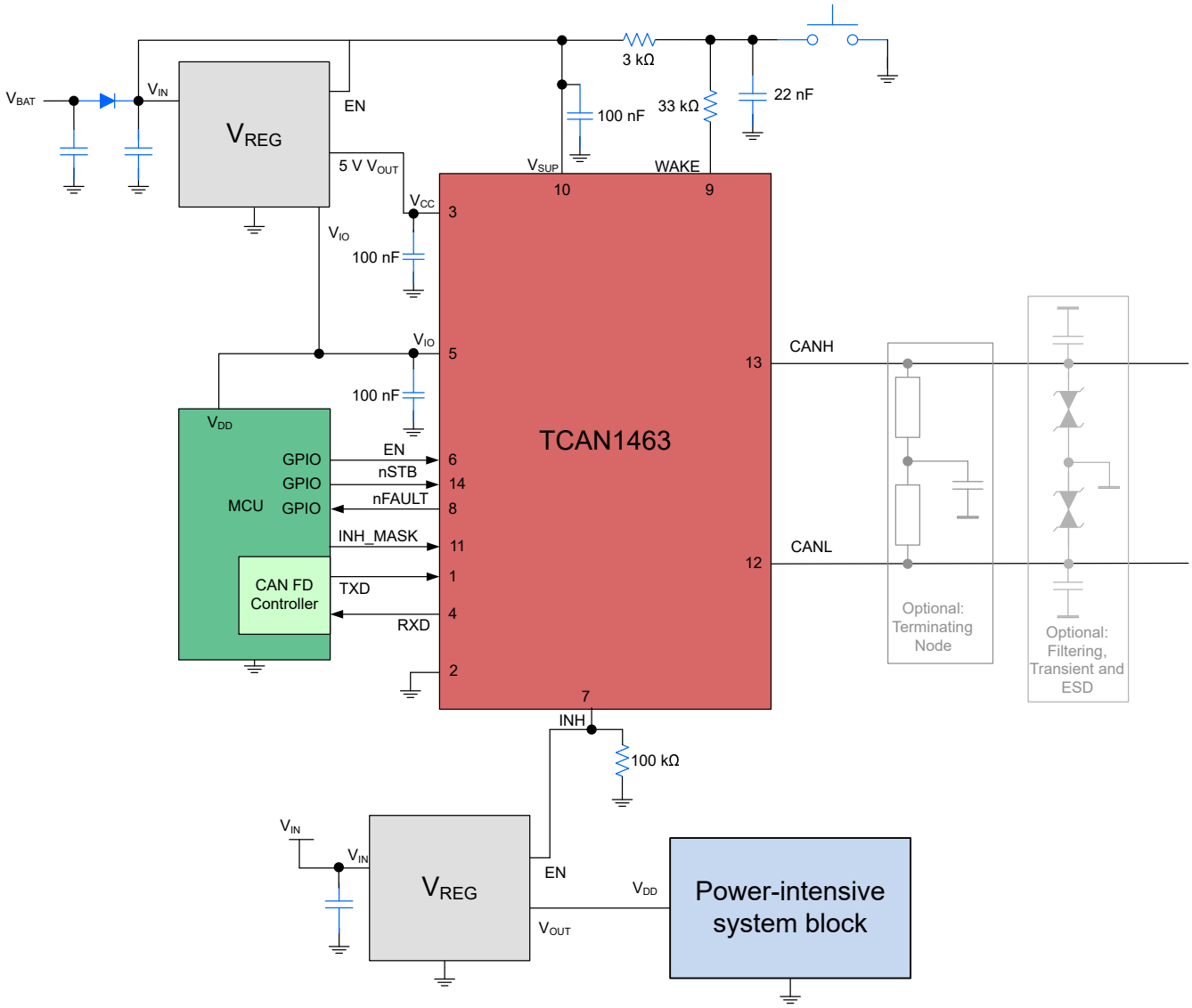


図 10-2. Typical Application (Using INH_MASK feature)

10.1.2 Design Requirements

10.1.2.1 Bus Loading, Length and Number of Nodes

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN1463-Q1.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO11898-2:2016 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC825, CANopen, DeviceNet, SAEJ2284, SAEJ1939, and NMEA200.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2016 specification the differential output driver is specified with a bus load that can range from 50 Ω to 65 Ω where the differential output must be greater than 1.5 V. The TCAN1463-Q1 is specified to meet the 1.5-V requirement down to 50 Ω and is specified to meet 1.4-V differential output at 45Ω bus load. The differential input resistance, R_{ID}, of the TCAN1463-Q1 is a minimum of 50 kΩ. If 100 TCAN1463-Q1 transceivers are in parallel on a bus, this is equivalent to a 500-Ω differential load in parallel with the nominal 60 Ω bus termination which gives a total bus load of approximately

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54 Ω. Therefore, the TCAN1463-Q1 theoretically supports over 100 transceivers on a single bus segment. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of its key strengths allowing for these system level network extensions and additional standards to build on the original ISO11898-2 CAN standard. However, when using this flexibility, the CAN network system designer must take the responsibility of good network design for a robust network operation.

10.1.3 Detailed Design Procedure

10.1.3.1 CAN Termination

Termination may be a single 120-Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired then split termination may be used, see 図 10-3. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

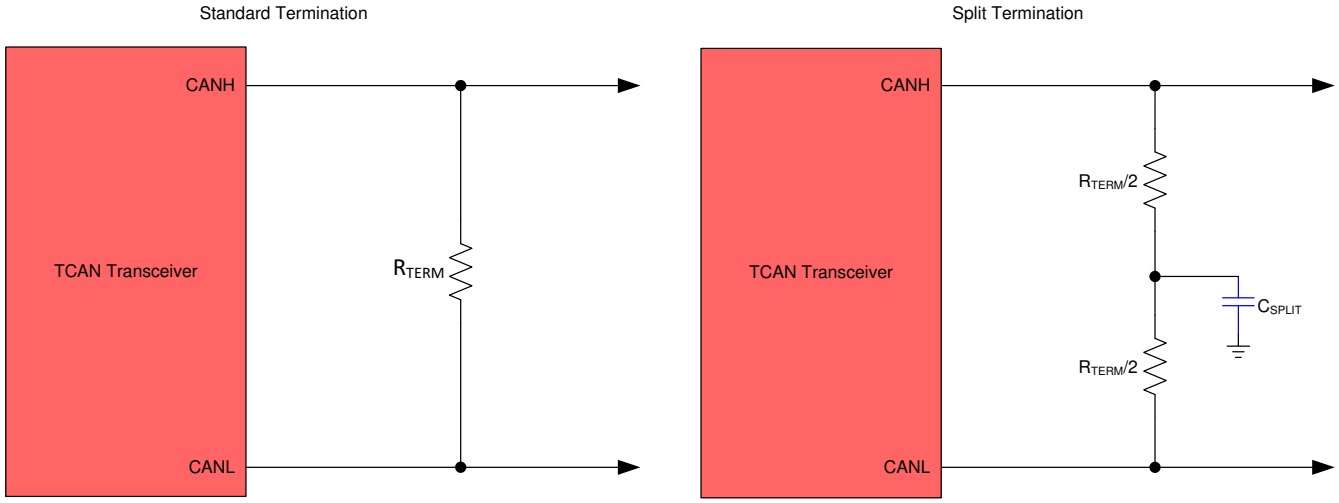


図 10-3. CAN Bus Termination Concepts

10.1.4 Application Curves

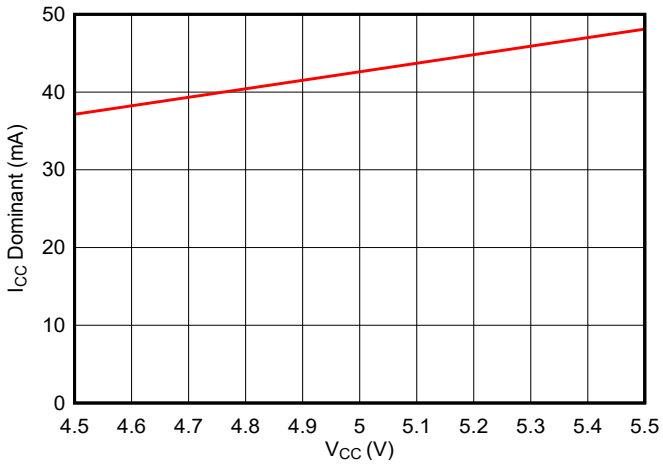


図 10-4. Current Consumption ($I_{CC(D)}$) in Dominant Mode vs V_{CC} Supply

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10.1.5 Power Supply Recommendations

The TCAN1463-Q1 is designed to operate off of three supply rails; V_{SUP}, V_{CC}, and V_{IO}. V_{SUP} is a high-voltage supply pin designed to connect to the V_{BAT} rail, V_{CC} is a low-voltage supply pin with an input voltage range from 4.5 V to 5.5 V that supports the CAN transceiver and V_{IO} is a low-voltage supply pin with an input voltage range from 1.7 V to 5.5 V that provides the I/O voltage to match the system controller. For a reliable operation, a 100 nF decoupling capacitor should be placed as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the output of switched-mode power supplies, and also helps to compensate for the resistance and inductance of the PCB power planes.

10.1.6 Layout

Robust and reliable CAN node design may require special layout techniques depending on the application and automotive design requirements. Since transient disturbances have high frequency content and a wide bandwidth, high-frequency layout techniques should be applied during PCB design.

10.1.6.1 Layout Guidelines

The layout example provides information on components around the device. Place the protection and filtering circuitry as close to the bus connector, J1, to prevent transients, ESD and noise from propagating onto the board. Transient voltage suppression (TVS) device can be added for extra protection, shown as D1. The production solution can be either a bi-directional TVS diode or varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors C6 and C7. A series common-mode choke (CMC) is placed on the CANH and CANL lines between the device and connector J1.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. Use supply and ground planes to provide low inductance. Note that high-frequency currents follow the path of least impedance and not the path of least resistance. Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

- Bypass and bulk capacitors should be placed as close as possible to the supply terminals of transceiver, examples are C1 on V_{CC}, C2 on V_{IO}, and C3 and C4 on the V_{SUP} supply.
- V_{IO} pin of the transceiver is connected to the microcontroller IO supply voltage 'µC V'.
- Bus termination: this layout example shows split termination. This is where the termination is split into two resistors, R3 and R4, with the center or split tap of the termination connected to ground via capacitor C5. Split termination provides common-mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to make sure the terminating node is not removed from the bus thus also removing the termination.
- INH, pin 7, can have a 100 kΩ resistor (R1) to ground.
- WAKE, pin 9, can recognize either a rising or a falling edge of a wake signal and is usually connected to an external switch. It should be configured as shown with C8 which is a 22 nF capacitor to GND where R5 is 33 kΩ and R6 is 3 kΩ.

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10.1.6.2 Layout Example

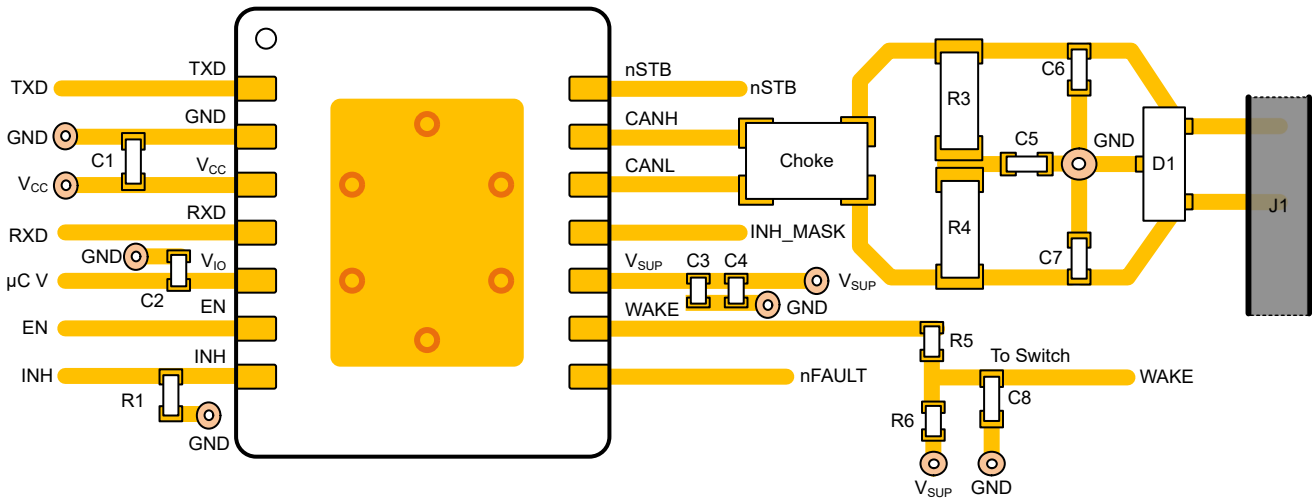


図 10-5. Example Layout

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11 Device and Documentation Support

11.1 Documentation Support

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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11.4 商標

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11.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCAN1463DMTRQ1	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	TCAN 1463
TCAN1463DMTRQ1.A	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	TCAN 1463
TCAN1463DRQ1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	TCAN1463
TCAN1463DRQ1.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	TCAN1463
TCAN1463DYYRQ1	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	TCAN1463
TCAN1463DYYRQ1.A	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	TCAN1463

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

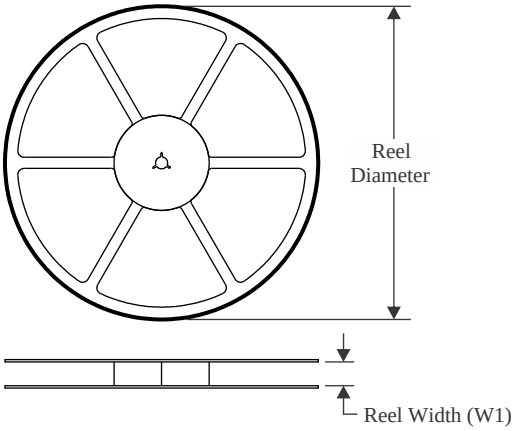
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

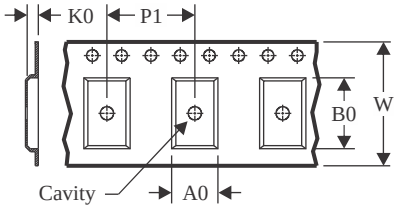
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

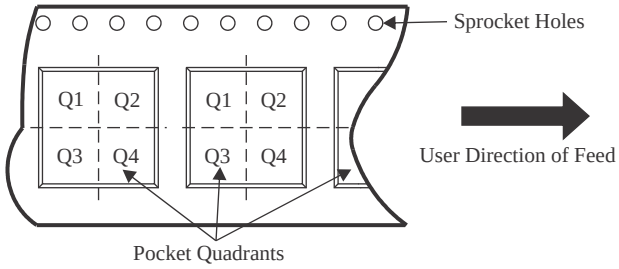


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

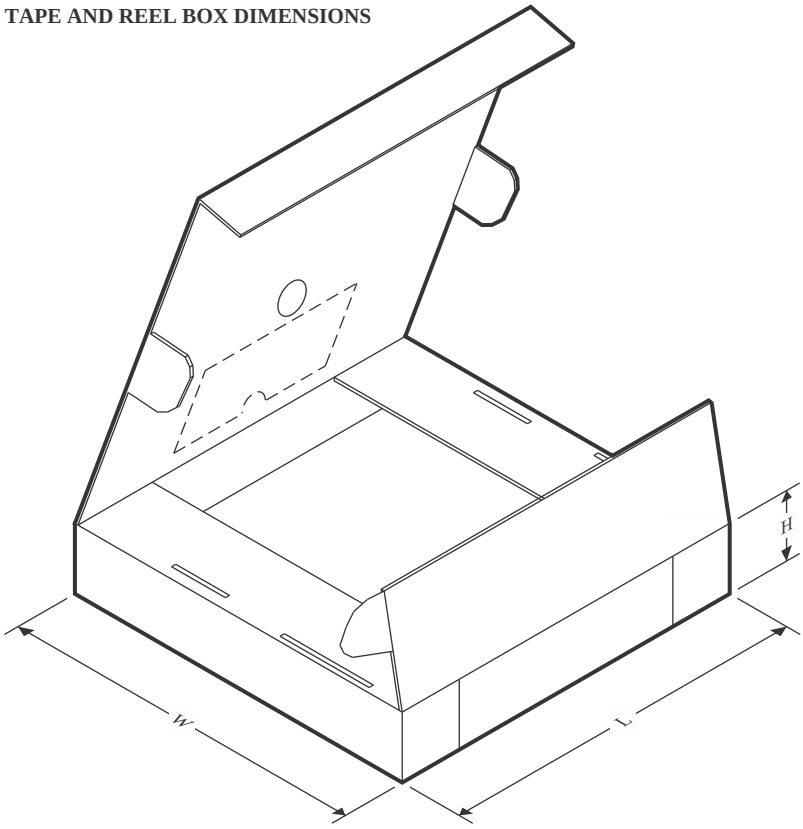
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

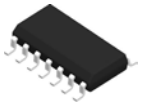
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1463DMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TCAN1463DRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TCAN1463DYYRQ1	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1463DMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0
TCAN1463DRQ1	SOIC	D	14	2500	353.0	353.0	32.0
TCAN1463DYYRQ1	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8

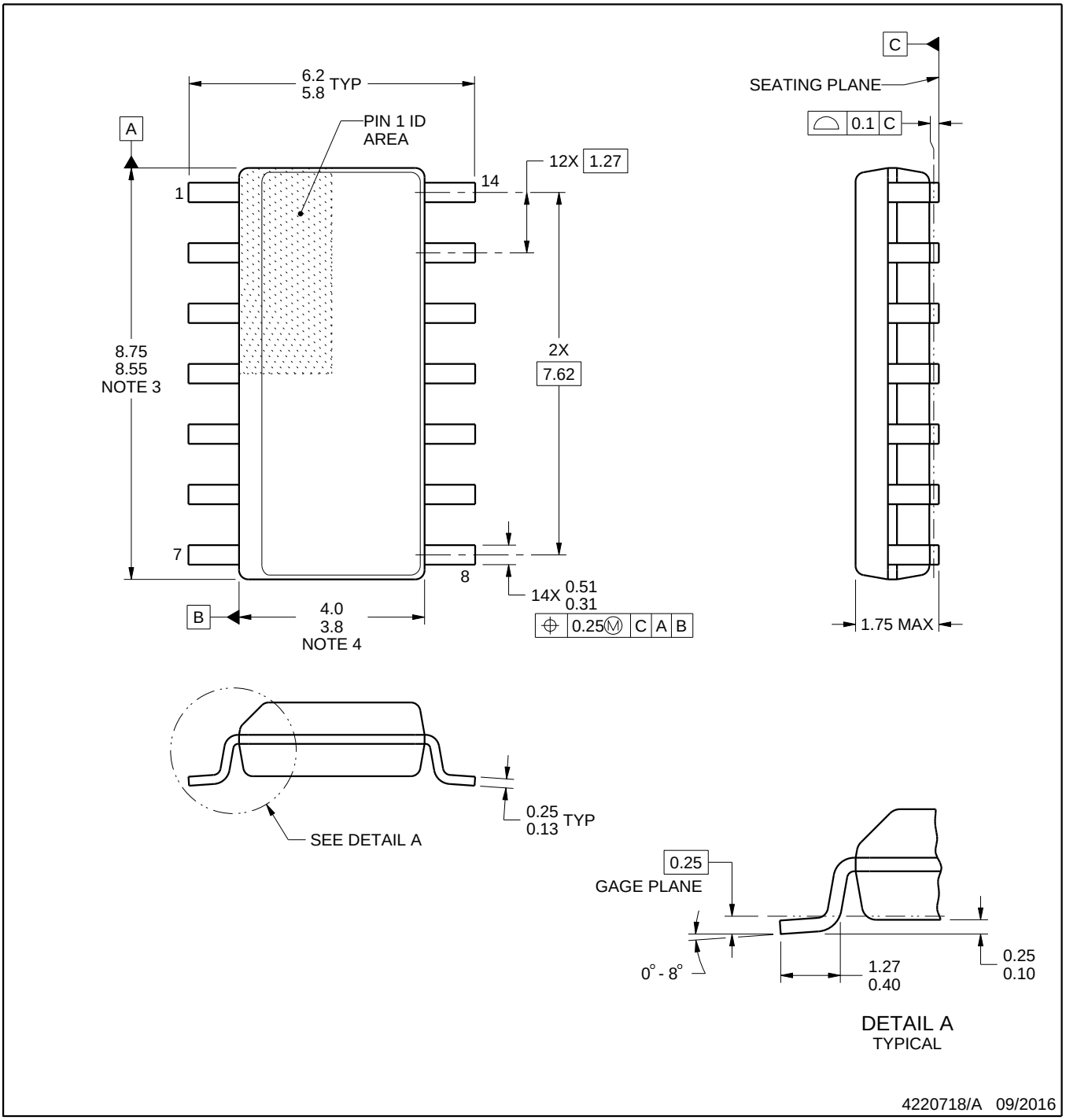


PACKAGE OUTLINE

D0014A

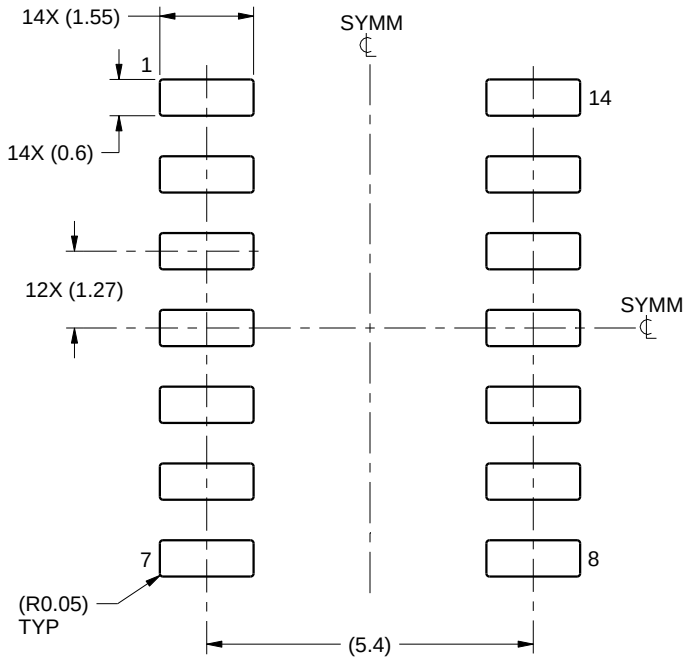
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

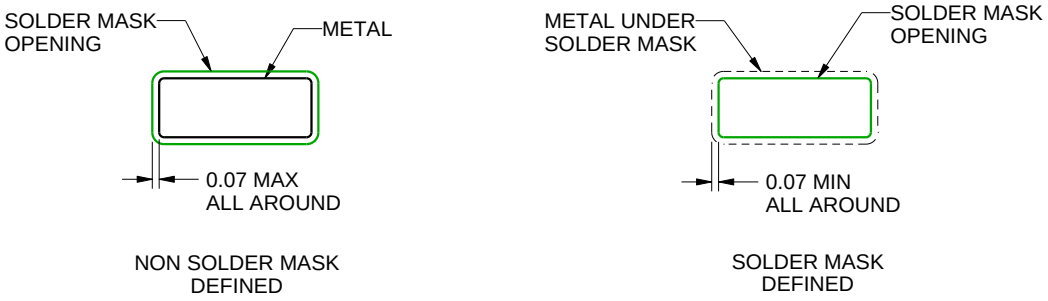


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

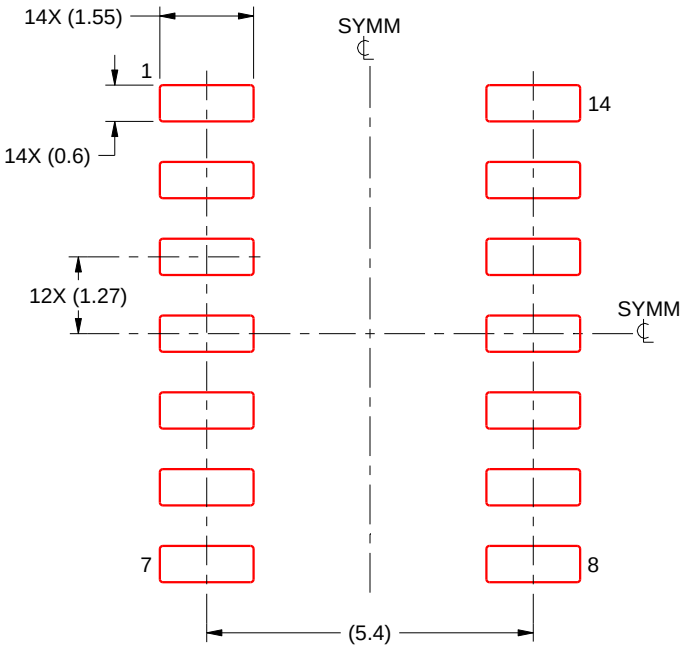
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

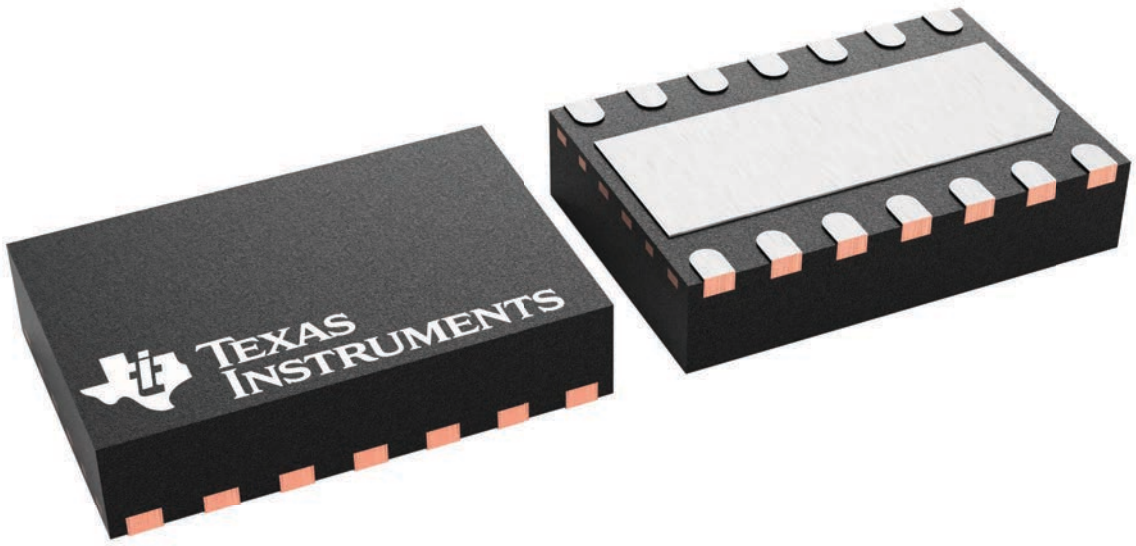
DMT 14

VSON - 0.9 mm max height

3 x 4.5, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



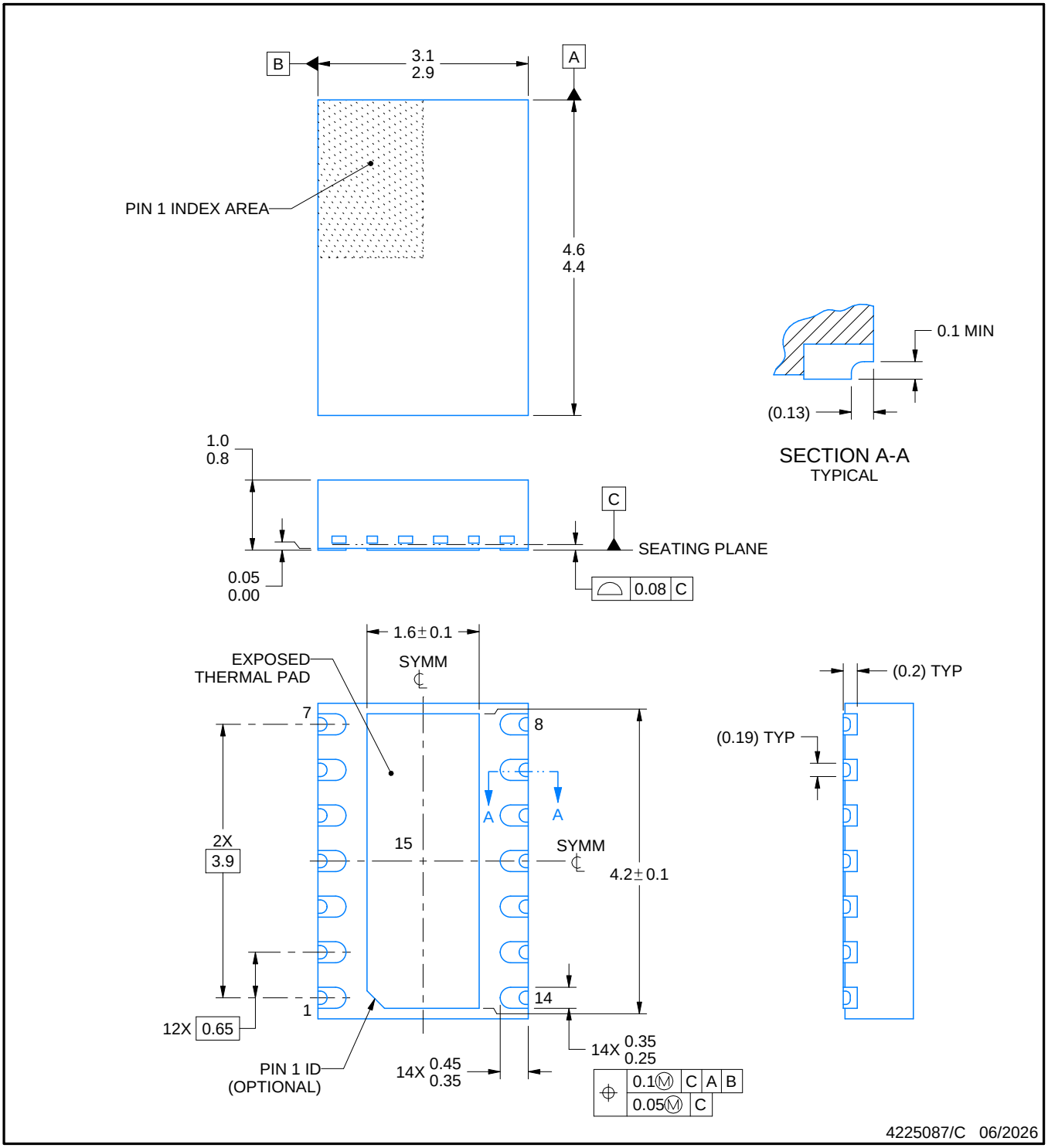
4225088/A

PACKAGE OUTLINE

DMT0014B

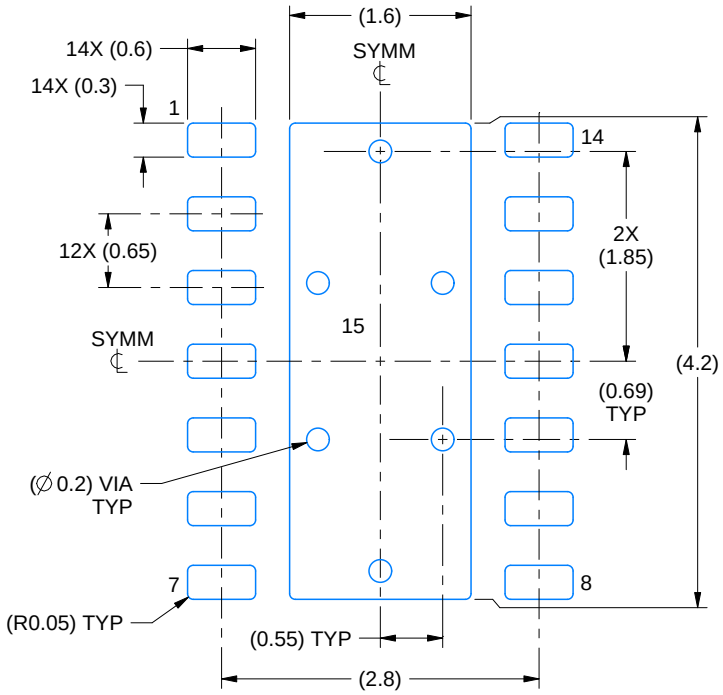
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

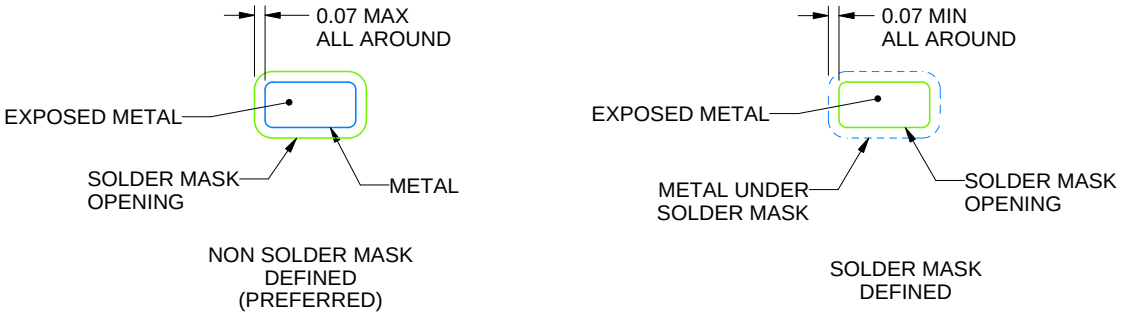


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Exposed side wall metal may vary is shape, size and quantity.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

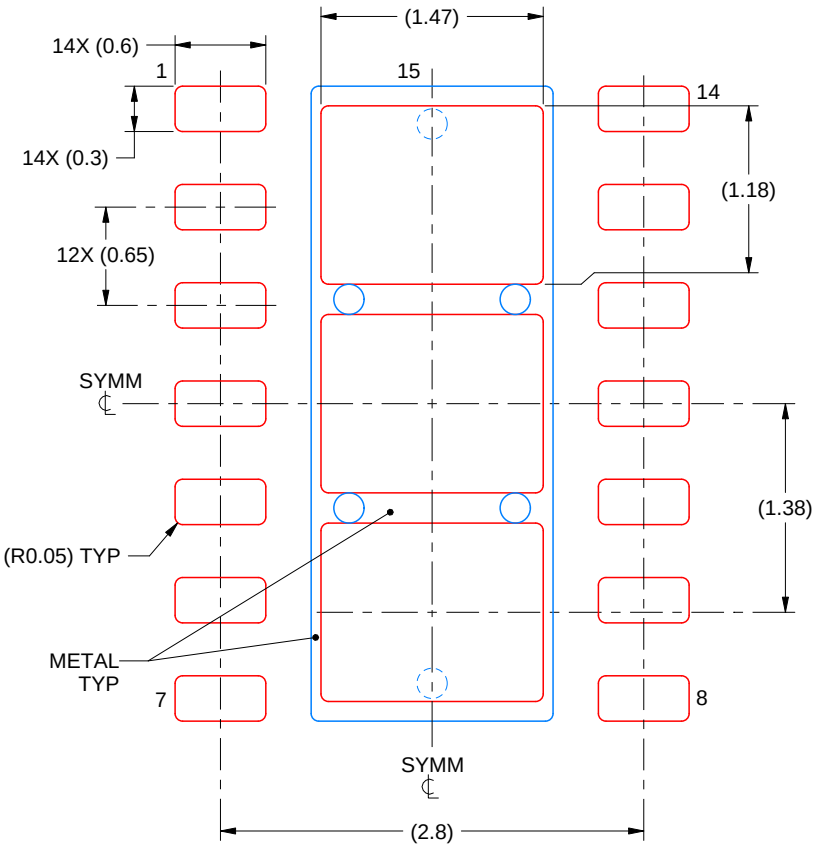


SOLDER MASK DETAILS

4225087/C 06/2026

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4225087/C 06/2026

NOTES: (continued)

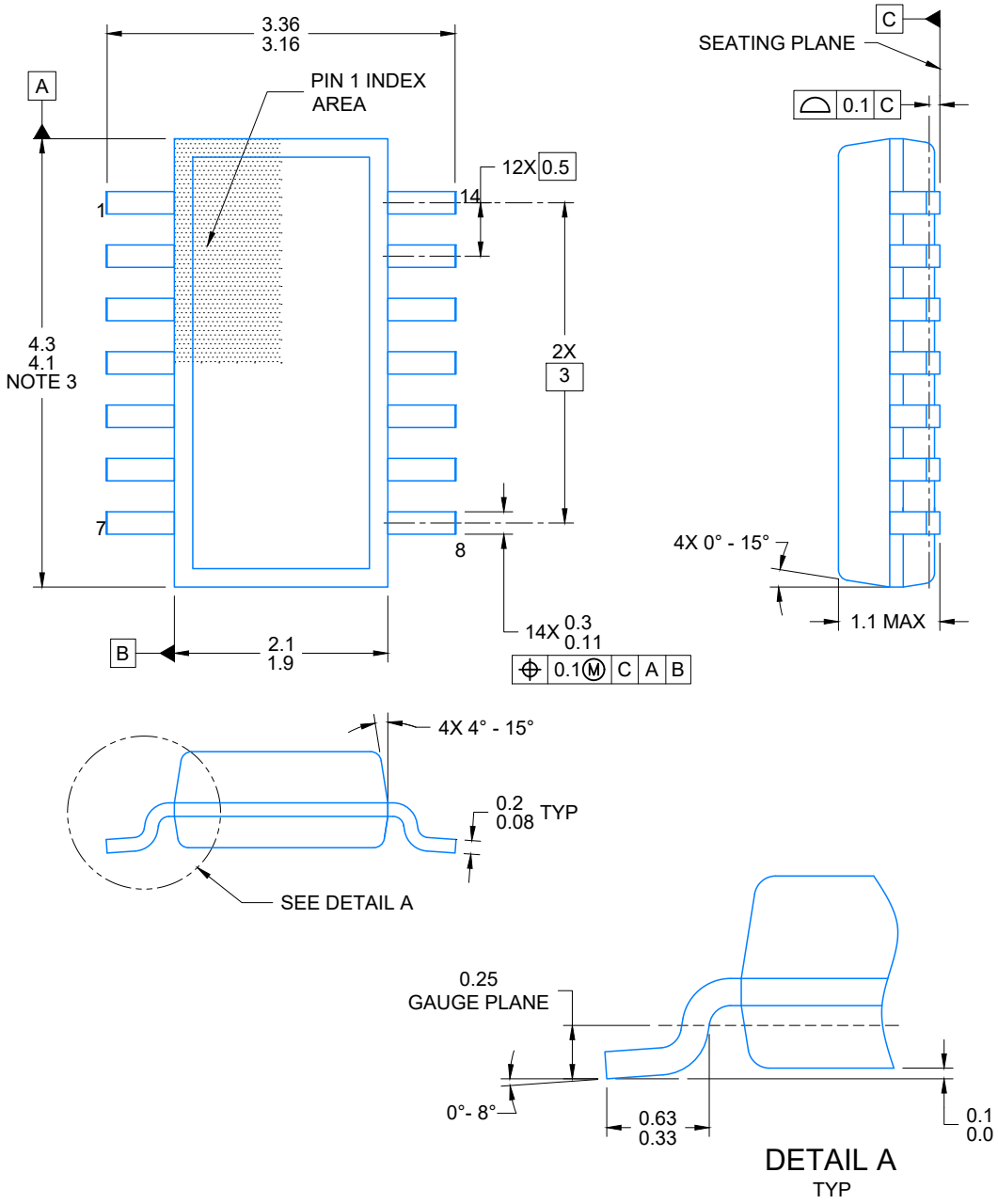
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYY0014A

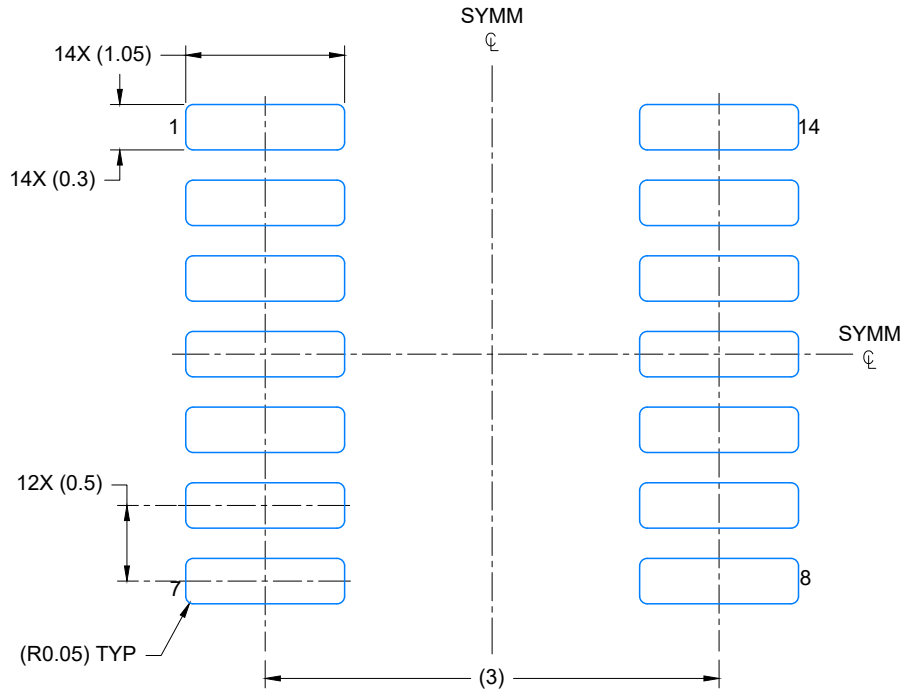
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

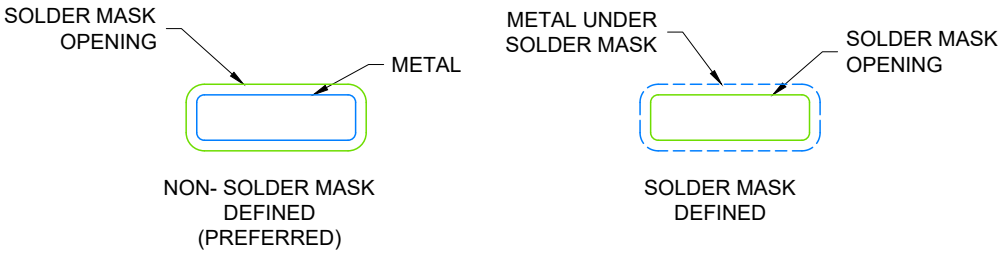


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

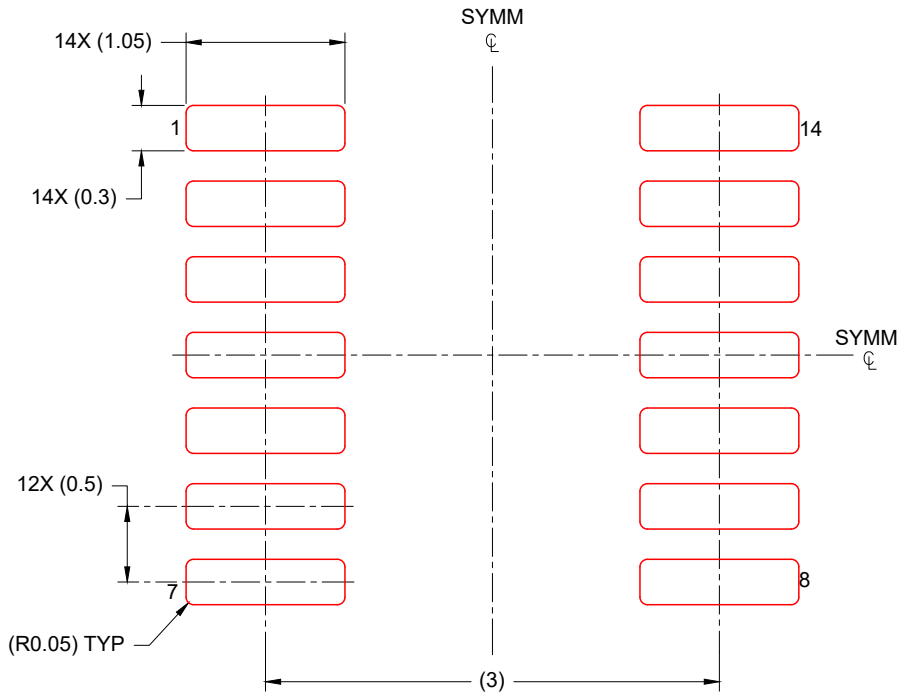


SOLDER MASK DETAILS

4224643/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月