TCAN1472-Q1 車載用、フォルト保護 CAN FD トランシーバ、信号改善機能 (SIC) およびスタンバイ モード付き

1 特長

- AEC Q100 (グレード 1): 車載アプリケーション認定済み
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 付則 A の CAN SIC 仕様を含む、ISO 11898-2:2024 規格の要件に適合
- Classical CAN および最大 8Mbps の CAN FD
  - 複雑なトポロジでのリンギング効果を低減することにより、バス信号をアクティブに改善
  - Classic CAN ネットワークでの使用に対する下位互換性
- V_{IO} レベル シフト対応: 1.7V～5.5V
- 動作モード
  - 通常モード
  - リモート ウェイクアップ要求をサポートする、低消費電力スタンバイ モード
- 電源非接続時のパッシブ動作
  - バスおよびロジック端子は高インピーダンス (動作中のバスまたはアプリケーションに無負荷)
  - ホットプラグ対応: バスおよび RXD 出力での電源オン / オフ時のグリッチ フリー動作
  - フローティング論理ピンと低電圧電源条件におけるデバイスの動作を定義
- 保護機能
  - バス ピンの IEC ESD 保護
  - CAN バスの障害耐性: ±58V
  - V_{CC} および V_{IO} (V バージョンのみ) 電源端子の低電圧保護
  - TXD ドミナント状態タイムアウト (TXD DTO)
  - サーマル シャットダウン保護 (TSD)
- SOIC (8)、小型フットプリント SOT-23 (8)、自動光学検査 (AOI) 性能を向上させたウェッタブル フランクのリードレス VSON (8) パッケージで供給

2 アプリケーション

- 車載ゲートウェイ
- 先進運転支援システム (ADAS)
- ボディ エレクトロニクスおよび照明
- ハイブリッド、電気、パワートレイン システム
- 車載インフォテインメントおよびクラスタ

3 概要

TCAN1472-Q1 デバイス は、ISO 11898-2:2024 附属書 A 信号改善機能 (SIC) 仕様の物理層要件を満たす高速 CAN (Controller Area Network) SIC トランシーバです。このデバイスは、ドミナントとリセッシブのエッジで信号リンギングを低減し、複雑なネットワーク トポロジで高いスループットを実現します。信号改善機能を活用すると、アプリケーションは複数の未終端のスタブを持つ大規模ネットワークで 2Mbps、5Mbps またはそれ以上で動作することで、CAN FD (フレキシブル データ レート) の真のメリットを引き出すことができます。

これらのデバイスは、ISO 11898-2:2024 附属書 A の SIC 仕様を満たしており、通常の CAN FD トランシーバと比較して、はるかに厳密なビット タイミング対称性を備えています。この結果、より大きなタイミング ウィンドウで正しいビットをサンプリングすることができ、リンギングとビット歪みを本質的に持つ大きく複雑なスター ネットワークでエラーフリーの通信を実現できます。

これらのデバイスは、TCAN1046A-Q1 や TCAN1042-Q1 など、8 ピンの CAN FD トランシーバとピン互換です。

「V」接尾辞付きの TCAN1472-Q1 デバイスには、V_{IO} ロジック電源ピン経由の内部ロジック レベル変換が搭載されており、1.8V、3.3V、5V のコントローラと直接接続できます。これらのトランシーバは低消費電力スタンバイ モードをサポートしており、ISO 11898-2:2024 に定義されたウェイクアップ パターン (WUP) に準拠した CAN バスによるリモート ウェイクアップが可能です。このデバイス ファミリは、低電圧検出、サーマル シャットダウン (TSD)、ドライバ ドミナント タイムアウト (TXD DTO)、±58V のバス フォルト保護などの多くの保護機能も備えています。

パッケージ情報

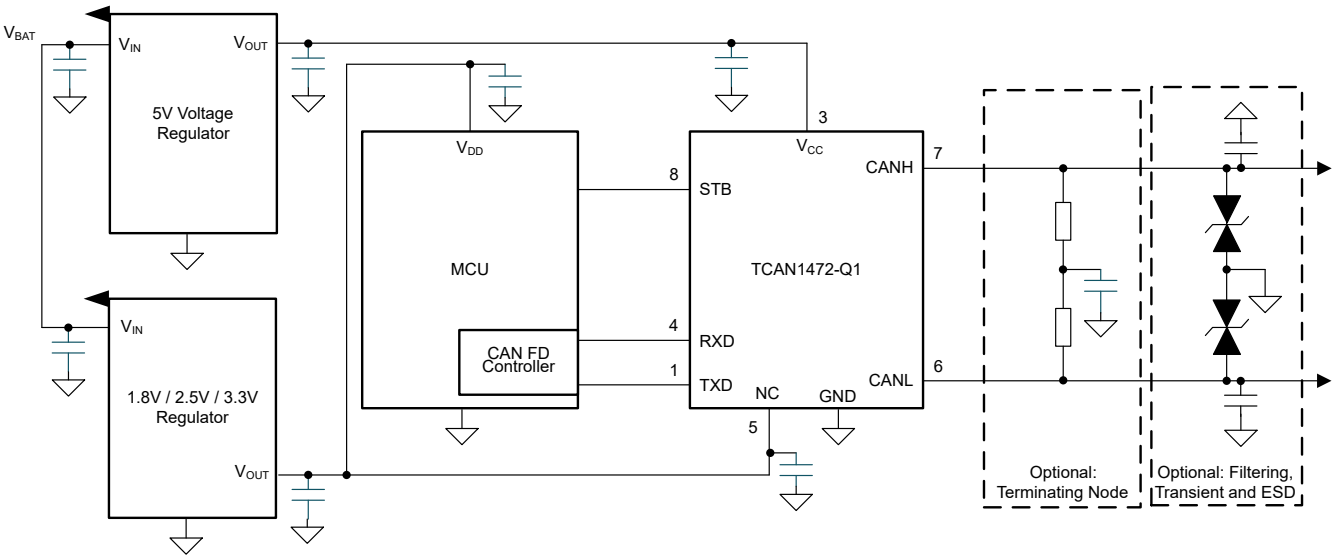
部品番号	パッケージ(1)	パッケージ サイズ(2)
TCAN1472-Q1	SOT-23 (DDF)	2.9 mm × 2.8mm
	VSON (DRB)	3 mm × 3mm
	SOIC (D)	4.9 mm × 6mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

デバイス比較表

デバイス番号	バス故障保護	ピン 5 で低電圧 I/O ロジックをサポート	ピン 8 のモード選択
TCAN1472-Q1	± 58V	なし	リモート ウェイクアップ機能付き低消費電力スタンバイ モード
TCAN1472V-Q1	± 58V	あり	



概略ブロック図

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4 Pin Configurations and Functions

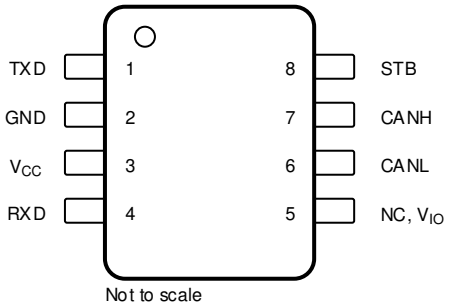


図 4-1. SOIC (D) and SOT-23 (DDF) Package, 8 Pin (Top View)

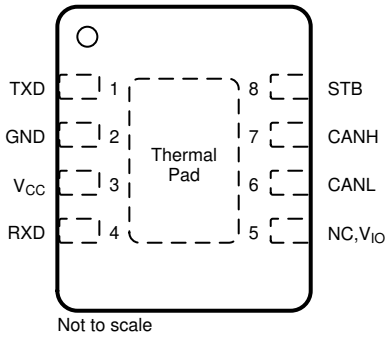


図 4-2. VSON (DRB) Package, 8 Pin (Top View)

表 4-1. Pin Functions

PINS		TYPE	DESCRIPTION
NAME	NO.		
TXD	1	Digital Input	CAN transmit data input, integrated pull-up
GND	2	GND	Ground connection
V_{CC}	3	Supply	5V supply voltage
RXD	4	Digital Output	CAN receive data output, tristate when powered off
V_{IO}	5	Supply	Logic supply voltage
NC		--	No Connect (not internally connected); Devices without V_{IO}
CANL	6	Bus IO	Low-level CAN bus input/output line
CANH	7	Bus IO	High-level CAN bus input/output line
STB	8	Digital Input	Standby mode control input, integrated pull-up
Thermal Pad (VSON only)	—		Electrically connected to GND, connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief

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5 Specifications

5.1 Absolute Maximum Ratings

(1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
V_{IO}	Supply voltage I/O level shifter (Devices with the "V" suffix)	–0.3	6	V
V_{BUS}	CAN bus I/O voltage range on CANH and CANL	–58	58	V
V_{DIFF}	Max differential voltage between CANH and CANL V_{DIFF} = (CANH - CANL)	–45	45	V
V_{Logic_Input}	Logic pin input voltage (TXD, STB)	–0.3	6	V
V_{RXD}	Logic output voltage range (RXD)	–0.3	6	V
$I_{O(RXD)}$	RXD output current	–8	8	mA
T_J	Junction temperature	–40	165	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

5.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	All pins	±4000	V
			CANH and CANL with respect to GND	±10000	V
		Charged-device model (CDM), per AEC Q100-011 for all pins		±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 ESD Ratings, IEC Transients

				VALUE	UNIT
V_{ESD}	System level electrostatic discharge	CAN bus terminals (CANH, CANL) to GND	SAE J2962-2 per ISO 10605 Powered contact discharge	±8000	V
			SAE J2962-2 per ISO 10605 Powered air discharge	±15000	V
			IEC 62228-3 per ISO 10605	±8000	V
V_{Tran}	ISO 7637-2 Transient immunity[1]		Pulse 1	–100	V
			Pulse 2a	75	V
			Pulse 3a	–150	V
			Pulse 3b	100	V
	Direct capacitor coupling, SAE J2962-2 per ISO 7637-3[2]		DCC slow transient pulse	±30	V

(1) Tested according to IEC 62228-3:2019 CAN Transceivers, Section 6.3; standard pulses parameters defined in ISO 7637-2 (2011)
(2) Tested according to SAE J2962-2

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5.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IO}	Supply voltage for I/O level shifter (Devices with V_{IO})	1.7		5.5	V
$I_{OH(RXD)}$	RXD terminal high-level output current	–1.5			mA
$I_{OL(RXD)}$	RXD terminal low-level output current			1.5	mA
T_J	Junction temperature	–40		150	°C

5.5 Thermal Characteristics

THERMAL METRIC(1)		TCAN1472(V)-Q1			UNIT
		D (SOIC)	DDF (SOT)	DRB (VSON)	
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	113.6	129.2	52.3	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	52.5	55.0	58.4	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	61.1	48.1	24.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.4	1.7	1.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	60.2	47.9	24.6	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	–	8.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Supply Characteristics

parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V (for devices with V_{IO}), Device ambient maintained at 27°C) unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current normal mode	Dominant	TXD = 0 V, STB = 0 V R_L = 60 Ω, C_L = open See 図 6-1		50	70	mA
		Dominant	TXD = 0 V, STB = 0 V R_L = 50 Ω, C_L = open See 図 6-1		55	80	mA
		Recessive	TXD = V_{IO}, STB = 0 V R_L = 50 Ω, C_L = open See 図 6-1		7	11	mA
		Dominant with bus fault	TXD = 0 V, STB = 0 V CANH = CANL = ±25 V R_L = open, C_L = open See 図 6-1			130	mA
	Supply current standby mode (devices with V_{IO})		TXD = STB = V_{IO} , R_L = 50 Ω, C_L = open, Tj <= 85 °C, See 図 6-1			1	µA
			TXD = STB = V_{IO} , R_L = 50 Ω, C_L = open, Tj <= 125 °C, See 図 6-1		0.2	2	
			TXD = STB = V_{IO} , R_L = 50 Ω, C_L = open, Tj <= 150 °C, See 図 6-1			5	
	Supply current standby mode (devices without V_{IO})		TXD = STB = V_{CC} , R_L = 50 Ω, C_L = open, Tj <= 85 °C, See 図 6-1			15	µA
			TXD = STB = V_{CC} , R_L = 50 Ω, C_L = open, Tj <= 125 °C, See 図 6-1			16	
			TXD = STB = V_{CC} , R_L = 50 Ω, C_L = open, Tj <= 150 °C, See 図 6-1			21	

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5.6 Supply Characteristics (続き)

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V (for devices with V_{IO}), Device ambient maintained at 27℃) unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IO} Devices with V_{IO}	I/O supply current normal mode	Dominant	TXD = 0 V, STB = 0 V R_L = 60 Ω, C_L = open RXD floating		125	300	µA
		Recessive	TXD = V_{IO}, STB = 0 V R_L = 60 Ω, C_L = open RXD floating		25	48	µA
	I/O supply current standby mode		TXD = V_{IO}, STB = V_{IO} R_L = 60 Ω, C_L = open RXD floating, Tj <= 85 °C			13.5	µA
			TXD = V_{IO}, STB = V_{IO} R_L = 60 Ω, C_L = open RXD floating, Tj <= 125 °C		8.5	15	
			TXD = V_{IO}, STB = V_{IO} R_L = 60 Ω, C_L = open RXD floating, Tj <= 150 °C			16	
$UV_{CC(R)}$	Undervoltage detection V_{CC} rising		Ramp up		4.2	4.4	V
$UV_{CC(F)}$	Undervoltage detection on V_{CC} falling		Ramp down	3.5	4		V
$UV_{IO(R)}$	Undervoltage detection V_{IO} rising (Devices with V_{IO})		Ramp up		1.6	1.65	V
$UV_{IO(F)}$	Undervoltage detection on V_{IO} falling (Devices with V_{IO})		Ramp down	1.4	1.5		V

5.7 Dissipation Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Average power dissipation Normal mode	V_{CC} = 5 V, V_{IO} = 3.3 V, T_J = 27°C, R_L = 60Ω, C_{L_RXD} = 15 pF TXD input = 250 kHz 50% duty cycle square wave		60		mW
		V_{CC} = 5.5 V, V_{IO} = 5.5 V, T_J = 150°C, R_L = 50Ω, C_{L_RXD} = 15 pF TXD input = 2.5 MHz 50% duty cycle square wave		120		mW
T_{TSD}	Thermal shutdown temperature			192		°C
T_{TSD_HYS}	Thermal shutdown hysteresis			10		

5.8 Electrical Characteristics

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27℃) unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Electrical Characteristics							
$V_{CANH(D)}$	Dominant output voltage normal mode	CANH	V_{CC} = 4.75 V to 5.25 V, TXD = 0 V, STB = 0 V 45 Ω ≤ R_L ≤ 65 Ω, C_L = open, See 図 6-2 and 図 7-5	3	3.5	4.26	V
$V_{CANL(D)}$		CANL		0.75	1.5	2.01	V
$V_{CANH(D)}$	Dominant output voltage normal mode	CANH	V_{CC} = 4.5 V to 5.5 V, TXD = 0 V, STB = 0 V 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, See 図 6-2 and 図 7-5	2.75	3.5	4.5	V
$V_{CANL(D)}$		CANL		0.5	1.5	2.25	V
$V_{CANH(R)}$, $V_{CANL(R)}$	Recessive output voltage normal mode	CANH and CANL	V_{CC} = 4.75 V to 5.25 V, TXD = V_{IO}, STB = 0 V 45 Ω ≤ R_L ≤ 65 Ω , C_L = open See 図 6-2 and 図 7-5	2.256		2.756	V

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5.8 Electrical Characteristics (続き)

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27℃) unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CANH(R)}$, $V_{CANL(R)}$	Recessive output voltage normal mode	CANH and CANL	V_{CC} = 4.5 V to 5.5 V, TXD = V_{IO}, STB = 0 V R_L = open (no load), C_L = open, See 図 6-2 and 図 7-5	2	2.5	3	V
V_{SYM}	Driver symmetry ($V_{O(CANH)}$ + $V_{O(CANL)}$)/($V_{CANH(R)}$ + $V_{CANL(R)}$)		V_{CC} = 4.75 V to 5.25 V, TXD = 250 kHz, 1 MHz, 2.5 MHz, STB = 0 V 45 Ω ≤ R_L ≤ 65 Ω, C_{SPLIT} = 4.7 nF, C_L = open, See 図 6-2 and 図 8-2	0.95		1.05	V/V
			V_{CC} = 4.5 V to 5.5 V, TXD = 250 kHz, 1 MHz, 2.5 MHz, STB = 0 V 45 Ω ≤ R_L ≤ 65 Ω, C_{SPLIT} = 4.7 nF, C_L = open, See 図 6-2 and 図 8-2	0.9		1.1	V/V
$V_{DIFF(D)}$	Differential output voltage normal mode Dominant	CANH - CANL	V_{CC} = 4.75 V to 5.25 V, TXD = 0 V, STB = 0 V 45 Ω ≤ R_L ≤ 65 Ω, C_L = open, See 図 6-2 and 図 7-5	1.5		3	V
			V_{CC} = 4.75 V to 5.25 V, TXD = 0 V, STB = 0 V 45 Ω ≤ R_L ≤ 70 Ω, C_L = open, See 図 6-2 and 図 7-5	1.5		3.3	V
			V_{CC} = 4.5 V to 5.5 V, TXD = 0 V, STB = 0 V 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, See 図 6-2 and 図 7-5	1.5		3	V
			V_{CC} = 4.5 V to 5.5 V, TXD = 0 V, STB = 0 V 45 Ω ≤ R_L ≤ 70 Ω, C_L = open, See 図 6-2 and 図 7-5	1.4		3.3	V
			TXD = 0 V, STB = 0 V R_L = 2240 Ω, C_L = open, See 図 6-2 and 図 7-5	1.5		5	V
$V_{DIFF(R)}$	Differential output voltage normal mode Dominant	CANH - CANL	TXD = V_{IO}, STB = 0 V 45 Ω ≤ R_L ≤ 65 Ω, C_L = open, See 図 6-2 and 図 7-5	–50		50	mV
	Differential output voltage normal mode Dominant		TXD = V_{IO}, STB = 0 V R_L = open, C_L = open, See 図 6-2 and 図 7-5	–50		50	mV
$V_{CANH(INACT)}$	Bus output voltage standby mode	CANH	TXD = STB = V_{IO} R_L = open , C_L = open, See 図 6-2 and 図 7-5	-0.1		0.1	V
$V_{CANL(INACT)}$		CANL		-0.1		0.1	V
$V_{DIFF(INACT)}$		CANH - CANL		-0.2		0.2	V
$R_{DIFF(DOM)}$	Differential input resistance in dominant phase		TXD= 0 V, STB = 0 V, See 図 7-2		40		Ω
$R_{SE_SIC_ACT_REC}$	Single ended resistance CANH/CANL in active recessive phase		V_{CC} = 4.75 V to 5.25 V, 2 V ≤ $V_{CANH/L}$ ≤ V_{CC} - 2 V	37.5	50	66.5	Ω
$R_{DIFF_ACT_REC}$	Differential input resistance in active recessive phase		V_{CC} = 4.75 V to 5.25 V,2 V ≤ $V_{CANH/L}$ ≤ V_{CC} - 2 V	75	100	133	Ω
$I_{CANH(OS)}$	Short-circuit bus output current, TXD is dominant or recessive or toggling, normal mode		$V_{(CANH)}$ = -15 V to 40 V, CANL = open, TXD = 0 V or V_{IO} or 250 kHz, 2.5 MHz square wave, See 図 6-7 and 図 7-5	–115		115	mA
$I_{CANL(OS)}$			$V_{(CAN_L)}$ = -15 V to 40 V, CANH = open, TXD = 0 V or V_{IO} or 250 kHz, 2.5 MHz square wave, See 図 6-7 and 図 7-5	–115		115	mA
Receiver Electrical Characteristics							
V_{IT}	Input threshold voltage normal mode		-12 V ≤ V_{CM} ≤ 12 V, STB= 0 V, See 図 6-3 and 図 7-6	500		900	mV

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5.8 Electrical Characteristics (続き)

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27℃) unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT(STB)}$	Input threshold standby mode	-12 V ≤ V_{CM} ≤ 12 V, STB= V_{IO} , See 図 6-3 and 図 7-6	400		1150	mV
$V_{DIFF_RX(D)}$	Normal mode dominant state differential input voltage range	-12 V ≤ V_{CM} ≤ 12 V, STB= 0 V, See 図 6-3 and 図 7-6	0.9		9	V
$V_{DIFF_RX(R)}$	Normal mode recessive state differential input voltage range	-12 V ≤ V_{CM} ≤ 12 V , STB= 0 V, See 図 6-3 and 図 7-6	-4		0.5	V
$V_{DIFF_RX(D_INACT)}$	Standby mode dominant state differential input voltage range	STB = V_{IO}, -12 V ≤ V_{CM} ≤ 12 V, See 図 6-3 and 図 7-6	1.15		9	V
$V_{DIFF_RX(R_INACT)}$	Standby mode recessive state differential input voltage range	STB = V_{IO}, -12 V ≤ V_{CM} ≤ 12 V, See 図 6-3 and 図 7-6	-4		0.4	V
V_{HYS}	Hysteresis voltage for input threshold normal mode	-12 V ≤ V_{CM} ≤ 12 V, STB= 0 V, See 図 6-3 and 図 7-6		100		mV
V_{CM}	Common mode range normal and standby modes	See 図 6-3 and 図 7-6	–12		12	V
$I_{LKG(OFF)}$	Unpowered bus input leakage current	CANH = CANL = 5 V, V_{CC} = V_{IO} = GND			5	µA
C_I	Input capacitance to ground (CANH or CANL)	TXD = V_{IO}			20	pF
C_{ID}	Differential input capacitance across bus terminals				10	pF
$R_{DIFF_PAS_REC}$	Differential input resistance in passive recessive phase	TXD = V_{IO}, STB = 0 V -12 V ≤ V_{CM} ≤ 12 V, Delta V/Delta I	40		90	kΩ
$R_{SE_PAS_REC}$	Single ended input resistance in passive recessive phase (CANH or CANL)		20		45	kΩ
m_R	Input resistance matching [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100 %	$V_{(CAN_H)}$ = $V_{(CAN_L)}$ = 5 V	–1		1	%
TXD Terminal (CAN Transmit Data Input)						
V_{IH}	High-level input voltage	Devices without V_{IO}	0.7 V_{CC}			V
V_{IH}	High-level input voltage	Devices with V_{IO}	0.7 V_{IO}			V
V_{IL}	Low-level input voltage	Devices without V_{IO}			0.3 V_{CC}	V
V_{IL}	Low-level input voltage	Devices with V_{IO}			0.3 V_{IO}	V
I_{IH}	High-level input leakage current	TXD = V_{CC} = V_{IO} = 5.5 V	–2.5	0	1	µA
I_{IL}	Low-level input leakage current	TXD = 0 V, V_{CC} = V_{IO} = 5.5 V	–200	-100	–20	µA
$I_{LKG_TXD(OFF)}$	Unpowered leakage current	TXD = 5.5 V, V_{CC} = V_{IO} = 0 V	–1	0	1	µA
C_{I_TXD}	Input capacitance			6		pF
RXD Terminal (CAN Receive Data Output)						
V_{OH}	High-level output voltage	Devices without V_{IO} I_O = –1.5 mA, See 図 6-3	0.8 V_{CC}			V
V_{OH}	High-level output voltage	I_O = –1.5 mA, Devices with V_{IO} See 図 6-3	0.8 V_{IO}			V
V_{OL}	Low-level output voltage	Devices without V_{IO} I_O = 1.5 mA, See 図 6-3			0.2 V_{CC}	V
V_{OL}	Low-level output voltage	Devices with V_{IO} I_O = 1.5 mA, Devices with V_{IO} See 図 6-3			0.2 V_{IO}	V
$I_{LKG_RXD(OFF)}$	Unpowered leakage current	RXD = 5.5 V, V_{CC} = V_{IO} = 0 V	–1	0	1	µA
STB Terminal (Standby Mode Input)						
V_{IH}	High-level input voltage	Devices without V_{IO}	0.7 V_{CC}			V
V_{IH}	High-level input voltage	Devices with V_{IO}	0.7 V_{IO}			V
V_{IL}	Low-level input voltage	Devices without V_{IO}			0.3 V_{CC}	V
V_{IL}	Low-level input voltage	Devices with V_{IO}			0.3 V_{IO}	V
I_{IH}	High-level input leakage current	V_{CC} = V_{IO} = STB = 5.5 V	–2		2	µA

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5.8 Electrical Characteristics (続き)

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27℃) unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Low-level input leakage current	V_{CC} = V_{IO} = 5.5 V, STB = 0 V	–20		–2	µA
$I_{LKG_STB(OFF)}$	Unpowered leakage current	STB = 5.5V, V_{CC}= V_{IO} = 0 V	–1	0	1	µA

5.9 Switching Characteristics

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27℃) unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	See 図 6-4 , normal mode, V_{IO} = 4.5 V to 5.5 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%)		90	145	ns
		See 図 6-4 , normal mode, V_{IO} = 3 V to 3.6 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%)		95	155	ns
		See 図 6-4 , normal mode, V_{IO} = 2.25 V to 2.75 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%)		110	170	ns
		See 図 6-4 , normal mode, V_{IO} = 1.71 V to 1.89 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%)		125	190	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive	See 図 6-4 , normal mode, V_{IO} = 4.5 V to 5.5 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%)		95	150	ns
		See 図 6-4 , normal mode, V_{IO} = 3 V to 3.6 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%)		100	160	ns
		See 図 6-4 , normal mode, V_{IO} = 2.25 V to 2.75 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%)		110	175	ns
		See 図 6-4 , normal mode, V_{IO} = 1.71 V to 1.89 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%)		125	190	ns
t_{MODE}	Mode change time, from normal to standby or from standby to normal	See 図 6-5			30	µs
t_{WK_FILTER}	Filter time for a valid wake-up pattern	See 図 7-7	0.5		0.95	µs
$t_{WK_TIMEOUT}$	Bus wake-up timeout value	See 図 7-7	0.8		6	ms
Tstartup	Time duration after V_{CC} or V_{IO} has cleared rising undervoltage threshold, and device can resume normal operation				1.5	ms
$T_{filter(STB)}$	Filter on STB pin to filter out any glitches		0.5	1	2	µs
Driver Switching Characteristics						
$t_{prop(TxD-busrec)}$	Propagation delay time, low-to-high TXD edge to driver recessive (dominant to recessive)	See 図 6-2 , STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), V_{IO} = 4.5 V to 5.5 V		35	70	ns
		See 図 6-2 STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), V_{IO} = 3 V to 3.6 V		40	70	ns
		See 図 6-2 STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), V_{IO} = 2.25 V to 2.75 V		40	75	ns
		See 図 6-2 STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), V_{IO} = 1.71 V to 1.89 V		42	80	ns

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5.9 Switching Characteristics (続き)

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27℃) unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{prop(TxD-busdom)}$	Propagation delay time, high-to-low TXD edge to driver dominant (recessive to dominant)	See 図 6-2 , STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), V_{IO} = 4.5 V to 5.5 V		35	75	ns
		See 図 6-2 STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), V_{IO} = 3 V to 3.6 V		35	75	ns
		See 図 6-2 STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), V_{IO} = 2.25 V to 2.75 V		40	80	ns
		See 図 6-2 STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), V_{IO} = 1.71 V to 1.89 V		42	80	ns
$t_{sk(p)}$	Pulse skew ($\|t_{prop(TxD-busrec)} - t_{prop(TxD-busdom)}\|$)	STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), See 図 6-2		1	10	ns
t_{BUS_R}	Differential output signal rise time	See 図 6-2 , STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%)		15	30	ns
t_{BUS_F}	Differential output signal fall time	See 図 6-2 , STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%)		15	40	ns
t_{TXD_DTO}	Dominant timeout	See 図 6-6 , 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), STB = 0 V	1.2		4.0	ms
Receiver Switching Characteristics						
$t_{prop(busrec-RXD)}$	Propagation delay time, bus recessive input to RXD high output (dominant to recessive)	See 図 6-3 , STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%), V_{IO} = 4.5 V to 5.5 V		60	85	ns
		See 図 6-3 STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%), V_{IO} = 3 V to 3.6 V		65	95	ns
		See 図 6-3 STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%), V_{IO} = 2.25 V to 2.75 V		70	105	ns
		See 図 6-3 STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%), V_{IO} = 1.71 V to 1.89 V		80	110	ns
$t_{prop(busdom-RXD)}$	Propagation delay time, bus dominant input to RXD low output (recessive to dominant)	See 図 6-3 , STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%), V_{IO} = 4.5 V to 5.5 V		50	75	ns
		See 図 6-3 STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%), V_{IO} = 3 V to 3.6 V		60	80	ns
		See 図 6-3 STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%), V_{IO} = 2.25 V to 2.75 V		65	90	ns
		See 図 6-3 STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%), V_{IO} = 1.71 V to 1.89 V		80	110	ns
t_{RXD_R}	RXD output signal rise time	See 図 6-3, STB = 0 V, $C_{L(RXD)}$ = 15 pF(≤ ±1%)		8	25	ns
t_{RXD_F}	RXD output signal fall time			7	30	ns
FD Timing Characteristics						

5.9 Switching Characteristics (続き)

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27℃) unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns	See 図 6-4, V_{CC} = 4.5 V to 5.5 V, STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω , C_L = 100 pF, $C_{L(RXD)}$ = 15 pF	490		510	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns	See 図 6-4, V_{CC} = 4.5 V to 5.5 V, STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω , C_L = 100 pF, $C_{L(RXD)}$ = 15 pF	190		210	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 125 ns	See 図 6-4, V_{CC} = 4.5 V to 5.5 V, STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω , C_L = 100 pF, $C_{L(RXD)}$ = 15 pF	115		135	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500 ns	See 図 6-4, V_{CC} = 4.75 V to 5.25 V, STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω , C_L = 100 pF, $C_{L(RXD)}$ = 15 pF	470		520	ns
		See 図 6-4, V_{CC} = 4.5 V to 5.5 V, STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω , C_L = 100 pF, $C_{L(RXD)}$ = 15 pF	470		525	ns
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200 ns	See 図 6-4, V_{CC} = 4.75 V to 5.25 V, STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω , C_L = 100 pF, $C_{L(RXD)}$ = 15 pF	170		220	ns
		See 図 6-4, V_{CC} = 4.5 V to 5.5 V, STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω , C_L = 100 pF, $C_{L(RXD)}$ = 15 pF	170		225	ns
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 125 ns	See 図 6-4, V_{CC} = 4.75 V to 5.25 V, STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω , C_L = 100 pF, $C_{L(RXD)}$ = 15 pF	95		145	ns
		See 図 6-4, V_{CC} = 4.5 V to 5.5 V, STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω , C_L = 100 pF, $C_{L(RXD)}$ = 15 pF	95		150	ns
Signal Improvement Timing Characteristics						
$t_{PAS_REC_START}$	Start time of passive recessive phase	Time duration from TXD rising 50% edge (<5ns slope) to start of passive recessive phase	420		530	ns
$t_{ACT_REC_START}$	Start time of active signal improvement phase	Time duration from TXD rising 50% edge (<5ns slope) to start of passive recessive phase			120	ns
$t_{ACT_REC_END}$	End time of active signal improvement phase		355			ns
$t_{\Delta\ Bit(Bus)}$	Transmitted bit width variation	V_{CC} = 4.75 V to 5.25 V, TXD <= 8Mbps, $t_{\Delta\ Bit(Bus)}$ = $t_{Bit(Bus)}$ - $t_{Bit(TxD)}$ STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%), See 図 6-4	–10		10	ns
		V_{CC} = 4.5 V to 5.5 V, TXD <= 8Mbps, $t_{\Delta\ Bit(Bus)}$ = $t_{Bit(Bus)}$ - $t_{Bit(TxD)}$ STB = 0 V, R_L = 60 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%), See 図 6-4	–10		10	ns

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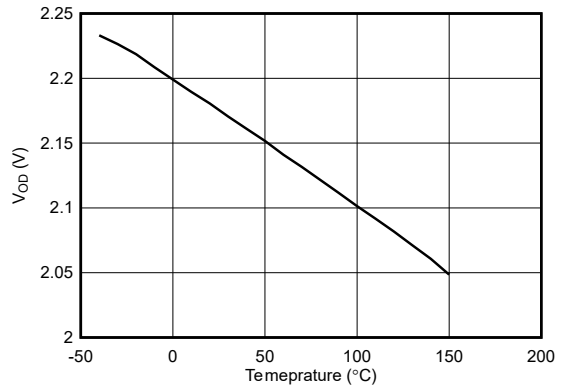
5.9 Switching Characteristics (続き)

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27℃) unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\Delta\ BIT(RxD)}$	Received bit width variation	V_{CC} = 4.75 V to 5.25 V, TXD <= 8Mbps, $t_{\Delta\ BIT(RxD)}$ = $t_{Bit(RxD)}$ - $t_{Bit(TxD)}$ STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF, See 図 6-4	–30		20	ns
		V_{CC} = 4.5 V to 5.5 V, TXD <= 8Mbps, $t_{\Delta\ BIT(RxD)}$ = $t_{Bit(RxD)}$ - $t_{Bit(TxD)}$ STB = 0 V, R_L = 60 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF, See 図 6-4	–30		20	ns
$t_{\Delta\ REC}$	Receiver timing symmetry	V_{CC} = 4.75 V to 5.25 V, TXD <= 8Mbps, $t_{\Delta\ REC}$ = $t_{Bit(RxD)}$ - $t_{Bit(Bus)}$ STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%), See 図 6-4	–20		15	ns
		V_{CC} = 4.5 V to 5.5 V, TXD <= 8Mbps, $t_{\Delta\ REC}$ = $t_{Bit(RxD)}$ - $t_{Bit(Bus)}$ STB = 0 V, R_L = 60 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%), See 図 6-4	–20		15	ns

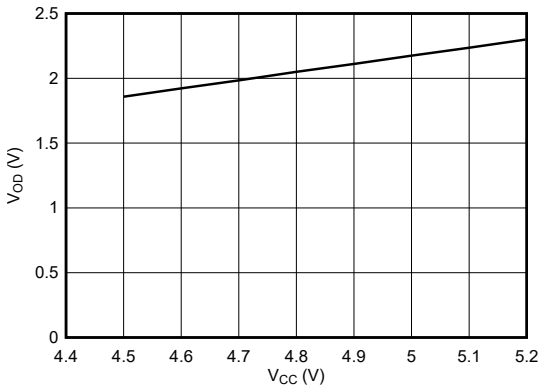
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5.10 Typical Characteristics



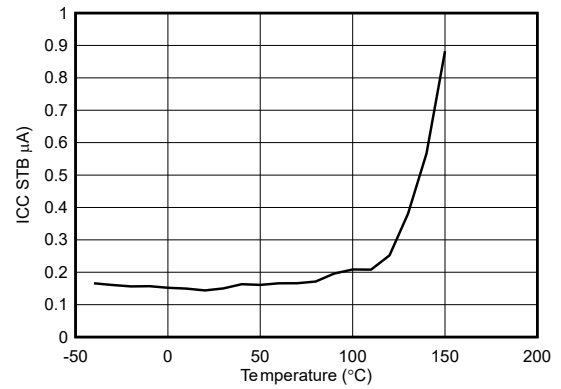
STB = GND Temp = Sweep R_L = 60Ω

図 5-1. $V_{OD(DOM)}$ Over temperature



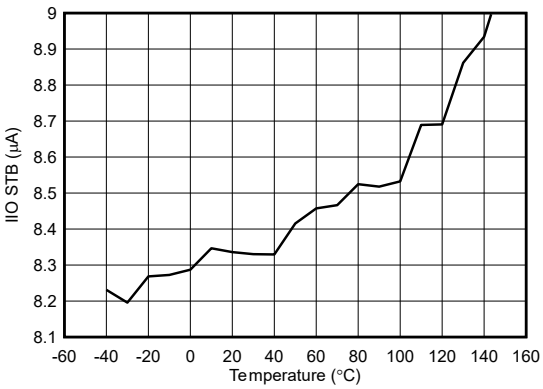
T_A = 25°C R_L = 60Ω STB = GND

図 5-2. $V_{OD(DOM)}$ over V_{CC}



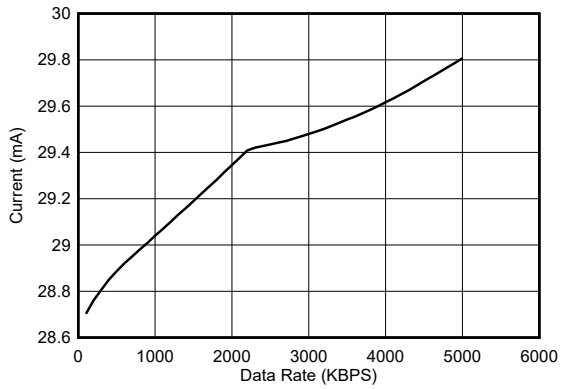
STB = GND Temp = Sweep R_L = OPEN

図 5-3. $I_{CC(standby)}$ vs Temperature



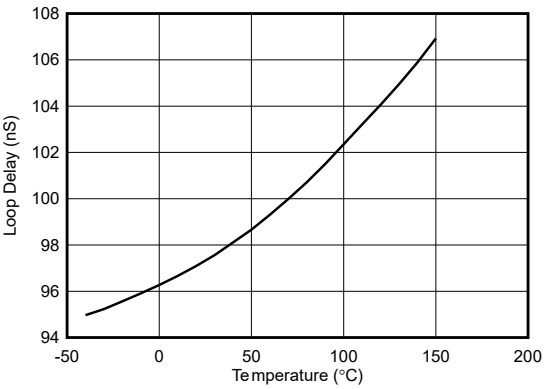
STB = GND Temp = Sweep R_L = 50Ω

図 5-4. $I_{IO(standby)}$ vs Temperature



TXD = toggling T_A = 25°C R_L = 60Ω

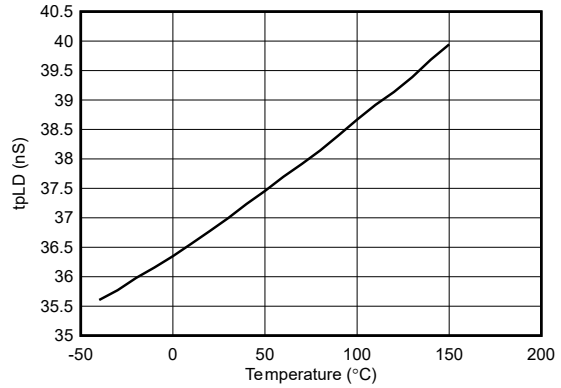
図 5-5. I_{CC} vs Data Rate



V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

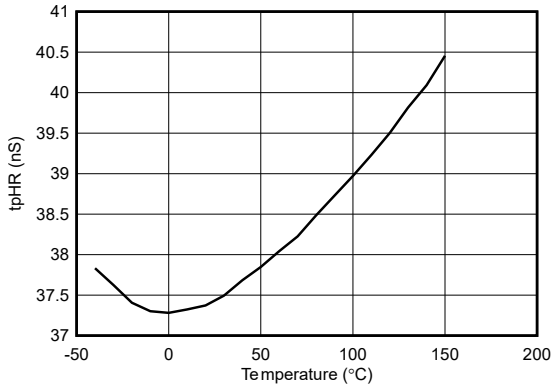
図 5-6. Loop delay vs Temperature

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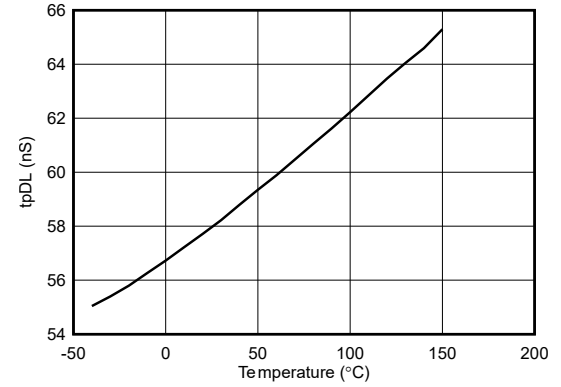
V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

図 5-7. Driver propagation delay - High to Low



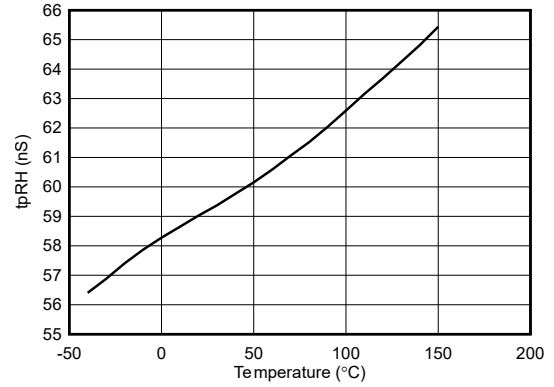
V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

図 5-8. Driver propagation delay - Low to High



V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

図 5-9. Receiver propagation delay - Bus dominant to RXD low



V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

図 5-10. Receiver propagation delay - Bus recessive to RXD high

6 Parameter Measurement Information

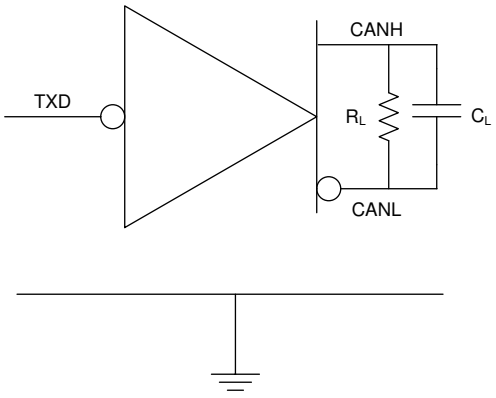


図 6-1. I_{CC} Test Circuit

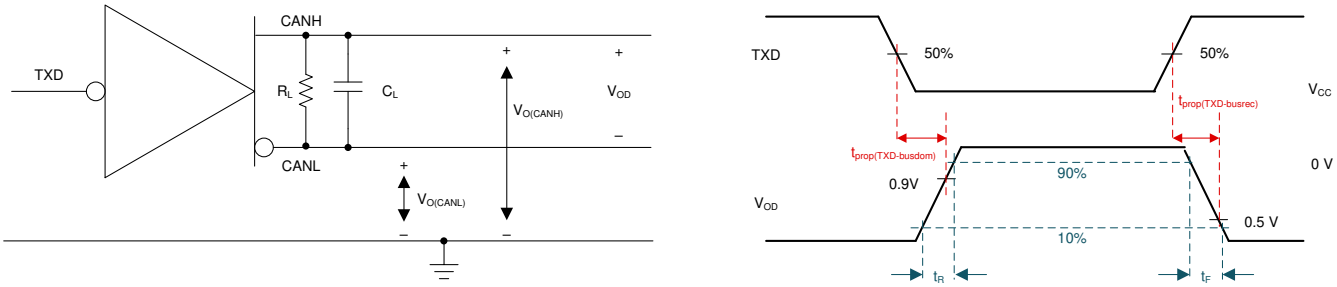


図 6-2. Driver Test Circuit and Measurement

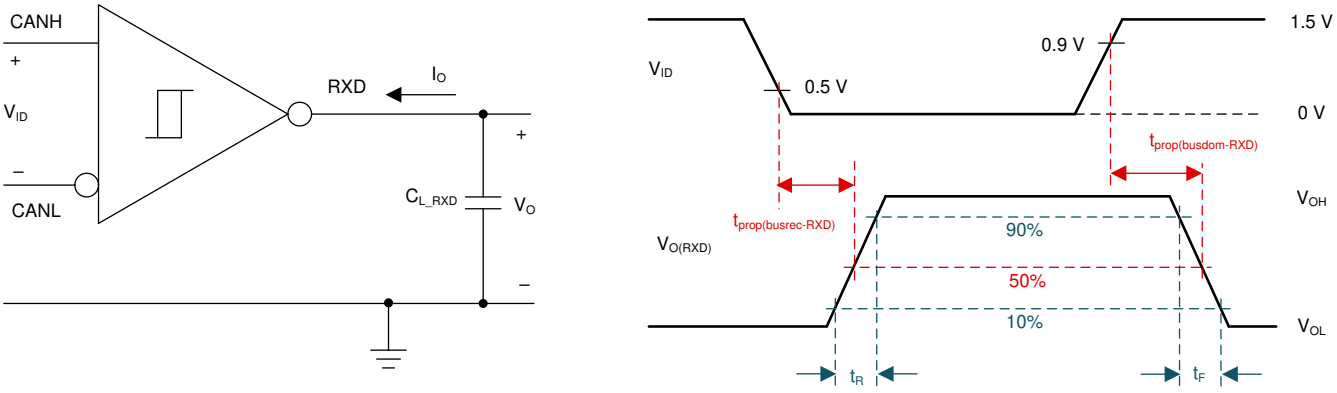
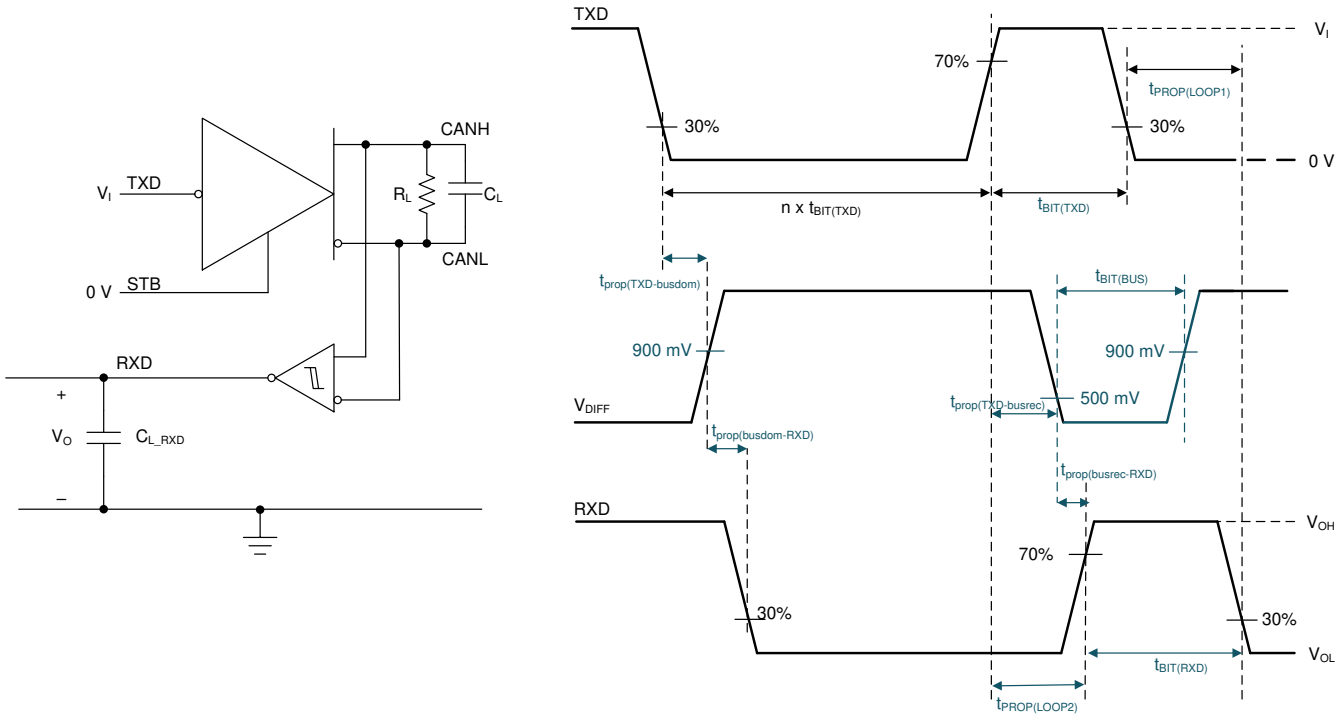


図 6-3. Receiver Test Circuit and Measurement

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n = 1 to 5;
TXD rise/fall time < 10 ns

図 6-4. Transmitter and Receiver Timing Behavior Test Circuit and Measurement

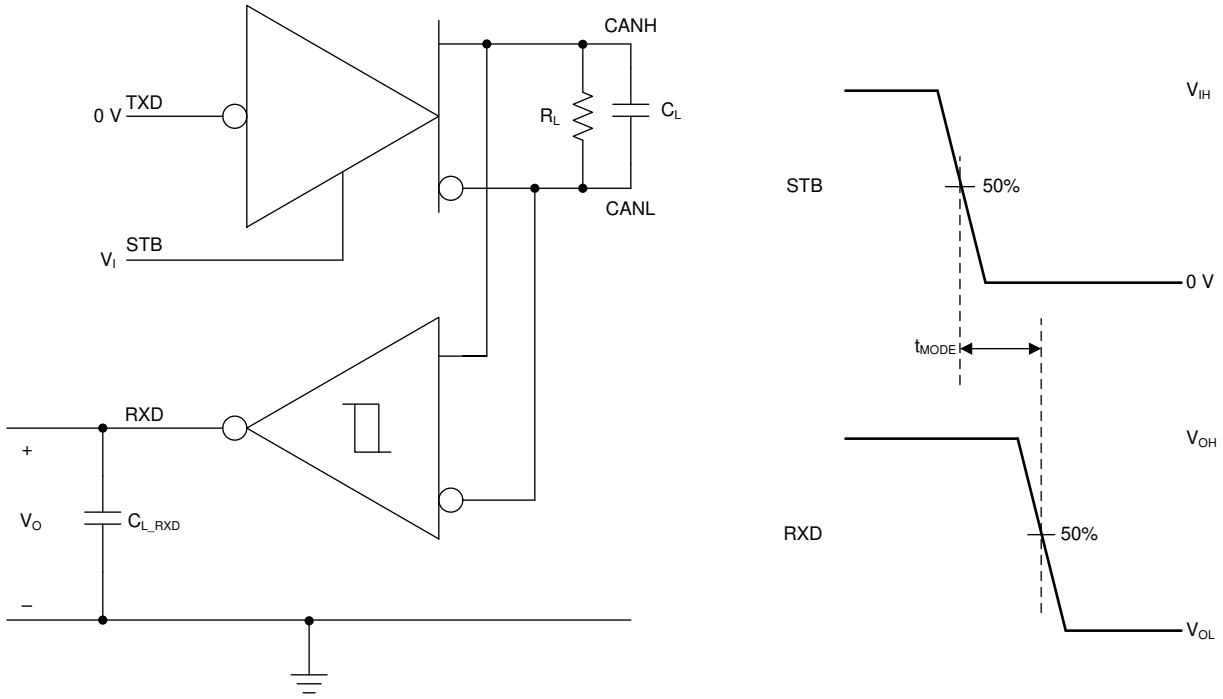


図 6-5. t_{MODE} Test Circuit and Measurement

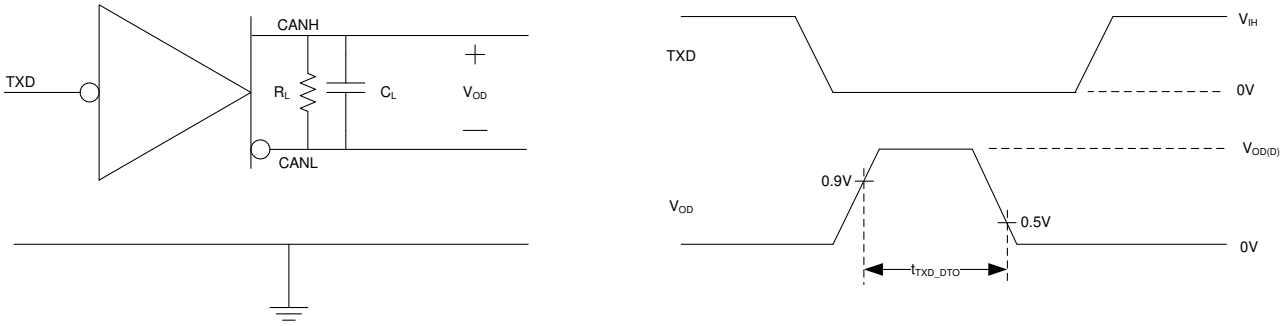


図 6-6. TXD Dominant Timeout Test Circuit and Measurement

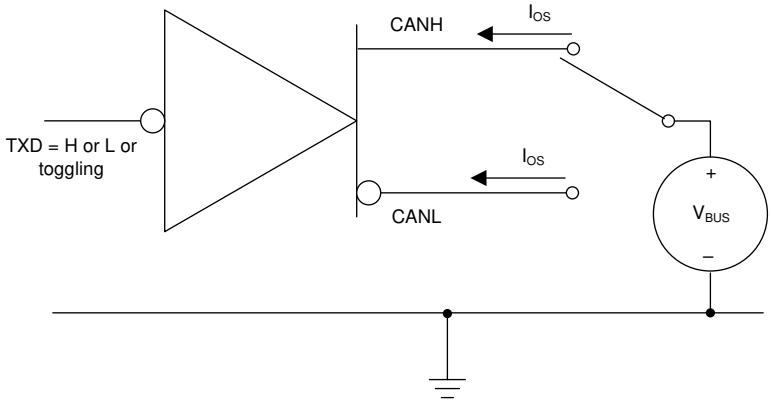


図 6-7. Driver Short-Circuit Current Test and Measurement

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7 Detailed Description

7.1 Overview

The TCAN1472-Q1 devices meet or exceed the specifications of the Annex A Signal Improvement capability (SIC) specification of ISO 11898-2:2024 Controller Area Network physical layer standard. The devices are data rate agnostic making them backward compatible for supporting classical CAN applications while also supporting CAN FD networks up to 8Mbps. These devices have standby mode support which puts the transceiver in ultra-low current consumption mode. Upon receiving a valid wake-up pattern (WUP) on the CAN bus, the device signals to the microcontroller through the RXD pin. The MCU can then put the device into normal mode using the STB pin.

The TCAN1472V-Q1 has two separate supply rails, V_{CC} bus-side supply and V_{IO} logic supply for logic-level translation for interfacing directly to 1.8V, 2.5V, 3.3V, or 5V controllers.

7.1.1 Signal Improvement

Signal improvement is an additional capability added to CAN FD transceiver that enhances the maximum data rate achievable in complex star topologies by minimizing signal ringing. Signal ringing is the result of reflections caused by impedance mismatch at various points in a CAN network due to the nodes that act as stubs.

An example of a complex network is shown in 図 7-1.

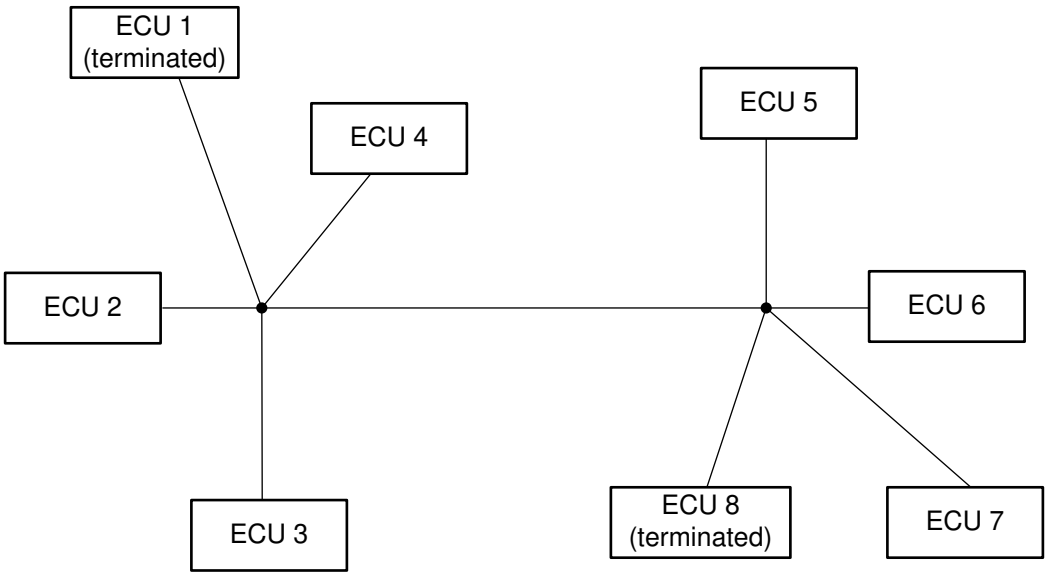


図 7-1. CAN Network: Star topology

Recessive-to-dominant signal edge is usually clean and driven by the transmitter. For a regular CAN FD transceiver, dominant-to-recessive edge is when the driver output impedance goes to approximately 60kΩ and signal reflected back experiences impedance mismatch which causes ringing. TCAN1472-Q1 resolves this issue by TX-based Signal improvement capability (SIC). The device continues to drive the bus recessive until $t_{SIC_TX_base}$, so the reflections die down and the recessive bit is clean at sampling point. In the active recessive phase, transmitter output impedance is low (approximately 100Ω). After this phase is over and device goes to passive recessive phase, driver output impedance goes to high-Z. This phenomenon is explained with 図 7-2.

For more information on the TI signal improvement technology and the compares with similar devices in market, please refer to the white paper *How Signal Improvement Capability Unlocks the Real Potential of CAN-FD Transceivers*.

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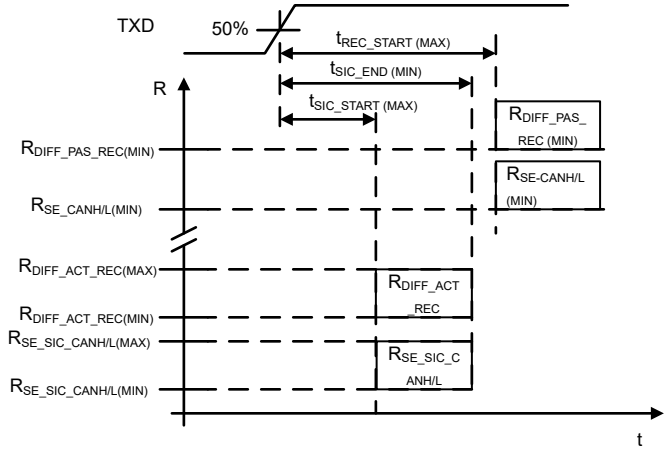


図 7-2. TX based SIC

7.2 Functional Block Diagram

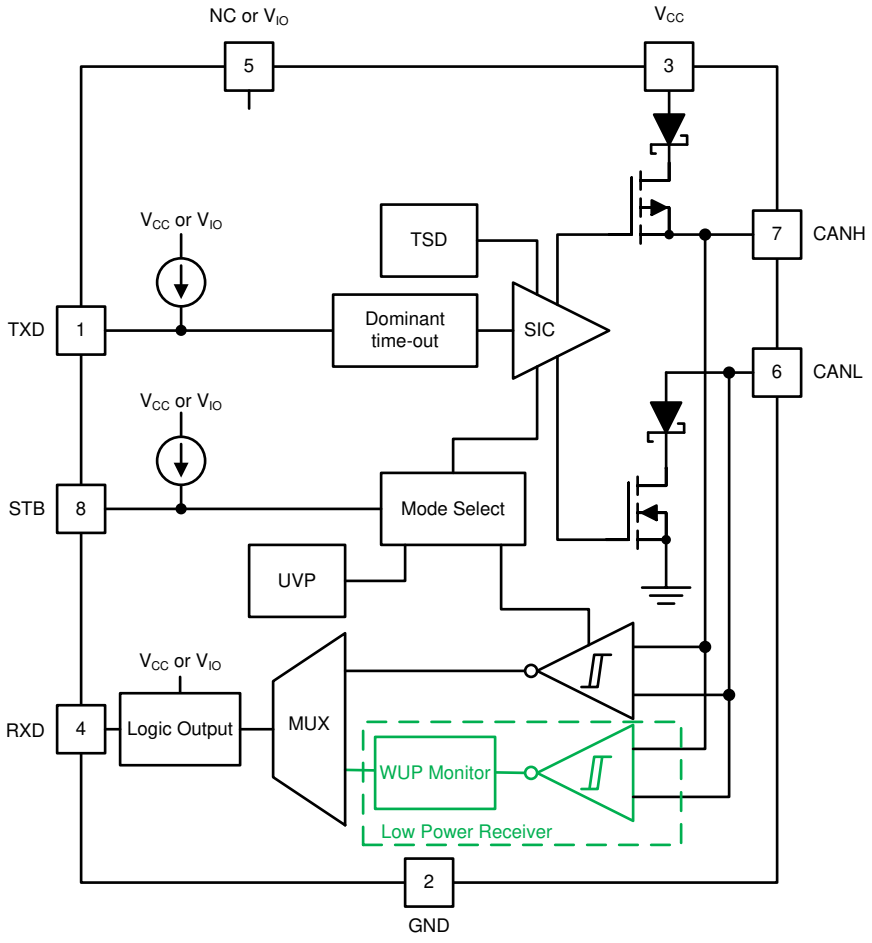


図 7-3. Block Diagram

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7.3 Feature Description

7.3.1 Pin Description

7.3.1.1 TXD

The TXD input is a logic-level signal from a CAN controller to the transceiver. The input is referenced to V_{CC} for TCAN1472-Q1, or to V_{IO} for TCAN1472V-Q1.

7.3.1.2 GND

GND is the ground pin of the transceiver. The pin must be connected to the PCB ground.

7.3.1.3 V_{CC}

V_{CC} provides the 5V power supply to the CAN transceiver.

7.3.1.4 RXD

The RXD output is a logic-level signal from the CAN transceiver to the CAN controller. The output is referenced to V_{CC} for TCAN1472-Q1 and V_{IO} for TCAN1472V-Q1. For TCAN1472V-Q1, RXD is only driven once V_{IO} is present.

When a wake event takes place, RXD is driven low.

7.3.1.5 V_{IO} (TCAN1472V-Q1 only)

The V_{IO} pin provides the digital I/O voltage to match the CAN controller voltage; thus, avoiding the requirement for a level shifter. The pin supports a wide range of controller interface voltage levels from 1.7V to 5.5V.

7.3.1.6 CANH and CANL

These are the CAN high and CAN low differential bus pins. The pins are connected to the CAN transceiver and the low-voltage WUP CAN receiver.

7.3.1.7 STB (Standby)

The STB pin is an input pin used for mode control of the transceiver. The STB pin can be supplied from either the system processor or from a static system voltage source. If normal mode is the only intended mode of operation, then the STB pin can be tied directly to GND.

7.3.2 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See 図 7-4 and 図 7-5.

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to V_{CC}/2 via the high-resistance internal input resistors (R_{IN}) of the receiver and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.

The TCAN1472-Q1 transceiver implements a low-power standby (STB) mode which enables a third bus state where the bus pins are weakly biased to ground via the high resistance internal resistors of the receiver. See 図 7-4 and 図 7-5.

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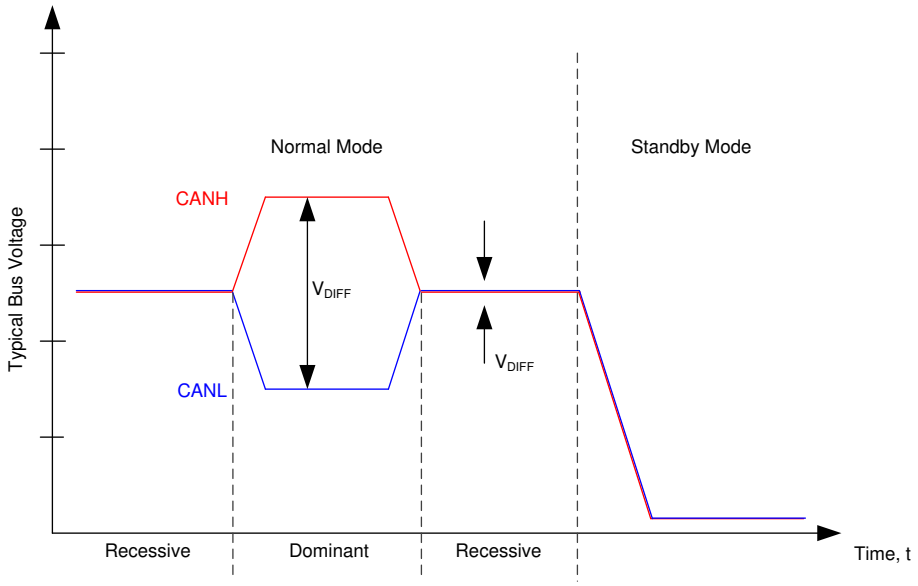
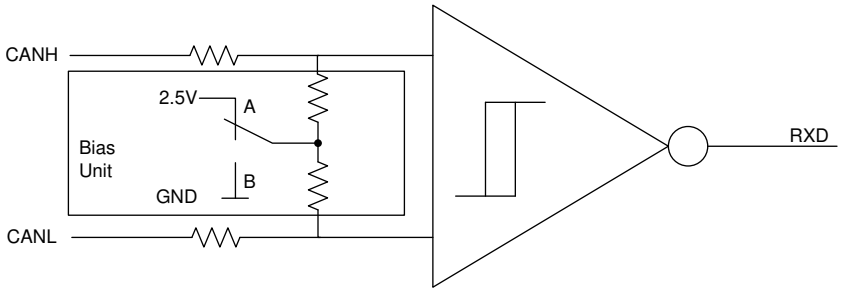


図 7-4. Bus States



A. Normal Mode
B. Standby Mode

図 7-5. Simplified Recessive Common Mode Bias Unit and Receiver

7.3.3 TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit, t_{TXD_DTO}, the CAN driver is disabled. Freeing the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin; thus, clearing the dominant time out. The receiver remains active and biased to V_{CC}/2 and the RXD output reflects the activity on the CAN bus during the TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using 式 1.

$$\text{Minimum Data Rate} = 11 \text{ bits} / t_{TXD_DTO} = 11 \text{ bits} / 1.2\text{ms} = 9.2\text{kbps} \quad (1)$$

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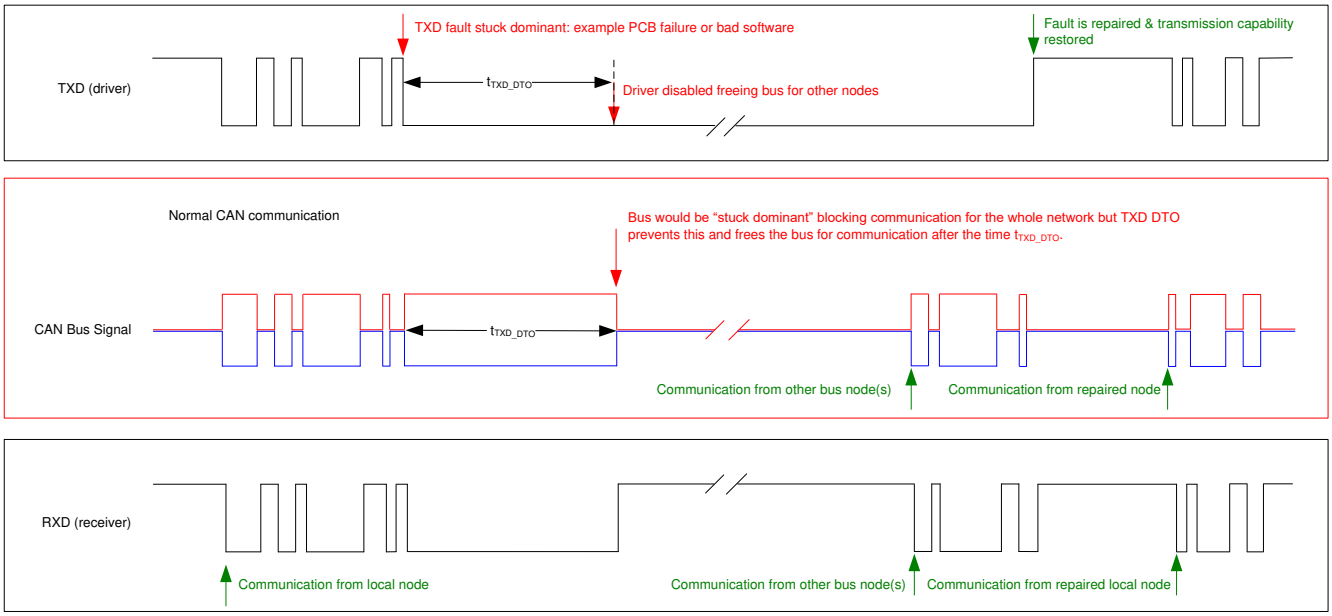


図 7-6. Example Timing Diagram for TXD Dominant Timeout

7.3.4 CAN Bus Short-circuit Current Limiting

The TCAN1472-Q1 has several protection features that limit the short-circuit current when a CAN bus line is shorted. These include CAN driver current limiting in the dominant and recessive states and TXD dominant state timeout which prevents permanently having the higher short-circuit current of a dominant state in case of a system fault. During CAN communication the bus switches between the dominant and recessive states; thus, the short-circuit current may be viewed as either the current during each bus state or as a DC average current. When selecting termination resistors or a common mode choke for the CAN design the average power rating, $I_{OS(AVG)}$, should be used. The percentage dominant is limited by the TXD DTO and the CAN protocol which has forced state changes and recessive bits due to bit stuffing, control fields, and inter frame space. These make sure there is a minimum amount of recessive time on the bus even if the data field contains a high percentage of dominant bits.

The average short-circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short-circuit currents. The average short-circuit current may be calculated using 式 2.

$$I_{OS(AVG)} = \%\ \text{Transmit} \times [(\%\ \text{REC_Bits} \times I_{OS(SS)_REC}) + (\%\ \text{DOM_Bits} \times I_{OS(SS)_DOM})] + [\%\ \text{Receive} \times I_{OS(SS)_REC}] \quad (2)$$

Where:

- $I_{OS(AVG)}$ is the average short-circuit current
- % Transmit is the percentage the node is transmitting CAN messages
- % Receive is the percentage the node is receiving CAN messages
- % REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- % DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)_REC}$ is the recessive steady state short-circuit current
- $I_{OS(SS)_DOM}$ is the dominant steady state short-circuit current

This short-circuit current and the possible fault cases of the network are taken into consideration when sizing the power supply used to generate the transceivers V_{CC} supply.

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7.3.5 Thermal Shutdown (TSD)

If the junction temperature of the TCAN1472-Q1 exceeds the thermal shutdown threshold, T_{TSD}, the device turns off the CAN driver circuitry and blocks the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below T_{TSD}. The CAN bus pins are biased to V_{CC}/2 during a TSD fault and the receiver to RXD path remains operational. The TCAN1472-Q1 TSD circuit includes hysteresis which prevents the CAN driver output from oscillating during a TSD fault.

7.3.6 Undervoltage Lockout

The supply pins, V_{CC} and V_{IO}, have undervoltage detection that places the device into a protected state. This protects the bus during an undervoltage event on either supply pin.

表 7-1. Undervoltage Lockout, TCAN1472-Q1

V_{CC}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	Protected	High impedance	High impedance

表 7-2. Undervoltage Lockout, TCAN1472V-Q1

V_{CC}	V_{IO}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	> UV_{VIO}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	> UV_{VIO}	STB = V_{IO}: standby mode	High impedance	V_{IO}: Remote wake request(1)
		STB = GND: Protected		Recessive
> UV_{VCC}	< UV_{VIO}	Protected		High impedance
< UV_{VCC}	< UV_{VIO}	Protected		High impedance

(1) See Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

Once the undervoltage condition is cleared and t_{MODE} has expired, the TCAN1472-Q1 transitions to normal mode and the host controller can send and receive CAN traffic again.

7.3.7 Unpowered Device

The TCAN1472-Q1 is designed to be a passive or no load to the CAN bus if the device is unpowered. The bus pins were designed to have low leakage currents when the device is unpowered to not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational.

The logic pins also have low leakage currents when the device is unpowered to not load other circuits which may remain powered.

7.3.8 Floating pins

The TCAN1472-Q1 has internal pull-ups on critical pins which place the device into known states if the pin floats. This internal bias should not be relied upon by design though, especially in noisy environments, but instead should be considered a failsafe protection feature.

When a CAN controller supporting open-drain outputs is used, an adequate external pull-up resistor must be chosen. Making sures the TXD output of the CAN controller maintains acceptable bit time to the input of the CAN transceiver. See 表 7-3 for details on pin bias conditions.

表 7-3. Pin Bias

Pin	Pull-up or Pull-down	Comment
TXD	Pull-up	Weakly biases TXD towards recessive to prevent bus blockage or TXD DTO triggering
STB	Pull-up	Weakly biases STB towards low-power standby mode to prevent excessive system power

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7.4 Device Functional Modes

7.4.1 Operating Modes

The TCAN1472-Q1 has two main operating modes; normal mode and standby mode. Operating mode selection is made by applying a high or low level to the STB pin on the TCAN1472-Q1.

表 7-4. Operating Modes

STB	Device Mode	Driver	Receiver	RXD Pin
High	Low current standby mode with bus wake-up	Disabled	Low-power receiver and bus monitor enable	High (recessive) until valid WUP is received. See (1)
Low	Normal Mode	Enabled	Enabled	Mirrors bus state

(1) See Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

7.4.2 Normal Mode

This is the normal operating mode of the TCAN1472-Q1. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on the TXD input to a differential output on the CANH and CANL bus pins. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD output.

7.4.3 Standby Mode

This is the low-power mode of the TCAN1472-Q1. The CAN driver and main receiver are switched off and bi-directional CAN communication is not possible. The low-power receiver and bus monitor circuits are enabled to allow for RXD wake-up requests via the CAN bus. A wake-up request is output to RXD as shown in 図 7-7. The local CAN protocol controller should monitor RXD for transitions (high-to-low) and reactivate the device to normal mode by pulling the STB pin low. The CAN bus pins are weakly pulled to GND in this mode (see 図 7-4 and 図 7-5).

In standby mode, only the V_{IO} supply is required therefore the V_{CC} may be switched off for additional system level current savings.

7.4.3.1 Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

The TCAN1472-Q1 supports a remote wake-up request that is used to indicate to the host controller that the bus is active and the node should return to normal operation.

The device uses the multiple filtered dominant wake-up pattern (WUP) from the ISO 11898-2:2024 standard to qualify bus activity. Once a valid WUP has been received, the wake request is indicated to the controller by a falling edge and low period corresponding to a filtered dominant on the RXD output of the TCAN1472-Q1.

The Wake-Up Pattern (WUP) comprises four pulses: a filtered dominant, followed by a filtered recessive, then another filtered dominant, and finally another filtered recessive. After the first filtered dominant pulse, the bus monitor waits for a filtered recessive without being reset by other bus traffic and does the same until second filtered recessive pulse. Upon receiving the second filtered recessive pulse, WUP is recognized. RXD is set permanently low upon subsequent dominant pulses.

For a dominant or recessive to be considered filtered, the bus must be in that state for more than the t_{WK_FILTER} time. Due to variability in t_{WK_FILTER} the following scenarios are applicable. Bus state times less than $t_{WK_FILTER(MIN)}$ are never detected as part of a WUP, and therefore, no wake request is generated. Bus state times between $t_{WK_FILTER(MIN)}$ and $t_{WK_FILTER(MAX)}$ may be detected as part of a WUP and a wake-up request may be generated. Bus state times greater than $t_{WK_FILTER(MAX)}$ are always detected as part of a WUP, and thus a wake request is always generated. See 図 7-7 for the timing diagram of the wake-up pattern.

The pattern and t_{WK_FILTER} time used for the WUP prevents noise and bus stuck dominant faults from causing false wake-up requests while allowing any valid message to initiate a wake-up request.

The ISO 11898-2:2024 standard has defined wakeup filter time to enable 1Mbps arbitration.

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For an additional layer of robustness and to prevent false wake-ups, the device implements a wake-up timeout feature. For a remote wake-up event to successfully occur, the entire WUP must be received within the timeout value t ≤ $t_{WK_TIMEOUT}$. If not, the internal logic is reset and the transceiver remains in the current state without waking up. The full pattern must then be transmitted again, conforming to the constraints mentioned in this section. See 図 7-7 for the timing diagram of the wake-up pattern with wake timeout feature.

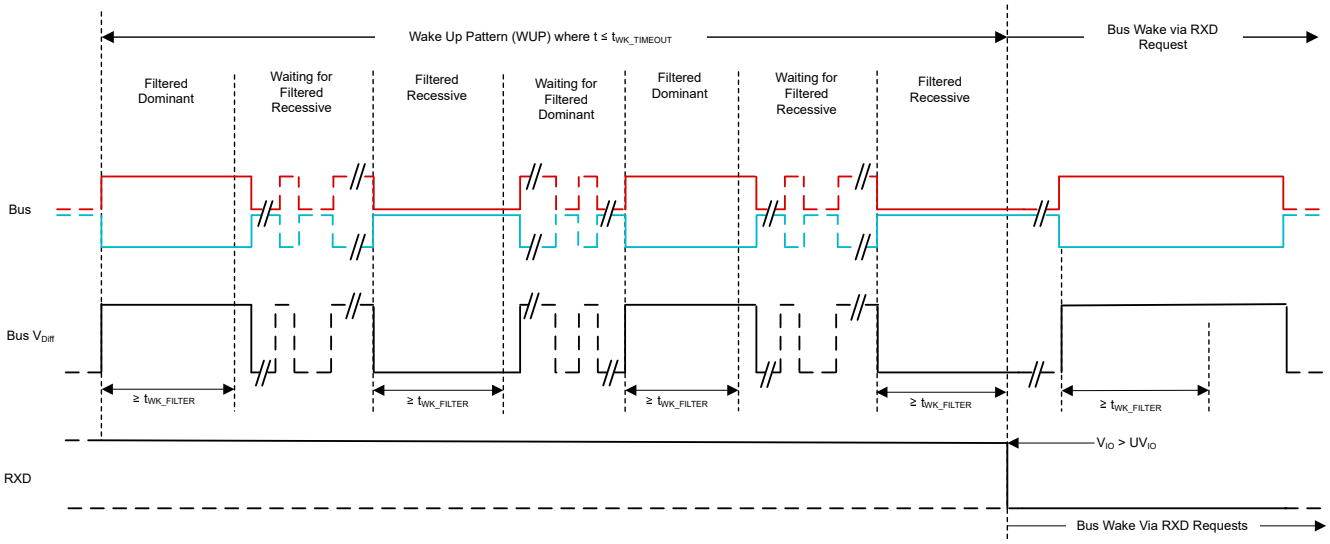


図 7-7. Wake-Up Pattern (WUP) with $t_{WK_TIMEOUT}$

7.4.4 Driver and Receiver Function

The digital logic input and output levels for the TCAN1472-Q1 are CMOS levels with respect to V_{CC}. For TCAN1472V-Q1, these are referred to V_{IO} for compatibility with MCUs having 1.8V, 2.5V, 3.3V, or 5V supply.

表 7-5. Driver Function Table

Device Mode	TXD Input(1)	Bus Outputs		Driven Bus State(2)
		CANH	CANL	
Normal	Low	High	Low	Dominant
	High or open	High impedance	High impedance	Biased recessive
Standby	X	High impedance	High impedance	Biased to ground

(1) X = irrelevant
(2) For bus state and bias see 図 7-4 and 図 7-5.

表 7-6. Receiver Function Table Normal and Standby Mode

Device Mode	CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus State	RXD Pin
Normal	V_{ID} ≥ 0.9V	Dominant	Low
	0.5V < V_{ID} < 0.9V	Undefined	Undefined
	V_{ID} ≤ 0.5V	Recessive	High
Standby	V_{ID} ≥ 1.15V	Dominant	High Low if a remote wake event occurred. See 図 7-7
	0.4V < V_{ID} < 1.15V	Undefined	
	V_{ID} ≤ 0.4V	Recessive	
Any	Open (V_{ID} ≈ 0V)	Open	High

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TCAN1472-Q1 transceiver can be used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. 図 8-1 shows a typical configuration for 5V controller applications. The bus termination is shown for illustrative purposes.

8.2 Typical Application

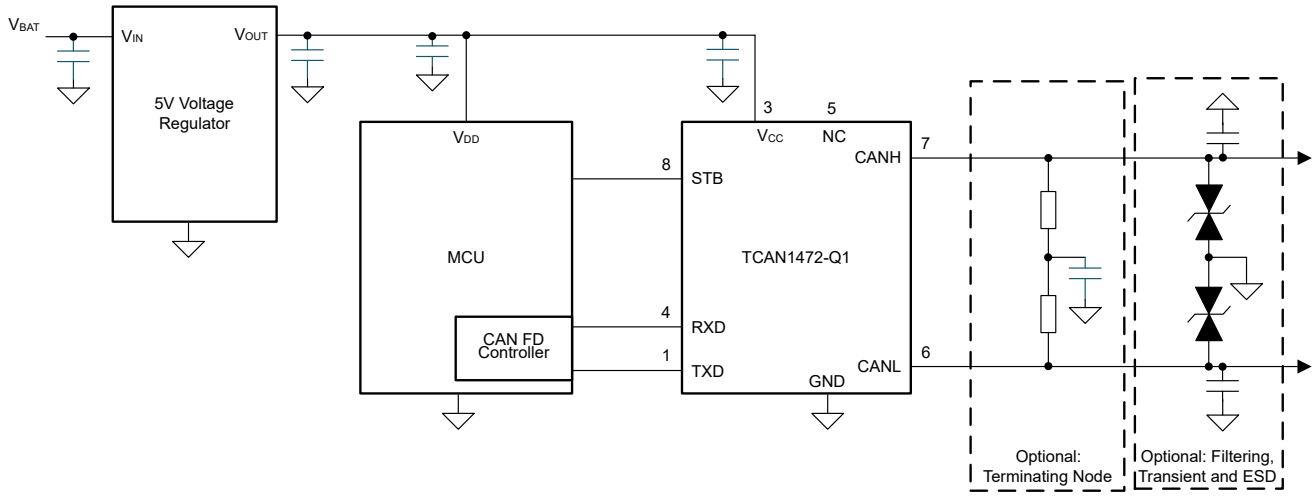


図 8-1. Transceiver Application Using 5V I/O Connections

8.2.1 Design Requirements

8.2.1.1 CAN Termination

Termination may be a single 120Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired then split termination may be used, see 図 8-2. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

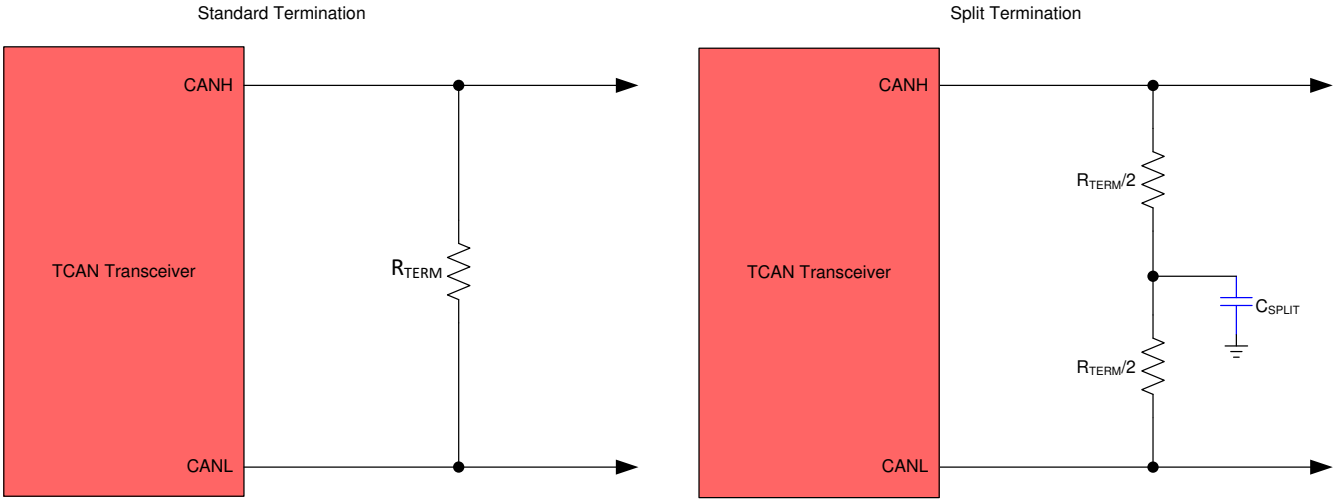


図 8-2. CAN Bus Termination Concepts

8.2.2 Detailed Design Procedures

8.2.2.1 Bus Loading, Length and Number of Nodes

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN1472-Q1. Additionally, since TCAN1472-Q1 has SIC, in a given network size, higher data rate can be achieved because signal ringing is attenuated.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. There are system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2024 specification, the driver differential output is specified with a bus load that can range from 45Ω to 65Ω where the differential output must be greater than 1.5V. The TCAN1472-Q1 family is specified to meet the 1.5V requirement down to 45Ω bus load. The differential input resistance of the TCAN1472-Q1 is a minimum of 40kΩ. If 100 TCAN1472-Q1 transceivers are in parallel on a bus, this is equivalent to a 400Ω differential load in parallel with the nominal 60Ω bus termination which gives a total bus load of approximately 52Ω. Therefore, the TCAN1472-Q1 family theoretically supports over 100 transceivers on a single bus segment. However, for a CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility

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the CAN network system, the designer must take the responsibility of good network design for a robust network operation.

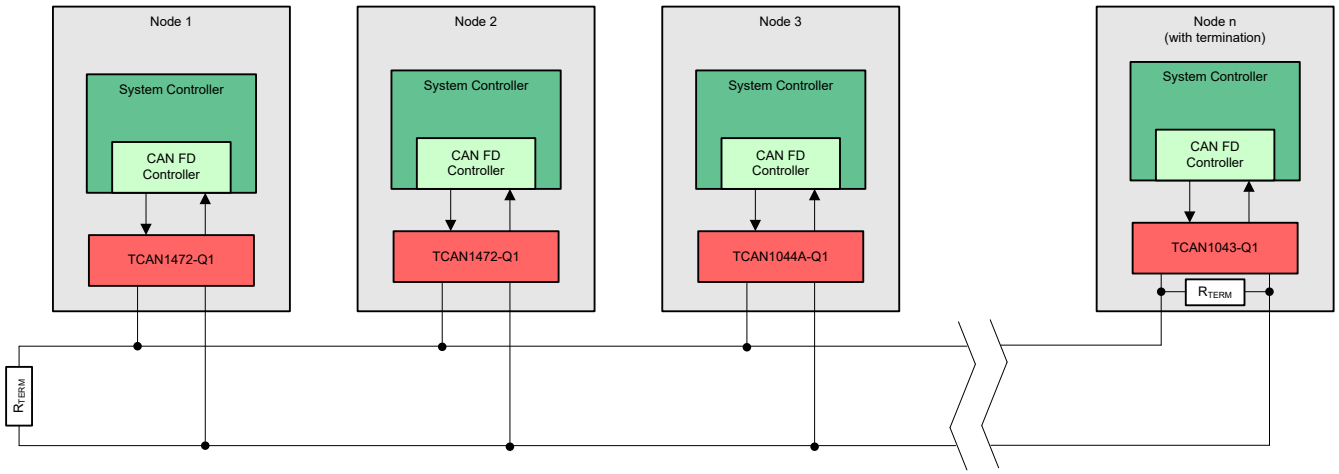
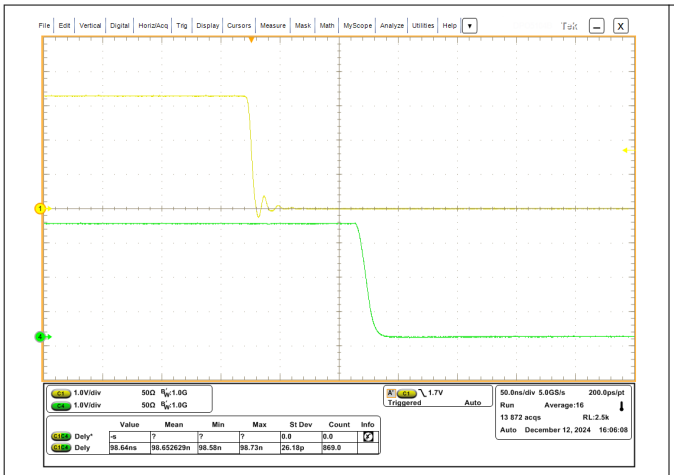


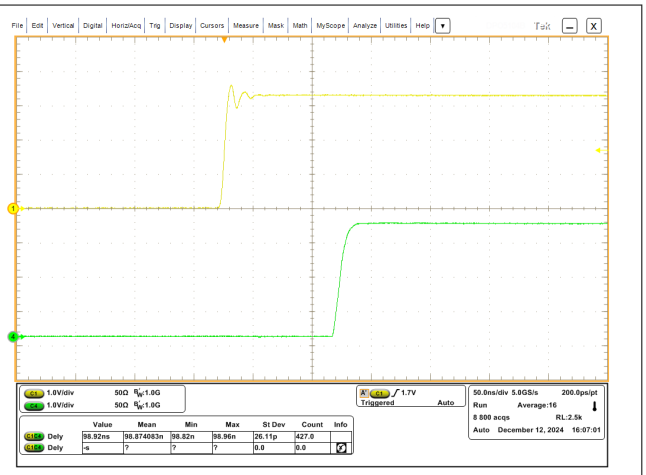
図 8-3. Typical CAN Bus

8.2.3 Application Curves



V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

図 8-4. $t_{PROP(LOOP1)}$



V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

図 8-5. $t_{PROP(LOOP2)}$

8.3 System Examples

The TCAN1472-Q1 CAN transceiver is typically used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. A 1.8V, 2.5V, or 3.3V application is shown in 図 8-6. The bus termination is shown for illustrative purposes.

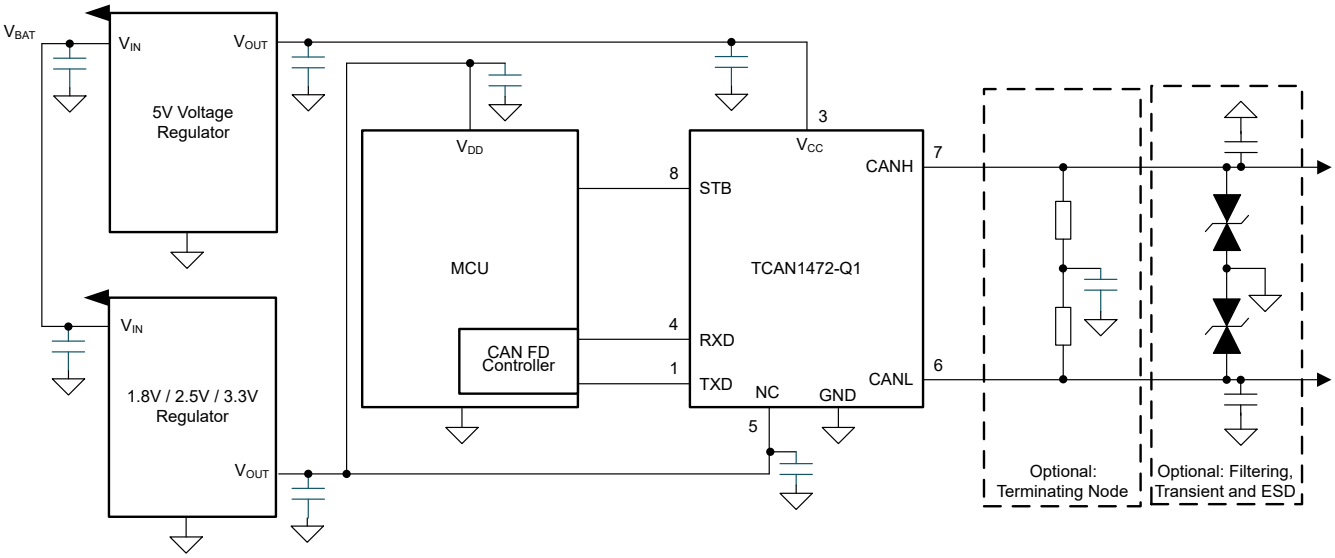


図 8-6. Typical Transceiver Application Using 1.8V, 2.5V, 3.3V IO Connections

8.4 Power Supply Recommendations

The TCAN1472-Q1 transceiver is designed to operate with a main V_{CC} input voltage supply range between 4.5V and 5.5V. The TCAN1472V-Q1 implements an I/O level shifting supply input, V_{IO}, designed for a range between 1.8V and 5.5V. Both supply inputs must be well regulated. A decoupling capacitance, typically 100nF, should be placed near the CAN transceiver main V_{CC} supply pin in addition to bypass capacitors. A decoupling capacitor, typically 100nF, should be placed near the CAN transceiver V_{IO} supply pin in addition to bypass capacitors.

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8.5 Layout

8.5.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connector, J1, to prevent transients, ESD, and noise from propagating onto the board. This layout example shows an optional transient voltage suppression (TVS) diode, D1, which may be implemented if the system-level requirements exceed the specified rating of the transceiver. This example also shows optional bus filter capacitors C4 and C5.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Decoupling capacitors should be placed as close as possible to the supply pins V_{CC} and V_{IO} of transceiver.
- Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

注

High frequency current follows the path of least impedance and not the path of least resistance.

- This layout example shows how split termination could be implemented on the CAN node. The termination is split into two resistors, R4 and R5, with the center or split tap of the termination connected to ground via capacitor C3. Split termination provides common mode filtering for the bus. See CAN Termination, and CAN Bus Short Circuit Current Limiting for information on termination concepts and power ratings needed for the termination resistor(s).

8.5.2 Layout Example

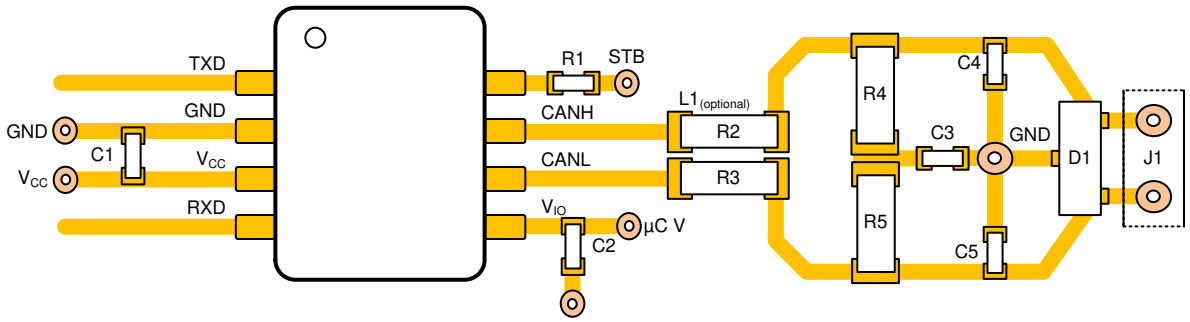


図 8-7. Layout Example

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 サポート・リソース

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9.3 Trademarks

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9.4 静電気放電に関する注意事項



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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

Changes from Revision * (June 2024) to Revision A (December 2024)	Page
• ドキュメントのステータスを「事前情報」から「量産データ」に変更	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCAN1472DDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	3LAF
TCAN1472DRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1472
TCAN1472DRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1472
TCAN1472DRQ1	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1472
TCAN1472DRQ1.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1472
TCAN1472VDDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	3LBF
TCAN1472VDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1472V
TCAN1472VDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1472V
TCAN1472VDRQ1	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1472V
TCAN1472VDRQ1.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1472V

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

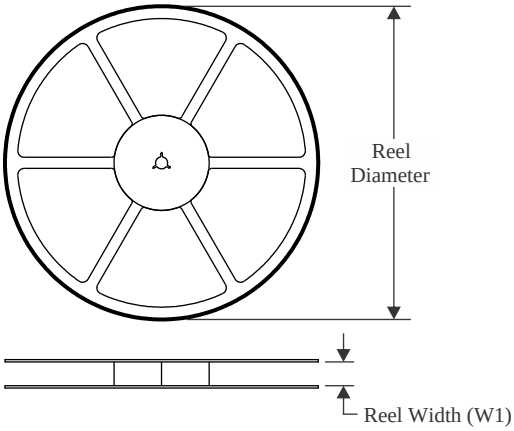
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

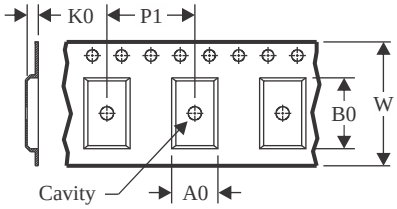
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

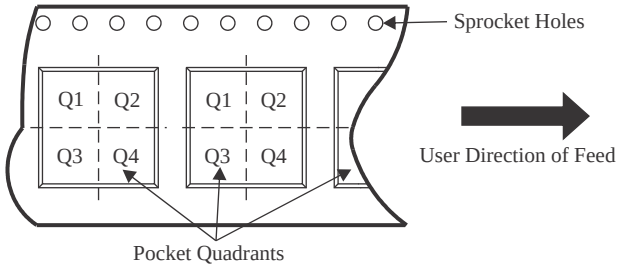


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

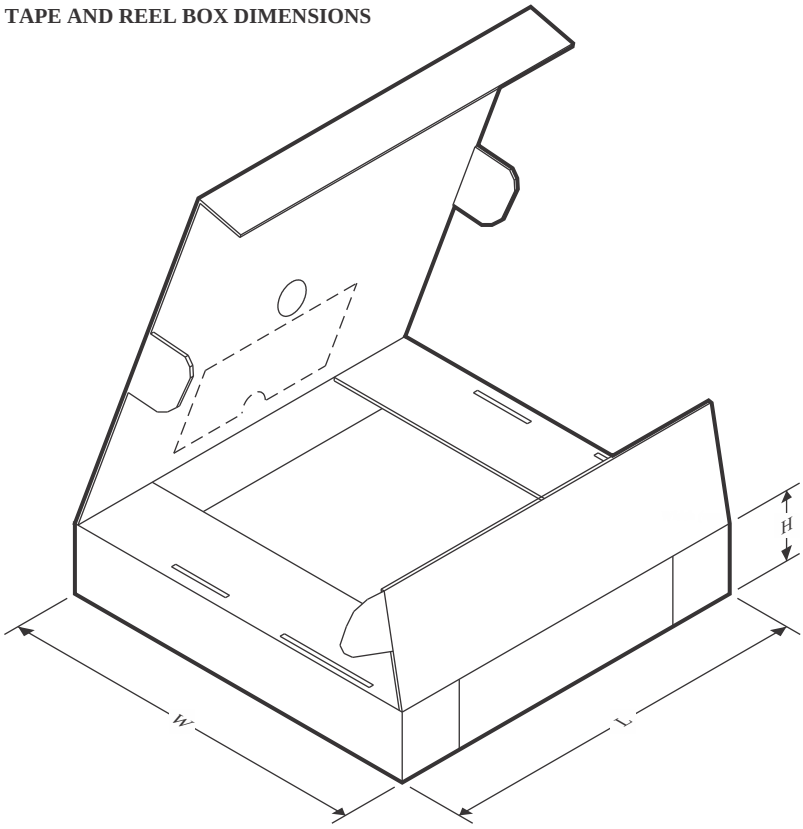
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1472DDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TCAN1472DRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TCAN1472DRQ1	SOIC	D	8	3000	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1472VDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TCAN1472VDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TCAN1472VDRQ1	SOIC	D	8	3000	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1472DDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TCAN1472DRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN1472DRQ1	SOIC	D	8	3000	340.5	338.1	20.6
TCAN1472VDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TCAN1472VDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN1472VDRQ1	SOIC	D	8	3000	340.5	338.1	20.6

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

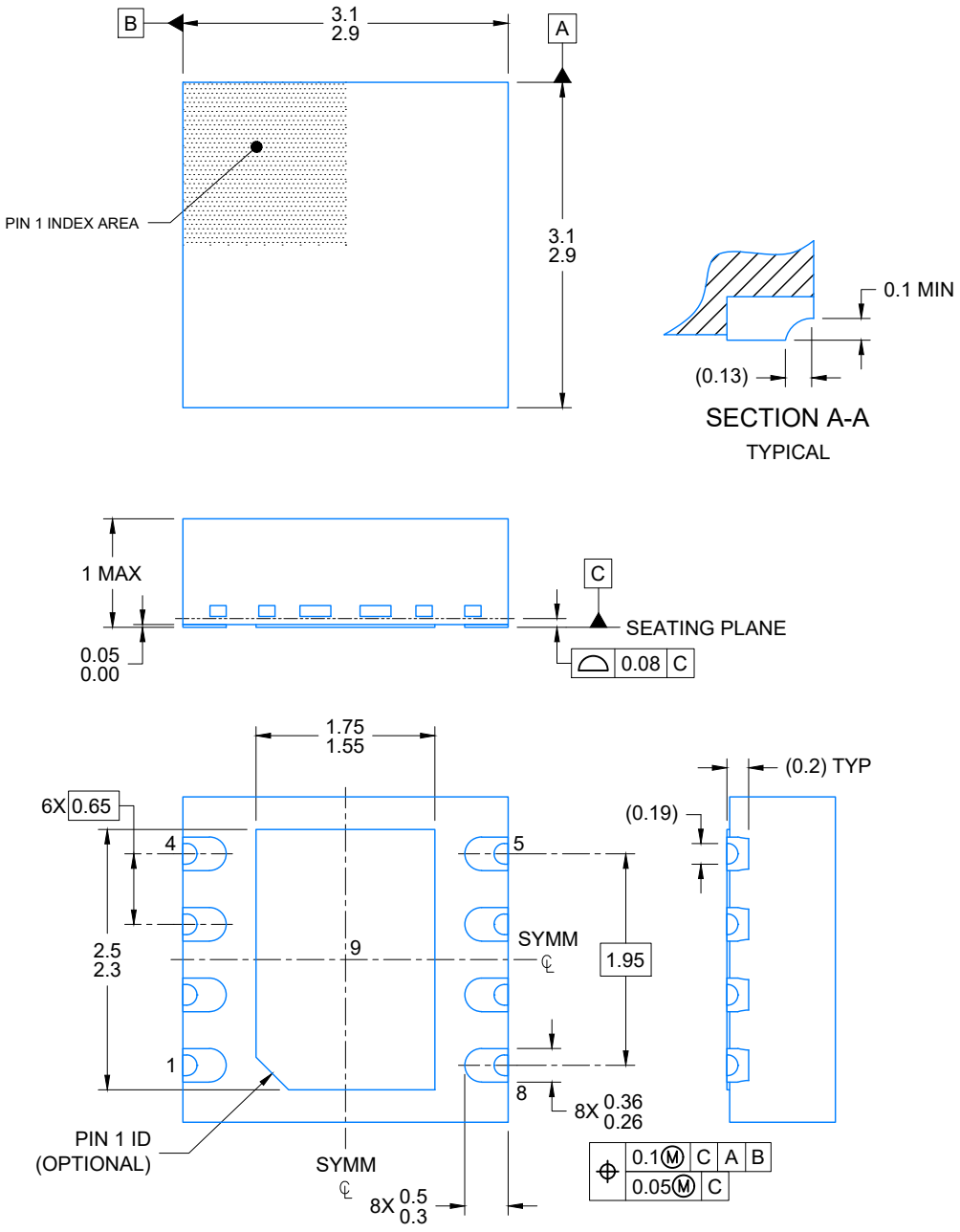
4203482/L

PACKAGE OUTLINE

DRB0008J

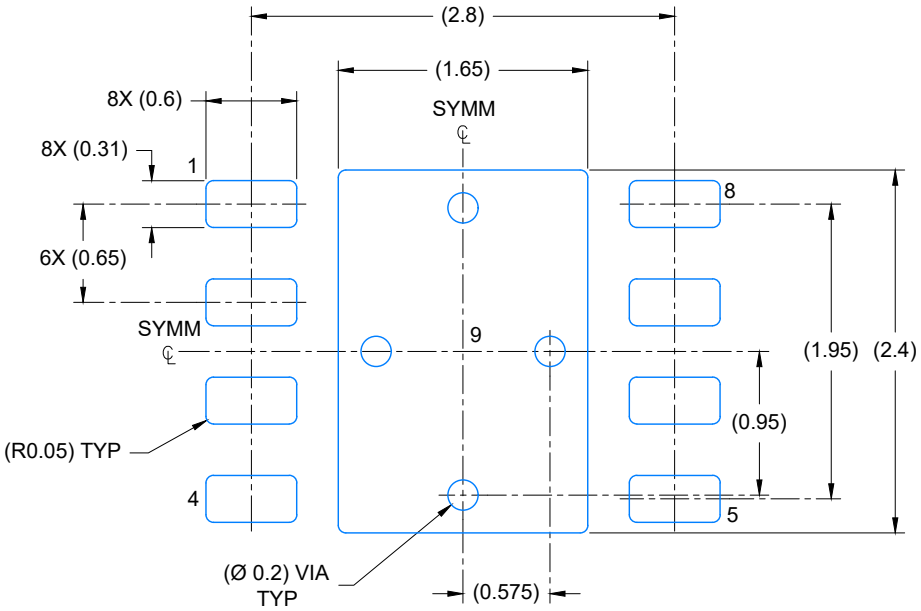
VSON - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

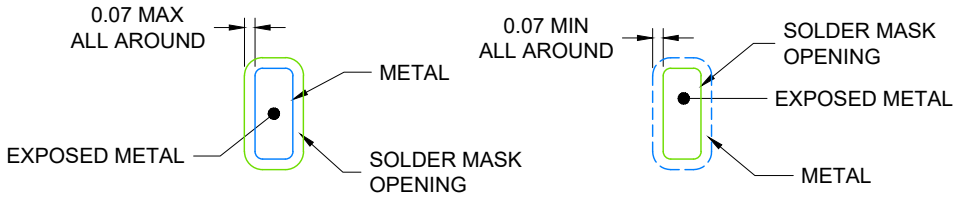


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON- SOLDER MASK
DEFINED
(PREFERRED)

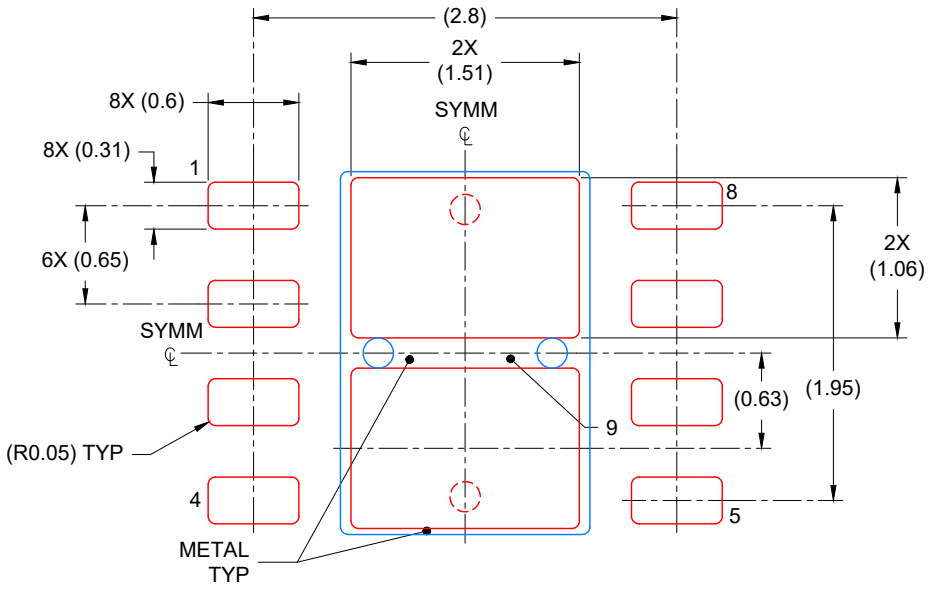
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225036/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

4225036/A 06/2019

NOTES: (continued)

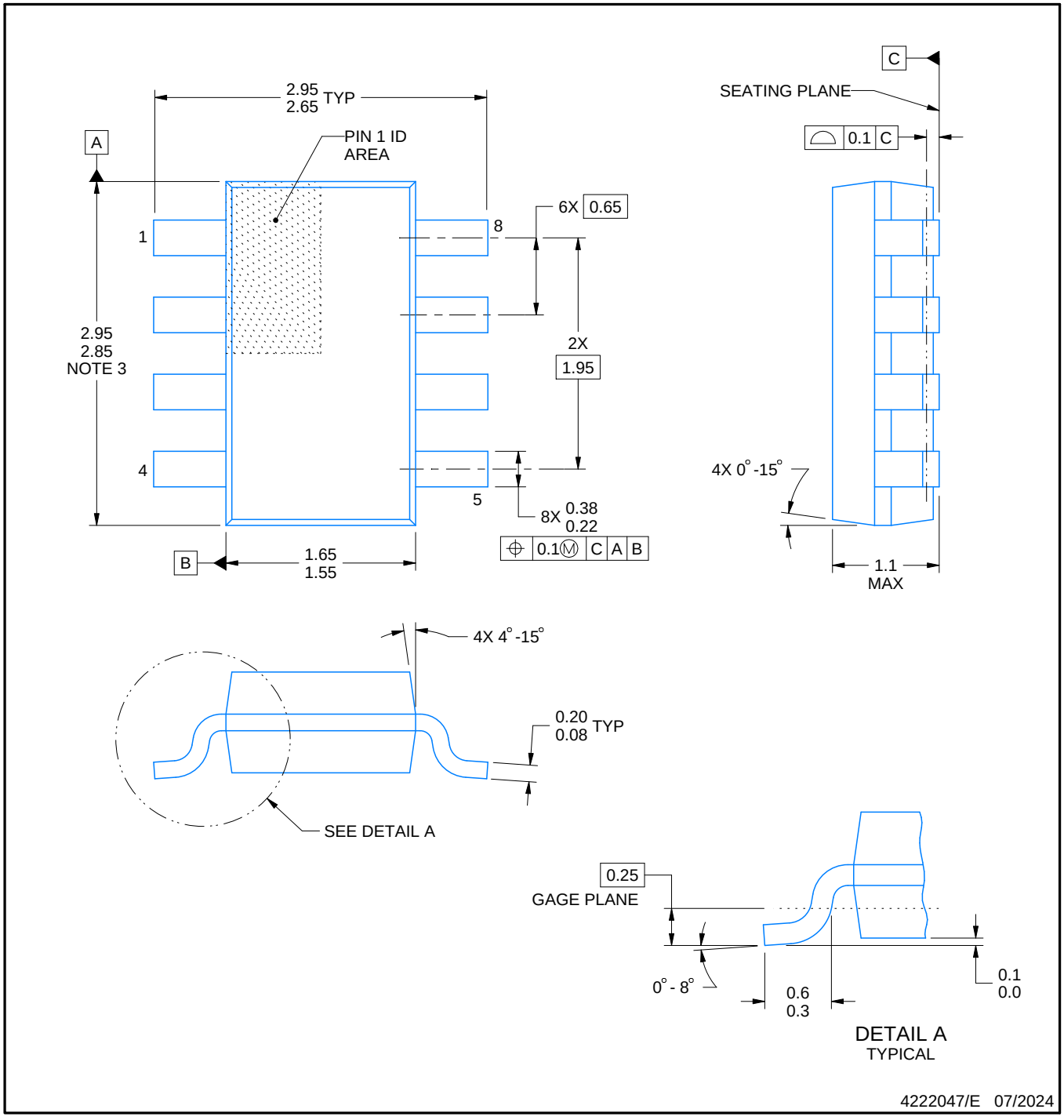
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DDF0008A

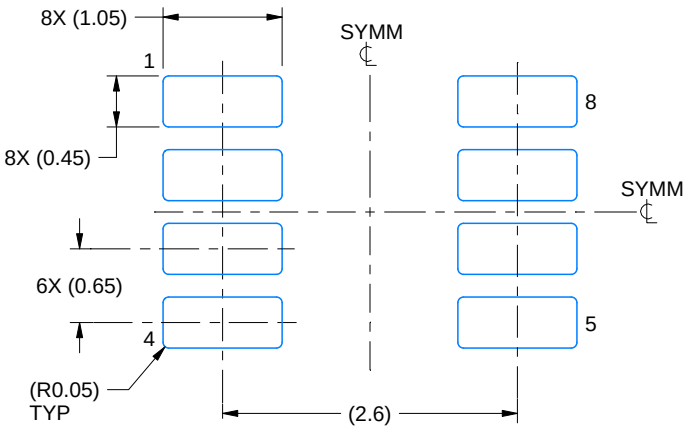
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

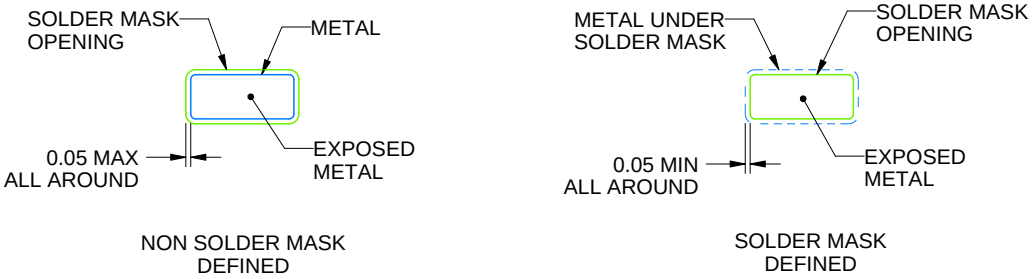


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

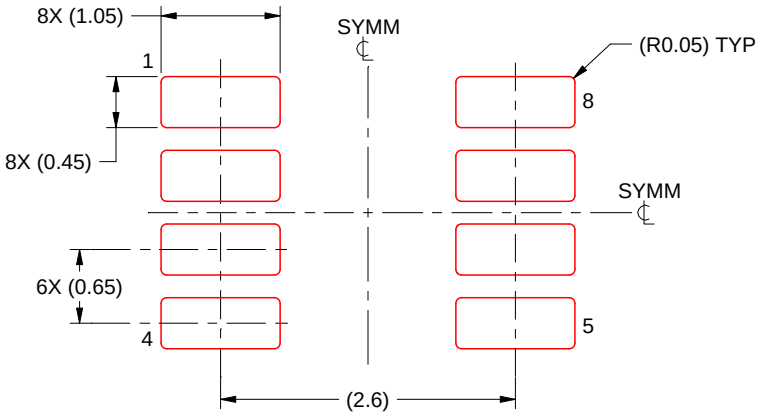
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

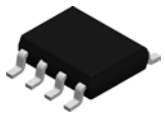


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

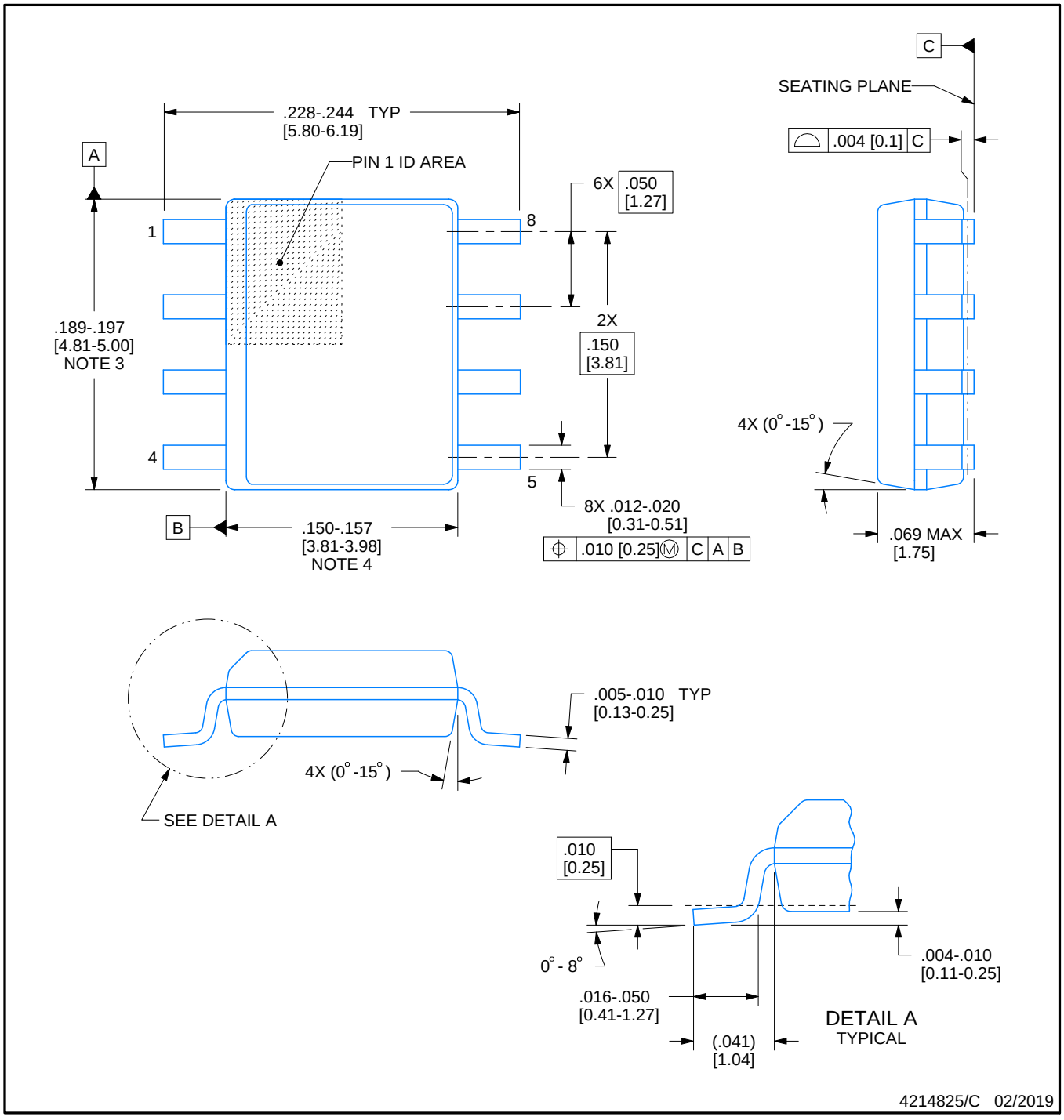


PACKAGE OUTLINE

D0008A

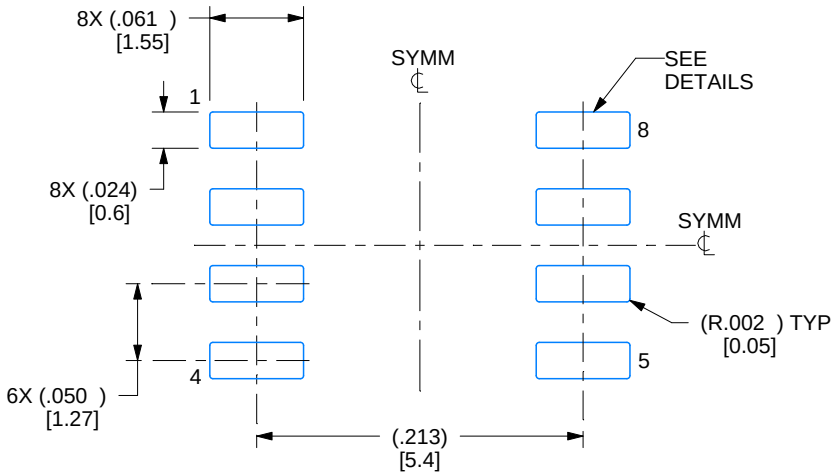
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

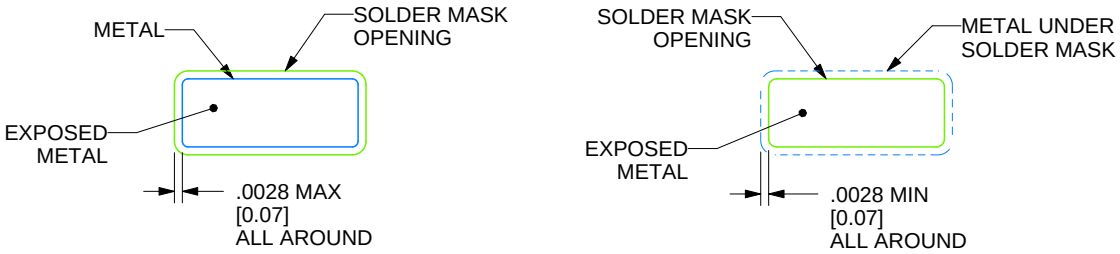


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

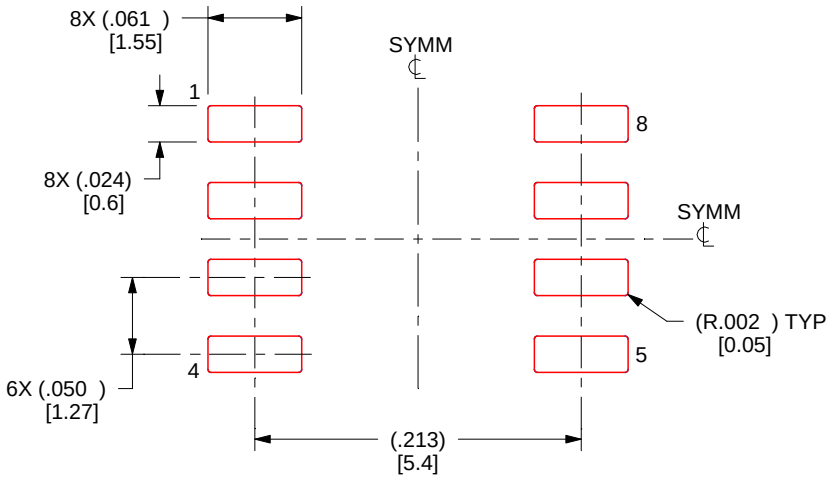
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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