

THS402x 2GHz、10V/V で安定、低ノイズ、高速アンプ

1 特長

- 1.2nV/√Hz の非常に低い電圧ノイズ
- 高速:
 - ゲイン帯域幅積: 2GHz
 - スルー レート: 470V/μs
 - 30ns のセトリング タイム (0.1%)
- 10V/V 以上のゲインで安定
- 出力駆動、 $I_O = 200\text{mA}$ (標準値)
- 非常に低い歪み:
 - THD = -68dBc ($f = 1\text{MHz}$, $R_L = 150\Omega$)
- 広範な電源:
 - $V_{CC} = \pm 4.5\text{V} \sim \pm 16\text{V}$
- THS4021 のオフセット nul ピン

2 アプリケーション

- 超音波スキャナ
- ソース メジャー ユニット (SMU)
- 電力品質メータ

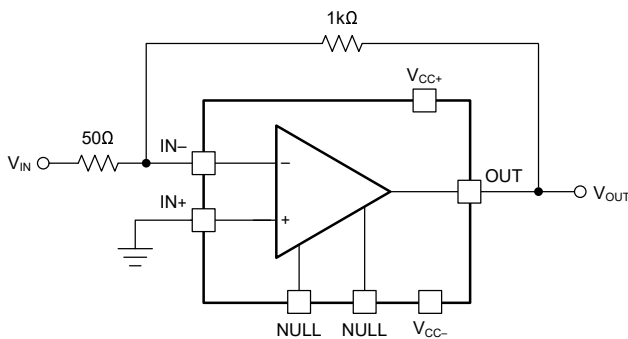
3 概要

THS4021 および THS4022 (THS402x) は電圧ノイズが非常に低い高速電圧帰還アンプで、通信やイメージングなど低い電圧ノイズが要求されるアプリケーションに最適です。シングルアンプの THS4021 とデュアルアンプの THS4022 は AC 性能が非常に優れており、10V/V のゲインで 290MHz の閉ループ帯域幅、470V/μs のスルーレート、30ns のセトリング タイム (0.1%) を実現します。THS402x は、10V/V 以上および -9V/V 以下のゲインで安定です。これらのアンプには、200mA の大きな駆動能力があり、アンプごとに 7.5mA の電流しか消費しません。f = 1MHz において全高調波歪み (THD) が -68dBc である THS402x は低歪みを必要とするアプリケーション用に設計されています。

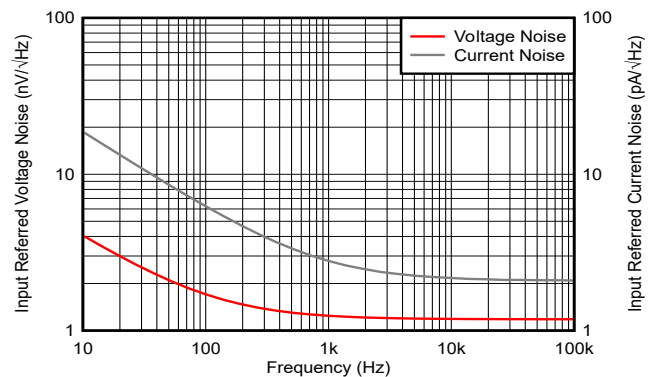
製品情報

部品番号	アンプ	パッケージ (1)
THS4021	1	D (SOIC, 8)
		DGN (HVSSOP, 8)
THS4022	2	DGN (HVSSOP, 8)

(1) 詳細については、[セクション 10](#) を参照してください。



アプリケーション概略図



電圧ノイズおよび電流ノイズと周波数との関係



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4 Pin Configuration and Functions

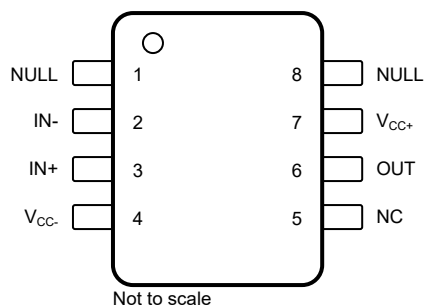


図 4-1. THS4021: D Package, 8-Pin SOIC, or DGN Package, 8-pin HVSSOP (Top View)

表 4-1. Pin Functions: THS4021

PIN		TYPE	DESCRIPTION
NAME	NO.		
IN–	2	Input	Inverting input
IN+	3	Input	Noninverting input
NC	5	—	No connection
NULL	1, 8	Input	Voltage offset adjust
OUT	6	Output	Output of amplifier
V _{CC–}	4	—	Negative power supply
V _{CC+}	7	—	Positive power supply

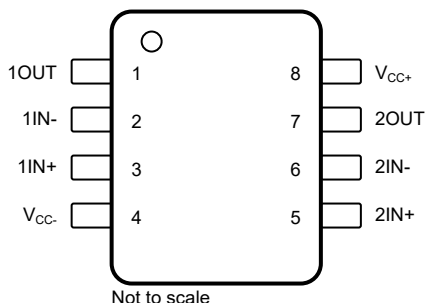


図 4-2. THS4022: DGN Package, 8-pin HVSSOP (Top View)

表 4-2. Pin Functions: THS4022

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN–	2	Input	Channel 1 inverting input
1IN+	3	Input	Channel 1 noninverting input
1OUT	1	Output	Channel 1 output
2IN–	6	Input	Channel 2 inverting input
2IN+	5	Input	Channel 2 noninverting input
2OUT	7	Output	Channel 2 output
V _{CC–}	4	—	Negative power supply
V _{CC+}	8	—	Positive power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC-} to V_{CC+}	Supply voltage			33	V
V_I	Input voltage			$\pm V_{CC}$	V
I_O	Output current ⁽²⁾			240	mA
V_{IO}	Differential input voltage			± 1.5	V
I_{IN}	Continuous input current			10	mA
T_J	Maximum junction temperature	Maximum junction temperature		150	°C
T_A	Operating free-air temperature	C-suffix	0	70	°C
		I-suffix	–40	85	
T_{stg}	Storage temperature		–65	150	°C
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds			300	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) When continuously operating at any output current, do not exceed the maximum junction temperature. Keep the output current less than the absolute maximum rating regardless of time interval.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	± 1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	± 1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Dual-supply	± 4.5	± 15	± 16	V
		Single-supply	9	30	32	
T_A	Operating free-air temperature	C-suffix	0	25	70	°C
		I-suffix	–40	25	85	

5.4 Thermal Information - THS4021

THERMAL METRIC ⁽¹⁾		THS4021		UNIT
		D (SOIC)	DGN (HVSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.5	58.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.0	4.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.2	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.6	N/A	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	71.4	N/A	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Thermal Information - THS4022

THERMAL METRIC ⁽¹⁾		THS4022		UNIT
		DGN (HVSSOP)		
		8 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	52		°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	75.2		°C/W
R _{θJB}	Junction-to-board thermal resistance	24.5		°C/W
Ψ _{JT}	Junction-to-top characterization parameter	4		°C/W
Ψ _{JB}	Junction-to-board characterization parameter	24.5		°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	9.1		°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.6 Electrical Characteristics - THS4021D and THS4022DGN

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, and $R_L = 150\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Small-signal bandwidth (−3 dB)	Gain = 10	V _{CC} = ±15 V		290		MHz
			V _{CC} = ±5 V		250		
		Gain = 20	V _{CC} = ±15 V		110		
			V _{CC} = ±5 V		100		
	Bandwidth for 0.1-dB flatness	Gain = 10	V _{CC} = ±15 V		17		
			V _{CC} = ±5 V		17		
	Full-power bandwidth ⁽¹⁾	V _{O(pp)} = 20 V, V _{CC} = ±15 V			7.5		
V _{O(pp)} = 5 V, V _{CC} = ±5 V			23.6				
SR	Slew rate ⁽²⁾	Gain = 10	V _{CC} = ±15 V, 20-V step		470		V/μs
			V _{CC} = ±5 V, 5-V step		370		
t _s	Settling time to 0.1%	Gain = −10	V _{CC} = ±15 V, 5-V step		30		ns
			V _{CC} = ±5 V, 2-V step		30		
	Settling time to 0.01%	Gain = −10	V _{CC} = ±15 V, 5-V step		160		
			V _{CC} = ±5 V, 2-V step		160		
NOISE AND DISTORTION PERFORMANCE							
THD	Total harmonic distortion	V _{O(pp)} = 2 V, f = 1 MHz, gain = 10, V _{CC} = ±15 V			−68		dBc
			R _L = 1 kΩ		−77		
		V _{O(pp)} = 2 V, f = 1 MHz, gain = 10, V _{CC} = ±5 V			−69		
			R _L = 1 kΩ		−78		
V _n	Input voltage noise	V _{CC} = ±5 V or ±15 V, f > 10 kHz			1.2		nV/√Hz
I _n	Input current noise	V _{CC} = ±5 V or ±15 V, f > 10 kHz			2.3		pA/√Hz
	Differential gain error	Gain = 10, NTSC, 40 IRE modulation, ±100 IRE ramp	V _{CC} = ±15		0.02		%
			V _{CC} = ±5 V		0.02		
	Differential phase error	Gain = 10, NTSC, 40 IRE modulation, ±100 IRE ramp	V _{CC} = ±15		0.08		°
			V _{CC} = ±5 V		0.06		
X _T	Channel-to-channel crosstalk (THS4022 only)	V _{CC} = ±5 V or ±15 V, f = 1 MHz			−54		dBc
DC PERFORMANCE							
	Open-loop gain	V _{CC} = ±15 V, V _O = ±10 V, R _L = 1 kΩ	T _A = 25°C	92	100		dB
			T _A = full range	91			
		V _{CC} = ±5 V, V _O = ±2.5 V, R _L = 1 kΩ	T _A = 25°C	86	98		
			T _A = full range	84			
V _{OS}	Input offset voltage	V _{CC} = ±5 V or ±15 V	T _A = 25°C		0.3	2	mV
			T _A = full range			3	
	Offset voltage drift	V _{CC} = ±5 V or ±15 V, T _A = full range			2		μV/°C
I _{IB}	Input bias current	V _{CC} = ±5 V or ±15 V	T _A = 25°C		9	20	μA
			T _A = full range			33	μA
I _{OS}	Input offset current	V _{CC} = ±5 V or ±15 V	T _A = 25°C		30	250	nA
			T _A = full range			400	nA
	Input offset current drift	V _{CC} = ±5 V or ±15 V, T _A = full range			0.2		nA/°C

5.6 Electrical Characteristics - THS4021D and THS4022DGN (続き)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, and $R_L = 150\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS							
V _{ICR}	Common-mode input voltage	V _{CC} = ±15 V		±13.8	±14.3		V
		V _{CC} = ±5 V		±3.8	±4.3		
CMRR	Common-mode rejection ratio	V _{CC} = ±15 V, V _{ICR} = ±12 V	T _A = 25 °C	95			dB
			T _A = full range	74			
		V _{CC} = ±5 V, V _{ICR} = ±2.5 V	T _A = 25 °C	100			
			T _A = full range	85			
r _i	Input resistance			1			MΩ
C _i	Input capacitance			1.5			pF
OUTPUT CHARACTERISTICS							
V _O	Output voltage swing	V _{CC} = ±15 V, R _L = 250 Ω		±12	±12.9		V
		V _{CC} = ±5 V, R _L = 150 Ω		±3	±3.5		
		V _{CC} = ±15 V, R _L = 1 kΩ		±13	±13.6		
		V _{CC} = ±5 V, R _L = 1 kΩ		±3.4	±3.8		
I _O	Output current	V _{CC} = ±15 V, R _L = 10 Ω		80	200		mA
		V _{CC} = ±5 V, R _L = 10 Ω		50	160		
R _O	Output resistance ⁽³⁾	Open-loop		5			Ω
POWER SUPPLY							
V _{CC}	Supply voltage	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I _{CC}	Supply current (per amplifier)	V _{CC} = ±15 V	T _A = 25°C	7.5		10	mA
			T _A = full range			11	
		V _{CC} = ±5 V	T _A = 25°C	6.5		9	
			T _A = full range			10.5	
PSRR	Power-supply rejection ratio	V _{CC} = ±5 V or ±15 V	T _A = 25 °C	95			dB
			T _A = full range	80			

(1) Full-power bandwidth = slew rate / [$\pi V_{O(P-P)}$].

(2) Slew rate is measured from an output level range of 25% to 75%.

(3) Keep junction temperature less than the absolute maximum rating when the output is heavily loaded or shorted; see also [セクション 5.1](#).

5.7 Electrical Characteristics - THS4021DGN

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, $R_L = 150\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Small-signal bandwidth (−3 dB)	Gain = 10	V _{CC} = ±15 V		350		MHz
			V _{CC} = ±5 V		280		
		Gain = 20	V _{CC} = ±15 V		80		
			V _{CC} = ±5 V		70		
	Bandwidth for 0.1-dB flatness	Gain = 10	V _{CC} = ±15 V		17		
			V _{CC} = ±5 V		17		
Full-power bandwidth ⁽¹⁾	V _{O(pp)} = 20 V, V _{CC} = ±15 V				3.7		
	V _{O(pp)} = 5 V, V _{CC} = ±5 V				11.8		
SR	Slew rate ⁽²⁾	Gain = 10	V _{CC} = ±15 V, 10-V step		470		V/μs
			V _{CC} = ±5 V, 5-V step		370		
t _s	Settling time to 0.1%	Gain = −10	V _{CC} = ±15 V, 5-V step		40		ns
			V _{CC} = ±5 V, 2-V step		50		
	Settling time to 0.01%	Gain = −10	V _{CC} = ±15 V, 5-V step		145		
			V _{CC} = ±5 V, 2-V step		150		
NOISE/DISTORTION PERFORMANCE							
THD	Total harmonic distortion	V _{O(pp)} = 2 V, f = 1 MHz, gain = 2, V _{CC} = ±15 V			−68		dBc
			R _L = 1 kΩ		−77		
		V _{O(pp)} = 2 V, f = 1 MHz, gain = 2, V _{CC} = ±5 V			−69		
			R _L = 1 kΩ		−78		
V _n	Input voltage noise	V _{CC} = ±5 V or ±15 V, f > 10 kHz			1.5		nV/√Hz
I _n	Input current noise	V _{CC} = ±5 V or ±15 V, f > 10 kHz			2		pA/√Hz
	Differential gain error	Gain = 2, NTSC, 40 IRE modulation, ±100 IRE ramp	V _{CC} = ±15		0.02		%
			V _{CC} = ±5 V		0.02		
	Differential phase error	Gain = 2, NTSC, 40 IRE modulation, ±100 IRE ramp	V _{CC} = ±15		0.08		°
			V _{CC} = ±5 V		0.06		
DC PERFORMANCE							
	Open-loop gain	V _{CC} = ±15 V, V _O = ±10 V, R _L = 1 kΩ	T _A = 25°C	40	60		V/mV
			T _A = full range	35			
		V _{CC} = ±5 V, V _O = ±2.5 V, R _L = 250 Ω	T _A = 25°C	20	35		
			T _A = full range	15			
V _{OS}	Input offset voltage	V _{CC} = ±5 V or ±15 V	T _A = 25°C		0.5	2	mV
			T _A = full range			3	
	Offset voltage drift	V _{CC} = ±5 V or ±15 V	T _A = full range		15		μV/°C
I _{IB}	Input bias current	V _{CC} = ±5 V or ±15 V	T _A = 25°C		3	6	μA
			T _A = full range			6	
I _{OS}	Input offset current	V _{CC} = ±5 V or ±15 V	T _A = 25°C		30	250	nA
			T _A = full range			400	
	Input offset current drift	T _A = full range				0.3	nA/°C

5.7 Electrical Characteristics - THS4021DGN (続き)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, $R_L = 150\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS							
V _{ICR}	Common-mode input voltage	V _{CC} = ±15 V		±13.8	±14.3		V
		V _{CC} = ±5 V		±3.8	±4.3		
CMRR	Common-mode rejection ratio	V _{CC} = ±15 V, V _{ICR} = ±12 V, T _A = full range		74	95		dB
r _i	Input resistance				1		MΩ
C _i	Input capacitance				1.5		pF
OUTPUT CHARACTERISTICS							
V _O	Output voltage swing	V _{CC} = ±15 V, R _L = 250 Ω		±12	±12.5		V
		V _{CC} = ±5 V, R _L = 150 Ω		±3	±3.3		
		V _{CC} = ±15 V, R _L = 150 Ω		±13	±13.5		
		V _{CC} = ±5 V, R _L = 150 Ω		±3.4	±3.8		
I _O	Output current	R _L = 20 Ω	V _{CC} = ±15 V	80	100		mA
			V _{CC} = ±5 V	50	75		
I _{SC}	Short-circuit current ⁽³⁾	V _{CC} = ±15 V			150		mA
R _O	Output resistance ⁽³⁾	Open loop			13		Ω
POWER SUPPLY							
V _{CC}	Supply voltage	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I _{CC}	Supply current (per amplifier)	V _{CC} = ±15 V	T _A = 25°C		7.8	10	mA
			T _A = full range			11	
		V _{CC} = ±5 V	T _A = 25°C		6.7	9	
			T _A = full range			10.5	
PSRR	Power-supply rejection ratio	V _{CC} = ±5 V or ±15 V, T _A = full range		80	95		dB

(1) Full-power bandwidth = slew rate / $2\pi V_{O(\text{Peak})}$.

(2) Slew rate is measured from an output level range of 25% to 75%.

(3) Keep junction temperature less than the absolute maximum rating when the output is heavily loaded or shorted; see also [セクション 5.1](#).

5.8 Typical Characteristics: THS4021D and THS4022DGN

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, gain = +10 V/V, $R_L = 150\ \Omega$, and $R_F = 220\ \Omega$ (unless otherwise noted)

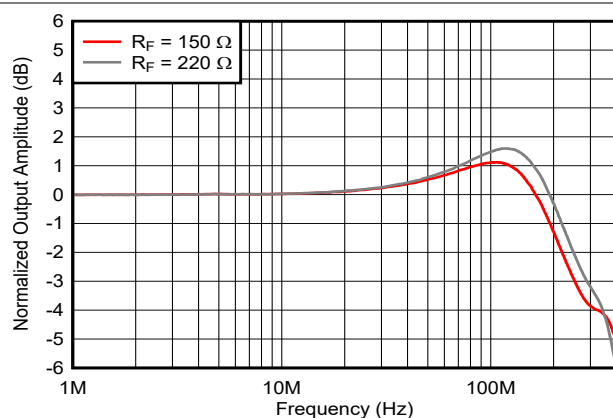


図 5-1. Frequency Response vs Feedback Resistance

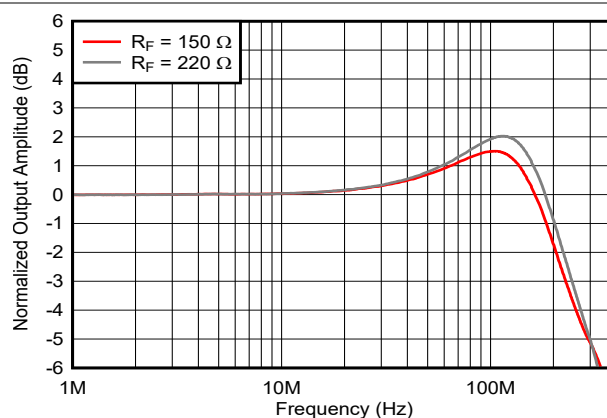


図 5-2. Frequency Response vs Feedback Resistance

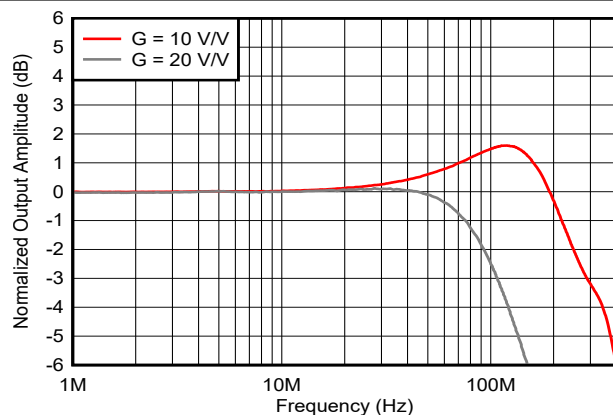


図 5-3. Frequency Response vs Gain

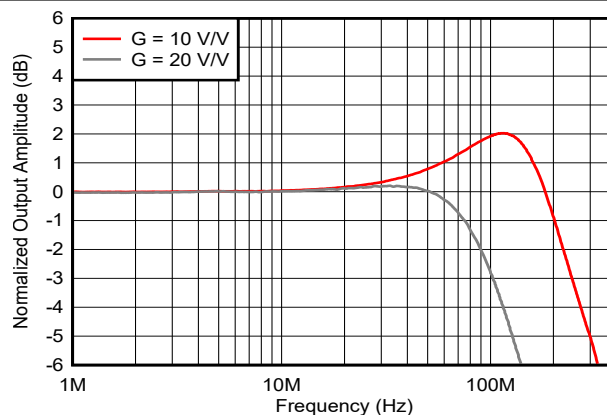


図 5-4. Frequency Response vs Gain

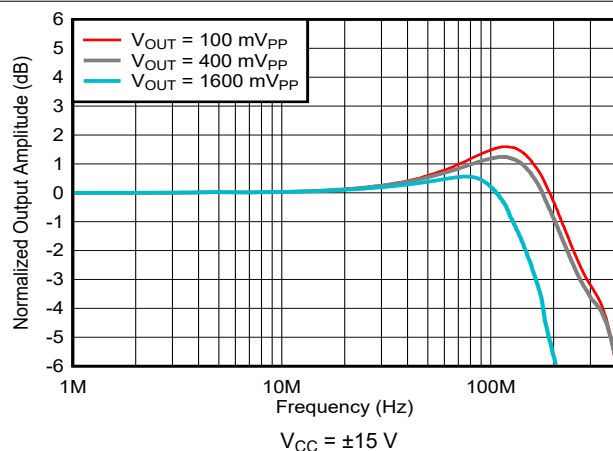


図 5-5. Large-Signal Frequency Response

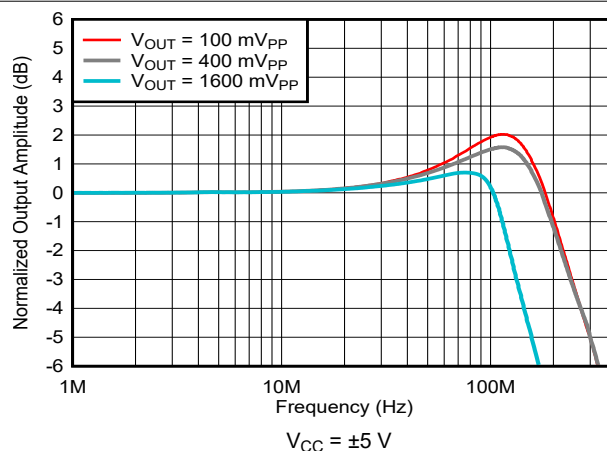


図 5-6. Large-Signal Frequency Response

5.8 Typical Characteristics: THS4021D and THS4022DGN (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, gain = +10 V/V, $R_L = 150\ \Omega$, and $R_F = 220\ \Omega$ (unless otherwise noted)

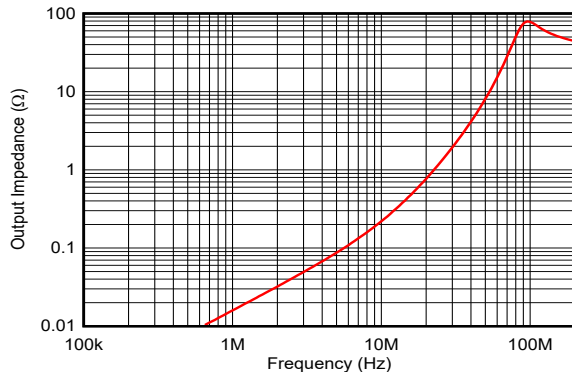


Figure 5-7. Closed-Loop Output Impedance

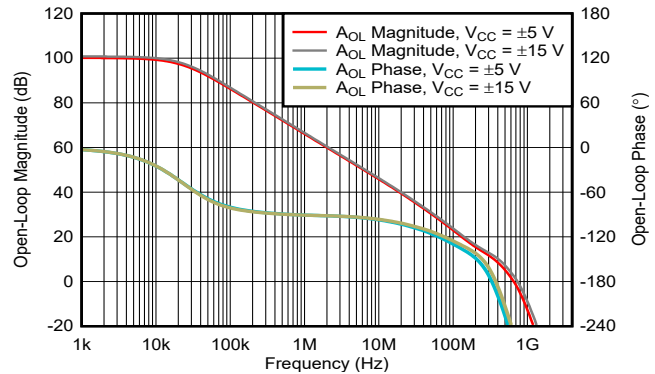


Figure 5-8. Open-loop Gain and Phase Response

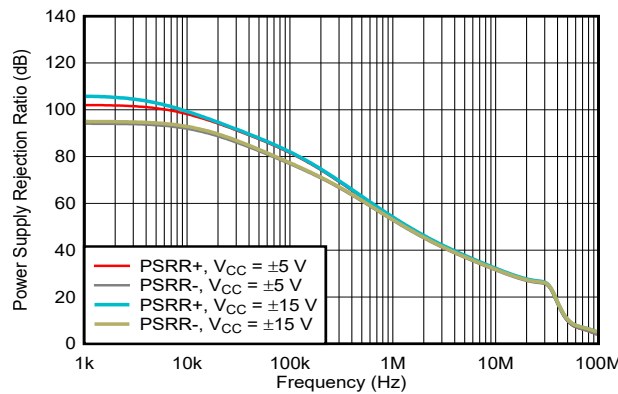


Figure 5-9. Power-Supply Rejection Ratio vs Frequency

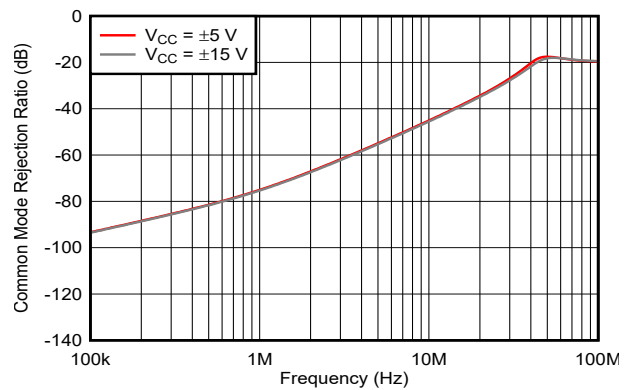


Figure 5-10. Common-Mode Rejection Ratio vs Frequency

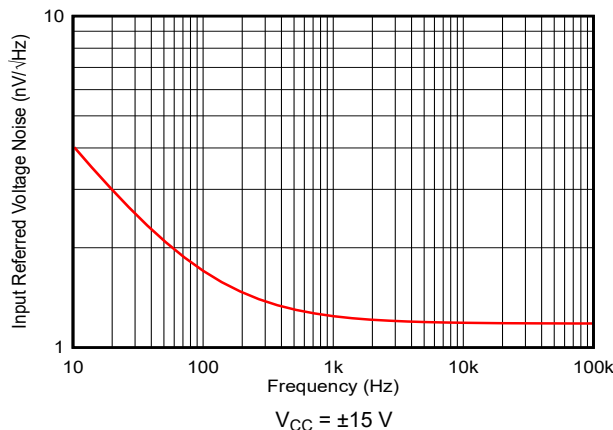


Figure 5-11. Input-Referred Voltage Noise vs Frequency

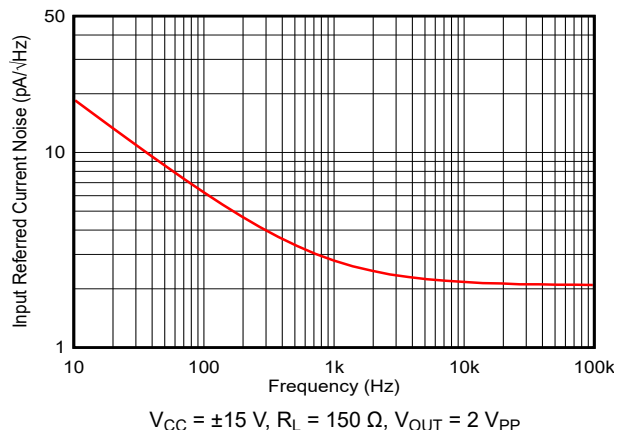


Figure 5-12. Input-Referred Current Noise vs Frequency

5.8 Typical Characteristics: THS4021D and THS4022DGN (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, gain = +10 V/V, $R_L = 150\ \Omega$, and $R_F = 220\ \Omega$ (unless otherwise noted)

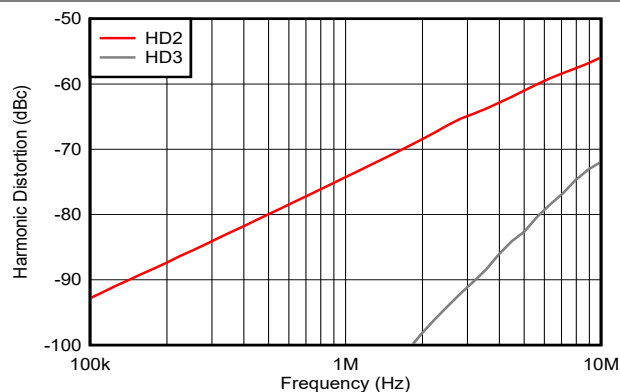


FIG 5-13. Harmonic Distortion vs Frequency

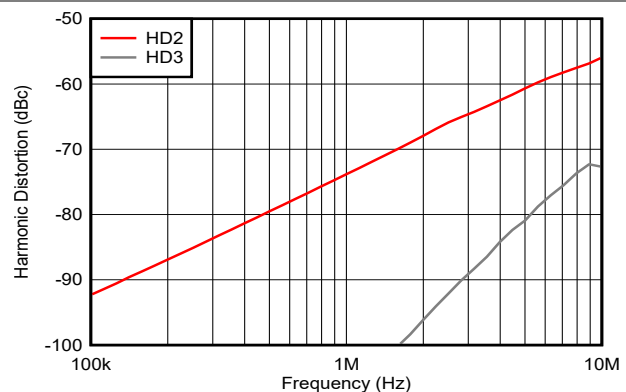


FIG 5-14. Harmonic Distortion vs Frequency

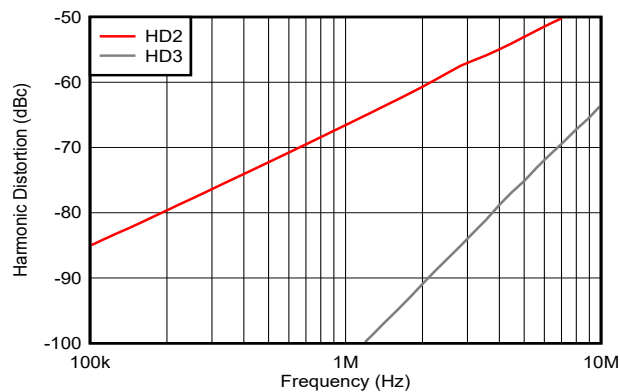


FIG 5-15. Harmonic Distortion vs Frequency

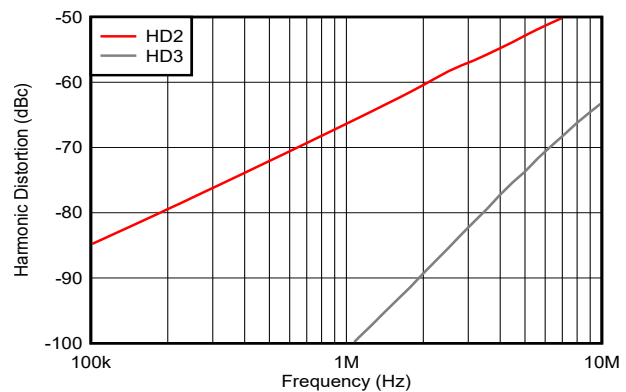


FIG 5-16. Harmonic Distortion vs Frequency

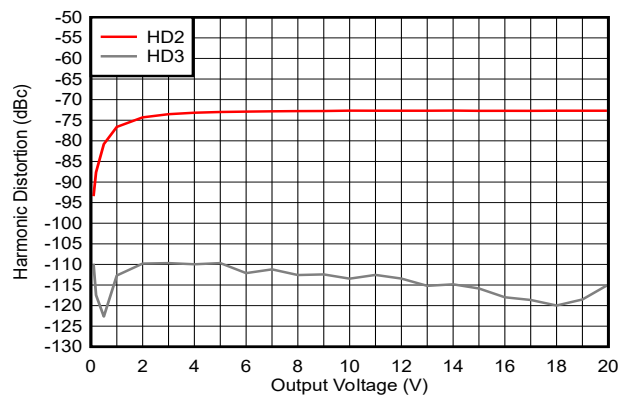


FIG 5-17. Harmonic Distortion vs Peak-to-Peak Output Voltage

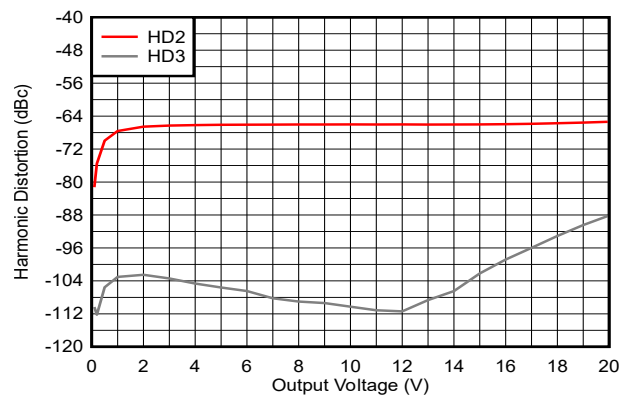


FIG 5-18. Harmonic Distortion vs Peak-to-Peak Output Voltage

5.8 Typical Characteristics: THS4021D and THS4022DGN (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, gain = +10 V/V, $R_L = 150\ \Omega$, and $R_F = 220\ \Omega$ (unless otherwise noted)

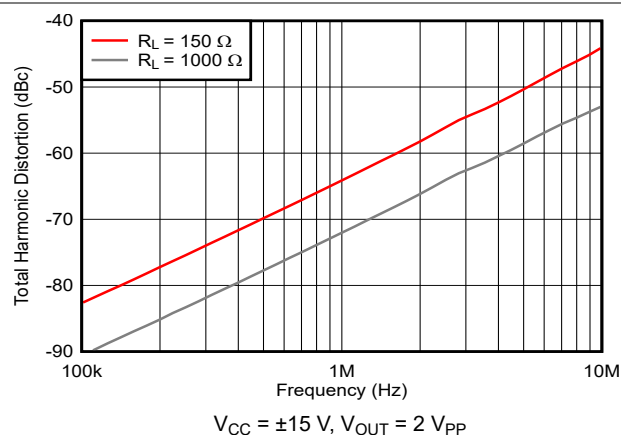


図 5-19. Total Harmonic Distortion vs Frequency

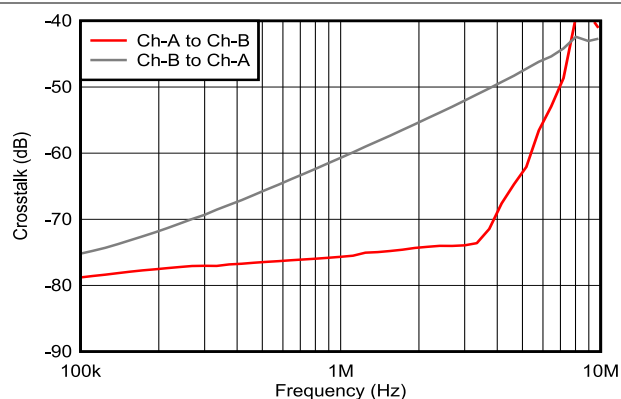


図 5-20. Crosstalk vs Frequency

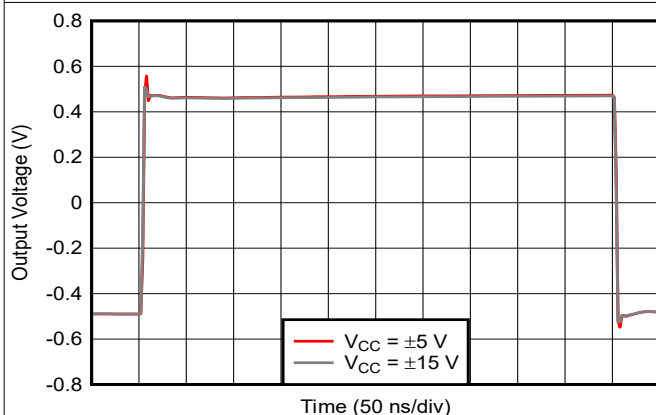


図 5-21. 1-V Step Response

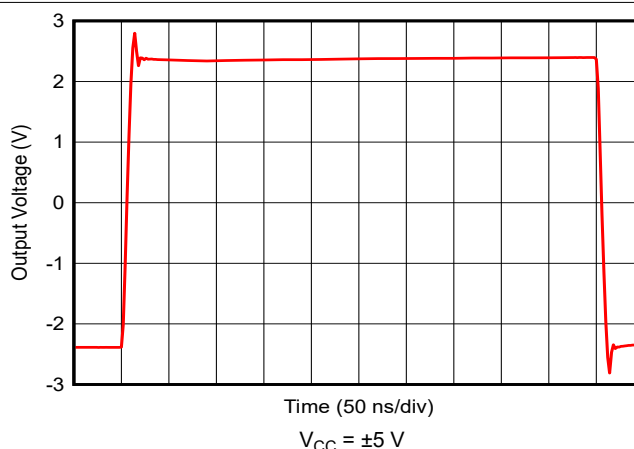


図 5-22. 5-V Step Response

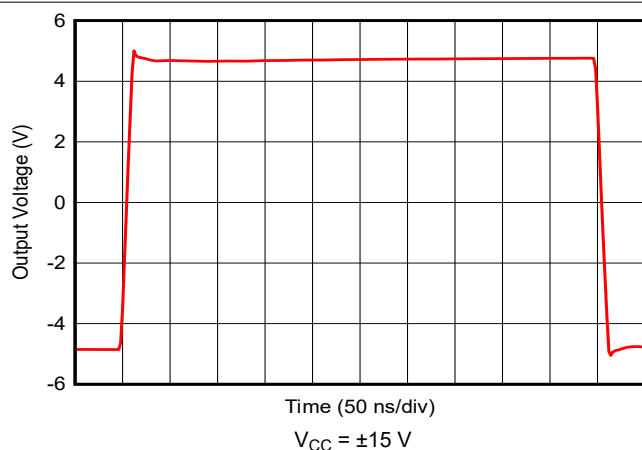


図 5-23. 10-V Step Response

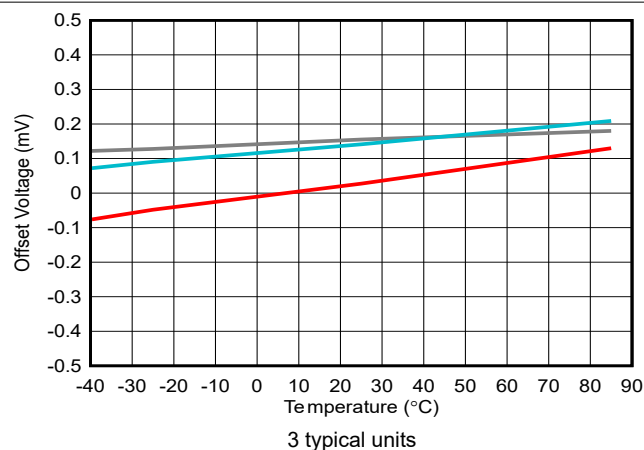


図 5-24. Input Offset Voltage vs Ambient Temperature

5.8 Typical Characteristics: THS4021D and THS4022DGN (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, gain = +10 V/V, $R_L = 150\ \Omega$, and $R_F = 220\ \Omega$ (unless otherwise noted)

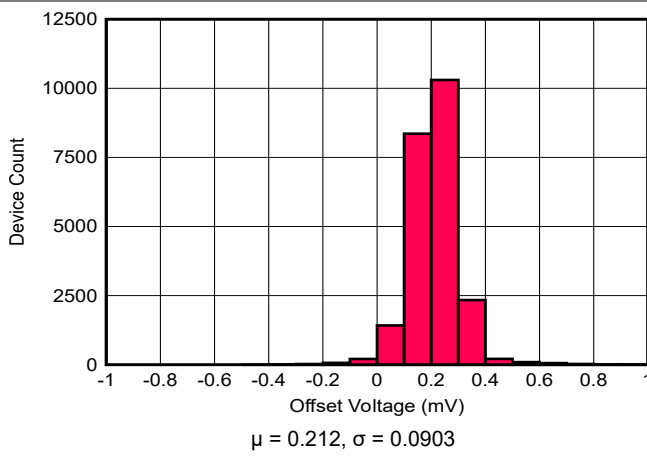


Figure 5-25. Voltage Offset Distribution

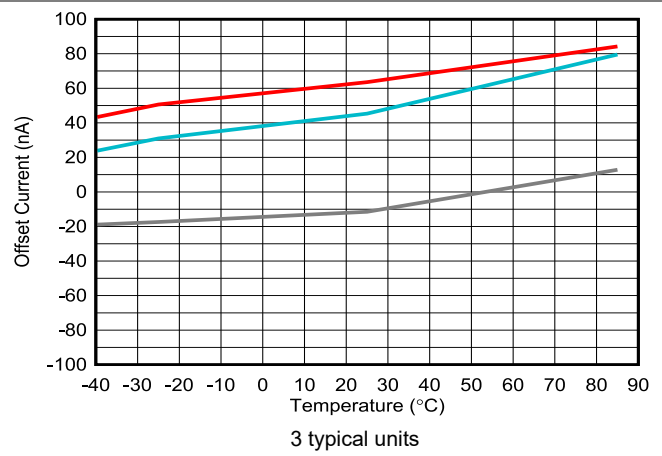


Figure 5-26. Input Offset Current vs Ambient Temperature

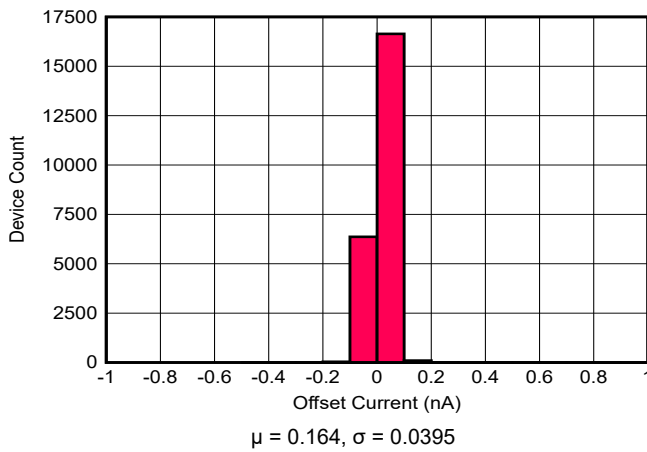


Figure 5-27. Input Offset Current vs Ambient Temperature

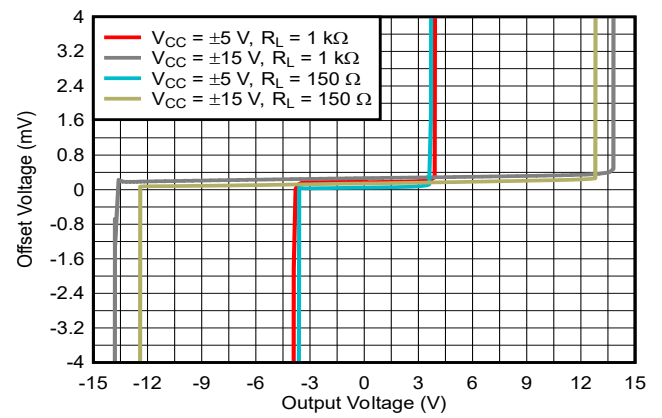


Figure 5-28. Offset Voltage vs Output Voltage

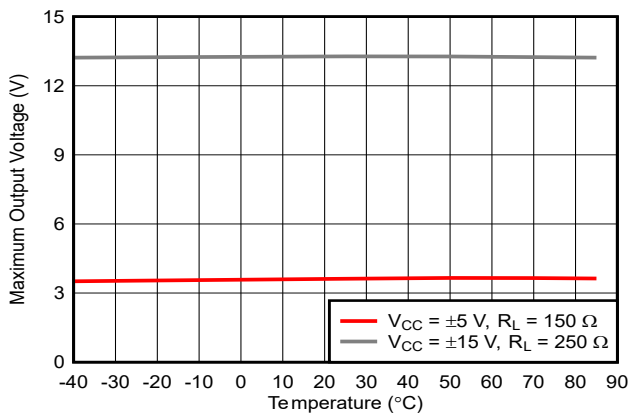


Figure 5-29. Maximum Output Voltage Swing vs Ambient Temperature

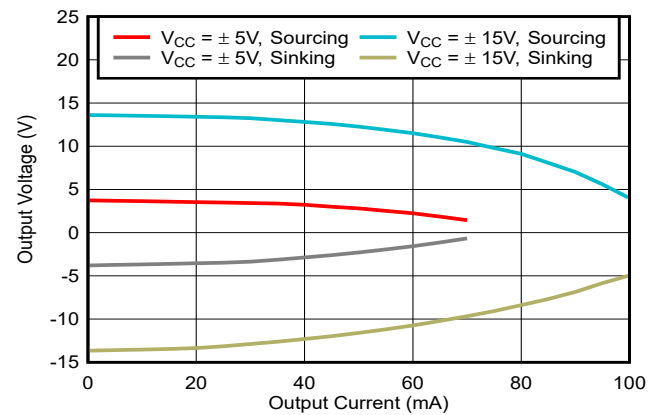


Figure 5-30. Output Swing vs Load Current

5.8 Typical Characteristics: THS4021D and THS4022DGN (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, gain = +10 V/V, $R_L = 150\ \Omega$, and $R_F = 220\ \Omega$ (unless otherwise noted)

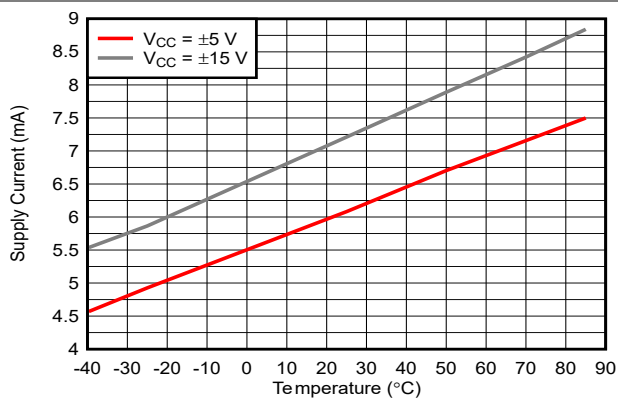


図 5-31. Supply Current vs Ambient Temperature

5.9 Typical Characteristics: THS4021DGN

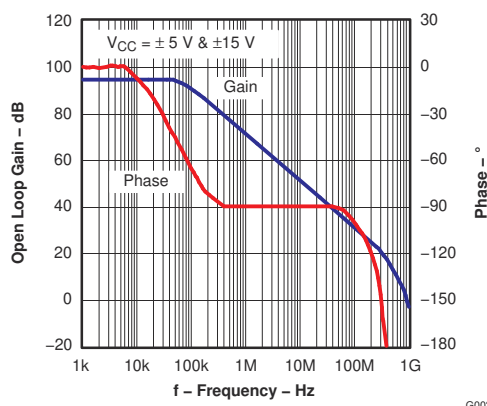


Figure 5-32. Open Loop Gain and Phase Response vs Frequency

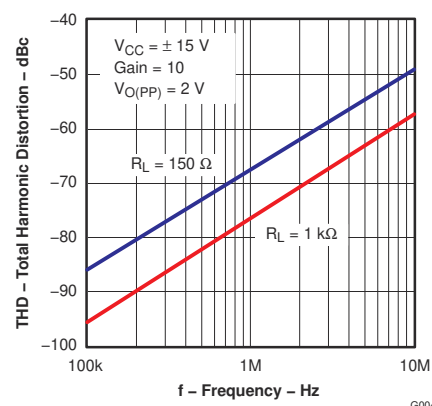


Figure 5-33. Total Harmonic Distortion vs Frequency

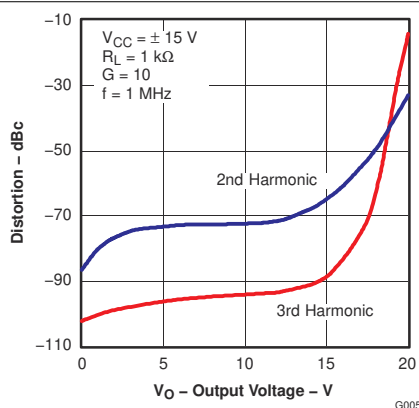


Figure 5-34. Distortion vs Output Voltage

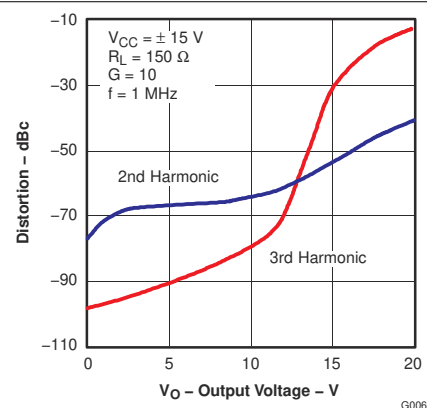


Figure 5-35. Distortion vs Output Voltage

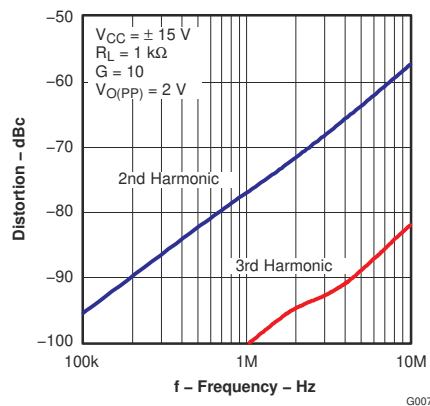


Figure 5-36. Distortion vs Frequency

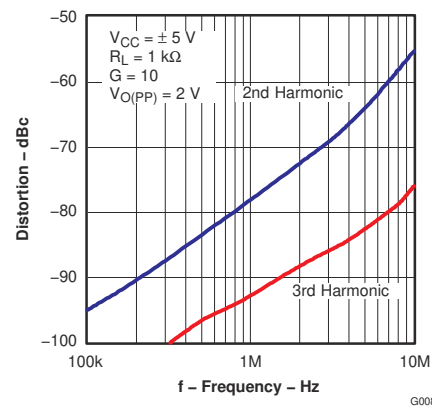


Figure 5-37. Distortion vs Frequency

5.9 Typical Characteristics: THS4021DGN (continued)

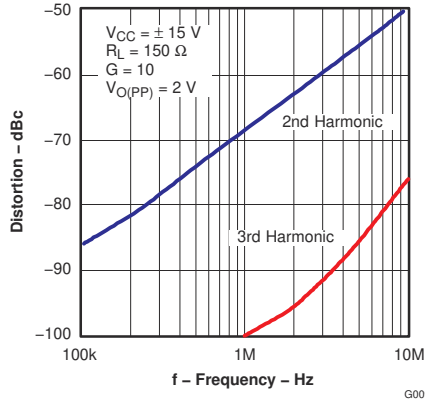


Figure 5-38. Distortion vs Frequency

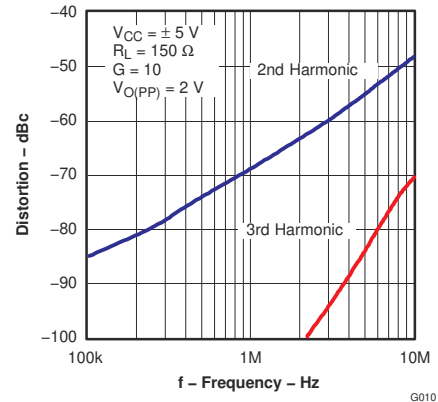


Figure 5-39. Distortion vs Frequency

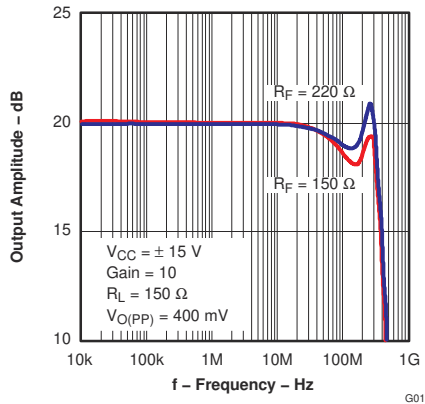


Figure 5-40. Output Amplitude vs Frequency

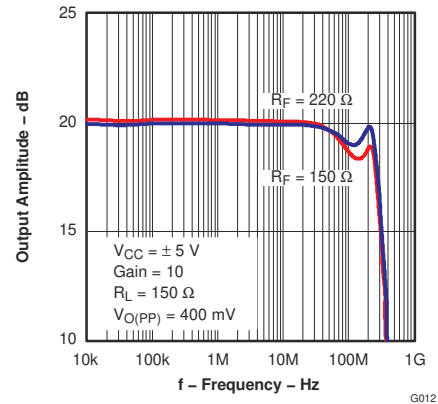


Figure 5-41. Output Amplitude vs Frequency

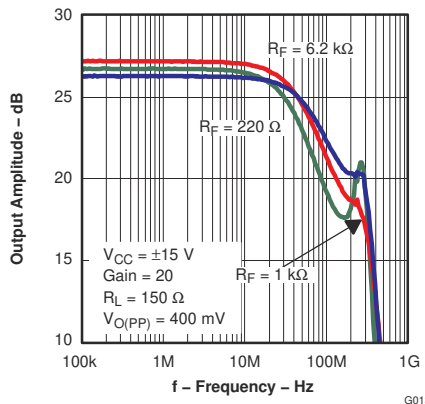


Figure 5-42. Output Amplitude vs Frequency

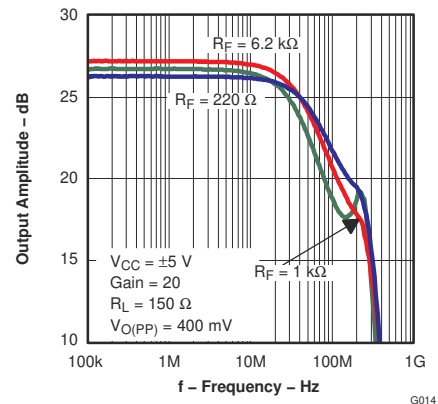


Figure 5-43. Output Amplitude vs Frequency

5.9 Typical Characteristics: THS4021DGN (continued)

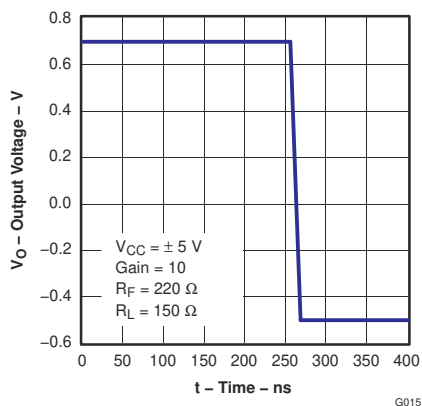


Figure 5-44. 1-V Step Response

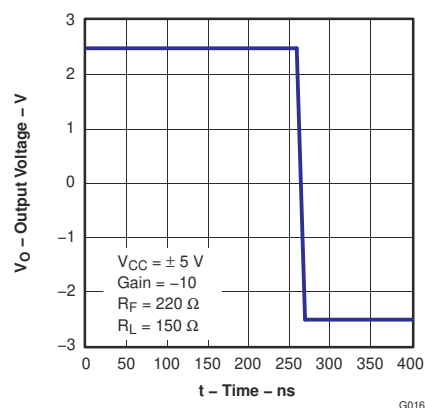


Figure 5-45. 5-V Step Response

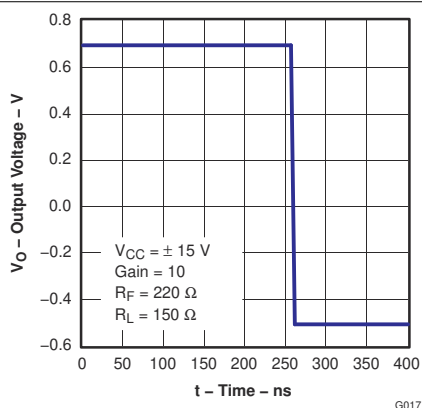


Figure 5-46. 1-V Step Response

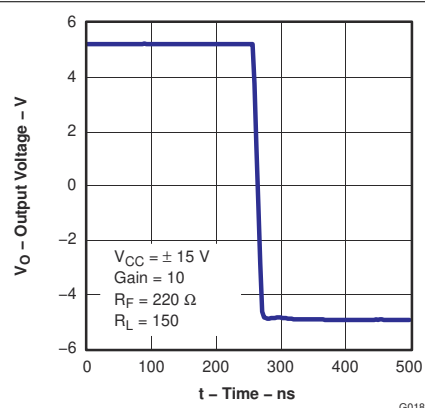


Figure 5-47. 10-V Step Response

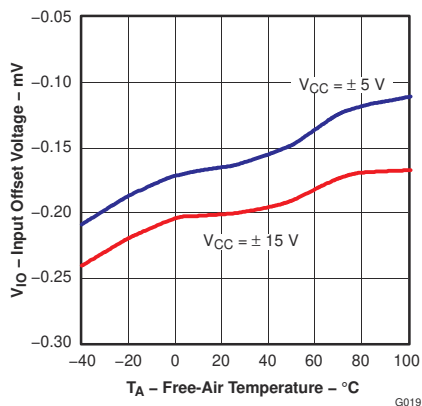


Figure 5-48. Input Offset Voltage vs Free-air Temperature

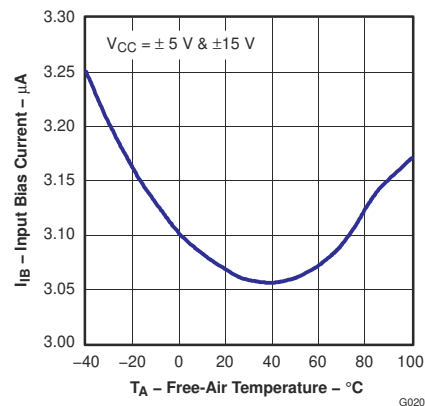


Figure 5-49. Input Bias Current vs Free-air Temperature

5.9 Typical Characteristics: THS4021DGN (continued)

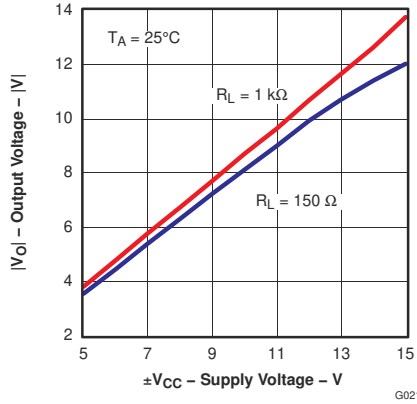


Figure 5-50. Output Voltage vs Supply Voltage

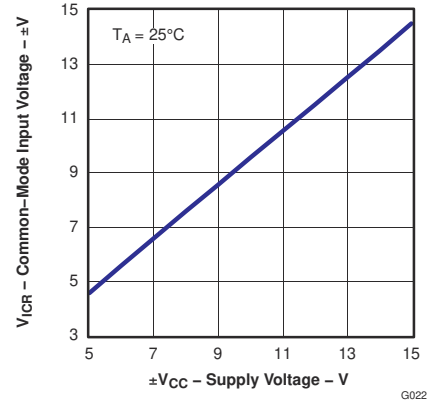


Figure 5-51. Common-mode Input Voltage vs Supply Voltage

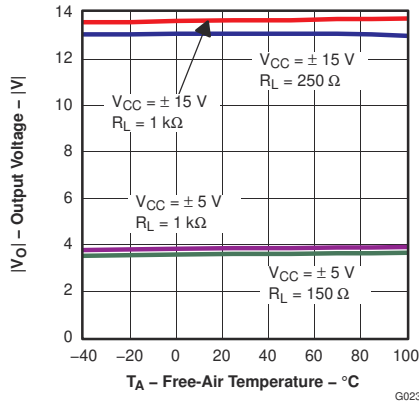


Figure 5-52. Output Voltage vs Free-air Temperature

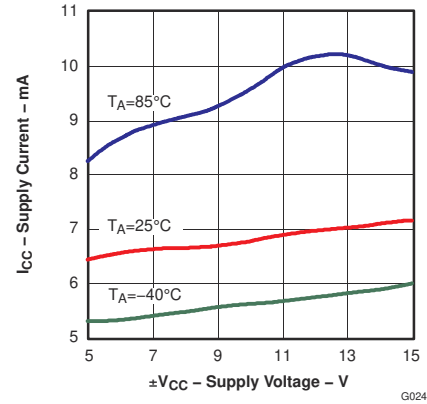


Figure 5-53. Supply Current vs Supply Voltage

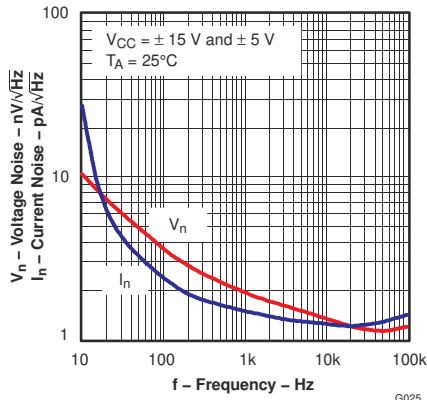


Figure 5-54. Voltage and Current Noise vs Frequency

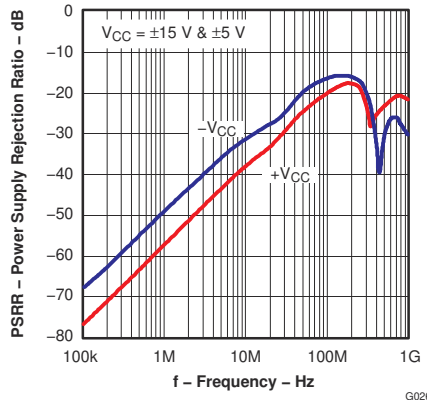


Figure 5-55. Power Supply Rejection Ratio vs Frequency

5.9 Typical Characteristics: THS4021DGN (continued)

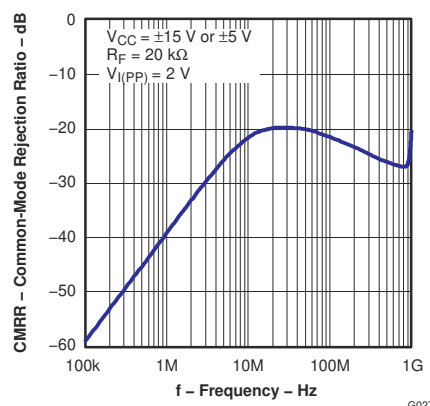


图 5-56. Common Mode Rejection Ratio vs Frequency

6 Detailed Description

6.1 Overview

The THS402x are high-speed operational amplifiers configured in a decompensated voltage-feedback architecture. The THS402x are stable with gain configurations of 10 V/V or greater. These amplifiers are built using a greater than 30-V, complementary, bipolar process with NPN and PNP transistors possessing an f_T of several GHz. This configuration results in exceptionally high-performance amplifiers with wide bandwidth, high slew rate, fast settling time, and low distortion.

6.2 Functional Block Diagram

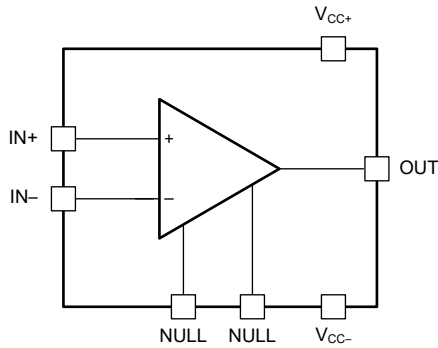


図 6-1. THS4021: Single Channel

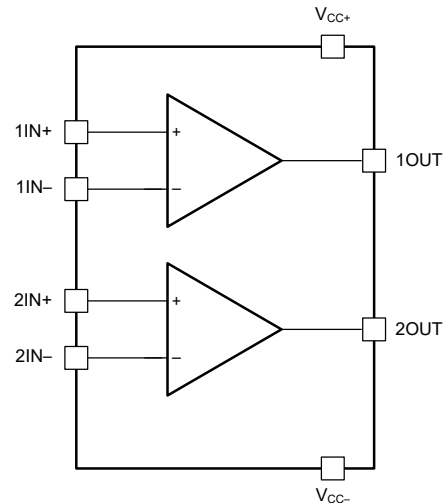
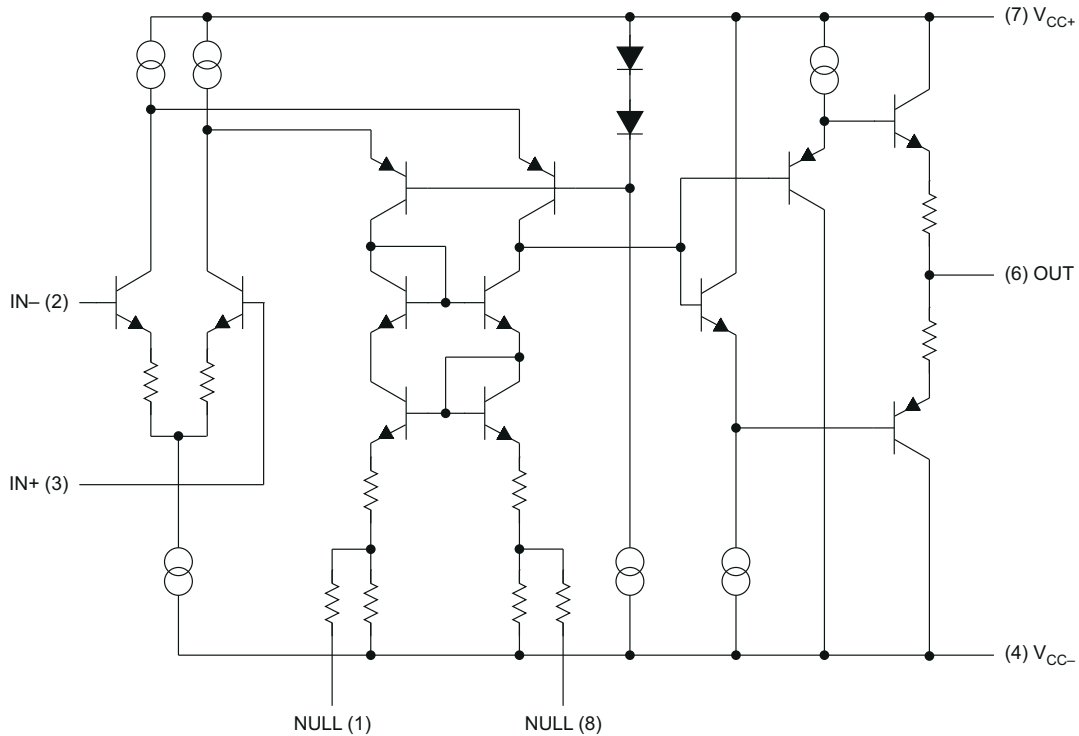


図 6-2. THS4022: Dual Channel



S0276-01

図 6-3. THS4021 Simplified Schematic

6.3 Feature Description

6.3.1 Offset Nulling

The THS402x have a very low input offset voltage for high-speed amplifiers. However, if additional correction is required, an offset nulling function has been provided on the THS4021. To adjust the input offset voltage, place a potentiometer between pin 1 and pin 8 of the device, and tie the wiper to the negative supply. [Figure 6-4](#) shows this feature.

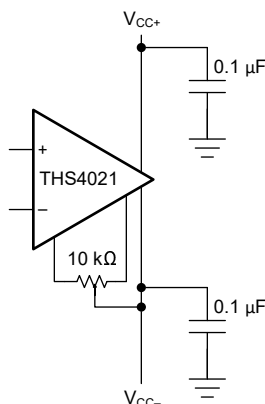


Figure 6-4. Offset Nulling Schematic

6.4 Device Functional Modes

The THS402x family has a single functional mode and can be used with both single-supply or split power-supply configurations. The power-supply voltage must be greater than 9 V (± 4.5 V) and less than 33 V (± 16.5 V).

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

7.1.1 Driving a Capacitive Load

The THS402x are internally compensated to maximize bandwidth and slew-rate performance. To maintain stability, take additional precautions when driving capacitive loads with a high-performance amplifier. As a result of the internal compensation, significant capacitive loading directly on the output node decreases the device phase margin, and potentially lead to high-frequency ringing or oscillations. Therefore, for capacitive loads greater than 10 pF, place an isolation resistor in series with the output of the amplifier. [図 7-1](#) shows this configuration. For most applications, a minimum resistance of 20 Ω is recommended. In 75- Ω transmission systems, setting the series resistor value to 75 Ω is a beneficial choice because this value isolates any capacitance loading and provides source impedance matching.

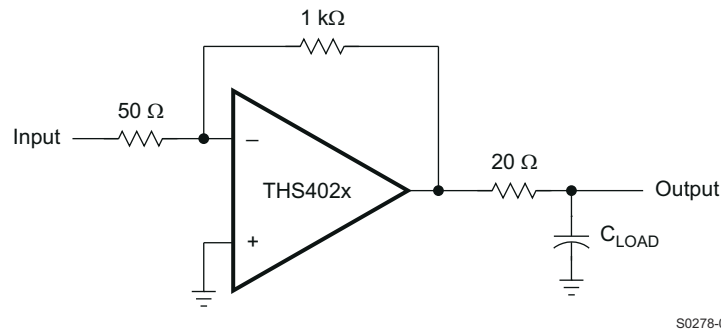


図 7-1. Driving a Capacitive Load

7.1.2 General Configuration

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. [図 7-2](#) shows how the simplest way to accomplish this limiting is to place an RC filter at the noninverting pin of the amplifier.

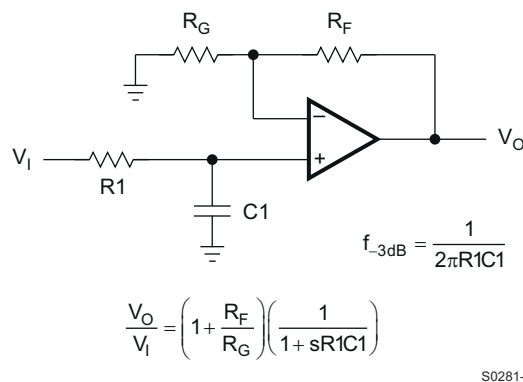


図 7-2. Single-Pole Low-Pass Filter

7.2 Power Supply Recommendations

The THS402x devices are designed to operate on power supplies ranging from ± 4.5 V to ± 16 V (single-ended supplies of 9 V to 32 V). Use a power-supply accuracy of 5% or better. When operated on a board with high-speed digital signals, make sure to provide isolation between digital signal noise and the analog input pins. The THS4021 and THS4022 are connected to the positive power supply (V_{CC+}) through pin 7 and pin 8, respectively. Both devices use pin 4 for the negative power supply (V_{CC-}). Decouple each supply pin to GND as close to the device as possible.

7.3 Layout

7.3.1 Layout Guidelines

To achieve the levels of high-frequency performance of the THS402x, follow proper printed-circuit board (PCB), high-frequency design techniques. The following is a general set of guidelines. In addition, a THS402x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- **Ground planes**—make sure that the ground plane used on the board provides all components with a low-inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize stray capacitance.
- **Proper power-supply decoupling**—use a 6.8- μ F tantalum capacitor in parallel with a 0.1- μ F ceramic capacitor on each supply pin. Sharing the tantalum capacitor among several amplifiers is possible depending on the application, but always use a 0.1- μ F ceramic capacitor on the supply pin of every amplifier. In addition, place the 0.1- μ F capacitor as close as possible to the supply pin. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. Strive for distances of less than 0.1 inch (2.54 mm) between the device power pins and the ceramic capacitors.
- **Short trace runs or compact part placements**—optimum high-frequency performance is achieved when stray series inductance has been minimized. To realize this, make the circuit layout as compact as possible, thereby minimizing the length of all trace runs. Pay particular attention to the inputs of the amplifier, keeping the trace lengths as short as possible. This layout helps to minimize stray capacitance at the input of the amplifier.

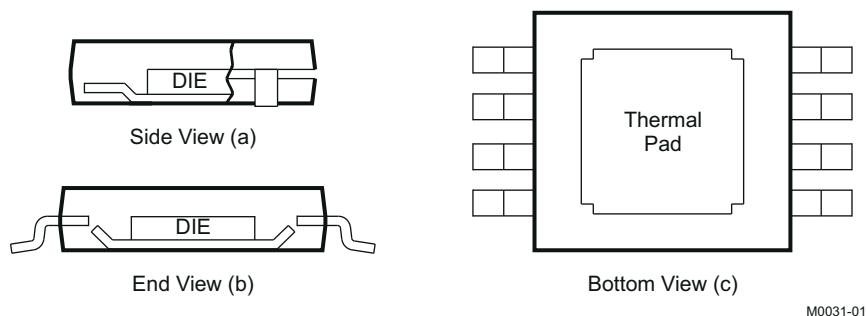
7.3.1.1 General PowerPAD™ Integrated Circuit Package Design Considerations

The THS402x is available in a thermally-enhanced DGN package, which is a member of the PowerPAD™ integrated circuit package family. [Figure 7-3 a](#) and [Figure 7-3 b](#) show that this package is constructed using a downset leadframe upon which the die is mounted. [Figure 7-3 c](#) that this arrangement results in the leadframe being exposed as a thermal pad on the underside of the package. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD integrated circuit package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD integrated circuit package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the previously awkward mechanical methods of heat sinking.

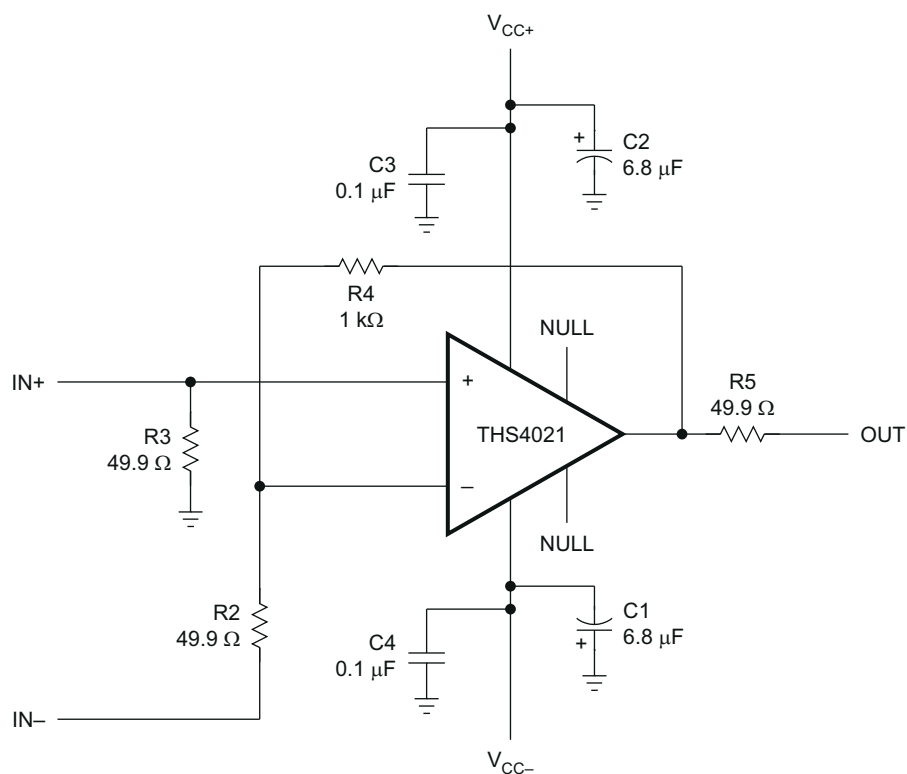
More complete details of the PowerPAD installation process and thermal management techniques are found in [PowerPAD Thermally-Enhanced Package](#). This document is found on the TI website (www.ti.com) by searching on the keyword PowerPAD. The document can also be ordered through your local TI sales office; refer to SLMA002 when ordering.



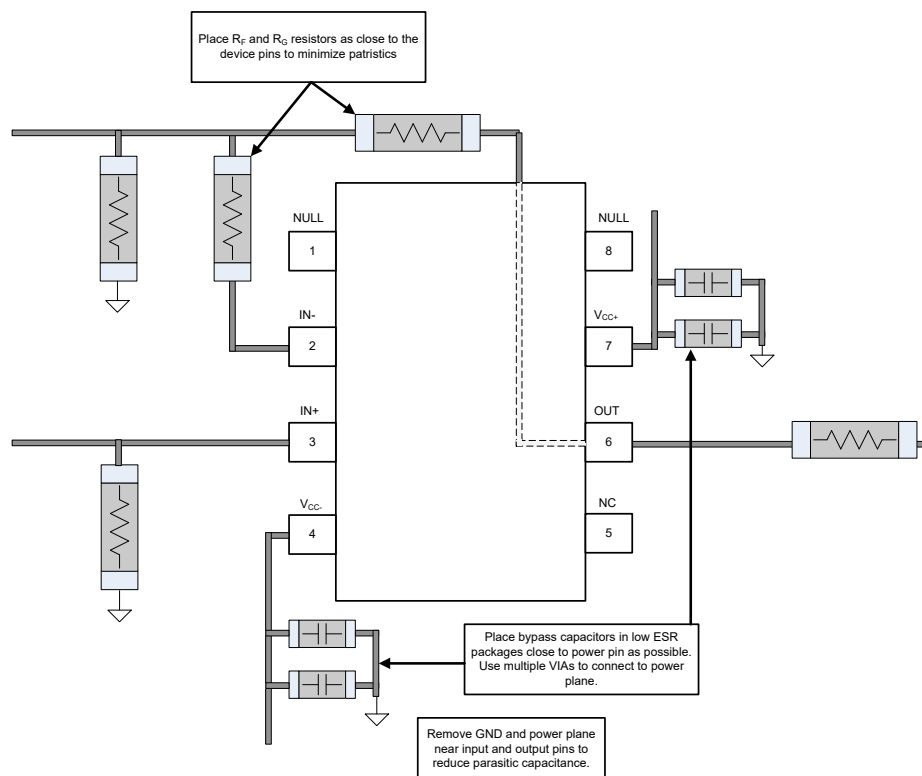
NOTE: The thermal pad (PowerPAD integrated circuit package) is electrically isolated from all other pins and can be connected to any potential from V_{CC-} to V_{CC+} . Typically, the thermal pad is connected to the ground plane because this plane tends to physically be the largest and is able to dissipate the most amount of heat.

Figure 7-3. Views of Thermally-enhanced DGN Package

7.3.2 Layout Example



S0282-01



7-4. Layout Recommendations

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Noise Analysis in Operational Amplifier Circuits](#) application report
- Texas Instruments, [PowerPAD Thermally Enhanced Package](#) application report
- Texas Instruments, [THS4021 High-Speed Operational Amplifier Evaluation Module](#) user's guide
- Texas Instruments, [THS4022 Dual High-Speed Operational Amplifier Evaluation Module](#) user's guide

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

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8.4 Trademarks

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8.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

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8.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (March 2024) to Revision F (July 2024)	Page
• Deleted Total harmonic distortion + noise and Intermodulation distortion specifications from <i>Electrical Characteristics: THS4021D and THS4022DGN</i>	6

Changes from Revision D (May 2023) to Revision E (March 2024)	Page
• ドキュメントから THS4022 D パッケージを削除.....	1
• 「アプリケーション概略図」の図を更新して正しいピン名を表示.....	1

• 「概要」の閉ループ帯域幅と電源電流を更新	1
• Updated <i>Thermal Information: THS4022</i>	5
• Changed title of <i>Electrical Characteristics: THS4021 (D Package)</i> to <i>Electrical Characteristics: THS4021D and THS4022DGN</i>	6
• Changed Channel-to-channel crosstalk from –60 dB to –54 dB in <i>Electrical Characteristics THS4021D and THS4022DGNB</i>	6
• Changed title of <i>Electrical Characteristics: THS4021 (DGN Package) and THS4022 (D and DGN Packages)</i> to <i>Electrical Characteristics: THS4021DGN</i>	8
• Changed title of <i>Typical Characteristics: THS4021 (D Package)</i> to <i>Typical Characteristics: THS4021D and THS4022DGN</i>	10
• Changed V_{CC} from ± 5 V to ± 15 V in <i>Typical Characteristics: THS4021D and THS4022DGN</i>	10
• Updated <i>Power-Supply Rejection Ratio vs Frequency</i> figure legend in <i>Typical Characteristics: THS4021D and THS4022DGN</i>	10
• Changed title of <i>Typical Characteristics: THS4021 (DGN Package) and THS4022 (D and DGN Packages)</i> to <i>Typical Characteristics: THS4021DGN</i>	16
• Updated <i>Crosstalk vs Frequency</i> figure and moved to <i>Typical Characteristics: THS4021D and THS4022DGN</i>	16

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS4021CD	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	0 to 70	4021C
THS4021CDGN	Active	Production	HVSSOP (DGN) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACK
THS4021CDGN.A	Active	Production	HVSSOP (DGN) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACK
THS4021CDGNR	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACK
THS4021CDGNR.A	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACK
THS4021IDGN	Active	Production	HVSSOP (DGN) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACL
THS4021IDGN.A	Active	Production	HVSSOP (DGN) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACL
THS4021IDGNR	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACL
THS4021IDGNR.A	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACL
THS4021IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4021I
THS4021IDR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4021I
THS4022CD	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	4022C
THS4022CD.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	4022C
THS4022CDGN	Obsolete	Production	HVSSOP (DGN) 8	-	-	Call TI	Call TI	0 to 70	ACA
THS4022CDGNR	Obsolete	Production	HVSSOP (DGN) 8	-	-	Call TI	Call TI	0 to 70	ACA
THS4022ID	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4022I
THS4022ID.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4022I
THS4022IDGN	Obsolete	Production	HVSSOP (DGN) 8	-	-	Call TI	Call TI	-40 to 85	ACB
THS4022IDGNR	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ACB
THS4022IDGNR.B	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ACB

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4021CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4021IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4021IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4022IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4021CDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4021IDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4021IDR	SOIC	D	8	2500	353.0	353.0	32.0
THS4022IDGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
THS4022CD	D	SOIC	8	75	505.46	6.76	3810	4
THS4022CD.A	D	SOIC	8	75	505.46	6.76	3810	4
THS4022ID	D	SOIC	8	75	505.46	6.76	3810	4
THS4022ID.A	D	SOIC	8	75	505.46	6.76	3810	4

GENERIC PACKAGE VIEW

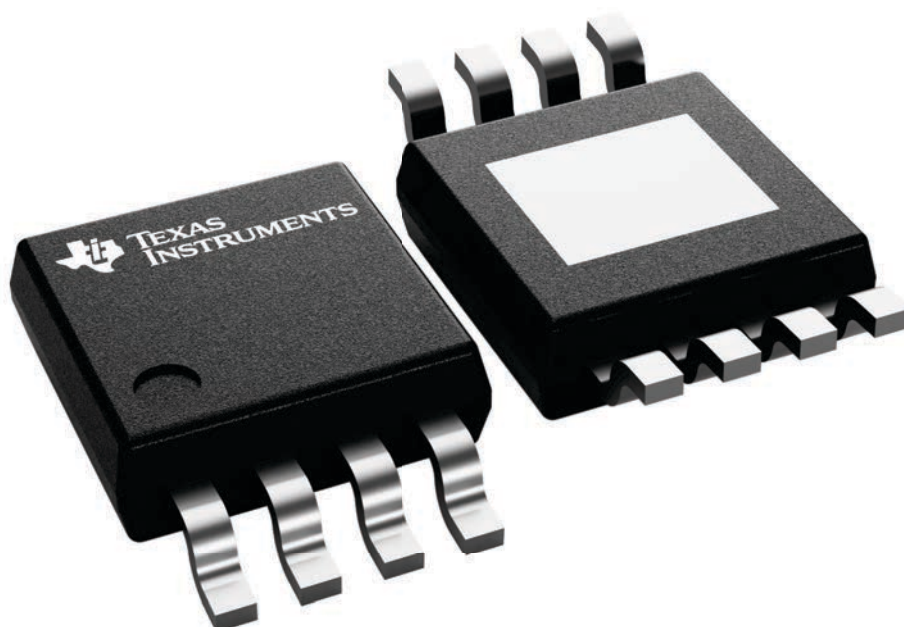
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

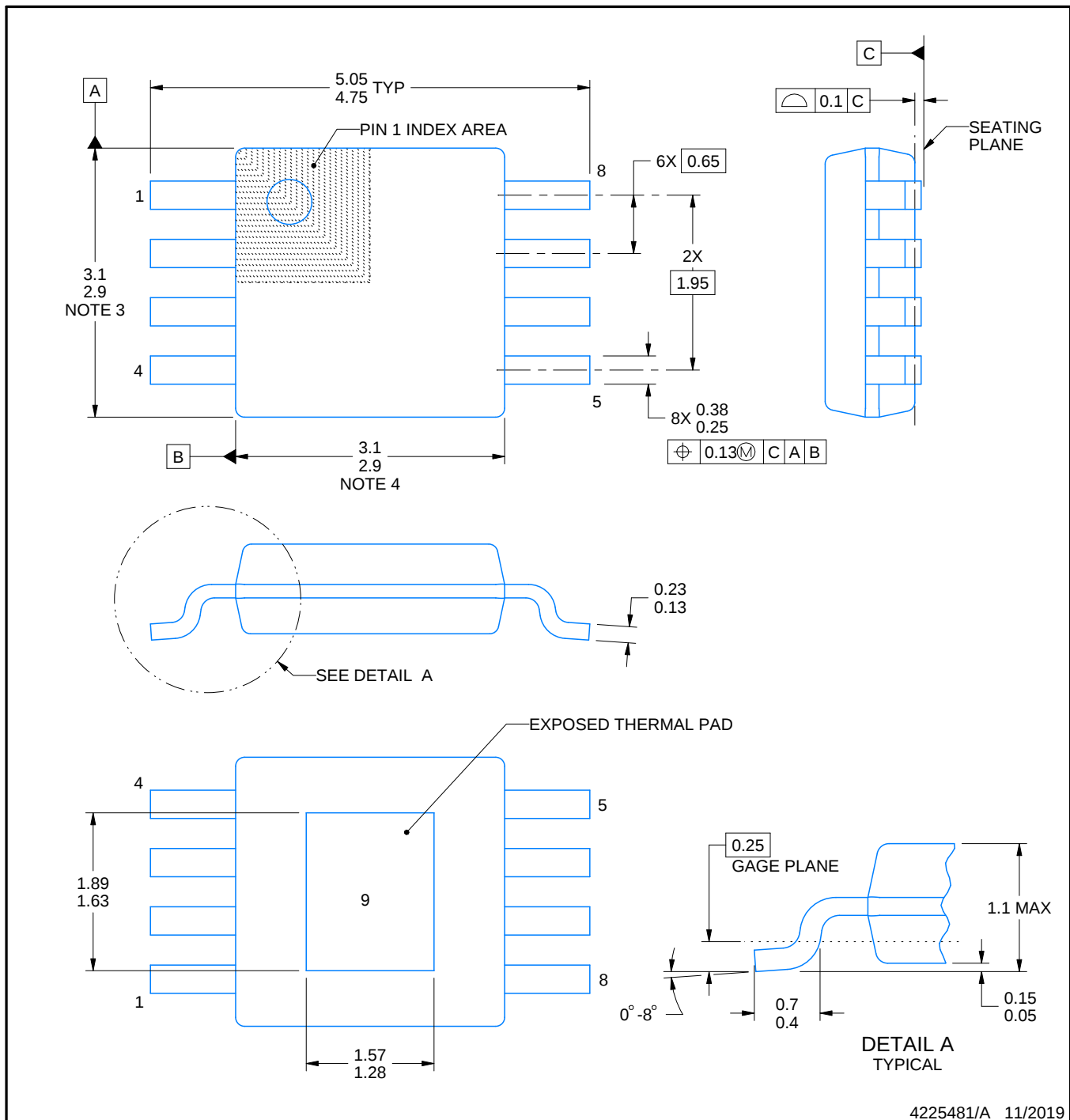
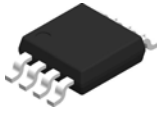
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B



4225481/A 11/2019

NOTES:

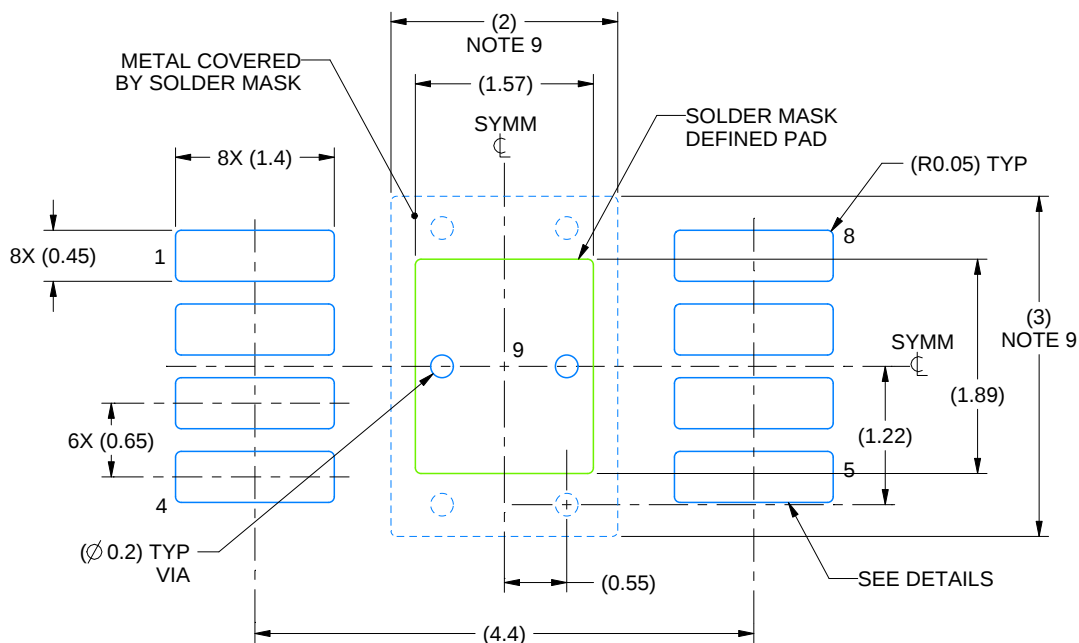
PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

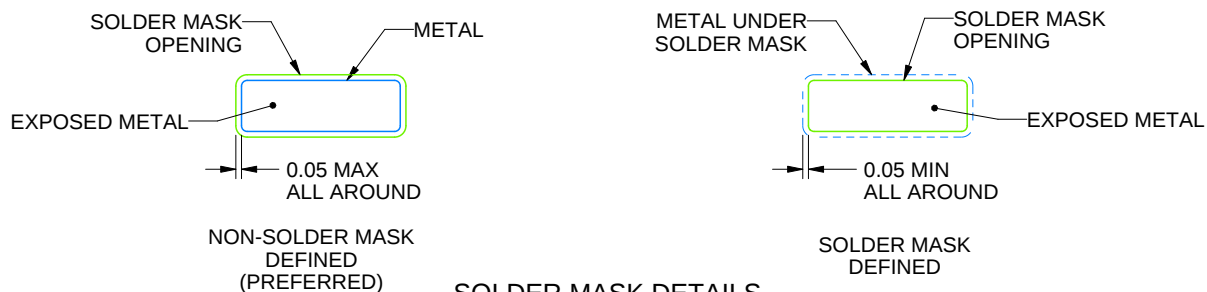
DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4225481/A 11/2019

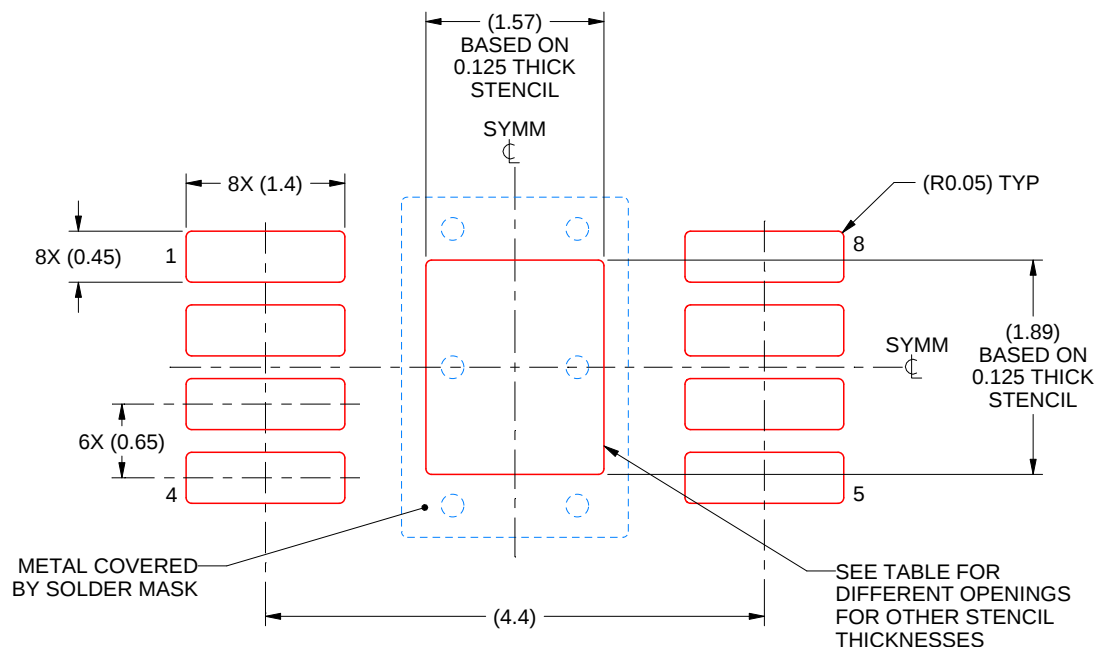
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE

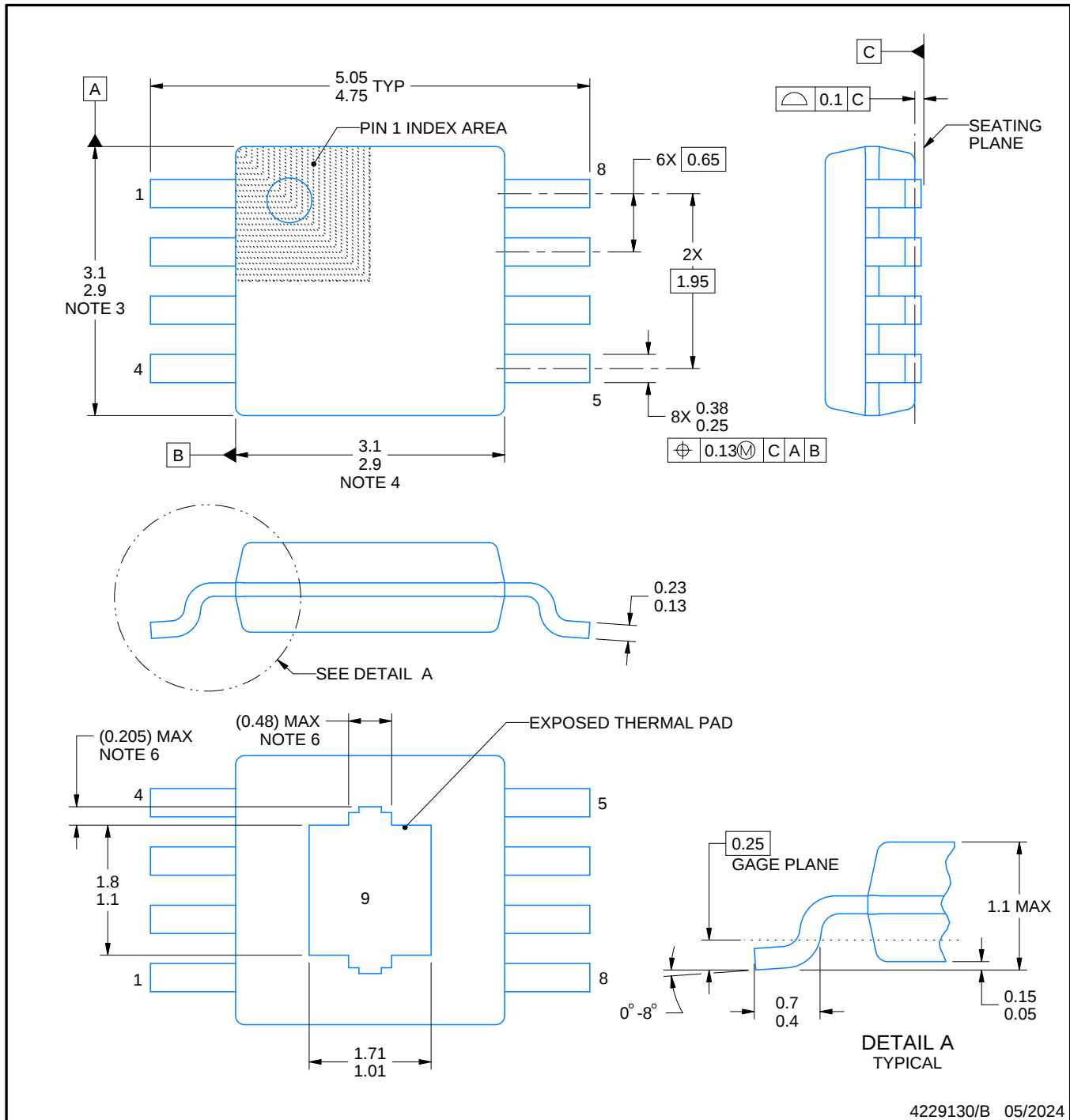
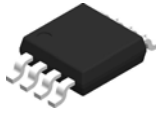
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.



4229130/B 05/2024

NOTES:

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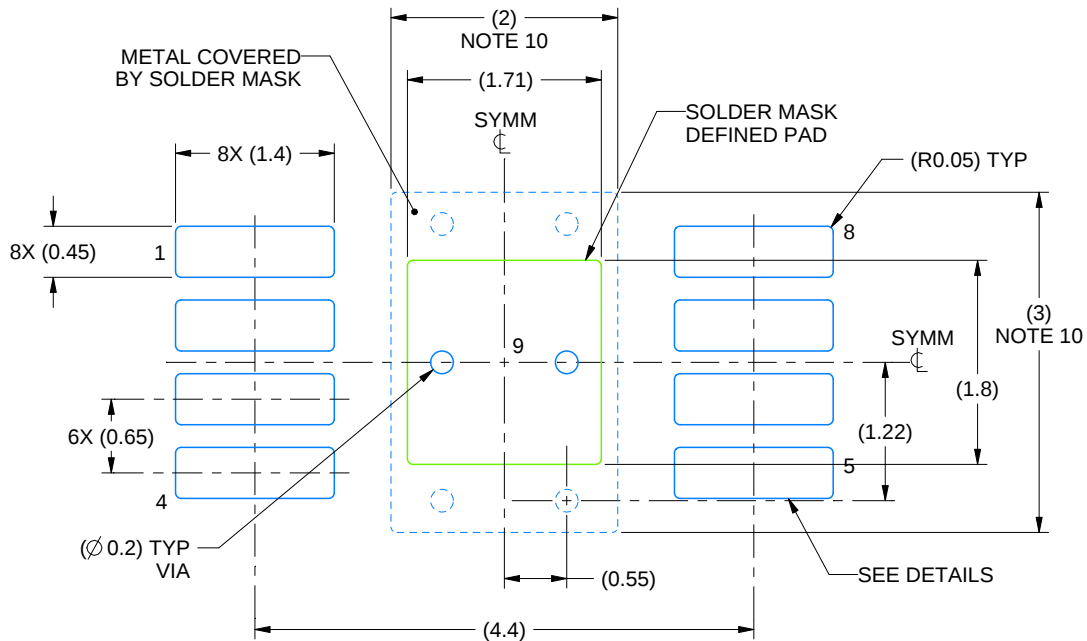
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

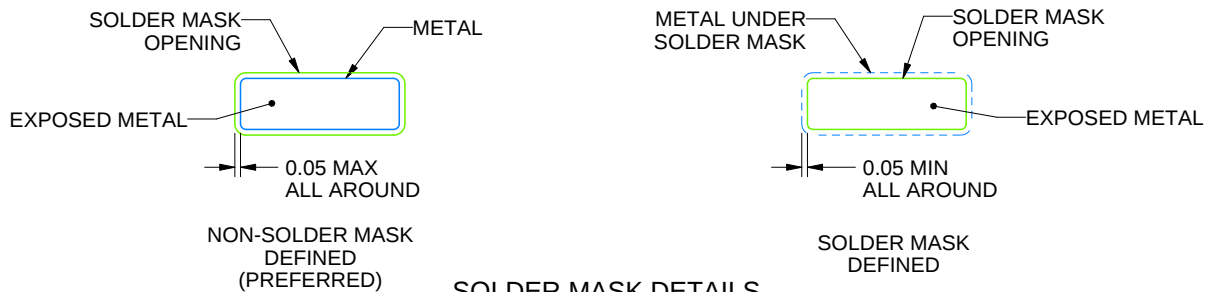
DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4229130/B 05/2024

NOTES: (continued)

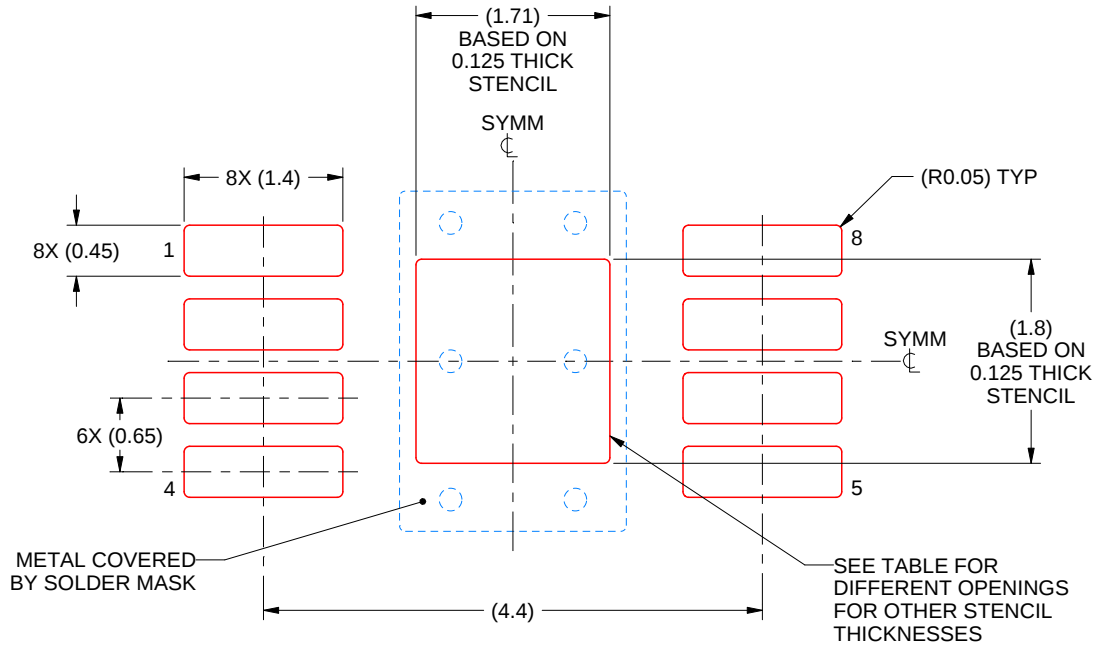
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.91 X 2.01
0.125	1.71 X 1.80 (SHOWN)
0.15	1.56 X 1.64
0.175	1.45 X 1.52

4229130/B 05/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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