THS4541-Q1 負レール入力、レール ツー レール出力、高精度、850MHz 完全差動アンプ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 1:-40℃～+125℃、T_A
- 帯域幅:500MHz (G = 2V/V)
- ゲイン帯域幅積:850MHz
- スルーレート:1500V/µs
- HD_2:–95dBc (10MHz、$2V_{PP}$、R_L = 500Ω)
- HD_3:–90dBc (10MHz、$2V_{PP}$、R_L = 500Ω)
- 入力電圧ノイズ: 2.2nV/√Hz (f > 100kHz)
- 小さいオフセットドリフト:±0.5µV/°C (標準値)
- 負のレール入力 (NRI)
- レール ツー レール出力 (RRO)
- 電源:
  - 単一電源電圧範囲:2.7V～5.4V
  - 両電源電圧範囲:±1.35V～±2.7V
  - 静止電流:10.1mA (5V 電源)
- パワーダウン機能:2 µA (標準値)

2 アプリケーション

- 機械式スキャン LIDAR
- 半導体 LIDAR
- 熱画像処理カメラ
- マイクロボロメータ カメラ
- タイム オブ フライト (ToF) カメラ

3 概要

THS4541-Q1 は、負のレールよりも低い入力同相範囲およびレール ツー レール出力を備えた、低消費電力、電圧フィードバック、全差動アンプ (FDA) です。高性能 A/D コンバータ (ADC) または D/A コンバータ (DAC) インターフェイス設計において、高密度化が重要な低消費電力データ アクイジション システム向けに設計されています。

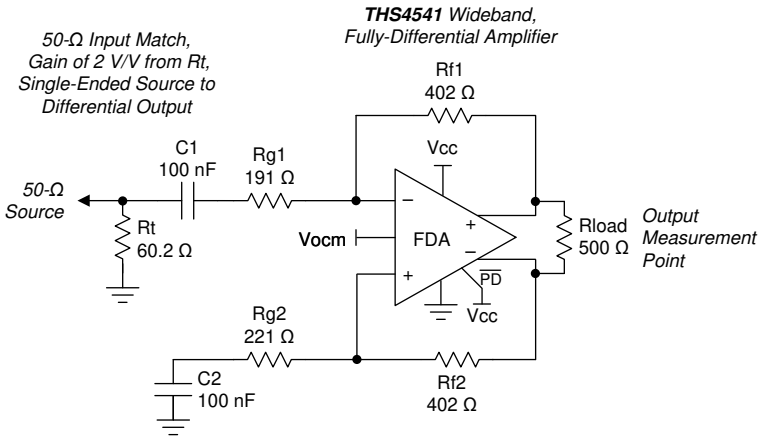
THS4541-Q1 は、DC 結合でグランド中心のソース信号のインターフェイスに必要とされる負のレール入力を備えています。この負のレール入力とレール ツー レール出力により、シングルエンド、グランド基準のバイポーラ信号源と、さまざまな逐次比較レジスタ (SAR)、デルタ シグマ (ΔΣ)、またはパイプライン ADC との間を 2.7V～5.4V の単一電源を使用して簡単に接続できます。

THS4541-Q1 は、–40℃～+125℃の広い温度範囲にわたって動作が規定されており、ウェッタブル フランク付き、およびウェッタブル フランクなしの両方について、16 ピン VQFN パッケージで供給されます。ウェッタブル フランク付きのパッケージは、組み立て後の目視検査が容易であり、THS4541W-Q1 として供給されます。

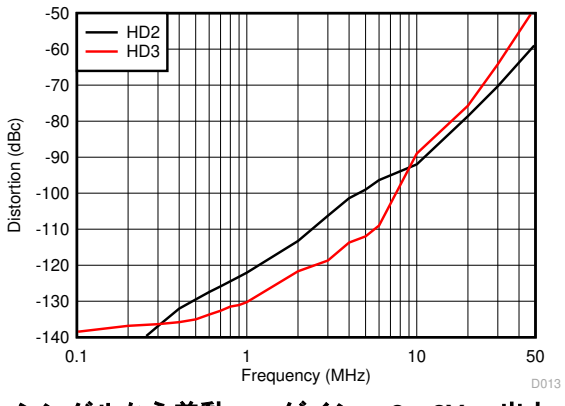
パッケージ情報

部品番号 (1)	パッケージ (2)	パッケージ サイズ (3)
THS4541-Q1	RGT (VQFN、16)	3mm × 3mm
THS4541W-Q1 (4)		

(1) セクション 4 を参照してください。
(2) 詳細については、セクション 12 を参照してください。
(3) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(4) ウェッタブル フランクのパッケージ オプション。



概略回路図



シングルから差動へ、ゲイン = 2、$2V_{PP}$ 出力

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4 Device Comparison Table

DEVICE	BW (MHz)	I_Q (mA)	THD (dBc) 2 V_{PP} AT 100 kHz	INPUT NOISE (nV/√Hz)	RAIL-TO-RAIL
THS4531A	36	0.25	–104	10	Out
THS4521	145	0.95	–102	4.6	Out
THS4520	620	14.2	–107	2	Out

5 Pin Configuration and Functions

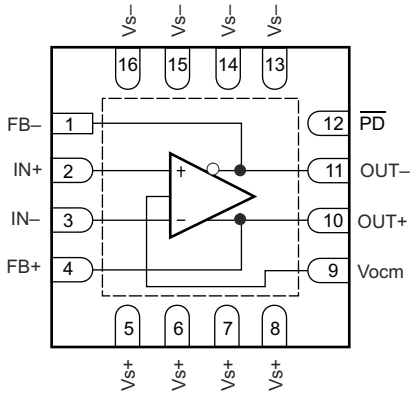


図 5-1. RGT Package, 16-Pin VQFN With Exposed Thermal Pad, (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.(1)		
FB+	4	Output	Noninverted (positive) output feedback
FB–	1	Output	Inverted (negative) output feedback
IN+	2	Input	Noninverting (positive) amplifier input
IN–	3	Input	Inverting (negative) amplifier input
NC	—	—	No internal connection
OUT+	10	Output	Noninverted (positive) amplifier output
OUT–	11	Output	Inverted (negative) amplifier output
$\overline{PD}$	12	Input	Power down. $\overline{PD}$ = logic low = power off mode; $\overline{PD}$ = logic high = normal operation.
Vocm	9	Input	Common-mode voltage input
Vs+	5–8	Input	Positive power-supply input
Vs–	13–16	Input	Negative power-supply input

(1) Solder the exposed thermal pad to a heat-spreading power or ground plane. This pad is electrically isolated from the die, but must be connected to a power or ground plane and not floated.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage, (Vs+) – Vs–		5.5	V
	Input/output voltage range	(Vs–) – 0.5	(Vs+) + 0.5	
	Differential input voltage		±1	
Current	Continuous input current		±20	mA
	Continuous output current		±80	
	Continuous power dissipation	See セクション 6.4 and セクション 7.8		
Temperature	Maximum junction		150	°C
	Operating free-air	–40	125	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Vs+	Single-supply voltage	2.7	5	5.4	V
T_A	Ambient temperature	–40	25	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		THS4541-Q1 RGT (VQFN) 16 PINS	THS4541W-Q1 RGT (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52	56.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69	69	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25	30.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.7	3.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25	30.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.3	14.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics: (Vs+) – Vs– = 5 V

at T_A ≈ 25°C, Vocm = open (defaults midsupply), Vout = 2 V_{PP}, Rf = 402 Ω, Rload = 499 Ω, 50-Ω input match, G = 2 V/V, single-ended input, differential output, and $\overline{PD}$ = +Vs (unless otherwise noted); see 図 7-1 for an ac-coupled gain of a 2-V/V test circuit, and 図 7-3 for a dc-coupled gain of a 2-V/V test circuit

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE							
	Small-signal bandwidth	Vout = 100 mV_{PP}, G = 1		620		MHz	C
		Vout = 100 mV_{PP}, G = 2 (see 図 7-1)		500			C
		Vout = 100 mV_{PP}, G = 5		210			C
		Vout = 100 mV_{PP}, G = 10		125			C
	Gain-bandwidth product	Vout = 100 mV_{PP}, G = 20		850		MHz	C
	Large-signal bandwidth	Vout = 2 V_{PP}, G = 2 (see 図 7-1)		340		MHz	C
	Bandwidth for 0.1-dB flatness	Vout = 2 V_{PP}, G = 2 (see 図 7-1)		100		MHz	C
	Slew rate(2)	Vout = 2-V_{PP}, FPBW (see 図 7-1)		1500		V/µs	C
	Rise/fall time	Vout = 2-V step, G = 2 input ≤ 0.3 ns t_r (see 図 7-3)		1.4		ns	C
	Settling time	To 1%, Vout = 2-V step, t_r = 2 ns, G = 2 (see 図 7-3)		4		ns	C
		To 0.1%,Vout = 2-V step, t_r = 2 ns, G = 2 (see 図 7-3)		8			C
	Overshoot and undershoot	Vout = 2-V step G = 2, input ≤ 0.3 ns t_r (see 図 7-3)		10%			C
	100-kHz harmonic distortion	Vout = 2 V_{PP}, G = 2, HD2 (see 図 7-1)		–140		dBc	C
		Vout = 2 V_{PP}, G = 2, HD3 (see 図 7-1)		–140			C
	10-MHz harmonic distortion	Vout = 2 V_{PP}, G = 2, HD2 (see 図 7-1)		–95		dBc	C
		Vout = 2 V_{PP}, G = 2, HD3 (see 図 7-1)		–90			C
	2nd-order intermodulation distortion	f = 10 MHz, 100-kHz tone spacing, Vout envelope = 2 V_{PP} (1 V_{PP} per tone) (see 図 7-1)		–90		dBc	C
	3rd-order intermodulation distortion	f = 10 MHz, 100-kHz tone spacing, Vout envelope = 2 V_{PP} (1 V_{PP} per tone) (see 図 7-1)		–85		dBc	C
	Input voltage noise	f > 100 kHz		2.2		nV/√Hz	C
	Input current noise	f > 1 MHz		1.9		pA/√Hz	C
	Overdrive recovery time	2 × output overdrive, either polarity		20		ns	C
	Closed-loop output impedance	f = 10 MHz (differential)		0.1		Ω	C

6.5 Electrical Characteristics: (Vs+) – Vs– = 5 V (続き)

at T_A ≈ 25°C, Vocm = open (defaults midsupply), Vout = 2 V_{PP}, Rf = 402 Ω, Rload = 499 Ω, 50-Ω input match, G = 2 V/V, single-ended input, differential output, and $\overline{PD}$ = +Vs (unless otherwise noted); see 図 7-1 for an ac-coupled gain of a 2-V/V test circuit, and 図 7-3 for a dc-coupled gain of a 2-V/V test circuit

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
DC PERFORMANCE								
A_{OL}	Open-loop voltage gain			100	119		dB	A
	Input-referred offset voltage	T_A = 25°C		–450	±100	450	μV	A
		T_A = 0°C to 70°C		–600	±100	600		B
		T_A = –40°C to +85°C		–700	±100	700		B
		T_A = –40°C to +125°C		–850	±100	850		B
	Input offset voltage drift(3)	T_A = –40°C to +125°C		–2.4	±0.5	2.4	μV/°C	B
	Input bias current (positive out of node)	T_A = 25°C			10	13	μA	A
		T_A = 0°C to 70°C			11	13.5		B
		T_A = –40°C to +85°C			12	14		B
		T_A = –40°C to +125°C			12	14.5		B
	Input bias current drift(3)	T_A = –40°C to +125°C			6	15	nA/°C	B
	Input offset current	T_A = 25°C		–500	±150	500	nA	A
		T_A = 0°C to 70°C		–550	±150	550		B
		T_A = –40°C to +85°C		–580	±150	580		B
		T_A = –40°C to +125°C		–620	±150	620		B
	Input offset current drift(3)	T_A = –40°C to +125°C		–1.3	±0.3	1.3	nA/°C	B
INPUT								
	Common-mode input low	< 3-dB degradation in CMRR from midsupply	T_A = 25°C		(Vs–) – 0.2	(Vs–) – 0.1	V	A
			T_A = –40°C to +125°C		(Vs–) – 0.1	Vs–		B
	Common-mode input high	< 3-dB degradation in CMRR from midsupply	T_A = 25°C	(Vs+) – 1.3	(Vs+) –1.2		V	A
			T_A = –40°C to +125°C	(Vs+) – 1.3				B
	Common-mode rejection ratio	Input pins at ((Vs+) – Vs–) / 2		85	100		dB	A
	Input impedance differential mode	Input pins at ((Vs+) – Vs–) / 2			110 || 0.85		kΩ || pF	C
OUTPUT								
	Output voltage low	T_A = 25°C			(Vs–) + 0.2	(Vs–) + 0.25	V	A
		T_A = –40°C to +125°C			(Vs–) + 0.2	(Vs–) + 0.25		B
	Output voltage high	T_A = 25°C		(Vs+) – 0.25	(Vs+) – 0.2		V	A
		T_A = –40°C to +125°C		(Vs+) – 0.25	(Vs+) – 0.2			B
	Output current drive	T_A = 25°C		±75	±100		mA	A
		T_A = –40°C to +125°C		±75				B

6.5 Electrical Characteristics: (Vs+) – Vs– = 5 V (続き)

at T_A ≈ 25°C, Vocm = open (defaults midsupply), Vout = 2 V_{PP}, Rf = 402 Ω, Rload = 499 Ω, 50-Ω input match, G = 2 V/V, single-ended input, differential output, and $\overline{PD}$ = +Vs (unless otherwise noted); see 図 7-1 for an ac-coupled gain of a 2-V/V test circuit, and 図 7-3 for a dc-coupled gain of a 2-V/V test circuit

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
POWER SUPPLY								
	Specified operating voltage			2.7	5	5.4	V	B
	Quiescent operating current	T_A = 25°C, Vs+ = 5 V		9.7	10.1	10.5	mA	A
		T_A = –40°C to +125°C		9.4	10.1	11		B
±PSRR	Power-supply rejection ratio	Either supply pin to differential Vout		85	100		dB	A
POWER DOWN								
	Enable voltage threshold			(Vs–) + 1.7			V	A
	Disable voltage threshold					(Vs–) + 0.7	V	A
	Disable pin bias current	$\overline{PD}$ = Vs– → Vs+			20	50	nA	B
	Power-down quiescent current	$\overline{PD}$ = (Vs–) + 0.7 V			6	30	µA	A
		$\overline{PD}$ = Vs–			2	8		A
	Turn-on time delay	Time from $\overline{PD}$ = low to Vout = 90% of final value			100		ns	C
	Turn-off time delay	Time from $\overline{PD}$ = low to Vout = 10% of final value			60		ns	C
OUTPUT COMMON-MODE VOLTAGE CONTROL(4)								
	Small-signal bandwidth	Vocm = 100 mV_{PP}			150		MHz	C
	Slew rate(2)	Vocm = 2-V step			400		V/µs	C
	Gain			0.975	0.982	0.995	V/V	A
	Input bias current	Considered positive out of node		–0.7	0.1	0.7	µA	A
	Input impedance	Vocm input driven to ((Vs+) – Vs–) / 2			47 || 1.2		kΩ || pF	C
	Default voltage offset from ((Vs+) – Vs–) / 2	Vocm pin open		–40	±8	40	mV	A
CM Vos	Common-mode offset voltage	Vocm input driven to ((Vs+) – Vs–) / 2	T_A = 25°C	–5	±2	5	mV	A
			T_A = 0°C to 70°C	–6	±2	5.8		B
			T_A = –40°C to +85°C	–6.2	±2	6.2		B
			T_A = –40°C to +125°C	–7	±2	7.08		B
	Common-mode offset voltage drift(3)	Vocm input driven to ((Vs+) – Vs–) / 2		–20	±4	+20	µV/°C	B
	Common-mode loop supply headroom to negative supply	< ±12-mV shift from midsupply CM Vos	T_A = 25°C	0.88			V	A
			T_A = 0°C to 70°C	0.91				B
			T_A = –40°C to +85°C	0.94				B
			T_A = –40°C to +125°C	0.94				B
	Common-mode loop supply headroom to positive supply	< ±12-mV shift from midsupply CM Vos	T_A = 25°C	1.1			V	A
			T_A = 0°C to 70°C	1.15				B
			T_A = –40°C to +85°C	1.2				B
			T_A = –40°C to +125°C	1.2				B

(1) Test levels (all values set by characterization and simulation): (A) 100% tested at T_A ≈ 25°C; over temperature limits by characterization and simulation. (B) Not tested in production; limits set by characterization and simulation. (C) Typical value only for information.
(2) This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: (V_P / √2) × 2π × f_{-3dB}.
(3) Input offset voltage drift, input bias current drift, input offset current drift, and Vocm drift are average values calculated by taking data at the at the maximum-range ambient-temperature end points, computing the difference, and dividing by the temperature range. Maximum drift set by distribution of a large sampling of devices. Drift is not specified by test or QA sample test.
(4) Specifications are from the input Vocm pin to the differential output average voltage.

6.6 Electrical Characteristics: (Vs+) – Vs– = 3 V

at T_A ≈ 25°C, Vocm = open (defaults midsupply), Vout = 2 V_{PP}, Rf = 402 Ω, Rload = 499 Ω, 50-Ω input match, G = 2 V/V, single-ended input, differential output, and $\overline{PD}$ = +Vs (unless otherwise noted); see 図 7-1 for an ac-coupled gain of a 2-V/V test circuit, and 図 7-3 for a dc-coupled gain of a 2-V/V test circuit

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE							
	Small-signal bandwidth	Vout = 100 mV_{PP}, G = 1		600		MHz	C
		Vout = 100 mV_{PP}, G = 2 (see 図 7-1)		500			C
		Vout = 100 mV_{PP}, G = 5		200			C
		Vout = 100 mV_{PP}, G = 10		120			C
	Gain-bandwidth product	Vout = 100 mV_{PP}, G = 20		850		MHz	C
	Large-signal bandwidth	Vout = 2 V_{PP}, G = 2 (see 図 7-1)		300		MHz	C
	Bandwidth for 0.1-dB flatness	Vout = 2 V_{PP}, G = 2 (see 図 7-1)		90		MHz	C
	Slew rate(2)	Vout = 2-V step, FPBW (see 図 7-1)		1300		V/µs	C
	Rise/fall time	Vout = 2-V step, G = 2, input ≤ 0.3 ns t_r (see 図 7-3)		1.8		ns	C
	Settling time	To 1%, Vout = 2-V step, t_r = 2 ns, G = 2 (see 図 7-3)		5		ns	C
		To 0.1%, Vout = 2-V step, t_r = 2 ns, G = 2 (see 図 7-3)		8			C
	Overshoot and undershoot	Vout = 2-V step G = 2, input ≤ 0.3 ns t_r (see 図 7-3)		10%			C
	100-kHz harmonic distortion	Vout = 2 V_{PP}, G = 2, HD2 (see 図 7-1)		–140		dBc	C
		Vout = 2 V_{PP}, G = 2, HD3 (see 図 7-1)		–140			C
	10-MHz harmonic distortion	Vout = 2 V_{PP}, G = 2, HD2 (see 図 7-1)		–92		dBc	C
		Vout = 2 V_{PP}, G = 2, HD3 (see 図 7-1)		–89			C
	2nd-order intermodulation distortion	f = 10 MHz, 100-kHz tone spacing, Vout envelope = 2 V_{PP} (1 V_{PP} per tone) (see 図 7-1)		–89		dBc	C
	3rd-order intermodulation distortion	f = 10 MHz, 100-kHz tone spacing, Vout envelope = 2 V_{PP} (1 V_{PP} per tone) (see 図 7-1)		–87		dBc	C
	Input voltage noise	f > 100 kHz		2.2		nV/√Hz	C
	Input current noise	f > 1 MHz		1.9		pA/√Hz	C
	Overdrive recovery time	2X output overdrive, either polarity		20		ns	C
	Closed-loop output impedance	f = 10 MHz (differential)		0.1		Ω	C

6.6 Electrical Characteristics: (Vs+) – Vs– = 3 V (続き)

at T_A ≈ 25°C, Vocm = open (defaults midsupply), Vout = 2 V_{PP}, Rf = 402 Ω, Rload = 499 Ω, 50-Ω input match, G = 2 V/V, single-ended input, differential output, and $\overline{PD}$ = +Vs (unless otherwise noted); see 図 7-1 for an ac-coupled gain of a 2-V/V test circuit, and 図 7-3 for a dc-coupled gain of a 2-V/V test circuit

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
DC PERFORMANCE								
A_{OL}	Open-loop voltage gain			100	119		dB	A
	Input-referred offset voltage	T_A = 25°C		–450	±100	400	μV	A
		T_A = 0°C to 70°C		–600	±100	600		B
		T_A = –40°C to +85°C		–700	±100	700		B
		T_A = –40°C to +125°C		–850	±100	850		B
	Input offset voltage drift(3)	T_A = –40°C to +125°C		–2.4	±0.5	2.4	μV/°C	B
	Input bias current (positive out of node)	T_A = 25°C			9	12	μA	A
		T_A = 0°C to 70°C			9	12.5		B
		T_A = –40°C to +85°C			9	13		B
		T_A = –40°C to +125°C			9	13.5		B
	Input bias current drift(3)	T_A = –40°C to +125°C			–5	15	nA/°C	B
	Input offset current	T_A = 25°C		–500	±150	500	nA	A
		T_A = 0°C to 70°C		–550	±150	550		B
		T_A = –40°C to +85°C		–580	±150	580		B
		T_A = –40°C to +125°C		–620	±150	620		B
	Input offset current drift(3)	T_A = –40°C to +125°C		–1.3	±0.3	1.3	nA/°C	B
INPUT								
	Common-mode input low	< 3-dB degradation in CMRR from midsupply	T_A = 25°C		(Vs–) – 0.2	(Vs–) – 0.1	V	A
			T_A = –40°C to +125°C		(Vs–) – 0.1	Vs–		B
	Common-mode input high	< 3-dB degradation in CMRR from midsupply	T_A = 25°C	(Vs+) – 1.3	(Vs+) –1.2		V	A
			T_A = –40°C to +125°C	(Vs+) – 1.3				B
	Common-mode rejection ratio	Input pins at ((Vs+) – Vs–) / 2		85	100		dB	A
	Input impedance differential mode	Input pins at ((Vs+) – Vs–) / 2			110 || 0.85		kΩ || pF	C
OUTPUT								
	Output voltage low	T_A = 25°C			(Vs–) + 0.2	(Vs–) + 0.25	V	A
		T_A = –40°C to +125°C			(Vs–) + 0.2	(Vs–) + 0.25		B
	Output voltage high	T_A = 25°C		(Vs+) – 0.25	(Vs+) – 0.2		V	A
		T_A = –40°C to +125°C		(Vs+) – 0.25	(Vs+) – 0.2			B
	Output current drive	T_A = 25°C		±55	±60		mA	A
		T_A = –40°C to +125°C		±55				B

6.6 Electrical Characteristics: (Vs+) – Vs– = 3 V (続き)

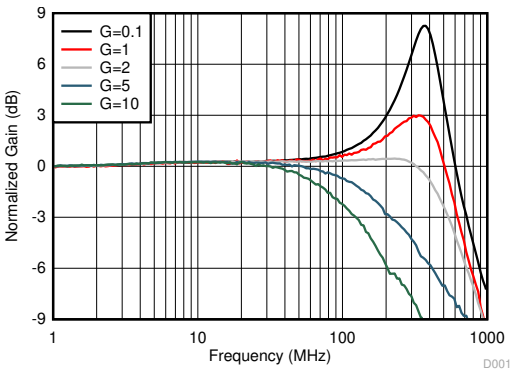
at T_A ≈ 25°C, Vocm = open (defaults midsupply), Vout = 2 V_{PP}, Rf = 402 Ω, Rload = 499 Ω, 50-Ω input match, G = 2 V/V, single-ended input, differential output, and $\overline{PD}$ = +Vs (unless otherwise noted); see 図 7-1 for an ac-coupled gain of a 2-V/V test circuit, and 図 7-3 for a dc-coupled gain of a 2-V/V test circuit

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
POWER SUPPLY								
	Specified operating voltage			2.7	3	5.4	V	B
	Quiescent operating current	T_A = 25°C, Vs+ = 3 V		9.3	9.7	10.1	mA	A
		T_A = –40°C to +125°C		9	9.7	10.6		B
±PSRR	Power-supply rejection ratio	Either supply pin to differential Vout		85	100		dB	A
POWER DOWN								
	Enable voltage threshold			(Vs–) + 1.7			V	A
	Disable voltage threshold					(Vs–) + 0.7	V	A
	Disable pin bias current	$\overline{PD}$ = Vs– → Vs+			20	50	nA	B
	Power-down quiescent current	$\overline{PD}$ = (Vs–) + 0.7 V			2	30	µA	A
		$\overline{PD}$ = Vs–			1.0	8.0		A
	Turn-on time delay	Time from $\overline{PD}$ = low to Vout = 90% of final value			100		ns	C
	Turn-off time delay	Time from $\overline{PD}$ = low to Vout = 10% of final value			60		ns	C
OUTPUT COMMON-MODE VOLTAGE CONTROL(4)								
	Small-signal bandwidth	Vocm = 100 mV_{PP}			140		MHz	C
	Slew rate(2)	Vocm = 1-V step			350		V/µs	C
	Gain			0.975	0.987	0.990	V/V	A
	Input bias current	Considered positive out of node		–0.7	0.1	0.7	µA	A
	Input impedance	Vocm input driven to ((Vs+) – Vs–) / 2			47 || 1.2		kΩ || pF	C
	Default voltage offset from ((Vs+) – Vs–) / 2	Vocm pin open		–40	±10	40	mV	A
CM Vos	Common-mode offset voltage	Vocm input driven to ((Vs+) – Vs–) / 2	T_A = 25°C	–5	±2	5	mV	A
			T_A = 0°C to 70°C	–5.8	±2	5.8		B
			T_A = –40°C to +85°C	–6.2	±2	6.2		B
			T_A = –40°C to +125°C	–7	±2	7		B
	Common-mode offset voltage drift(3)	Vocm input driven to ((Vs+) – Vs–) / 2		–20	±4	20	µV/°C	B
	Common-mode loop supply headroom to negative supply	< ±12-mV shift from midsupply CM Vos	T_A = 25°C	0.88			V	A
			T_A = 0°C to 70°C	0.91				B
			T_A = –40°C to +85°C	0.94				B
			T_A = –40°C to +125°C	0.94				B
	Common-mode loop supply headroom to positive supply	< ±12-mV shift from midsupply CM Vos	T_A = 25°C	1.1			V	A
			T_A = 0°C to 70°C	1.15				B
			T_A = –40°C to +85°C	1.2				B
			T_A = –40°C to +125°C	1.2				B

(1) Test levels (all values set by characterization and simulation): (A) 100% tested at T_A ≈ 25°C; over temperature limits by characterization and simulation. (B) Not tested in production; limits set by characterization and simulation. (C) Typical value only for information.
(2) This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: (V_P / √2) × 2π × f_{-3dB}.
(3) Input offset voltage drift, input bias current drift, input offset current drift, and Vocm drift are average values calculated by taking data at the at the maximum-range ambient-temperature end points, computing the difference, and dividing by the temperature range. Maximum drift set by distribution of a large sampling of devices. Drift is not specified by test or QA sample test.
(4) Specifications are from input Vocm pin to differential output average voltage.

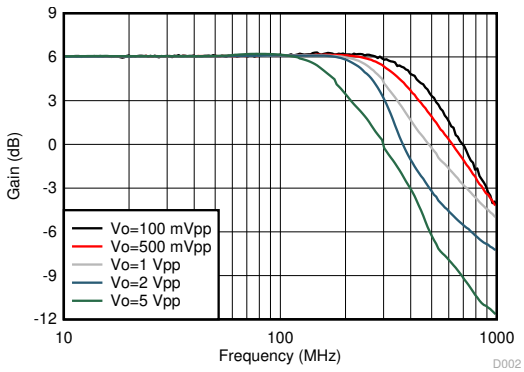
6.7 Typical Characteristics: 5-V Single Supply

at Vs+ = 5 V, Vs– = GND, Vocm is open, 50-Ω single-ended input to differential output, gain = 2 V/V, Rload = 500 Ω, and T_A ≈ 25°C (unless otherwise noted)



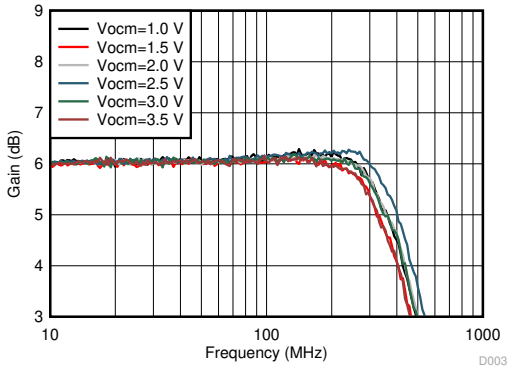
Rf = 402 Ω, see 図 7-1 and 表 8-1 for resistor values

図 6-1. Small-Signal Frequency Response vs Gain



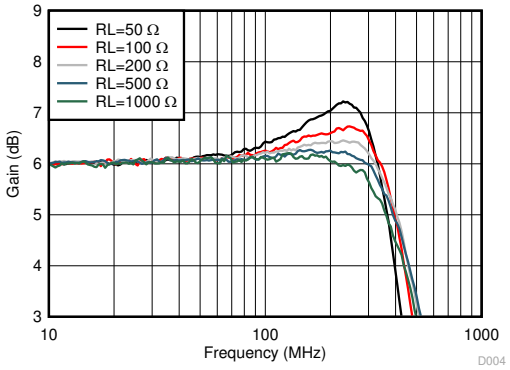
See 図 7-1

図 6-2. Frequency Response vs Vopp



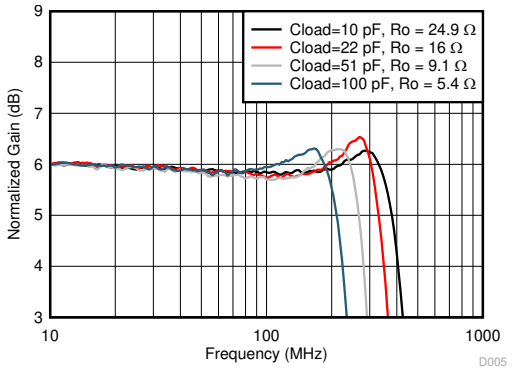
Vout = 100 mV_{PP}, see 図 7-1 with Vocm adjusted

図 6-3. Small-Signal Frequency Response vs Vocm



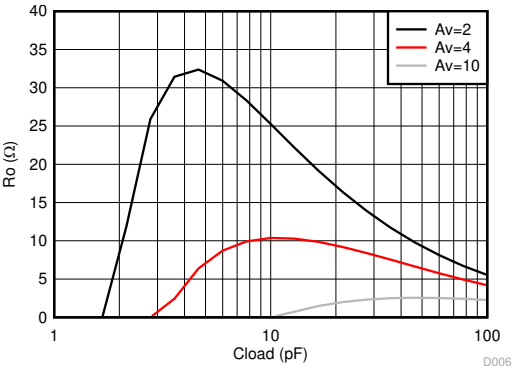
Vout = 100 mV_{PP}, see 図 7-1 with RL adjusted

図 6-4. Small-Signal Frequency Response vs Rload (RL)



100 mV_{PP} at load, Av = 2 (see 図 7-11), two series Ro added at output before Cload

図 6-5. Small-Signal Frequency Response vs Cload

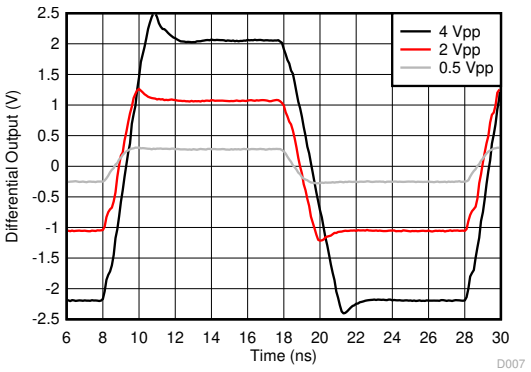


Ro is two series output resistors to a differential Cload in parallel with 500 Ω, see 図 7-11 and 表 8-1

図 6-6. Recommended Ro vs Cload

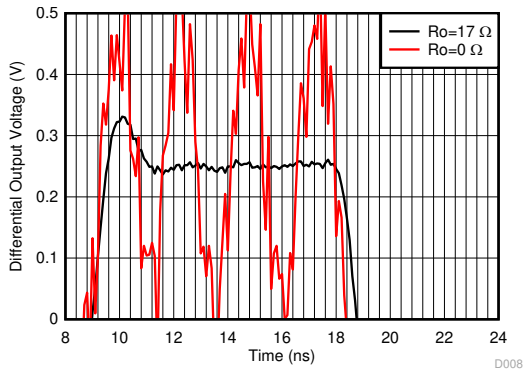
6.7 Typical Characteristics: 5-V Single Supply (continued)

at Vs+ = 5 V, Vs– = GND, Vocm is open, 50-Ω single-ended input to differential output, gain = 2 V/V, Rload = 500 Ω, and T_A ≈ 25°C (unless otherwise noted)



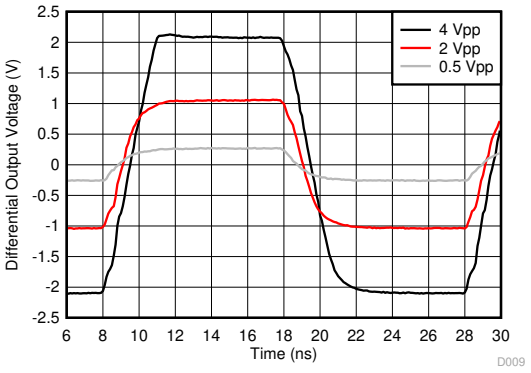
50-MHz input, 0.3-ns input edge rate, single-ended to differential output, DC coupled, see 図 7-3

図 6-7. Small- and Large-Signal Step Response



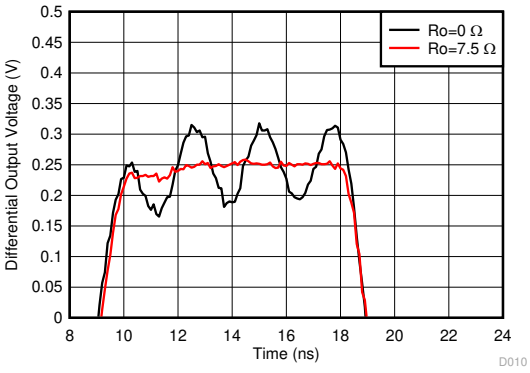
Av = 2, 500-mV_{PP} output into 22-pF Cload, see 図 7-11

図 6-8. Step Response into Capacitive Load



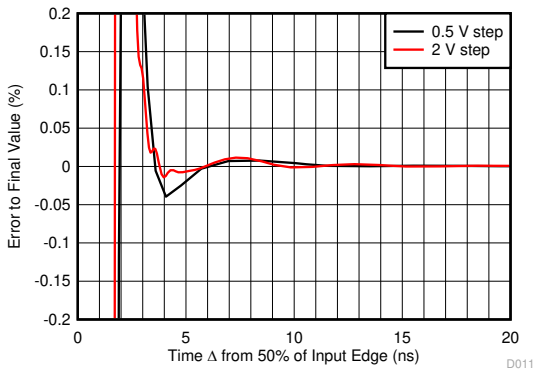
G = 5 V/V, 50-MHz input, 0.3-ns input edge rate, single-ended input to differential output, see 図 7-3

図 6-9. Small- and Large-Signal Step Response



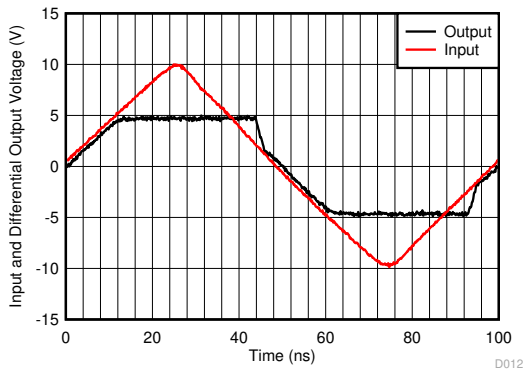
G = 5 V/V, 500-mV_{PP} output into 22-pF Cload, see 図 7-11 and 表 8-1

図 6-10. Step Response into Capacitive Load



Simulated with 2-ns input transition time, see 図 7-3

図 6-11. Small- and Large-Signal Step Settling Time

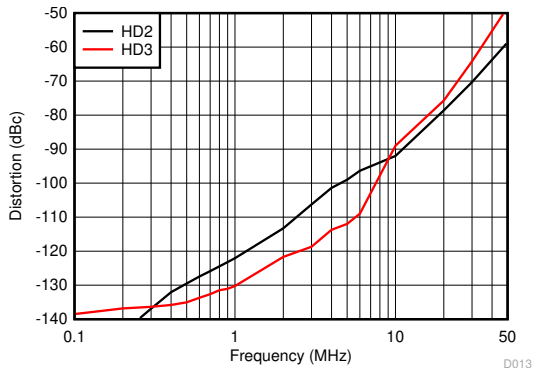


Single-ended to differential gain of 2 (see 図 7-3), 2 × input overdrive

図 6-12. Overdrive Recovery Performance

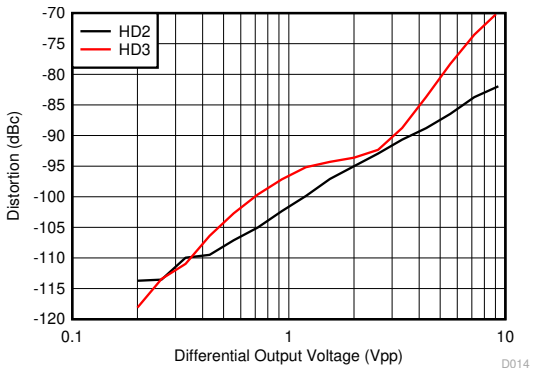
6.7 Typical Characteristics: 5-V Single Supply (continued)

at Vs+ = 5 V, Vs– = GND, Vocm is open, 50-Ω single-ended input to differential output, gain = 2 V/V, Rload = 500 Ω, and T_A ≈ 25°C (unless otherwise noted)



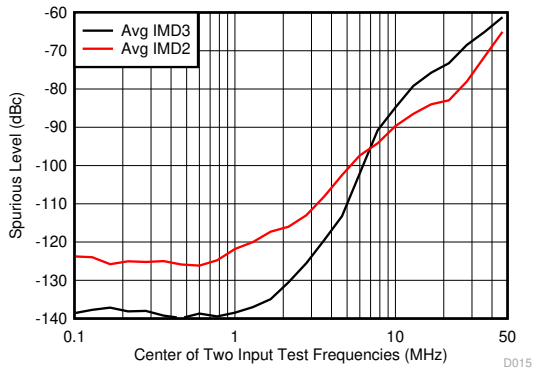
2-V_{PP} output, see 図 7-1

図 6-13. Harmonic Distortion Over Frequency



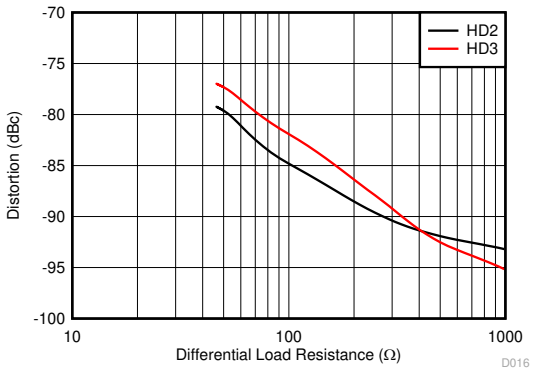
10 MHz, see 図 7-1

図 6-14. Harmonic Distortion vs Output Swing



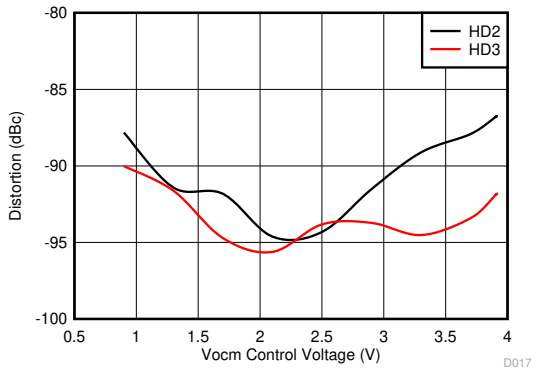
1 V_{PP} each tone, see 図 7-1

図 6-15. IMD2 and IM3 Over Frequency



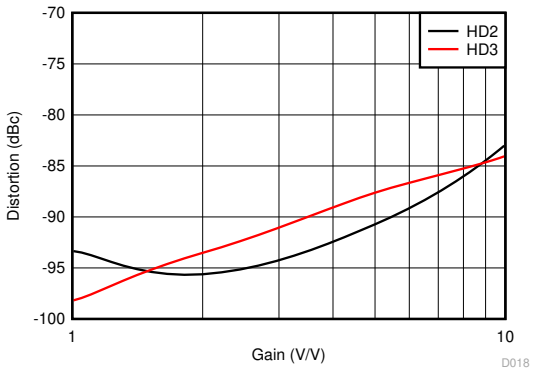
f = 10 MHz, see 図 7-1 with Rload adjusted

図 6-16. Harmonic Distortion vs Rload



f = 10 MHz, 2-V_{PP} output,
see 図 7-3 with Vocm adjusted

図 6-17. Harmonic Distortion vs Vocm

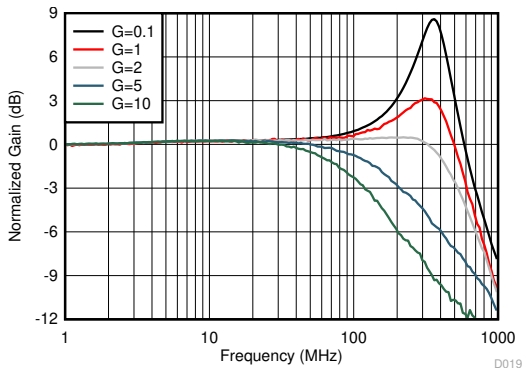


10 MHz, 2-V_{PP} output,
see 図 7-1 and 表 8-1 for gain setting

図 6-18. Harmonic Distortion vs Gain

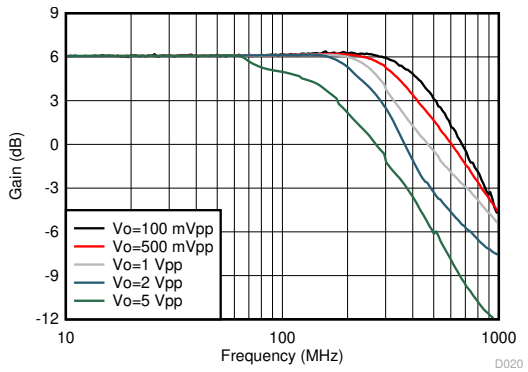
6.8 Typical Characteristics: 3-V Single Supply

at Vs+ = 3 V, Vs– = GND, Vocm is open, 50-Ω single-ended input to differential output, gain = 2 V/V, Rload = 500 Ω, and T_A ≈ 25°C (unless otherwise noted)



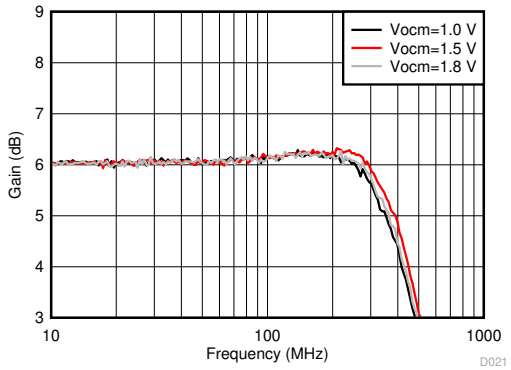
Rf = 402 Ω, Vout = 100 mV_{PP}, see 図 7-1 and 表 8-1 for resistor values

図 6-19. Small-Signal Frequency Response vs Gain



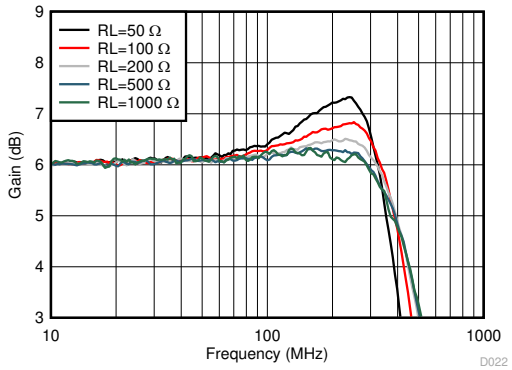
See 図 7-1 with V_{CC} = 3 V and Vocm = 1.5 V

図 6-20. Frequency Response vs Vopp



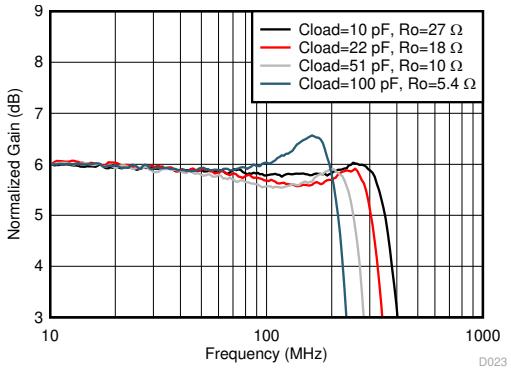
Vout = 100 mV_{PP}, see 図 7-1 with Vocm adjusted

図 6-21. Small-Signal Frequency response vs Vocm



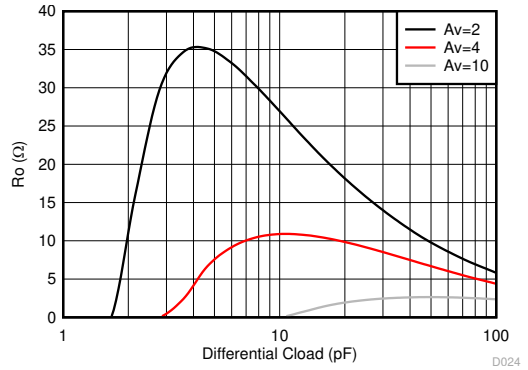
Vout = 100 mV_{PP}, see 図 7-1 with the Rload adjusted

図 6-22. Small-Signal Frequency Response vs Rload



100 mV_{PP} at load, Av = 2 (see 図 7-11), two series Ro added at output before Cload

図 6-23. Small-Signal Frequency Response vs Cload

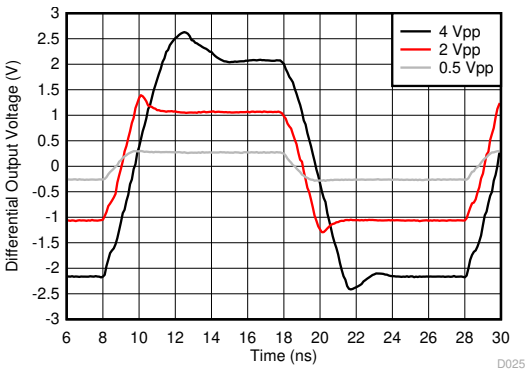


Two Ro at output to differential Cload in parallel with 500 Ω, see 図 7-11 and 表 8-1

図 6-24. Recommended Ro vs Cload

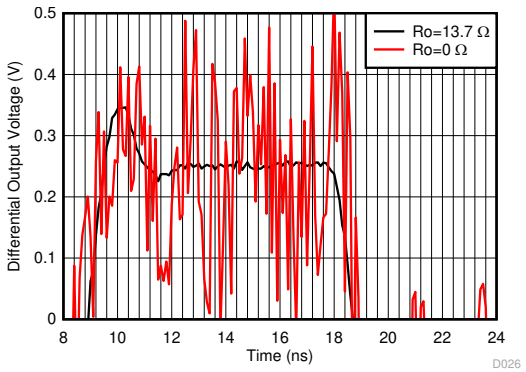
6.8 Typical Characteristics: 3-V Single Supply (continued)

at Vs+ = 3 V, Vs– = GND, Vocm is open, 50-Ω single-ended input to differential output, gain = 2 V/V, Rload = 500 Ω, and T_A ≈ 25°C (unless otherwise noted)



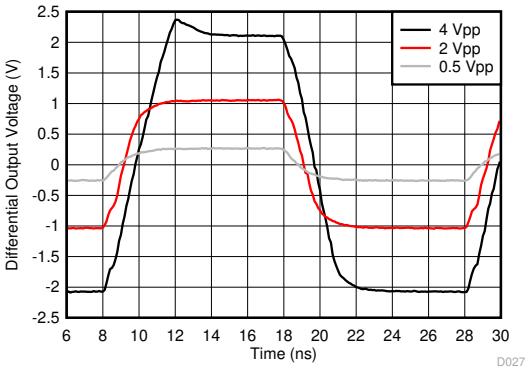
50-MHz input, 0.3-ns input edge rate, single-ended input to differential output, DC coupled, see 図 7-3

図 6-25. Small- and Large-Signal Step Response



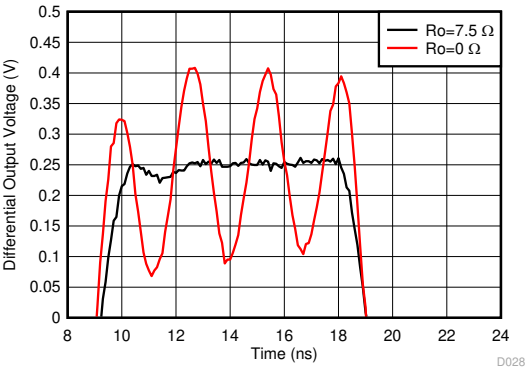
500-mV_{PP} output into 22-pF Cload, see 図 7-11 with Vs+ = 3 V and Vocm = 1.5 V

図 6-26. Step Response Into Capacitive Load



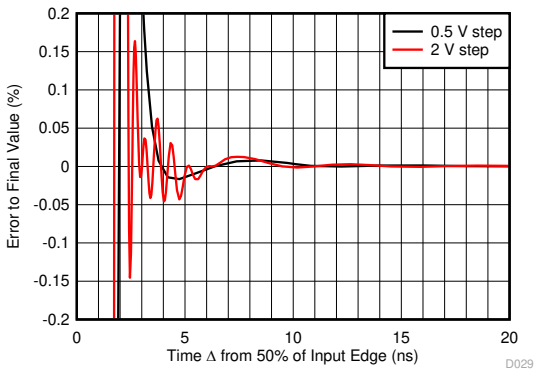
G = 5 V/V, 50-MHz input, 0.3-ns input edge rate, single-ended input to differential output, see 図 7-1

図 6-27. Small- and Large-Signal Step Response



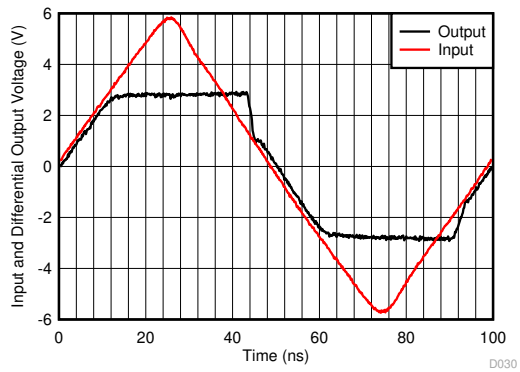
G = 5 V/V, 500-mVpp output into 22-pF Cload, see 図 7-11 and 表 8-1

図 6-28. Step Response into Capacitive Load



Simulated with 2-ns input transition time, see 図 7-3

図 6-29. Small- and Large-Signal Step Settling Time

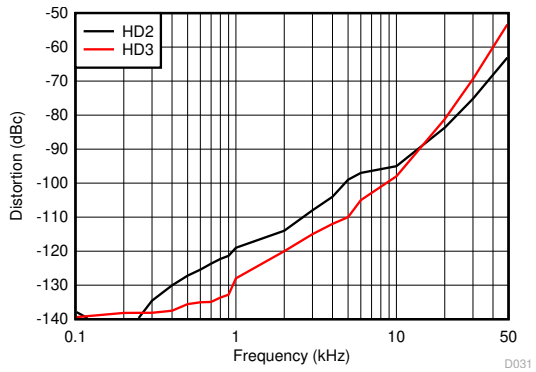


Single-ended to differential gain of 2 (see 図 7-3), > 2 × input overdrive

図 6-30. Overdrive Recovery Performance

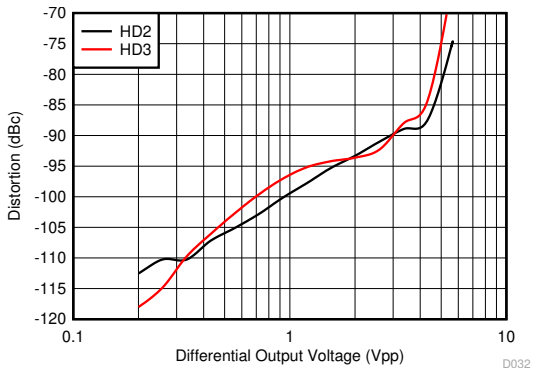
6.8 Typical Characteristics: 3-V Single Supply (continued)

at Vs+ = 3 V, Vs– = GND, Vocm is open, 50-Ω single-ended input to differential output, gain = 2 V/V, Rload = 500 Ω, and T_A ≈ 25°C (unless otherwise noted)



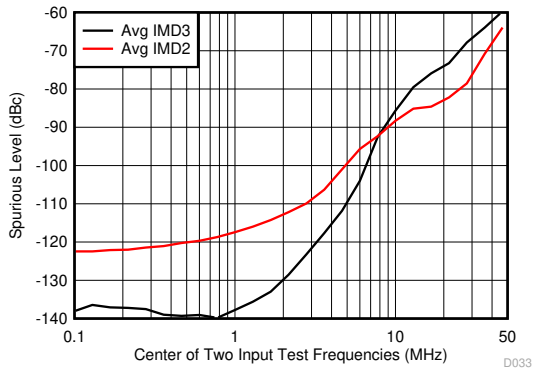
2-V_{PP} output, see 図 7-1 with Vs+ = 3 V, Vocm = 1.5 V

図 6-31. Harmonic Distortion Over Frequency



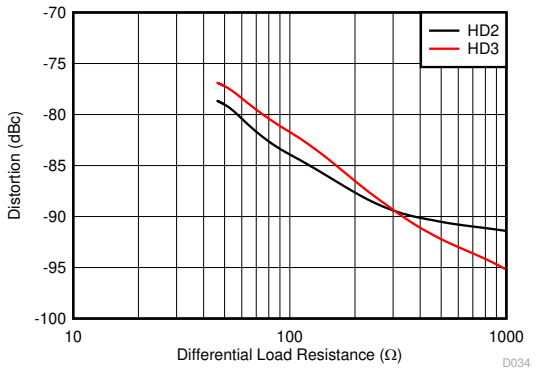
f = 10 MHz, see 図 7-1 with Vs+ = 3 V, Vocm = 1.5 V

図 6-32. Harmonic Distortion vs Output Swing



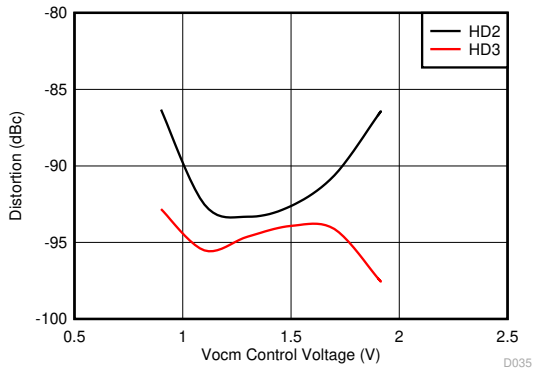
1 V_{PP} each tone, see 図 7-1 with Vs+ = 3 V, Vocm = 1.5 V

図 6-33. IMD2 and IM3 Over Frequency



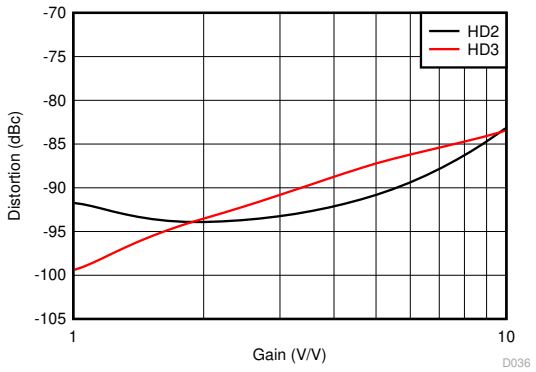
f = 10 MHz, see 図 7-1 with Vs+ = 3 V, Vocm = 1.5 V

図 6-34. Harmonic Distortion vs Rload



f = 10 MHz, 2-V_{PP} output,
ee 図 7-3 with Vocm adjusted

図 6-35. Harmonic Distortion vs Vocm



f = 10 MHz, 2-V_{PP} output,
see 図 7-1 and 表 8-1 for gain setting

図 6-36. Harmonic Distortion vs Gain

6.9 Typical Characteristics: 3-V to 5-V Supply Range

at Vs+ = 3 V and 5 V, Vs– = GND, Vocm is open, 50-Ω single-ended input to differential output, gain = 2 V/V, Rload = 500 Ω, and T_A ≈ 25°C (unless otherwise noted)

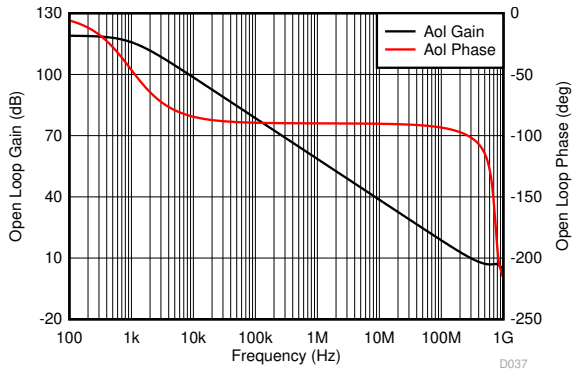
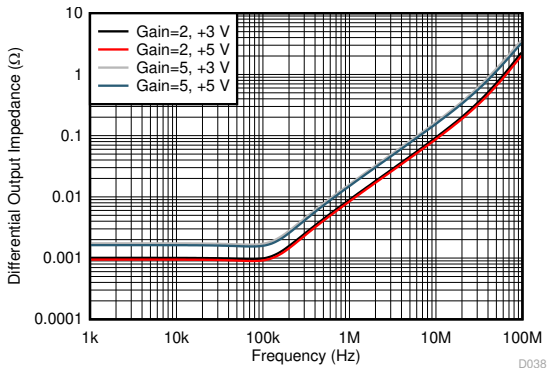


図 6-37. Main Amplifier Differential Open-Loop Gain and Phase vs Frequency



Single-ended input to differential output, simulated differential output impedance, (closed-loop) gain of 2 and 5, see 図 7-1

図 6-38. Closed-Loop Output Impedance

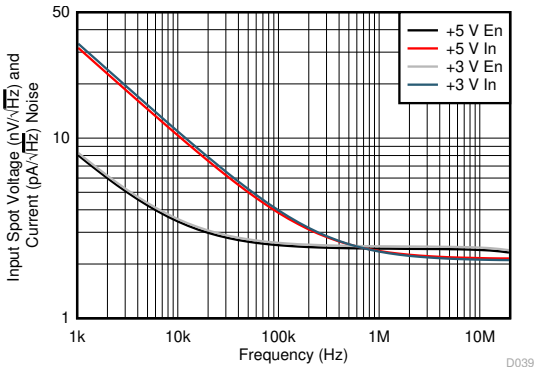
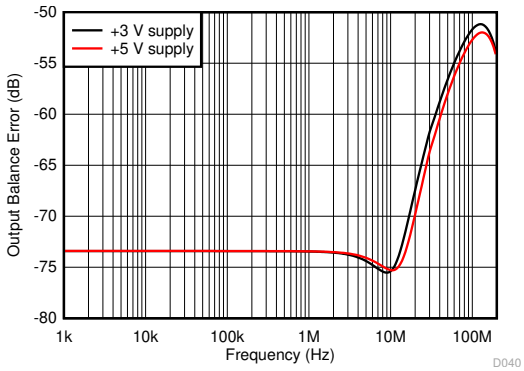
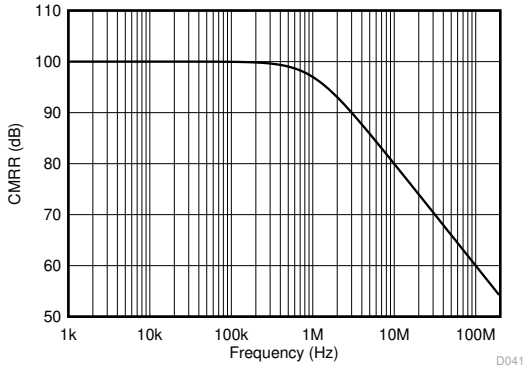


図 6-39. Input Spot Noise Over Frequency



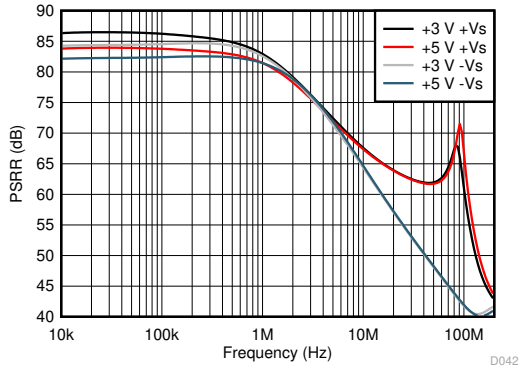
Single-ended input to differential output, gain of 2 (see 図 7-1), simulated with 1% resistor, worst-case mismatch

図 6-40. Output Balance Error Over Frequency



Common-mode in to differential out, gain of 2 simulation

図 6-41. CMRR Over Frequency



Single-ended to differential, gain of 2 (see 図 7-1) PSRR simulated to differential output

図 6-42. PSRR Over Frequency

6.9 Typical Characteristics: 3-V to 5-V Supply Range (continued)

at Vs+ = 3 V and 5 V, Vs– = GND, Vocm is open, 50-Ω single-ended input to differential output, gain = 2 V/V, Rload = 500 Ω, and T_A ≈ 25°C (unless otherwise noted)

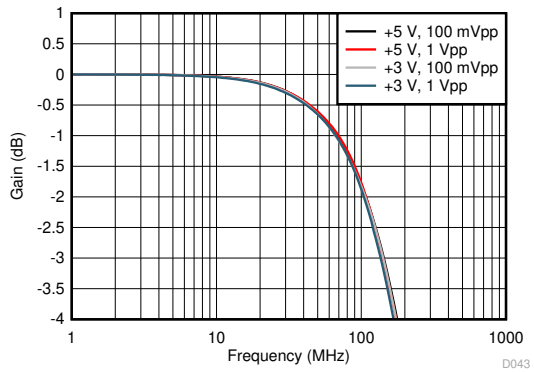


図 6-43. Common-Mode, Small- and Large-Signal Response (Vocm pin driven)

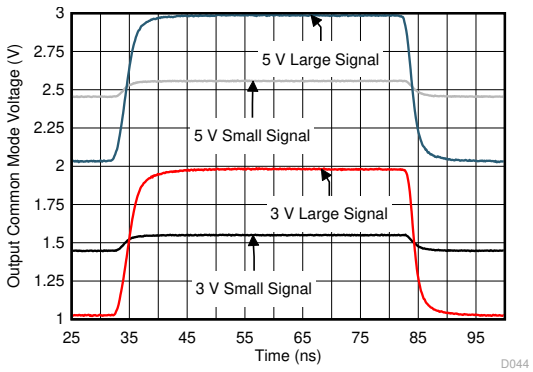
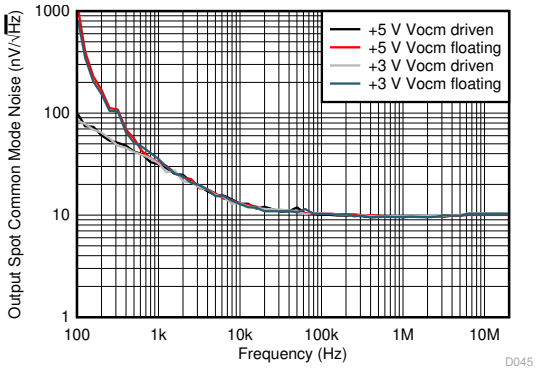
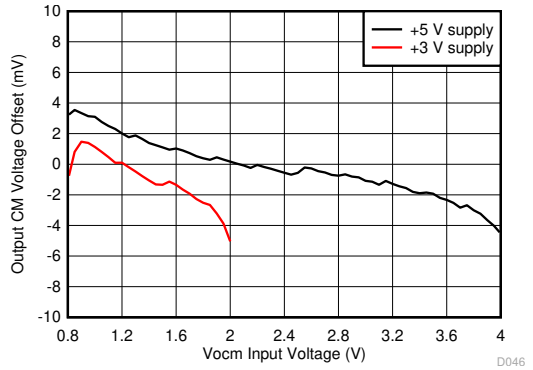


図 6-44. Common-Mode, Small- and Large-Step Response (Vocm pin driven)



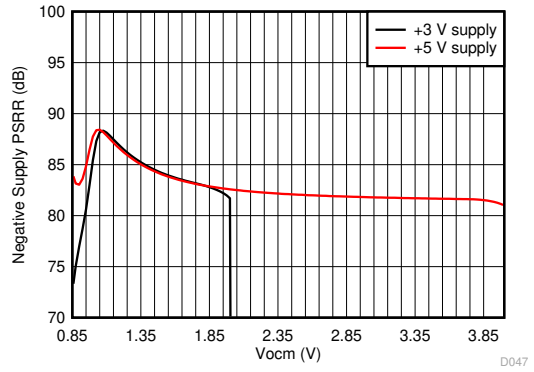
Vocm input either driven to midsupply by low impedance source, or allowed to float and default to midsupply

図 6-45. Output Common-Mode Noise



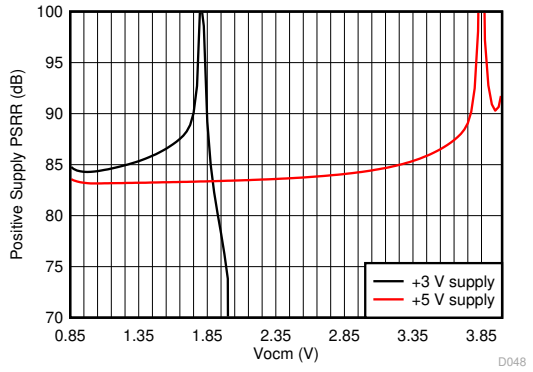
Average Vocm output offset of 37 units, standard deviation < 2.5 mV, see 図 7-3

図 6-46. Vocm Offset vs Vocm Setting



Single-ended to differential gain of 2 (see 図 7-1), PSRR for negative supply to differential output (1-kHz simulation)

図 6-47. –PSRR vs Vocm Approaching Vs–

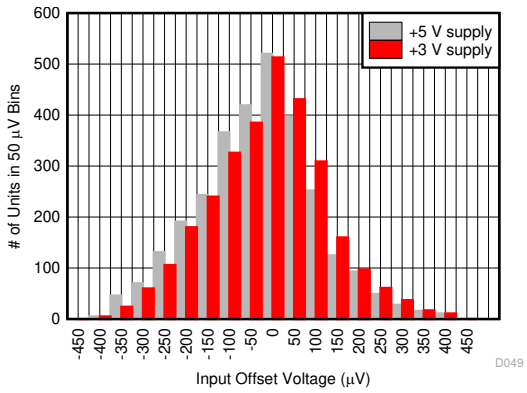


Single-ended to differential gain of 2 (see 図 7-1), PSRR for positive supply to differential output (1-kHz simulation)

図 6-48. +PSRR vs Vocm Approaching Vs+

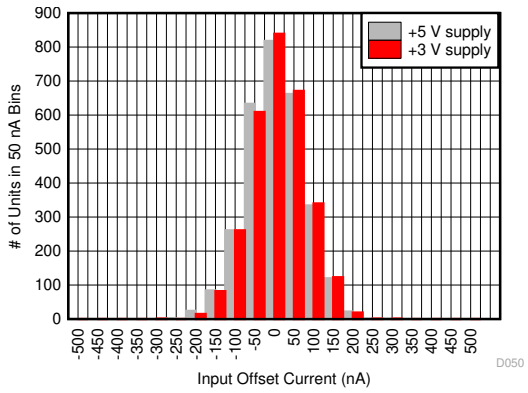
6.9 Typical Characteristics: 3-V to 5-V Supply Range (continued)

at Vs+ = 3 V and 5 V, Vs– = GND, Vocm is open, 50-Ω single-ended input to differential output, gain = 2 V/V, Rload = 500 Ω, and T_A ≈ 25°C (unless otherwise noted)



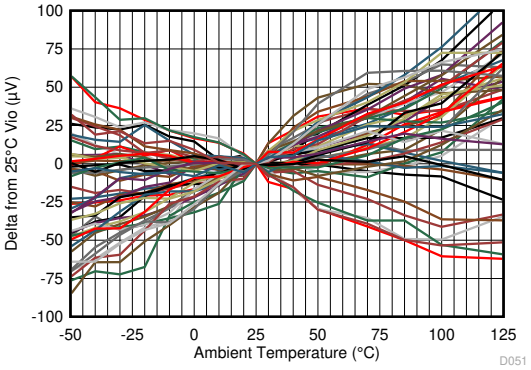
3 lots, total of 2962 units trimmed at 5-V supply

図 6-49. Input Offset Voltage



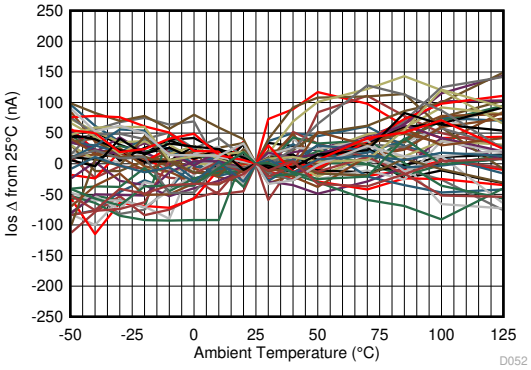
3 lots, total of 2962 units

図 6-50. Input Offset Current



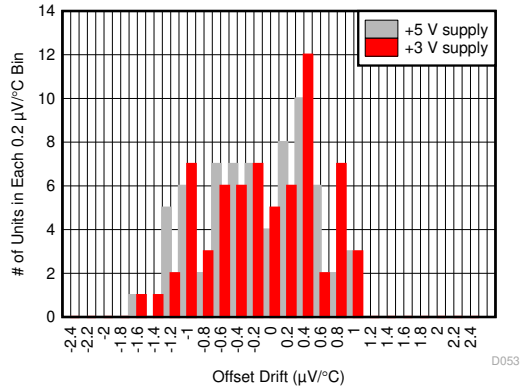
5-V and 3-V delta from 25°C V_{IO}, 25 units

図 6-51. Input Offset Voltage Over Temperature



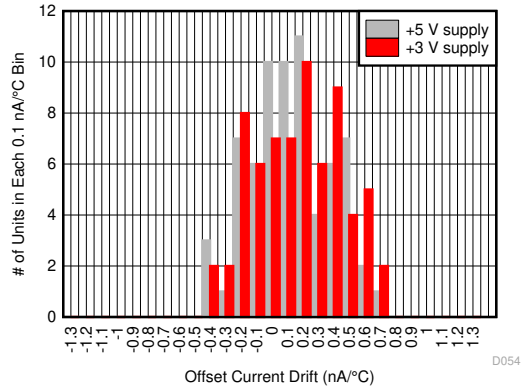
5-V and 3-V over temperature I_{OS}, 25 units

図 6-52. Input Offset Current Over Temperature



–40°C to +125°C endpoint drift, 3 lots, total of 68 units

図 6-53. Input Offset Voltage Drift

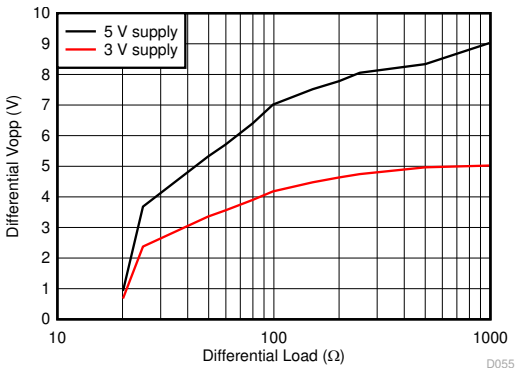


–40°C to +125°C endpoint drift, 3 lots, total of 68 units

図 6-54. Input Offset Current Drift

6.9 Typical Characteristics: 3-V to 5-V Supply Range (continued)

at Vs+ = 3 V and 5 V, Vs– = GND, Vocm is open, 50-Ω single-ended input to differential output, gain = 2 V/V, Rload = 500 Ω, and T_A ≈ 25°C (unless otherwise noted)



Maximum differential output swing, Vocm at midsupply

図 6-55. Maximum Vopp vs Rload

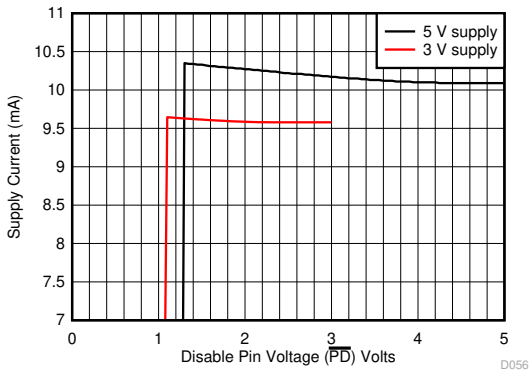
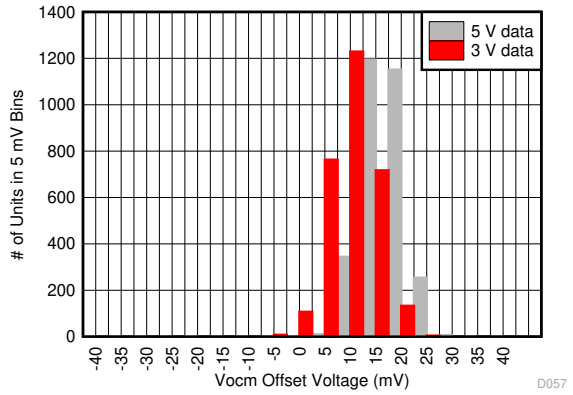
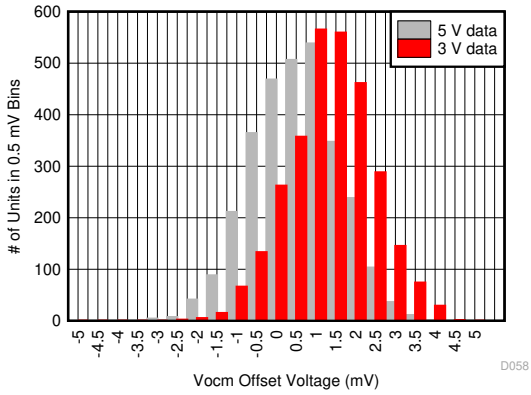


図 6-56. Supply Current vs PD Voltage



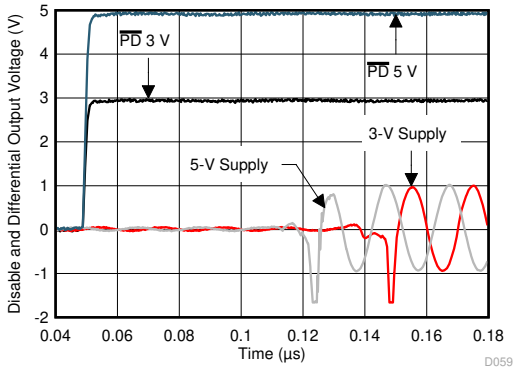
Vocm input floating, 3 lots, total of 2962 units

図 6-57. Common-Mode Output Offset from Vs+ / 2 Default Value



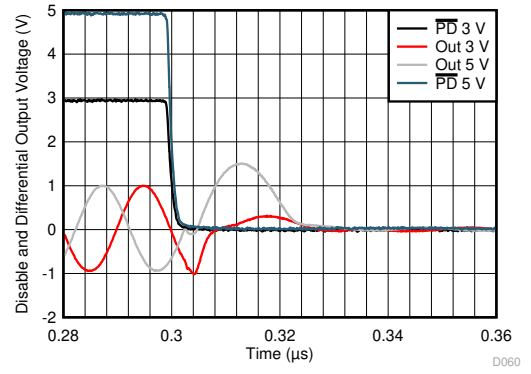
Input driven midsupply, 3 lots, total of 2962 units

図 6-58. Common-Mode Output Offset from Driven Vocm



10 MHz, 1-Vpp input single to differential gain of 2, see 図 7-3

図 6-59. PD Turn On Waveform



10 MHz, 1-V_{PP} input single to differential gain of 2, see 図 7-3

図 6-60. PD Turn Off Waveform

7 Parameter Measurement Information

7.1 Example Characterization Circuits

The THS4541-Q1 offers the advantages of a fully differential amplifier (FDA) design, with the trimmed input offset voltage of a precision op amp. The FDA is an extremely flexible device that provides a purely differential output signal centered on a settable output common-mode level. The primary options revolve around the choices of single-ended or differential inputs, ac-coupled or dc-coupled signal paths, gain targets, and resistor-value selections. The characterizations shown in 図 6-1 to 図 6-36 focus on single-ended-to-differential designs as the more challenging application requirement. Differential sources can certainly be supported and are often simpler to both implement and analyze.

Because most lab equipment is single-ended, the characterization circuits typically operate with a single-ended, matched, 50-Ω input termination to a differential output at the FDA output pins. That output is then translated back to single-ended through a variety of baluns (or transformers) depending on the test and frequency range. DC-coupled, step-response testing uses two 50-Ω scope inputs with trace math. The starting point for any single-ended-to-differential, ac-coupled characterization plot is shown in 図 7-1.

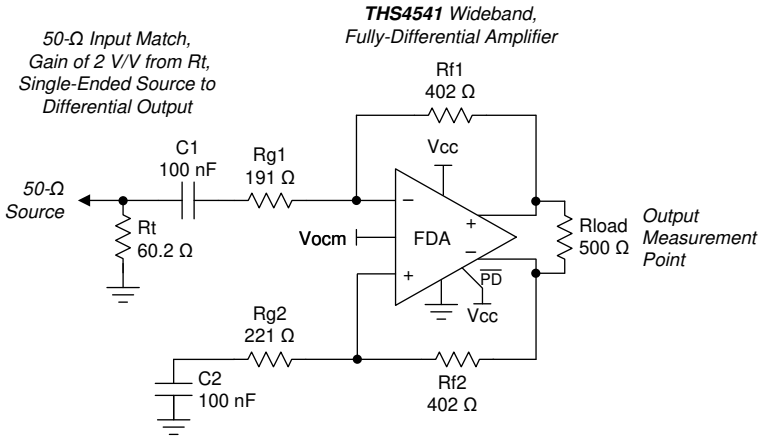


図 7-1. AC-Coupled, Single-Ended Source to a Differential Gain of a 2-V/V Test Circuit

Most characterization plots fix the R_f (R_{f1} = R_{f2}) value at 402 Ω, as shown in 図 7-1. This element value is completely flexible in application, but the 402 Ω provides a good compromise for the parasitic issues linked to this value, specifically:

- Added output loading. The FDA appears like an inverting op amp design with both feedback resistors as an added load across the outputs (approximate total differential load in 図 7-1 is 500 Ω || 804 Ω = 308 Ω).
- Noise contributions because of the resistor values. The resistors contribute both a 4kTR term and provide gain for the input current noise (see *セクション 7.5*).
- Parasitic feedback pole at the input summing nodes. This pole created by the feedback R value and the 0.85-pF differential input capacitance (as well as any board layout parasitic) introduces a zero in the noise gain, decreasing the phase margin in most situations. This effect must be managed for best frequency response flatness or step response overshoot. The 402-Ω value selected does degrade the phase margin slightly over a lower value, but does not decrease the loading significantly from the nominal 500-Ω value across the output pins.

The frequency domain characterization curves start with the selections of 図 7-1. Then, various elements are modified to show the impact over a range of design targets, specifically:

- Gain setting is changed by adjusting R_t and the 2 – R_g elements (holding a 50-Ω input match).
- Output loading, including both resistive and capacitive load testing.
- Power-supply settings. Most often, a single +5-V test uses a ±2.5-V supply, and a +3-V test uses ±1.5-V supplies.
- The disable control pin is tied to Vs+ for any active channel test.

Because most network and spectrum analyzers are a single-ended input, the output network on the THS4541-Q1 characterization tests typically show the desired load connected through a balun to a single-ended, 50-Ω load, while presenting a 50-Ω source from the balun output back into the balun. For instance, 図 7-2 shows a wideband MA/Com balun used for 図 7-1. This network shows a 500-Ω differential load to the THS4541-Q1, but an ac-coupled, 50-Ω source to the network analyzer. Distortion testing typically uses a lower-frequency, dc-isolated balun (such as the TT1-6T) that is rotated 90° from the wider band interface of 図 7-2.

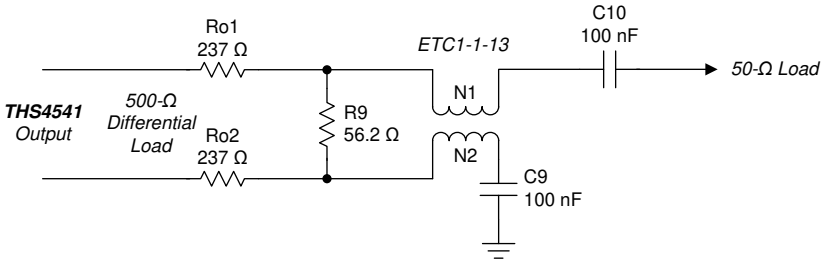


図 7-2. Example 500-Ω Load to a Single-Ended, Doubly-Terminated, AC-Coupled, 50-Ω Interface

This approach allows a higher differential load, but with a wideband 50-Ω output match at the cost of considerable signal-path insertion loss. This loss is acceptable for characterization, and is normalized out to show the characterization curves.

For time-domain or dc-coupled testing, the circuit of 図 7-3 is used as a starting point, where the gain of a 5-V/V setting used in 図 6-9 and 図 6-27 are illustrated.

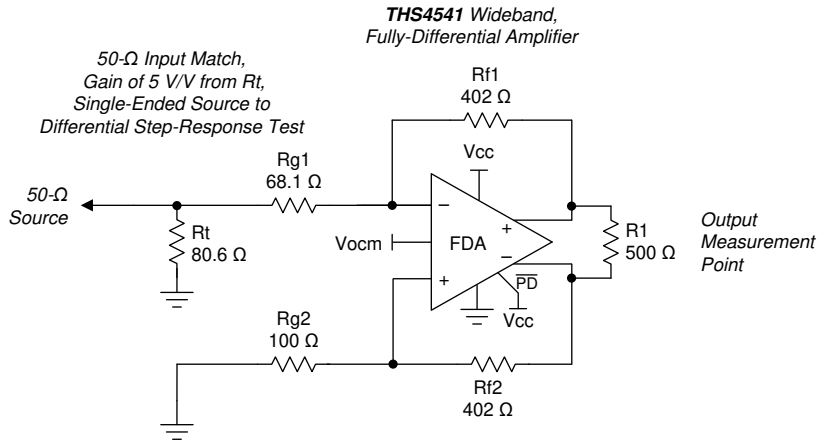


図 7-3. DC-Coupled, Single-Ended-to-Differential, Basic Test Circuit Set for a Gain of 5 V/V

In this case, the input is dc-coupled, showing a 50-Ω input match to the source, gain of 5 V/V to a differential output, again driving a nominal 500-Ω load. Using a single supply, the Vocm control input can either be floated (defaulting to midsupply) or be driven within the allowed range for the Vocm loop (see the headroom limits on Vocm in the *Electrical Characteristics* tables). To use this circuit for step-response measurements, load each of the two outputs with a 250-Ω network, translating to a 50-Ω source impedance driving into two 50-Ω scope inputs. Then, difference the scope inputs to generate the step responses of 図 6-9 and 図 6-27. 図 7-4 shows the output interface circuit. This grounded interface pulls a dc load current from the output Vocm voltage for single-supply operation. Running this test with balanced bipolar power supplies eliminates this dc load current and gives similar waveform results.

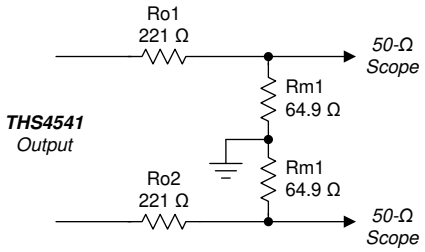


図 7-4. Example 500-Ω Load to Differential, Doubly-Terminated, DC-Coupled 50-Ω Scope Interface

7.2 Frequency-Response Shape Factors

図 6-1 illustrates the small-signal response shape versus gain using a fixed 402-Ω feedback resistor in the circuit of 図 7-1. Being a voltage-feedback based FDA, the THS4541-Q1 shows a response shape that varies with gain setting, largely determined by the loop-gain crossover frequency and phase margin at the crossover. This loop-gain crossover frequency is where the open-loop response and the noise gain intersect (where the loop gain drops to 1). The noise gain is the inverse of the voltage divider from the outputs back to the differential inputs; use a balanced divider ratio on each feedback path. In general, the noise gain (NG) does not equal the signal gain for designs providing an input match from a source impedance. NG is given by 1 + Rf / (total impedance from the inverting summing junction to ground). Using the resistor values computed in the gain sweep of 表 8-1, and repeating that sweep showing the NG gives 表 7-1, where only the exact R solutions are shown.

表 7-1. Resistor Values and Noise Gain for Swept Gain With Rf = 402 Ω

SIGNAL GAIN(1)	Rt, EXACT (Ω)	Rg1, EXACT (Ω)	Rg2, EXACT (Ω)	NOISE GAIN
1	55.2	399	425	1.94
2	60.1	191	218	2.85
3	65.6	124	153	3.63
4	72	89.7	119	4.37
5	79.7	67.8	98.3	5.09
6	89.1	54.2	86.5	5.65
7	101	43.2	76.6	6.25
8	117	35.2	70.1	6.74
9	138	29	65.8	7.11
10	170	23.6	62.5	7.44
11	220	18.7	59.3	7.78
12	313	14.6	57.7	7.97
13	545	10.8	56.6	8.11
14	2209	7.26	56.1	8.16

NG is critically important for bandwidth and all output error terms (such as dc offset and noise). For lower-speed devices, normally only the dc noise gain is considered. However, for the THS4541-Q1, with loop gain crossover

at greater than 300 MHz, the feedback network produces a parasitic pole to the differential summing junctions that causes the noise gain to increase with frequency. This pole causes a lower crossover frequency than is expected with added phase shift around the loop. Consider the feedback network (single-ended) of 図 7-5, showing a parasitic 0.2 pF on the feedback 402-Ω resistor. The 0.85-pF differential input capacitance of the THS4541-Q1 is converted to single-ended as a 1.7-pF parasitic for this single-sided analysis circuit (the Rg shown is Rg2 in 図 7-1).

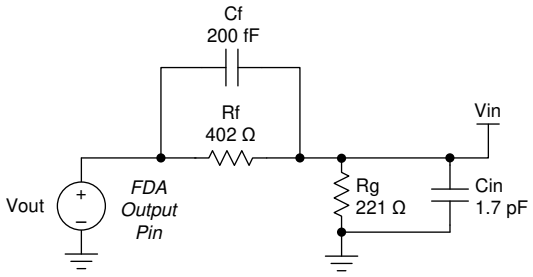


図 7-5. Feedback Network for the Gain of 2 Configuration Using 402 Ω and Matching to a 50-Ω Source

The response shape from Vout to Vin in 図 7-5 has a pole and then a zero. To describe NG, invert the Laplace transform of Vin and Vout from 図 7-5 to provide the frequency-dependent NG response of 式 1, where a zero comes in first and then a pole.

$$NG = \left(1 + \frac{Cin}{Cf}\right) \frac{s + \dfrac{1 + \dfrac{Rf}{Rg}}{Rf\,(Cf + Cin)}}{s + \dfrac{1}{Rf \bullet Cf}} \tag{1}$$

The zero location is key. Using the gain of 2 values of 図 7-5, the estimated zero in the NG is 588 MHz. Limiting the parasitic capacitance at the summing junctions, either differentially or signal-ended, to a ground or power plane is critical in board layouts.

Using this feedback model, and the open-loop gain and phase data for the THS4541-Q1, allows the Aol and NG curves over frequency to be drawn, as shown in 図 7-6, where the peaking in the noise gain pulls the intersection point back in frequency.

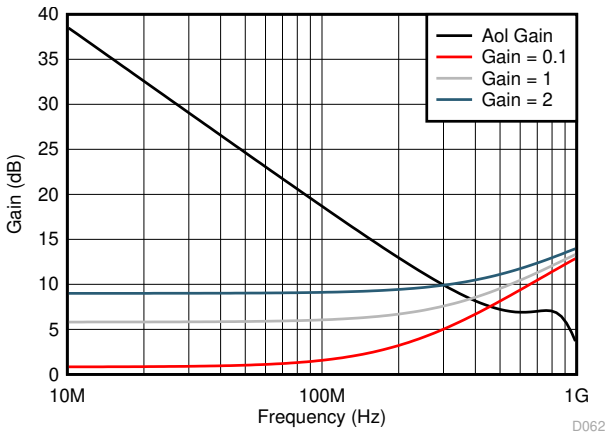


図 7-6. Aol and Noise Gain Plots for the Lower Gains of 図 6-1

To assess closed-loop bandwidth and peaking, the noise-gain phase must be subtracted from the THS4541-Q1 AoI phase to obtain the total phase around the loop, as shown in 図 7-7.

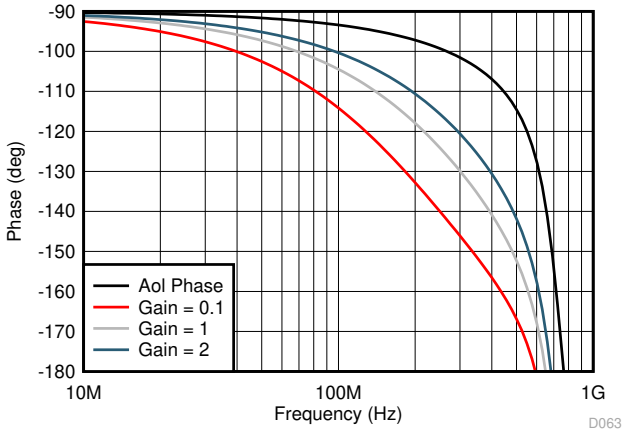


図 7-7. Loop-Gain Phase for the Three Lower Gains of 表 7-2

From 図 7-6 and 図 7-7, using 表 7-2, tabulate the loop-gain crossover frequency and phase margin at these crossovers to explain the response shapes of 図 6-1.

表 7-2. Estimated Crossover Frequency and Phase Margin for Gains of 0.1, 1, and 2 in 図 6-1

GAIN	DC NG (V/V)	0-dB LG (MHz)	PHASE MARGIN (°)
0.1	1.1	457	18
1	1.94	380	41
2	2.85	302	59

From these crossover (or 0-dB loop gain) frequencies, a good approximation for the resulting f_{-3dB} is to multiply the crossover frequencies by 1.6 when the phase margin is less than 65°. Ideally, a 65° phase margin at loop-gain crossover provides a flat Butterworth closed-loop response. The 59° phase margin for the gain of 2 setting explains the nearly flat response for this condition with 1.6 × 302 MHz = 483 MHz, estimated with f_{-3dB} closely matching the measured 500-MHz SSBW.

The very low phase margin in the attenuator setting at 0.1 V/V explains the highly peaked response in 図 6-1. This peaking can be easily compensated, as shown in the *セクション 9.2.1* section, using feedback capacitors and a differential capacitor across the inputs.

Considering the noise gain zero as part of the loop-gain analysis shows the importance of using relatively-low, feedback-resistor values and minimizing layout parasitic capacitance on the input pins of the THS4541-Q1 to reduce the effects of this feedback pole. The TINA model does a good job of predicting these issues (the model includes the 0.85-pF differential internal capacitance); add any estimated external parasitic capacitance on the summing junctions in simulation to predict the response shape more accurately.

7.3 I/O Headroom Considerations

The starting point for most designs is usually to assign an output common-mode voltage. For ac-coupled signal paths, this voltage is often the default midsupply voltage to retain the most available output swing around the centered Vocm. For dc-coupled designs, set this voltage with consideration for the required minimum headroom to the supplies shown in the specifications for the Vocm control. From the target output Vocm, the next step is to verify that the desired output differential V_{PP} stays within the supplies. For any desired differential Vopp, check that the absolute maximum output pin swings with 式 2 and 式 3, and confirm the differential Vopp are within the supply rails for this rail-to-rail (RR) output device.

$$Vo_{min} = Vocm - \frac{Vopp}{4} \quad (2)$$

$$Vo_{max} = Vocm + \frac{Vopp}{4} \quad (3)$$

For instance, driving the ADC3223 with a 0.95 Vcm control using a single 3.3-V supply, the maximum output swing is set by the negative-going signal from 0.95 Vcm to +0.2 V above ground. This 0.75-V, single-sided swing becomes an available 4 × 0.75 V = 3 V_{PP} differential around the nominal 0.95 Vcm output common mode. On the high side, the maximum output is 0.95 + 0.75 = 1.7 V. This result is well within the allowed maximum of 3.3 V – 0.2 V = 3.1 V. This 3 V_{PP} is also well beyond the maximum required 2-V_{PP} full-scale differential input for this ADC. However, having this extra swing range is useful if an interstage filter to the ADC adds insertion loss.

With the output headrooms confirmed, the input junctions must also stay within the operating range. The input range extends to the negative supply voltage (over the full temperature range); therefore, input range limitations usually appear only approaching the positive supply, where a maximum 1.3-V headroom is required over the full temperature range.

The input pins operate at voltages set by the external circuit design, the required output Vocm, and the input signal characteristics. For differential-to-differential designs where the input Vicm voltage does not move with the input signal, there are two configurations to consider:

- AC-coupled, differential-input designs have a Vicm equal to the output Vocm. The input Vicm requires approximately a 1.3-V headroom to the positive supply; therefore, the maximum Vocm to that value reduces from the Vocm positive headroom requirement of 1.2 V to the 1.3 V required on the input pins. The lower limit on the output Vocm is approximately 0.95 V to the negative supply over the full temperature range, and well within the 0-V minimum headroom on the input Vicm.
- DC-coupled, differential-input designs, check the voltage divider from the source Vcm to the THS4541-Q1 Vocm setting to confirm the resulting voltage divider solves to an input Vicm within the allowed range. If the source Vcm can vary over some voltage range, this result must be validated over that range.

For single-ended input to differential output designs, there is a dc Vicm voltage set by the external configuration with a small-signal related swing around that. The two conditions to consider are:

- AC-coupled, single-ended input to differential designs place an average input Vicm equal to the output Vocm voltage with an ac-coupled swing around that Vocm following the input voltage.
- DC-coupled, single-ended input to differential designs get a nominal input Vicm set by the source-signal common mode and the output Vocm setting with a small, signal-related swing around the dc Vicm level set by the voltage divider.

One method of deriving the voltage range for Vicm for any single-ended input to differential output design is to determine the voltage swing on the nonsignal-input side of the FDA outputs and simply take the respective divider back to the input pin to ground or the dc reference used on that side. An example analysis is shown in 図 7-8, where the circuit of 図 7-1 is simplified to show just a Thevenized source impedance.

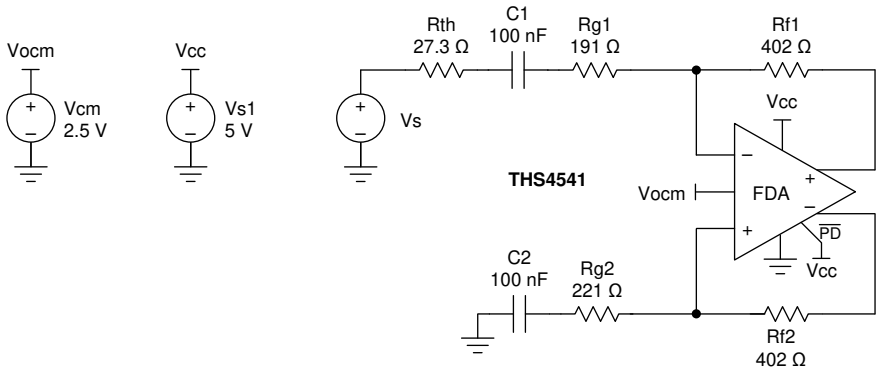


図 7-8. Input Swing Analysis Circuit From 図 7-1 With Thevenized Source

For this ac-coupled input analysis, the nominal dc input Vicm is simply the output Vocm (2.5 V in this example design). Then, considering the lower side of the feedback networks, any desired maximum output differential V_{PP} generates a known ac V_{PP} at the junction of Rg2 and Rf2. For instance, if the design intends a maximum 4-V_{PP} differential output, each FDA output pin is ±1 V around the Vocm (= 2.5 V), and then back to the Vicm, which produces a ±1 V × 221 / (221 + 402) = ±0.355 V around the dc setting of Vocm. This simple approach to assessing the input Vicm range for a single-ended to differential design can be applied to any design using an FDA by reducing the input side circuits to a divider to either the signal source and ground or voltage reference on the nonsignal input side.

7.4 Output DC Error and Drift Calculations and the Effect of Resistor Imbalances

The THS4541-Q1 offers a trimmed input offset voltage and extremely low offset drift over the full –40°C to +125°C operating range. This offset voltage combines with several other error contribution terms to produce an initial 25°C differential offset error band, and then a drift over temperature. For each error term, a gain must be assigned to that term. For this analysis, only DC-coupled signal paths are considered. One new source of output error (versus typical op amp analysis) arises from the effect that mismatched resistor values and ratios can have on the two sides of the FDA. Any common-mode voltage or drift creates a differential output error through the slight mismatches arising from the external feedback and gain-setting resistor tolerances, and the approximation (or snap) to standard value.

The error terms (25°C and drift), along with the gain to the output differential voltage, include:

- Input offset voltage—this voltage has a gain equal to the noise gain or 1 + Rf / Rg, where Rg is the total DC impedance from the input pins back to the source, or a DC reference (typically ground).
- Input offset current—this current has a gain to the differential output through the average feedback resistor value.

The remaining terms arise from an assumed range on both the absolute feedback resistor mismatch and the mismatch in the divider ratio on each side of the FDA. The first of these resistor mismatch terms is the input bias current creating a differential output offset because of Rf mismatch. For simplicity, the upper Rf and Rg values are called Rf1 and Rg1 with a ratio of Rf1 / Rg1 ≡ G1. The lower elements are defined as Rf2 and Rg2 with a ratio of Rf2 / Rg2 ≡ G2. To compute worst-case contributions, a maximum variation in the design resistor tolerance is used in the absolute and ratio mismatches. For instance, ±1% tolerance resistors are assumed, giving a worst-case G1 that is 2% higher than nominal and a G2 that is 2% lower than nominal, with a worst-case Rf value mismatch of 2% as well. For matched impedance designs with Rt and Rg1 on a single-ended to differential stage, the standard value snap imposes a fixed mismatch in the initial feedback ratios with the resistor tolerance adding a mismatch to this initial ratio mismatch. Define the selected external resistor tolerance as ±T (so for 1% tolerance resistors, T = 0.01).

- Total gain for bias current error is ±2 × T × Rfnom

Anything that generates an output common-mode level or shift over temperature also generates an output differential error term if the two feedback ratios, G1 and G2, are not equal. An error trying to produce a shift in the output common-mode is overridden by the common-mode control loop, where any feedback ratio mismatch creates a balanced, differential error around the Vocm output.

The terms that create a differential error from a common-mode term and feedback ratio mismatch include the desired Vocm voltage, any source common-mode voltage, any drift on the reference bias to the Vocm control pin, and any internal offset and drift in the Vocm control path.

Considering just the output common-mode control and the source common-mode voltage (Vicm), the conversion to output differential offsets is done by using 式 4:

$$\text{Vod} = \frac{\text{Vocm}(\text{G1} - \text{G2}) - \text{Vicm}(\text{G1} - \text{G2})}{1 + \frac{\text{G1} + \text{G2}}{2}} \tag{4}$$

Neglecting any G1 and G2 mismatch because of standard values snap, the conversion gain for these two terms can be recast in terms of the nominal Rf / Rg ≡ G, and tolerance T, as shown in 式 5. As G increases, this conversion gain approaches 4T, as a worst-case gain for these terms to output differential offset.

$$\frac{\text{Vod}}{\text{Vocm}} = \frac{\text{G}}{(1 + \text{G})} \bullet \frac{4T}{(1 - T^2)} \tag{5}$$

This conversion gain to differential output error is applied to two error terms: Vocm, assuming the input control pin is driven and not floating, and the source Vicm voltage. The source common-mode voltage is assumed to be 0 V in this example. If not, apply this gain to the source common-mode value or range in the intended application.

As a full example of using these terms to estimate the worst-case output 25°C error band, and then the worst-case drift (by adding all the error terms together independently), use the gain of 2 V/V configuration of 図 7-3 with Rf = 402 Ω, and assume ±1% tolerance on the resistors with the standard values used in 図 7-9.

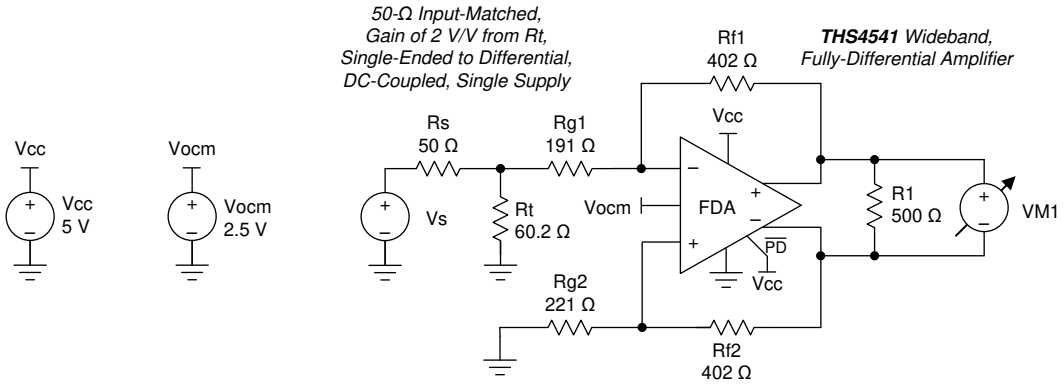


図 7-9. DC-Coupled Gain of 2 with Rf = 402 Ω and a Single-Ended to Differential Matched Input 50-Ω Impedance

The standard value snap on the signal-input side actually produces added G mismatch along with the resistor tolerances. For 図 7-9, G2 = 402 / 221 = 1.819; and G1 = 402 / 218.3 = 1.837 nominally, with a ±2% tolerance around this initial mismatch for G2 and G1, if 1% resistors are used.

Using the maximum 25°C error terms, and a nominal 2.5-V input to the Vocm control pin, gives 表 7-3 with the error terms, the gains to the output differential error (Vod), and then the summed output error band at 25°C.

表 7-3. Worst-Case Output Vod Error Band

ERROR TERM	25°C MAXIMUM VALUE	GAIN TO Vod	OUTPUT ERROR
Input Vio	±0.45 mV	2.85 V/V	±1.2825 mV
Input Ios	±0.5 µA	402 Ω	±0.201 mV
Input Ibcm, Rf mismatch	13 µA	±8.04 Ω	±0.105 mV
Vocm input, G mismatch	2.5 V	±0.0322	±80.5 mV
		Total	±82.09 mV

The 0.03222 conversion gain for the G ratio mismatch is the worst case, starting from the initially higher G1 value because of standard value snap, and using a ±1% tolerance on the Rf and Rg elements of that ratio. The actual Vocm conversion gain range is not symmetric, but is shown that way here. The initial 25°C worst-case error band is dominated by the Vocm conversion to Vod through the feedback resistor ratio mismatch. Improve this G match and tolerances to reduce this term.

Normally, the expected drift in the output Vod is of more interest than an initial error band. 表 7-4 shows these terms and the summed results, adding all the terms independently to obtain a worst-case drift.

表 7-4. Worst-Case Output Vod Drift Band

ERROR TERM	DRIFT MAXIMUM VALUE	GAIN TO Vod	OUTPUT ERROR
Input Vio	±2.4 µV/°C	2.85 V/V	±6.84 µV/°C
Input Ios	±1.3 nA/°C	402 Ω	±0.522 µV/°C
Input Ibcm, Rf mismatch	15 nA/°C	±8.04 Ω	±0.121 µV/°C
Vocm input, G mismatch	±12 µV/°C	±0.0322	±0.386 µV/°C
		Total	±7.86 µV/°C

In this calculation, the input offset voltage drift dominates the output differential offset drift. For the last term, the drift for the Vocm path is just for the internal offset drift of the common-mode path. Make sure to also consider the added external drift on the source of the Vocm input.

The absolute accuracy and drift for the THS4541-Q1 are exceptionally good. Mismatched resistor feedback ratios combined with a high drift in the Vocm control input can actually dominate the output Vod drift. Where the output differential precision is more important than the input matching accuracy, consider matching the networks on the two input sides to achieve improved nominal G1 to G2 match. The gains for the input bias current error terms are relatively low in this example design using 402-Ω feedback values. Higher Rf values give these terms more gain. A less conservative estimate of output drift considers the terms to be uncorrelated and RMS half of each terms worst-case span shown in 表 7-4. Performing this calculation for this example estimates a less conservative output offset drift of ±3.42 µV/°C; essentially, half the worst-case span of the input offset drift term. Follow these steps to estimate the output differential offset and drift for any external configuration.

7.5 Noise Analysis

The first step in the output noise analysis is to reduce the application circuit to the simplest form with equal feedback and gain setting elements to ground, as shown in 図 7-10, with the FDA and resistor noise terms to be considered.

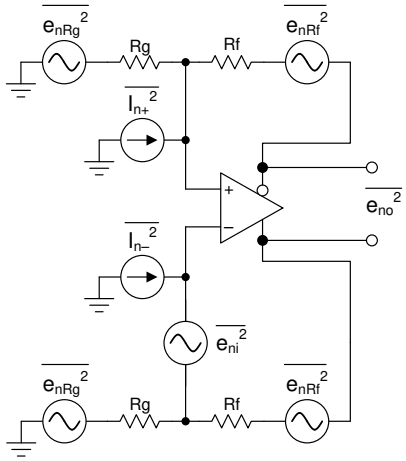


図 7-10. FDA Noise-Analysis Circuit

The noise powers are shown for each term. When the Rf and Rg terms are matched on each side, the total differential output noise is the RSS of these separate terms. Using NG ≡ 1 + Rf / Rg, the total output noise is given by 式 6. Each resistor noise term is a 4k*T*R power.

$$e_{no} = \sqrt{(e_{ni}NG)^2 + 2(i_nRf)^2 + 2(4kTRfNG)} \quad (6)$$

The first term is simply the differential input spot noise times the noise gain. The second term is the input current noise terms times the feedback resistor (and because there are two terms, the power is two times one of the terms). The last term is the output noise resulting from both the Rf and Rg resistors, again times two, for the output noise power of each side added together. Using the exact values for a 50-Ω, matched, single-ended to differential gain, sweep with a fixed Rf = 402 Ω (see 表 8-1) and the intrinsic noise e_{ni} = 2.2 nV and I_n = 1.9 pA for the THS4541-Q1, gives an output spot noise from 式 6. Then, dividing by the signal gain (Av) gives the input-referred, spot-noise voltage (e_i) shown in 表 7-5.

表 7-5. Swept Gain Output and Input-Referred, Spot-Noise Calculations

Av(1)	Rt, EXACT (Ω)	Rg1, EXACT (Ω)	Rg2, EXACT (Ω)	NOISE GAIN	e_{no} (nV/√Hz)	e_i (nV/√Hz)
1	55.2	399	425	1.94	6.64	6.64
2	60.1	191	218	2.85	8.71	4.36
3	65.6	124	153	3.63	10.7	3.56
4	72	89.7	119	4.37	12.1	3.03
5	79.7	67.8	98.3	5.09	13.7	2.74
6	89.1	54.2	86.5	5.65	15.4	2.56
7	101	43.2	76.6	6.25	16.7	2.39
8	117	35.2	70.1	6.74	17.3	2.16
9	138	29.0	65.8	7.11	18.6	2.06
10	170	23.6	62.5	7.44	18.9	1.89
11	220	18.7	59.3	7.78	19.6	1.78
12	313	14.6	57.7	7.97	20.0	1.66
13	545	10.8	56.6	8.11	20.3	1.56
14	2209	7.26	56.1	8.16	21.1	1.50

(1) Rf = 402 Ω.

Notice that the input-referred e_i is less than 2.2 nV/√Hz for just the THS4541-Q1 above a gain of 7 V/V. This result is because NG is less than Av when the source impedance is included in the NG calculation.

7.6 Factors Influencing Harmonic Distortion

As shown in the swept frequency harmonic distortion plots, the THS4541-Q1 provides extremely low distortion at lower frequencies. In general, FDA output harmonic distortion mainly relates to the open-loop linearity in the output stage corrected by the loop gain at the fundamental frequency. As the total load impedance decreases (including the effect of the feedback resistor elements in parallel for loading purposes), the output-stage, open-loop linearity degrades, increasing the harmonic distortion, as illustrated in 図 6-16 and 図 6-34. As the output voltage swings increase, very fine-scale, open-loop, output-stage nonlinearities increase, also degrading the harmonic distortion, as illustrated in 図 6-14 and 図 6-32. Conversely, decreasing the target output voltage swings drops the distortion terms rapidly. For harmonic-distortion testing, 2 V_{PP} is used as a nominal swing because this value represents a typical ADC, full-scale, differential input range.

Increasing the gain acts to decrease the loop gain, resulting in the increasing harmonic distortion terms, as illustrated in 図 6-18 and 図 6-36. One advantage to the capacitive compensation for the attenuator design (described in the *セクション 9.2.1* typical application example) is that the noise gain is shaped up with frequency to achieve a crossover at an acceptable phase margin at higher frequencies. This compensation holds the loop gain high at frequencies lower than the noise-gain zero, improving distortion in these lower bands.

Anything that moves the output pin voltage swings close to clipping into the supplies rapidly degrades harmonic distortion. Output clipping can occur from either absolute differential swing, or the swing can be moved closer to the supplies with the common-mode control. This effect is illustrated in 図 6-17 and 図 6-35.

The THS4541-Q1 does an exceptional job of converting from single-ended inputs to differential outputs with very low harmonic distortions. External resistors of 1% tolerance are used in characterization with good results. Imbalancing the feedback divider ratios does not degrade distortion directly. Imbalanced feedback ratios convert common-mode inputs to differential mode at the outputs with the gain described in the *セクション 7.4* section.

7.7 Driving Capacitive Loads

A very common requirement is driving the capacitive load of an ADC or some other next stage device. Directly driving a capacitive load with a closed-loop amplifier such as the THS4541-Q1 can lead to an unstable response, as shown in the step response plots into a capacitive load (see 図 6-8 and 図 6-26). One typical remedy for this instability is to add two small series resistors (Ro in 図 7-11) at the outputs of the THS4541-Q1. 図 6-6 and 図 6-24 provide parametric plots of recommended Ro values versus differential capacitive load values and gain.

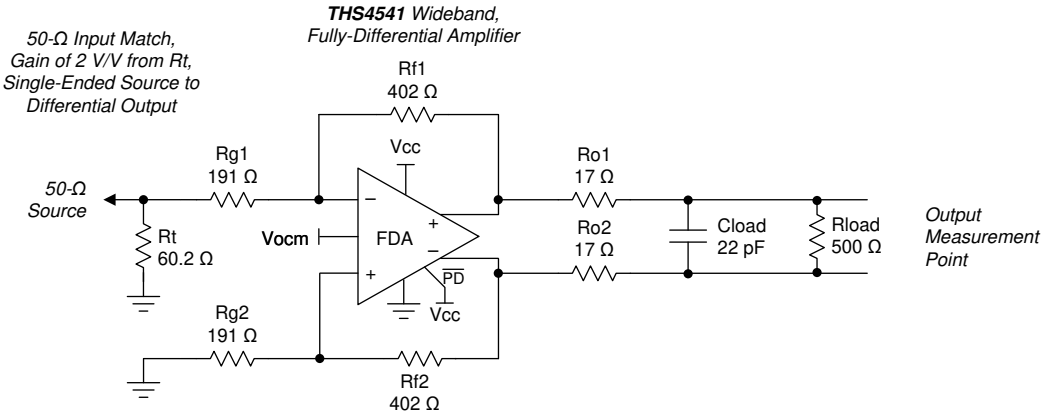


図 7-11. Including Ro When Driving Capacitive Loads

Operating at higher gains requires lower Ro values to achieve a ±0.5-dB flat response for the same capacitive load. Some direct parasitic loading is acceptable with no series Ro that increases with gain setting, as illustrated in 図 6-6 and 図 6-24 where the Ro value is 0 Ω. Even when these plots suggest no series Ro is required, good practice is to include a place for the Ro elements in the board layout (0-Ω load initially) for later adjustment, in case the response appears unacceptable. The TINA simulation model does a good job of predicting this effect and showing the impact for different choices of capacitive load isolating resistors (Ro).

7.8 Thermal Analysis

The relatively low internal quiescent power dissipation for the THS4541-Q1, combined with the excellent thermal impedance of the 16-pin VQFN (RGT) package, limits the possibility of excessively-high, internal-junction temperatures.

To estimate the internal junction temperature (T_J), an estimate of the maximum internal power dissipation (P_D) is first required. There are two pieces to the internal power dissipation: quiescent current power and the power used in the output stage to deliver load current. To simplify the latter, the worst-case, output-stage power is driving a dc differential voltage across a load using half the total supply voltage. As an example:

1. Assume a worst-case, 5% high 5-V supply. This 5.25-V supply with a maximum I_{CC} of 11 mA gives a quiescent power term = 58 mW.
2. Assume a 100-Ω differential load with a static 2.5-V differential voltage established across the load. This 25 mA of dc load current generates a maximum output stage power of (5.25 V – 2.5 V) × 25 mA = 69 mW.
3. From this total worst-case internal P_D = 127 mW, multiply times the 52°C/W thermal impedance to get a 7°C rise from ambient.

Even for this extreme condition and the maximum rated ambient temperature of 125°C, the junction temperature is a maximum 132°C (less than the rated absolute maximum of 150°C). Follow this same calculation sequence for the exact application and package selected to predict the maximum T_J.

8 Detailed Description

8.1 Overview

The THS4541-Q1 is a voltage-feedback (VFA) based, fully-differential amplifier (FDA) offering greater than 500-MHz, small-signal bandwidth at a gain of 2 V/V with trimmed supply current and input offset voltage. The core differential amplifier is a slightly decompensated voltage-feedback design with a high slew-rate, precision input stage. This design gives the 500-MHz gain of 2-V/V small-signal bandwidth shown in the characterization curves, with a 1500-V/µs slew rate, yielding approximately a 340-MHz, 2-V_{PP}, large-signal bandwidth in the same circuit configuration.

The outputs offer near rail-to-rail output swing (0.2-V headroom to either supply), while the device inputs are negative rail inputs with approximately 1.2 V of headroom required to the positive supply. This negative rail input directly supports a bipolar input around ground in a DC-coupled, single-supply design (see 図 7-3). Similar to all FDA devices, the output average voltage (common-mode) is controlled by a separate common-mode loop. The target for this output average is set by the Vocm input pin that can be either floated to default near midsupply or driven to a desired output common-mode voltage. The Vocm range extends from a very low 0.91 V greater than the negative supply to 1.1 V less than the positive supply, supporting a wide range of modern analog-to-digital converter (ADC) input common-mode requirements using a single 2.7-V to 5.4-V supply range for the THS4541-Q1.

A power-down pin ($\overline{PD}$) is included. Pull the $\overline{PD}$ pin voltage to the negative supply to turn the device off, putting the THS4541-Q1 into a very-low quiescent current state. For normal operation, the $\overline{PD}$ pin must be asserted high. When the device is disabled, remember that the signal path is still present through the passive external resistors. Input signals applied to a disabled THS4541-Q1 still appear at the outputs at some level through this passive resistor path as is the case for any disabled FDA device.

8.1.1 Terminology and Application Assumptions

Like all widely-used devices, numerous common terms have developed that are unique to this type of device. These terms include:

- Fully differential amplifier (FDA)—In this document, this term is restricted to devices offering what appears similar to a differential inverting op amp design element that requires an input resistor (not high-impedance input) and includes a second internal control-loop setting the output average voltage (Vocm) to a default or set point. This second loop interacts with the differential loop in some configurations.
- The desired output signal at the two output pins is a *differential* signal swinging symmetrically around a *common-mode* voltage where that is the average voltage for the two outputs.
- Single-ended to differential—always use the outputs differentially in an FDA; however, the source signal can be either a single-ended source or differential, with a variety of implementation details for either. When the FDA operation is single-ended to differential, only one of the two input resistors receives the source signal with the other input resistor connected to a dc reference (often ground) or through a capacitor to ground.

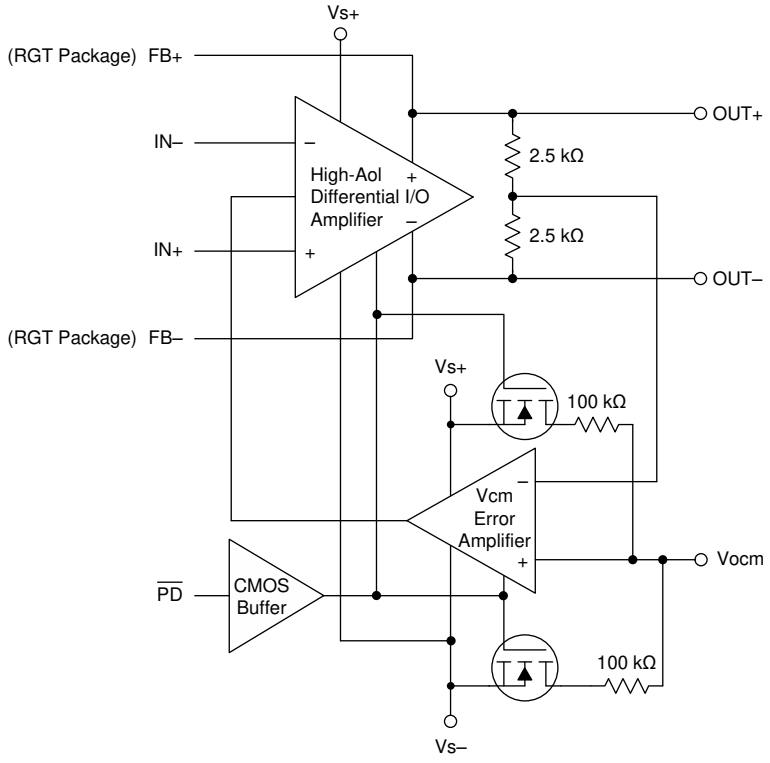
To simplify, several features in the application of the THS4541-Q1 are not explicitly stated, but are necessary for correct operation. These requirements include:

- Good power-supply decoupling is required. Minimize the distance (< 0.1") from the power-supply pins to high-frequency, 0.1-µF decoupling capacitors. Often a larger capacitor (2.2 µF is typical) is used along with a high-frequency, 0.1-µF supply decoupling capacitor at the device supply pins (share this capacitor for the four supply pins in the package). For single-supply operation, only the positive supply has these capacitors. When a split supply is used, use these capacitors for each supply to ground. If necessary, place the larger capacitors somewhat farther from the device and share these capacitors among several devices in the same area of the printed circuit board (PCB). For each THS4541-Q1, attach a separate 0.1-µF capacitor to a nearby ground plane. With cascaded or multiple parallel channels, including ferrite beads from the larger capacitor is often useful to the local high-frequency decoupling capacitor.
- Minimize the distance (< 0.1") from the power-supply pins to high-frequency, 0.1-µF decoupling capacitors. At the device pins, the ground and power plane layout must not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling

capacitors. Always decouple the power-supply connections (on pins 4 and 7) with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) improves 2nd-harmonic distortion performance. Use larger (2.2 µF to 6.8 µF) decoupling capacitors, effective at lower frequency, on the main supply pins. Place these capacitors somewhat farther from the device. These capacitors can be shared among several devices in the same area of the PCB.

- Although not always stated, tie the power disable pin to the positive supply when only an enabled channel is desired.
- Virtually all ac characterization equipment expects a 50-Ω termination from the 50-Ω source, and a 50-Ω single-ended source impedance from the device outputs to the 50-Ω sensing termination. This termination is achieved in all characterizations (often with some insertion loss), but is not necessary for most applications. Matching impedance is most often required when transmitting over longer distances. Tight layouts from a source, through the THS4541-Q1, and on to an ADC input do not require doubly-terminated lines or filter designs; the exception is if the source requires a defined termination impedance for correct operation (for example, a SAW filter source).
- The amplifier signal path is flexible for single or split-supply operation. Most applications are intended to be single supply, but any split-supply design can be used, as long as the total supply across the TH4541-Q1 is less than 5.5 V and the required input, output, and common-mode pin headrooms to each supply are observed. Left open, the Vocm pin defaults to near midsupply for any combination of split or single supplies used. The disable pin is negative-rail referenced. Using a negative supply requires the disable pin to be pulled down to within 0.7 V of the negative supply to disable the amplifier.
- External element values are normally assumed to be accurate and matched. In an FDA, match the feedback resistor values and also match the (dc and ac) impedance from the summing junctions to the source on one side and the reference or ground on the other side. Unbalancing these values introduces nonidealities in the signal path. For the signal path, imbalanced resistor ratios on the two sides create a common-mode to differential conversion. Also, mismatched Rf values and feedback ratios create some added differential output error terms from any common-mode dc, ac signal, or noise terms. Snapping to standard 1% resistor values is a typical approach and generally leads to some nominal feedback ratio mismatch. Mismatched resistors or ratios do not in themselves degrade harmonic distortion. If there is meaningful CM noise or distortion coming in, those errors are converted to a differential error through element or ratio mismatch.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Differential I/O

The THS4541-Q1 combines a core differential I/O, high-gain block with an output common-mode sense that is compared to a reference voltage and then fed back into the main amplifier block to control the average output to that reference. The differential I/O block is a classic, high open-loop gain stage with a dominant pole at approximately 900 Hz. This voltage feedback structure projects a single-pole, unity-gain Aol at 850 MHz (gain bandwidth product). The high-speed differential outputs include an internal averaging resistor network to sense the output common-mode voltage. This voltage is compared by a separate Vcm error amplifier to the voltage on the Vocm pin. If floated, this reference is at half the total supply voltage across the device using two 100-kΩ resistors. This Vcm error amplifier transmits a correction signal into the main amplifier to force the output average voltage to meet the target voltage on the Vocm pin. The bandwidth of this error amplifier is approximately the same bandwidth as the main differential I/O amplifier.

The differential outputs are collector outputs to obtain the rail-to-rail output swing. These outputs are relatively high-impedance, open-loop sources; however, closing the loop provides a very low output impedance for load driving. No output current limit or thermal shutdown features are provided in this lower-power device. The differential inputs are PNP inputs to provide a negative-rail input range.

To operate the THS4541-Q1 , connect external resistors from the FB– pin to the IN+ pins, and the FB+ pin to the IN– pins. Bring in the inputs through additional resistors to the IN+ and IN– pins. The differential I/O op amp operates similarly to an inverting op amp structure where the source must drive the input resistor and the gain is the ratio of the feedback to the input resistor.

8.3.2 Power-Down Control Pin ($\overline{PD}$)

The THS4541-Q1 includes a power-down control pin, $\overline{PD}$. This pin must be asserted high for correct amplifier operation. The $\overline{PD}$ pin cannot be floated because there is no internal pullup or pulldown resistor on this pin to reduce disabled power consumption. Asserting this pin low (within 0.7 V of the negative supply) puts the THS4541-Q1 into a very low quiescent state (approximately 2 µA). Switches in the default Vocm resistor string open to eliminate the fixed bias current (25 µA) across the supply in this 200-kΩ voltage divider to midsupply.

8.3.2.1 Operating the Power Shutdown Feature

Assert this CMOS input pin to the desired voltage for operation. For applications that require the device to only be powered on when the supplies are present, tie the $\overline{PD}$ pin to the positive supply voltage.

When the $\overline{PD}$ pin is somewhat below the positive supply pin, slightly more quiescent current is drawn; see 図 6-56. For the minimum-on power, assert this pin to the positive supply.

The disable operation is referenced from the negative supply; normally, ground. For split-supply operation, with the negative supply below ground, a disable control voltage below ground is required to turn the THS4541-Q1 off when the negative supply exceeds –0.7 V.

For single-supply operation, a minimum of 1.7 V greater than the negative supply (ground, in this case) is required to maintain operation. This minimum logic-high level allows for direct operation from 1.8-V supply logic.

8.3.3 Input Overdrive Operation

The THS4541-Q1 input stage architecture is intrinsically robust to input overdrives with the series input resistor required by all applications. High input overdrives cause the outputs to limit into the maximum swings with the remaining input current through the Rg resistors absorbed by internal, back-to-back protection diodes across the two inputs. These diodes are normally off in application, and only turn on to absorb the currents that a large input overdrive can produce through the source impedance and or the series Rg elements required by all designs. 図 6-12 and 図 6-30 illustrate the exceptional output limiting and short recovery time for an input overdrive that is attempting to drive the outputs to two times the available swing.

The internal input diodes can safely absorb up to ±15 mA in an overdrive condition. For designs that require more current to be absorbed, consider adding an external protection diode such as the BAV99 device used in the example ADC interface design of 図 9-4.

8.4 Device Functional Modes

This wideband FDA requires external resistors for correct signal-path operation. When configured for the desired input impedance and gain setting with these external resistors, the amplifier can be either *on* with the $\overline{PD}$ pin asserted to a voltage greater than (Vs–) + 1.7 V, or turned *off* by asserting $\overline{PD}$ low. Disabling the amplifier shuts off the quiescent current and stops correct amplifier operation. The signal path is still present for the source signal through the external resistors.

The Vocm control pin sets the output average voltage. If left open, Vocm defaults to an internal midsupply value. Driving this high-impedance input with a voltage reference within the valid range sets a target for the internal Vcm error amplifier.

8.4.1 Operation from Single-Ended Sources to Differential Outputs

One of the most useful features supported by the FDA device is an easy conversion from a single-ended input to a differential output centered on a user-controlled, common-mode level. While the output side is relatively straightforward, the device input pins move in a common-mode sense with the input signal. This common-mode voltage at the input pins moving with the input signal acts to increase the apparent input impedance to be greater than the Rg value. This input active impedance issue applies to both ac- and dc-coupled designs, and requires somewhat more complex solutions for the resistors to account for this active impedance, as shown in the following subsections.

8.4.1.1 AC-Coupled Signal Path Considerations for Single-Ended Input to Differential Output Conversion

When the signal path can be ac coupled, the dc biasing for the THS4541-Q1 becomes a relatively simple task. In all designs, start by defining the output common-mode voltage. The ac-coupling issue can be separated for the input and output sides of an FDA design. The input can be ac coupled and the output dc coupled, or the output can be ac coupled and the input dc coupled, or both can be ac coupled. One situation where the output can be dc coupled (for an ac-coupled input), is when driving directly into an ADC where the Vocm control voltage uses the ADC common-mode reference to directly bias the FDA output common-mode to the required ADC input common-mode. In any case, the design starts by setting the desired Vocm. When an ac-coupled path follows the output pins, the best linearity is achieved by operating Vocm at midsupply. The Vocm voltage must be within the linear range for the common-mode loop, as specified in the headroom specifications (approximately 0.91 V greater than the negative supply and 1.1 V less than the positive supply). If the output path is also ac coupled, simply letting the Vocm control pin float is usually preferred to get a midsupply default Vocm bias with minimal elements. To limit noise, place a 0.1-µF decoupling capacitor on the Vocm pin to ground.

After Vocm is defined, check the target output voltage swing to confirm that the Vocm plus the positive or negative output swing on each side does not clip into the supplies. If the desired output differential swing is defined as Vopp, divide by 4 to obtain the ±Vp swing around Vocm at each of the two output pins (each pin operates 180° out of phase with the other). Check that Vocm ±Vp does not exceed the absolute supply rails for this rail-to-rail output (RRO) device.

Going to the device input pins side, because both the source and balancing resistor on the nonsignal input side are dc blocked (see 図 7-1), no common-mode current flows from the output common-mode voltage, thus setting the input common-mode equal to the output common-mode voltage.

This input headroom also sets a limit for higher Vocm voltages. Because the input Vicm is the output Vocm for ac-coupled sources, the 1.2-V minimum headroom for the input pins to the positive supply overrides the 1.1-V headroom limit for the output Vocm. Also, the input signal moves this input Vicm around the dc bias point, as described in the *セクション 8.4.1.3* section.

8.4.1.2 DC-Coupled Input Signal Path Considerations for Single-Ended to Differential Conversion

The output considerations remain the same as for the ac-coupled design. Again, the input can be dc coupled while the output is ac coupled. A dc-coupled input with an ac-coupled output can have some advantages to move the input Vicm down if the source is ground referenced. When the source is dc coupled into the THS4541-Q1 (see 図 7-3), both sides of the input circuit must be dc coupled to retain differential balance. Normally, the nonsignal input side has an Rg element biased to whatever the source midrange is expected to be. Providing

this midscale reference gives a balanced differential swing around Vocm at the outputs. Often, Rg2 is simply grounded for dc-coupled, bipolar-input applications. This configuration gives a balanced differential output if the source is swinging around ground. If the source swings from ground to some positive voltage, grounding Rg2 gives a unipolar output differential swing from both outputs at Vocm (when the input is at ground) to one polarity of swing. Biasing Rg2 to an expected midpoint for the input signal creates a differential output swing around Vocm.

One significant consideration for a dc-coupled input is that Vocm sets up a common-mode bias current from the output back through Rf and Rg to the source on both sides of the feedback. Without input balancing networks, the source must sink or source this dc current. After the input signal range and biasing on the other Rg element is set, check that the voltage divider from Vocm to Vin through Rf and Rg (and possibly Rs) establishes an input Vicm at the device input pins that is in range. If the average source is at ground, the negative rail input stage for the THS4541-Q1 is in range for applications using a single positive supply and a positive output Vocm setting because this dc current lifts the average FDA input summing junctions up off of ground to a positive voltage (the average of the V+ and V– input pin voltages on the FDA).

8.4.1.3 Resistor Design Equations for the Single-Ended to Differential Configuration of the FDA

The design equations for setting the resistors around an FDA to convert from a single-ended input signal to differential output can be approached from several directions. Here, several critical assumptions are made to simplify the results:

- The feedback resistors are selected first and set equal on the two sides.
- The dc and ac impedances from the summing junctions back to the signal source and ground (or a bias voltage on the nonsignal input side) are set equal to retain feedback divider balance on each side of the FDA

Both of these assumptions are typical and aimed to delivering the best dynamic range through the FDA signal path.

After the feedback resistor values are chosen, the aim is to solve for the Rt (a termination resistor to ground on the signal input side), Rg1 (the input gain resistor for the signal path), and Rg2 (the matching gain resistor on the nonsignal input side); see 図 7-1 and 図 7-3. The same resistor solutions can be applied to either ac- or dc-coupled paths. Adding blocking capacitors in the input-signal chain is a simple option. Adding these blocking capacitors after the Rt element (as shown in 図 7-1) has the advantage of removing any dc currents in the feedback path from the output Vocm to ground.

Earlier approaches to the solutions for Rt and Rg1 (when the input must be matched to a source impedance, Rs) follow an iterative approach. This complexity arises from the active input impedance at the Rg1 input. When the FDA is used to convert a single-ended signal to differential, the common-mode input voltage at the FDA inputs must move with the input signal to generate the inverted output signal as a current in the Rg2 element. A more recent solution is shown as 式 7, where a quadratic in Rt can be solved for an exact required value. This quadratic emerges from the simultaneous solution for a matched input impedance and target gain. The only inputs required are:

1. The selected Rf value.
2. The target voltage gain (Av) from the input of Rt to the differential output voltage.
3. The desired input impedance at the junction of Rt and Rg1 to match Rs.

Solving this quadratic for Rt starts the solution sequence, as shown in 式 7.

$$Rt^2 - Rt\frac{2Rs\left(2Rf + \frac{Rs}{2}Av^2\right)}{2Rf\left(2 + Av\right) - RsAv(4 + Av)} - \frac{2RfRs^2Av}{2Rf\left(2 + Av\right) - RsAv(4 + Av)} = 0 \quad (7)$$

Being a quadratic, there are limits to the range of solutions. Specifically, after Rf and Rs are chosen, there is physically a maximum gain beyond which 式 7 starts to solve for negative Rt values (if input matching is a requirement). With Rf selected, use 式 8 to verify that the maximum gain is greater than the desired gain.

$$Av_{max} = \left(\frac{Rf}{Rs} - 2\right) \bullet \left[1 + \sqrt{1 + \frac{4\frac{Rf}{Rs}}{\left(\frac{Rf}{Rs} - 2\right)^2}}\right] \quad (8)$$

If the achievable Av_{max} is less than desired, increase the Rf value. After Rt is derived from 式 7, the Rg1 element is given by 式 9:

$$Rg1 = \frac{2\frac{Rf}{Av} - Rs}{1 + \frac{Rs}{Rt}} \quad (9)$$

Then, the simplest approach is to use a single Rg2 = Rt || Rs + Rg1 on the nonsignal input side. Often, this approach is shown as the separate Rg1 and Rs elements. Using these separate elements provides a better divider match on the two feedback paths, but a single Rg2 is often acceptable. A direct solution for Rg2 is given as 式 10:

$$Rg2 = \frac{2\frac{Rf}{Av}}{1 + \frac{Rs}{Rt}} \quad (10)$$

This design proceeds from a target input impedance matched to Rs, signal gain Av from the matched input to the differential output voltage, and a selected Rf value. The nominal Rf value chosen for the THS4541-Q1 characterization is 402 Ω. As discussed previously, going lower improves noise and phase margin, but reduces the total output load impedance possibly degrading harmonic distortion. Going higher increases the output noise, and can reduce the loop-phase margin because of the feedback pole to the input capacitance, but reduces the total loading on the outputs. Using 式 8 to 式 10 to sweep the target gain from 1 to Av_{max} < 14.3 V/V gives 表 8-1, which shows exact values for Rt, Rg1, and Rg2, where a 50-Ω source must be matched while setting the two feedback resistors to 402 Ω. One possible solution for 1% standard values is shown, and the resulting actual input impedance and gain with % errors to the targets are also shown in 表 8-1.

表 8-1. Required Resistors for a Single-Ended to Differential FDA Design Stepping Gain From 1 V/V to 14 V/V

Av(1)	Rt, EXACT (Ω)	Rt 1%	Rg1, EXACT (Ω)	Rg1 1%	Rg2, EXACT (Ω)	Rg2 1%	ACTUAL Z_{IN}	%ERR TO Rs	ACTUAL GAIN	%ERR TO Av
1	55.2	54.9	395	392	421	422	49.731	–0.54%	1.006	0.62%
2	60.1	60.4	193	191	220	221	50.171	0.34%	2.014	0.72%
3	65.6	64.9	123	124	151	150	49.572	–0.86%	2.983	–0.57%
4	72.0	71.5	88.9	88.7	118	118	49.704	–0.59%	4.005	0.14%
5	79.7	80.6	68.4	68.1	99.2	100	50.451	0.90%	5.014	0.28%
6	89.1	88.7	53.7	53.6	85.7	86.6	49.909	–0.18%	6.008	0.14%
7	101	102	43.5	43.2	77.1	76.8	50.179	0.36%	7.029	0.42%
8	117	118	35.5	35.7	70.6	69.8	50.246	0.49%	7.974	–0.32%
9	138	137	28.8	28.7	65.4	64.9	49.605	–0.79%	9.016	0.18%
10	170	169	23.5	23.7	62.0	61.9	50.009	0.02%	9.961	–0.39%
11	220	221	18.8	18.7	59.6	59.0	49.815	–0.37%	11.024	0.22%
12	313	316	14.7	14.7	57.9	57.6	50.051	0.10%	11.995	–0.04%
13	545	549	10.9	11.0	56.7	56.2	49.926	–0.15%	12.967	–0.25%
14	2209	2210	7.26	7.32	56.2	56.2	50.079	0.16%	13.986	–0.10%

(1) Rf = 402 Ω, Rs = 50 Ω, and Av_{MAX} = 14.32 V/V.

These equations and design flow apply to any FDA. Using the feedback resistor value as a starting point is particularly useful for current-feedback-based FDAs such as the LMH6554, where the value of these feedback resistors determines the frequency response flatness. Similar tables can be built using the equations provided here for other source impedances, Rf values, and gain ranges.

Note the extremely low Rg1 values at the higher gains. For instance, at a gain of 14 V/V, that 7.32-Ω standard value is transformed by the action of the common-mode loop moving the input common-mode voltage to appear like a 50-Ω input match. This active input impedance provides an improved input-referred noise at higher gains; see also セクション 7.5. The TINA model correctly shows this actively-set input impedance in the single-ended to differential configuration, and is a good tool to validate the gains, input impedances, response shapes, and noise issues.

8.4.1.4 Input Impedance for the Single-Ended to Differential FDA Configuration

The designs so far have included a source impedance, Rs, that must be matched by Rt and Rg1. The total impedance at the junction of Rt and Rg1 for the circuit of 図 7-3 is the parallel combination of Rt to ground, and the ZA (active impedance) presented by Rg1. The expression for ZA, assuming Rg2 is set to obtain the differential divider balance, is given by 式 11:

$$ZA = Rg1\frac{\left(1+\frac{Rg1}{Rg2}\right)\left(1+\frac{Rf}{Rg1}\right)}{2+\frac{Rf}{Rg2}} \tag{11}$$

For designs that do not need impedance matching, but instead come from the low impedance output of another amplifier for instance, Rg1 = Rg2 is the single-to-differential design used without an Rt to ground. Setting Rg1 = Rg2 = Rg in 式 11 gives the input impedance of a simple input FDA driving from a low-impedance, single-ended source to a differential output as shown in 式 12:

$$ZA = 2Rg\frac{1+\frac{Rf}{Rg}}{2+\frac{Rf}{Rg}} \tag{12}$$

In this case, setting a target gain as Rf / Rg ≡ α, and then setting the desired input impedance, allows the Rg element to be resolved first, and then the required Rf to get the gain. For example, targeting an input impedance of 200 Ω with a gain of 4 V/V, 式 13 gives the physical Rg element. Multiplying this required Rg value by a gain of 4 gives the Rf value and the design of 図 8-1.

$$Rg = ZA\frac{2+\alpha}{2(1+\alpha)} \tag{13}$$

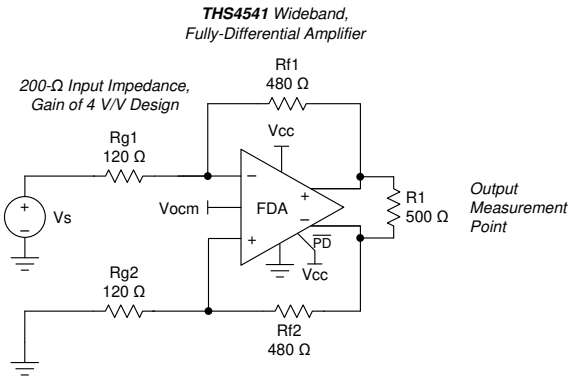


図 8-1. 200-Ω Input Impedance, Single-Ended to Differential DC-Coupled Design with Gain of 4 V/V

After being designed, this circuit can also be ac coupled by adding blocking caps in series with the two 120-Ω Rg resistors. This active input impedance has the advantage of increasing the apparent load to the prior stage using lower resistors values, leading to lower output noise for a given gain target.

8.4.2 Differential-Input to Differential-Output Operation

In many ways, this method is a much simpler way to operate the FDA from a design equations perspective. Again, assuming the two sides of the circuit are balanced with equal Rf and Rg elements, the differential input impedance is now just the sum of the two Rg elements to a differential inverting summing junction. In these designs, the input common-mode voltage at the summing junctions does not move with the signal, but must be dc biased in the allowable range for the input pins with consideration given to the voltage headroom required from each supply. Slightly different considerations apply to ac- or dc-coupled, differential-in to differential-out designs, as described in the following sections.

8.4.2.1 AC-Coupled, Differential-Input to Differential-Output Design Issues

There are two typical ways to use the THS4541-Q1 with an ac-coupled differential source. In the first method, the source is differential and can be coupled in through two blocking capacitors. The second method uses either a single-ended or a differential source and couples in through a transformer (or balun). 図 8-2 shows a typical blocking capacitor approach to a differential input. An optional input differential termination resistor (Rm) is included in this design. This Rm element allows the input Rg resistors to be scaled up while still delivering lower differential input impedance to the source. In this example, the Rg elements sum to show a 200-Ω differential impedance, while the Rm element combines in parallel to give a net 100-Ω, ac-coupled, differential impedance to the source. Again, the design proceeds by selecting the Rf element values, then the Rg to set the differential gain, then an Rm element (if needed) to achieve a target input impedance. Alternatively, the Rm element can be eliminated, the Rg elements set to the desired input impedance, and Rf set to the get the differential gain (= Rf / Rg).

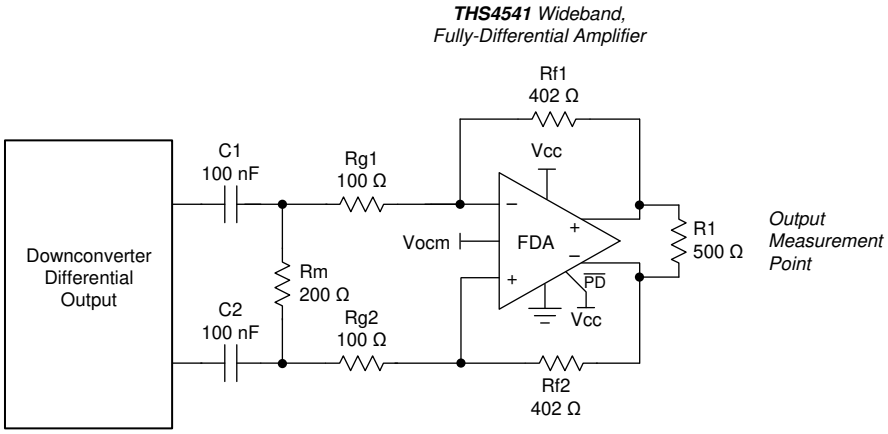


図 8-2. Example Down-Converting Mixer Delivering an AC-Coupled Differential Signal to the THS4541-Q1

The dc biasing here is very simple. The output Vocm is set by the input control voltage and, because there is no dc current path for the output common-mode voltage, that dc bias also sets the input pins common-mode operating points.

Transformer input coupling allows either a single-ended or differential source to be coupled into the THS4541-Q1; possibly also improving the input-referred noise figure. These designs assume a source impedance that must be matched in the balun interface. The simplest approach is shown in 図 8-3, where an example 1:2 turns ratio step-up transformer is used from a 50-Ω source.

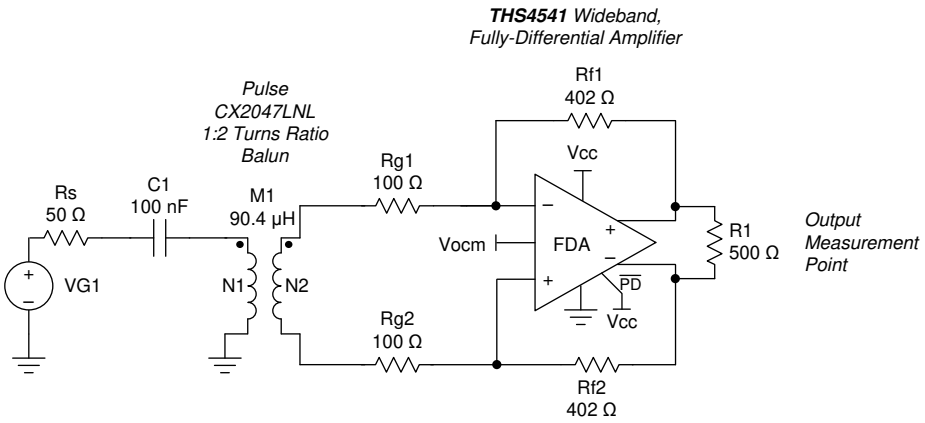


図 8-3. Input Balun Interface Delivers a Differential Input to the THS4541-Q1

In this example, this 1:2 turns ratio step-up transformer provides a source and load match from the 50-Ω source if the secondary is terminated in 200 Ω (turns-ratio squared is the impedance ratio across a balun). The two Rg elements provide that termination as the elements sum to the differential virtual ground at the FDA summing junctions. The input blocking cap (C1) is optional and included only to eliminate dc shorts to ground from the source. This solution often improves the input-referred noise figure more so than just the FDA using this passive (zero power dissipation) input balun. Defining a few ratios allows a noise figure expression to be written as 式 14:

$$NF = 10 \bullet Log\left(1 + \frac{(1+\beta^2)}{\beta^2} + \frac{8}{\alpha\beta^2} + \frac{4}{(\alpha\beta)^2} + \frac{\left(\frac{e_{ni}}{\beta n} \bullet \left(\frac{1}{2} + \frac{1}{\alpha}\right)\right)^2 + \frac{1}{2}\frac{(n \bullet i_n \bullet Rs)^2}{\beta^2}}{kTRs}\right) \quad (14)$$

where

- n ≡ turns ratio (the ohms ratio is then n^2)
- α ≡ differential gain in the FDA = Rf / Rg
- β ≡ transformer insertion loss in V/V (from a dB insertion loss, convert to linear attenuation = β)
- kT = 4e-21J at 290 K (17°C)

One way to use 式 14 is to fix the input balun selection, and then sweep the FDA gain by stepping up the Rf value. The lowest-noise method uses just the two Rg elements for termination matching (no Rm element, such as in 図 8-3) and sweep the Rf values up to assess the resulting input-referred noise figure. While this method can be used with all FDAs and a wide range of input baluns, relatively low-frequency input baluns are an appropriate choice here because the THS4541-Q1 holds exceptional SFDR for less than 40-MHz applications. Two representative selections, with typical measured spans and resulting model elements, are shown in 表 8-2. For these two selections, the critical inputs for the noise figures are the turns ratio and the insertion loss (the 0.2 dB for the CX2014LNL becomes a β = 0.977 in the NF expression).

表 8-2. Example Input Step-Up Baluns and Associated Parameters

PART NUMBER	Rs (Ω)	–1-dB FREQUENCY (MHz)		INSERTION LOSS (dB)	MFR	NO. OF DECADES		–3-dB FREQUENCY (MHz)		TURNS RATIO	MODEL ELEMENTS			
		MIN	MAX			–1-dB POINTS	–3-dB POINTS	MIN	MAX		L1 (µH)	L2 (µH)	k	M (µH)
ADT2-1T	50	0.1	463	0.3	MiniCircuits	3.67	4.22	0.05	825	1.41	79.57747	158.50797	0.99988	112.19064
CX2047LNL	50	0.083	270	0.2	Pulse Eng	3.51	3.93	0.044	372	2	90.42894	361.71578	0.99976	180.81512

Using the typical input referred noise terms for the THS4541-Q1 (e_{ni} = 2.2 nV and i_n = 1.9 pA) and sweeping the total gain from the input of the balun to the differential output over a 10-dB to 24-dB span, gives the input noise figure shown in 図 8-4.

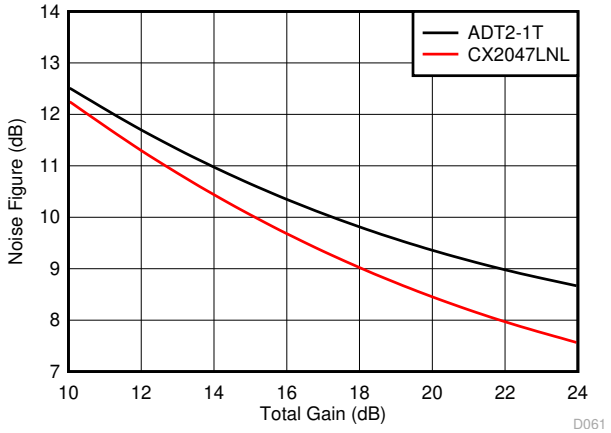


図 8-4. Noise Figure versus Total Gain With the Two Input Baluns of 表 8-2

The 50-Ω referred noise figure estimates show a decreasing input-referred noise for either balun as the gain increases through 24 dB. To achieve the total target gain after the step up from the input balun, the only elements changing in these sweeps are the feedback-resistor values. The example of 図 8-3 is a gain of 7.86 V/V, or a 17.9-dB gain where a 9.0-dB input noise figure is predicted from 図 8-4. Another advantage for this method is that the effective noise gain (NG) is reduced by the source impedance appearing as part of the total Rg element in the design. The example of 図 8-3 operates with a NG = 1 + 402 / (100 + 100) = 3 V/V, giving greater than 300-MHz SSBW in the THS4541-Q1 portion of the design. Combining that capability with the 372 MHz in the balun gives greater than 200 MHz in this 18-dB gain stage; or an equivalent greater than 1.6-GHz gain bandwidth product in a low-power, high dynamic range interface.

Added features and considerations for the balun input of 図 8-3 include:

- Many of these baluns offer a secondary centertap. Leave the centertap unconnected for the best HD2 suppression and dc biasing (do not include a capacitor from this centertap to ground).
- With a floating secondary centertap, the input pins common-mode voltage again equals the output Vocm setting because there is no dc path for the output common-mode voltage to create a common-mode current (I_{CM}).

8.4.2.2 DC-Coupled, Differential-Input to Differential-Output Design Issues

Operating the THS4541-Q1 with a DC-coupled differential input source is very simple and only requires that the input pins stay in range of the DC common-mode operating voltage. One example is a DC-to-50-MHz quadrature down-converter output. These outputs typically sit on a DC level with some internal source impedance to the external loads. The example of 図 8-5 shows a design using the THS4541-Q1 with a simple, passive RLC filter to the inputs (the Rg elements act as the differential termination for the filter design). From the original source behind the internal 250-Ω outputs, this circuit is a gain of 1 to the THS4541-Q1 output pins. The DC common-mode operating voltage level shifts from the 1.2-V internal, to the mixer, to an output at the ADC Vcm voltage of 0.95 V. In this case, a simple average of the two DC voltages in the gain of 1 stage gives a 1.08-V input pin common-mode result that is well within range.

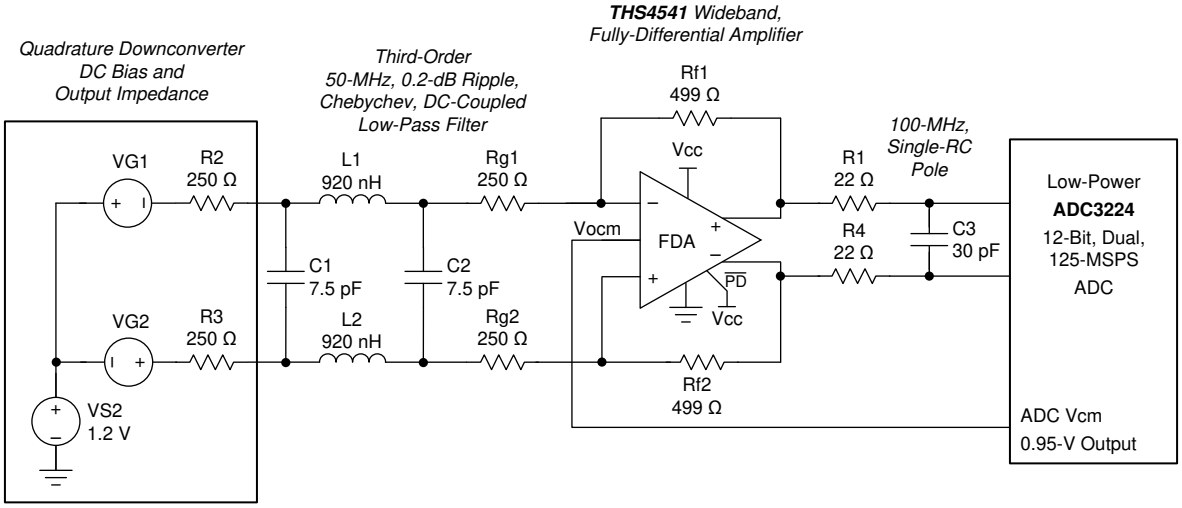


図 8-5. Example DC-Coupled, Differential I/O Design from a Quadrature Mixer to an ADC

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The THS4541-Q1 is effective over a broad range of applications. Two examples are developed here. First, an attenuator stage that directly receives a higher input signal voltage and translates the voltage to a lower differential swing on a fixed common-mode is shown. This design requires some attention to frequency-response flatness issues, and one approach to managing these issues is shown. The second example is a gain of 2 V/V, matched input of 50 Ω to an output set to 0.95 V common-mode followed by a third-order Bessel filter with approximately 20 MHz of bandwidth feeding into the ADC34J22, a low-power, 12-bit, quad 50-MSPS JESD 204B ADC.

9.2 Typical Applications

9.2.1 Designing Attenuators

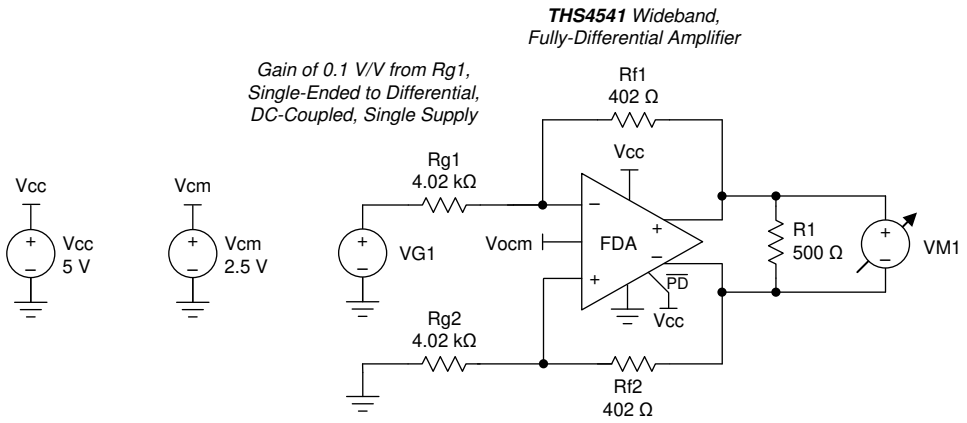


図 9-1. Divide-by-10 Attenuator Application for the THS4541-Q1

9.2.1.1 Design Requirements

In this design, the aim is to:

1. Present a 4-kΩ input impedance to a ±40-V input signal (maximum ±10 mA from the prior stage).
2. Attenuate that swing by a factor 1/10 (–20 dB) to a differential output swing.
3. Place that swing on a 2.5-V common-mode voltage at the THS4541-Q1 outputs.
4. Operate on a single +5-V supply and ground.
5. Tune the frequency response to a flat Butterworth response with external capacitors.

9.2.1.2 Detailed Design Procedure

Operating the THS4541-Q1 at a low dc noise gain, or with higher feedback resistors, can cause a lower phase margin to exist, giving the response peaking shown in 図 6-1 for the gain of 0.1 (a 1/10 attenuator) condition. Although operating the THS4541-Q1 as an attenuator (taking a large input range to a purely differential signal around a controlled-output, common-mode voltage) is often useful, the response peaking illustrated in 図 6-1 is usually undesirable. Several methods can be used to reduce or eliminate this peaking; usually, at the cost of higher output noise. Using dc techniques always increases the output noise broadband, while using an ac noise-gain-shaping technique peaks the noise, but only at higher frequencies that can then be filtered off with the

typical passive filters often used after this stage. 図 9-1 shows a simplified schematic for the gain of 0.1 V/V test from 図 7-1.

This configuration shows a nominal 18° phase margin (from 表 7-2); therefore, a very highly-peaked response is illustrated in 図 6-1. This peaking can be eliminated by placing two feedback capacitors across the Rf elements and a differential input capacitor. Adding these capacitors provides a transition from a resistively set noise gain (NG1 here; 1.1 in 表 7-2) to a capacitive divider at high-frequency flattening out to a higher noise gain (NG2 here). The key for this approach is to target a Zo, where the noise gain begins to peak up. Using only the following terms, and targeting a closed-loop flat (Butterworth) response, gives this solution sequence for Zo and then the capacitor values.

1. Gain bandwidth product in Hz (850 MHz for the THS4541-Q1)
2. Low frequency noise gain, NG1 (= 1.1 in the attenuator gain of 0.1 V/V design)
3. Target high-frequency noise gain selected to be higher than NG1 (NG2 = 3.1 V/V is selected for this design)
4. Feedback resistor value, Rf (assumed balanced for this differential design = 402 Ω for this design example)

From these elements, for any decompensated voltage-feedback op amp or FDA, solve for Zo (in Hz) using 式 15:

$$Zo = \frac{GBP}{NG1^2}\left(1 - \frac{NG1}{NG2} - \sqrt{1 - 2\frac{NG1}{NG2}}\right) \tag{15}$$

From this target zero frequency in the noise gain, solve for the feedback capacitors using 式 16:

$$Cf = \frac{1}{2\pi \bullet Rf \bullet Zo \bullet NG2} \tag{16}$$

The next step is to resolve the input capacitance on the summing junction. 式 17 is for a single-ended op amp (for example, OPA847) where that capacitor goes to ground. To use 式 17 for a voltage-feedback FDA, cut the target value in half, and place the result across the two inputs (reducing the external value by the specified internal differential capacitance).

$$Cs = (NG2 - 1)Cf \tag{17}$$

Setting the external compensation elements using 式 15 to 式 17 allows an estimate of the resulting flat bandwidth f_{-3dB} frequency, as shown in 式 18:

$$f_{-3dB} \approx \sqrt{GBP \bullet Zo} \tag{18}$$

Running through these steps for the THS4541-Q1 in the attenuator circuit of 図 9-1 gives the proposed compensation of 図 9-2 where 式 18 estimates a bandwidth of 252 MHz (Zo target is 74.7 MHz).

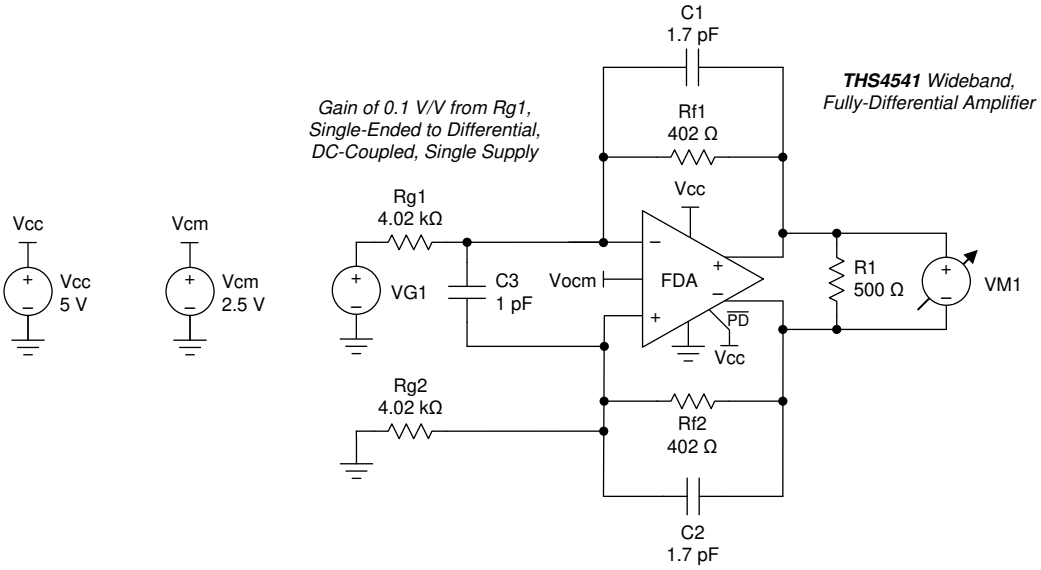


図 9-2. Compensated Attenuator Circuit Using the THS4541-Q1

The 1 pF across the inputs is really a total 1.85 pF, including the internal differential capacitance, and a Cs = 3.7 pF for a single-ended design from 式 17.

These two designs (with and without the capacitors) were both bench tested and simulated using the THS4541 TINA model giving the results of 図 9-3.

This method does a good job of flattening the response for what starts out as a low phase-margin attenuator application. The simulation model does a very good job of predicting the peaking and showing the same improvement with the external capacitors; both giving a flat, approximately 250-MHz, closed-loop bandwidth for this gain of a 0.1-V/V design. In this example, the output noise begins to peak up (as a result of the noise-gain shaping of the capacitors) above 70 MHz. Use postfiltering to minimize any increase in the integrated noise using this technique. Using this solution to deliver an 8-V_{PP} differential output to a successive approximation register (SAR) ADC (using the 2.5-V Vocm shown), the circuit accepts up to ±40-V inputs, where the 4-kΩ input Rg1 draws ±10 mA from the source.

9.2.1.3 Application Curve

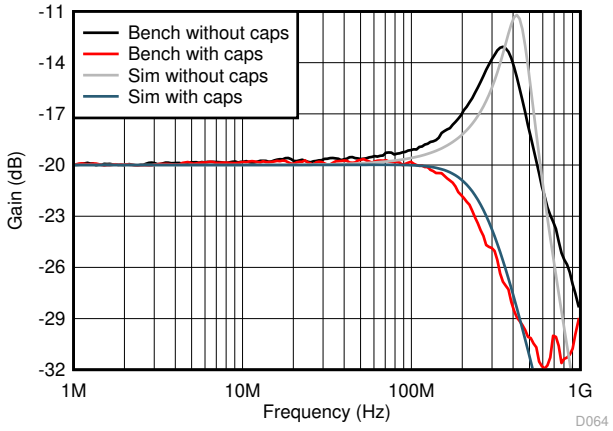


図 9-3. Attenuator Response Shapes with and without External Compensation

9.2.2 Interfacing to High-Performance ADCs

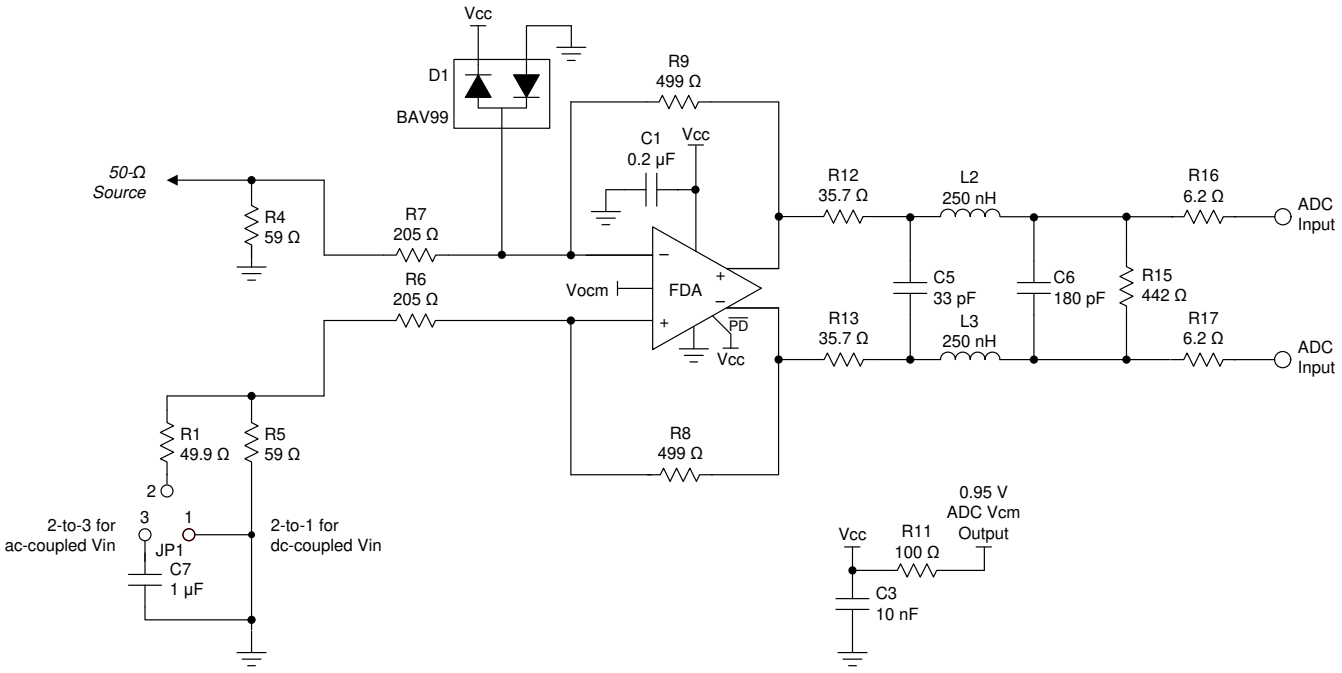


図 9-4. DC-Coupled, Bipolar Input Gain of 2 V/V Single-Ended to Differential Interface to ADC

9.2.2.1 Design Requirements

In this example design, an impedance matched input assuming a 50-Ω source is implemented with a DC-coupled gain of 2 V/V to the ADC. This configuration effectively reduces the required full-scale input to ±0.5 V for a 2-V_{PP} full-scale input ADC. Add a low insertion-loss interstage filter to the ADC to control the broadband noise where the goal is to show minimal SNR reduction in the FFT, as well as minimal degradation in SFDR performance.

9.2.2.2 Detailed Design Procedure

The THS4541-Q1 provides a very flexible element for interfacing from a variety of sources to a wide range of ADCs. Because all precision and high-speed ADCs require a differential input on a common-mode voltage, this design is the primary application for the THS4541-Q1.

The THS4541-Q1 provides a simple interface to a wide variety of precision SAR, ΔΣ, or higher-speed pipeline ADCs. To deliver the exceptional distortion at the output pins, considerably wider bandwidth than typically required in the signal path to the ADC inputs is provided by the THS4541-Q1. For instance, the gain of 2 single-ended to differential design example provides approximately a 500-MHz, small-signal bandwidth. Even if the source signal is Nyquist bandlimited, this broad bandwidth can possibly integrate enough THS4541-Q1 noise to degrade the SNR through the ADC if the broadband noise is not bandlimited between the amplifier and ADC.

図 9-4 shows an example DC-coupled, gain of 2 interface with a controlled, interstage-bandwidth filter implemented on the demonstration board for the JESD digital-output interface, ADC34J22 (a 50-MSPS, quad, 12-bit ADC). This board is called the DEV-ADC34J22 ADC HSMC MODULE with complete documentation at http://dallaslogic.com/prod_dev-adc34j/.

Designed for a DC-coupled 50Ω input match, this design starts with a 499-Ω feedback resistor, and provides a gain of 2.35V/V to the THS4541-Q1 output pins. The third-order interstage, low-pass filter provides a 20-MHz Bessel response with a 0.85 V/V insertion loss to the ADC, providing a net gain of 2 V/V from board edge to the ADC inputs. Although the THS4541-Q1 can absorb overdrives, an external protection element is added using the BAV99 low-capacitance device, shown in 図 9-4. For DC-coupled testing, pins 1 and 2 are jumpered together. When the source is an AC-coupled, 50-Ω source, pins 2 and 3 are jumpered to maintain differential

balance. FFT testing normally uses a bandpass filter into the board; an AC-coupled source. A typical 5-MHz, full-scale, single-tone FFT is shown in 図 9-5, where the jumper is placed from pins 2 to 3. The reported SNR of 70.09 dBFs is only a slight reduction from the tested ADC-only performance of 70.42 dBFs, showing the value of the interstage noise bandwidth limiting filter. The exceptionally low harmonic distortion for the THS4541-Q1 also shows up in the very low SFDR and THD shown in 図 9-5. This 96-dB SFDR and 92.83-dB THD are comparable to the ADC-only test results.

9.2.2.3 Application Curve

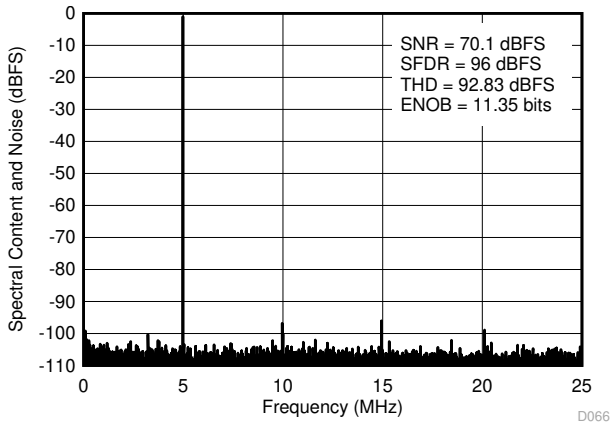


図 9-5. 5-MHz FFT, 50-MSPS Test for the Gain of 2 Interface in Figure 10-4

9.3 Power Supply Recommendations

The THS4541-Q1 is principally intended to operate with a nominal single-supply voltage of 3 V to 5 V. Supply-voltage tolerances are supported with the specified operating range of 2.7 V (10% low on a 3-V nominal supply) and 5.4 V (8% high on a 5-V nominal supply). Supply decoupling is required, as described in the *セクション 8.1.1* section. Split (or bipolar) supplies can be used with the THS4541-Q1, as long as the total value across the device remains less than 5.5 V (absolute maximum). The thermal pad on the package is electrically isolated; connect the thermal pad to any power or ground plane for heat spreading.

Using a negative supply to deliver a true swing to ground output in driving SAR ADCs can be desired. While the THS4541-Q1 features a rail-to-rail output, linear operation requires approximately a 200-mV headroom to the supply rails. One easy option for extending the linear output swing to ground is to provide the small negative supply voltage required using the LM7705 fixed –230-mV, negative-supply generator. This low-cost, fixed negative-supply generator accepts the 3-V to 5-V positive supply input used by the THS4541-Q1 and provides a –230-mV supply for the negative rail. Using the LM7705 provides an effective resolution, as described in the *Extending Rail-to-Rail Output Range for Fully Differential Amplifiers to Include True Zero Volts* reference guide.

9.4 Layout

9.4.1 Layout Guidelines

Similar to all high-speed devices, the best system performance is achieved with a close attention to board layout. The THS4541-Q1 evaluation module (EVM) shows a good example of high-frequency layout techniques as a reference. This EVM includes numerous extra elements and features for characterization purposes. General high-speed, signal-path layout suggestions include:

- Continuous ground planes are preferred for signal routing with matched impedance traces for longer runs; however, open up both ground and power planes around the capacitive sensitive input and output device pins. After the signal is sent into a resistor, parasitic capacitance becomes more of a bandlimiting issue and less of a stability issue.
- Use good, high-frequency decoupling capacitors (0.1 µF) on the ground plane at the device power pins. Higher value capacitors (2.2 µF) are required, but can be placed further from the device power pins and

shared among devices. For best high-frequency decoupling, consider X2Y supply-decoupling capacitors that offer a much higher self-resonance frequency over standard capacitors.

- When using differential signal routing over any appreciable distance, use microstrip layout techniques with matched impedance traces.
- Higher-speed FDAs, such as the THS4541-Q1, include a duplicate of the output pins on the input feedback side of the package. This duplication is intended to allow the external feedback resistors to be connected with virtually no trace length on the input side of the package. Use this layout approach with no extra trace length on this critical feedback path.
- The input summing junctions are very sensitive to parasitic capacitance. Connect any Rg elements into the summing junction with minimal trace length to the device pin side of the resistor. The other side of the Rg elements can have more trace length if needed to the source or to ground.

9.4.2 Layout Example

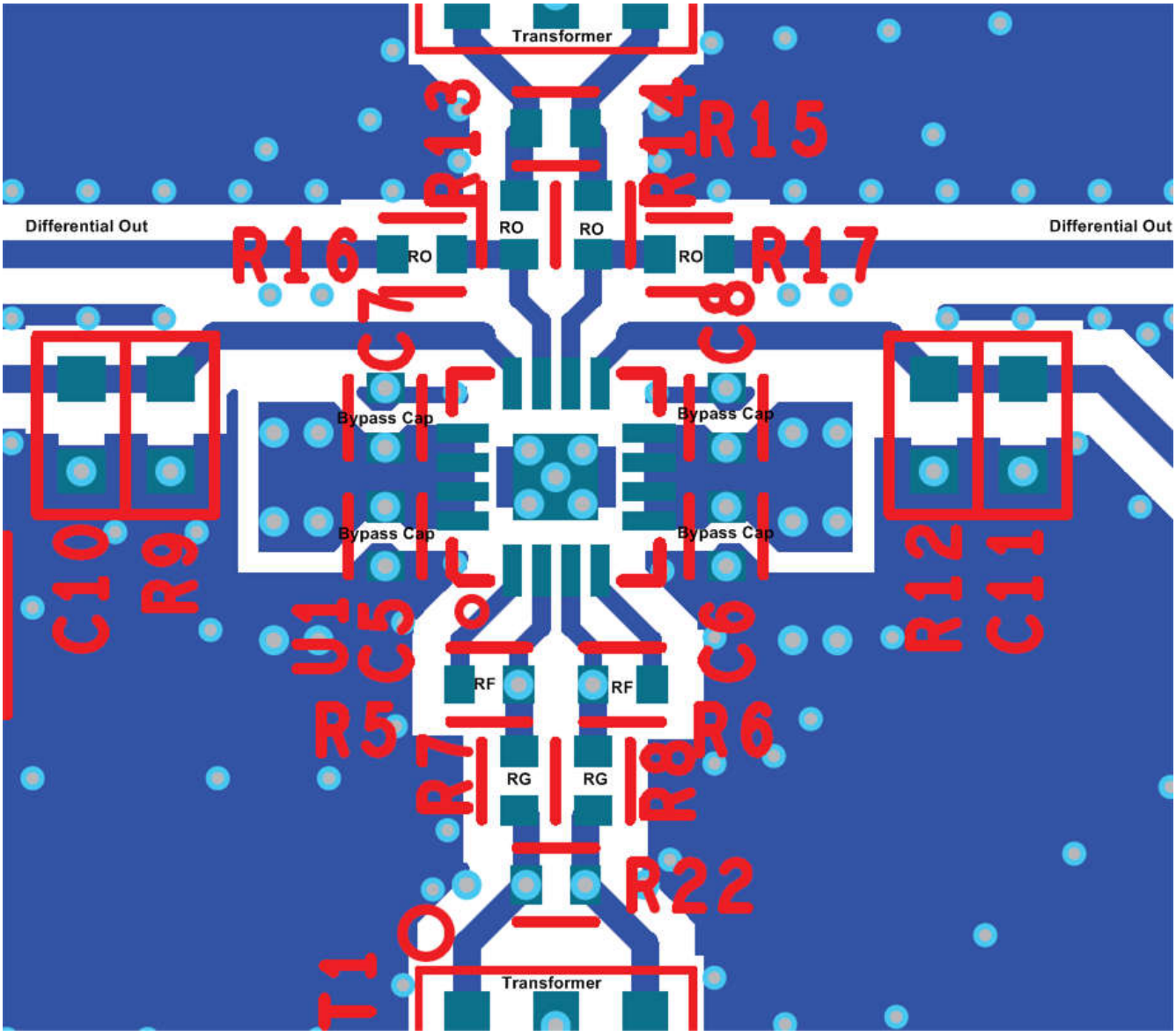


図 9-6. Layout Example

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

10.1.1.1 TINA Simulation Model Features

The device model is available as part of the TINA model library. The model includes numerous features intended to speed designer progress over a wide range of application requirements. The following list shows the performance parameters included in the model:

- For the small-signal response shape with any external circuit:
  - Differential open loop gain and phase
  - Parasitic input capacitance
  - Open-loop differential output impedance
- For noise simulations:
  - Input differential spot voltage noise and a 100-kHz 1/f corner
  - Input current noise on each input with a 1-MHz 1/f corner
- For time-domain, step-response simulations:
  - Differential slew rate
  - I/O headroom models to predict clipping
  - Fine-scale, DC precision terms:
    - PSRR
    - CMRR

The typical characterization curves show more detail than the macromodels can provide; some of those unmodeled features include:

- Harmonic distortion
- Temperature drift in DC error terms (V_{IO} and I_{OS})

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *ADC34J2x Quad-Channel, 12-Bit, 50-MSPS to 160-MSPS, Analog-to-Digital Converter with JESD204B Interface* data sheet
- Texas Instruments, *Design for a Wideband, Differential Transimpedance DAC Output* application report
- Texas Instruments, *Extending Rail-to-Rail Output Range for Fully Differential Amplifiers to Include True Zero Volts* reference guide
- Texas Instruments, *LM7705 Low-Noise Negative Bias Generator* data sheet
- Texas Instruments, *LMH6554 2.8-GHz Ultra Linear Fully Differential Amplifier* data sheet
- Texas Instruments, *THS4541RGT EVM* user guide
- Texas Instruments, *Maximizing the dynamic range of analog front ends having a transimpedance amplifier* technical brief

10.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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10.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (November 2019) to Revision C (October 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• Deleted input bias current minimum values from *Electrical Characteristics: (Vs+) – Vs– = 5 V*	5
• Deleted input bias current minimum values from *Electrical Characteristics: (Vs+) – Vs– = 3 V*	8

Changes from Revision A (November 2015) to Revision B (November 2019)	Page
• AEC-Q100 固有の「特長」項目を変更	1
• 「アプリケーション」セクションを変更	1
• ウェッタブル フランク パッケージ (THS4541W-Q1) の情報をドキュメントに追加	1

Changes from Revision * (November 2015) to Revision A (November 2015)	Page
• デバイスのステータスを「製品プレビュー」から「量産データ」へ変更	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS4541QRGTRQ1	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4541Q1
THS4541QRGTRQ1.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4541Q1
THS4541QWRGTRQ1	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	4541W
THS4541QWRGTRQ1.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	4541W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF THS4541-Q1 :

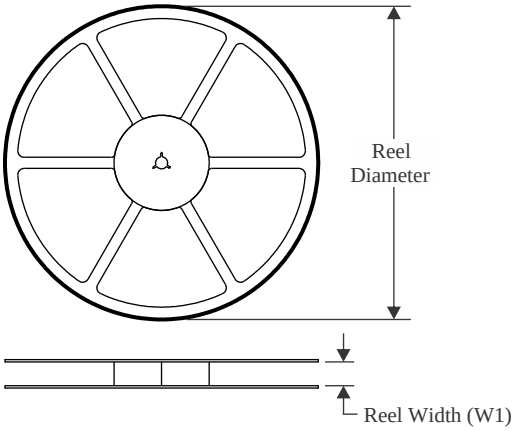
- Catalog : THS4541

NOTE: Qualified Version Definitions:

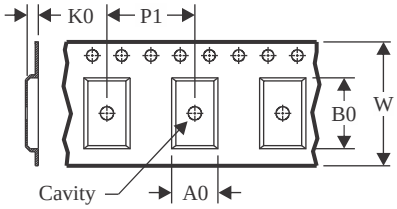
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

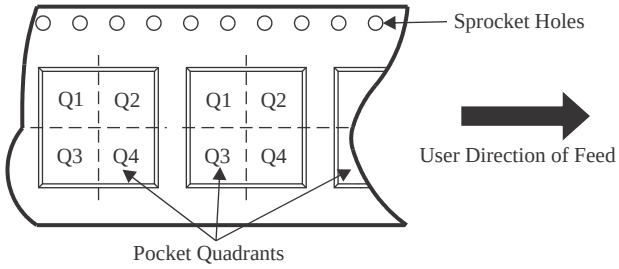


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

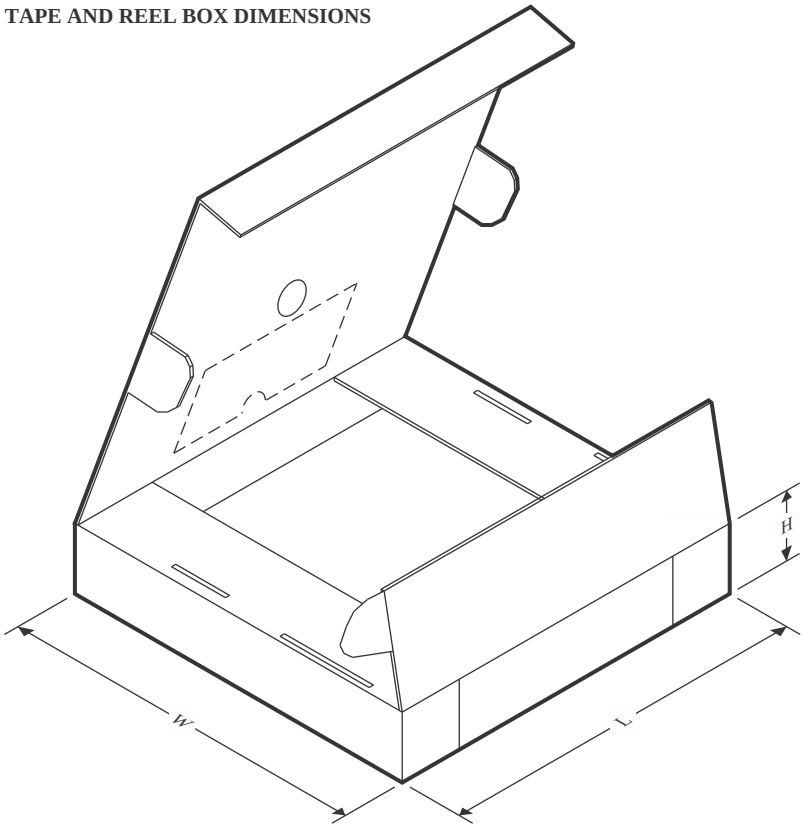
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4541QRGTRQ1	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THS4541QWRGTRQ1	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

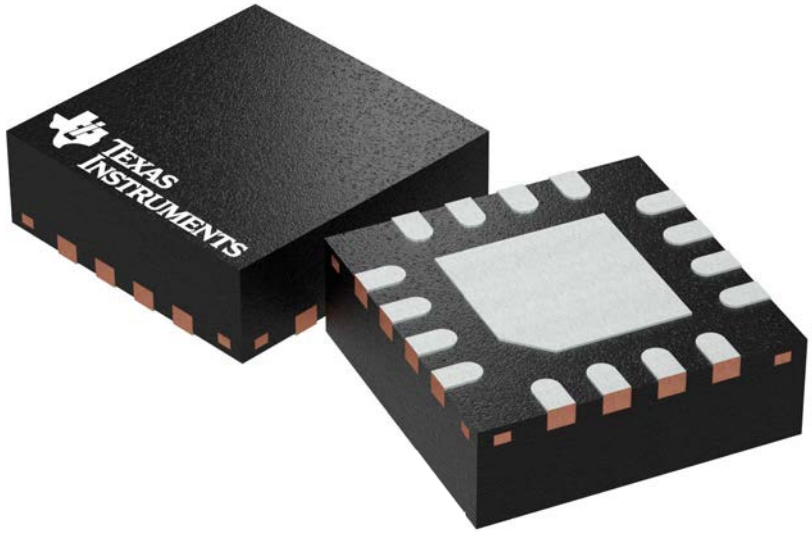


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4541QRGTRQ1	VQFN	RGT	16	3000	346.0	346.0	33.0
THS4541QWRGTRQ1	VQFN	RGT	16	3000	367.0	367.0	38.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



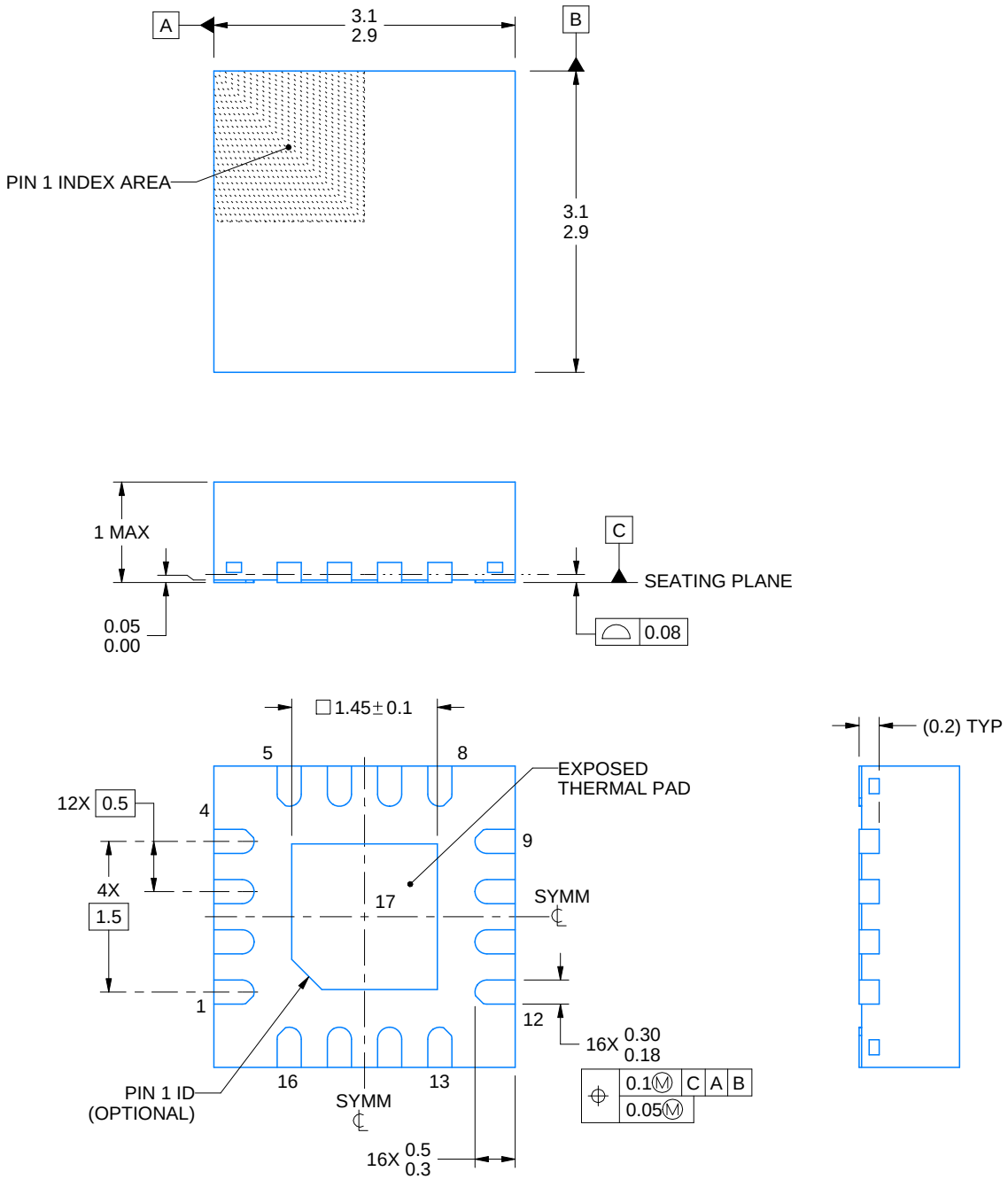
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT0016A

PACKAGE OUTLINE

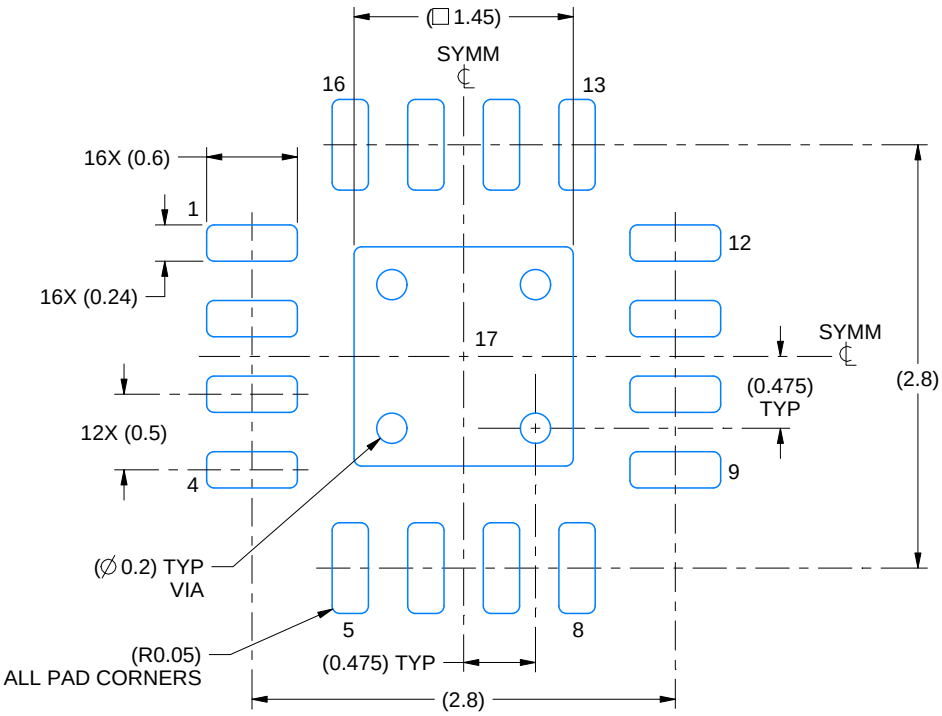
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

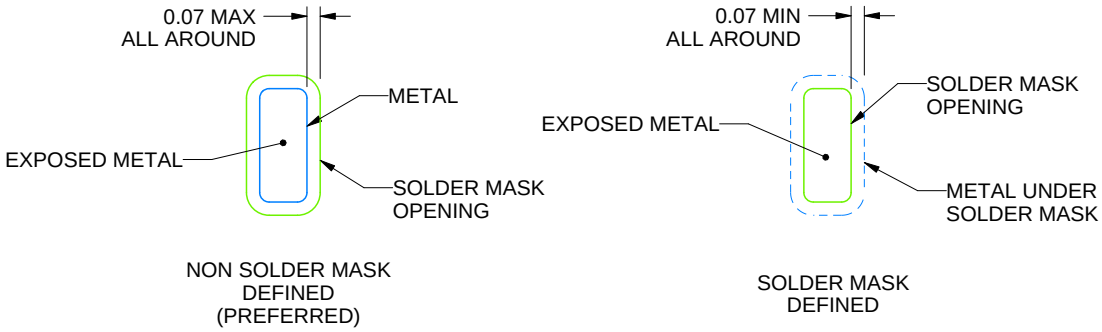


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

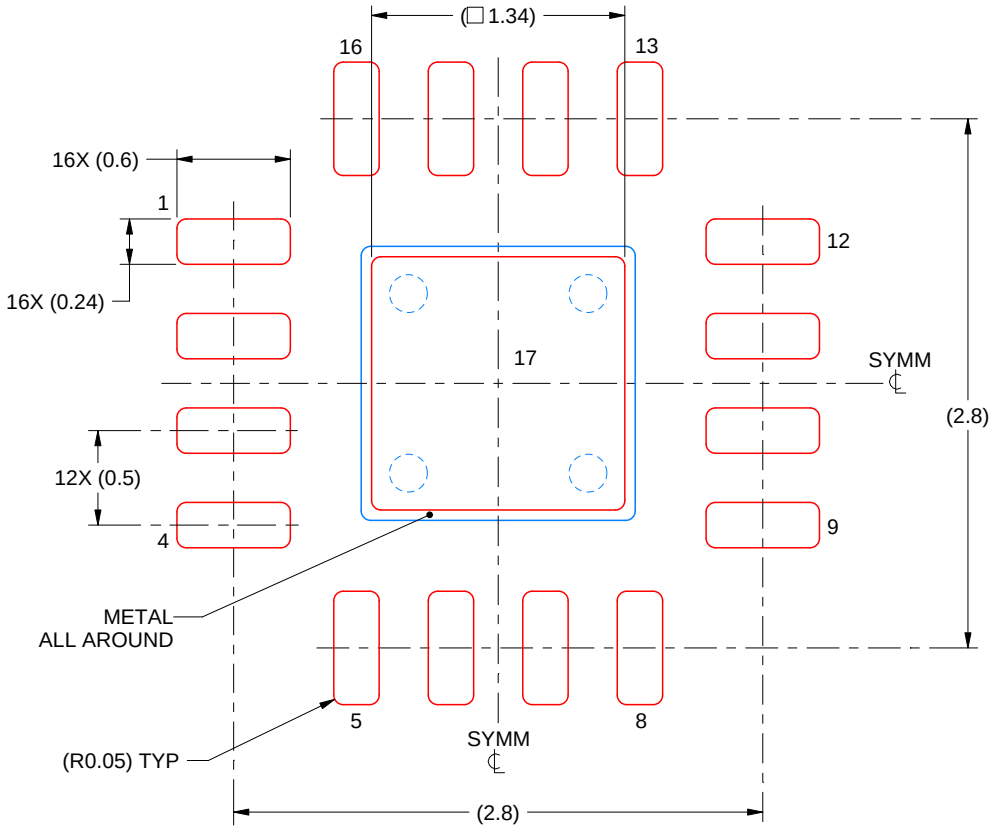


SOLDER MASK DETAILS

4219032/A 02/2017

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219032/A 02/2017

NOTES: (continued)

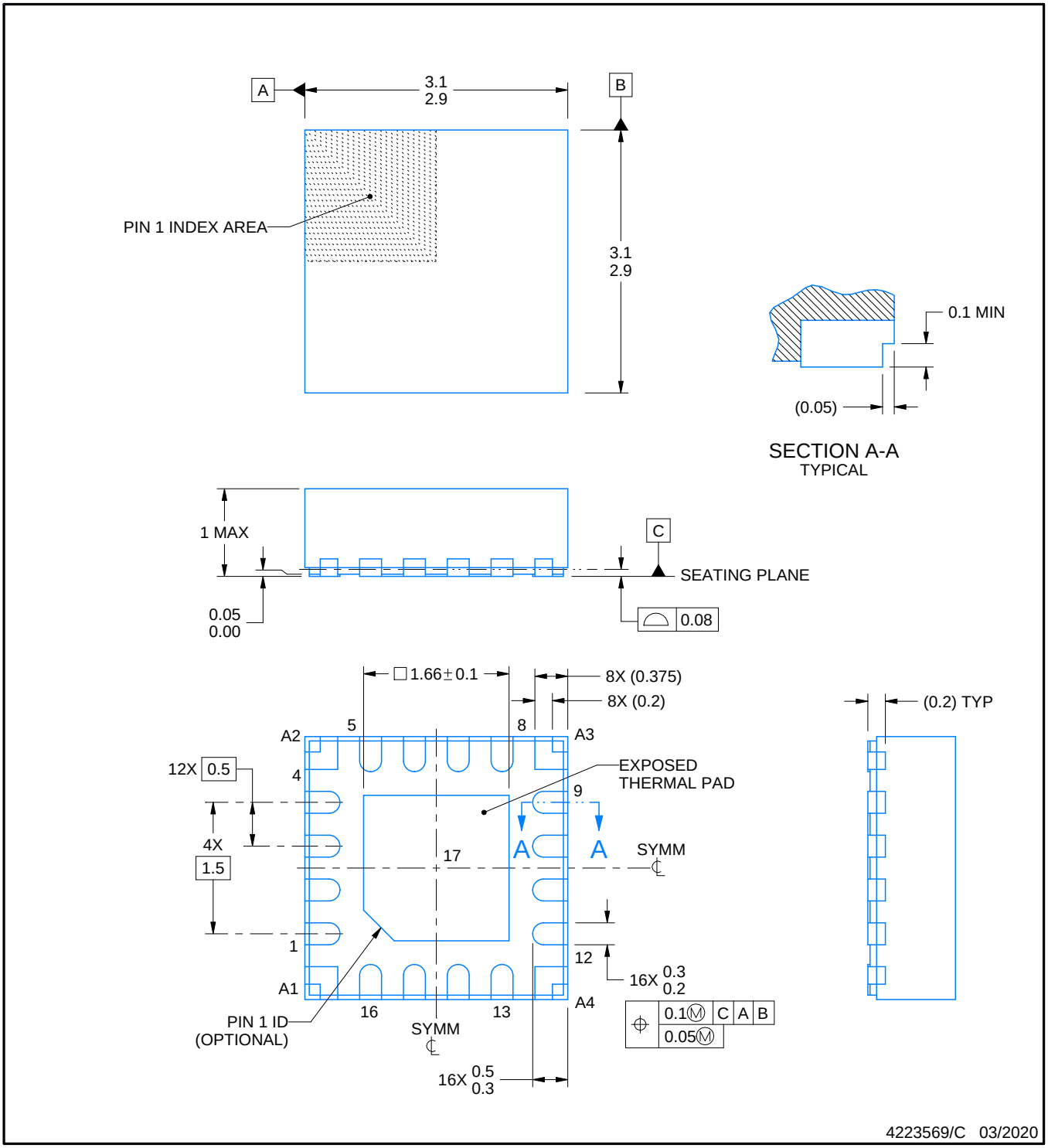
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RGT0016H

PACKAGE OUTLINE

VQFN - 1 mm max height

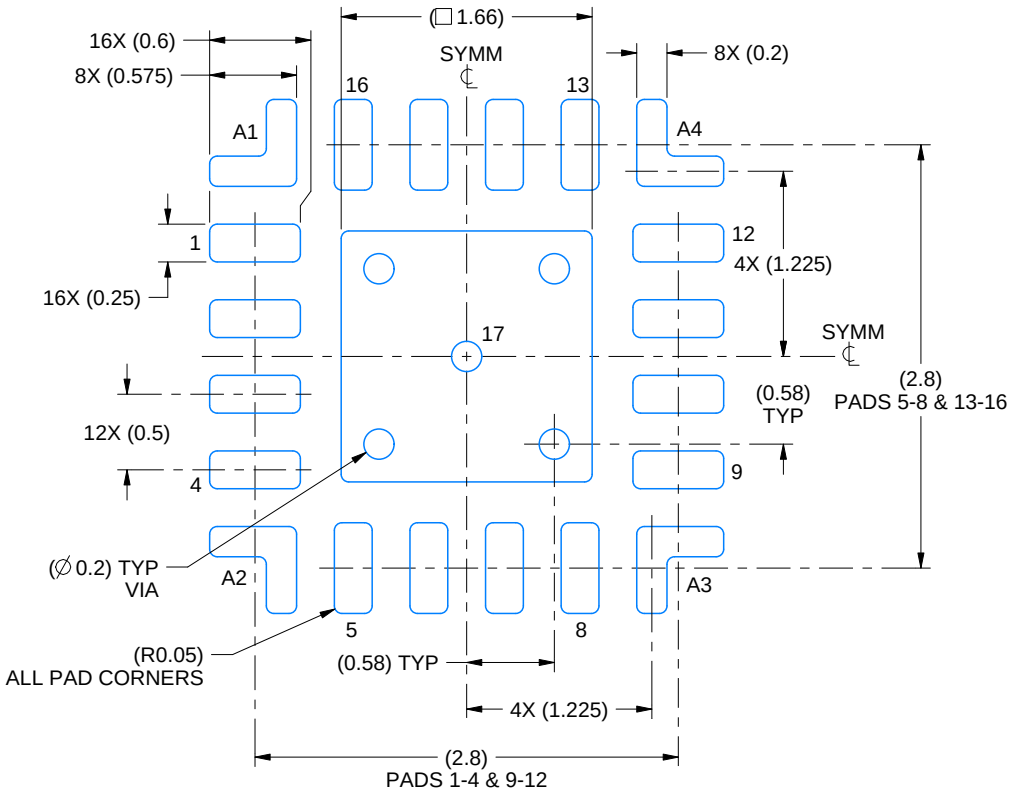
PLASTIC QUAD FLATPACK - NO LEAD



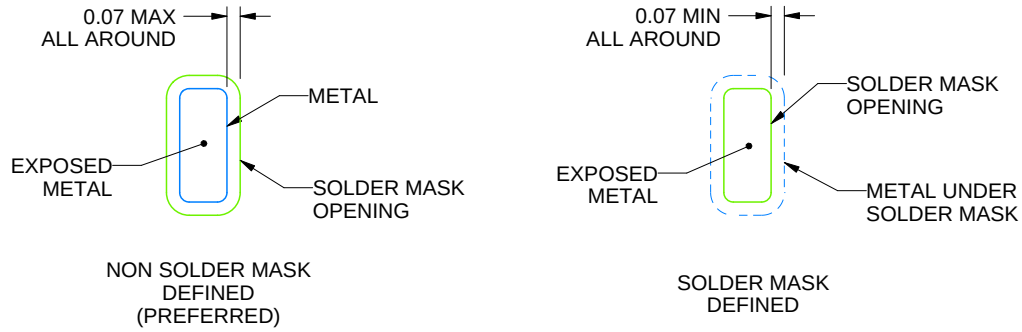
4223569/C 03/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

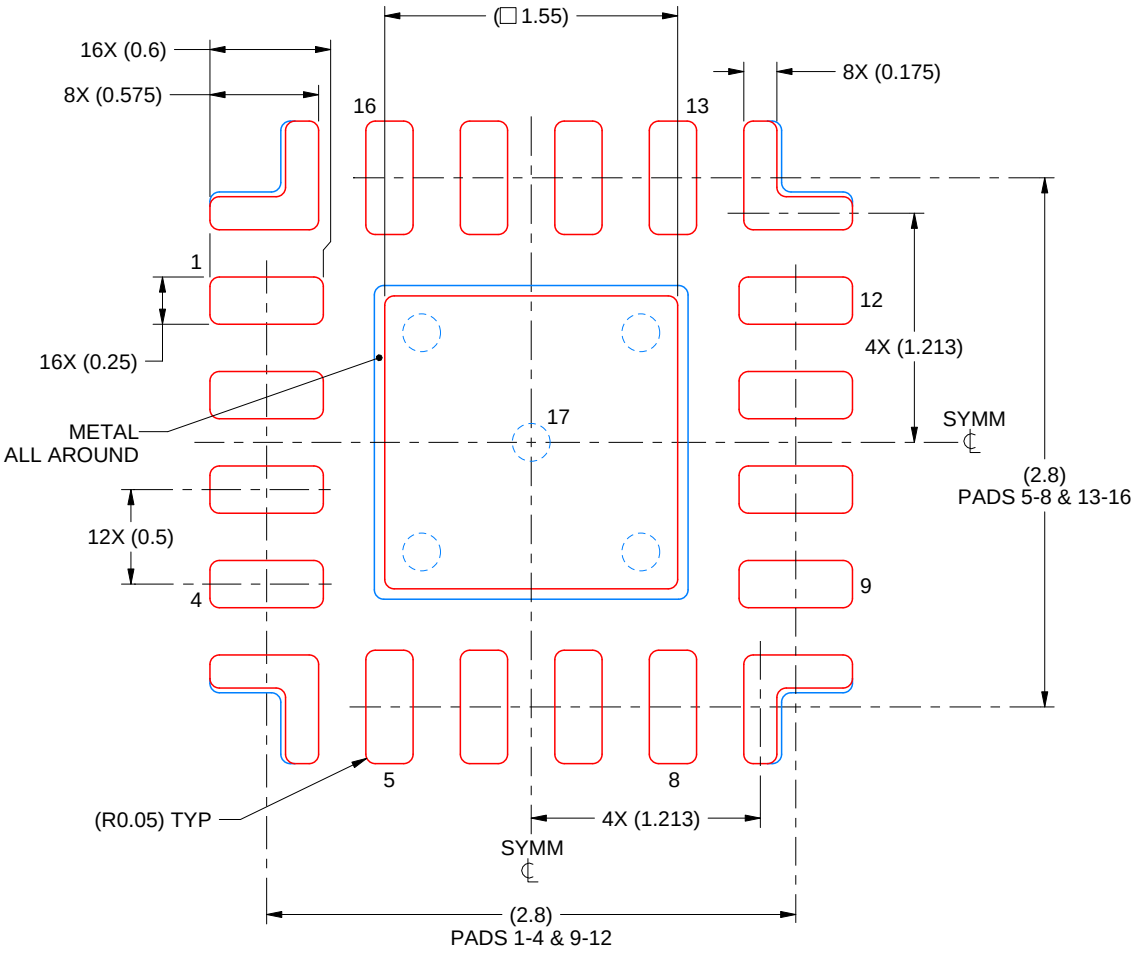


SOLDER MASK DETAILS

4223569/C 03/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
THERMAL PAD 17: 87% - PADS A1, A2, A3, & A4: 89%
SCALE:25X

4223569/C 03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月